A Brief Summary of the MSP430

The “classic” (though not original) Forth processor was the Digital Equipment Corporation PDP-11. Its 16-bit ALU, eight general-purpose registers, and eight amazingly flexible addressing modes were perfectly suited to writing a Forth interpreter.

Today, the Texas Instruments MSP430 microprocessor has an architecture remarkably similar to the PDP-11. It has sixteen 16-bit general-purpose registers, including the Program Counter (PC) and Stack Pointer (SP). The instruction set is completely orthogonal: any instruction, and any addressing mode, may be used with any register.

There are four source addressing modes, and two destination addressing modes, as illustrated in Figure 1.2. Using Indexed mode with the PC register (R0) gives PC-relative addressing. Using Autoincrement mode with the PC register gives immediate addressing (the data follows the instruction).

Two of the registers, R2 and R3, are "constant generators," called CG1 and CG2, for fast generation of six common constants (0, -1, +1, +2, +4, +8). Each Constant Generator register can produce four different values when used as a source operand, depending on addressing mode.

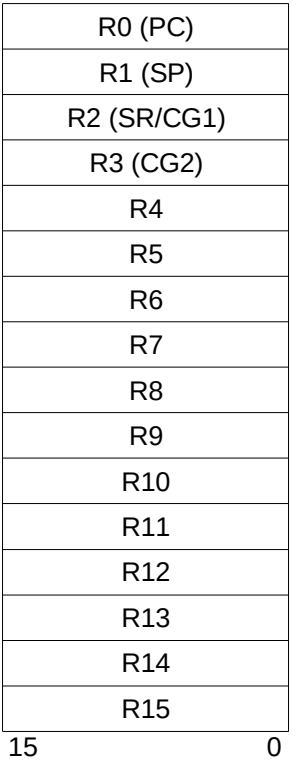

Figure 1.1: MSP430 Registers

Mode	Source Syntax	Destination Syntax	R2 value	R3 value
Register (direct)	Rn	Rn	SR	0
Indexed	X(Rn)	X(Rn)	Abs.	+1
Indirect	@Rn	not available	+4	+2
Autoincrement	@Rn+	not available	+8	-1

Figure 1.2: MSP430 Addressing Modes

Using Indexed mode with R2 (Constant Generator 1), as either source or destination, gives Absolute addressing. In this mode the effective address is simply the index X. Using direct mode, known as "register" mode on the MSP430, R2 accesses the Status Register SR.

There are only 27 instructions in the MSP430, most of which should be familiar to an assembly-language programmer. BIC is "bit clear," and BIS is "bit set" (logical OR).[4] DADD is decimal add with carry; SWPB is "swap bytes"; SXT is "sign extend into high byte." The arithmetic and logical instructions can operate on 16-bit words or 8-bit bytes (with the .B suffix). Memory is byte-addressable and little-endian; word operations must use even addresses.

MOV(.B) src,dst	BIT(.B) src,dst	RETI
ADD(.B) src,dst	BIC(.B) src,dst	JMP label
ADDC(.B) src,dst	BIS(.B) src,dst	JEQ/JZ label
SUB(.B) src,dst	PUSH(.B) src	JNE/JNZ label
SUBC(.B) src,dst	RRC(.B) dst	JC/JHS label
CMP(.B) src,dst	RRA(.B) dst	JNC/JLO label
DADD(.B) src,dst	SWPB dst	JN label
AND(.B) src,dst	SXT dst	JGE label
XOR(.B) src,dst	CALL dst	JLT label

Figure 1.3: MSP430 Instruction Set

One might think there are several operations missing from this set, such as Rotate Left and Return from Subroutine. Those operations can actually be performed with the basic instructions. For example,

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INC dst     becomes     ADD #1,dst
NOP         becomes     MOV #0,R3
POP dst     becomes     MOV @SP+,dst
RET         becomes     MOV @SP+,PC
RLC dst     becomes     ADDC dst,dst
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Few processors can be so completely described in just two pages of text. Yet the MSP430 is sufficiently powerful that many Forth primitives can be implemented in one or two machine instructions. It is ideally suited to illustrate the implementation of a Forth kernel.

4 PDP-11 fans will recognize BIC and BIS from the PDP-11 instruction set.