Breaking the 64K Limit

Handling Extended Memory in Forth
(a historical overview)

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When olden chips
had sixteen bits
and sixty—four K ceilings

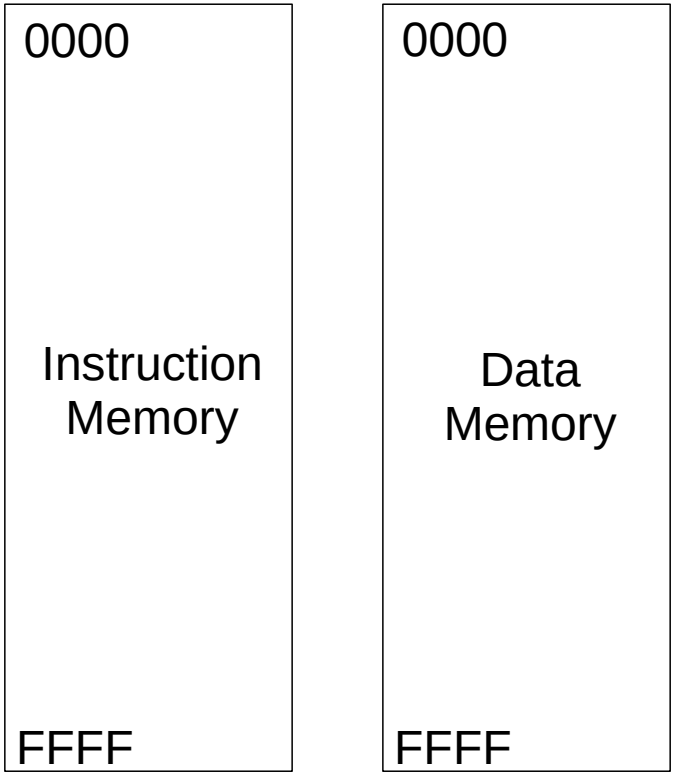
These odd designs
gave address lines
and some are still appealing

0. Use a 32-bit CPU

- 32-bit CPUs are cheap and plentiful
- All extended memory schemes violate ANS
  - Single, linear address space
  - Address size < cell size

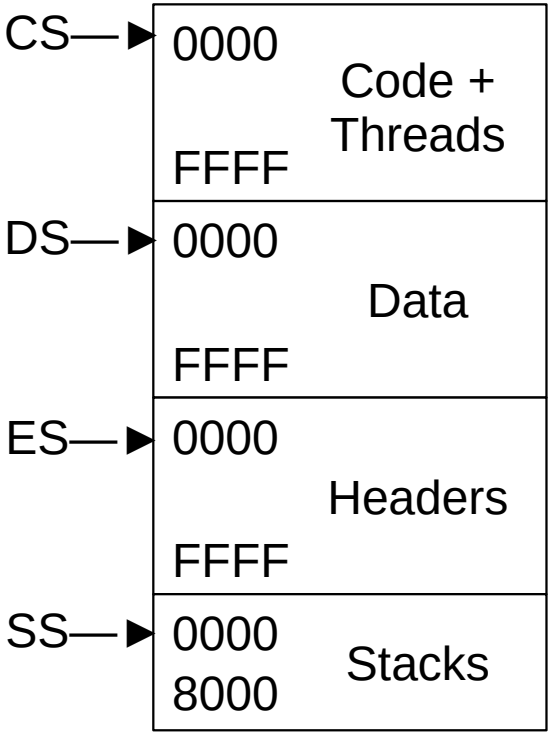
1. Split Instruction/Data memory

- Examples: Z8, 8051
- Mods similar to RAM/ROM systems
- Adds I@, I!, IDP, etc.
- Not ANS



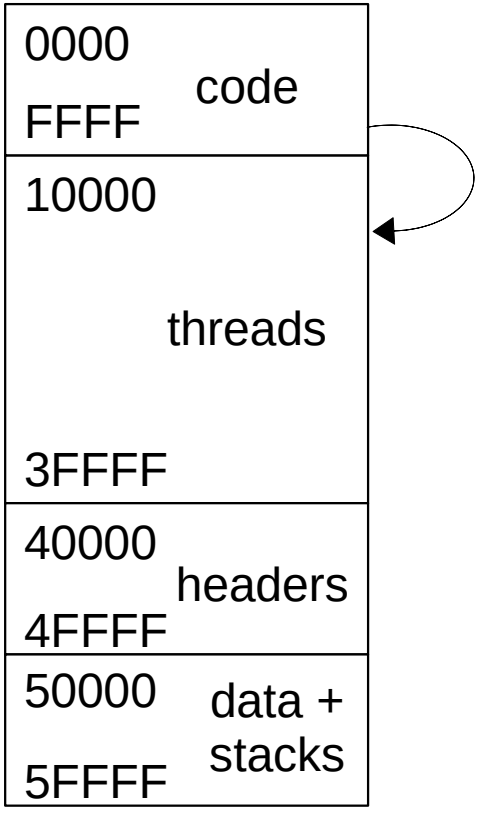
2. Segmented Memory

- Example: 8086
- Code, Data, Stacks, Threads, Headers
- More operators! H@, H!, HC@, etc.
- Separate stacks/data?

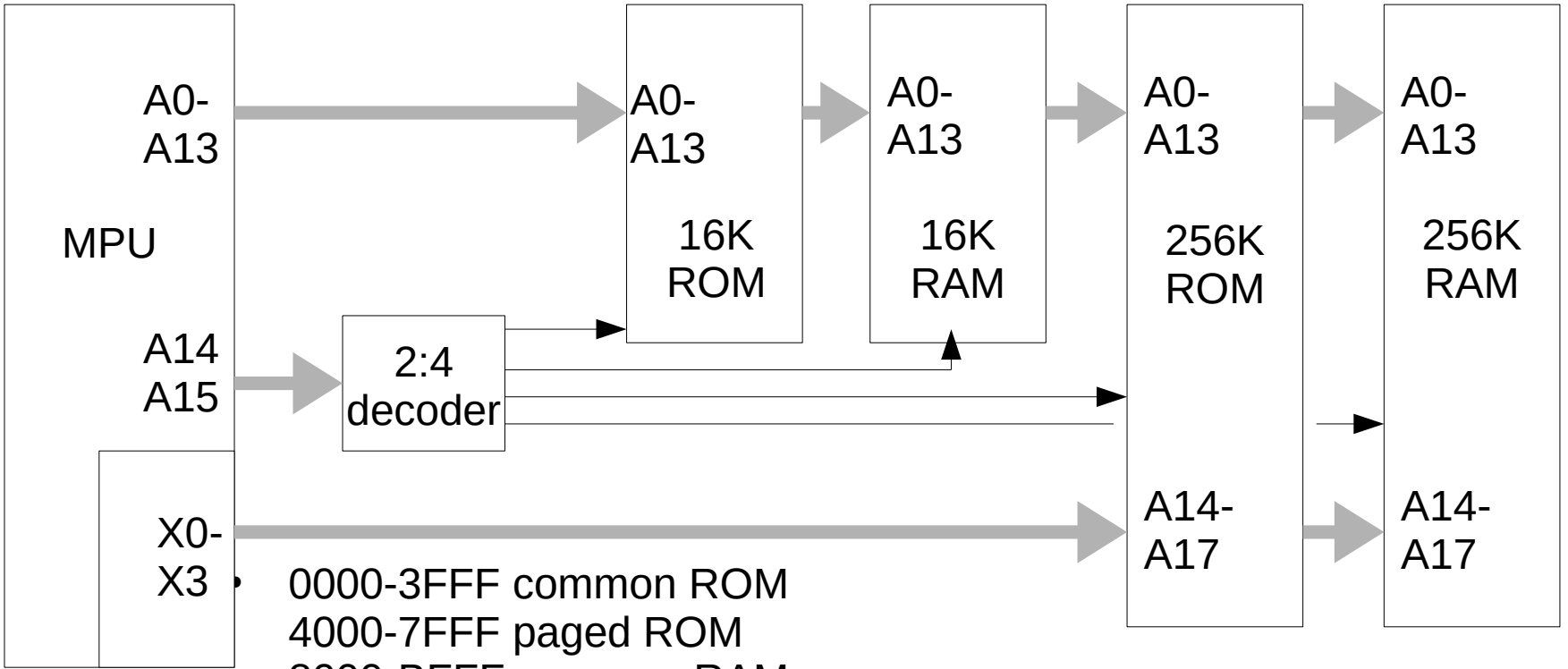


3. Segmented with long IP

- Example: 56800E, MSP430X
  (24/20 bit address registers)
- Simulate segments with
  high address bits
- All XTs in Code space
  (with pointers to threads)
- Return address is two cells



4. Conventional Paging



4. Conventional Paging

- Example: MC9S12, 65C816
  (PPAGE, RPAGE, EPAGE) (DBR, PBR)
- Can use I/O port
- Interpage “Long Call” & return

LCALL	page	word address

- Requires compiler mod
- L@, L! etc. For data. Needs LEXECUTE

5. “Page Prefix” words

- Example: H8S
- Prefix word $0180, 2, 4...

$018n	word address

- 64K pages
- Long call out of page zero, vs. when page changes

```
        .ORG 0180h
        JR DOPREFIX
        JR DOPREFIX
            ...
DOPREFIX:
; R3 = W = $018n
        MOV.W  R3,E3
        SHLR.W E3
        AND.W  #7,E3
; ER5 is IP
        MOV.W  @ER5+,R3
        JMP    @ER3
```

Applications

- 56800E, H8S – obsolete?
- MSP430X, 9S12 – current
- 6502, 65C816? – historical

Questions?

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