UNIVERSITA' DI PISA
Laurea Magistrale in Ingegneria Elettronica

VHDL Design and FPGA Prototyping of a Dynamic Acquisition Window in the Digital Pulse Processing of the Streaming Readout of Nuclear Physics Experiments

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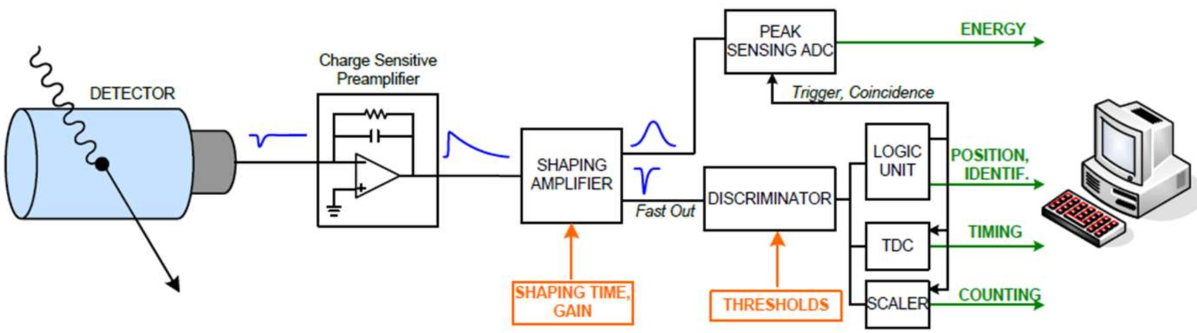
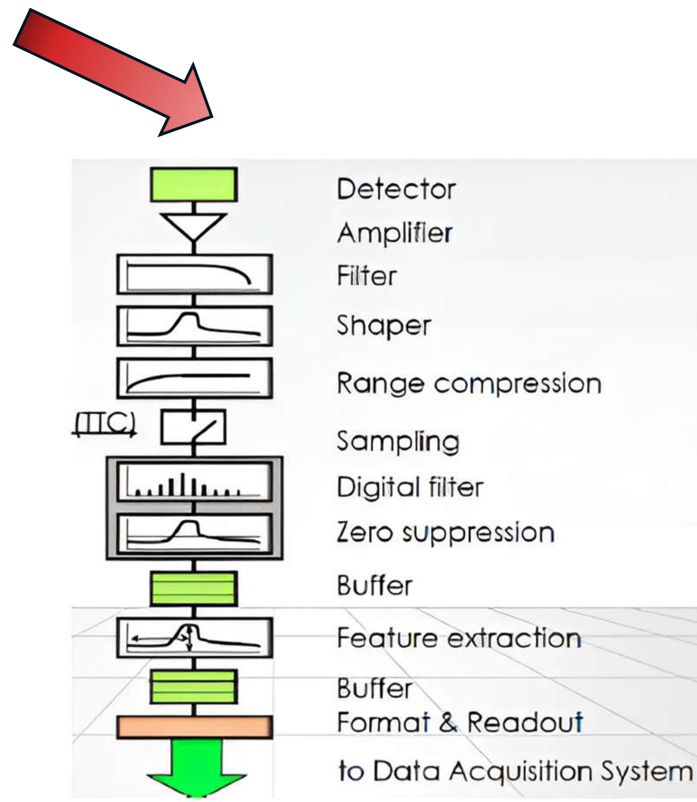
WHAT IS A D.A.Q.?

Analog Data Acquisition System



Digital Data Acquisition System



Fundamental Requirements for a DAQ:

- Collection of data from detector ADC
- Buffering of data until activation of acquisition
- Recording of data after activation of acquisition
- Keeping record of boundary conditions

WHAT ARE TRIGGER AND D.P.P.?

In Nuclear Physics **TRIGGERING** is the system used as criteria to decide which event in a detector should be saved.

\+

DIGITAL PULSE PROCESSING (D.P.P.), i.e. **ONLINE ANALYSIS** of the signal before further downstream software analysis

⇓

THESE ARE NECESSARY BECAUSE IT IS **NOT POSSIBLE TO SAVE DATA INDISCRIMINATELY**.
Ideally, the user would like to save as much data as possible in order to reconstruct an event.
In reality, this is **IMPOSSIBLE DUE TO FINITE MEMORY LIMITS**.

DPPS MADE IN CAEN

DPP PHA

Pulse Height Analysis

DPP PSD

Pulse Shape Discrimination

DPP ZLE PLUS

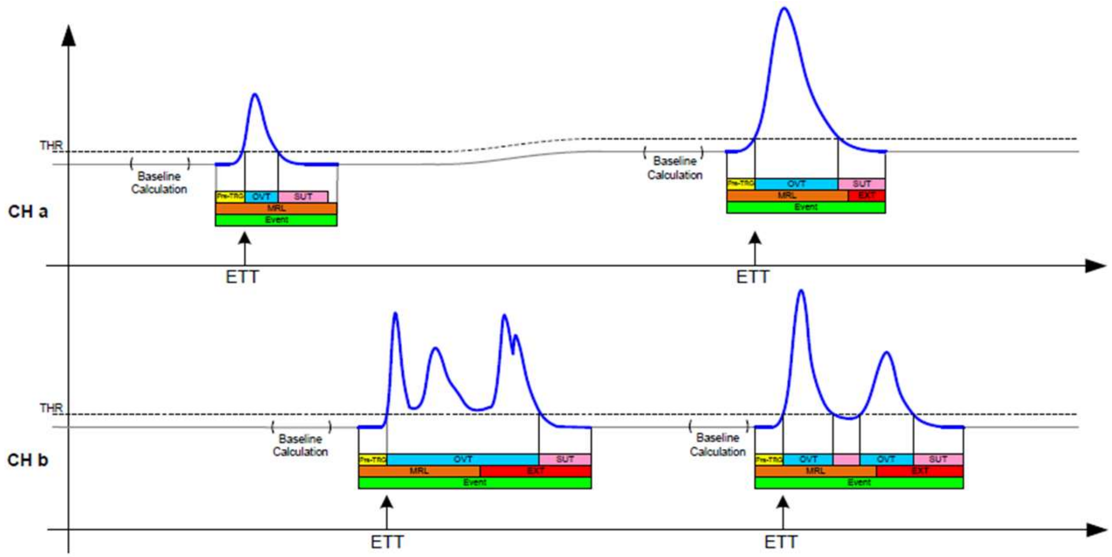
Zero Length Encoding

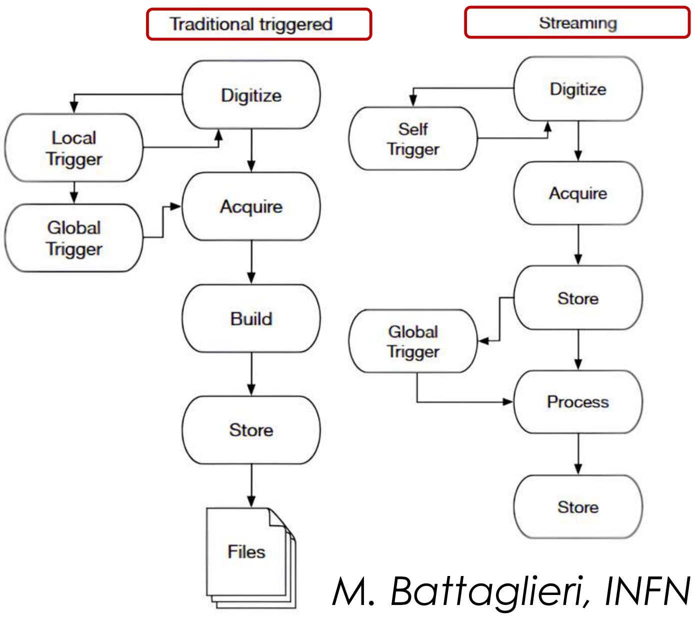
DPP DAW

DYNAMIC ACQUISITION WINDOW:
a hybrid system towards the
STREAMING READOUT (S.R.O.) to
OVERCOME ALGORITHMIC HARDWARE RIGIDITY
and
POSTPONE ANALYSIS TO DOWNSTREAM SOFTWARE

DPP-DAW FOR STREAMING READOUT (SRO)

DYNAMIC ACQUISITION WINDOW:
based on CHANNEL LOCAL SELF-TRIGGER and can DYNAMICALLY ADJUST ACQUISITION RECORD LENGTH TO MATCH DURATION OF INPUT PULSES





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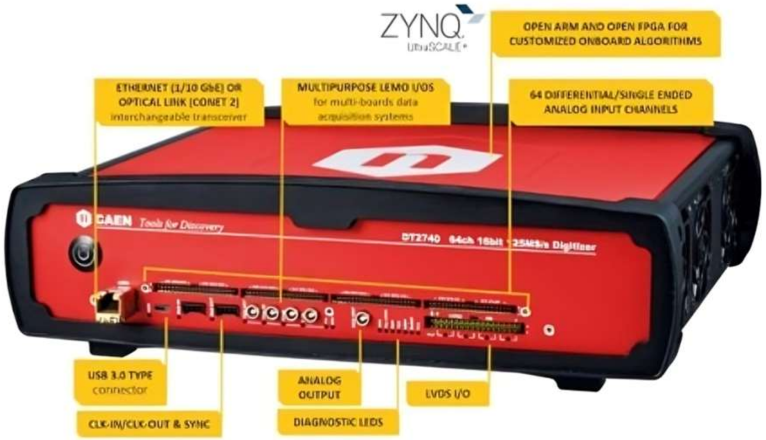
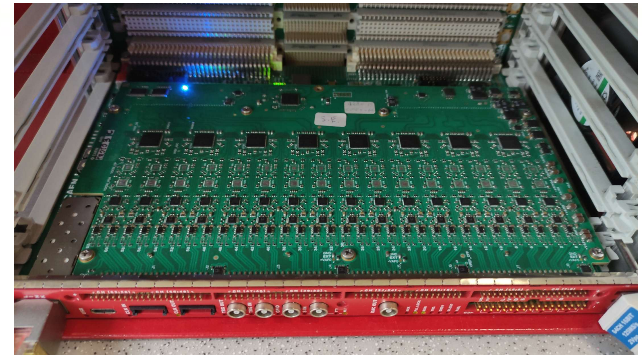
PREVENTS ACCIDENTAL CLIPPING AND DATA LOSS ASSOCIATED WITH FIXED ACQUISITION WINDOW IF THE PULSE (EVENT) IS LONGER THAN EXPECTED

DPP-DAW ON CAEN V2740 DIGITIZER

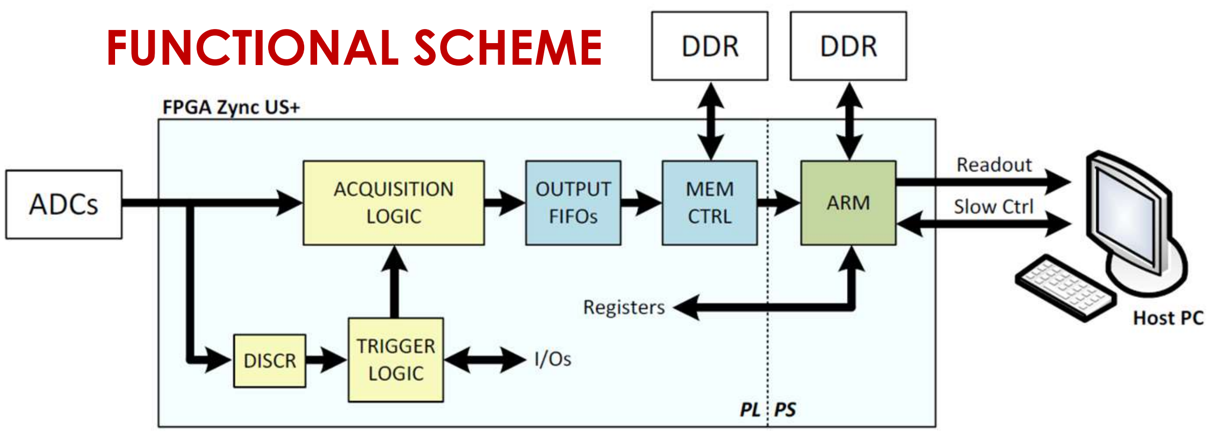


ADCs piggyback
64 channels 125 MHz 16bit

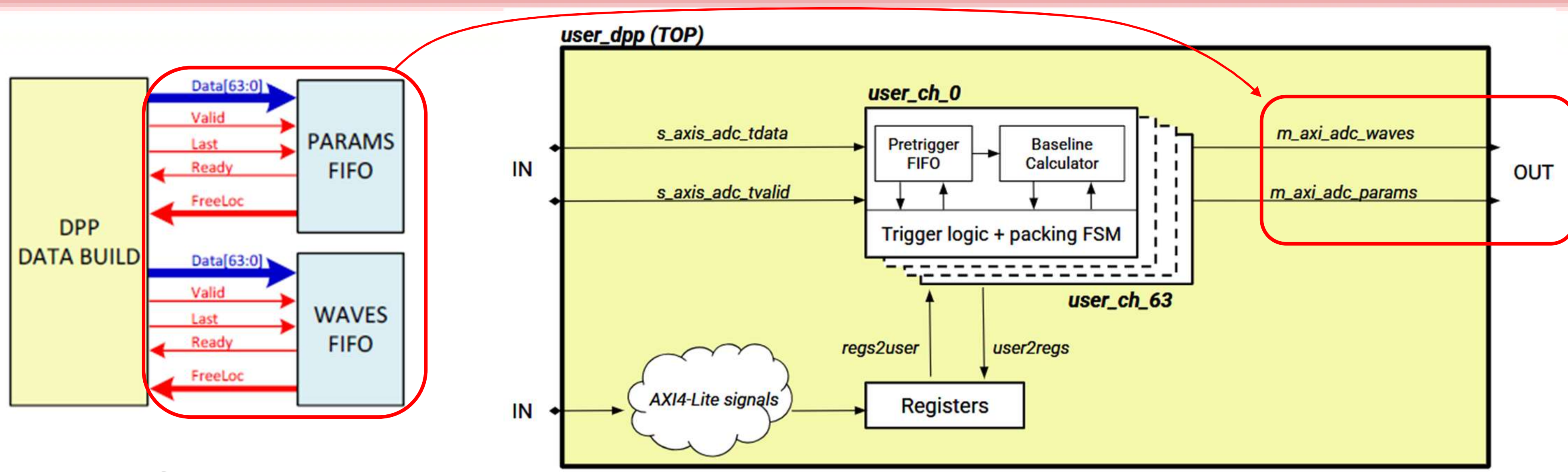


Motherboard with Zynq

FUNCTIONAL SCHEME



DAW FIRMWARE INFRASTRUCTURE



TWO BUFFER MEMORIES BEFORE DDR-RAM

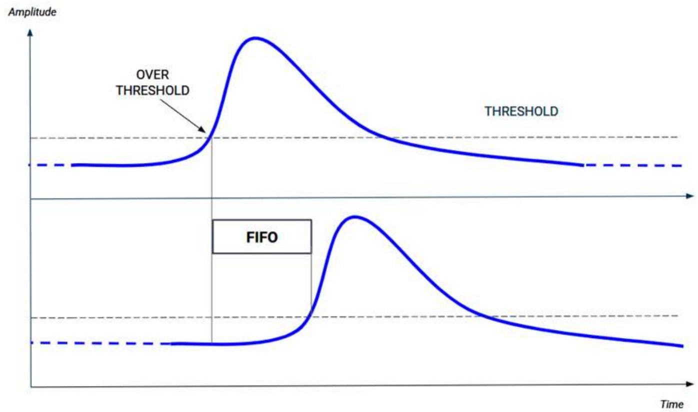
- ONE FOR PARAMETERS
- ONE FOR WAVEFORMS

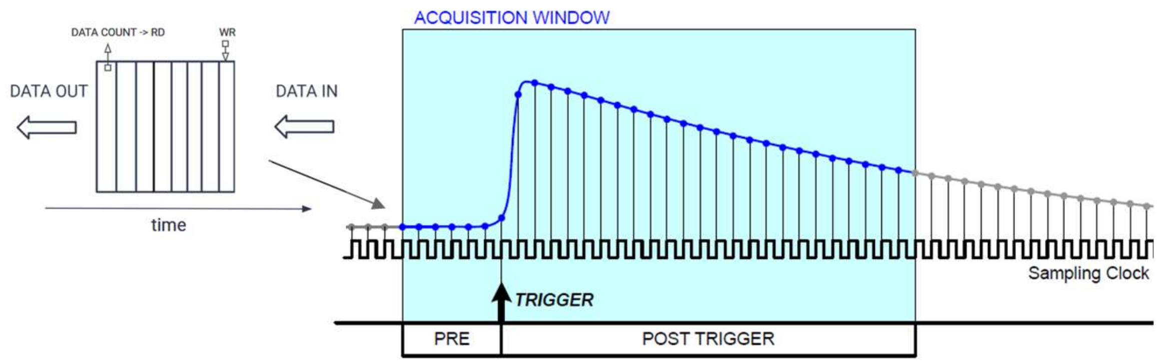
MAIN COMPONENTS OF DAW

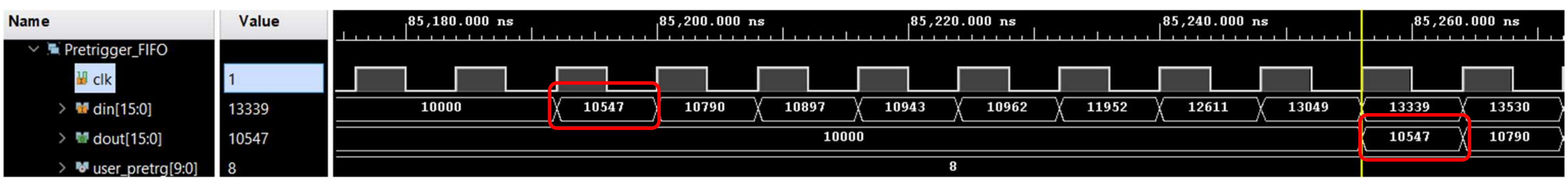
- PRE-TRIGGER FIFO
- BASELINE CALCULATOR
- SELF-TRIGGER LOGIC (OVER-THRESHOLD)
- ACQUISITION FSM

PRE-TRIGGER FIFO

WHEN A TRIGGER ARRIVES, PHYSICISTS are interested NOT ONLY in what happens AFTER, BUT ALSO BEFORE THE TRIGGER OCCURS. THE PRE-TRIGGER FIFO CREATES A "TIME WINDOW" GRANTING ACCESS TO DATA BEFORE TRIGGERING.







SIGNAL BASELINE

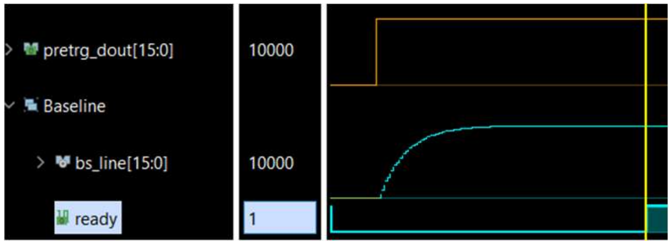
It is used to CREATE **RELATIVE THRESHOLD FOR THE TRIGGER**.

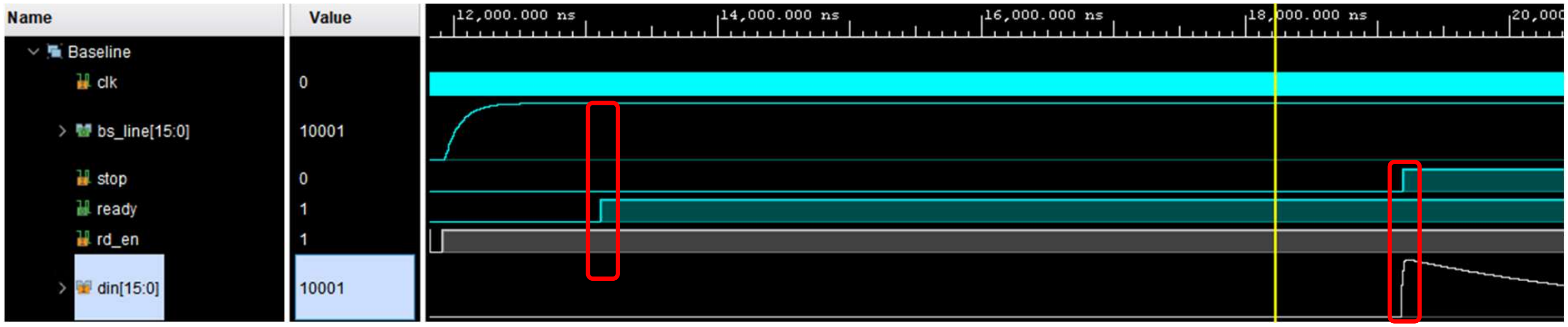
DYNAMIC BASELINE ENABLES THE TRIGGER TO ADAPT to the signal, **COMPENSATING TEMPERATURE DRIFT** => **SELF-TRIGGER CHANNEL MANAGEMENT**

EXPONENTIAL MOVING AVERAGE

$$EMA = y(n) = \alpha\, x[n] + (1-\alpha)\, y[n-1]$$

$$\tau = \frac{1}{\alpha} = 2^n\, samples = filter\ sensitivity$$



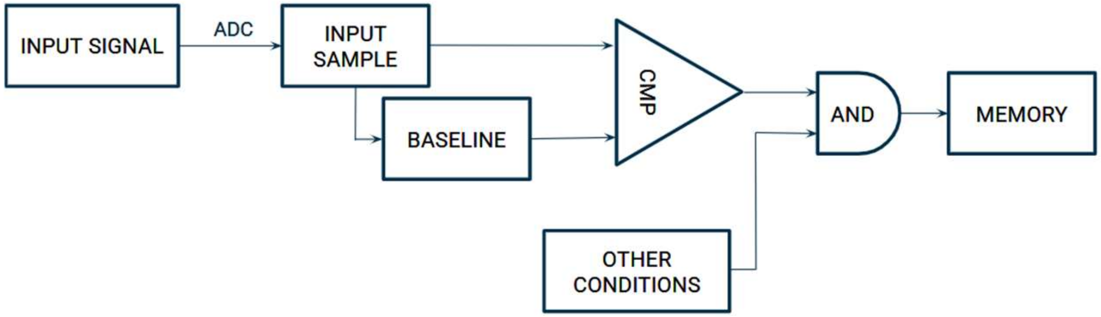


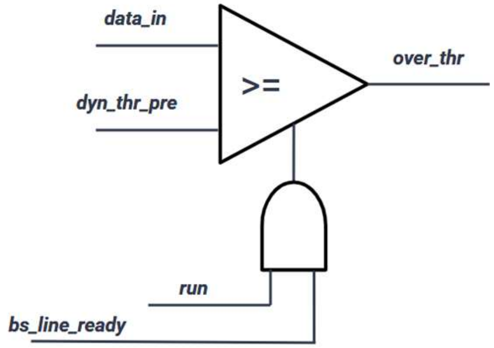
$t_{settling} = -2^n\, ln(1-P)$ SETTLING TIME OK INCOMING SIGNAL => STOP BSL CALC

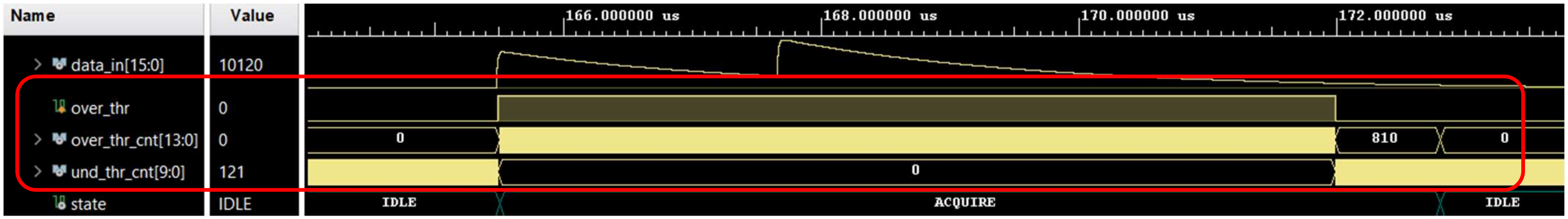
OVER-THRESHOLD SELF-TRIGGER

It is FUNDAMENTAL for SELECTING RELEVANT EVENTS AND REDUCING DATA AMOUNT.

Flag and Counters work as REFERENCE for FSM transitions.



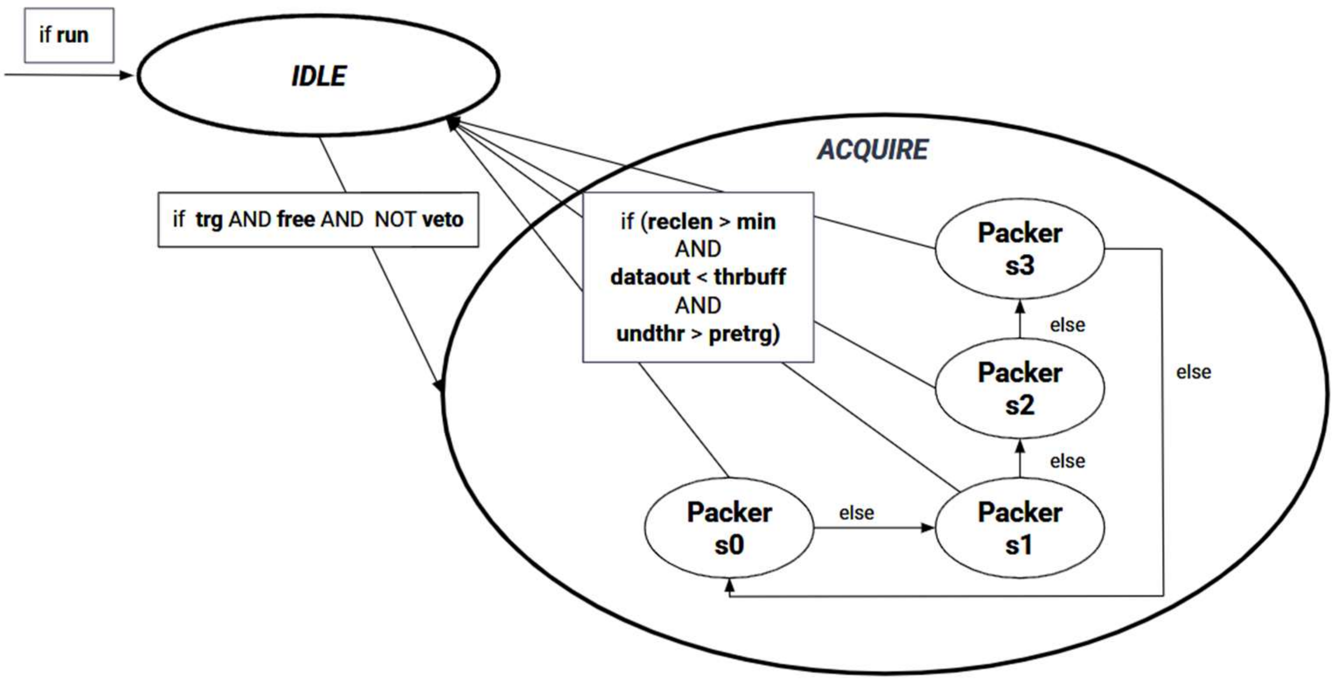




ACQUISITION FSM

FSM has been used for TWO specific functions:

- MOVING BETWEEN *IDLE* AND *ACQUIRE* STATES
- PACKAGING OF THE WORDS FOR SOFTWARE ANALYSIS



FROM *IDLE* TO *ACQUIRE*:
timestamp, channel ID…
TO FIFO PARAMETERS

IN *ACQUIRE*: WAVEFORMS

FROM *ACQUIRE* TO *IDLE*:

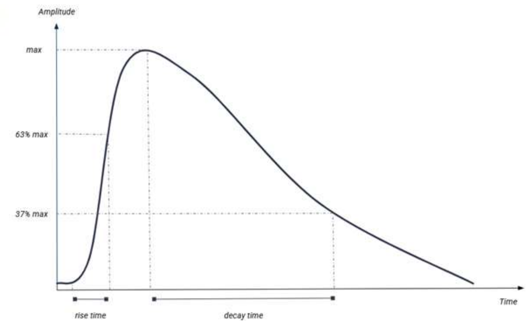
- BASELINE
- OVER-THR COUNTER
- TAIL FLAG
- STOP CONDITIONS
- PILE-UPs COUNTER

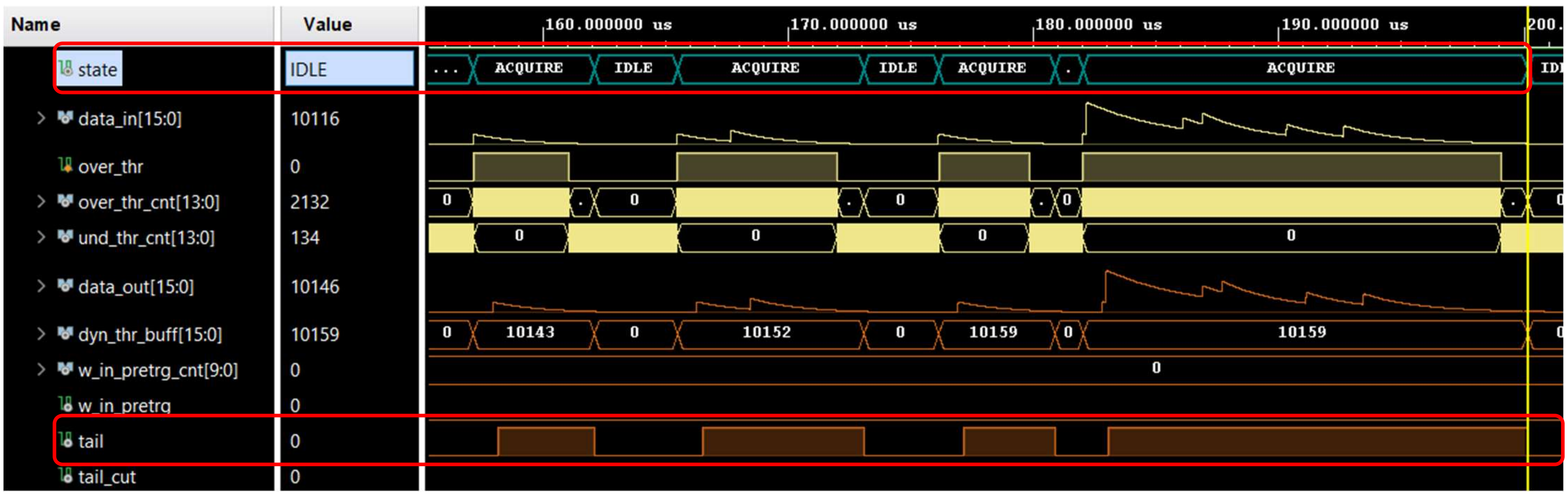
TO FIFO PARAMETERS

ACQUISITION SIMULATIONS

OUTPUT FROM DETECTOR:

SCINTILLATION LIGHT PULSE





SOFTWARE ANALYSIS (DATA FORMATS)

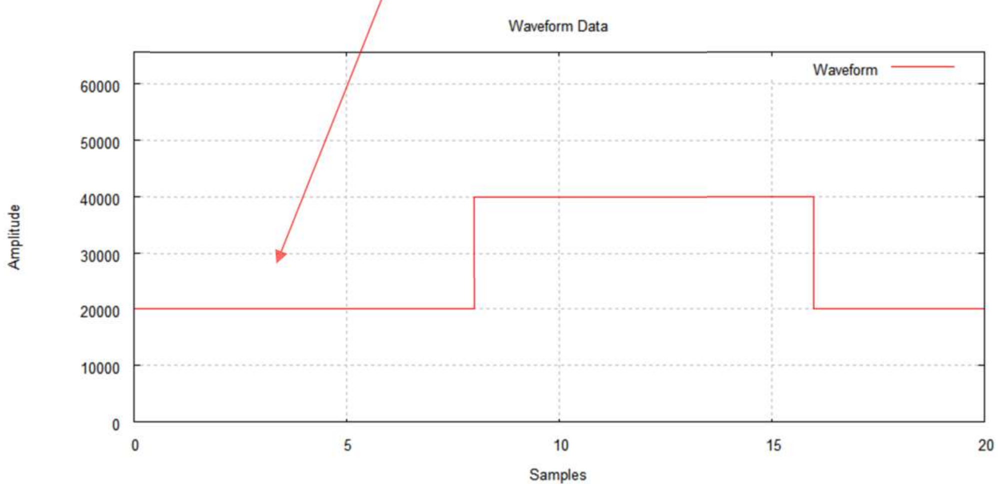
READ AND PROCESS DATA COMING FROM FPGA: *struct event* (C language)

RAW format

0x0000013E4D861070	280000010001c201
0x0000013E4D861078	00000000001314ba
0x0000013E4D861080	fff0340020004e20
0x0000013E4D861088	0000000000000006
0x0000013E4D861090	4e204e204e204e20
0x0000013E4D861098	4e204e204e204e20
0x0000013E4D8610A0	9c409c409c409c40
0x0000013E4D8610A8	9c409c409c409c40
0x0000013E4D8610B0	4e204e204e204e20
0x0000013E4D8610B8	0000000000004e20

BASELINE

4e20 = 20000
9c40 = 40000



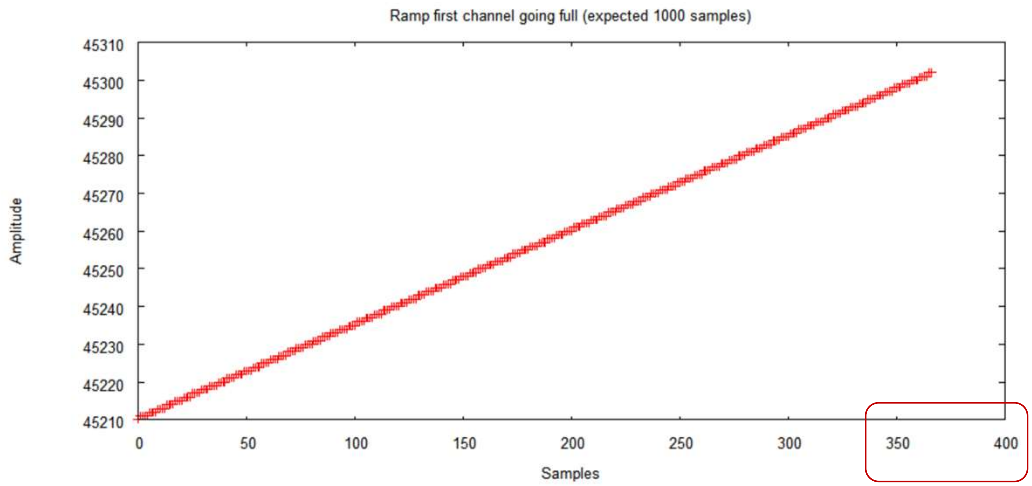
DECODED format

&evt	0x0000002f3c1ff968 {0x000001
	0x000001ce976e9f80 {channel
channel	63 '?'
timestamp	303753
user_info_size	1 '\x1'
energy	20000 BASELINE
fine_timestamp	0
psd	1600
flags_a	205 'Í'
flags_b	9
event_size	3256
waveform	0x000001ce97796660 {20000}
n_allocated_samples	16380
n_samples	1616
&evt->event_size	0x000001ce976e9fa0 {3256}

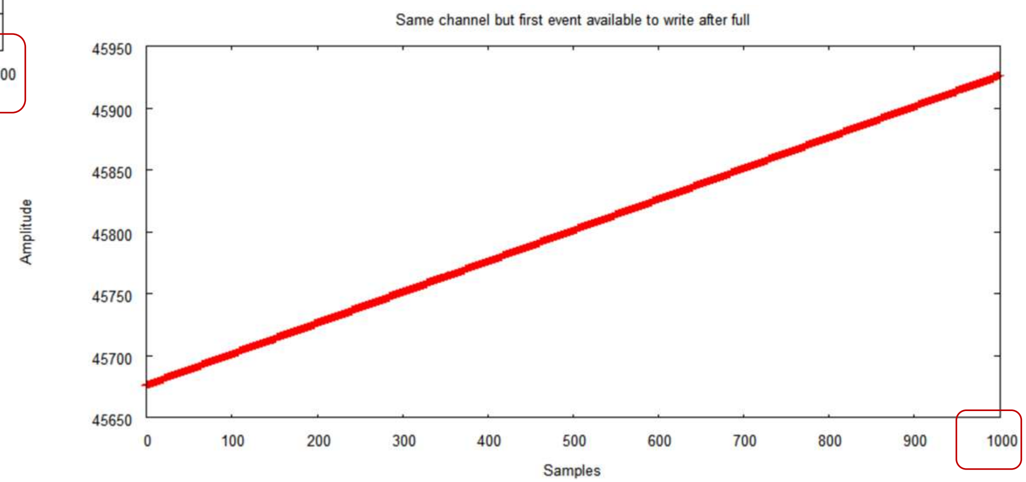
SOFTWARE ANALYSIS (MEMORY FULL MANAGEMENT)

HISTOGRAM DISTRIBUTION OF DELAYS (Δt)

MEM-FULL EVENT (350 instead of 1000 samples saved)

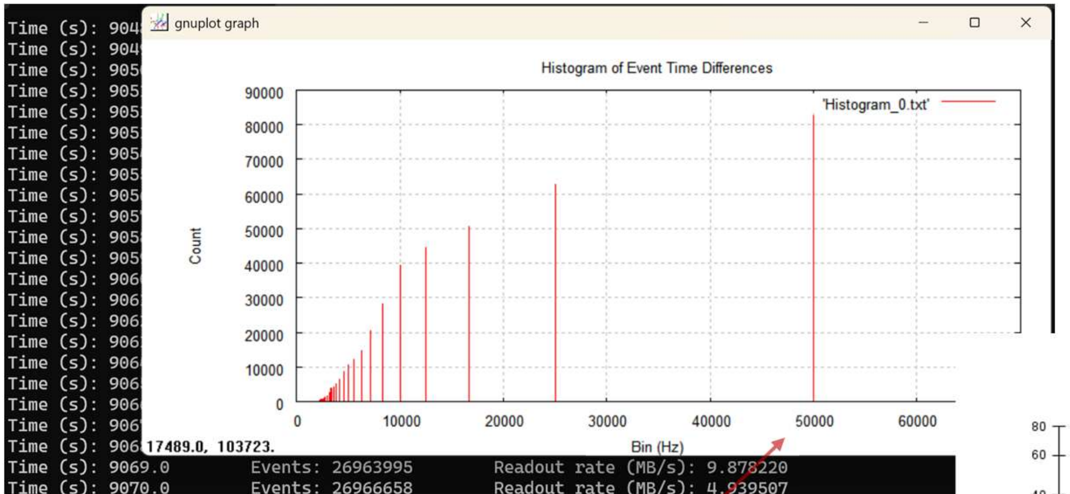


FIRST EVENT AFTER MEM-FULL



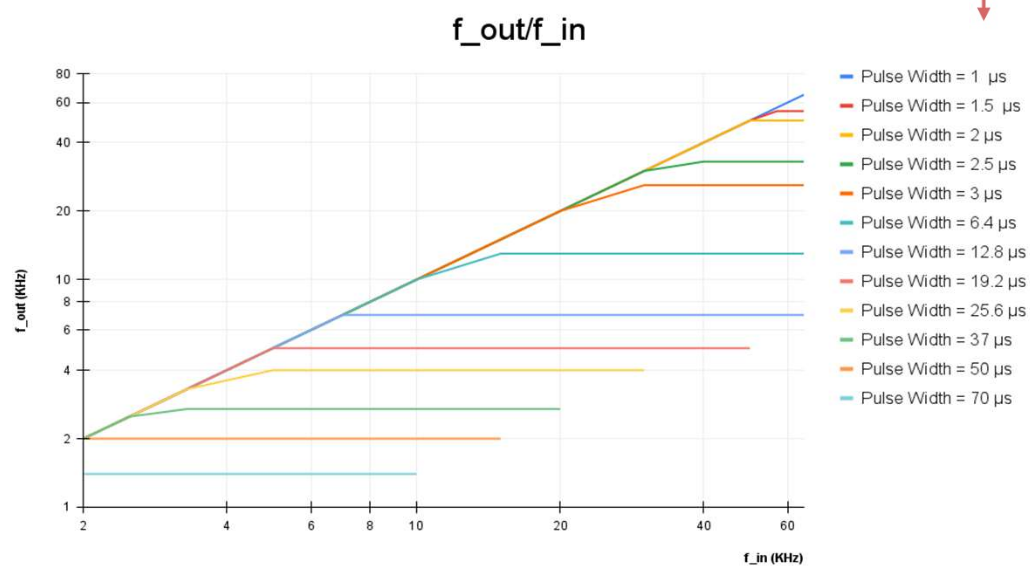
SOFTWARE ANALYSIS (MEMORY FULL MANAGEMENT)

HISTOGRAM DISTRIBUTION OF DELAYS (Δt)



INCREASING PULSE WIDTH

(MORE INFO TO SAVE)

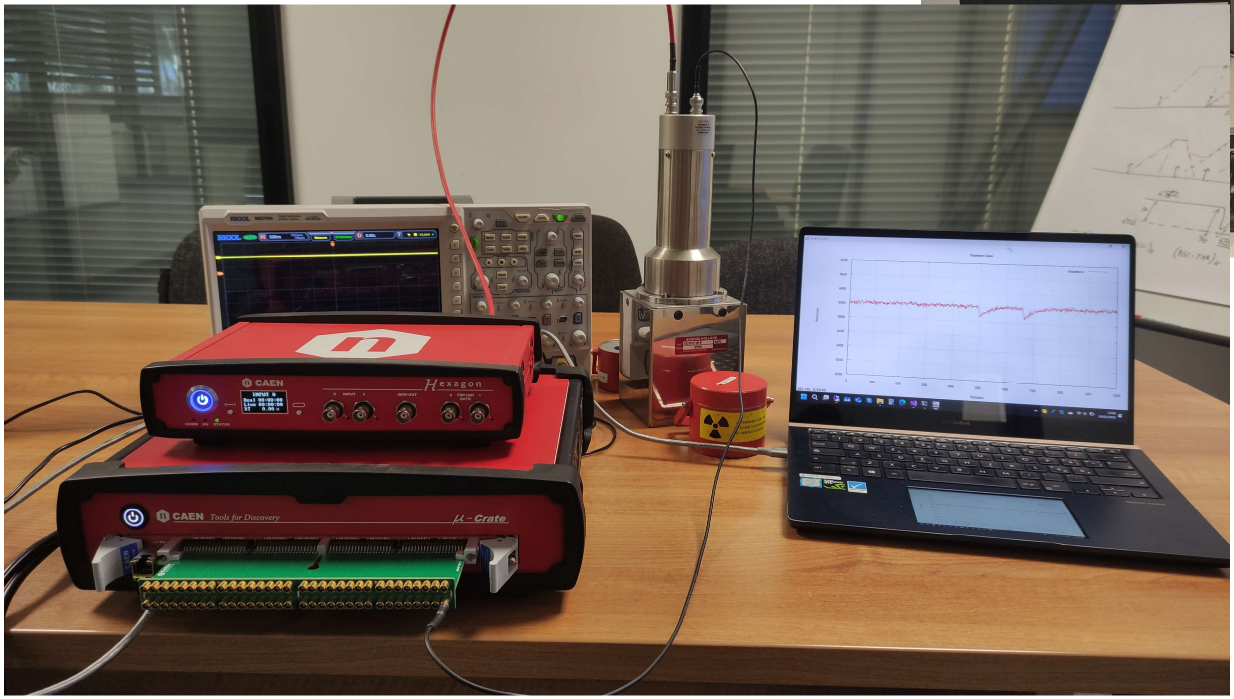


PERIODIC EVENT RATE

(PULSE PERIOD 20 µs)

EXPERIMENTAL RESULTS ^{60}Co: SETUP

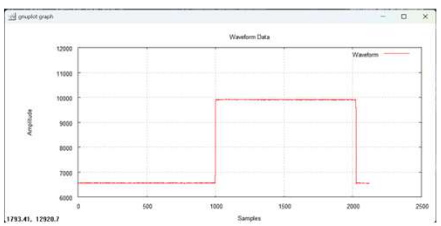
WITH PULSE GENERATOR



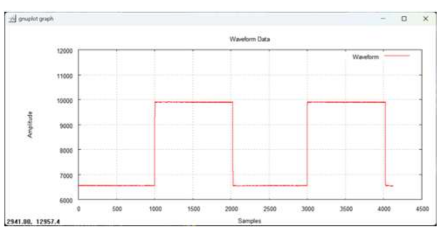
WITH SCINTILLATOR

^{60}Co ISOTOPE DECAYS: PILED-UP EVENTS

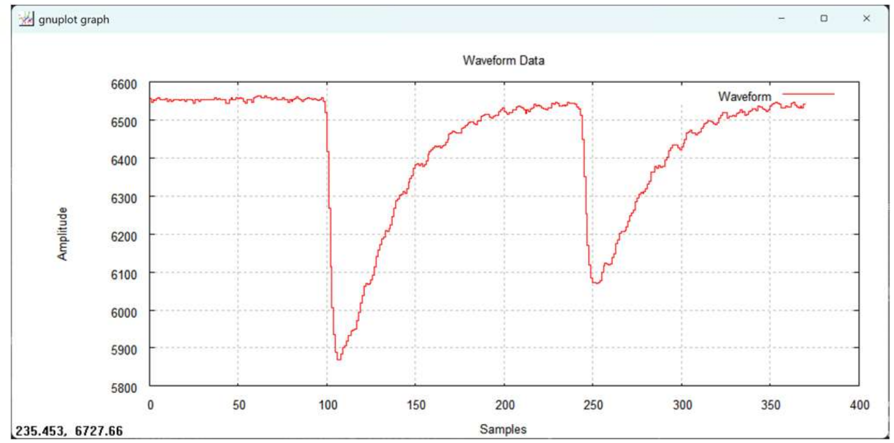
PILED-UP if pulses are "close":
Event Rate > Event Rate limit
(every 17μs here)

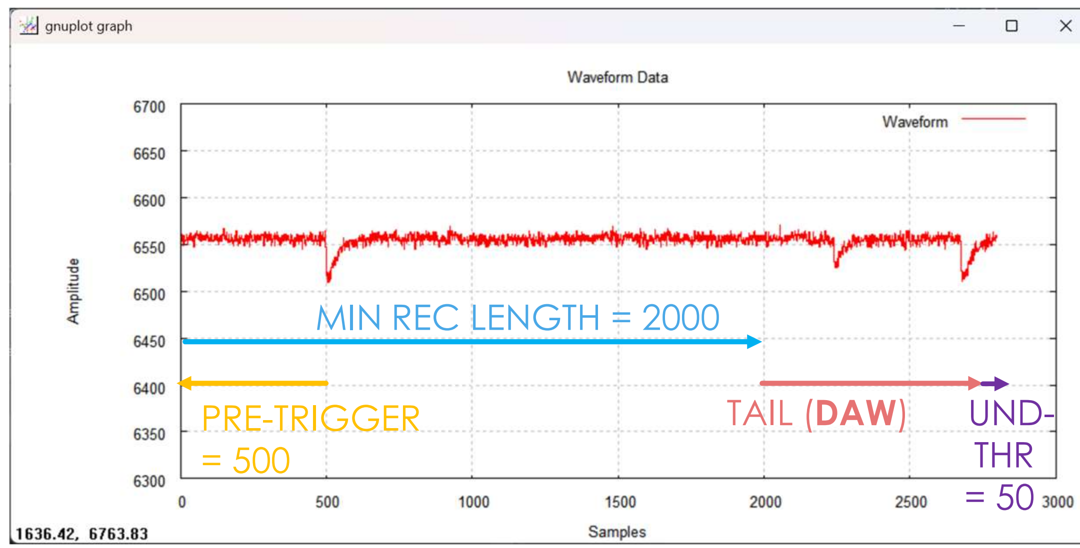


E.R. every 18μs
=> NO PILE-UP



E.R. every 16μs
=> PILE-UP





CONCLUSIONS

DYNAMIC ACQUISITION WINDOW (DAW) FIRMWARE REPRESENTS
A SIGNIFICANT UPGRADE for DIGITAL PULSE PROCESSING (DPP).

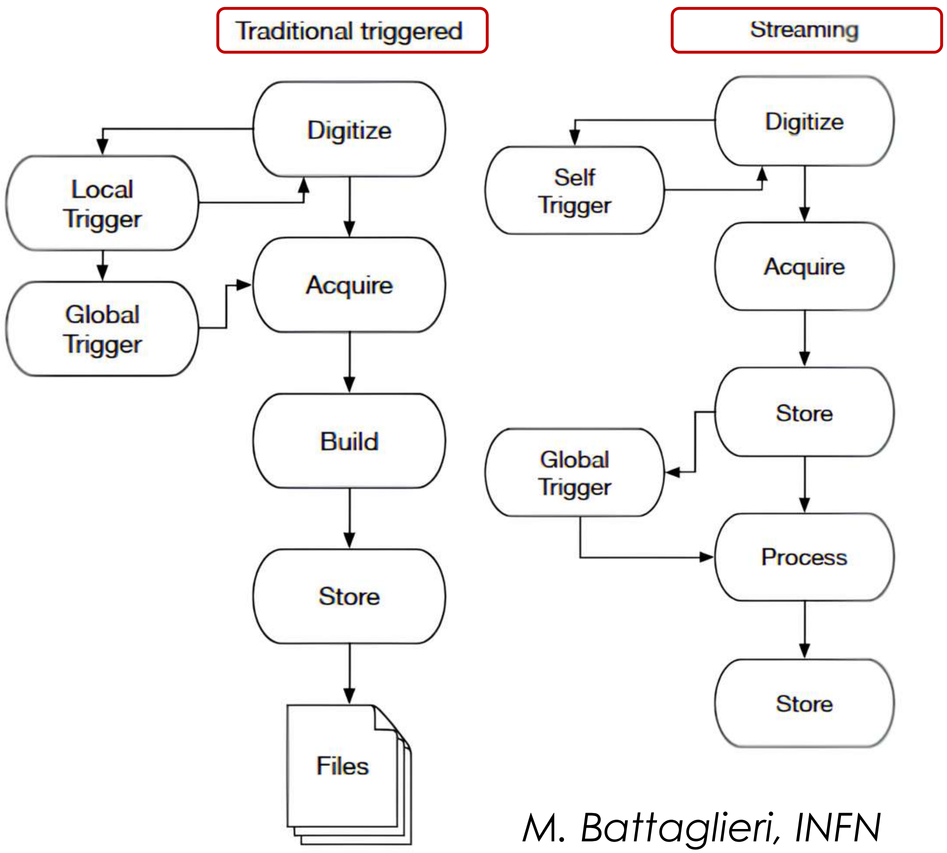
USING VARIABLE-LENGTH ACQUISITION, CONTINUOUS BUFFERING
WITH PRETRIGGER MEMORY AND SMART INDIVIDUAL SELF-TRIGGER THRESHOLDS
THE SYSTEM REPRESENTS A STEPPINGSTONE FOR CONTINUOUS ACQUISITION FROM ADCs
BASED ON PURE TRIGGER-LESS AND STREAMING READOUT (SRO)
PARADIGMS IN NUCLEAR PHYSICS.

BACKUP SLIDES

FEATURES OF DAW for SRO

- INDEPENDENT TRIGGERS PER CHANNEL
- SMART THRESHOLD BASED SELF-TRIGGERS
- VARIABLE-LENGTH ACQUISITION WINDOW
- PROGRAMMABLE *PRE* and *POST* TRIGGER SAMPLES

HYBRID “TRIGGER-LESS” SYSTEM



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BACKUP SLIDES

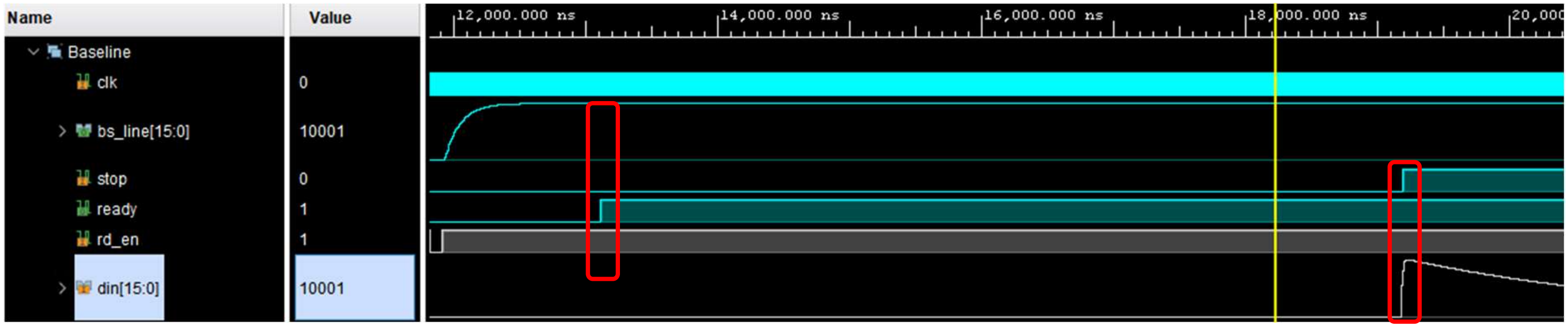
$$\boldsymbol{y(t) = x(t)\left(1 - e^{-t/\tau}\right)} \rightarrow H(s) = \frac{1}{1+\tau s} \rightarrow \mathrm{H(z)} = \frac{\alpha}{1-(1-\alpha)z^{-1}} \; with\; \boldsymbol{\alpha = \frac{T}{T+\tau} \cong \frac{T}{\tau} \cong \frac{1}{\tau}}$$

$$\rightarrow \boldsymbol{y(n) = \alpha\, x[n] + (1-\alpha)\, y[n-1]}$$

In the EMA, alpha determines sensitivity of the filter:

HIGHER N.OF SAMPLES => LESS SENSITIVE TO INCOMING SAMPLE

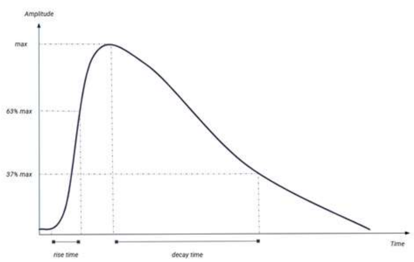
LOWER N.OF SAMPLES => MORE SENSITIVE TO INCOMING SAMPLE

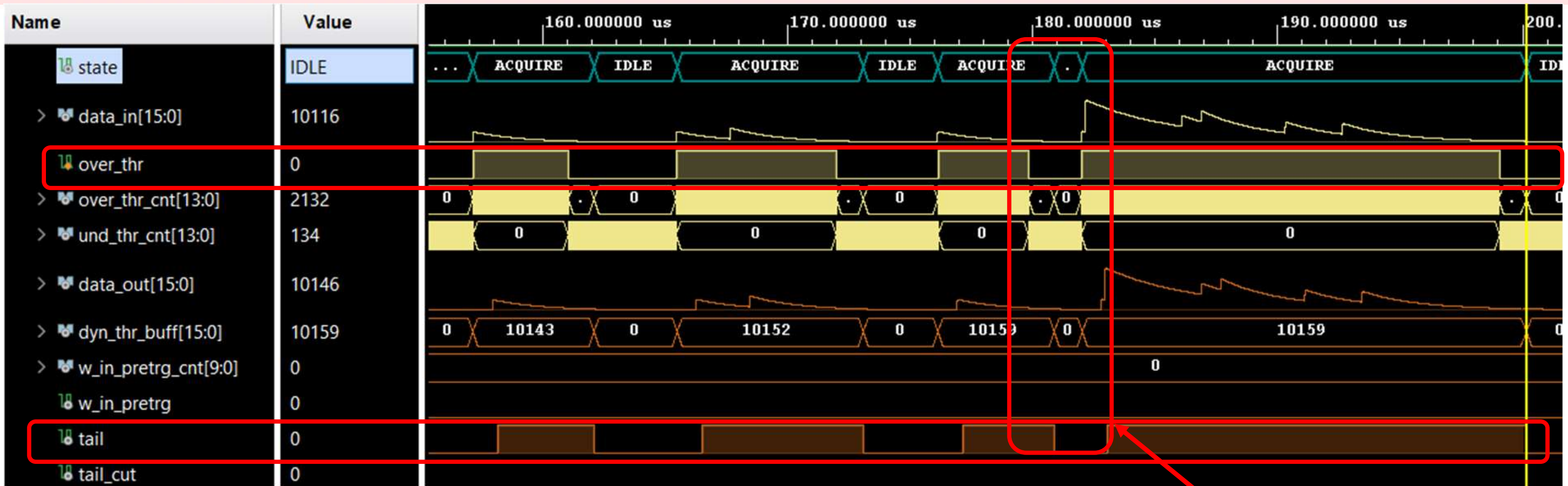


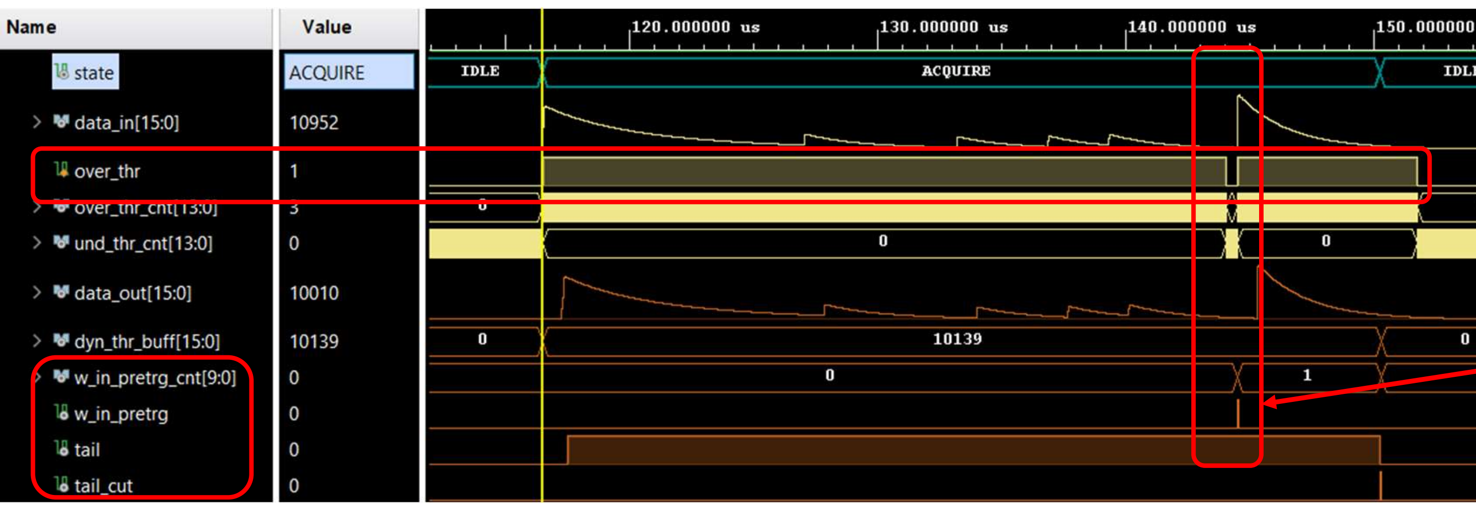
$t_{settling} = -2^n\, ln(1-P)$ **SETTLING TIME OK** **INCOMING SIGNAL => STOP BSL CALC**

ACQUISITION SIMULATIONS

SCINTILLATION LIGHT PULSE







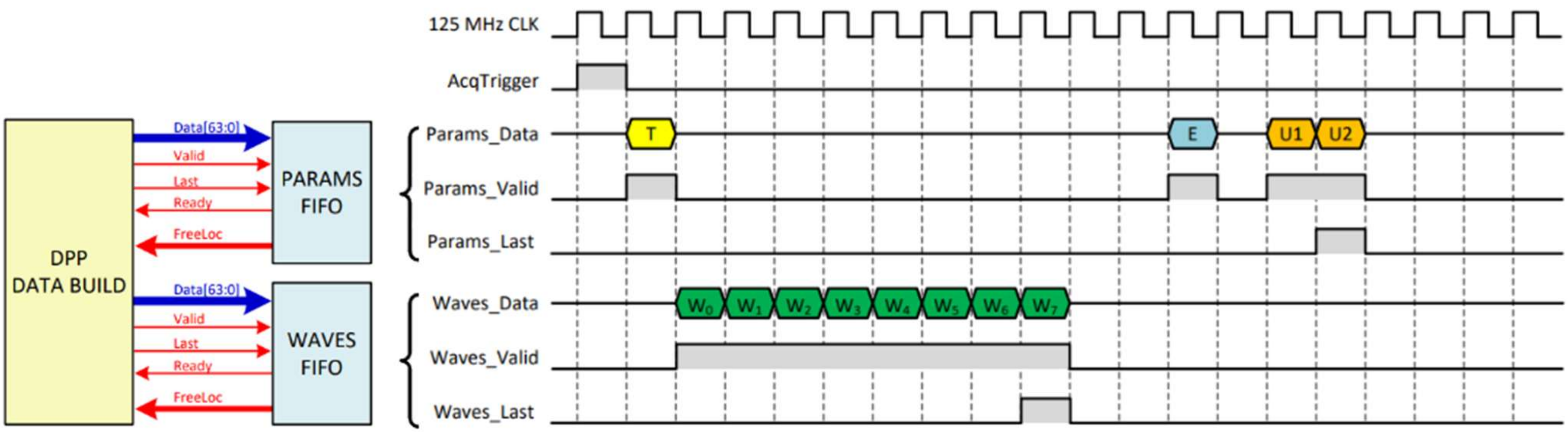
NO PILE-UP

PILE-UP

(corner case)

BACKUP SLIDES

Waves and **parameters** of the acquisition are saved temporarily in **two FIFOs** also on AXI4-Lite bus.



BACKUP SLIDES

Waves and **parameters** are packed in the following way. A decoding device is added at the bottom.

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W	S	ChID[5:0]						SE	Info[6:0]							TimeStamp[47:0]																																															

First *parameters word*

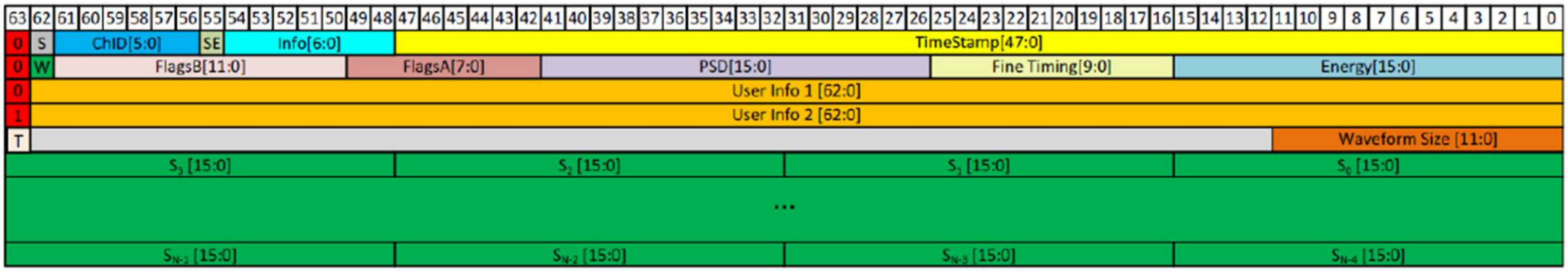
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Re	Rw	Custom parameters[61:16]																																														Baseline[15:0]															

Last *parameters word*

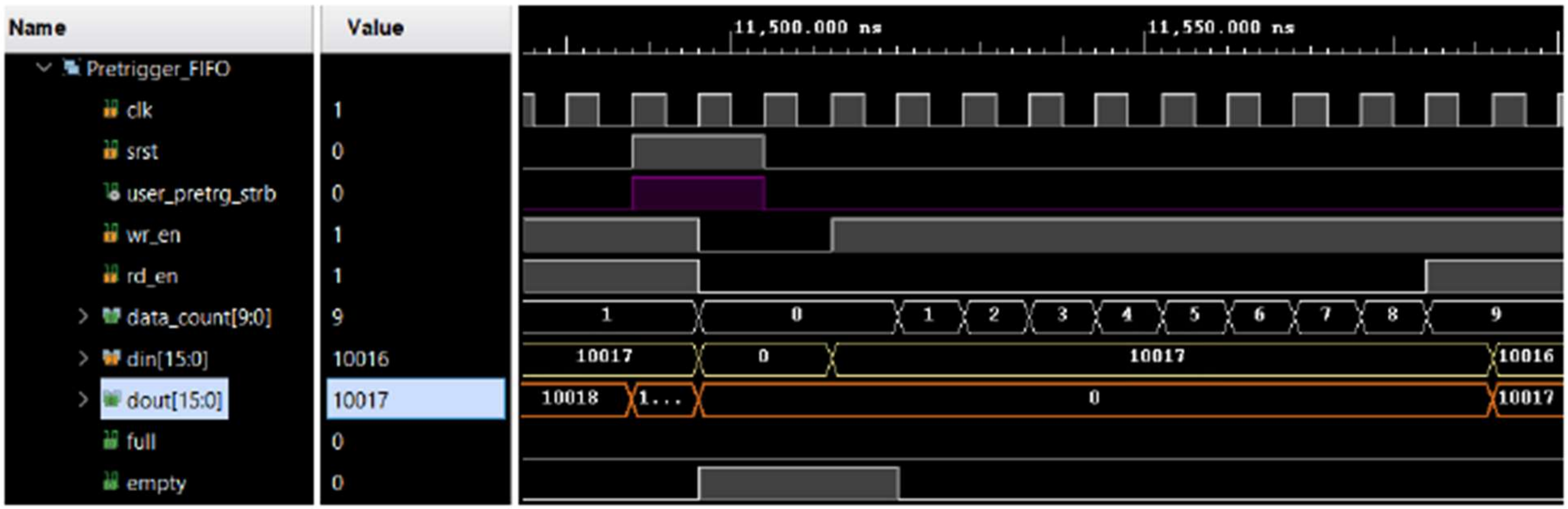
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sample(n+3)[15:0]																Sample(n+2)[15:0]																Sample(n+1)[15:0]																Sample(n)[15:0]															

Waveforms *word*

BACKUP SLIDES



BACKUP SLIDES



BACKUP SLIDES

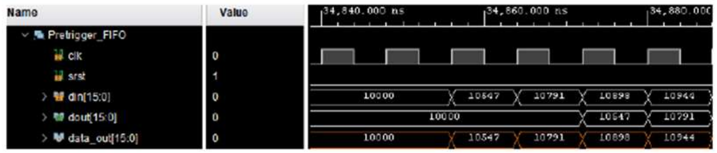


Figure 5.10: FIFO bypass with user pretrigger at 0 (short circuit)

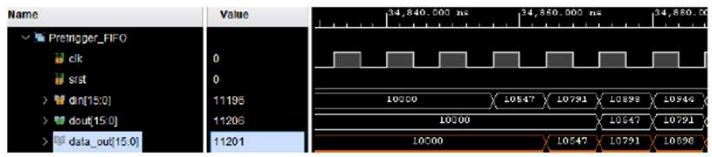


Figure 5.11: FIFO bypass with user pretrigger at 1 (sampled)

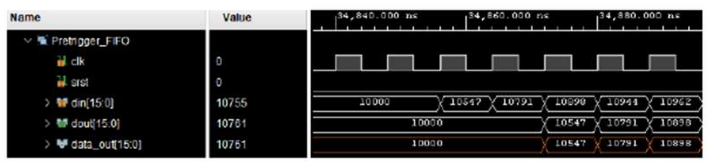


Figure 5.12: FIFO with user pretrigger at 2

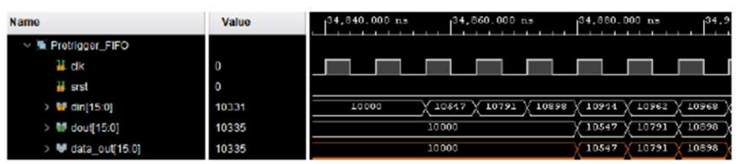
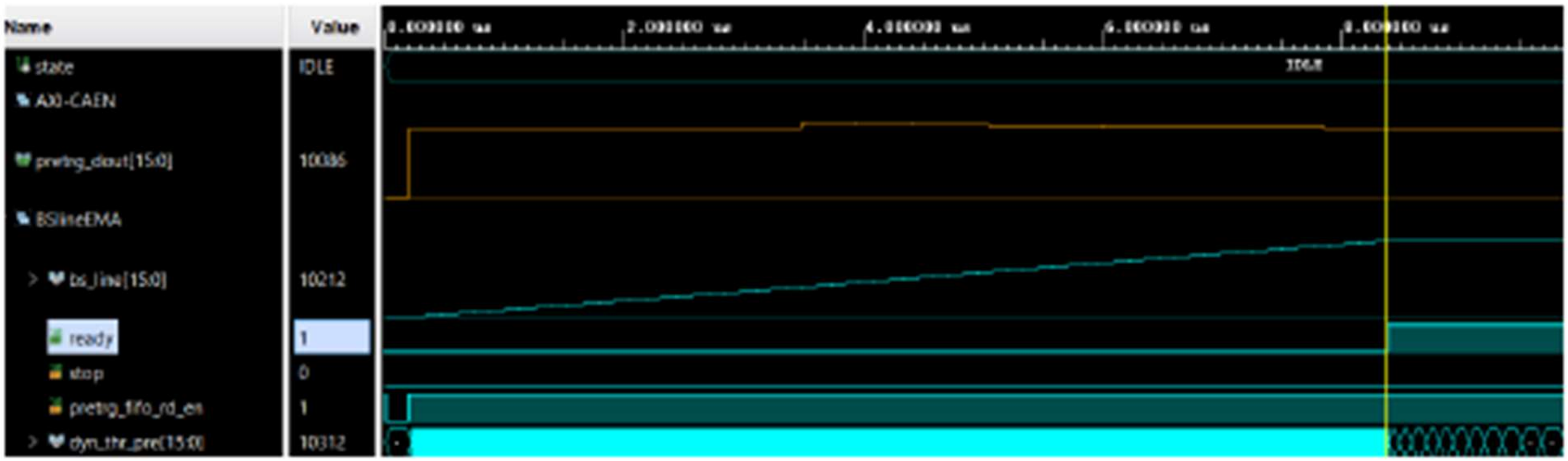


Figure 5.13: FIFO with user pretrigger at 3

BACKUP SLIDES



BACKUP SLIDES

Name	CLB LUTs (274080)	CLB Registers (548160)	CARRY8 (34260)	Block RAM Tile (912)	Bonded IOB (328)	GLOBAL CLOCK BUFFERs (404)
sample_packer_axi	303	478	24	0.5	155	1
BaseLine_comp (baseline_low_pass)	93	57	10	0	0	0
pretrig_FIFO_comp (fifo_generator_0)	63	57	6	0.5	0	0

Name	CLB LUTs (274080)	CLB Registers (548160)	CARRY8 (34260)	F7 Muxes (137040)	F8 Muxes (68520)	F9 Muxes (34260)	Block RAM Tile (912)	Bonded IOB (328)	GLOBAL CLOCK BUFFERs (404)
sample_packer_axi	846	485	71	128	64	32	0.5	155	1
BaseLine_comp (baseline_sma_array)	578	64	57	128	64	32	0	0	0
pretrig_FIFO_comp (fifo_generator_0)	63	57	6	0	0	0	0.5	0	0

Name	CLB LUTs (274080)	CLB Registers (548160)	CARRY8 (34260)	Block RAM Tile (912)	Bonded IOB (328)	GLOBAL CLOCK BUFFERs (404)
sample_packer_axi	692	535	87	0.5	155	1
BaseLine_comp (baseline_sma)	354	114	73	0	0	0
pretrig_FIFO_comp (fifo_generator_0)	63	57	6	0.5	0	0

BACKUP SLIDES

Figures 9.8 and 9.9 depict a macro view of the AXI4-Lite management.

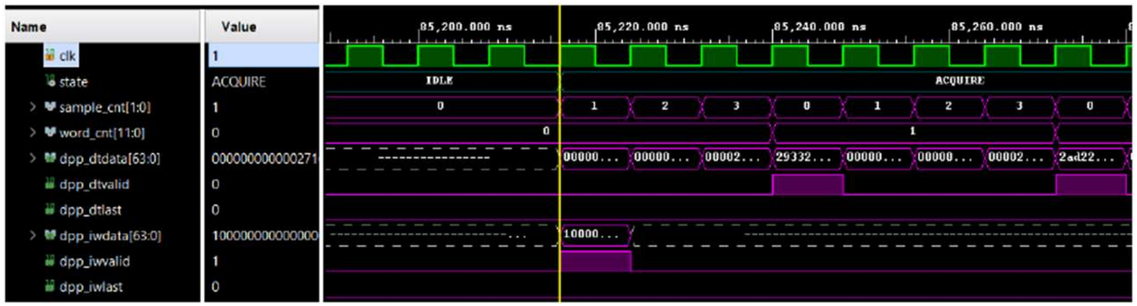


Figure 9.8: AXI4-Lite bus macro view from IDLE to ACQUIRE state

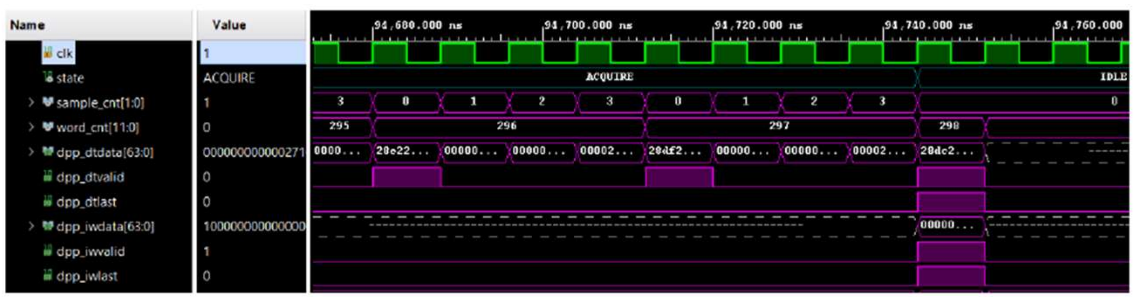


Figure 9.9: AXI4-Lite bus macro view from ACQUIRE to IDLE state

BACKUP SLIDES

Resource	Utilization	Available	Utilization %
LUT	182175	522720	34.85
LUTRAM	5124	161280	3.18
FF	259592	1045440	24.83
BRAM	215.50	984	21.90
URAM	80	128	62.50
DSP	32	1968	1.63
IO	252	512	49.22
GT	35	48	72.92
BUFG	26	940	2.77
MMCM	4	11	36.36
PLL	3	22	13.64

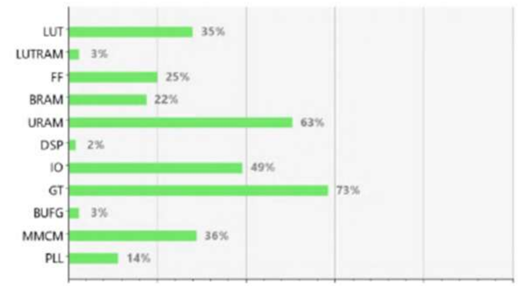


Figure 10.3: Utilization report after implementation V2740 module

Name	CLB LUTs (522720)	CLB Registers (1045440)	CARRY8 (65340)	F7 Muxes (261360)	F8 Muxes (130680)	Block RAM Tile (984)	URAM (128)	DSPs (1968)
vx2740_top	193592	263562	3996	5835	2139	215.5	80	32
dbg_hub (dbg_hub_CV)	0	0	0	0	0	0	0	0
digit2_wrapper_inst (digit2_wrapper)	153425	216240	1878	5228	1920	183.5	80	32
digit2_i (digit2)	153425	216240	1878	5228	1920	183.5	80	32
user_dpp_inst (user_dpp)	40167	47322	2118	607	219	32	0	0

Figure 10.4: Utilization report recap after implementation V2740 module

ACKUP SLIDES

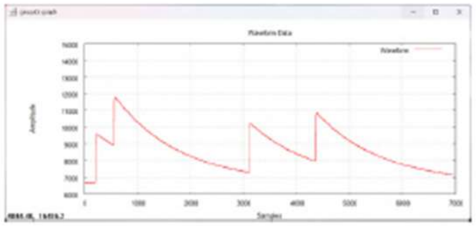


Figure 12.5: Event dynamically saved with multiple stacked pulses

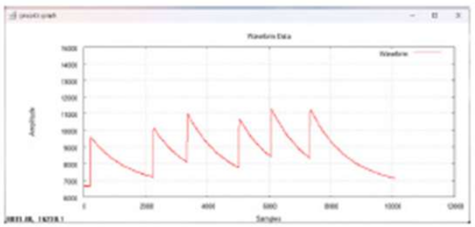


Figure 12.6: Event dynamically saved with multiple stacked pulses

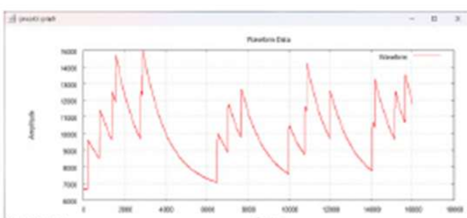


Figure 12.7: Event Tail cut due to maximum record length with multiple stacked pulses

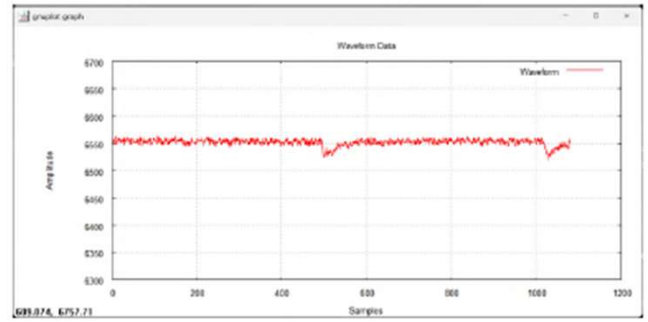


Figure 12.14: Event with two stacked pulses with Threshold 20, Pretrigger 500, Underthreshold 50, Minimum Record length 1000, Tail 15K (exit acquisition due to DAW)

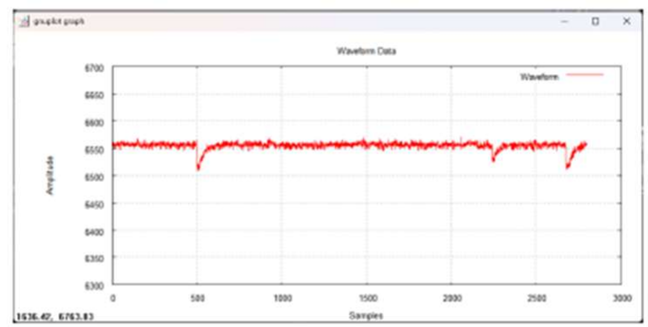


Figure 12.15: Event with three stacked pulses with Threshold 20, Pretrigger 500, Underthreshold 50, Minimum Record length 2000, Tail 14K (exit acquisition due to DAW)