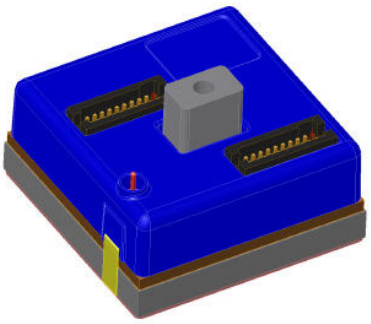
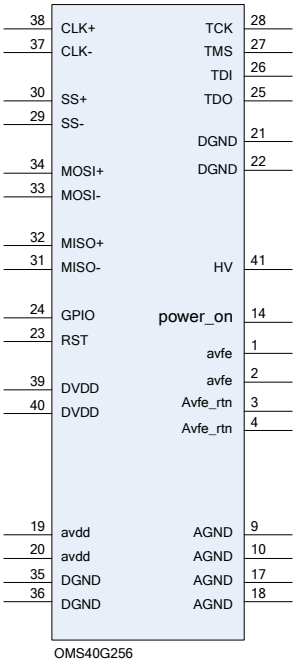
OMS40G256
256 channel CZT gamma radiation Detector.

General description.

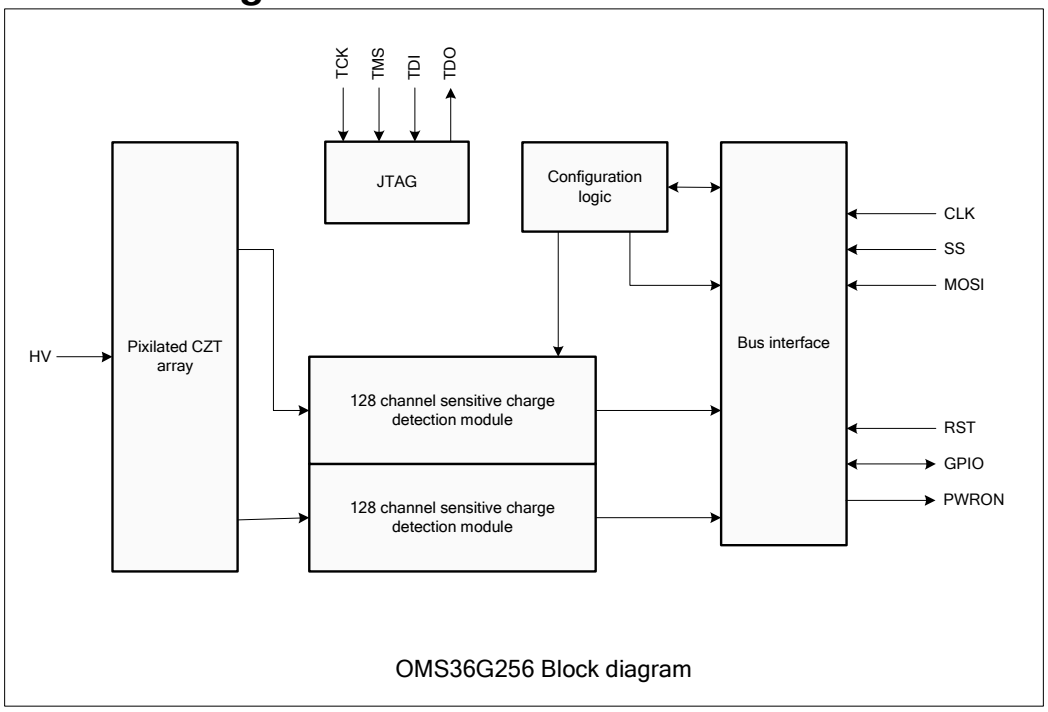
The OMS40G256 is a 256 channel Gamma radiation detector.
It is organized in a 16x16 matrix with a pitch of 2.46mm between pixels.
The OMS40G256 supports energy signals up to 200Kev.





OMS40G256

Function diagram.



OMS36G256 Block diagram

Pin description.

Signal name	Pin #	Type	Function
CLK+, CLK-	38,37	LVDS	Serial communication interface
SS+, SS-	30,29	LVDS	
MOSI+, MOSI-	34,33	LVDS	
MISO+, MISO-	32,31	LVDS	
GPIO	24	LVTTL I/O	General purpose line, programmable via the communication protocol.
PWRON	14	LVTTL OUT	Active low signal indicating detector is powered on.
RST	23	LVTTL IN	Reset
TCK	28	LVTTL IN	JTAG interface,
TMS	27	LVTTL IN	
TDI	26	LVTTL IN	
TDO	25	LVTTL OUT	
AVFE	1,2	Power	+1.5v analog
AVFE_RTN	3,4	Power	+1.5v analog rtn
AVDD	19,20	Power	Analog positive supply +3.3V
AGND	9,10,17,18	Power	Analog section GND
DVDD	39,40	Power	Digital section +3.3V supply
DGND	21,22,35,36	Power	Digital section GND
HV	41	Power	High voltage CZT bias.

Notes:

- AVFE power supply is dedicated for the front end electronics of the asic The avfe_rtn is the return line of the supply.

Absolute maximum ratings.

AVDD Supply voltage	+3.6V
DVDD Supply voltage	+3.6V
AVFE Supply voltage	+3.6V
HV Supply voltage	-1000V
Storage temperature	TBD
ESD rating	TBD

Operating ratings.

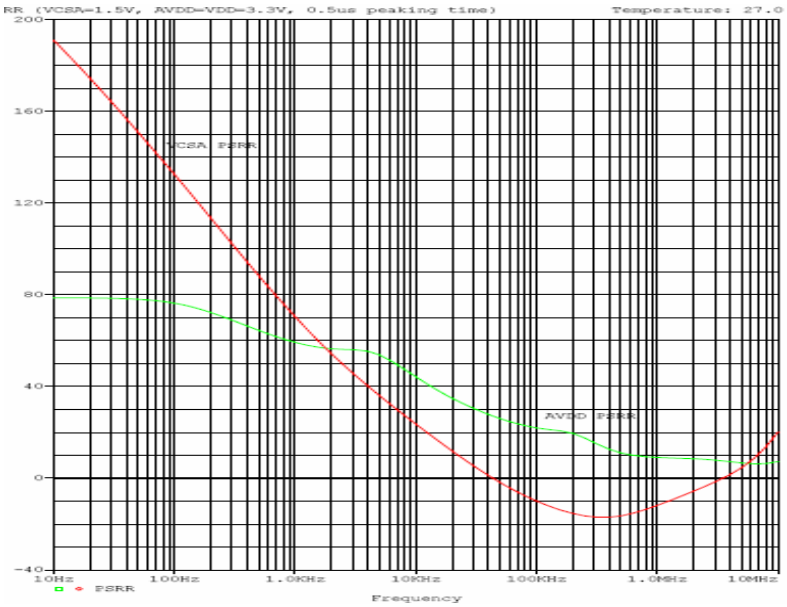
AVDD Supply voltage	+3.3V ±5%
AVFE Supply voltage	+1.5V to +3.3V
DVDD Supply voltage	+3.3V ±5%
AVDD, AVFE maximum ripple	See next page
AVFE typical current consumption	30 ma
AVDD typical current consumption	40 mA
DVDD typical current consumption	50 mA
HV Supply voltage	-550V to -800V
HV Supply voltage maximum ripple	See next page
Operating temperature	4°C to 34°C

Notes:

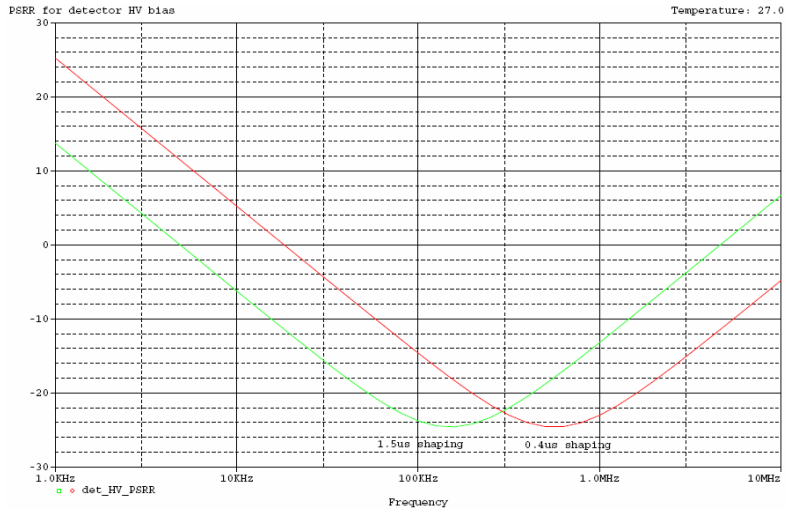
- The recommended power up sequence is dvdd, after ~200ms avdd and than after ~200ms avfe.. Than high voltage power supply should be powered ~ 0.5sec after the LV. supplies been powered.
- The temperature sensing of the module deviates $\sim 0.5°c$ from the CZT surface temperature.
- The output peak drift should be less $0.15kev/°c$

Power supplies characteristics

Below is a graph showing the power supply rejection ratio for AVDD and AVFE



HV ripple increase the total noise and degrade the energy resolution of the detector, below is a graph representing the HV power supply PSRR.

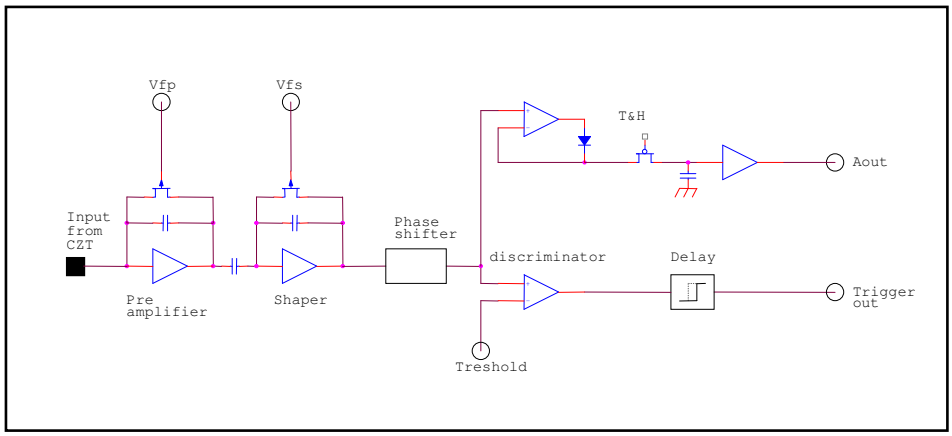


DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Low level LVDS output voltage	0.9	1.075	1.25	V
V_{OH}	High level LVDS output voltage	1.25	1.425	1.6	V
V_I	LVDS Input Voltage	0		2.925	V
V_{ODIFF}	LVDS differential Output Voltage	250	350	450	mV
V_{OCM}	LVDS output Common Mode Voltage	1.125	1.25	1.375	V
V_{ICM}	LVDS input Common Mode Voltage	0.05	1.25	2.35	V
V_{IDIFF}	LVDS input Differential Voltage	100	350		mV
V_{IL}	Low level input voltage	-0.3		0.8	V
V_{IH}	High level input voltage	2		D_{VDD+}0.3	V
V_{OL}	Low level output voltage			0.4	V
V_{OH}	High level output voltage	2.925			V
I_{IL}	Low level input current			12	mA
I_{IH}	High level input current			12	mA
I_{OL}	Low level output current			10	uA
I_{OH}	High level output current			10	uA

Operation theory.

- **Charge sensitive input module.**



Each channel in the OMS40G256 consists of a charge-sensitive preamplifier followed by a shaping filter (shaper) that will amplify and shape a gamma ray generated charge-signal in the CZT detector into a semi-gaussian pulse. Then, after a phase shifter, the signal path is split into two branches.

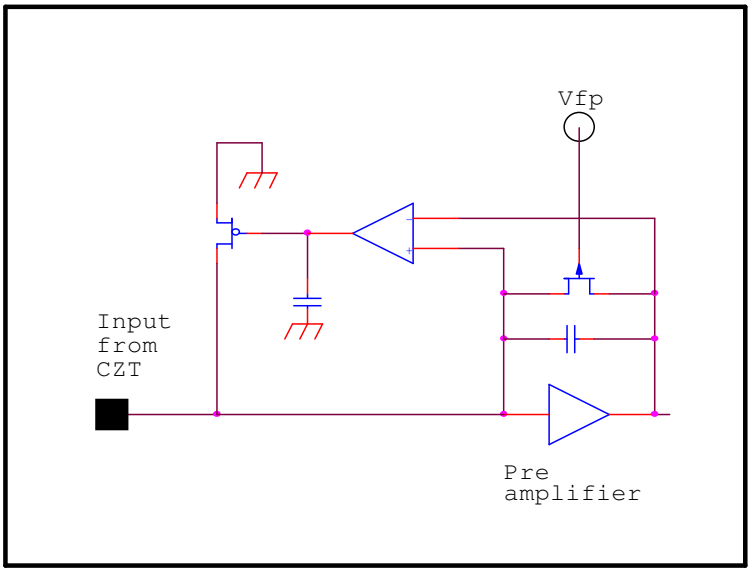
The upper branch is a stretcher that provides an (“upper-side”) envelope of the semi-gaussian pulse, followed by a track-hold device and a buffer. The stretcher is there to provide a “flat” peak of the semi-gaussian shape in order to avoid time-walk due to time-jitter on the sampling-time caused by the depth of interaction in the CZT.

The lower branch consists of a level-sensitive discriminator followed by a time-delay circuit. The discriminator compares the output pulse of the shaper with a preset (adjustable) threshold. If the signal rises above this level, the discriminator output will be high.

The discriminator output triggers the acquisition bus interface, which stores the energy and resets the channel’s energy.

All input channels have a common reset signal (RST).

An active feedback system is implemented in all channels in order to compensate for leakage current occurring in the CZT. The principle is described in the diagram below:



- **Pixel Map.**

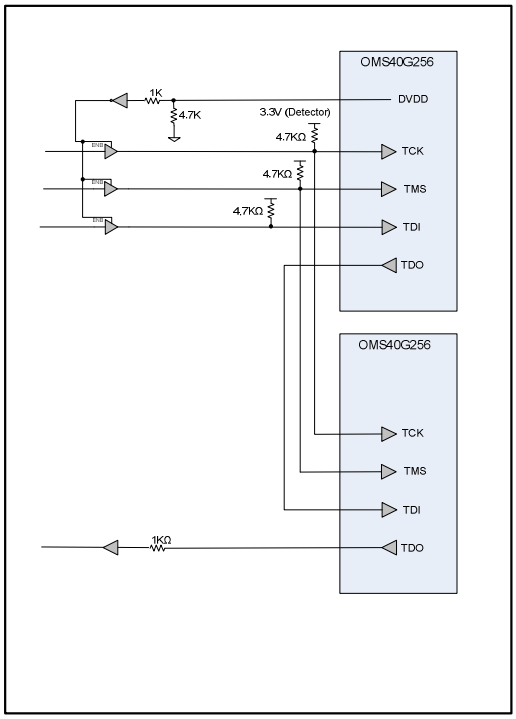
Each Channel is physically connected to one of the 256 device pixels.
The OMS40G256 though the internal implementation may have different physical mapping of the channels, the detector has a built-in conversation system providing a linear mapping for the pixels.

All pixels mapping viewed from the device CZT side. The device is oriented in such a way that the HV pin located at the upper left corner (pixel A1).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	000	001	002	003	004	005	006	007	008	009	010	011	012	013	014	015
B	016	017	018	019	020	021	022	023	024	025	026	027	028	029	030	031
C	032	033	034	035	036	037	038	039	040	041	042	043	044	045	046	047
D	048	049	050	051	052	053	054	055	056	057	058	059	060	061	062	063
E	064	065	066	067	068	069	070	071	072	073	074	075	076	077	078	079
F	080	081	082	083	084	085	086	087	088	089	090	091	092	093	094	095
G	096	097	098	099	100	101	102	103	104	105	106	107	108	109	110	111
H	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
J	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
K	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
L	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
M	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
N	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
P	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
R	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
T	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255

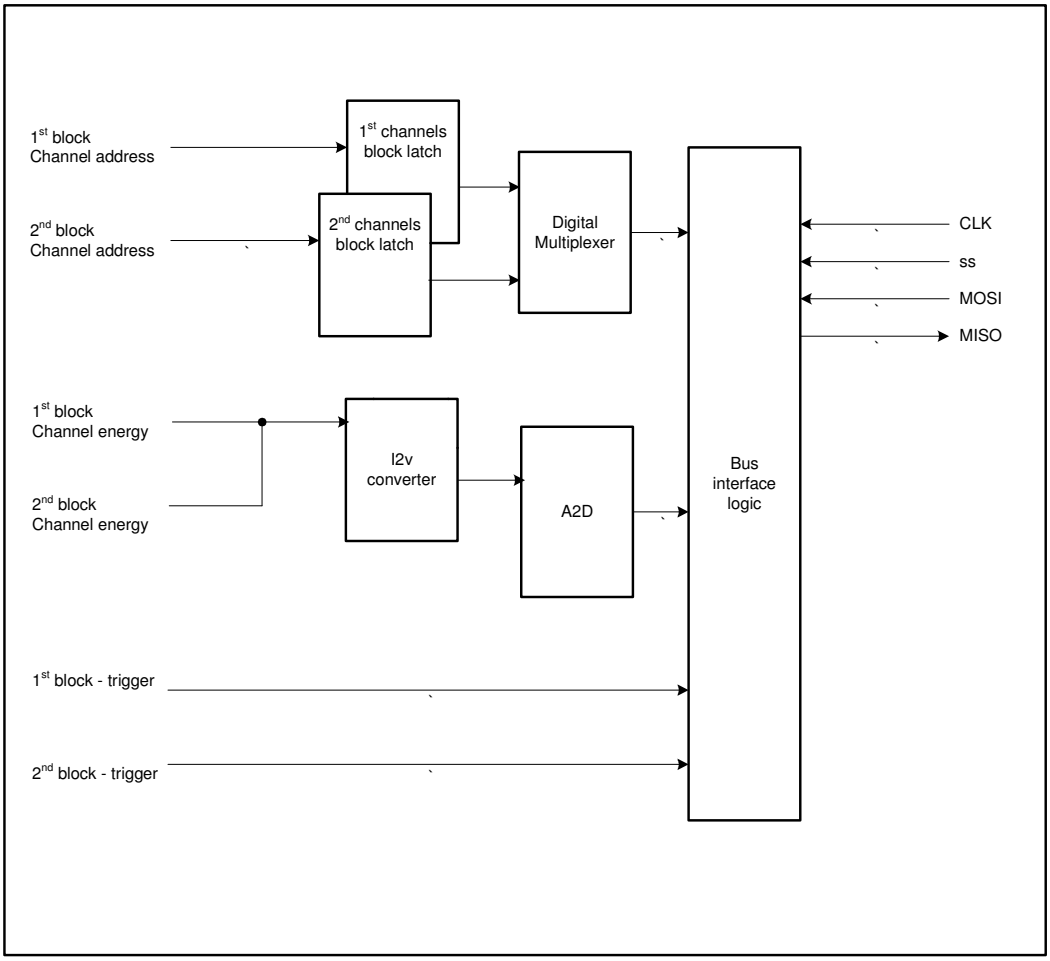
- **JTAG interface.**

The OMS40G256 provide a standard JTAG interface enabling updating the device firmware with newer versions.
The drawing below shows a typical connection circuitry to the JTAG signals, the JTAG line timing is



- **BUS interface.**

All communication between the detector and the system is done with the bus interface section; this interface supports setup, inquiring commands and photon interaction events readout.
The events readout section contains a control block, two latches and two sample and hold blocks to store events from each of the two analog channel blocks.
The analog channels in the OMS40G256 consist of two blocks of 128 channels each. Each block transfers events to the readout module.



- **BUS interface – Low level protocol.**

The BUS interface is based on SPI communication protocol, this protocol uses 4 lines to communicate. The detector is the slave while the system is the serves as the master.

SPI Signals

SS "Slave Select" signal is active low chip selecting signal. This signal controlled by the master changing it on the clock rising edge, the signal is sampled by the slave on the clock failing edge.

MOSI "Master Out Slave In" signal is a serial data input to the module, this signal is valid only when SS active. This signal controlled by the master changing it on the clock rising edge, the signal is sampled by the slave on the clock failing edge.

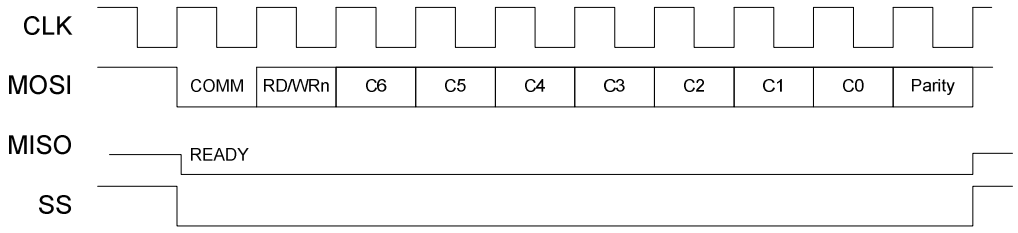
MISO "Master In Slave Out" signal is the detector serial output data. This signal controlled by the detector changing it on the clock rising edge, the signal is sampled by the master on the clock rising edge.
While the detector is not selected (SS not active) the detector does not drive this signal (Tri-State).

CLK A continues CLK signal drives the detector communication as well as other detector functions, this signal must run continuously (even when the communication is idle).

Parameter	Symbol	Min	Max	Unit
CLK frequency	FCLK	10	30	MHz
SS to CLK failing edge	SSSU	2.5		nS
MOSI to CLK failing edge	MOSISU	2.5		nS
Hold time from SS to CLK failing edge	SSHD	7.5		nS
Hold time from MOSI to CLK failing edge	MOSIHD	7.5		nS
SCLK to MISO delay	MISOD		16	nS

The master (system) controls the SPI bus and sends instructions to the slave (detector), every instruction start with command cycle, then data read or write cycle if needed. The detector also support event read cycle which is similar to the data read cycle but with a different length.

Command cycle.



The command cycle is 10 bit in length; it starts at the falling edge of SS.
The command cycle always starts with a '0' on the first bit to sign a command cycle.
The second bit defines the direction (Read or write) of the command to follow:

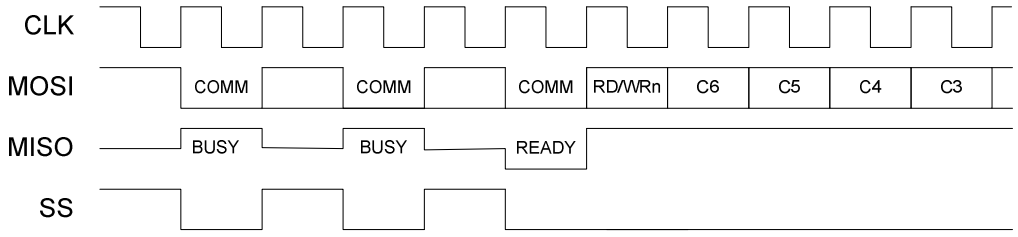
'0' = write.
'1' = read.

Then a 7 bits command ID is transmitted.
The last bit is an event parity bit (the numbers of ones in the command is always even).
Following the 10 command bits the SS signal must rise for at least one clock.

Ready / Busy indication.
At the command starts (Failing edge of SS) the slave sends ready/busy signal to the master on the MISO line.

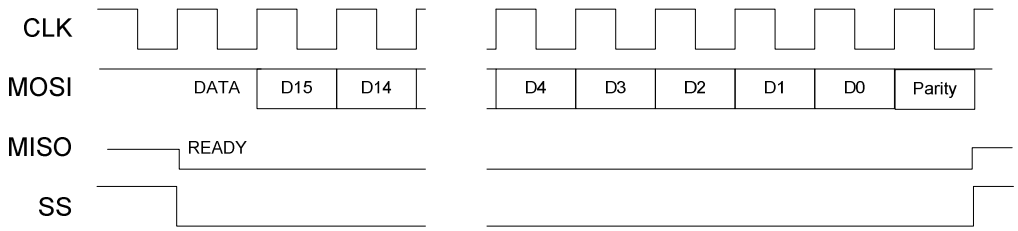
If MISO is '0' then the slave is ready for received the command.
If MISO is '1' the slave is still busy with the previous instruction.

In the case of busy, the master should stop the cycle by pulling up the SS signal high for at least one clock and try again later. In some commands, the master is allowed to continue even though the detector is busy (Beak command as an example) – this is mentioned specifically in those commands.



Please note that while the device is in the event read mode, the ready/busy indication will get the functionality of event exist flag and therefore can not be used – instead, the read status command can be used.

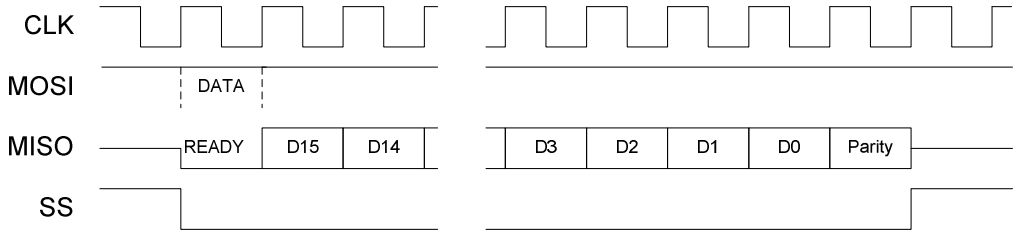
Data write cycle.



The data write cycle is 18 bit length; it starts at the falling edge of SS.
The command cycle always starts with a '1' on the first bit to sign a data cycle.
The next 16 bits are the data (MSB first)
The last bit is an event parity bit (the numbers of ones in the command is always even).
Following the 18 bits the SS signal must rise for at least one clock.

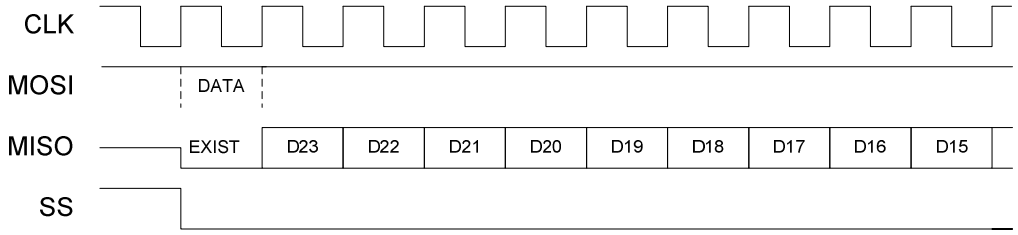
The master should check and handle BUSY situation (please refere to command cycle for more information).

Data read cycle.



The data read cycle is 18 bit length; it starts at the falling edge of SS.
The master should set MOSI to '1' for the first bit to sign a data cycle.
The first bit on MISO is '0' when date is ready. Some instructions takes time to prepare the data, in case the data is not read yet, a busy signal (MISO='1') will be transmitted, that until the detector will complete the data preparation.
The master should abort the command by releasing SS and initiate again.
The next 16 bits are the data.
The last bit is an event parity bit (the numbers of ones in the command is always even).
Following the 18 bits the SS signal must rise for at least one clock.

Event read cycle.



Event read cycle is constructed the same as data read cycle, except that the cycle is 26 bit in length and the event data is 24 bit long.
8 MSB are channel address, the next 12 bits are event energy. Additional 4 reserved bits added for future use.
The last bit is an event parity bit (the numbers of ones in the command is always even).
Following the 26 bits the SS signal must rise for at least one clock.
The cycle starts with an "exist" bit, if this bit value is '1' then the detector does not have any stored events and the master should abort the event read command.
To allow event readout, the event read mode should be activated – please refer to the protocol commands section for further information.

Normally, while the module is in “event read mode”, the module does not handle other commands, however, these is an option to send other commands to the module during this mode. During this mode, the ready/busy flag will get the functionality of event exist flag. Then, when in event read mode, the master should use the read status command instead of using the ready/busy bit. In addition, data read and write cycles can be initiated only while the detector does not have events stored.

If the module is **not** in "events read mode" and the module is not in hold state (for further information please refer to the protocol), then events received by the module will be written to an internal FIFO.

Commands list.

Command	Description
Information.	
E0H-E9H	Read part number
9DH	Read serial number (lower part)
9EH	Read serial number (Higher part)
86H	Read Firmware version
A**3**H	Read Module version
96H	Read status
9AH	Read temperature
Configuration and Control	
02H	Break
85H	Event mode on
05H	Event mode off
8CH	FIFO clear
21H	Set Energy threshold
A1H	Read Energy threshold
1FH	Set GPIO signal mode
9FH	Read GPIO signal mode
20H	Set Clock frequency
A0H	Read Clock frequency
81H	Restore previous setup
01H	Update stored setup
32H	Update Peaking time
B2H	Read Peaking time
34H	Run self test
B4H	Read self test results
Channels control.	
07H	Set channel number
87H	Read selected channel number
0BH	Enable/Disable the selected channel
8BH	Read Enable/Disable status of the selected channel

Commands – Detailed.

E0H-E9H – Read part number.
Those instructions returns the module part number (A 20 characters string), each command return 16bits (two characters) E0H returns the first two characters while E9H returns the last two characters. Command data: None. Reply data: 16bits representing two characters of the module part number, the first character is located in the 8 LSB.

9DH – Read Serial number (lower part)
This instruction returns 16 LSB of module serial number (32 bits). Command data: None. Reply data: 16 LSB of serial number

9EH – Read Serial number (Higher part)
This instruction returns 16 MSB of module serial number (32 bits). Command data: None. Reply data: 16 MSB of serial number

86H – Read Firmware version.
This command returns the Detector firmware version. None. Command data: Reply data: 8 bits – Firmware version.

A3H – Read Module version
This command returns the module hardware version. None. Command data: Reply data: 8 bits – Firmware version.

96H – Read device status.

Returns the OMS36G256 current device status.

Command data: None.
Reply date: A word, holding the current device status:

Bit	Description
0	Ready/Busy
1	Events FIFO not empty
2	Events FIFO full (To clear this bit, FIFO clear command must be issued).
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Events read mode is ON
9	Reserved
10	GPIO input state.
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Parity Error – This bit is set when a parity error is detected while receiving, the bit is cleared by reading the status command or by BREAK command.

9A - Read Temperature (Optionally on some models)

Returns the temperature measured on the detector heat-sink.

Command data: None.
Reply data: 8 bits, signed number returning the temperature in Degrease Celsius.
While in Event read mode, a 1mSec delay should be added between the command and the data read cycle, otherwise a pervious temperature measurement will be returned.

02H – Break
This command stops all currently activated processes, exit from event read mode, reset the FIFO and release module HOLD. Command data: None. Reply data: None.

85H – Event mode ON
This command sets the detector event mode on, it update the internal circuitry if needed on any change done to the configuration. In this mode the device allow event data to be read out. Command data: None. Reply data: None.

05H – Event mode OFF
This command exits from event read mode. Command data: None. Reply data: None.

8CH – FIFO Clear.
This command clears the internal events FIFO. Command data: None Reply data: None

21H – Set energy threshold.

This command sets the events energy threshold.

Command data: A linear value defining the device energy threshold.

value	Energy
0	0 Kev
1023	200 Kev (Full scale)

Reply data: None

The default value is 40kev

A1H – Read energy threshold.

This command reads the events energy threshold.

Command data: None

Reply data: Energy value (10 bits)

1FH – Set GPIO signal mode

This command define the function of GPIO port

Command data: A number defining the GPIO function:

Value	Function
0	General purpose input pin – read by status command
1	Events disable input.
2	FIFO not empty output
4	General purpose output – low state
5	General purpose output – high state
6,7	Reserved

Reply data: None.

9FH - Read GPIO signal mode

Returns the function of GPIO port.

Command data: None.
Reply data: See perverse command.

20H – Sets clock frequency.

Sets the detector clock frequency – The system must define the operating clock frequency for proper event readout operation.

Command data: Operating frequency.

Value	Frequency
6	30MHz
5	25MHz
4	20MHz
3	15MHz
2	10MHz

Reply data: None.

A0H – Read the current clock setting.

This command returns the current operating clock settings.

Command data: None.

Reply data: Clock setting in the same format as in “Sets clock frequency” command.

81H – Restore previous setup.

This command restores the detector setup as it was updated using “Update stored setup” command – All modification since the last update command will be cleared

Command data: None.

Reply data: None.

01H – Update stored setup.

This command update the detector non volatile memory with the currently detector setup. This setup will be used at the default when powering up the detector.

Command data: None.

Reply data: None.

32H – Sets Peaking time.

Sets the detector Peaking time –

Command data:

Value	time
0	1.33us
1	1us
2	0.8us
3	0.66us
4	0.57 us
5	0.5us
6	0.44us
7	0.4us

Reply data: None.

The default peaking time is 1.33us(0)

B2H – Read the Peaking time.

This command returns the Peaking time.settings.

Command data: None.

Reply data: Return value 0 to 7 (see perverse command)

34H – Run self test

The command starts run the self test process.
The self test takes less then 3 seconds (for 30Mhz clock).
The result is in the test results register.
Any command that arrived while self test is running, will return busy signal.

Command data: None.

Reply data: None.

B4H – Read tests results.

The command return the self test results

Command data: None.

Reply data: Bit 0 – shift parameters done. 0= OK, 1=fail.
Bit 1 – reserved.
Bit 2 – self test results 0=OK, 1= fail.
Bits 7:3 – reserved.

Bits 15:8 – return the number of the fail pixel in self test in case of fail.

07H – Set channel number.

This command Sets the current channel number to be effected by the channel specific commands.

Command data: Channel number (0-255).

Reply data: None.

87H – Read selected channel number.

This command returns the currently selected channel number to be effected by the channel specific commands.

Command data: None.

Reply data: Channel number (0-255).

0BH – Enable/Disable the selected channel

This command enables or disables the selected channel.

Command data: 0 = Channel enabled.
1 = Channel Disabled.

Reply data: None.

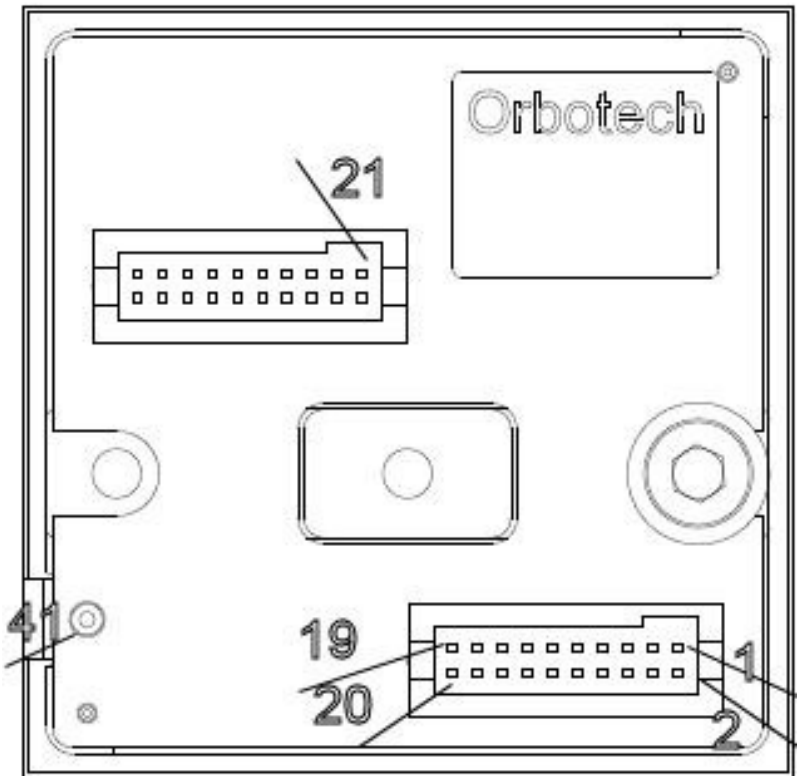
8BH – Read Enable/Disable status of the selected channel.

This command returns the selected channel enable/disable status.

Command data: None.

Reply data: 0 = Channel enabled.
1 = Channel Disabled.

Detector pin-out.

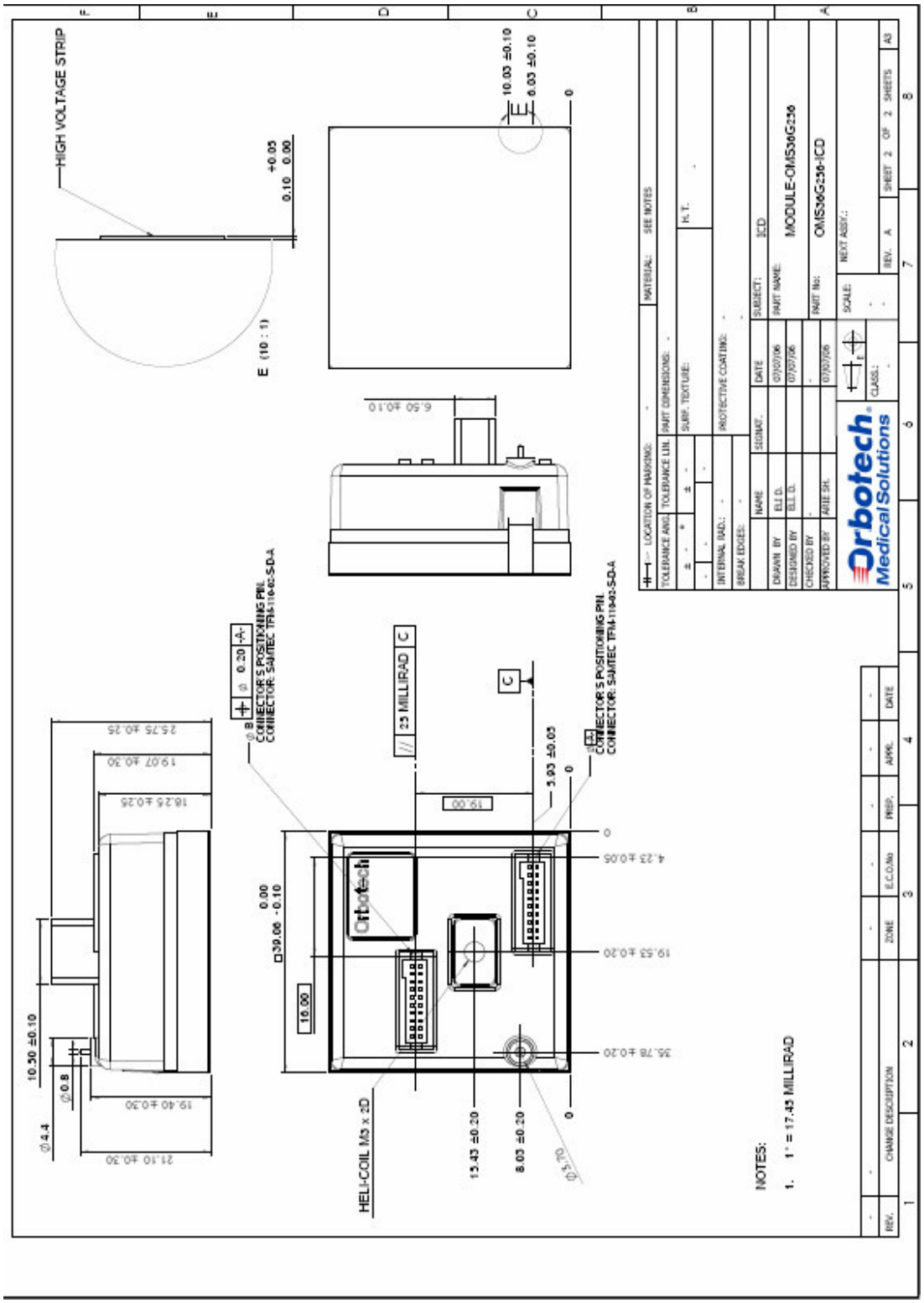


- **Multi-pin connector**
  SAMTEC SFM-110-02-S-D-A or equivalent.

- **HV Connector**
  MILL-MAX 0284-0-15-01-16-27-10-0 or equivalent.

  - The cooling finger should be electrically isolated from the system ground

Mechanical dimensions.



Containing PCB suggested dimensions