ECE 592
Project 3 Report
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The two protocols FBV and SSCI give the same results as the implementation is same for both. We see that when we increase the Cache size keeping the block size same the miss rate decreases and so does the number of writebacks occurring.
When we increase the block size the miss rate decreases and so does the number of writebacks.

**Comparison between SSCI and FBV:**
Memory:
The SSCI protocol seems more complex but it will save on the amount of pre-allocated memory. If there are no sharers there will be no memory allocated in the list whereas for FBV the memory will still be allocated with bit values=FALSE.

Speed:
The speed of the two cannot be compared here at software level, but maybe at hardware level FBV will be faster, since memory is pre-allocated and the hardware just has to change the states of the memory.
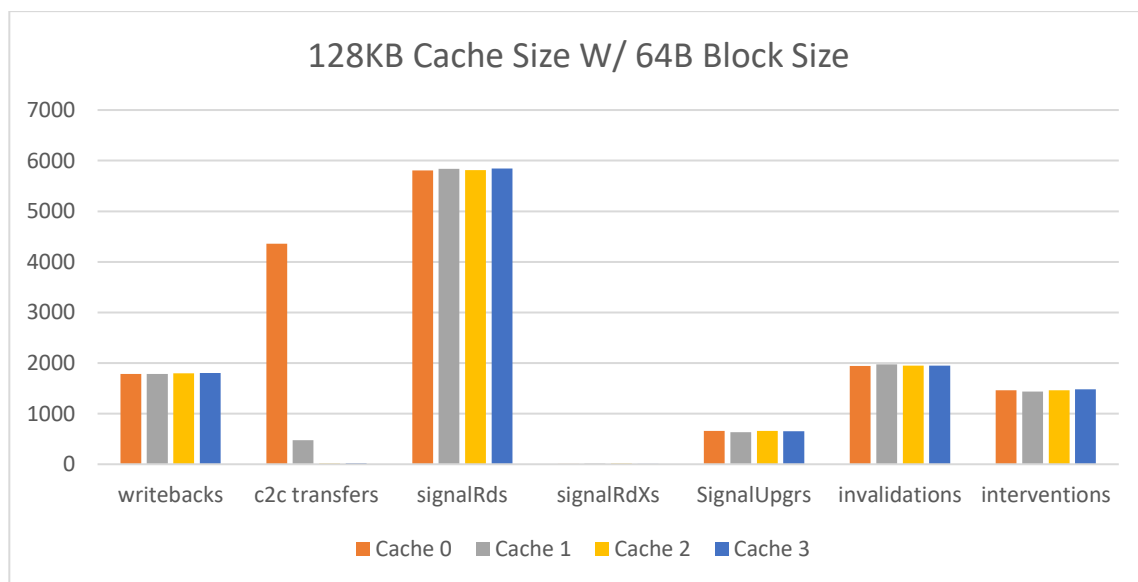
Altering Cache Size:

32KB Cache Size W/ 64B Block Size	Cache 0	Cache 1	Cache 2	Cache 3
Reads	112661	110830	114938	113428
read misses	6361	6391	6382	6404
writes	11942	11710	12383	12108
write misses	39	41	42	39
total miss rate	0.051363	0.052489	0.050455	0.051324
writebacks	2124	2087	2135	2185
c2c transfers	4751	1623	48	55
signalRds	6361	6391	6382	6404
signalRdXs	39	41	42	39
SignalUpgrs	674	650	674	662
invalidations	2014	2034	2008	2020
interventions	1574	1539	1586	1624
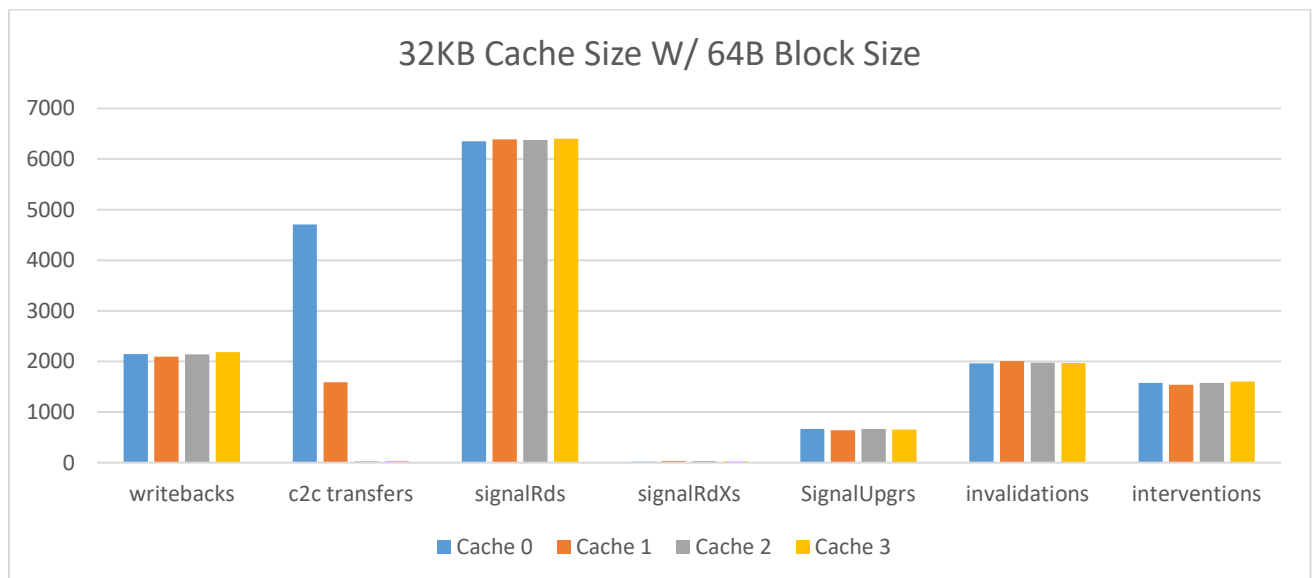
32KB Cache Size W/ 64B Block Size

64KB Cache Size W/ 64B Block Size		Cache 0	Cache 1	Cache 2	Cache 3
reads		112661	110830	114938	113428
read misses		6044	6063	6044	6070
writes		11942	11710	12383	12108
write misses		39	41	42	39
total miss rate		0.048819	0.049812	0.0478	0.048663
writebacks		1976	1952	1994	2043
c2c transfers		4564	1553	49	57
signalRds		6044	6063	6044	6070
signalRdXs		39	41	42	39
SignalUpgrs		674	650	674	662
invalidations		2014	2034	2008	2020
interventions		1505	1487	1519	1558

64KB Cache Size W/ 64B Block Size
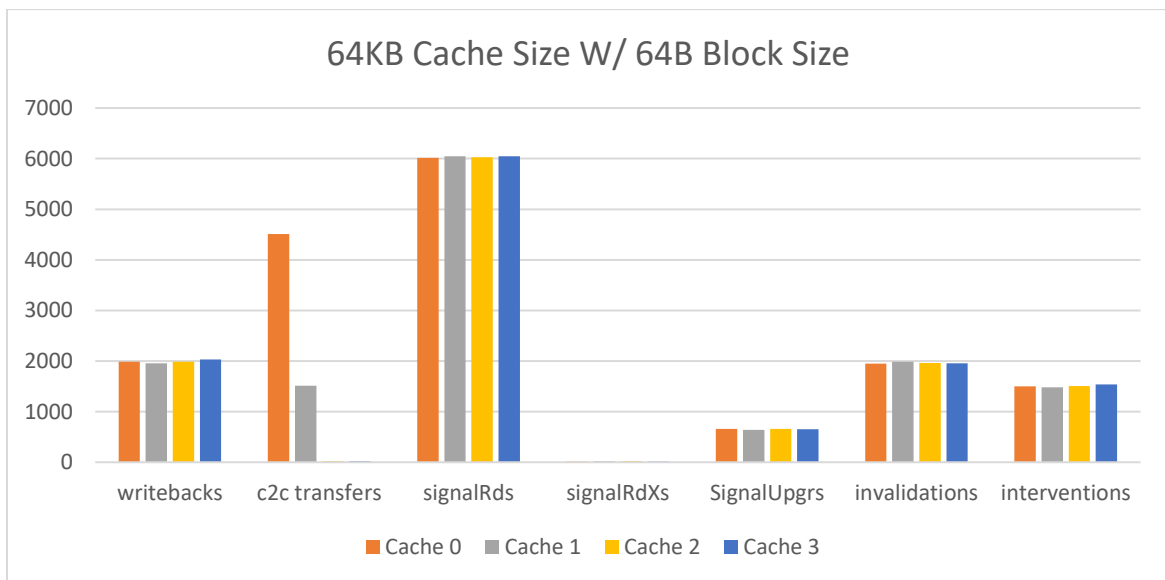
128KB Cache Size W/ 64B Block Size	Cache 0	Cache 1	Cache 2	Cache 3
reads	112661	110830	114938	113428
read misses	5842	5865	5837	5879
writes	11942	11710	12383	12108
write misses	39	41	42	39
total miss rate	0.047198	0.048197	0.046175	0.047142
writebacks	1786	1790	1810	1829
c2c transfers	4424	1519	53	58
signalRds	5842	5865	5837	5879
signalRdXs	39	41	42	39
SignalUpgrs	674	650	674	662
invalidations	2014	2034	2008	2020
interventions	1471	1447	1479	1503

256KB Cache Size W/ 64B Block Size	Cache 0	Cache 1	Cache 2	Cache 3
reads	112661	110830	114938	113428
read misses	5775	5805	5771	5813
writes	11942	11710	12383	12108
write misses	39	41	42	39
total miss rate	0.04666	0.047707	0.045656	0.046616
writebacks	1609	1575	1627	1625
c2c transfers	4372	1510	56	64
signalRds	5775	5805	5771	5813
signalRdXs	39	41	42	39
SignalUpgrs	674	650	674	662
invalidations	2014	2034	2008	2020
interventions	1468	1432	1469	1479
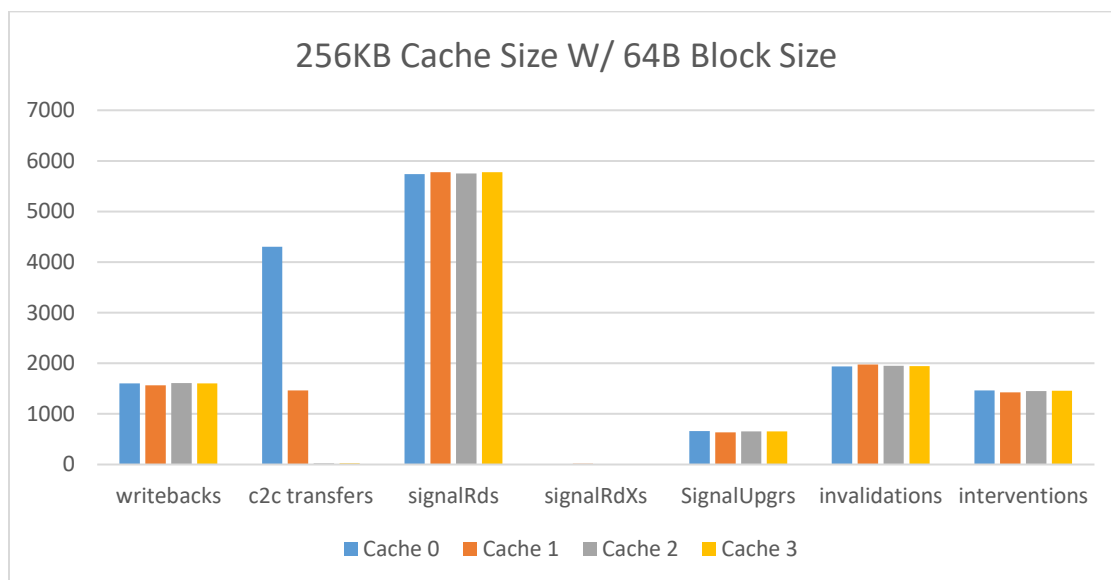
256KB Cache Size W/ 64B Block Size

512KB Cache Size W/ 64B Block Size	Cache 0	Cache 1	Cache 2	Cache 3
reads	112661	110830	114938	113428
read misses	5757	5792	5756	5796
writes	11942	11710	12383	12108
write misses	39	41	42	39
total miss rate	0.046516	0.047601	0.045538	0.046481
writebacks	1540	1507	1549	1557
c2c transfers	4359	1508	57	64
signalRds	5757	5792	5756	5796
signalRdXs	39	41	42	39
SignalUpgrs	674	650	674	662
invalidations	2014	2034	2008	2020
interventions	1466	1429	1465	1474

512KB Cache Size W/ 64B Block Size
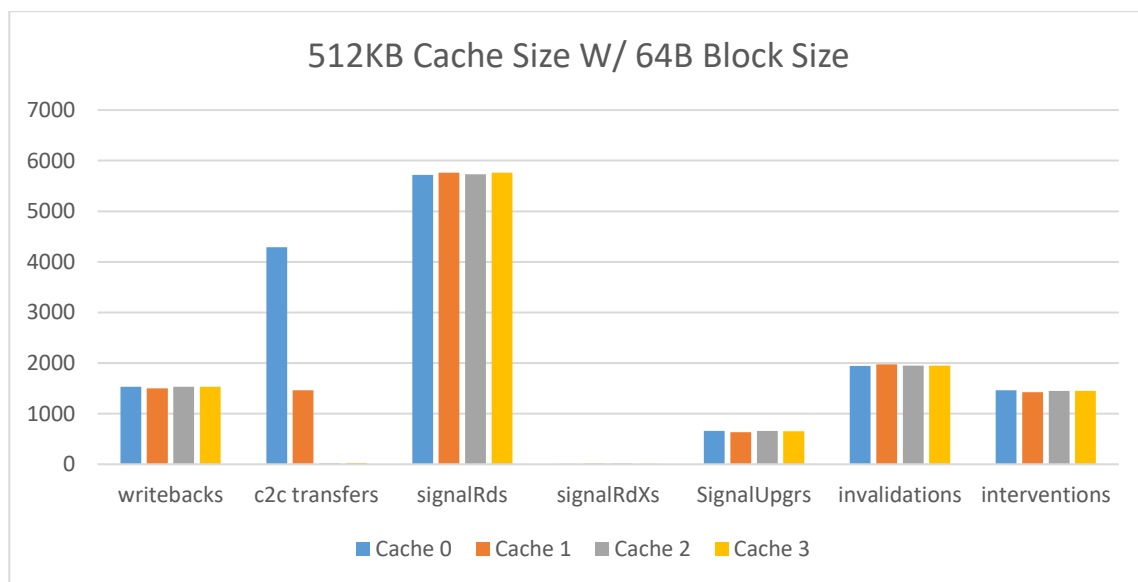
Altering Block Size:

64B Block Size W/ 1MB Cache Size				
	Cache 0	Cache 1	Cache 2	Cache 3
reads	112661	110830	114938	113428
read misses	5752	5781	5752	5790
writes	11942	11710	12383	12108
write misses	39	41	42	39
total miss rate	0.046476	0.047511	0.045507	0.046433
writebacks	1518	1490	1529	1542
c2c transfers	4356	1507	57	64
signalRds	5752	5781	5752	5790
signalRdXs	39	41	42	39
SignalUpgrs	674	650	674	662
invalidations	2014	2034	2008	2020
interventions	1464	1428	1464	1474
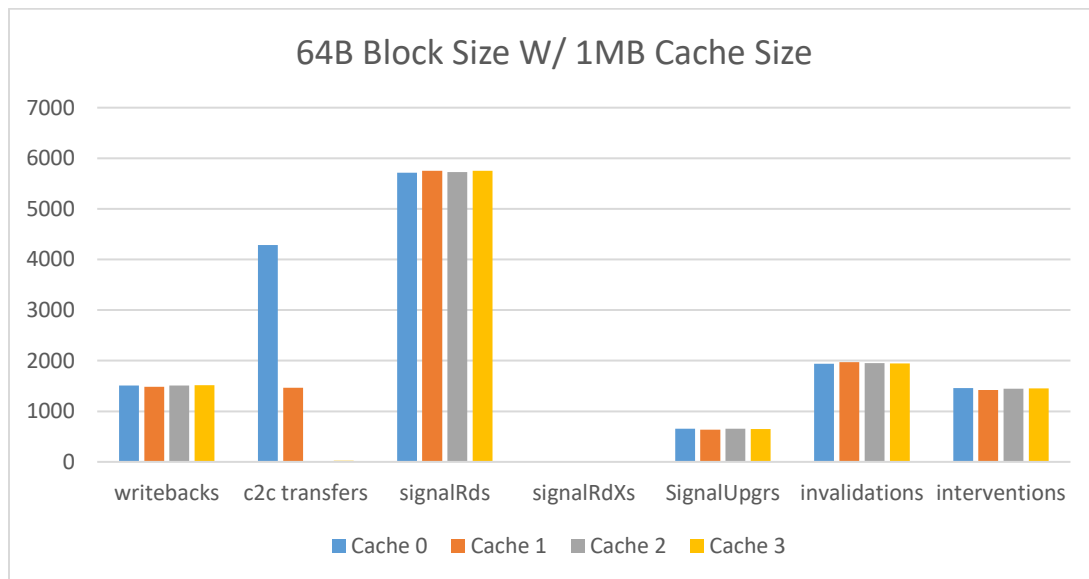
128B Block Size W/ 1MB Cache Size				
	Cache 0	Cache 1	Cache 2	Cache 3
reads	112661	110830	114938	113428
read misses	5340	5386	5341	5384
writes	11942	11710	12383	12108
write misses	39	40	42	39
total miss rate	0.043169	0.044279	0.042279	0.043199
writebacks	1478	1458	1494	1519
c2c transfers	4071	1413	65	71
signalRds	5340	5386	5341	5384
signalRdXs	39	40	42	39
SignalUpgrs	688	663	695	682
invalidations	2066	2089	2053	2068
interventions	1367	1337	1377	1385
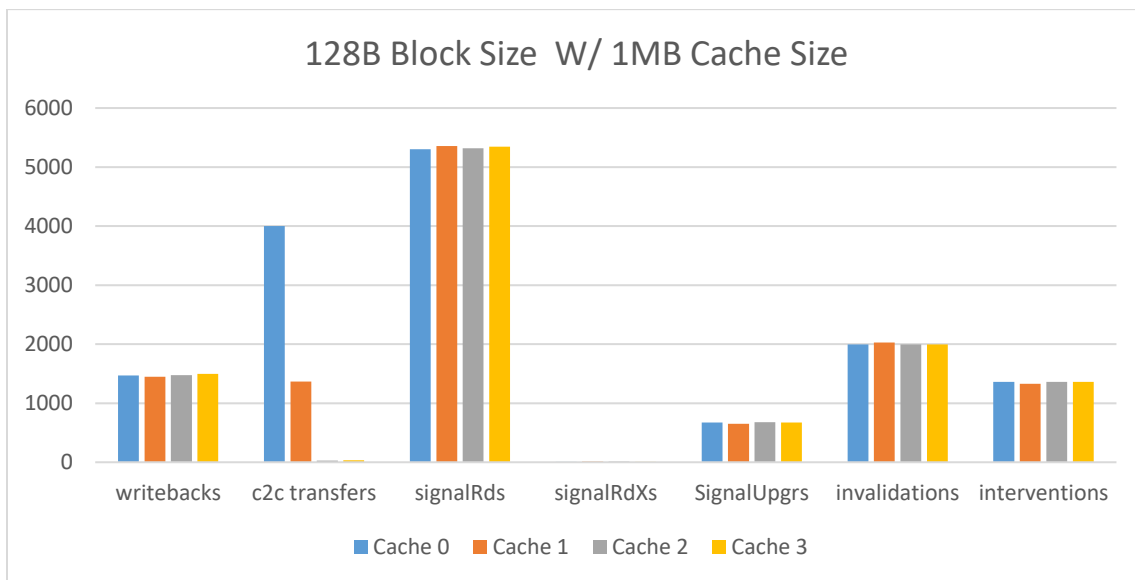
256B Block Size W/ 1MB Cache Size				
	Cache 0	Cache 1	Cache 2	Cache 3
reads	112661	110830	114938	113428
read misses	5023	5070	5004	5084
writes	11942	11710	12383	12108
write misses	39	40	42	39
total miss rate	0.040625	0.041701	0.039632	0.040809
writebacks	1435	1448	1473	1471
c2c transfers	3858	1336	76	81
signalRds	5023	5070	5004	5084
signalRdXs	39	40	42	39
SignalUpgrs	710	687	731	692
invalidations	2131	2157	2107	2148
interventions	1283	1284	1321	1309

256B Block Size W/ 1MB Cache Size