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CSEN 702: Microprocessors
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Practice assignment 1

1) Consider the following fragment of C code:

```
for (i = 0; i <= 100; i++)
{ A[i] = B[i] + C; }
```

Assume that A and B are arrays of 64-bit integers, and C and i are 64-bit integers.
Assume that all data values and their addresses are kept in memory (at addresses 1000, 3000, 5000, and 7000 for A, B, C, and i, respectively). Assume that values in registers are lost between iterations. of the loop. You might need to load value 0 in variable i.

a) Write the code for MIPS64.
b) How many instructions are required dynamically?
c) How many memory-data references will be executed?
d) What is the code size in bytes?

2) Of the three factors in the equation:

(*EXECUTION TIME CPU = Number of instructions * CPI * Cycle Time*)

Which is most influenced by?
(a) The technology
(b) The compiler
(c) The computer architecture

3) When running an integer benchmark on a RISC machine, the average instruction mix was as follows:

Instructions	Average Frequency
Load	26%
Store	9%
Arithmetic	14%
Compare	13%
Cond. branch	16%
Uncond. branch	1%
Call/returns	2%
Shift	4%
Logical	9%
Other (Misc.)	6%

Note than an unconditional Branch is a jump. Also calls and returns are jumps. The following measurements of average CPI for individual instruction categories were made:

Instruction type	Average CPI (clock cycles)
All ALU instructions	1
Load–store	1.4
Taken Conditional branches	2.0
Not taken Conditional branches	1.5
Jumps	1.2

Assume that 60% of the conditional branches are taken and that all instructions in the Misc. category are ALU instructions. What is the CPI of the benchmark on this RISC machine?

4) Consider the un-pipelined processor that has a 1.2 ns clock cycle and that it uses 3 cycles for ALU operations and branches and 4 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20%, and 40%, respectively.

Suppose that due to clock skew and setup, pipelining the processor adds 0.1 ns of overhead to the clock.
How much speedup in the instruction execution rate will we gain from a pipeline? (Assume ideal pipeline without any stalls)

5) Consider a 5-stage pipelined microprocessor that has an average stalls per instruction equal to 1.5.
Calculate the speedup of this processor over its un-pipelined version.

6) We begin with a computer implemented in single-cycle implementation. When the stages are split by functionality (pipelining), the stages do not require exactly the same amount of time. The original machine had a clock cycle time of 7 ns. After the stages were split, the measured times were:
IF 1 ns;
ID 1.5 ns;
EX 1 ns; MEM
2 ns; WB 1.5
ns.
Also, the pipeline register delay is 0.1 ns.
a) What is the clock cycle time of the 5-stage pipelined machine?
b) If there is a stall every 4 instructions, what is the CPI of the new machine?
c) Calculate the speedup of the pipelined over the un-pipelined:

7) In this problem, we will explore how deepening the pipeline affects performance in two ways: faster clock cycle and increased stalls due to data and control hazards.
- Assume that the original machine is a 5-stage pipeline with a 1 ns clock cycle.
- The second machine is a 12-stage pipeline with a 0.6 ns clock cycle.
- The 5-stage pipeline experiences 1 stall due to a data hazard every 5 Instructions
- The 12-stage pipeline experiences 3 stalls every 8 instructions due to data hazards.

A) What is the speedup of the 12-stage pipeline over the 5-stage pipeline, taking into account only data hazards?

B) Assume branches constitute 20% of the instructions, and the mis-prediction rate for both machines is 5%.

If the branch mispredict penalty for the first machine is 2 cycles but the second machine is 5 cycles, what are the CPIs of each, taking into account the stalls due to branch mispredictions in addition to the data hazards stalls in part A?

C) Calculate the speedup in part B and discuss the effects.