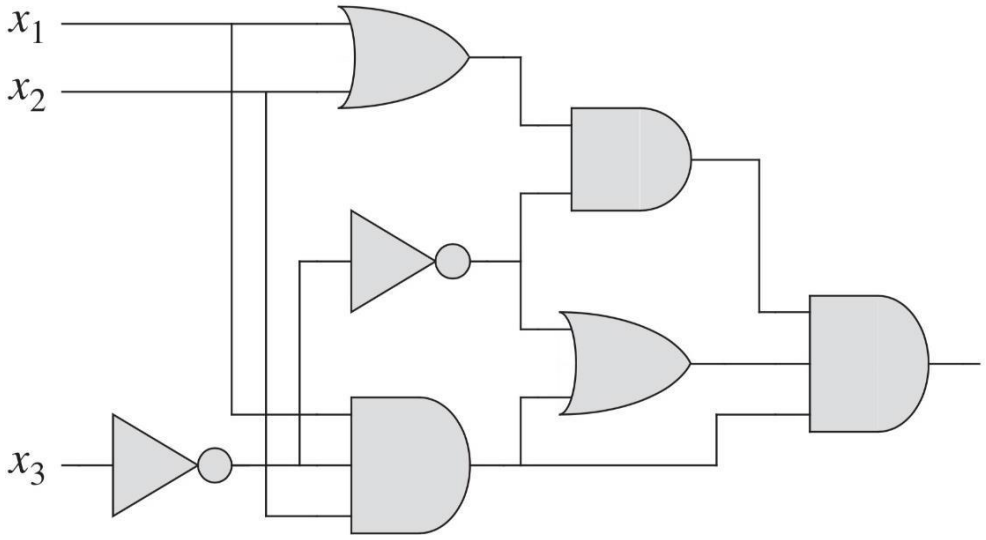
WORCESTER POLYTECHNIC INSTITUTE
ELECTRICAL AND COMPUTER ENGINEERING
ECE2029 INTRODUCTION TO DIGITAL CIRCUIT DESIGN
FALL-B-2024

Name:
Number:

Experiment 2 – Implementation of Boolean Functions and Gate-Level Minimization in Verilog

Q1) Write the Verilog code for following combinational logic.



Q2) For the function given in sum-of-minterms form,

$$F(A, B, C, D) = \Sigma(0,2,6,7,8,10,15)$$

3) Complete the truth table for all possible inputs and corresponding outputs.
4) Please, write Verilog code without simplification.

Q3) Create a 4-bit prime number detector. The circuit has four inputs-N3, N2, N1, and NO—that correspond to a 4-bit number (N3 is the most significant bit) and one output P that is 1 when the input is a prime number and that is 0 otherwise.