

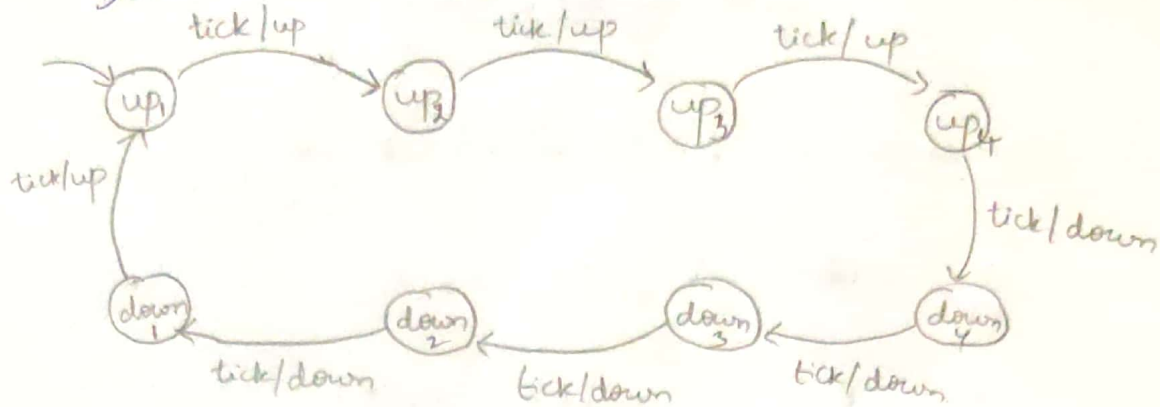
CPES FINAL EXAM SET-1

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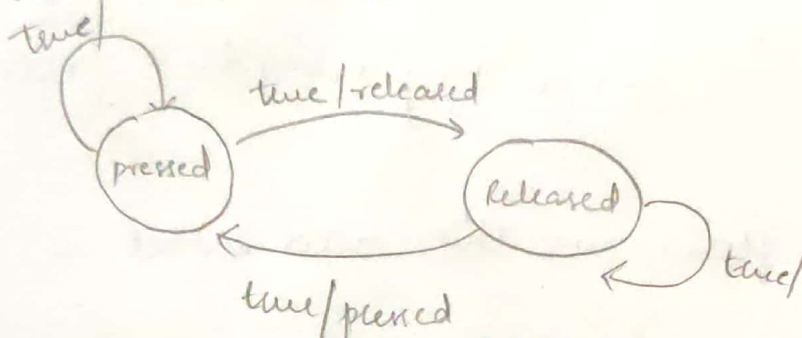
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1.)

Deterministic FSM A:-



Non deterministic FSM B:-



For deterministic FSM:- (FSM A)

states - {up, down, up₂, up₃, up₄, down₂, down₃, down₄}

Inputs - ({tick} → {present, absent})

outputs - ({up, down} → {present, absent})

initial state - up.

update (s, i) = {

- (up, up) → if s = up ∧ i(tick) = ^{up}~~present~~
- (down, down) → if s = down ∧ i(tick) = ^{down}~~present~~
- (^{down}~~up~~, up) → if s = down ∧ i(tick) = ^{up}~~present~~
- (up, down) → if s = up ∧ i(tick) = down.

~~FSM~~ For Non deterministic FSM-B

states $\rightarrow \{ \text{pressed, released} \}$

Input $\rightarrow \{ \text{tick} \} \rightarrow \{ \text{press, release} \}$

output $\rightarrow \{ \text{press, release} \} \rightarrow \{ \text{pressed, released} \}$

Input state $\rightarrow \{ \text{none} \}$.

updates $(s, i) \rightarrow$

1.) $\{ \text{released, released} \}$ of

$s = \text{pressed} \wedge i = \text{released}$

2.) $\{ \text{released, released} \}$

if $s = \text{released} \wedge i = \text{released}$

3.) $\{ \text{pressed, pressed} \}$

if $s = \text{released} \wedge i = \text{press}$.

4.) $\{ \text{pressed, pressed} \}$

if $s = \text{pressed} \wedge i = \text{pressed}$.

3.) ~~Formal model~~ ~~General model~~ Actor model (General):-

b.) Formal model (Actor model in next page)

$$y_1 = x_2(t) \Rightarrow y_1(t) = x_2(t)$$

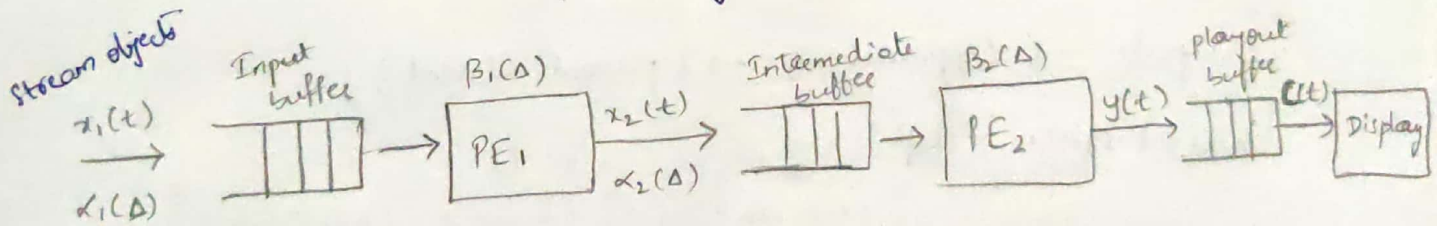
$$y_3 = x_3(t) \quad y_3(t) = x_3(t)$$

$$y_3(t) = i + \int_0^t x_1(\tau) d\tau + \int_0^t x_2(\tau) d\tau + \int_0^t x_3(\tau) d\tau$$

Data that flows in this actor model is synchronous.

a.) ~~Model~~ Model for question:-

processing is done in PE1



$$B_2(t) \geq \begin{cases} 0 & \text{if } t \leq d_1 \\ (C \circ x_2^1)(t, d) & \text{if } t > d_1 \end{cases}$$

with $d > d_1$.

states can be
input, intermediate
display, playout buffer.

Input = {Stream obj}

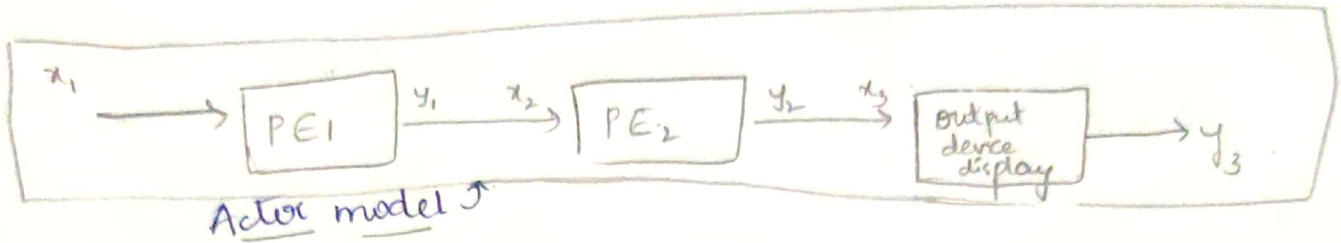
output = {processed obj}

initial states = {input buffer}

$$\therefore B_1(t) \geq (\angle_2^1 \odot \angle_1^1)(t), \forall t \geq 0.$$

payload delay redistribution.

$$C(t, d) = \begin{cases} 0 & \text{if } t \leq d \\ c(t-d) & \text{if } t > d \end{cases}$$



20)

Register bank Read1 AR2

Register bank Read2 AR3 A

ALU

AR2 A

ALU

AR3

~~1 2 3~~

~~cycles~~

register bank read1	AR2			A			
register bank read2	AR3			A			
ALU		AR2			A		
ALU		AR3			A		
ALU							
data memory			AR2*AR3				A
register bank write			AR2*AR3				A