ITWS-II

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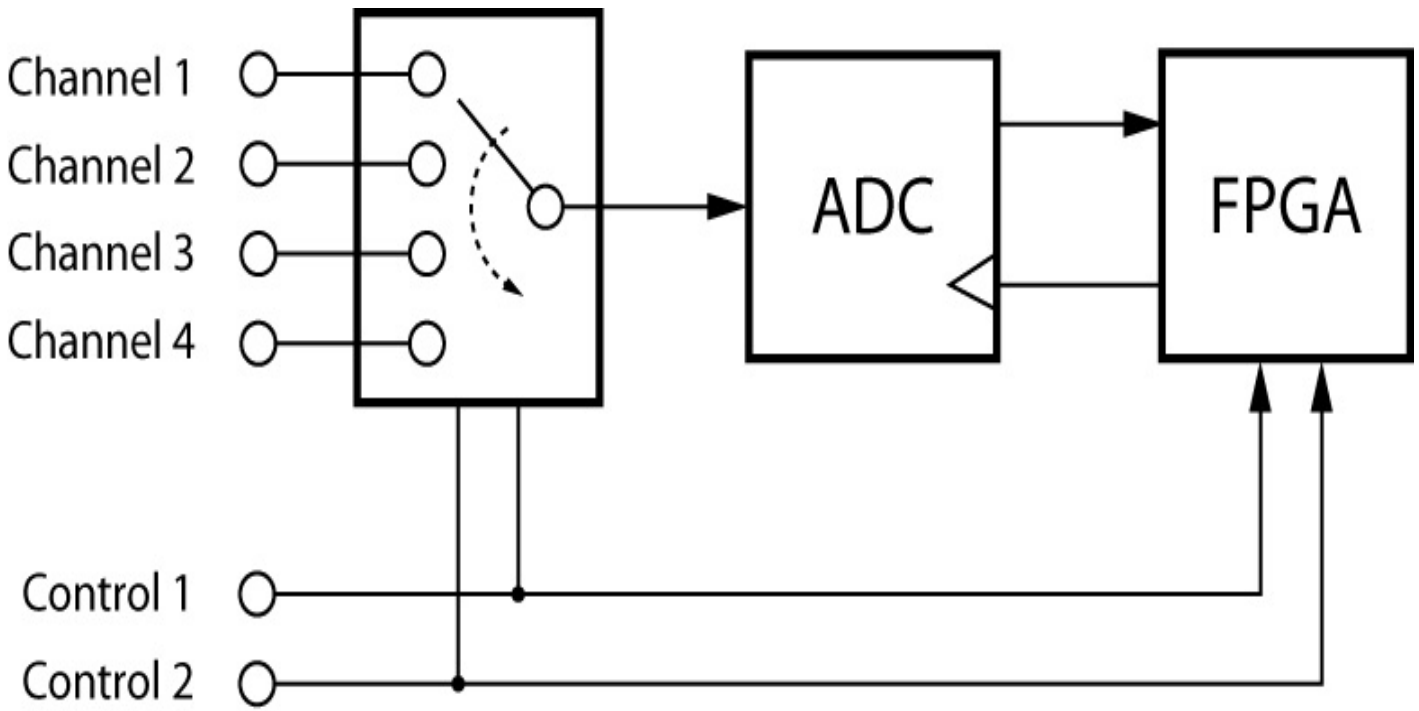
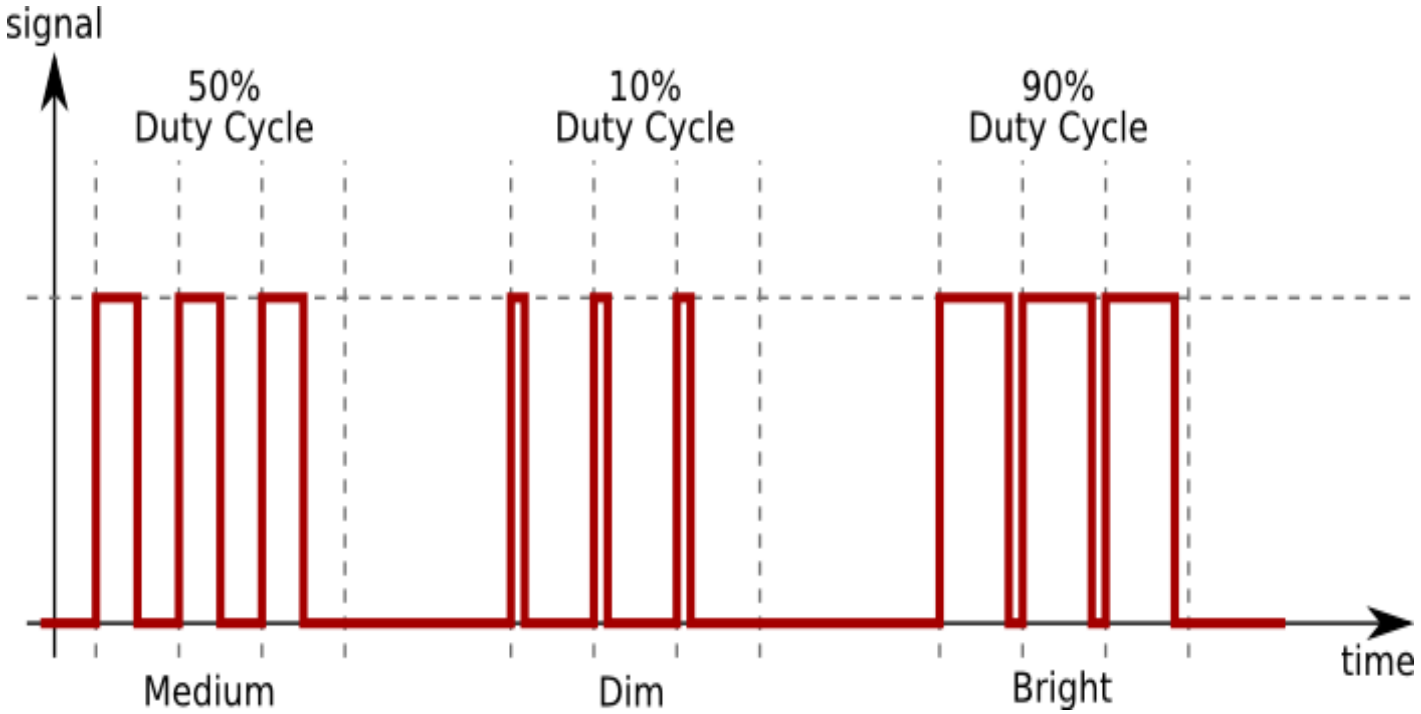
ADC with multiple inputs

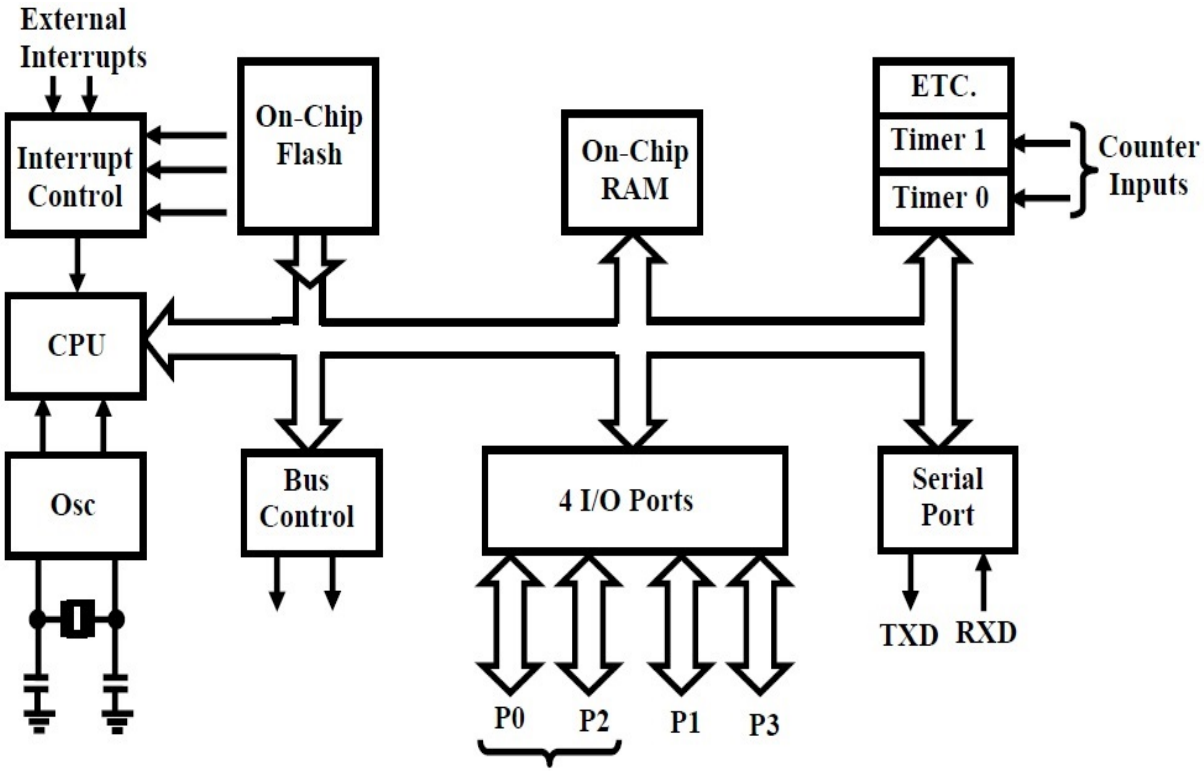


Pulse Width Modulation

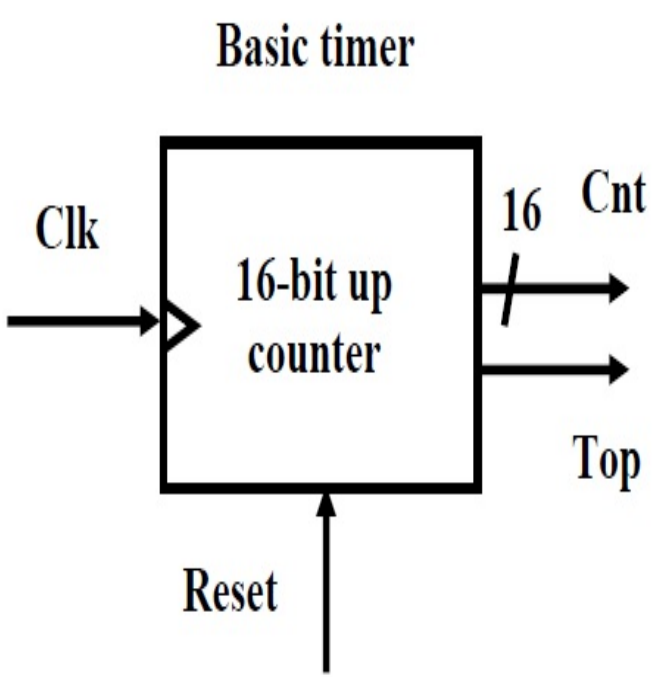


$$N = \frac{V}{K * \phi} \tag{1}$$

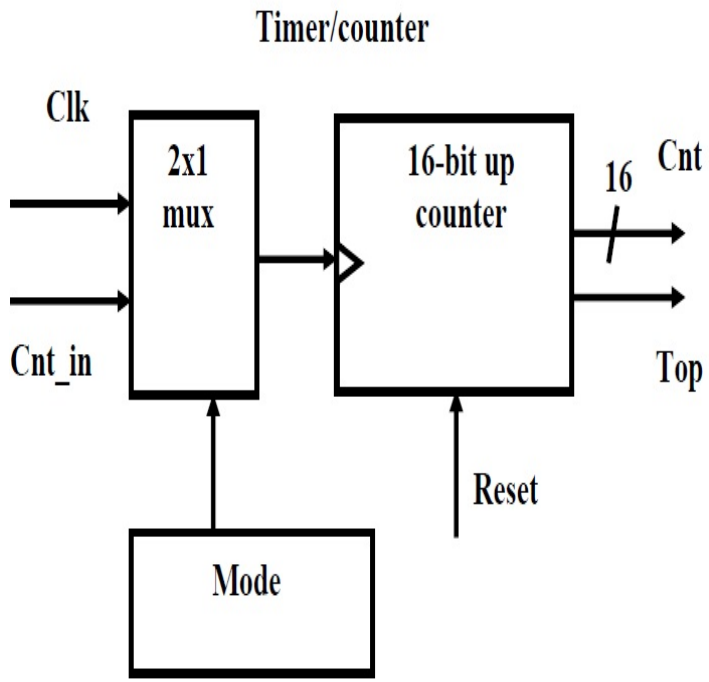
Timers


External Interrupts
Interrupt Control
On-Chip Flash
On-Chip RAM
ETC.
Timer 1
Timer 0
Counter Inputs
CPU
Osc
Bus Control
4 I/O Ports
Serial Port
TXD
RXD
P0
P2
P1
P3

Timers

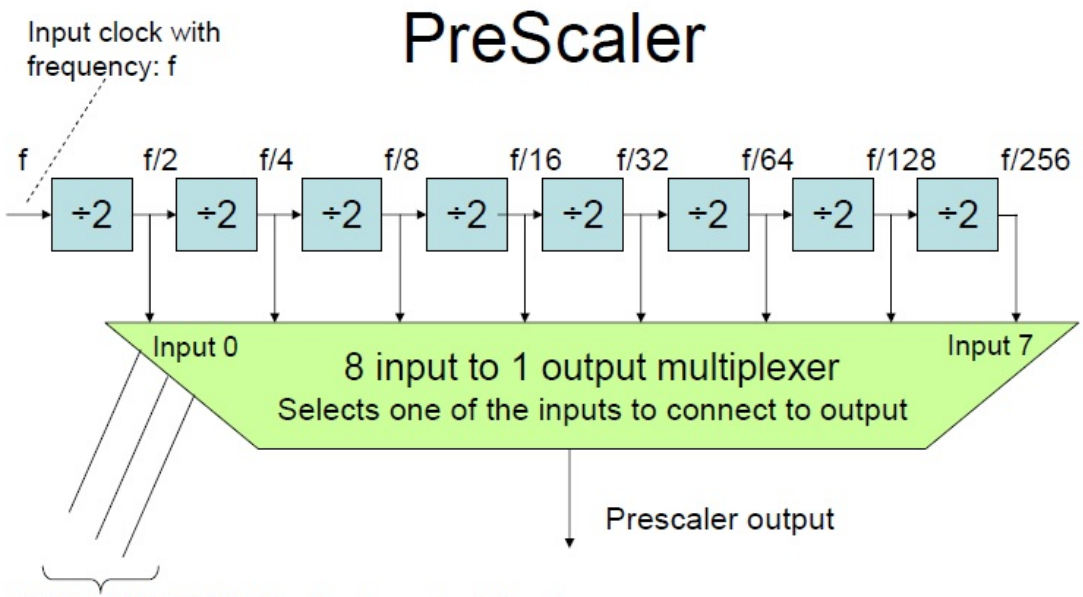

Basic timer
Clk
16-bit up
counter
16
Cnt
Top
Reset

(d)

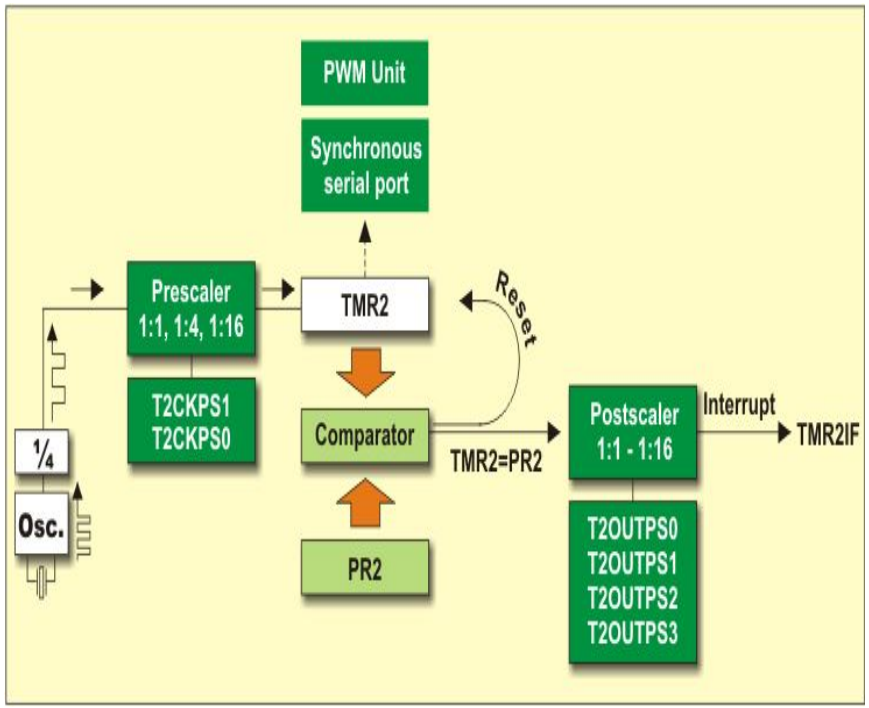

Timer/counter
Clk
Cnt_in
2x1
mux
16-bit up
counter
16
Cnt
Top
Reset
Mode

(e)

Timers - Prescaler



Timers - Postscaler



$$fout = \frac{fclk}{4 * Prescaler * (PR2\text{-}TMR2) * Postscaler * Count}$$

$$Tout = \frac{1}{fout}$$

1 second from 4 MHZ clock and prescaler of 1:1 and postscaler of 1:16 for TMR1=0 and PR2=255

count ?

BUS

- CPU Communicates with Memory and I/O using BUS
- Not just Physical wires
- Protocol for communication/transportion of signals
- Bus are shared between CPU, Memory and I/O

Definition of Bus

1. Transaction protocol
2. Timing and Signaling
3. Electrical Specifications
4. Physical and Mechanical speifications

Different Bus and Characteristics

- Address
- Data: Between source and destination
- Control: for Transaction/Transport protocol

Bus signals Tristated ?
Address and Data
Maximum Bus load - maximum devices
Increase Bus Bandwidth
1.Non multiplexed Address/Data lines
2. Increase the width of Data Bus (for word length of 16 and a bus 64 bit)
3. Block transfer - Single Address but multiple data to be sent

BUS

Differentition interms of Instruction and Data access.

- Von Neumann Architecture
- Harvard Architecture
- Modified Harvard Architecture

Von Neumann architecture

Single Bus for Instructions and Data

- Bit widths should be same for Instruction and Data
- Data Transfers and Instructions fetches should be Scheduled
- Pipelining is complex
- Early Systems

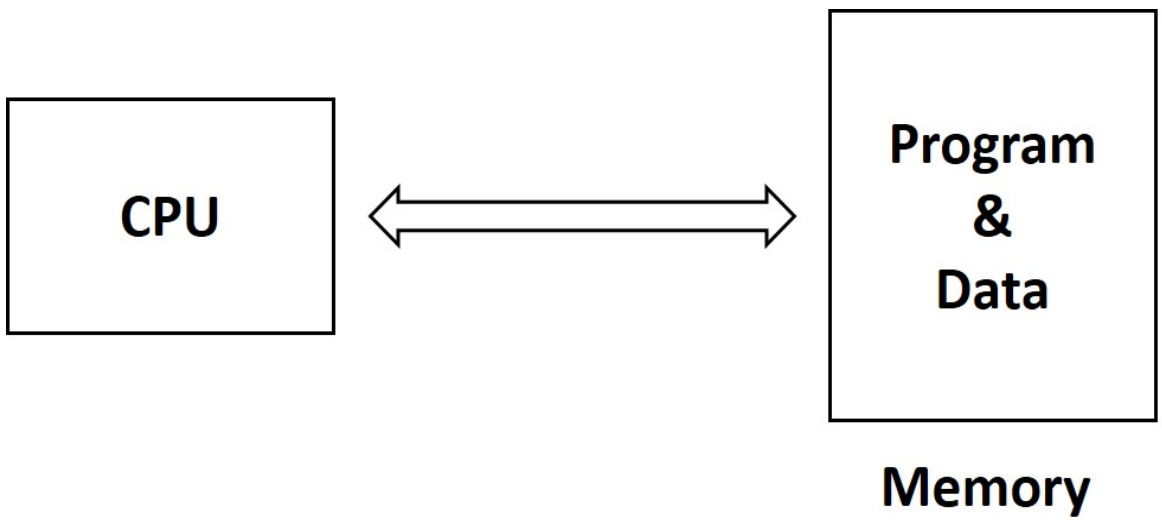


Figure: Von Nuemann Architecture

Harvard Architecture

Seperate instruction and Data buses

- Different Widths for Data and Instruction
- Simultaneous and faster operation
- Pipelining is Easier than Von Nuemann
- Most of the Modern Systems
- Examples: DSP processors, ARM, AVR, ATMEL, PIC etc.

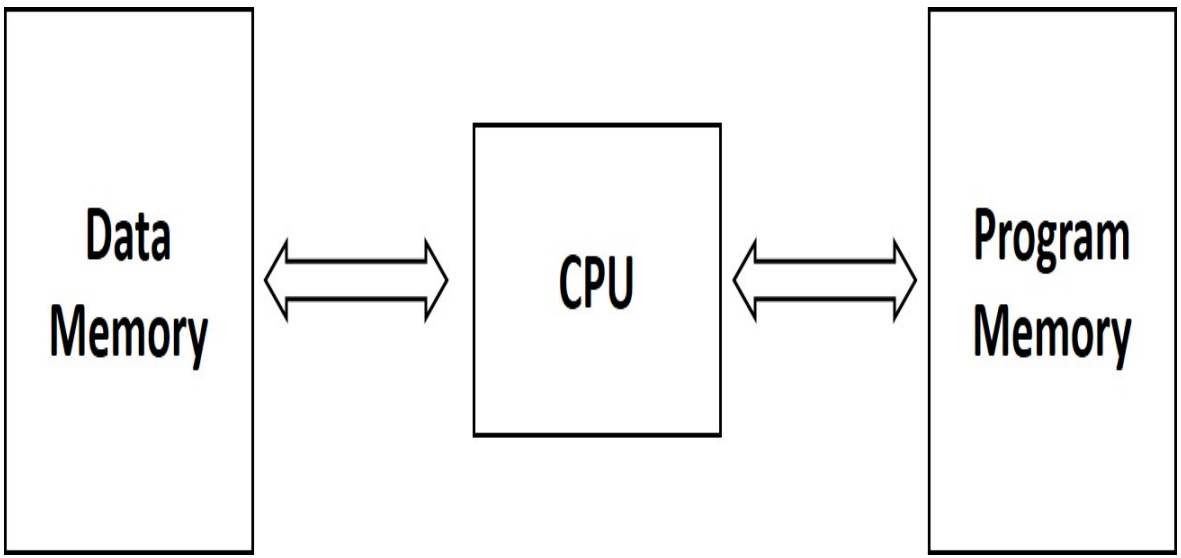
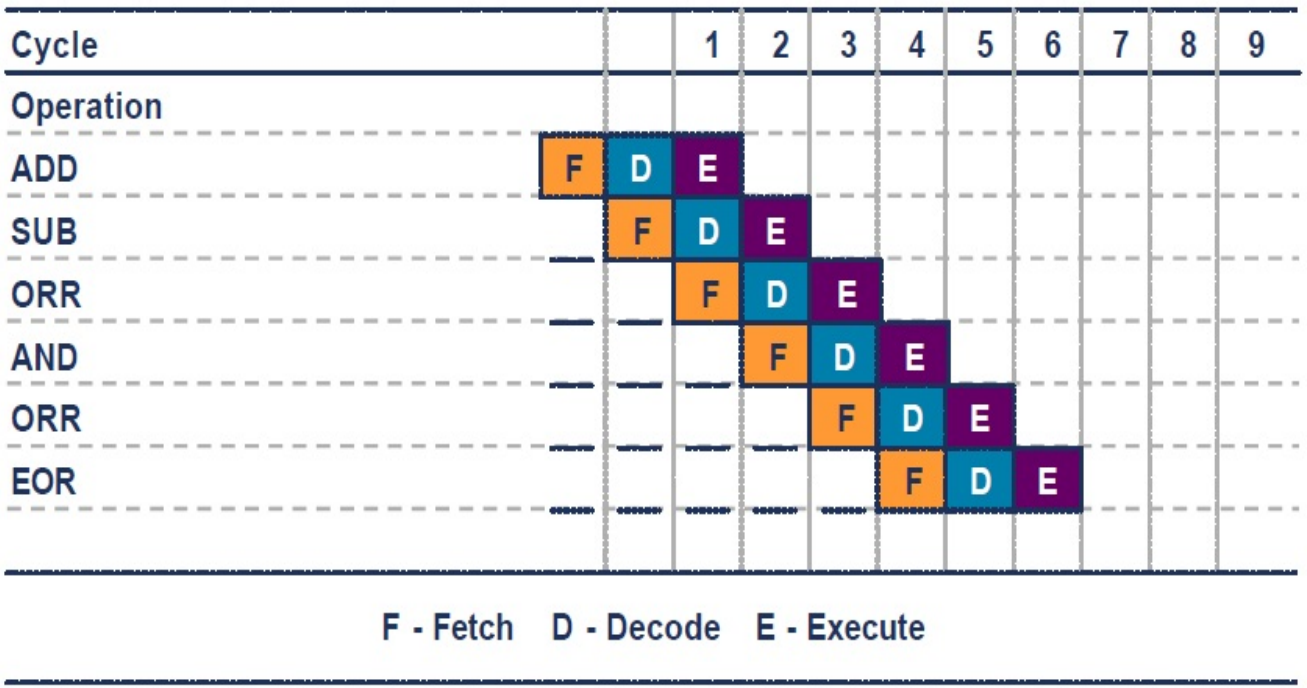


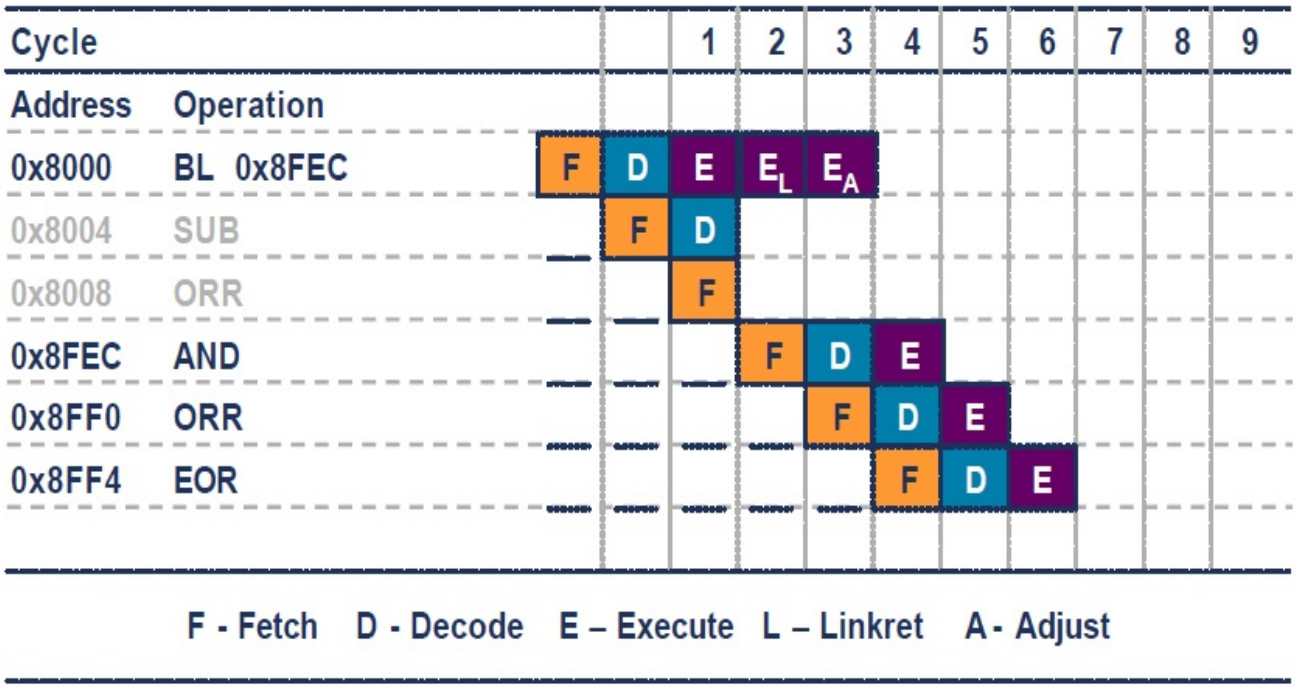
Figure: Harvard Architecture

Optimal Pipelining



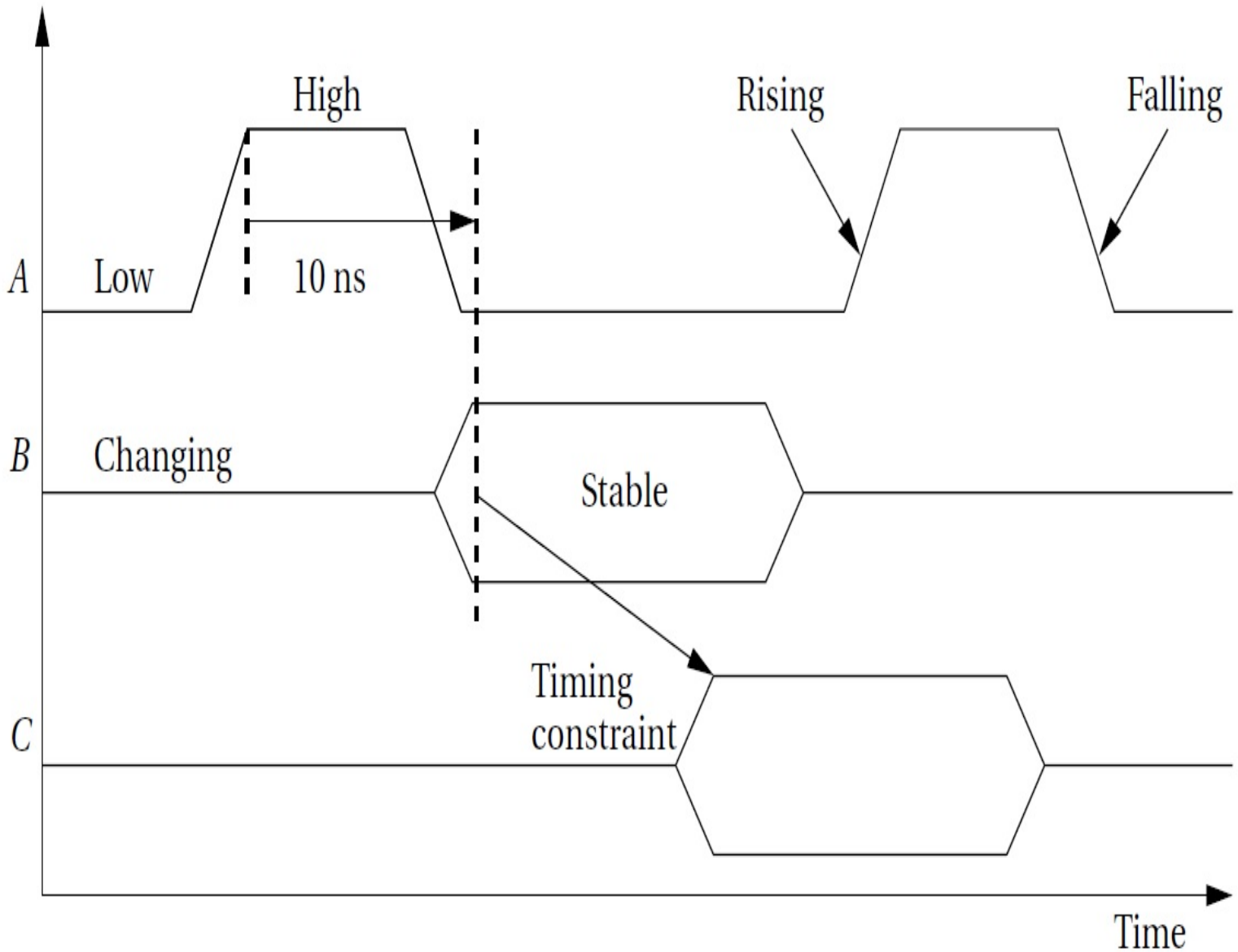
- All operations here are on registers (single cycle execution)
- In this example it takes 6 clock cycles to execute 6 instructions
- Clock cycles per Instruction (CPI) = 1

Branch Pipeline Example

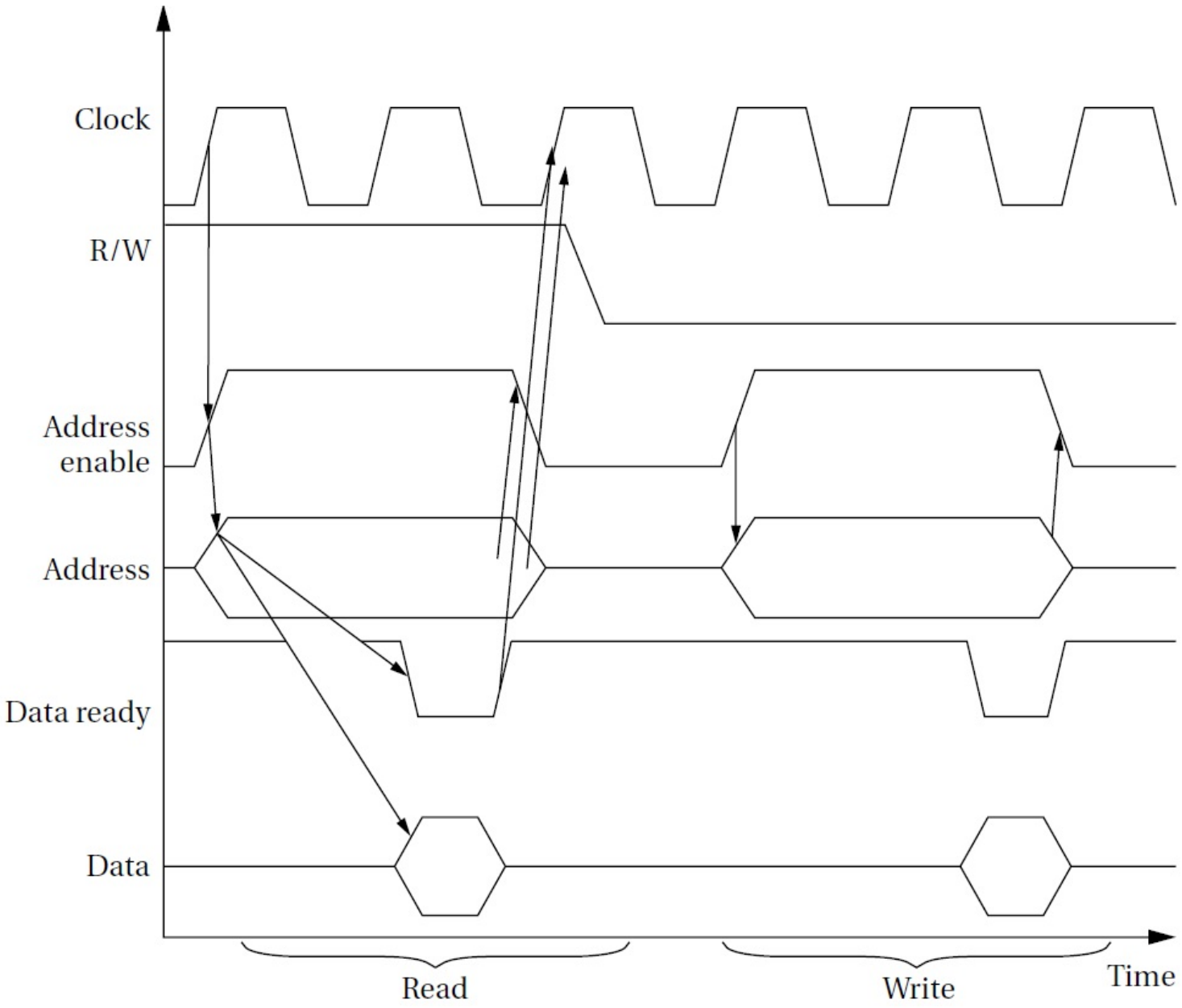


- Breaking the pipeline
- Note that the core is executing in ARM state

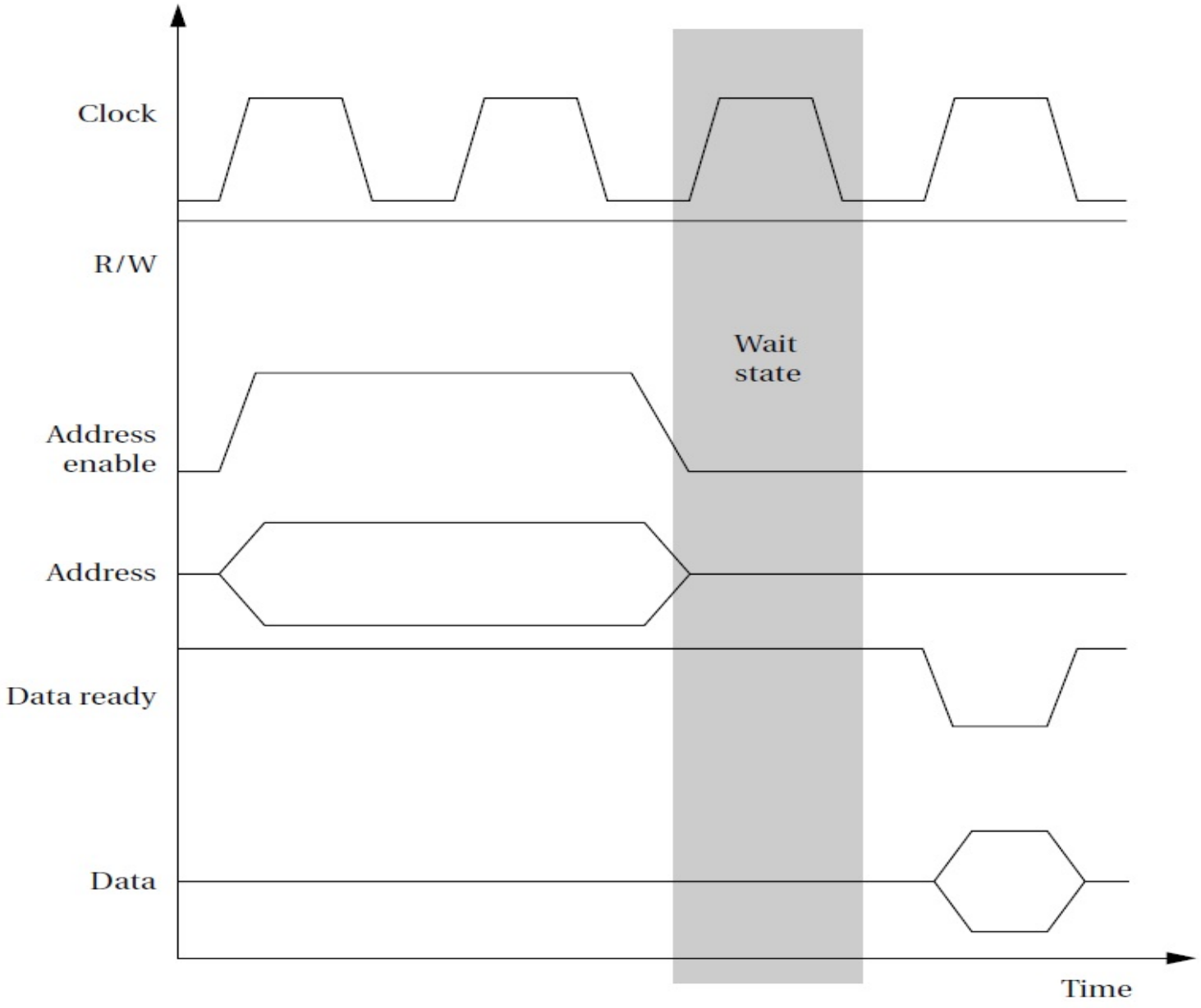
Timing Diagrams for Bus



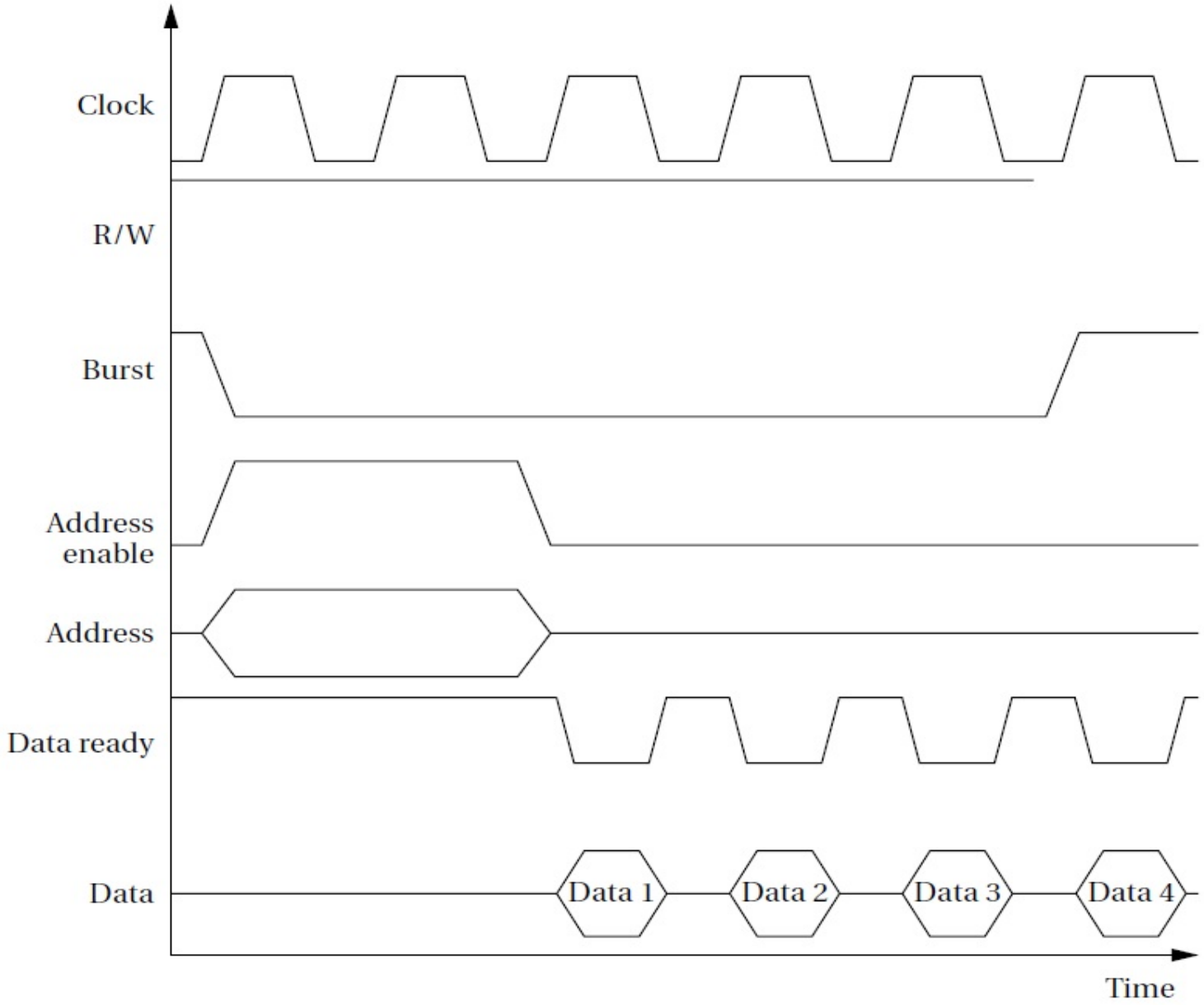
Timing Diagrams for Bus



Timing Diagrams for Bus



Timing Diagrams for Bus



Serial Protocols

For moving data quickly one device to other

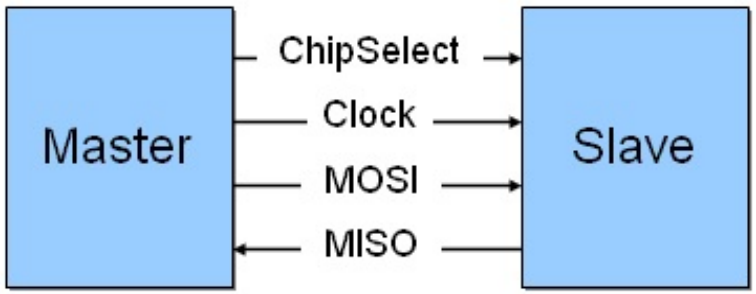
I2C

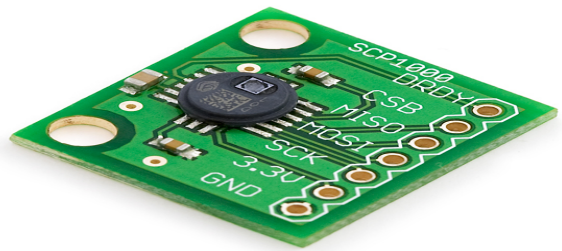
Serial Pheripharal Interface (SPI)

- Short Distances
- Less wires
- Lower foot print
- Low cost
- Low Complexity

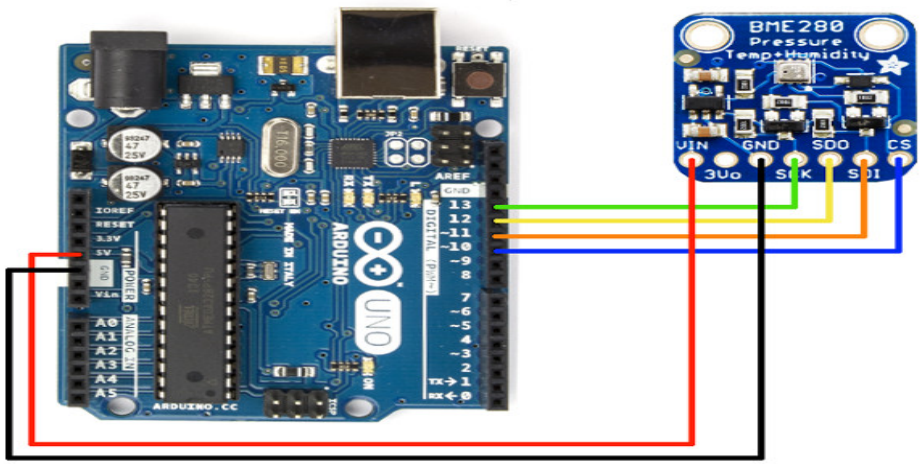
SPI

- Full duplex
- EEPROM, ADC etc.
- Faster than I2C



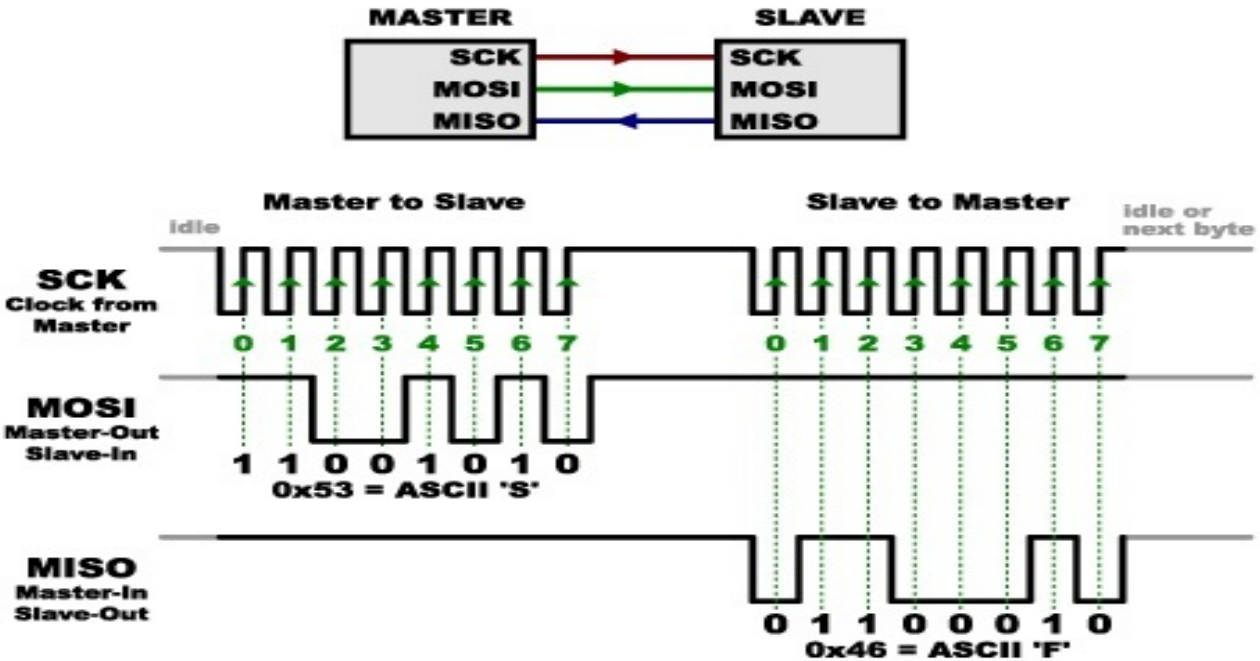


(h) Pressure Sensor with SPI

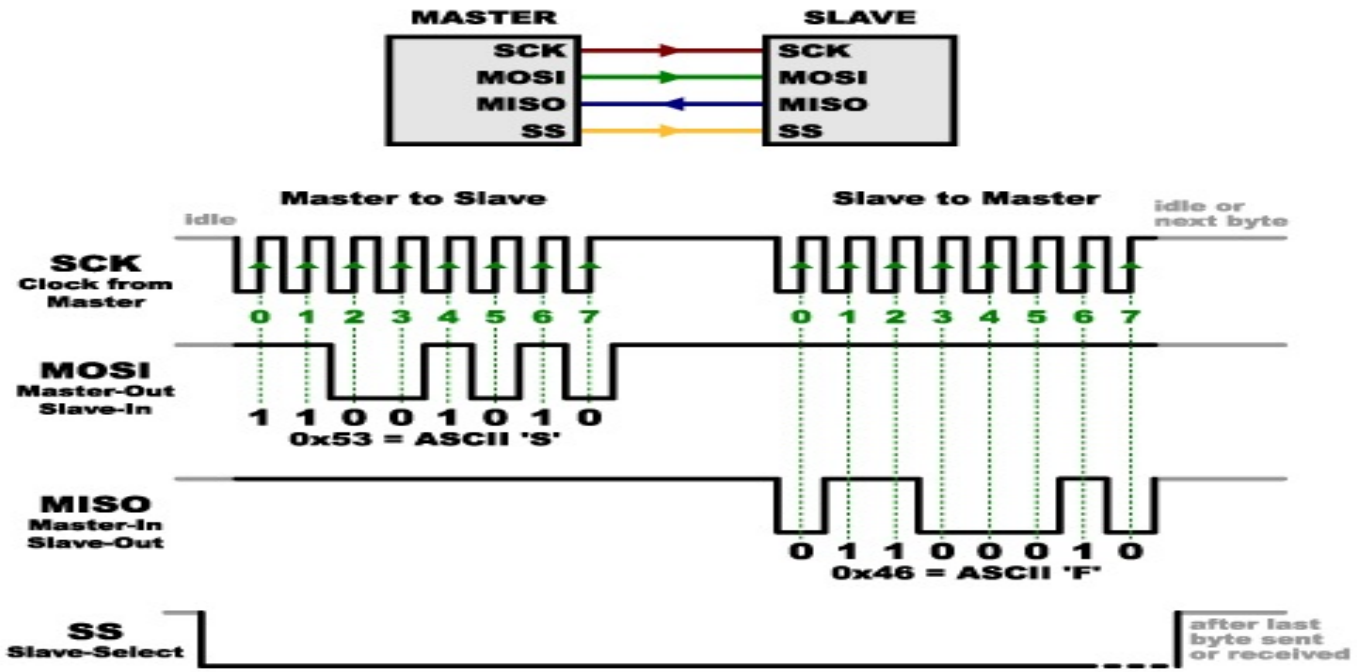


(i) Pressure Sensor with SPI

SPI - Master to Slave and Slave to Master



SPI - Slave to Master



I2C - Inter-Integrated Circuit

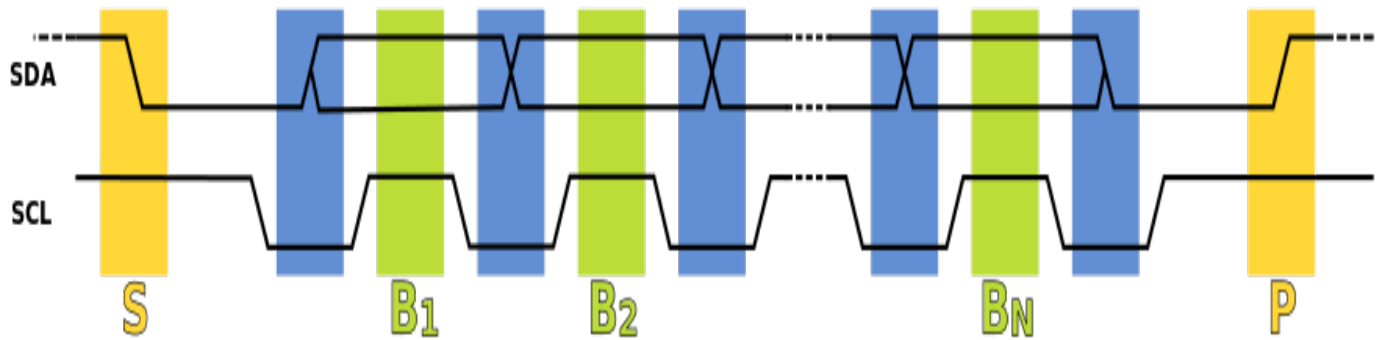
- Communication between 2 ICs
- Control Interface for specific applications
- EEPROMS, Sensors, RTC
- RF tuners, Video decoders, Audio processors

Features:

- Data is bidirectional
- Half duplex - 1 clock and 1 data line
- Synchronous - Clock drives data
- Clock speed can vary even in synchronous
- Slow (100 KBPS), Fast (400 KBPS), High Speed (1.4 MBPS)

I2C

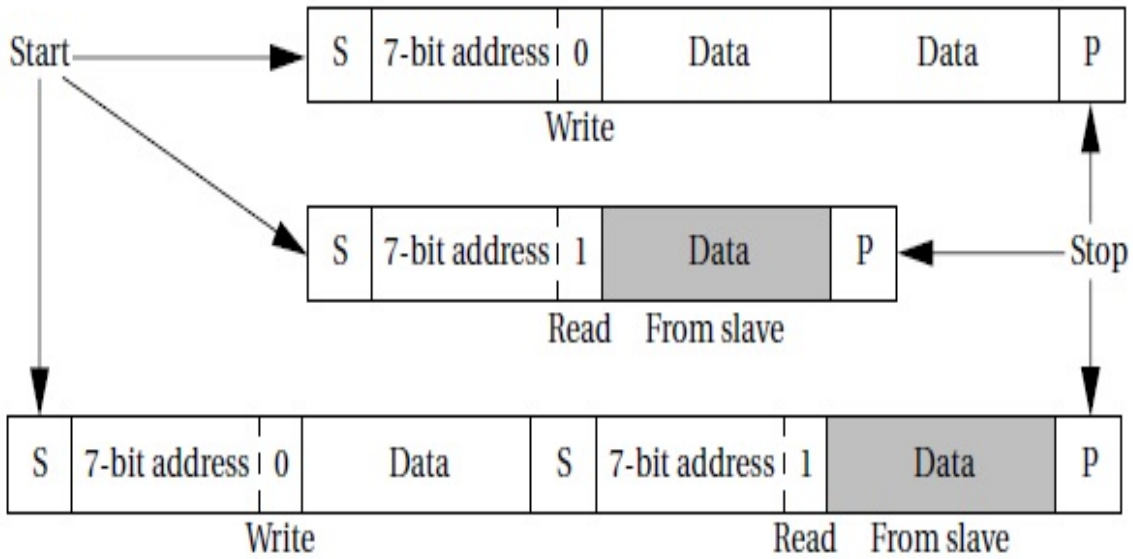
- SDA - Serial Data and SCL - Serial Clock
- SCL high indicates valid data, Data Change during low clock
- Start - S and Stop - P, Data is between S and P

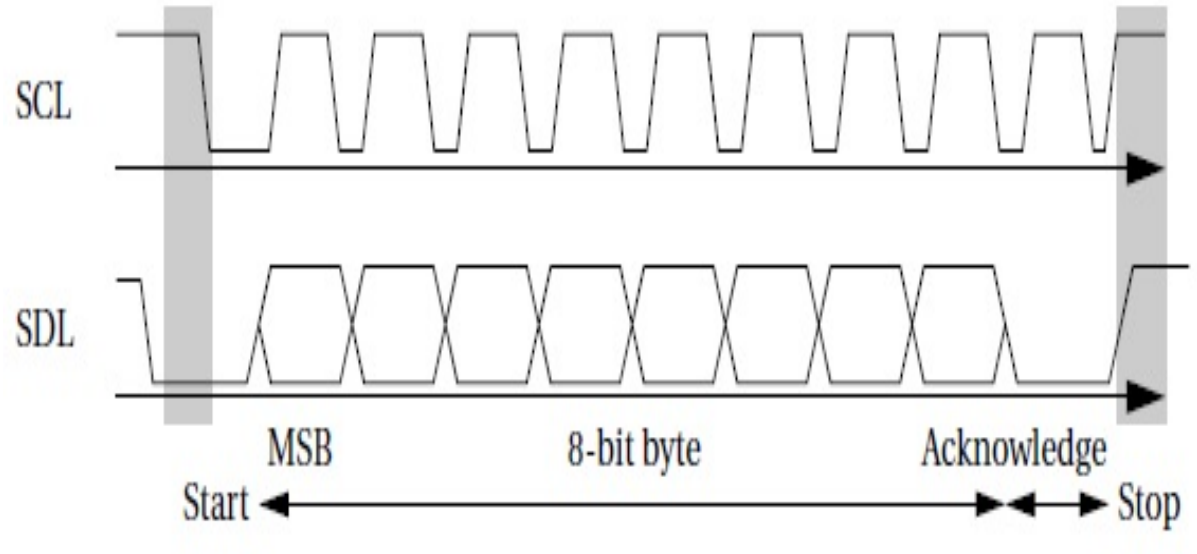


I2C - Protocol

- 8 bits and 1 ACk bit
- Most Significant bit first
- Address of reciepent - is also data
- First byte is address - Master- Tx and slave address is sent
- 7 bit address and last bit decide weather read or write

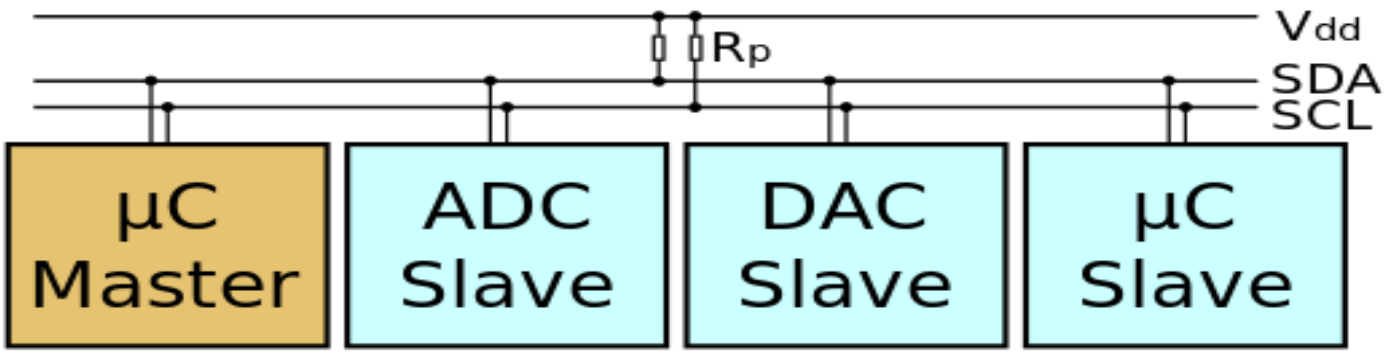
I2C - Protocol





I2C - Protocol

- master and slave - interchangeable
- Master drives clock
- Slave pulls clock low - No Data transfer - wait state - speed mismatch
- All slaves are controlled by master
- Arbitration is available with only 2 wires



I2C - Protocol

- for occasionally used devices communication on board
- Easy to link multiple devices
- Cost and complexity do not scale up with devices
- COmplexity of supporting software can be higher