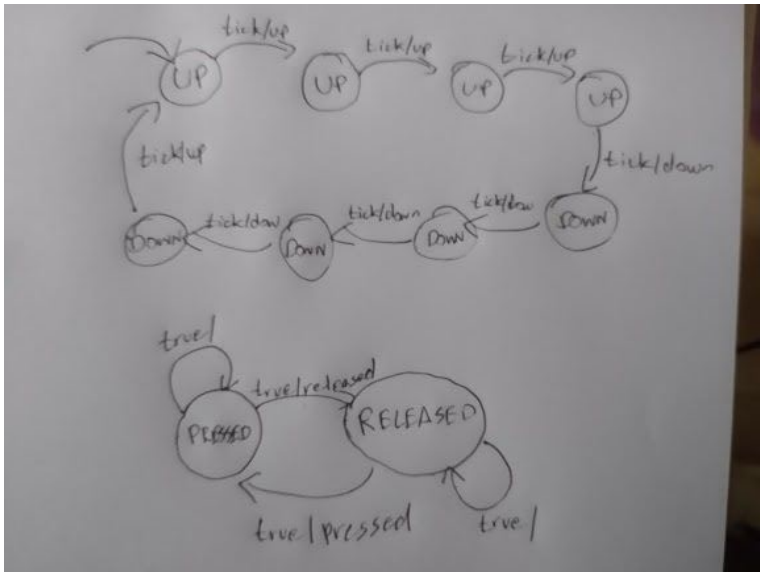
SET - 1

1.

2. Ans:



Is this right?
Any idea about the model?

GOt a similar one. We can write acc to this.

This is a formal model, he is aski

Solution: The FSM description is:

$$
\begin{aligned}
States &= \{\text{red}, \text{yellow}, \text{green}\} \\
Inputs &= (\{tick\} \to \{present, absent\}) \\
Outputs &= (\{go, stop\} \to \{present, absent\}) \\
initialState &= \text{red}
\end{aligned}
$$

The update function is defined as:

$$
update(s,i) = \begin{cases}
(\text{green}, go) & \text{if } s = \text{red} \wedge i(tick) = present \\
(\text{yellow}, stop) & \text{if } s = \text{green} \wedge i(tick) = present \\
(\text{red}, stop) & \text{if } s = \text{yellow} \wedge i(tick) = present \\
(s, absent) & \text{otherwise}
\end{cases}
$$

ng for mathematical. Are they the same?
Yes. I'm sure.

Yeah!! Thank You How do you come up with mathematical model for this?

3.

2. *Embedded Processors:* Answer the following question. This question carries 15 marks. The question is immediately given below this text. As a reference to this question the Example 8.6 is given from the textbook as a shadowed box.

Consider the following instruction, discussed in Example 8.6:

```
MAC *AR2+, *AR3+, A
```

Suppose the processor has three ALUs, one for each arithmetic operation on the addresses contained in registers AR2 and AR3 and one to perform the addition in the MAC multiply-accumulate instruction. Assume these ALUs each require one clock cycle to execute. Assume that a multiplier also requires one clock cycle to execute. Assume further that the register bank supports two reads and two writes per cycle, and that the accumulator register A can be written separately and takes no time to write. Give a reservation table showing the execution of a sequence of such instructions.

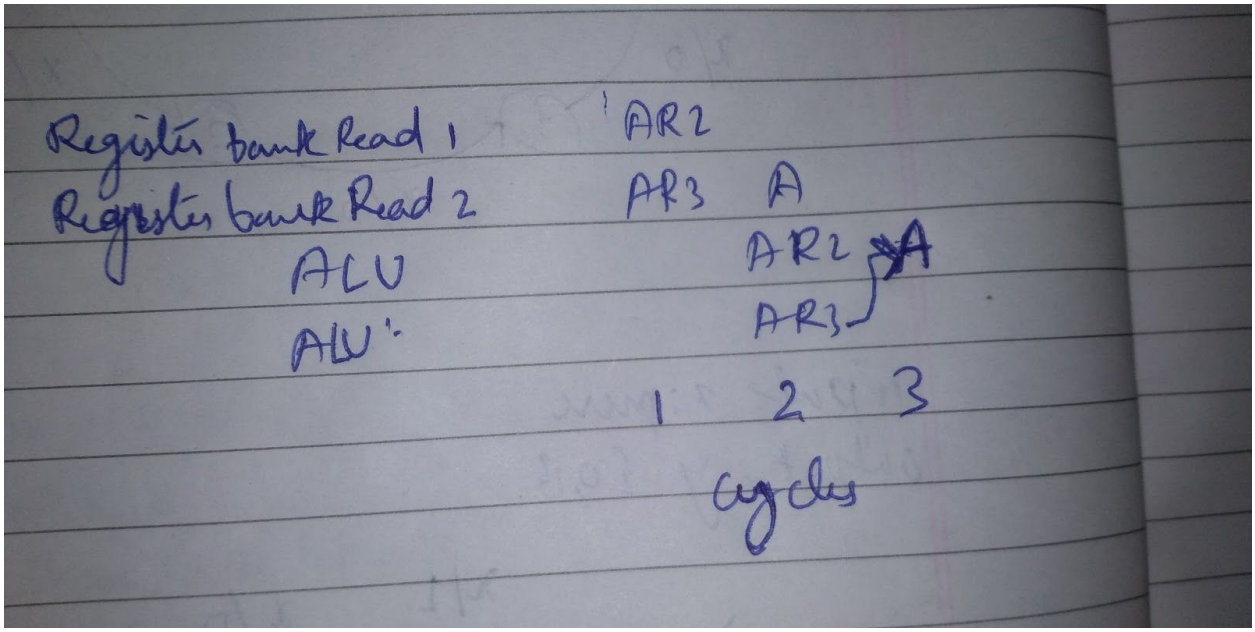
Example 8.6: The Texas Instruments TMS320c54x family of DSP processors is intended to be used in power-constrained embedded applications that demand high signal processing performance, such as wireless communication systems and personal digital assistants (**PDA**s). The inner loop of an FIR computation (8.1) is

```
1 RPT numberOfTaps - 1
2 MAC *AR2+, *AR3+, A
```

The first instruction illustrates the **zero-overhead loop**s commonly found in DSPs. The instruction that comes after it will execute a number of times equal to one plus the argument of the RPT instruction. The MAC instruction is a **multiply-accumulate instruction**, also prevalent in DSP architectures. It has three arguments specifying the following calculation,

$$a := a + x * y \,,$$

where a is the contents of an accumulator register named A, and x and y are values found in memory. The addresses of these values are contained by auxiliary registers AR2 and AR3. These registers are incremented automatically after the access. Moreover, these registers can be set up to implement circular buffers, as described in the box on page 221. The c54x processor includes a section of on-chip memory that supports two accesses in a single cycle, and as long as the addresses refer to this section of the memory, the MAC instruction will execute in a single cycle. Thus, each cycle, the processor performs two memory fetches, one multiplication, one ordinary addition, and two (possibly modulo) address increments. All DSPs have similar capabilities.



ITNA HI SMJH AAYA. aage karo koi.
ANYONE?

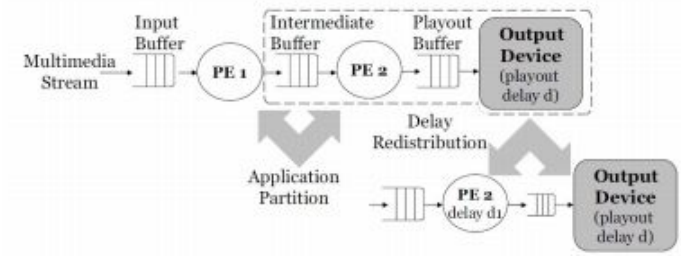
4.

Ans: Chapter 8 question 2 exercise problem...kisiko answer mila

5.

3. *Discrete /Continuous Dynamics: (30 marks)* For the below specification given:
   a. Construct the Actor model for design and analysis of the below problem statement *(20 marks)*,
   b. Write the formal model for the actor model you have constructed. *(10 marks)*.

Consider our system model shown in Figure, and assume a streaming application that is partitioned into tasks and mapped to the Processing Elements (PEs) of the system. A constant bit rate input stream arrives at the input buffer, PE 1 partially processes it and writes it to the intermediate buffer. PE 2 reads items from the intermediate buffer, completely processes the stream, and writes it to the playout buffer. Finally, the display device consumes items from the playout buffer at a constant rate. The display device reads items from the playout buffer after an initial delay *d*. At time instance zero, PE1 starts to process items from the input buffer. After a delay *d1*, PE2 processes items from the intermediate buffer. The display device displays 30 frames per second.



Not sure if this is from the book. But problem statement is taken from https://dl.acm.org/doi/pdf/10.1145/1278480.1278664 (page 740 left side). Can someone confirm?

Ans:

SET 2

NOTICE for set 2:
Ques 3 is a chapter 2 Ques 7 exercise problem.
Can someone confirm if that is right in 3rd question

1. Answer the following question. This question carries 15 marks.

EMBEDDED PLATFORMS

You are considering a particular small and inexpensive microcontroller for use in a product. The processor used in this microcontroller includes a pipeline. Hardware is included in the processor to detect and mitigate all structural and control hazards. However, to reduce the cost of the processor, there is no detection or mitigation of data hazards.

a. Would you expect the pipelining to improve the latency, the throughput, or both for this processor over an equivalent sequential processor without pipelining?
b. The processor does not handle data hazards. What does this imply about your programs?

1.

Ans.
Question Source:
https://www.chegg.com/homework-help/questions-and-answers/6-6-pts-considering-particular-small-inexpensive-microcontroller-use-product-processor-use-q46054845

a. Pipelining increases the CPU instruction throughput - the number of instructions completed per unit of time. But it does not reduce the execution time of an individual instruction. In fact, it usually slightly increases the execution time of each instruction due to overhead in the pipeline control.The increase in instruction throughput means that a program runs faster and has lower total execution time.

   Latency ka koi search kro? Latency = Exec time ?? So it increases..

- *Each instruction takes a certain time to complete.*

- *This is the latency for that operation.*
- *It's the amount of time between when the instruction is* **issued** *and when it completes.*

Latency of the instruction increases as there is now a overhead too.

b. 2nd part book wali example hai copy kar do page 225 Apne shabdo me likhna .

B. The processor does not handle data hazard means the next instruction coming in does not need to depend on the previous instruction. Meaning the sequential instructions in programs are independent from each other only then the data hazard doesn't occur and the processor doesn't need to take care for that or the dependeant instruction come in when the instruction it's dependeant on executes and writes it to result register. Ise bhi apne shabdo me

+

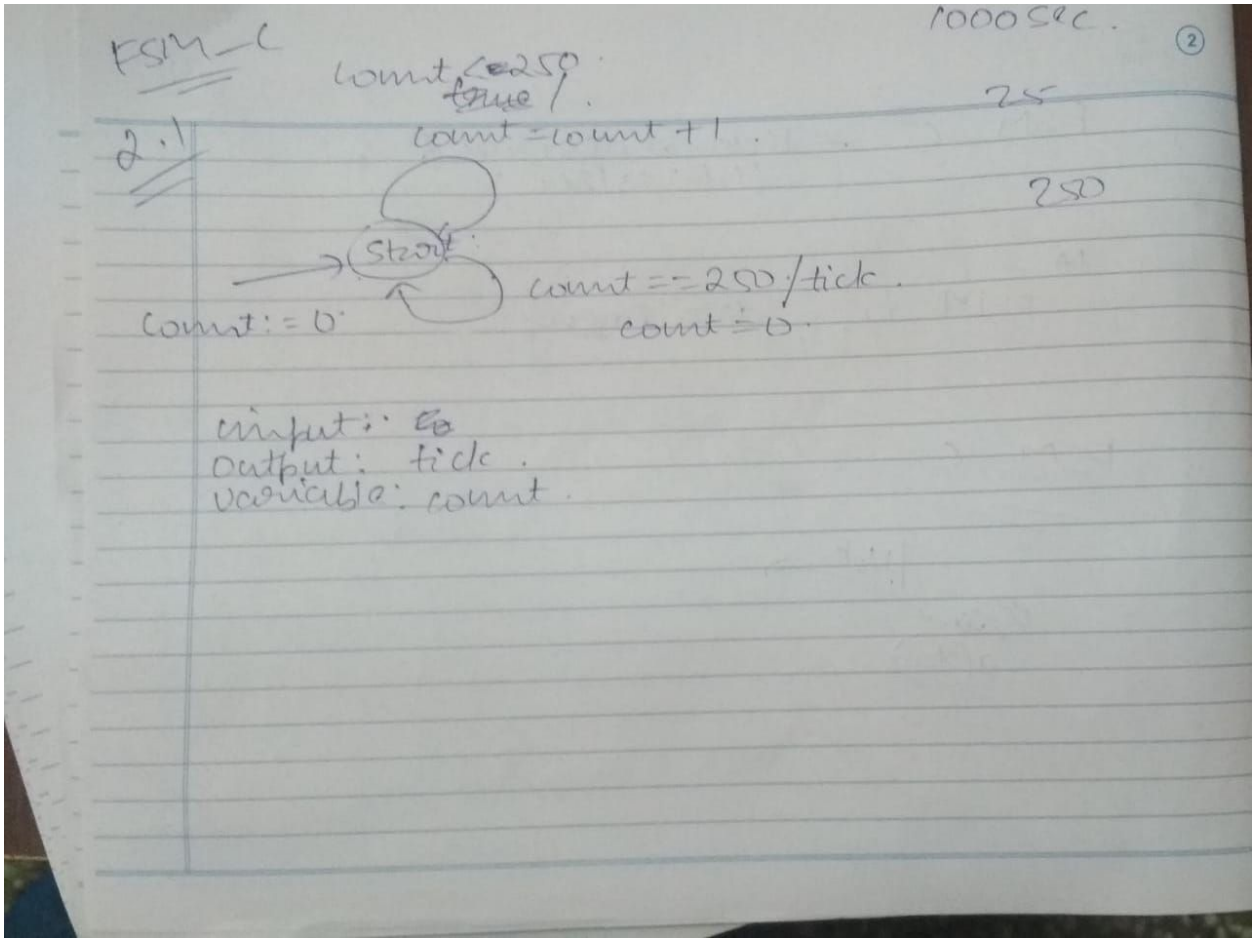
2.

2. Answer the following question. This question carries 30 marks (each question carries 15 marks). For both the below questions draw the finite state machine and present the mathematical model for it. If they are any behavior and/or parameters not defined assume appropriately. Based on the system definition choose if you need a deterministic or non-deterministic state machine.
(*ignore the reference to the figure in the text book in the first question*)

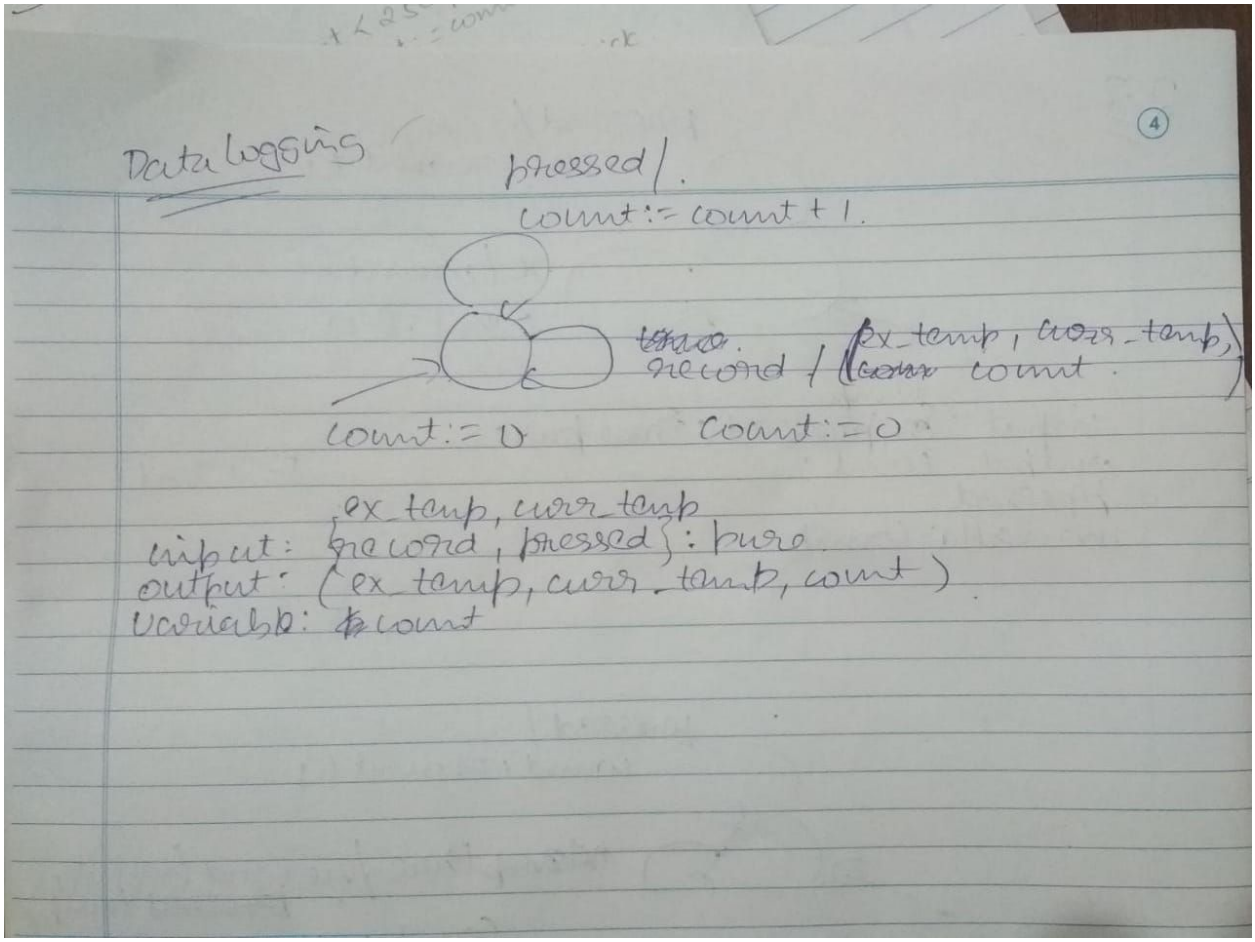
Define a (possibly extended) state machine (call it FSM_C) that models a timer interrupt service routine. FSM_C outputs a pure periodic signal tick at a desired frequency (say 4 times per second). Assume that you can set up the timer so that the interrupt occurs 1000 times per second; FSM_C could look a lot like what you can see in Figure 9.5 in the text.

Define another state machine (call it FSM_D) that models a data logging system. Every 30 seconds it reads the temperature from an external sensor and records the current temperature and the number of times the button was pressed and released since the last log entry.

Ans. [5 pts] Define a deterministic FSM (call it FSM_A) that has one pure input (tick) and two pure outputs (up and down). FSM_A outputs up for 4 ticks...
Question yaha pe hai exact wahi answer search karo



Please confirm ????



Please confirm?????

Top loop => pressed /

Count := count+1

Right loop => record / (curr_temp, count)

Count := 0

Can anyone confirm if this is right?

3.

3. *Actor Models (30 marks)*: An actor model for the helicopter is depicted below. For the below-given actor model, do the following:
    a. Derive the equations for the model; Before deriving your equations, clearly, state the domain and co-domain of every function you use; explain each component in the actor model shown below; state the mapping of the functions for each component in the actor model; and *(20 marks)*

b. State if the model is casual or not, and justify your answer *(10 marks)*.

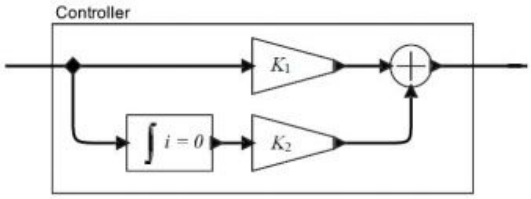
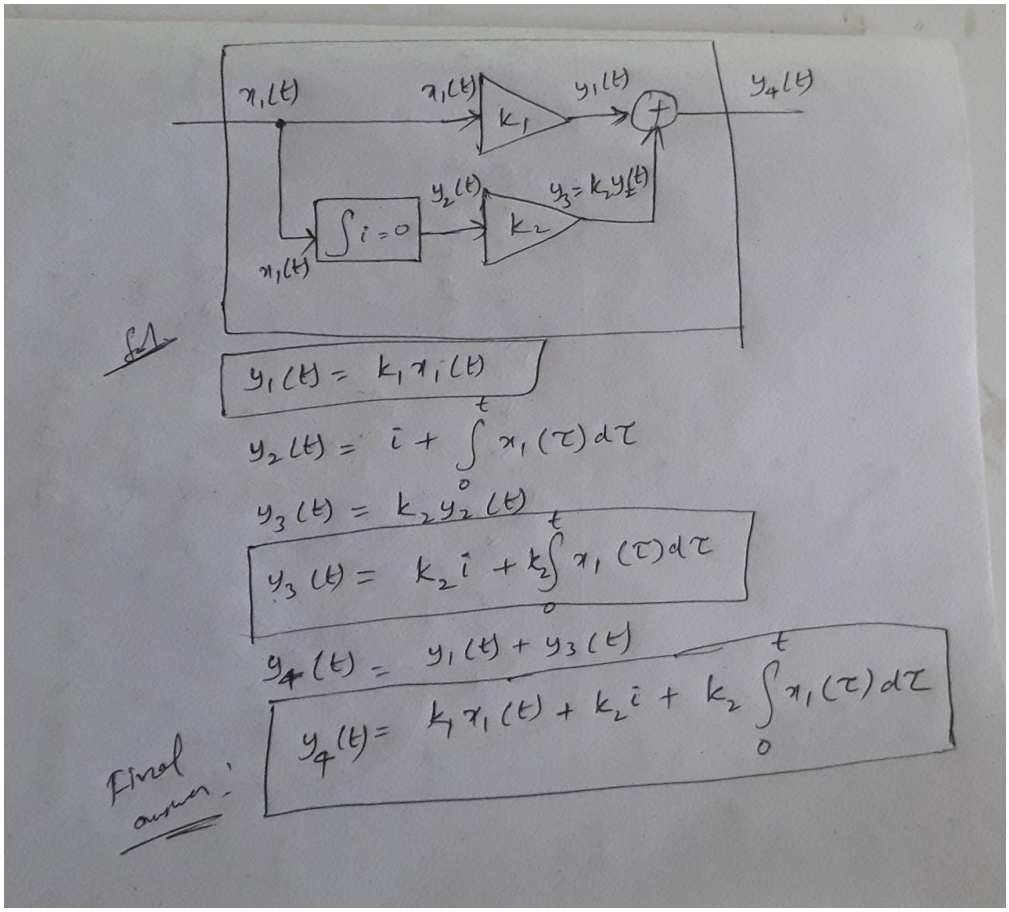


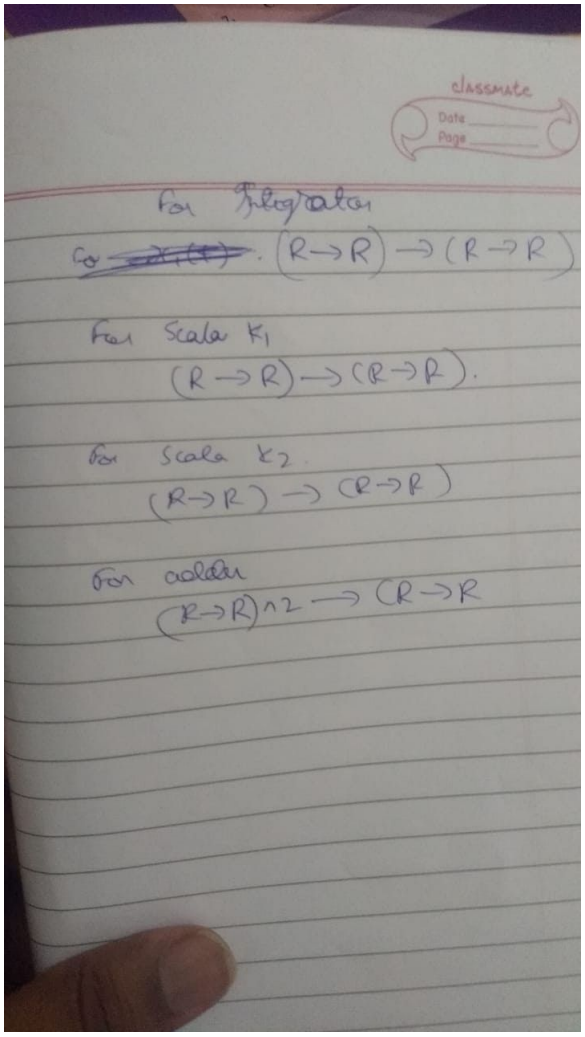
Figure 2.6: A PI controller for the helicopter.

Yeh chapter 2 question 7 hai: Answer Next page

Koi kr dega isse



Can someone confirm if this is right?
I think answer is right just integrator mein i = 0 so i ko zero rakh do final expression mein koi jarurat nahi hai-> HAAN



Pls confirm ? For the above image??
I think sahi hai mujhe book mein bhi yahi mil raha.

Domain, codomain?? (I think its S: X->Y, X=R^R) not sure though)
For y4(t) Domain (R->R)^2 Codomain : R->R .. anyone confirm ?

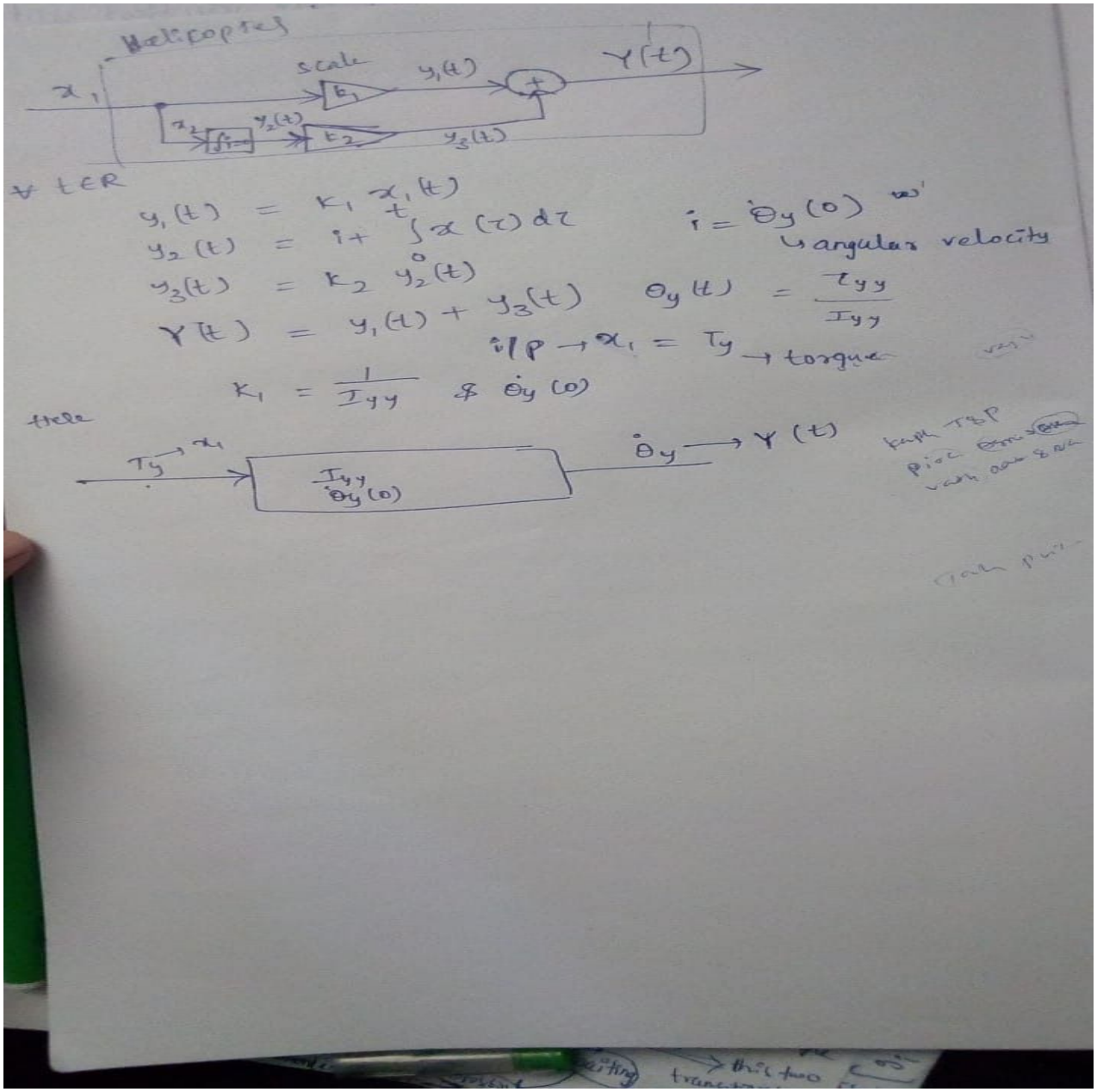
=>
t is always R ;/

We have to write for evry function^^^ ->
yes

Ab causal wala prove kar do koi
I think causal hai because equation only depends on current and past inputs.

x1(t) is present and integration wala part past pe hai. (please confirm anyone?) haan sahi lag rha hai

Check this for 3b

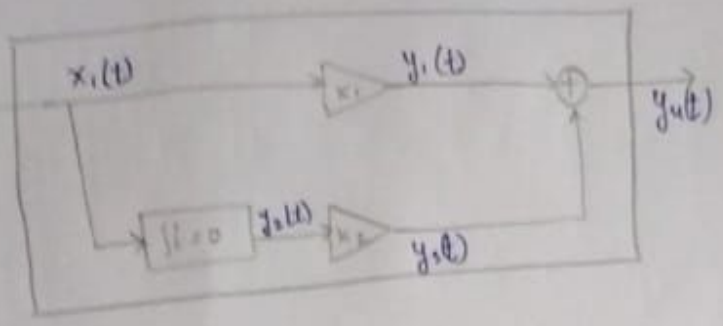


Check this for 3b

Anyone upload ur written sheet for 3a ques final changes.

Sol 2

Q3. a



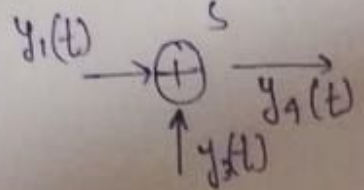
$x_1(t) : \mathbb{R} \longrightarrow \mathbb{R}$

$\forall\ t \in \mathbb{R},\ y_1(t) = K_1\, x_1(t)$

$\forall\ t \in \mathbb{R},\ y_2(t) = \cancel{i^{\,0}} + \int_0^t x_1(\tau)\, d\tau$

$\forall\ t \in \mathbb{R},\ y_3(t) = K_2\, y_2(t)$

$= K_2 \int_0^t x_1(\tau)\, d\tau$



$S : (\mathbb{R} \to \mathbb{R})^2 \longrightarrow (\mathbb{R} \to \mathbb{R})$

$\forall t \in \mathbb{R},\ y_4(t) = y_1(t) + y_3(t)$

$= K_1 x_1(t) + K_2 \int_0^t x_1(\tau)\, d\tau$

Q3 b.

As we know that an integration factor is strictly causal. This can be proved using below property.

$\forall\ x_1, x_2 \in X$ for a system $S: X \to Y$ and $\tau \in \mathbb{R}$

$$x_1|_{t<\tau} = x_2|_{t<\tau}$$

$$\Rightarrow \quad S(x_1)|_{t\leq\tau} = S(x_2)|_{t\leq\tau}$$

Also we know that adder is a causal

$\therefore$ model is causal as it is comprising of integrator & adder.