CO: Computer Organization

Memory System

Indian Institute of Information Technology, Sri City

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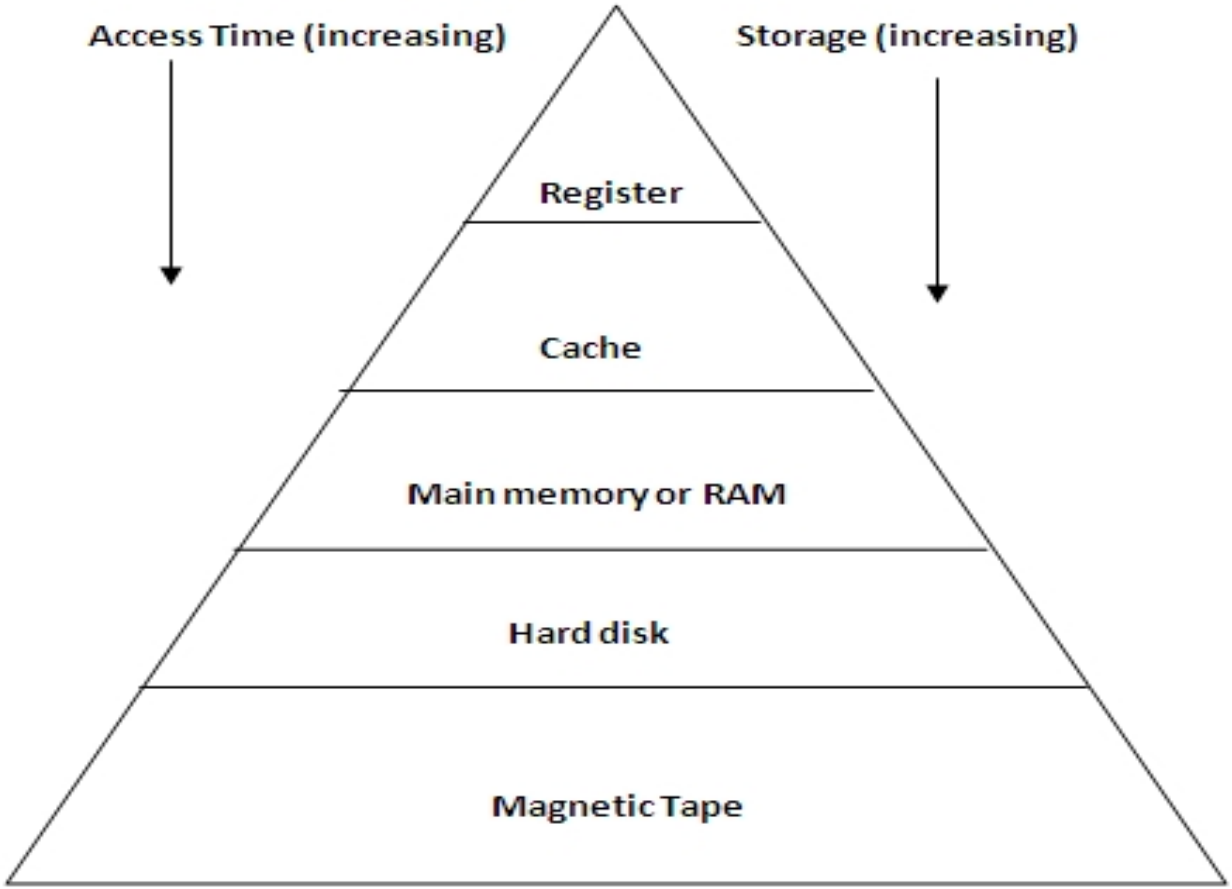
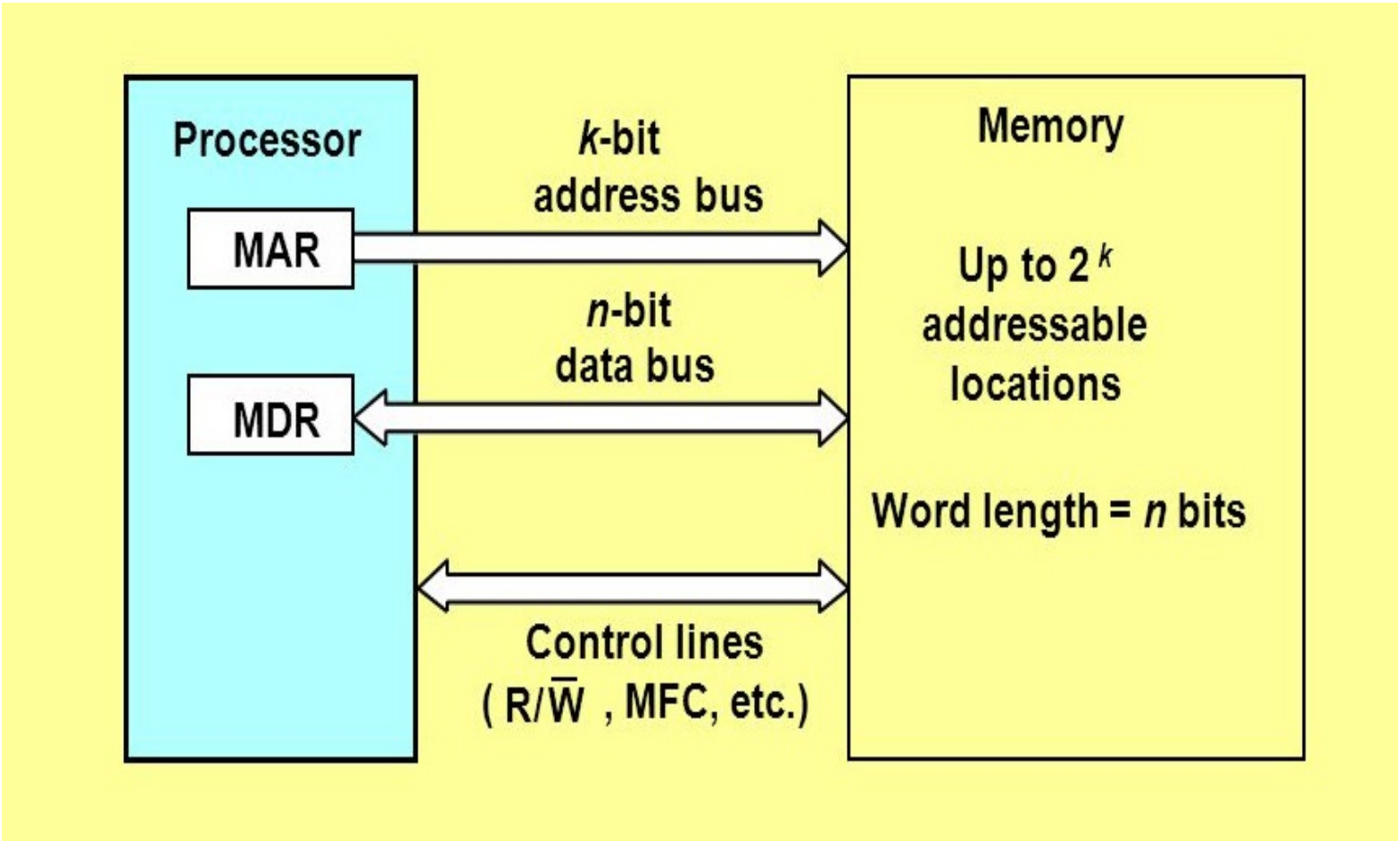
Memory System

1. Objective: Memory would be fast, large, and inexpensive.

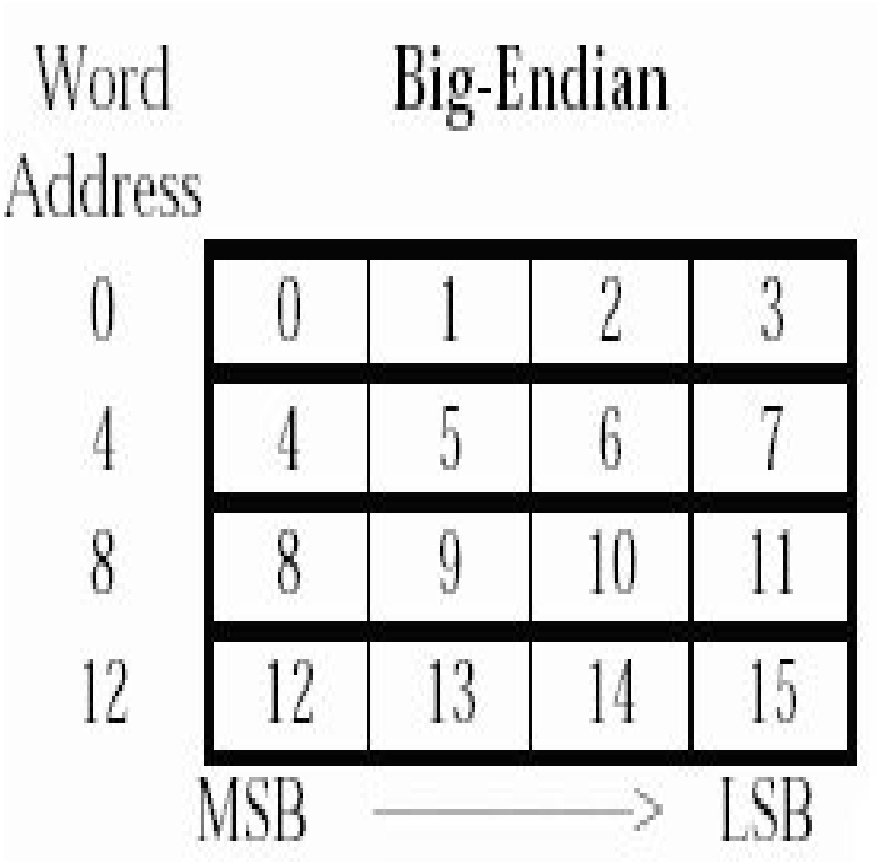


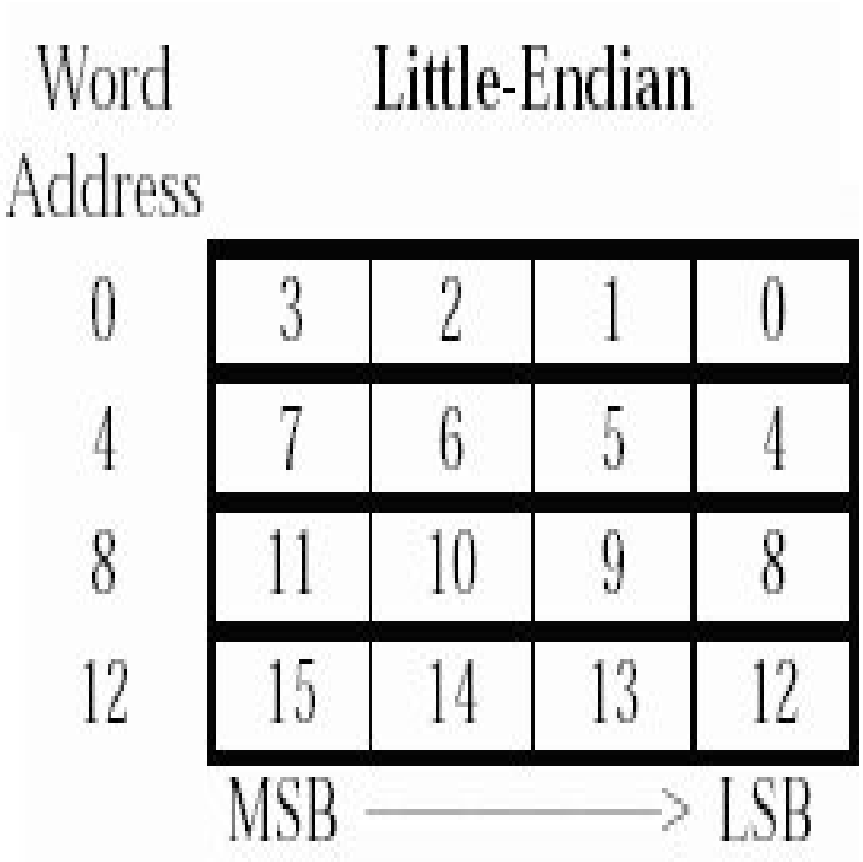
Connections between the processor and memory



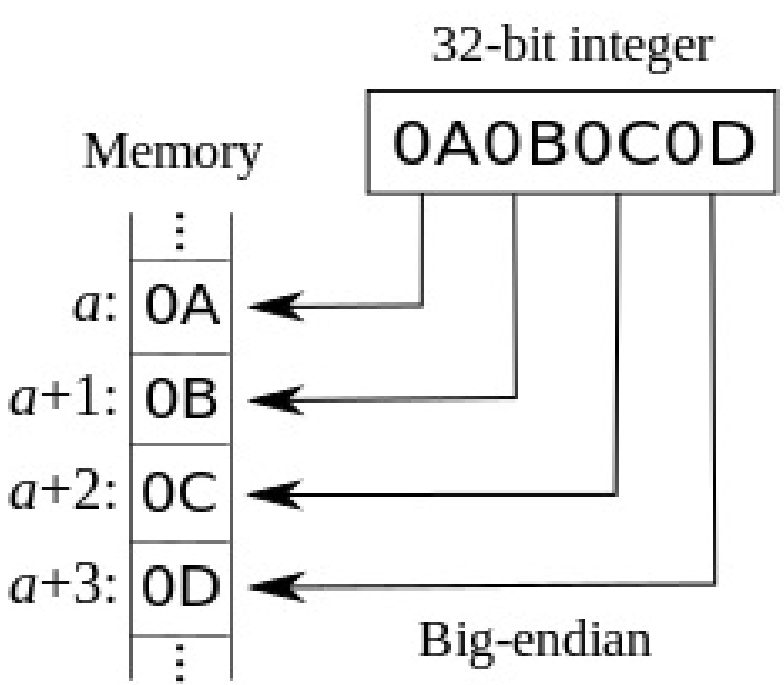
Memory System

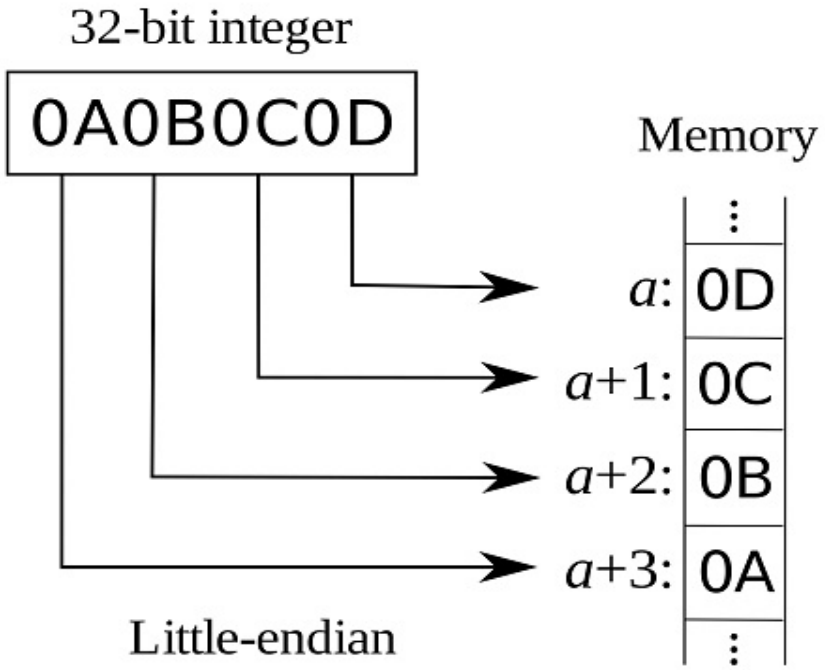
1. If there is a 4-bit address bus and 32-bit data bus then the memory locations are





Higher-order 2-bits determine word address and lower-order 2-bits determine byte location.





- Intel and ARM processors are Little-endian.
- Power PC (by Motorola) and Spark (by Sun) are Big-endian.
- Current generation ARM processors are bi-endian. Bi-endian processors can run in both modes (little and big endian).

Memory System
Read Operation

1. Processor reads data from the memory by loading the required address into MAR.
2. Set $R/\overline{W}$ line to 1.
3. The memory responds by placing the data from the addressed location onto datalines,and issues MFC (Memory Function Complete) signal.
4. Upon receiving MFC signal, the processor loads the data on the data lines into the MDR register.

Memory Access Time (MAT) is the time between the Read and MFC signal.

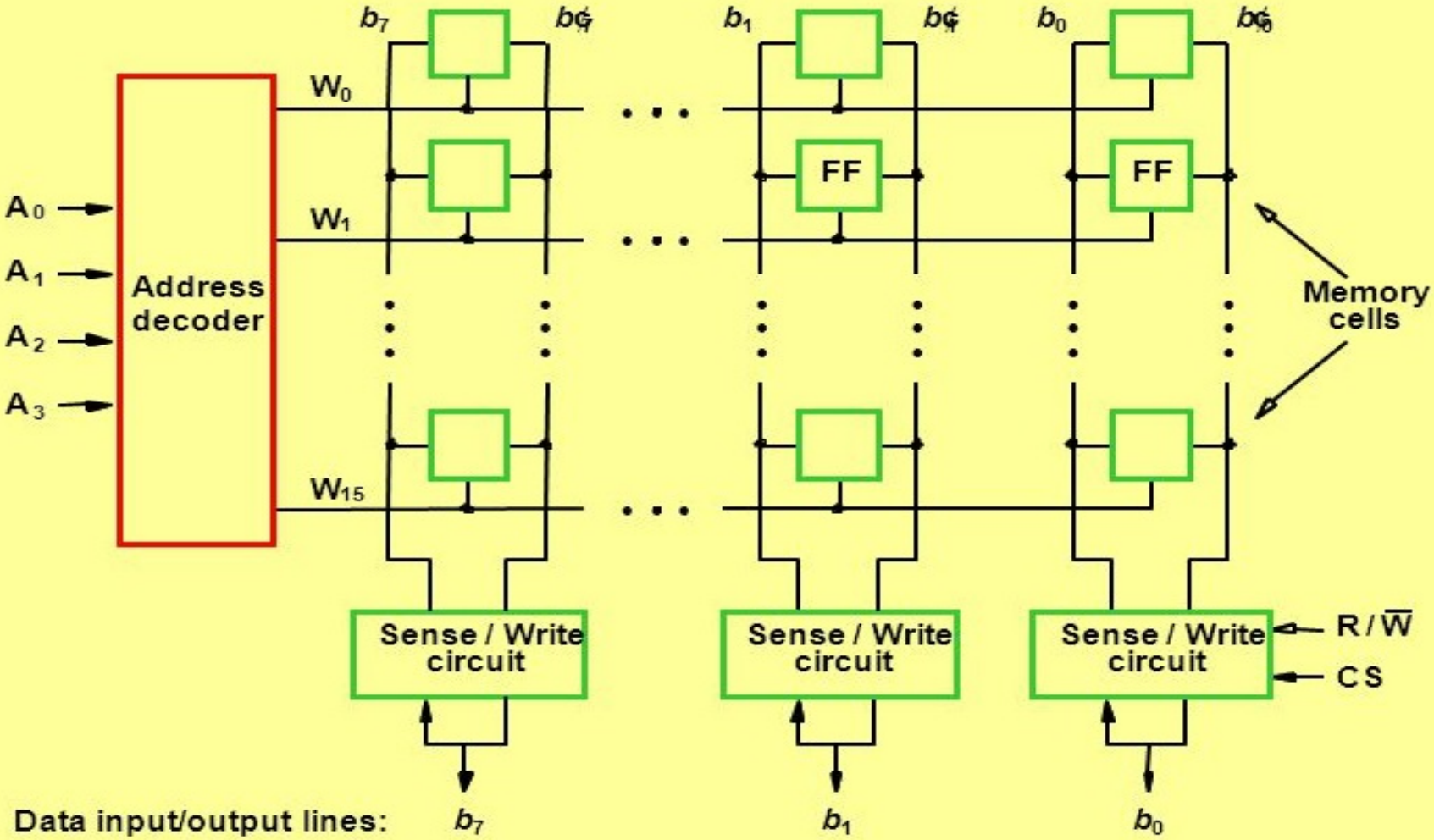
Memory System
Write Operation

1. Processor writes data into a memory by loading the required address into MAR and loading data into MDR.
2. Set $R/\overline{W}$ line to 0.
3. Place the contents of MDR into data bus and wait for MFC (Memory Function Complete) signal.
4. Upon receiving MFC signal, the next memory operation will be initiated.

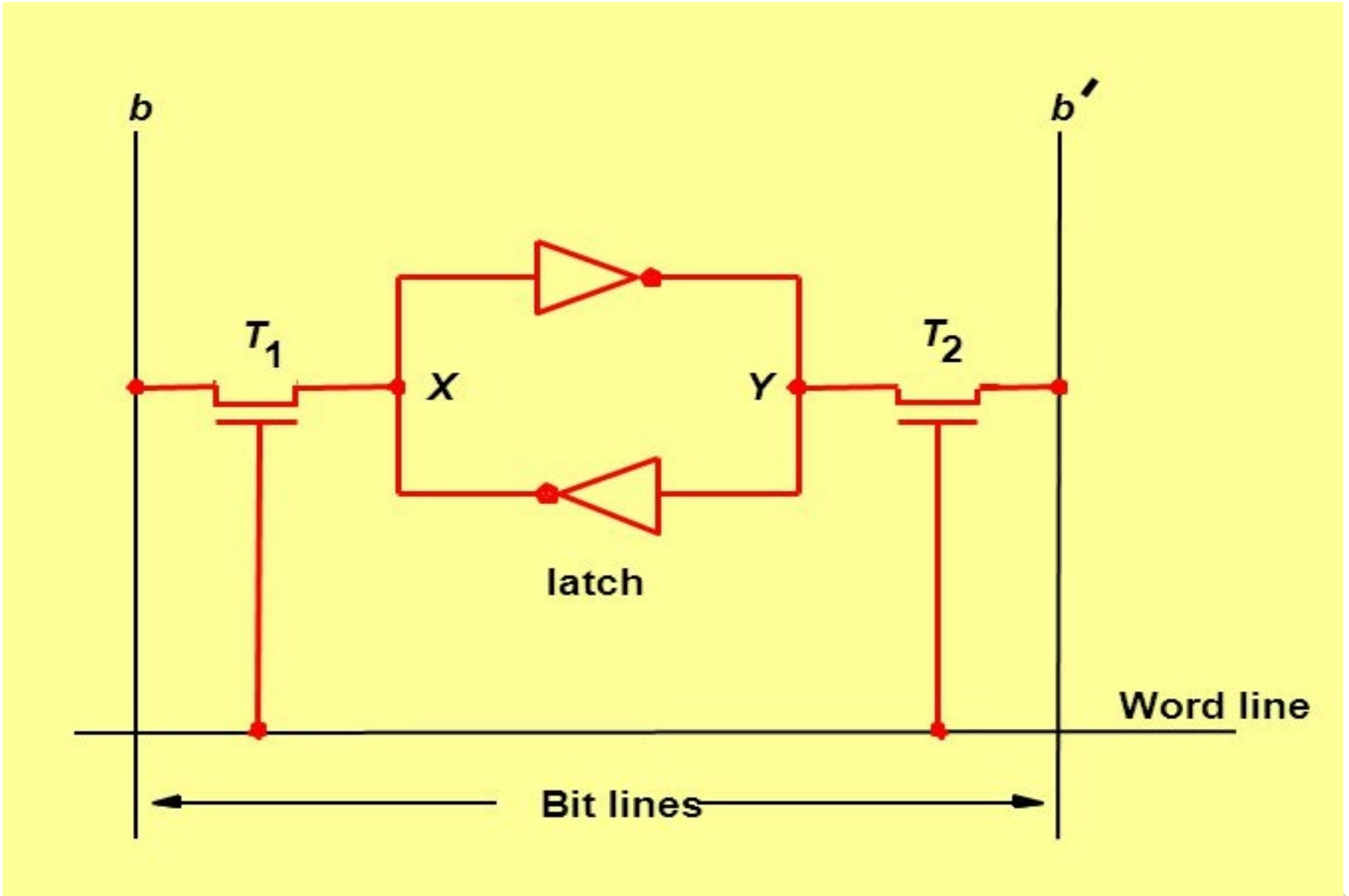
Memory Cycle Time (MCT) is the minimum time delay required between the initiation of two successive memory operations.

MAT $<$ MCT.

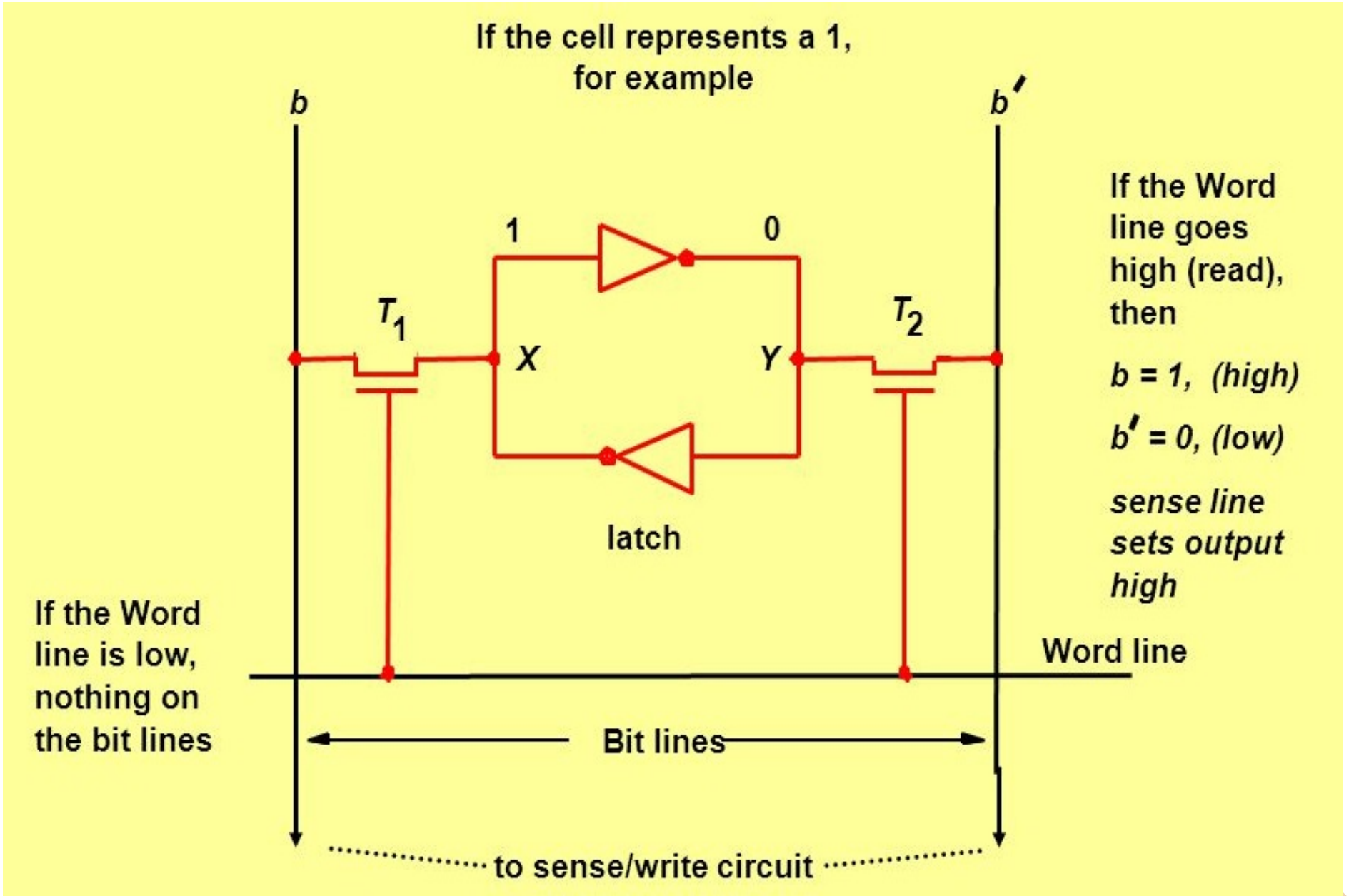
Organization of bit cells in a memory chip



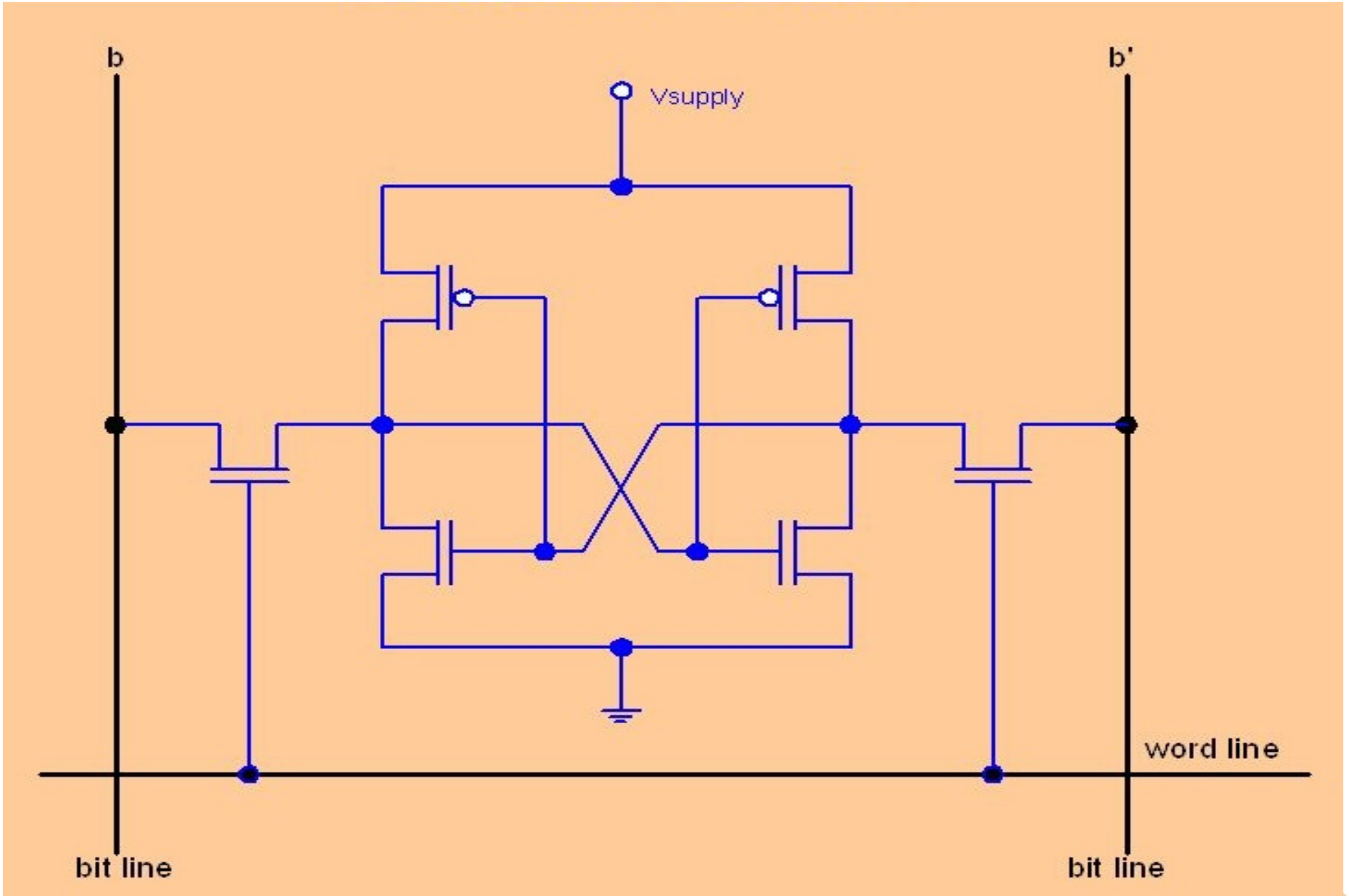
A Memory Cell



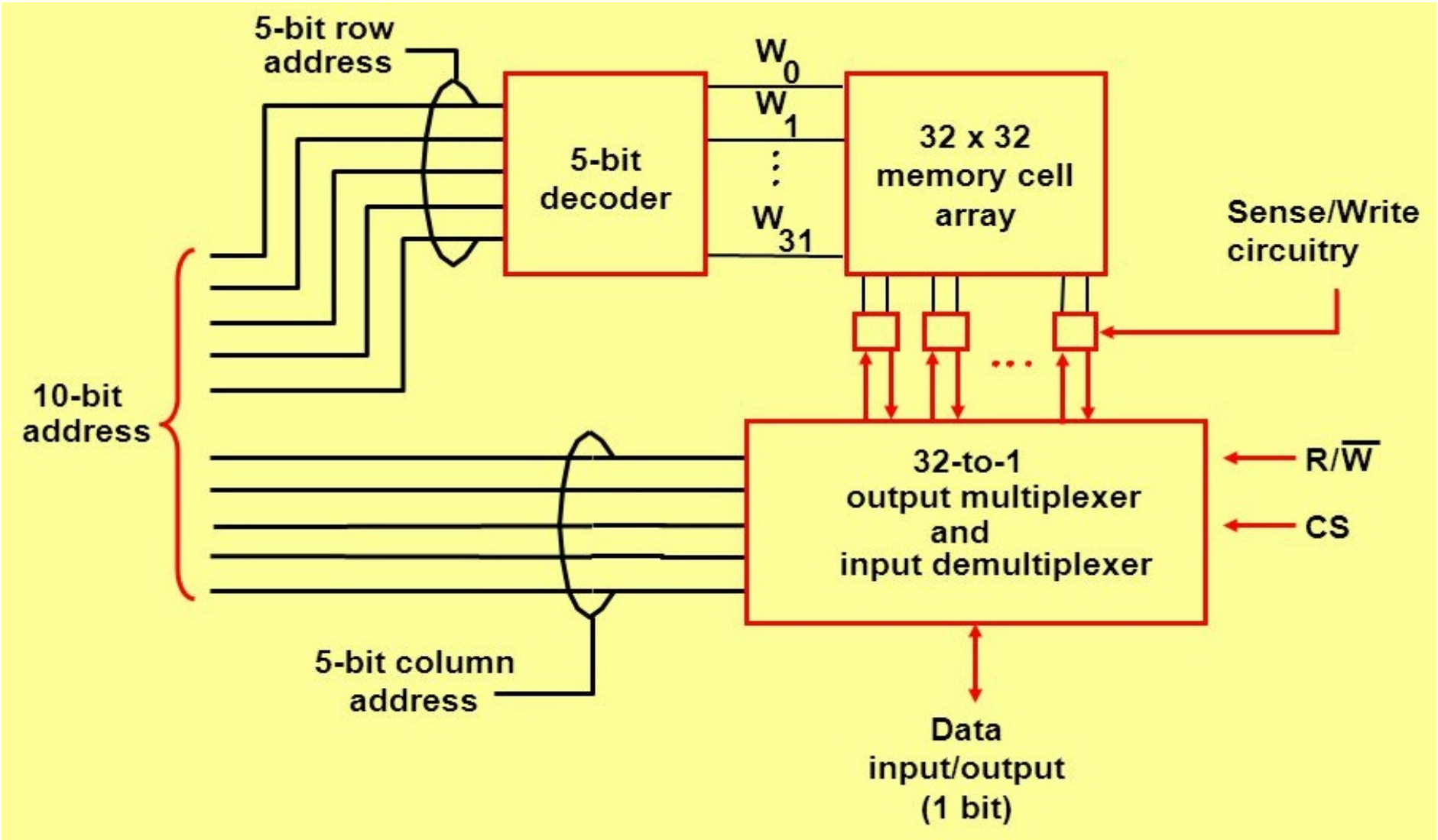
A Memory Cell



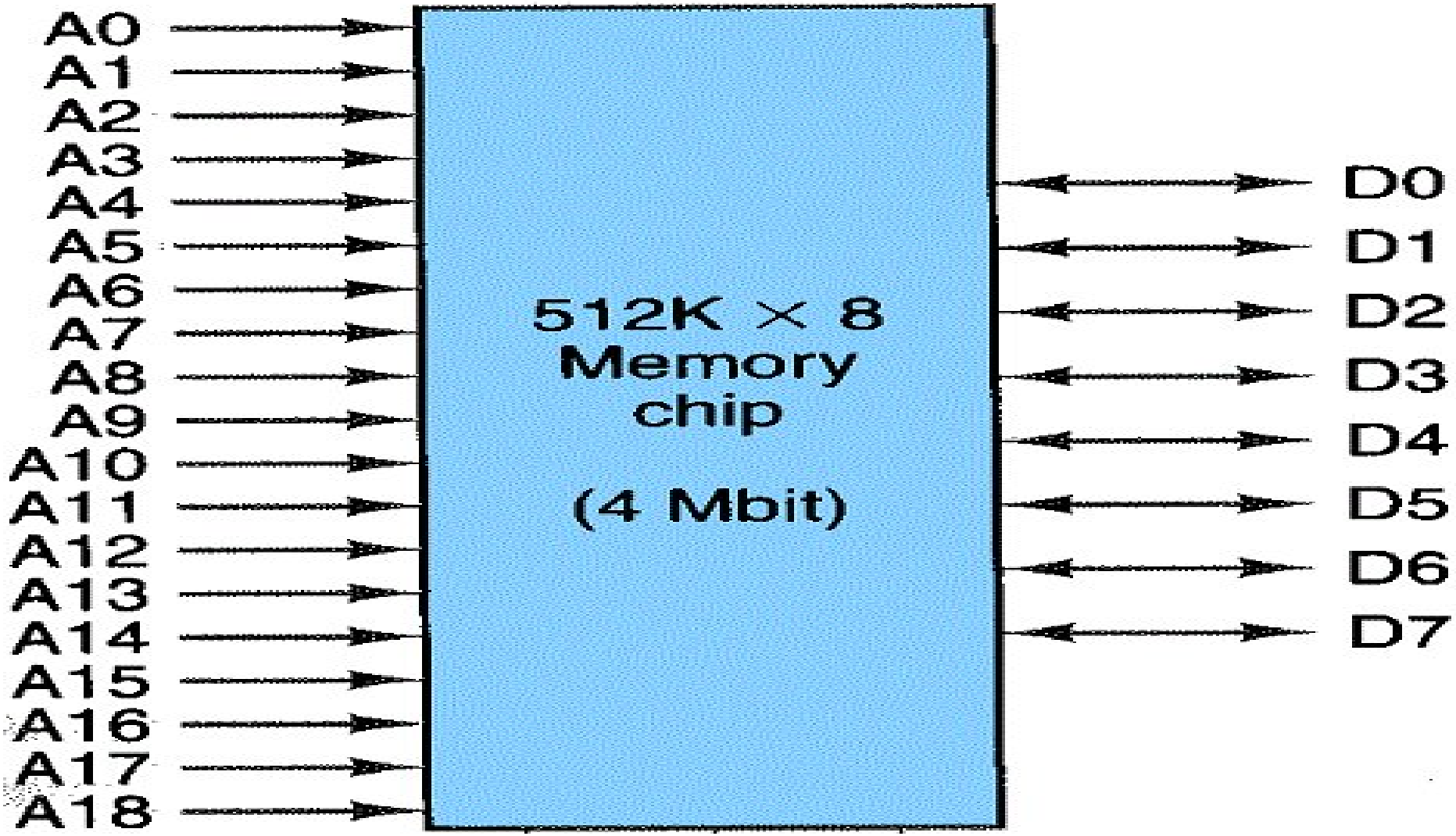
A Memory Cell



Organization of 1K x 1 memory chip



Organization of 512K x 8



Organization of 2M x 32 memory module using 512K x 8