CO: Computer Organization

Day3

Indian Institute of Information Technology, Sri City

Jan - May - 2018

http://co-iiits.blogspot.in/

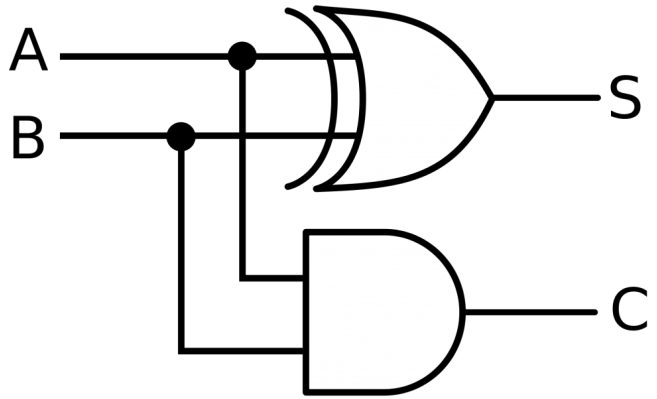
Arithmetic Operations on Integers

- Addition
  - Two 1-bit numbers
  - Two 4-bit numbers
  - Two 16-bit numbers
  - Two 64-bit numbers

Half Adder Truth Table

A	B	Carry(C)	Sum(S)
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$Sum(S) = A \bigoplus B$
$Carry(C) = AB$



If each gate delay is $1\mathcal{T}$, S and C are available after $1\mathcal{T}$.

Full Adder Truth Table

C_{in}	A	B	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$S = C_{in}^{1}(A \bigoplus B) + C_{in}(A \bigoplus B)^{1} = C_{in} \bigoplus (A \bigoplus B)$$
$$C_{out} = AB + C_{in}(A \bigoplus B)$$

Full Adder Circuit

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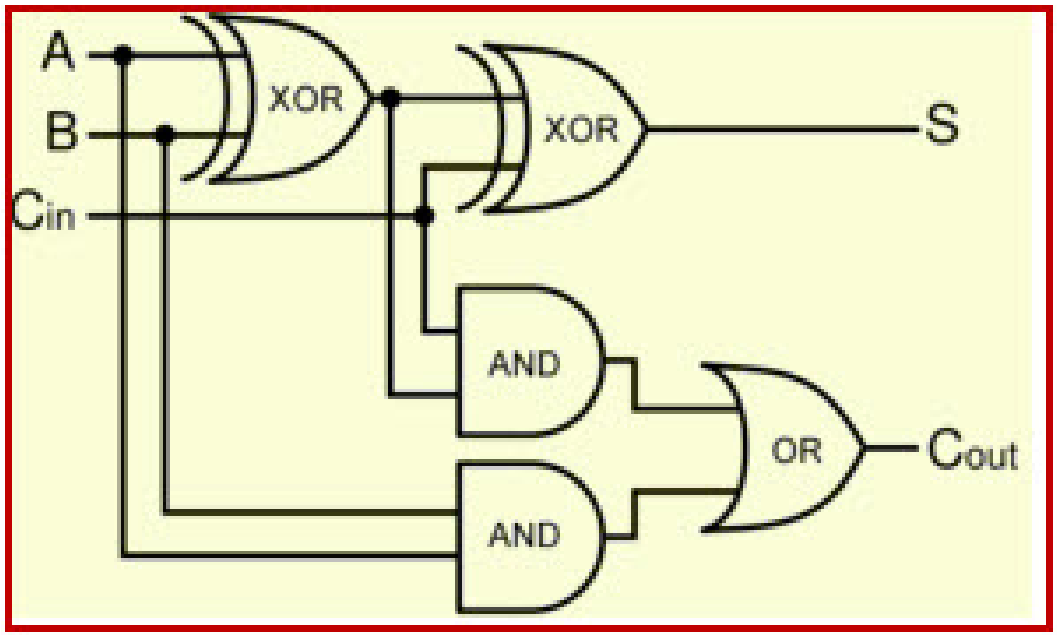
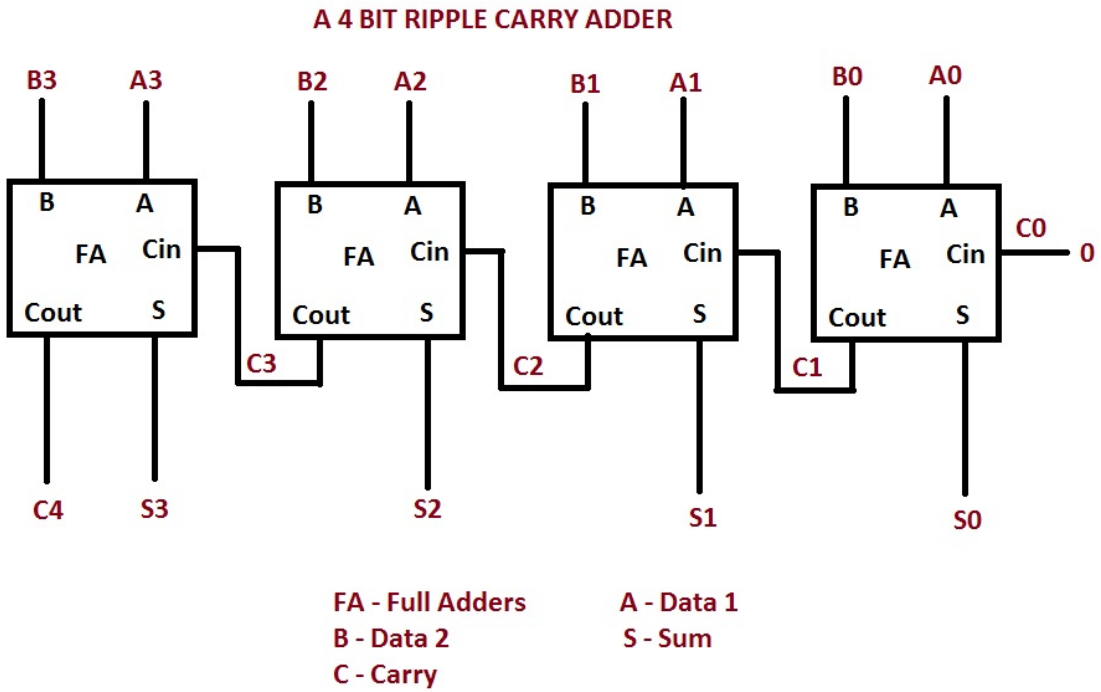


if each gate delay is $1\mathcal{T}$, then S is available after $2\mathcal{T}$ and C_{out} is available after $3\mathcal{T}$.

Addition of two 4-bit numbers

Ripple Carry Adder

Input $A = A_3 A_2 A_1 A_0$
Input $B = B_3 B_2 B_1 B_0$
Carry $C = C_3 C_2 C_1 C_0$(initial carry)
Sum $S = C_4 S_3 S_2 S_1 S_0$



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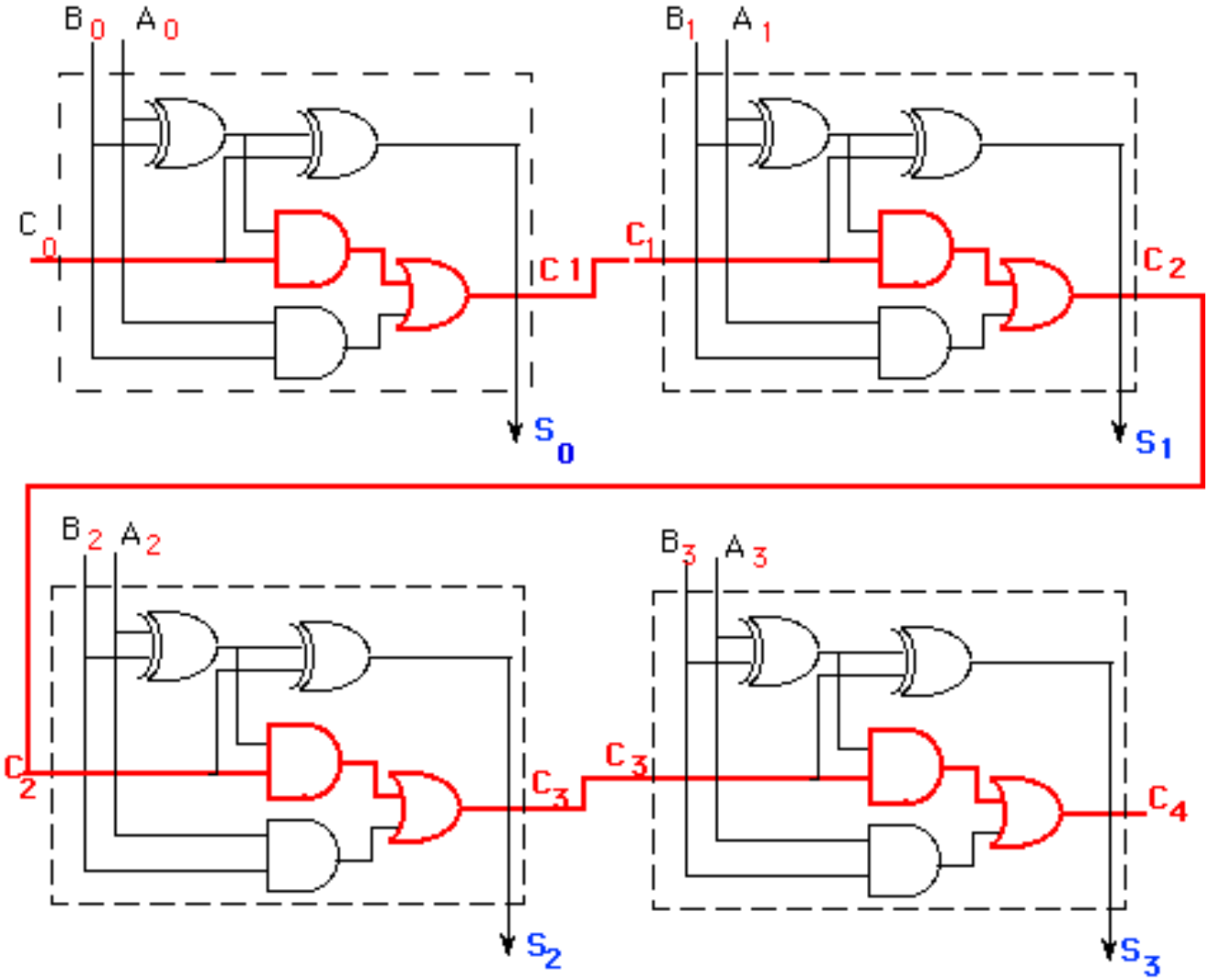

Addition of two 4-bit numbers

Ripple Carry Adder

- C_1 is available after $3\mathcal{T}$.
- C_2 is available after $5\mathcal{T}$.
- C_3 is available after $7\mathcal{T}$.
- C_4 is available after $9\mathcal{T}$.

So the delay of 4-bit ripple carry adder is $9\mathcal{T}$.

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4-bit Adder

Carry Look Ahead Logic

$S_i = C_i \bigoplus (A_i \bigoplus B_i)$

$C_{i+1} = A_i B_i + C_i(A_i \bigoplus B_i)$

Let $G_i = A_i.B_i$ and $P_i = A_i \bigoplus B_i$

then $S_i = C_i \bigoplus P_i$

$C_{i+1} = G_i + C_i P_i$

So the value of C_1, C_2, C_3, C_4 are:

$C_1 = G_0 + C_0 P_0$

$C_2 = G_1 + C_1 P_1 = G_1 + G_0 P_1 + C_0 P_0 P_1$

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$C_4 = G_3 + C_3 P_3$

$\quad = G_3 + G_2 P_3 + G_1 P_2 P_3 + G_0 P_1 P_2 P_3 + C_0 P_0 P_1 P_2 P_3$

G_i and P_i are available after $1\mathcal{T}$.

Thereafter C_1, C_2, C_3, C_4 are available in $2\mathcal{T}$.

Thereafter S_0, S_1, S_2, S_3 are available in $1\mathcal{T}$.

$\therefore$ Delay of CLA is $4\mathcal{T}$.

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G_i and P_i are available after $1\mathcal{T}$.

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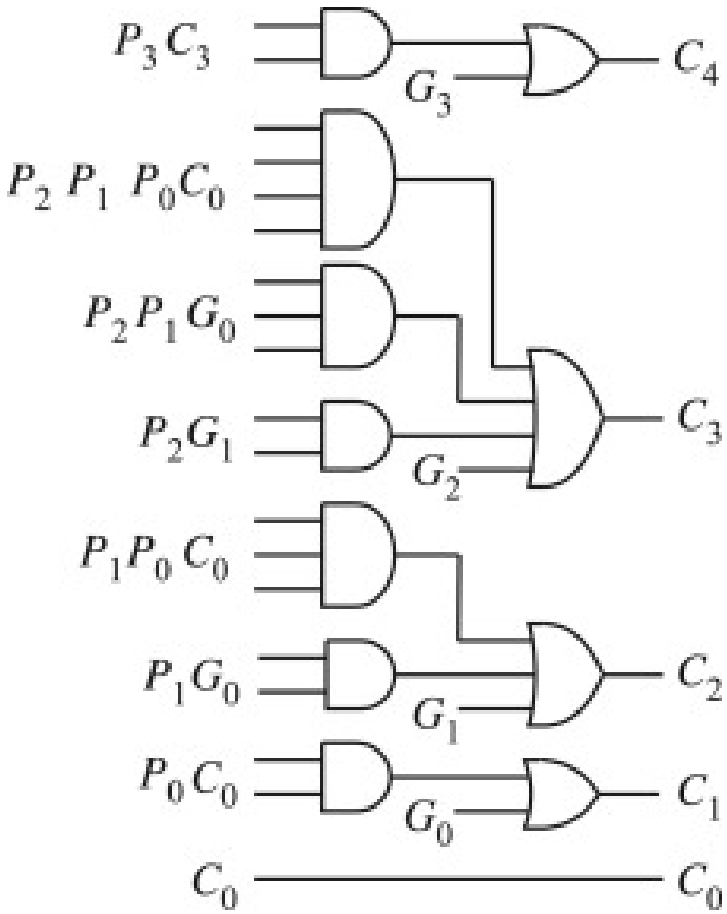
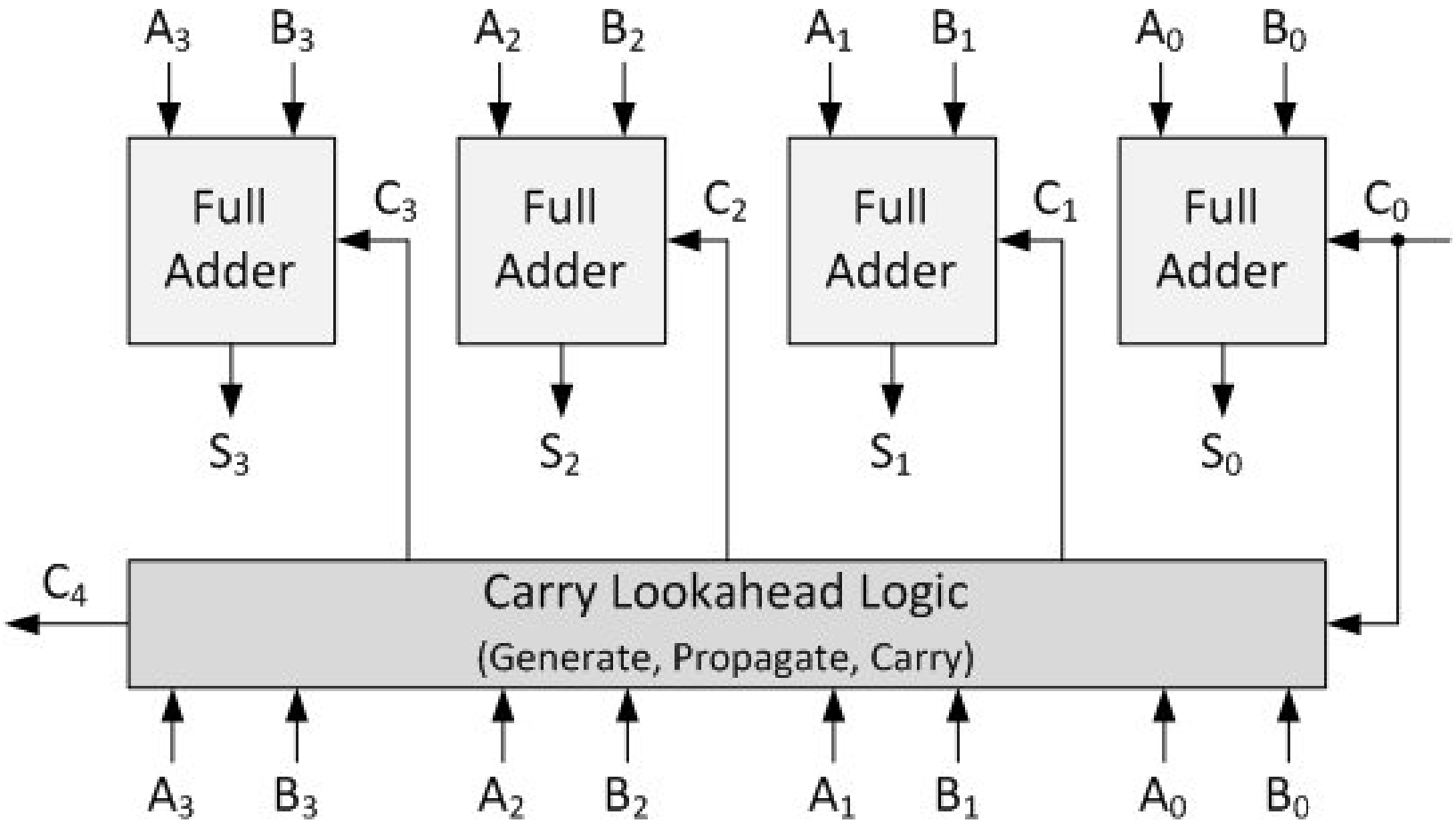
Carry Look Ahead Circuit



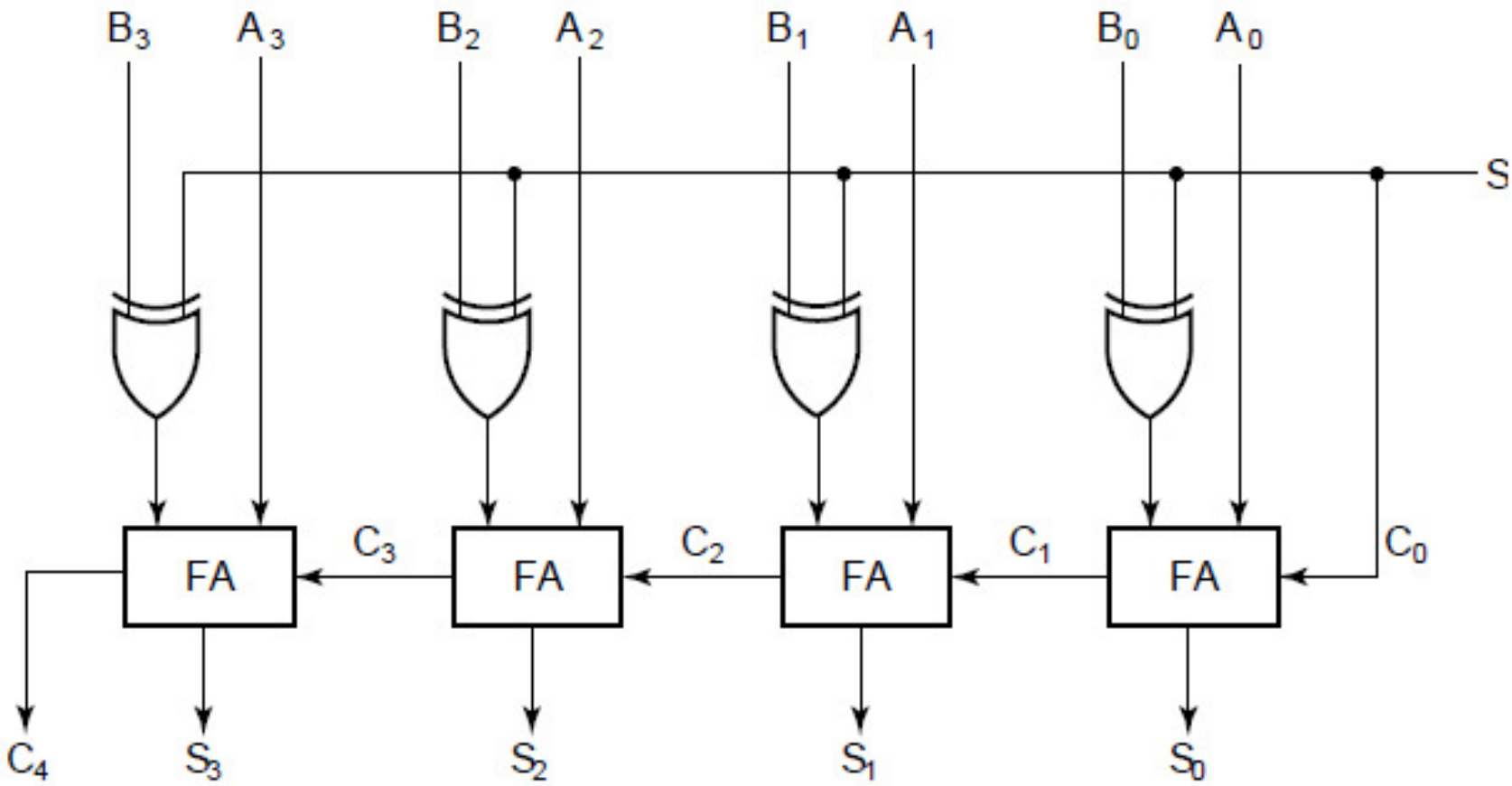
4-bit Adder using CLA Logic



Think and Try

1. Speedup of 4-bit CLA adder as compared with 4-bit RCA(Ripple Carry Adder).
2. How to design a 16-bit adder using 4-bit RCAs.
3. How to design a 16-bit adder using 4-bit CLAs.
4. Latency of N-bit adder using L-bit CLAs.
5. How to design a 64-bit adder using 16-bit adders. The 16-bit adders are designed using 4-bit CLAs.

A 4-bit adder or subtractor



Write equations for Carry(C) and Overflow detection.

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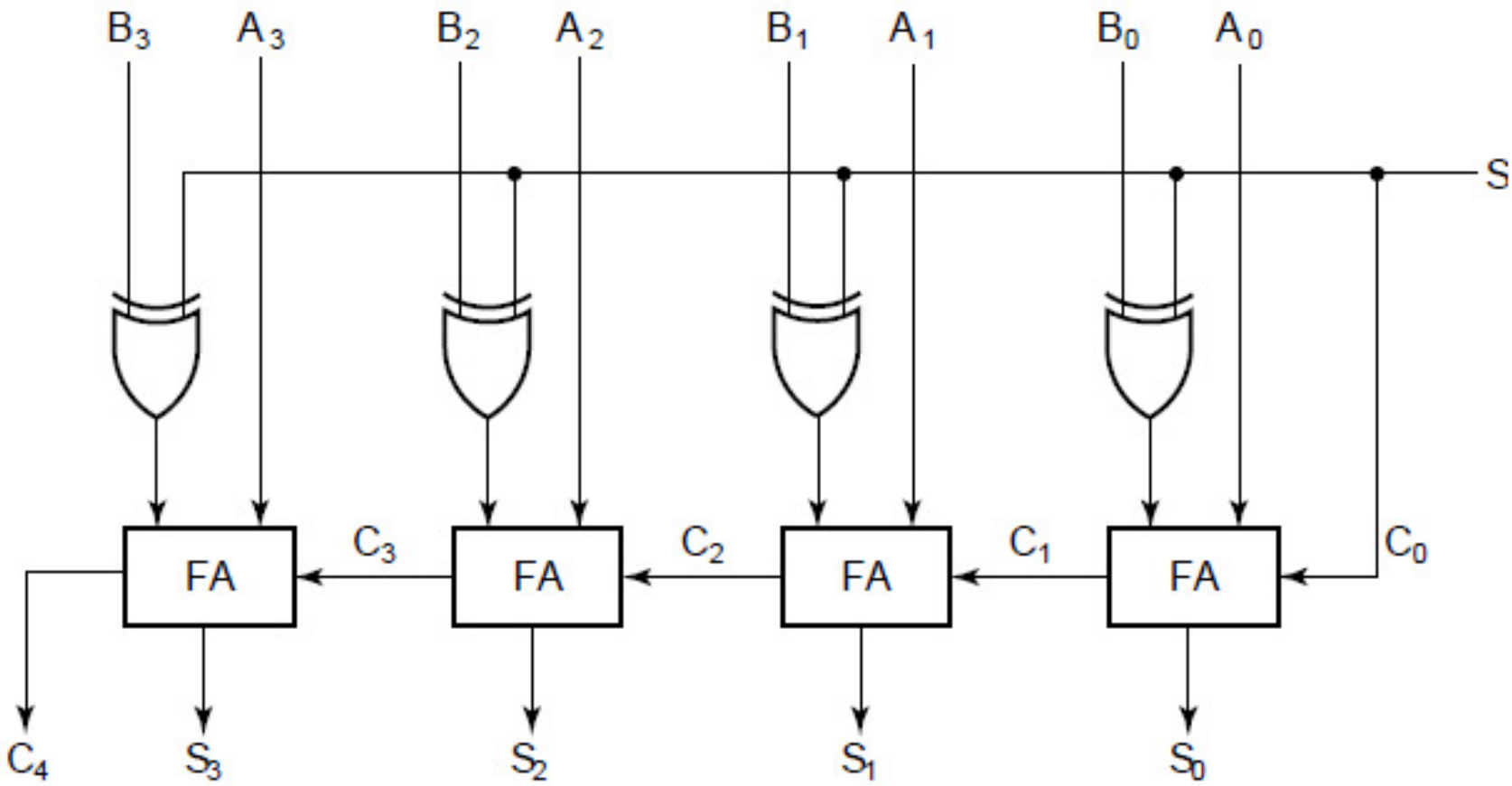

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