CO: Computer Organization

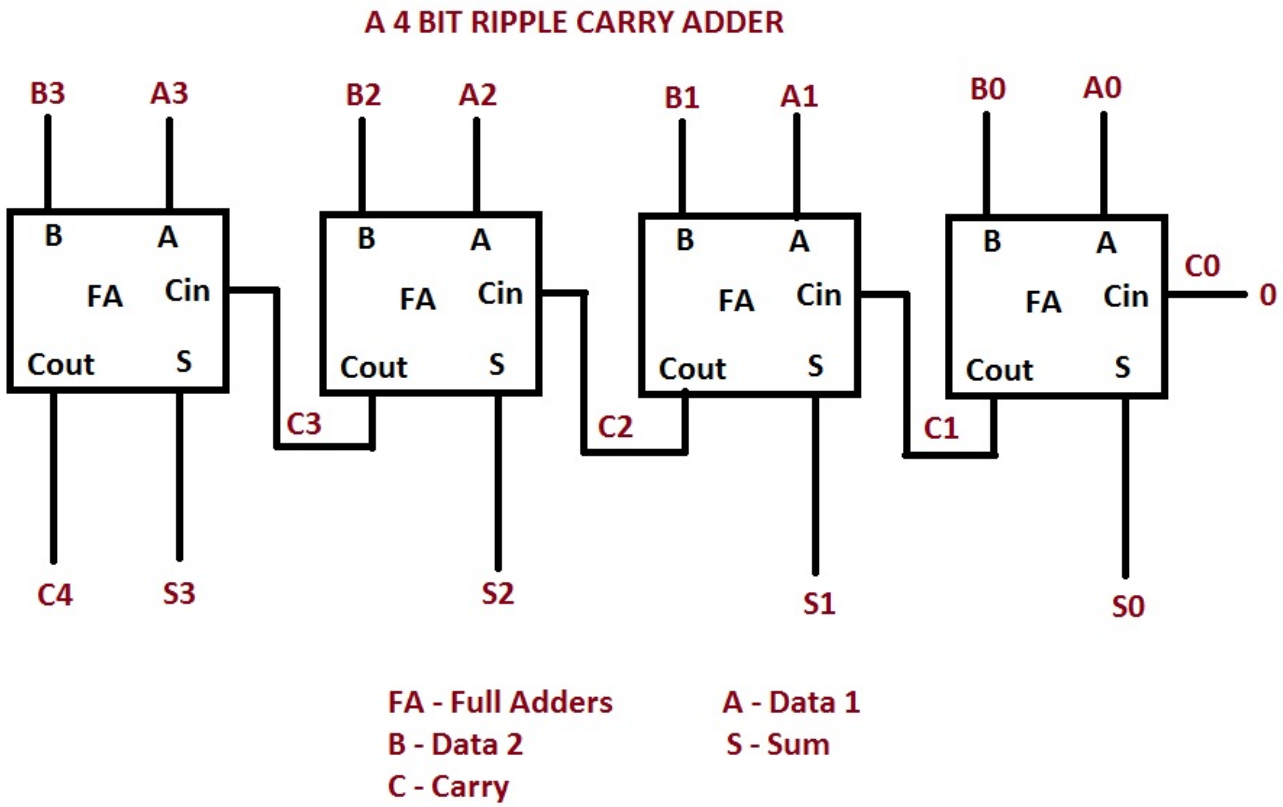
Day 4

Indian Institute of Information Technology, Sri City

Jan - May - 2018

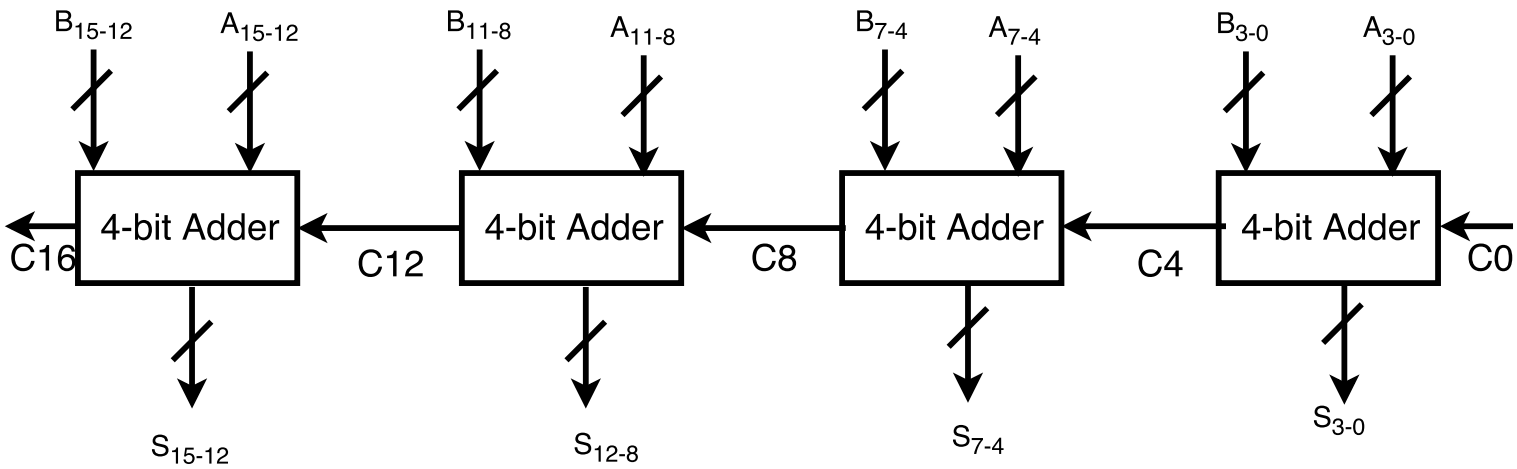
http://co-iiits.blogspot.in/

Arithmetic Operations on Integers



Arithmetic Operations on Integers

A 16-bit Ripple Carry Adder



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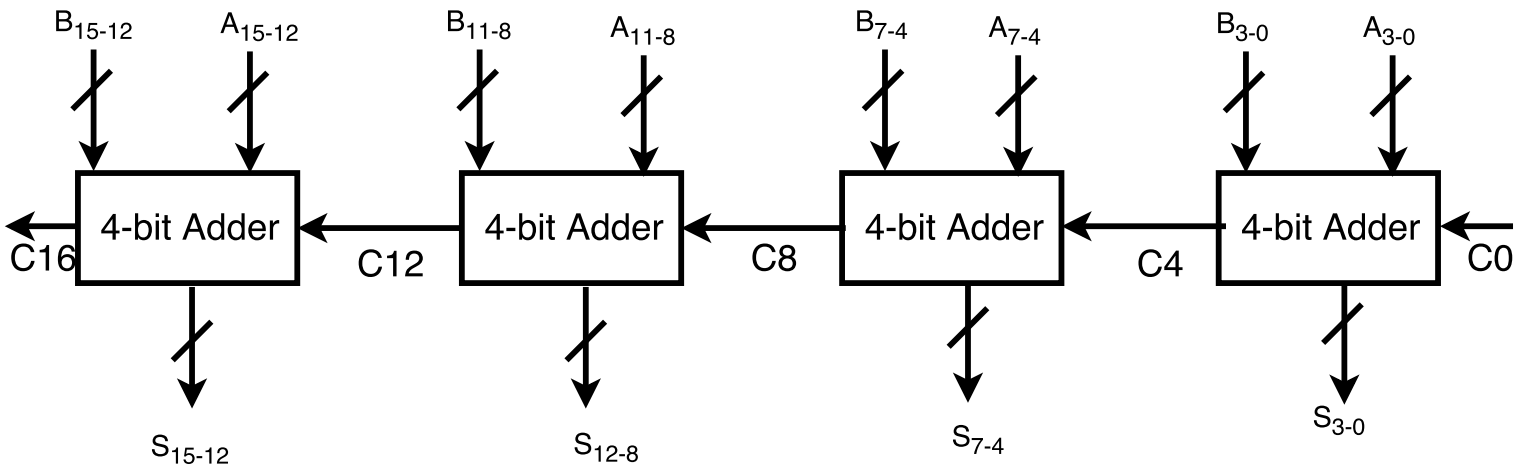

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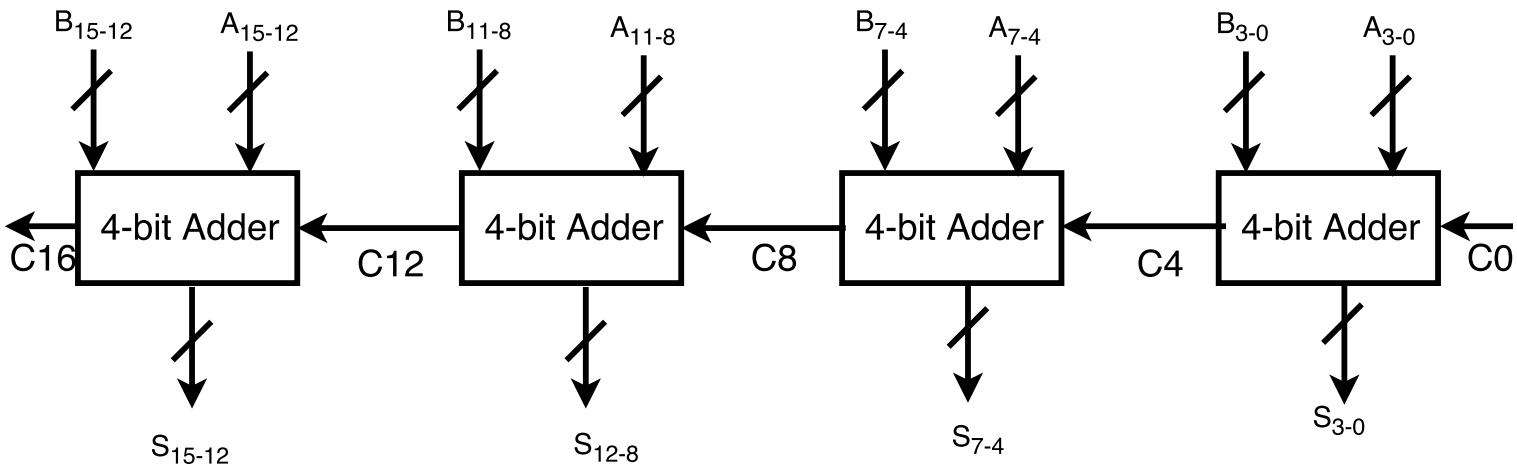

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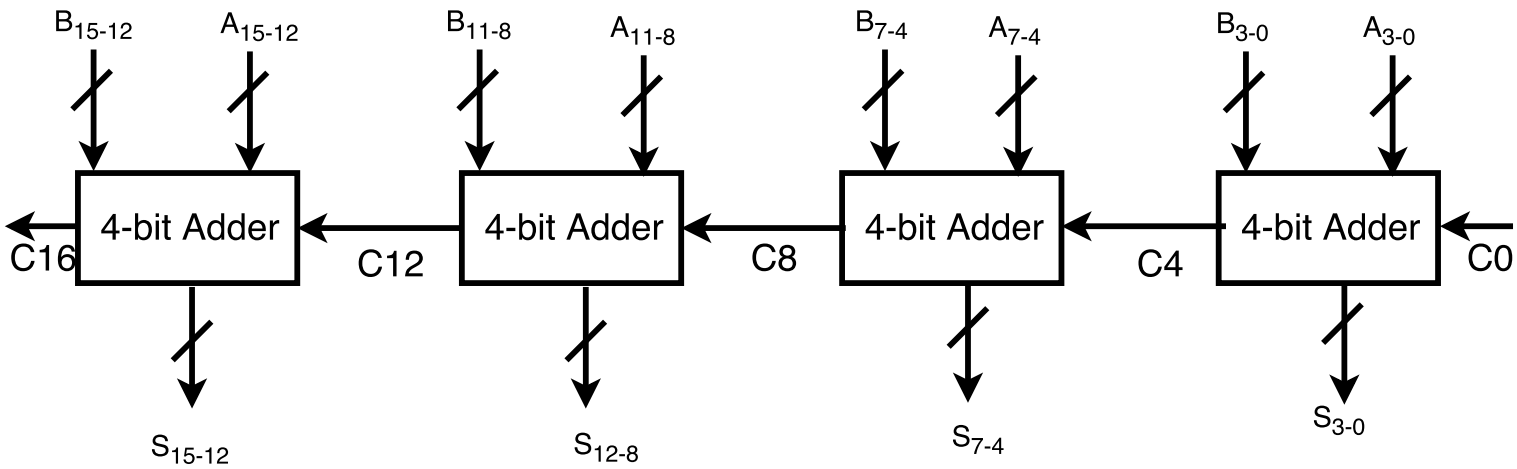

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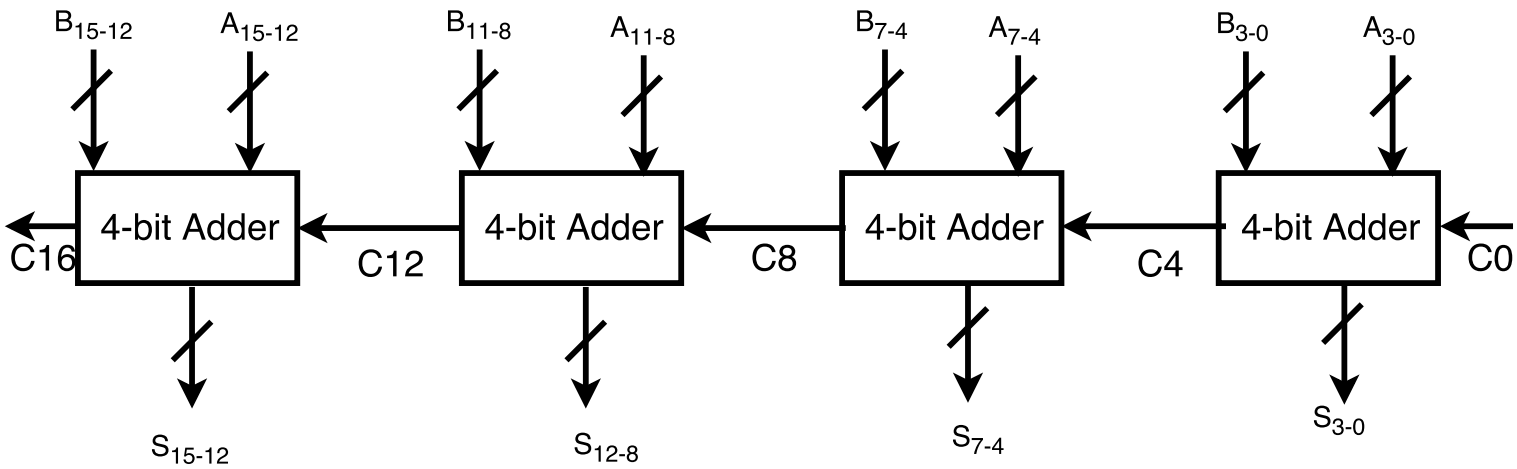

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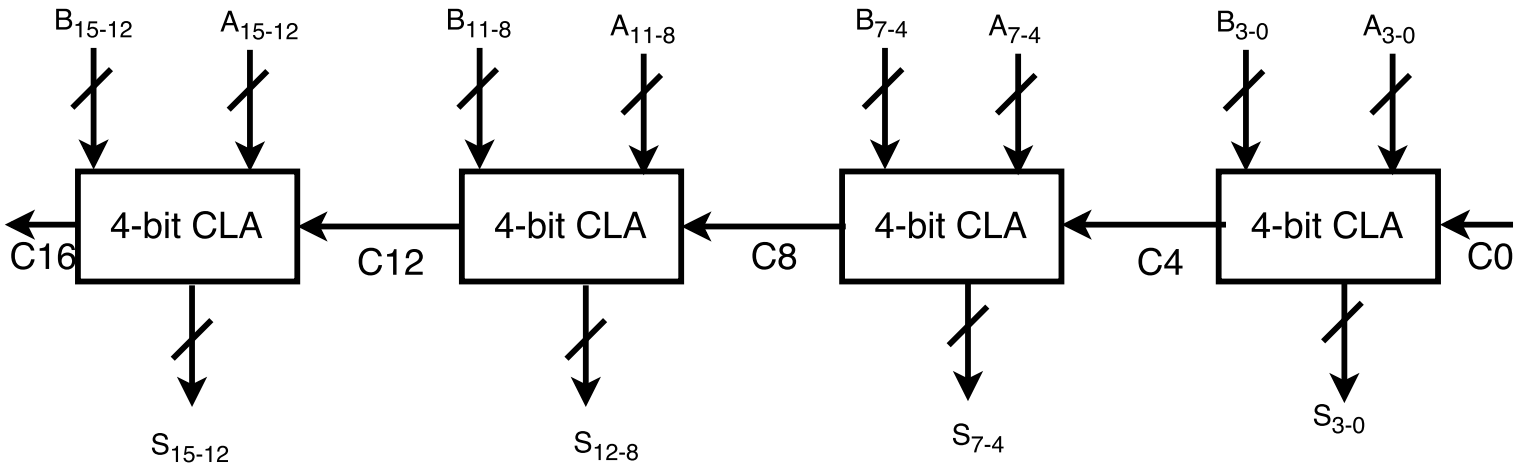
Arithmetic Operations on Integers

A 16-bit adder using 4-bit CLAs



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$\therefore$ Latency of N-bit Adder using L-bit CLAs :$(2\frac{N}{L}+2)\mathcal{T}$.

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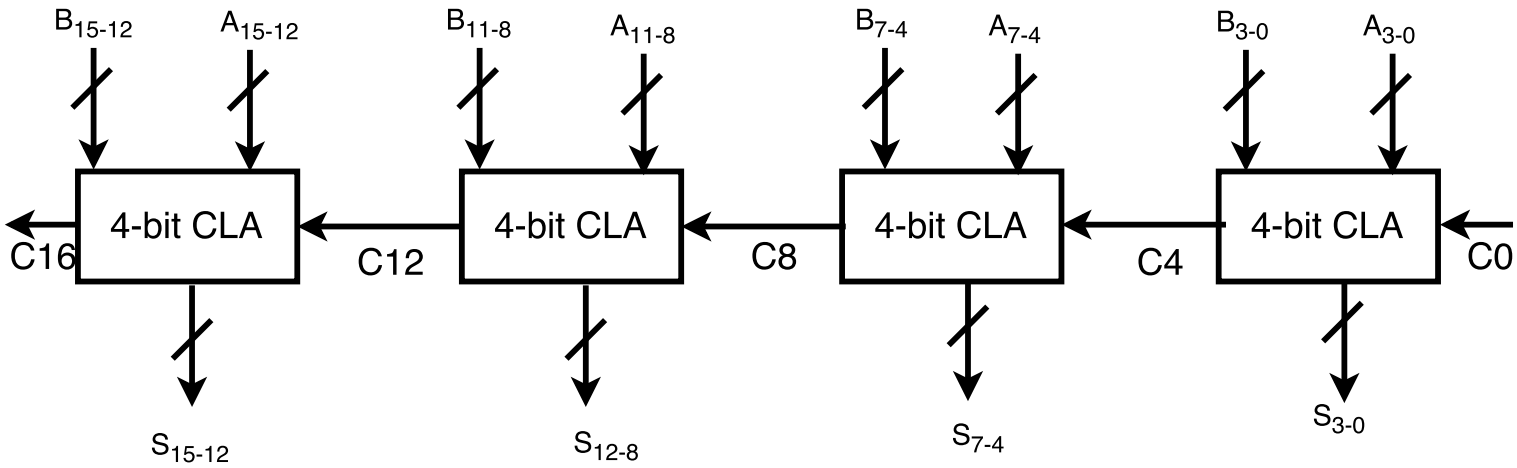

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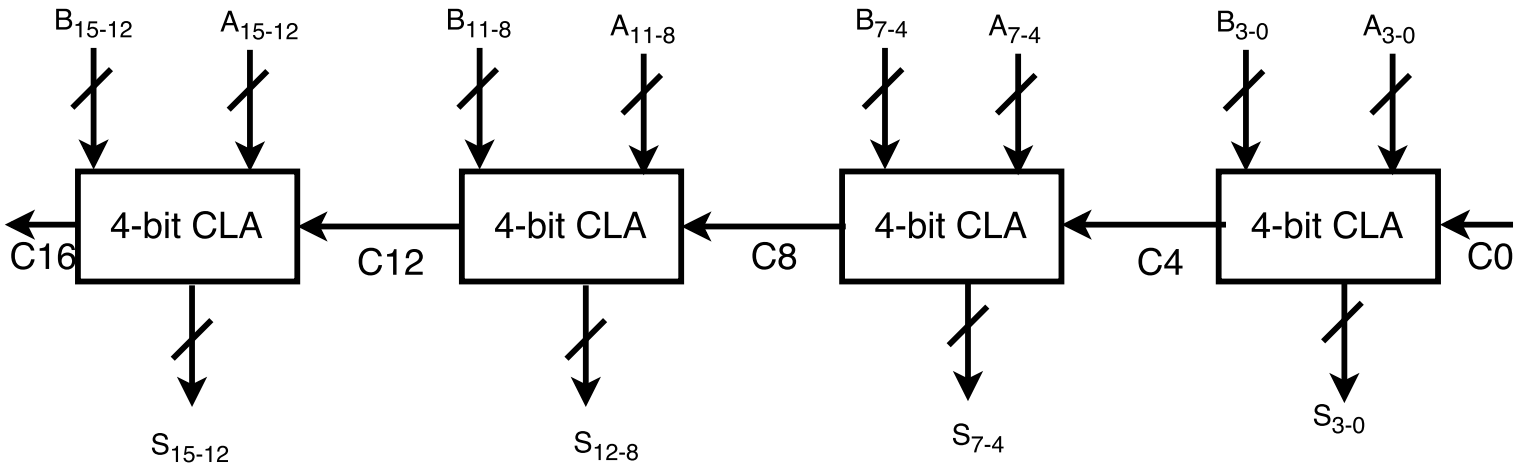

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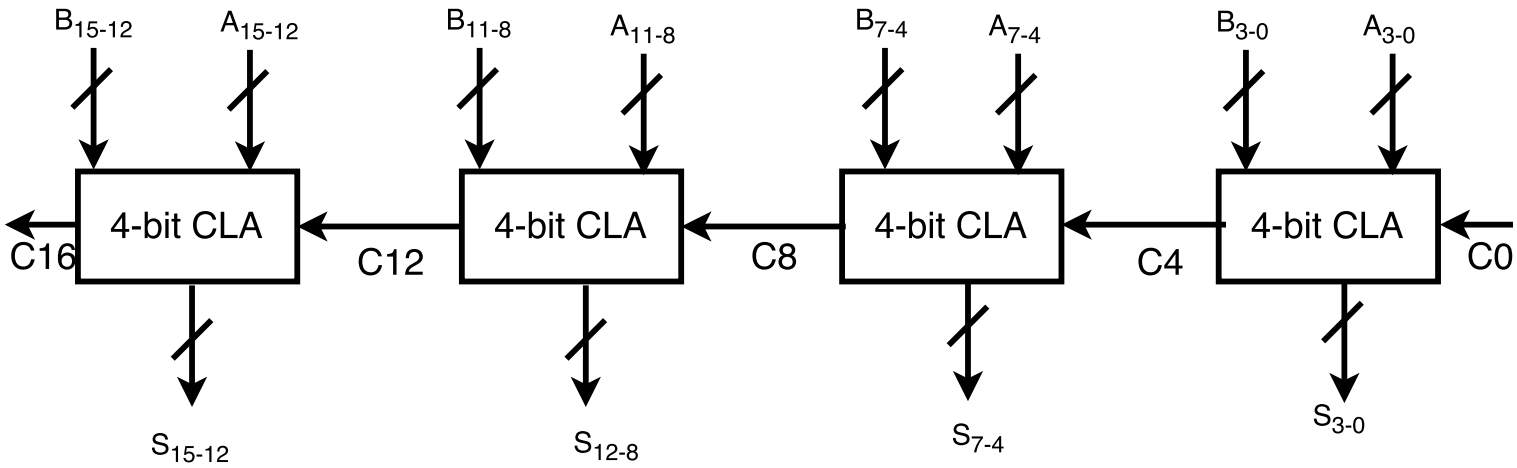

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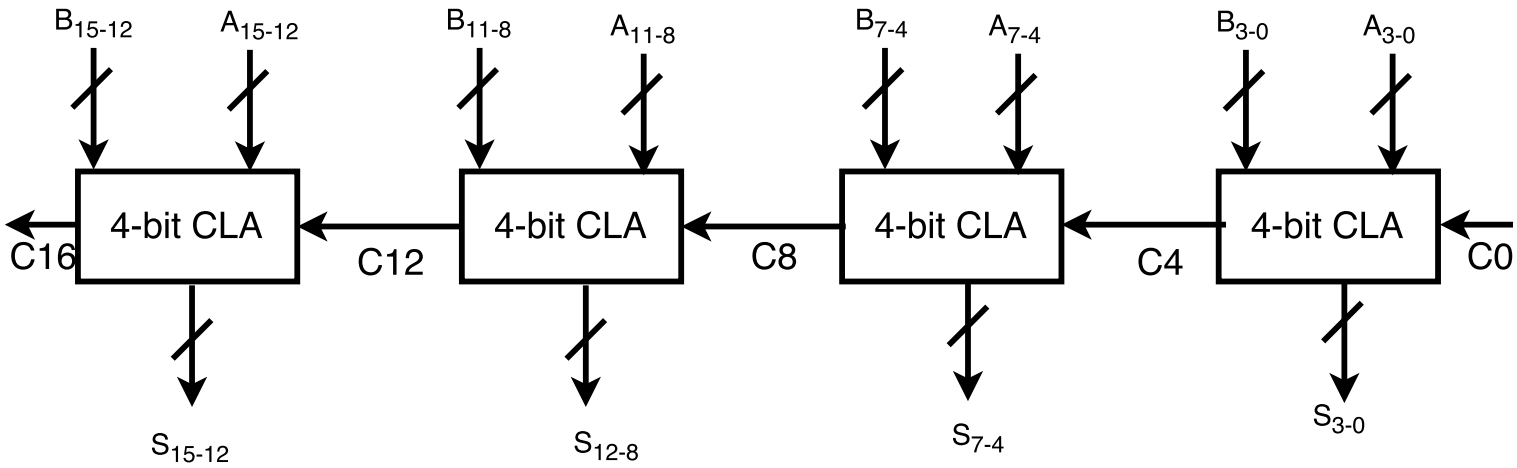

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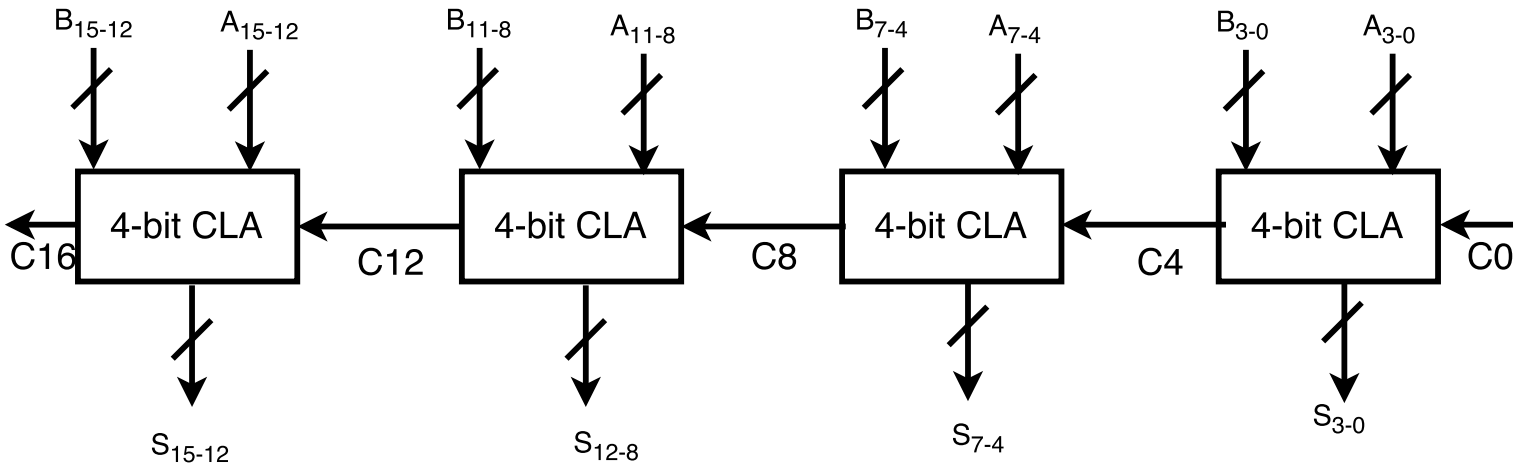

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'M' Integer Additions.
Each Integer of size N-bits.

1. **Using N-bit adders and L-bit CLAs:** $M(2\frac{N}{L}+2)\mathcal{T}$.
2. How could we design a Pipeline Adder. ? ☺
3. Pipeline can have $\frac{N}{L}$ Stages.
4. In each stage performs L-bit addition using CLA Adder.

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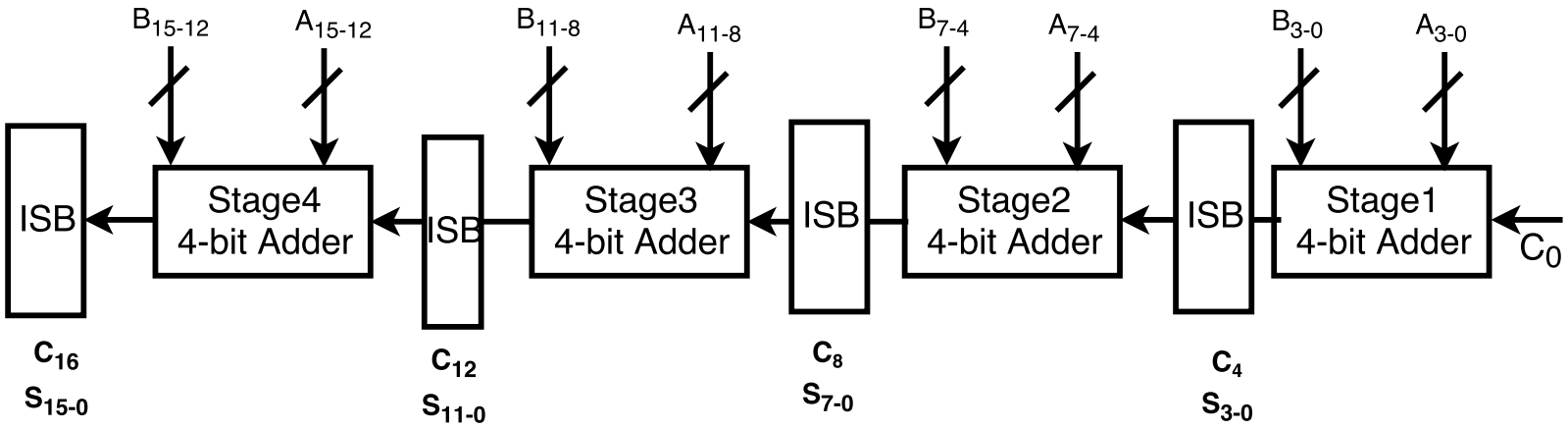
4-Stage Pipeline Adder



$$X_1 Y_1 (S_{3-0})$$

$$X_1 Y_1 (S_{7-0}) \quad X_2 Y_2 (S_{3-0})$$

$$X_1 Y_1 (S_{11-0}) \quad X_2 Y_2 (S_{7-0}) \quad X_3 Y_3 (S_{3-0})$$

$$X_1 Y_1 (S_{15-0}) \quad X_2 Y_2 (S_{11-0}) \quad X_3 Y_3 (S_{7-0}) \quad X_4 Y_4 (S_{3-0})$$

The delay of a 4-bit adder is $4\mathcal{T}$ and a ISB (Inter Stage Buffer) is $2\mathcal{T}$.

$\therefore$ **Duration of pipeline clock signal is: $6\mathcal{T}$.**

Then the time to perform 'M' additions is: $(4 + M - 1)6\mathcal{T}$.

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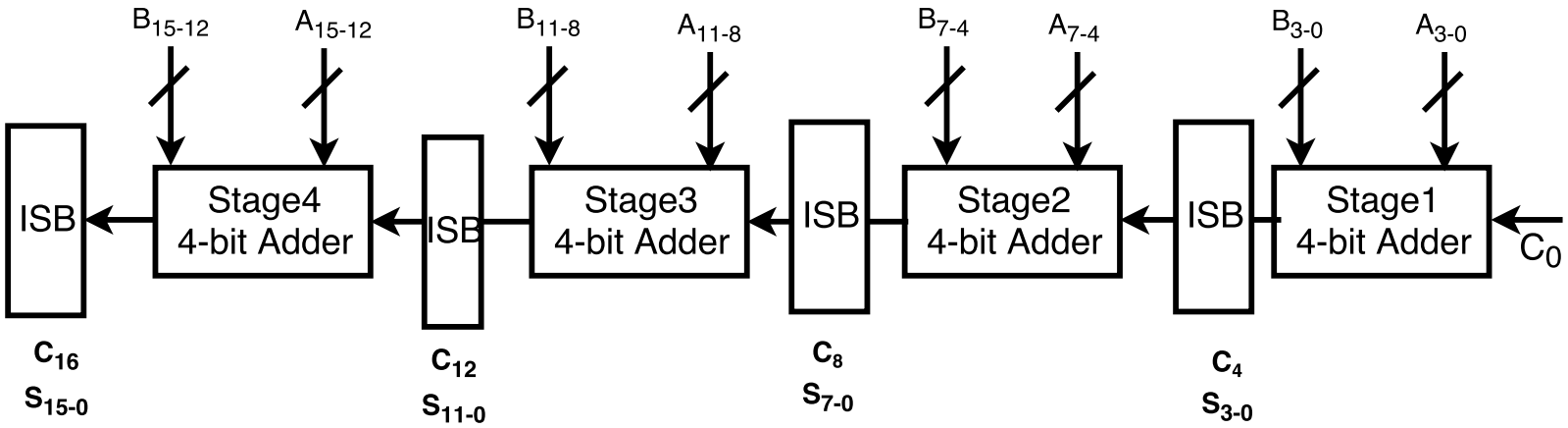

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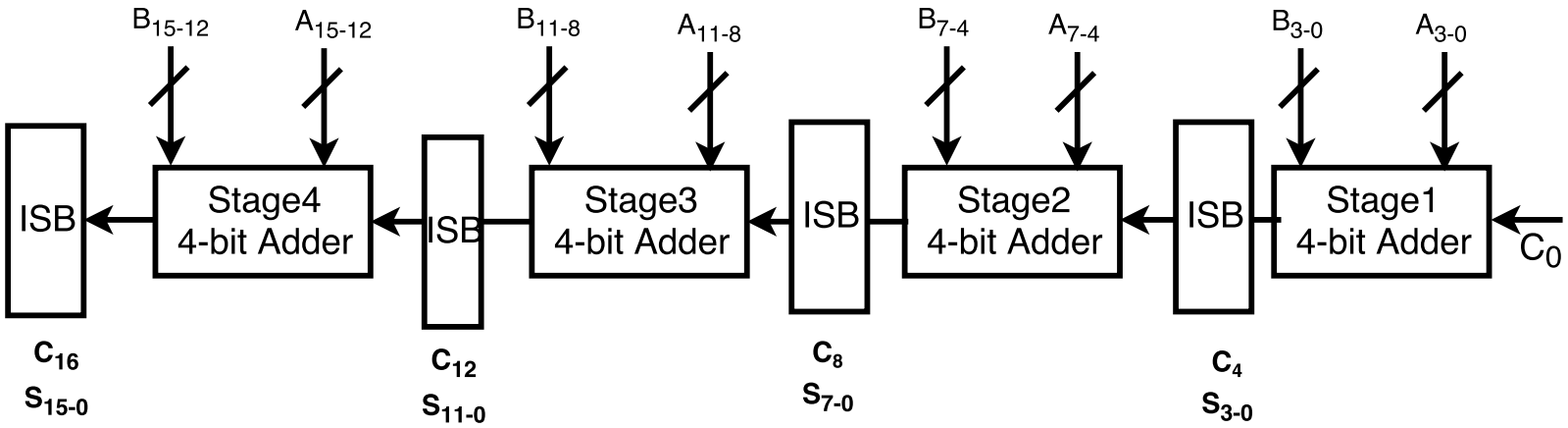

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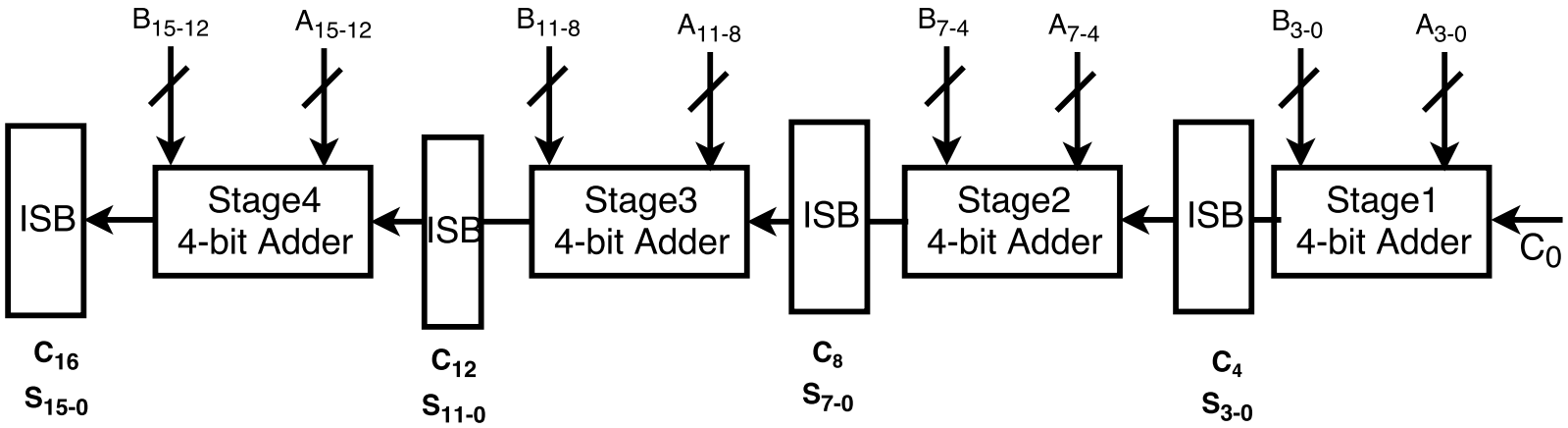

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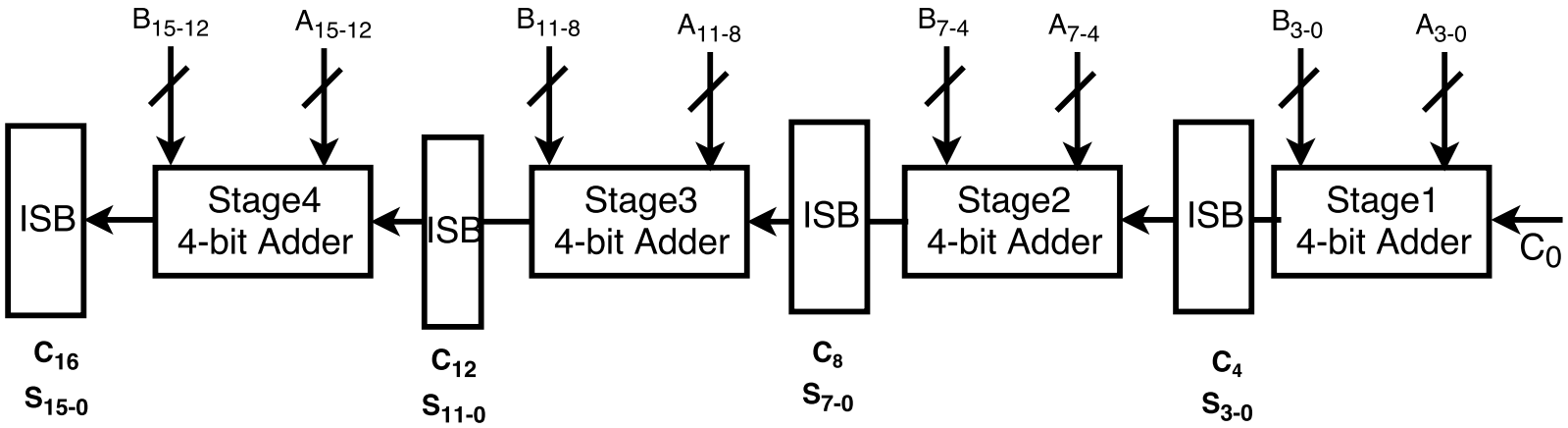

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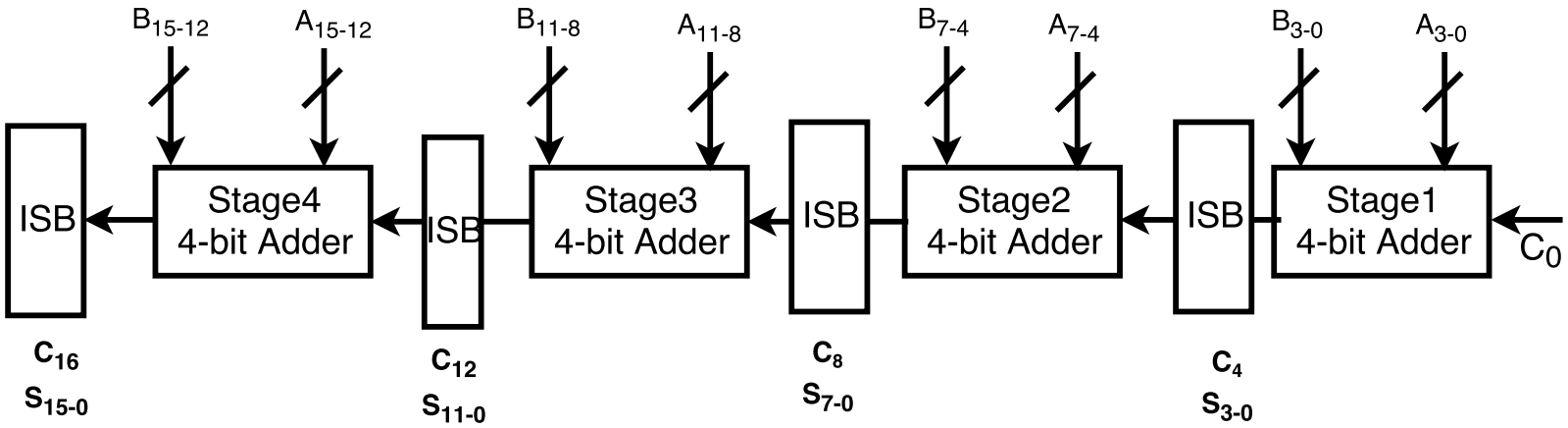

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