EC3057D Modelling and Testing of Digital Systems
Winter 2021

Assignment - 2

Guidelines for preparing report:

1. Report should contain Question, Gate level Circuit diagram and/or Truth Table, Verilog Code including testbench and Simulation Waveform.
2. Testbench is mandatory for all the designs.
3. Use the font **`Courier New size 10 Bold`** for Verilog code
4. Use font Times New Roman, size 12 for text, 14 for headings and single line spacing.
5. **Do all the simulations and prepare the report on your own. If found to be copied, marks will not be awarded for Assignments.**

Exercises

1) Write a behavioral level Verilog code for a 4-bit mod-13 up-down counter and a testbench to verify.

2) Write a module in Verilog called **`bitreverse`** that has one input and one output signal. Output should be the bit reversed version of the input signal. Size of the signal is defined as a parameter called MAXBITS with a default value of 32. Implement the bit reversal as a
   a) Function
   b) Task
   Write different testbenches by instantiating the DUT with different parameter values 4 and 8. Simulate and display the results for atleast four different input signals.

3) Draw the state transition diagram of a sequence detector which detects 0011 using Moore FSM. Assume LSB enters the system first. Model this FSM in Verilog using separate always blocks for next state logic, sequential logic and output logic. Write a testbench to verify the design.

4) Write a parameterized N-bit ripple carry adder using generate statements. Write two different testbenches – one for verifying 8-bit adder and another for verifying a 16-bit adder by overriding the parameter value of the design.