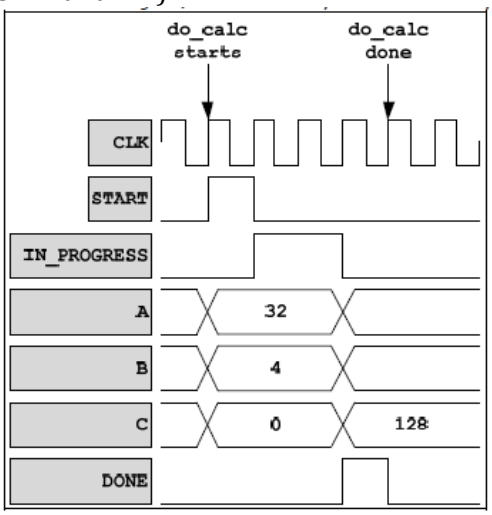
National Institute of Technology Calicut
Department of Electronics and Communication Engineering
B. Tech, Winter Semester 2019 – 2020
S6 End Semester Examination, August 2020
EC3057D Modeling and Testing of Digital Systems

Total Marks: 20 **Duration: 2 Hours**

1. Create a Verilog task called do_calc that mimics the following waveform. Assume that the clock is provided by another piece of code and task is responsible for driving the values of START, IN_PROGRESS, C and DONE. The values must be visible externally while they are toggling. The values A, B and C are integers (make "A" and "B" inputs, and "C" is an output, which gives the multiplied result of the inputs "A" and "B"). **(3 Marks)**



2. Draw the circuits that corresponds to the following codes. **(1.5 + 1.5 = 3 Marks)**

a.
```
module lfsr1(
      input [2:0] R,
      input Load,
      input Clk,
      output reg [2:0] Q
      );
  always@ (posedge Clk)
    if (Load)
      Q <= R;
    else
      Q <= {Q[1], Q[0]^Q[2], Q[2]};
  endmodule
```

b.
```
module lfsr2(R, Load, Clk, Q);
  input [2:0] R;
  input Load, Clk;
  output reg [2:0] Q;
  always@ (posedge Clk)
     if (Load)
       Q <= R;
     else begin
       Q[0] = Q[2];
       Q[1] = Q[0] ^ Q[2] ;
       Q[2] = Q[1];
     end
  endmodule
```

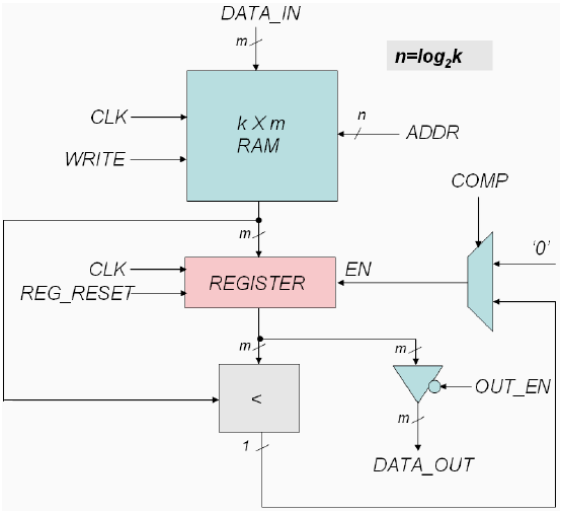
3. An RTL description for a circuit is given below. **(1.5 + 0.5 = 2 Marks)**

```
module circuit1(x, y, a, b, c, d);
parameter x_delay = 3, y_delay = 7;
input a, b, c, d;
output x, y;
assign #y_delay y = (a | b) & (c | ~d);
assign #x_delay x = a ^~ b;
endmodule
```

   a. Rewrite the circuit1 using Verilog built-in primitives as structural code. The design should have the same overall delays (from module inputs to module outputs) as the original code.

b. Show how to use the `timescale directive so that the x_delay and y_delay correspond to 0.3 ns and 0.7 ns, respectively and the simulator time step is 1 ps.

4. Write a Verilog behavioural code for the following figure for k = 256 and m = 16 and "<" indicates "less than" operation. **(5 + 2 = 7 Marks)**



a. Write a self-checking testbench that generates all the combinations of the inputs and verifies the correctness of the output for the design in Q4.

5. Consider the following Verilog module **(5 Marks)**

```
module gcd(clk,start,Ain,Bin,answer,done);
input clk,start;
input [15:0] Ain,Bin;
output reg [15:0] answer;
output reg done;
reg [15:0] a,b;
  always @ (posedge clk) begin
     if (start) begin a <= Ain; b <= Bin; done <= 0; end
     else if (b == 0) begin answer <= a; done <= 1; end
     else if (a > b) a <= a – b;
     else b <= b – a;
  end
endmodule
```

Complete the timing diagram below. Use "???" to indicate values that cannot be determined from the information given.