MTDS

Kevin Joji Mathews

Date: B180880EC

END EXAM

1. task gensig (output A, G1, G2);
   begin
   A = 0;
   G1 = 0;
   G2 = 1;
   #40 A = 1;
   #20 G1 = 1;
   #20 G2 = 0;
   #20 A = 0;
   #20 G1 = 0;
   #20 G2 = 1;
   #20;
   end
endtask

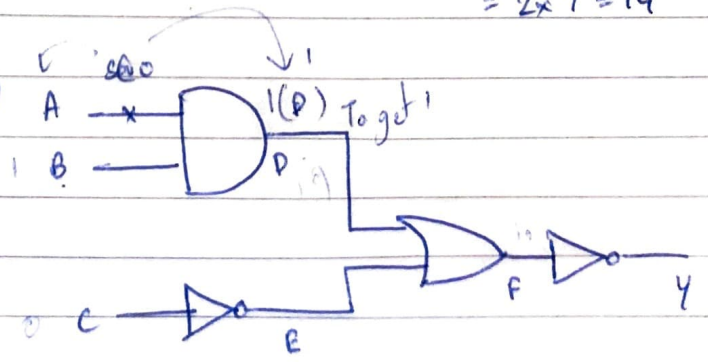
To invoke, inside the module write after mentioning A, G1 & G2 as op-

always
gensig (A, G1, G2);

3. No. of lines, k = 7
∴ No. of single stuck at ~~fault~~ faults possible = 2k
= 2 × 7 = 14

A s@0
∴ Test vector = 11

A s@1
Test vector = 0



Alwin Joji Mathews

Date: B1S0S8O8C

A s@1

Test vector = 011

B s@0

Test vector = 111

B s@1

Test vector = 101

C s@0

Test vector = 0X1 , X01

C s@1

Test vector = 0X0 , X00

D s@0

Test vector = 111

D s@1

Test vector = 0X1 , X01

E s@0

Test vector = 0X0 , X00

E s@1

Test vector = 0X1 , X01

F s@0

Test vector = ~~110 111 000 000~~ XX0 , 11X

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Date: B180550EC

F s@1
Test vector = 0x1, x01

Y s@0
Test vector = 0x1, x01

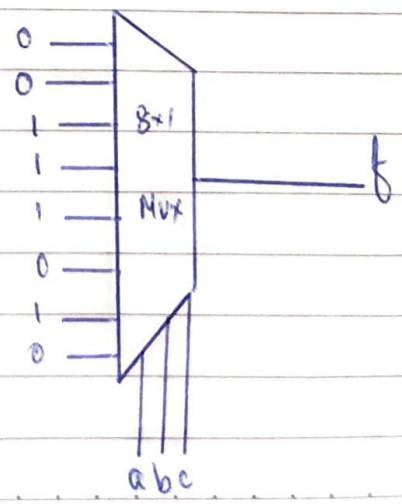
Y s@1
Test vector = xx0, 11x

Test vector	Faults detectable
011	A1, C0, D1, E1, F1, Y0
111	A0, B0, D0, F0, Y1
101	B1, C0, D1, E1, F1, Y0
000	C1, E0, F0, Y1

∴ Min no of test vector to detect all faults = 4.

2. $f = a\bar{c} + \bar{a}b$

a	b	c	f
0	0	0	0+0=0
0	0	1	0+0=0
0	1	0	0+1=1
0	1	1	0+1=1
1	0	0	1+0=1
1	0	1	0+0=0
1	1	0	1+0=1
1	1	1	0+0=0



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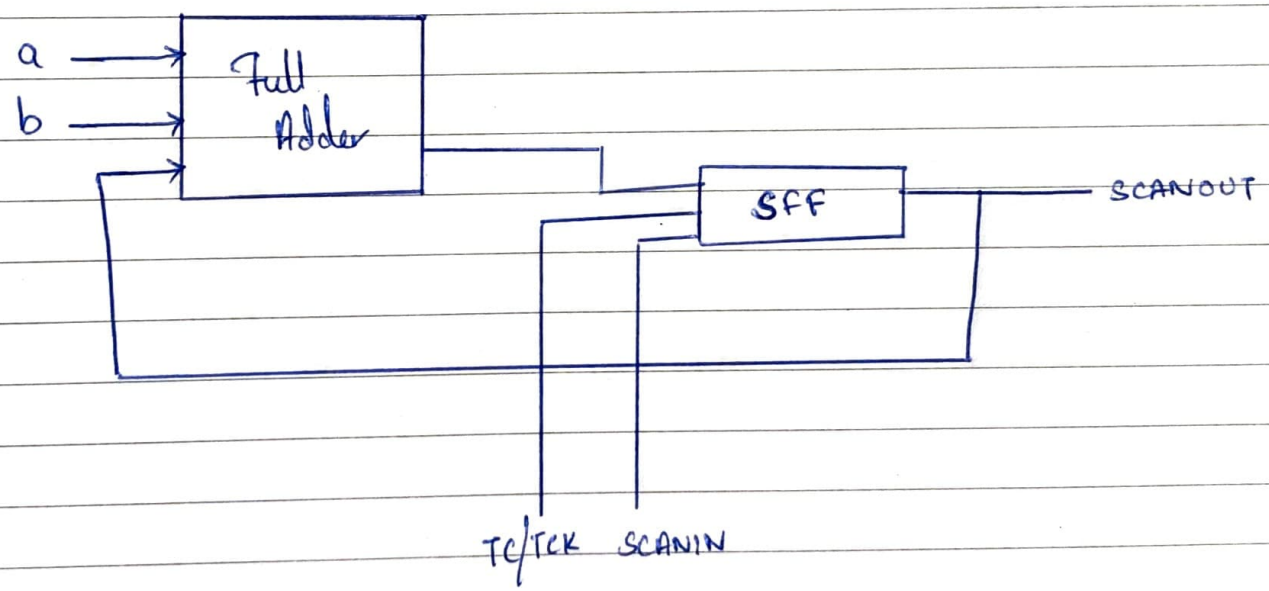
5 Since LFSR requires a fewer number of hardware than a binary counter in BIST architecture, it is less expensive and is hence more preferred method.

6. Since it is impossible to store all the output responses on chip or board or in the system to perform bit by bit comparisons. Output response compactor is used to compact the output responses into a signature, which is then compared with a golden signature.

4. A scan method is preferred for the serial adder ckt.
In this method we change the flip flop with a scan flip-flop (SFF).



And now we test the scan ckt.
2 phases → Shift & Combinational tests.

In the shift test
- We toggle a sequence 0011001100... of length 5 (nsff+1) in the SCANIN
- The reason why we use this particular sequence is because it tests all possible combinations, 00, 01, 10 & 11.

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- This test covers most of the single stuck at faults in the FF and also ~~the~~ checks the correctness of the shift operation.

In the combinational test.

- We first add the primary input signals and switch the system to test mode.
- Then we add the scan test patterns and apply a ~~clk~~ test clock (TC), until the flip flop is set.
- Then switch to normal mode and apply a functional clk.
- Probe the primary out signals, switch to test mode and SCAN OUT.