EC3057D Modelling and Testing of Digital Systems
Winter 2021

Assignment – 1

Deadline: 20/02/2022, 6.00PM

Guidelines for preparing report:

1. Start preparing your report well in advance instead of doing everything close to the dead line.
2. Report should contain Question, Gate level Circuit diagram and/or Truth Table, Verilog Code including testbench and Simulation Waveform.
3. Circuit Diagrams may be neatly hand-drawn. Make sure that all signals both at the interface and internal signals are named properly and use the same name in the code. Name all the instances as well.
4. Testbench is mandatory for all the designs.
5. Use the font **`Courier New size 10 Bold`** for Verilog code
6. Use font Times New Roman, size 12 for text, 14 for headings and single line spacing.
7. **Do all the simulations and prepare the report on your own. If found to be copied, marks will not be awarded for Assignments.**

Exercises

1) Write structural level Verilog code of the following:
    a) 2x1 Mux
    b) 4x1 Mux
    c) 4x1 Mux using 2x1 Mux
    d) 8x1 Mux using 4x1 and 2x1 Mux
    e) Half Adder
    f) Full Adder using Half Adders
    g) 4-bit Ripple Carry Adder using Full Adders

2) Write data flow level Verilog code using conditional operator for the following:

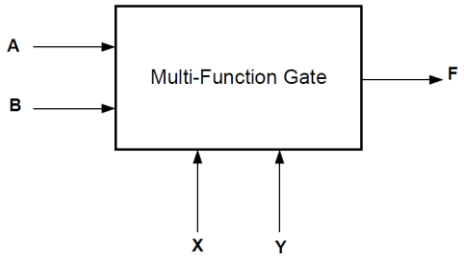
   a) 2x1 Mux

   b) 4x1 Mux

   c) 2 to 4 Decoder

   d) 4 to 2 Encoder

3) Design a Multi-function gate which can work as a two input (A, B) one output (F) logic gate based on the control values placed on two other inputs X and Y. Control input values and the corresponding function is given in the table below. After obtaining the schematic, write structural level verilog code for it.



X	Y	Function
0	0	AND
0	1	OR
1	0	NOR
1	1	NAND

4) Write behavioral level Verilog code for the following:

   a) T Flip flop

   b) 4-bit up-down counter

   c) 8-bit shift register which is capable of doing right shift and left shift

   d) 4-bit Johnson counter