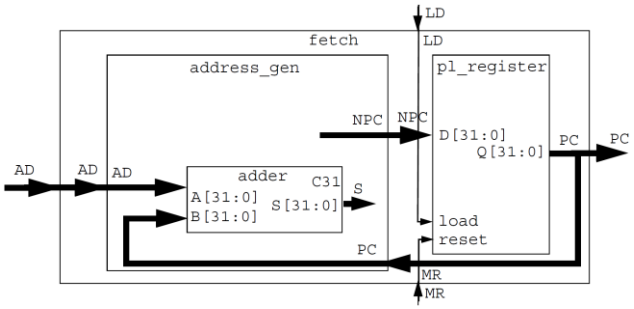
EC3057D Modeling and Testing of Digital Systems
Quiz – 12 April 2021

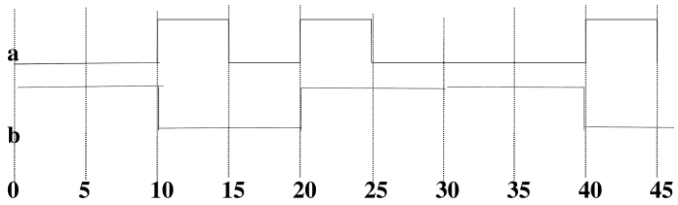
Time: 60 min Maximum Marks: 10

Answer **All** the questions

1. Write the Verilog module, input, output, declarations, instantiations and endmodule statements for the hierarchical circuit described by the following diagram. Carefully declare the required signals using proper names as mentioned in the diagram with appropriate size. Do not change the name of the signals. It is not required to describe the functionality. **(4M)**



2. Write separate always blocks containing statements that will generate the following waveforms on signals ‘a’ and ‘b’ that repeat every 30 ns as shown below. **(2M)**



3. Write a behavioural verilog code for a loadable N bit shift register with synchronous reset. Show how to get 32 bit and 64 bit shift registers using this inside another module. **(4M)**