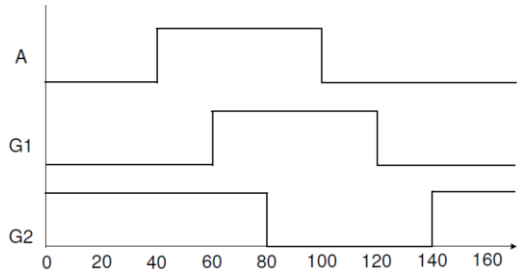
EC3057D Modeling and Testing of Digital Systems

End Semester Examination – 11 May 2021

Time: 90 min Maximum Marks: 20

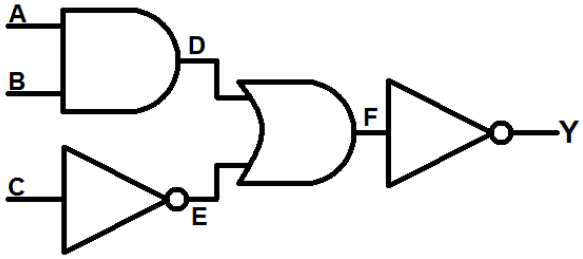
Answer **All** the questions

1. Write a Verilog task named **`gensig`** and generate the signals as shown in the figure below. Show how to invoke the task such that the signals are generated periodically every 160 time units. **(4M)**

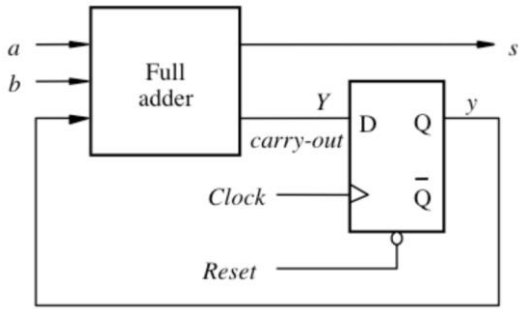


2. Show how a 3-LUT can be used to implement the logic function f=ac'+a'b **(3M)**

3. How many single stuck at faults are possible in the logic circuit given below? Determine all the test vectors that could be used to detect each of those faults. What is the minimum number of test vectors required to detect all the faults and list those test vectors? Show all the steps. **(6M)**



4. Demonstrate a suitable DFT technique for the Serial Adder circuit shown below. Draw the circuit with DFT inserted and write the steps in detail. **(5M)**



5. Why is LFSR preferred over a binary counter in BIST architecture for test vector generation? **(1M)**

6. What is the advantage of using an output response compactor in BIST architecture? **(1M)**