National Institute of Technology Calicut

Department of Electronics and Communication Engineering

EC3057D Modelling and Testing of Digital Systems, Quiz, June 2020

Total Marks: 30 Answer All Questions **Duration: 60Min**

Part A – 1 mark for each question

1. _____ is the keyword used to drive a value onto a net in dataflow modeling.

2. If A=1'b1, B=2'b01, C=2'b00 then y = {4{A},2{B},C} equals ----------

3. The left hand side of continuous assignment can be
   a) Register or concatenation of registers b) Can be both registers or nets
   c) Net or concatenation of nets d) Array of registers

4. The expression 3'b1xx !== 3'b1xz; returns a ---------

5. What is the time period of clock #15clock = ~clock?
   a)25 b) 15 c)7.5 d) none of the above

6. Which of the following statement is correct?
   a) A function can have nonblocking statements.
   b) A function without a range defaults to one bit reg for the return value.
   c) A function can use constructs like #.@ etc for advancing simulation-time.
   d) One can declare an object with name same as the function inside the scope of function.

7.
```
wire [7:0] net1;
wire signed [3:0] net2;
assign net1=net2;
```

   Which one of the below statements are true?
   a) Net1[3:0] is connected to net2[3:0]
   b) Net1[7:4] is connected to net2[3:0]
   c) Is an error

8. Find the answer of the following statement
```
wire signed [7:0]a=-27;
wire [7:0] b,c;
assign b= (a>>2)+(a<<2);
assign c= (a>>>2)+(a<<<2);
```

   a) b = 7'b11001101 & c = 7'b11001101
   b) b = 7'b11001101 & c = 7'b10001101
   c) b = 7'b10001101 & c = 7'b10001101
   d) b = 7'b10001101 & c = 7'b11001101

9. If a =1; assign y=(a==2'b11) then value of y will be
    a) 1
    b) 1'b0
    c) 2'b11
    d) None of above

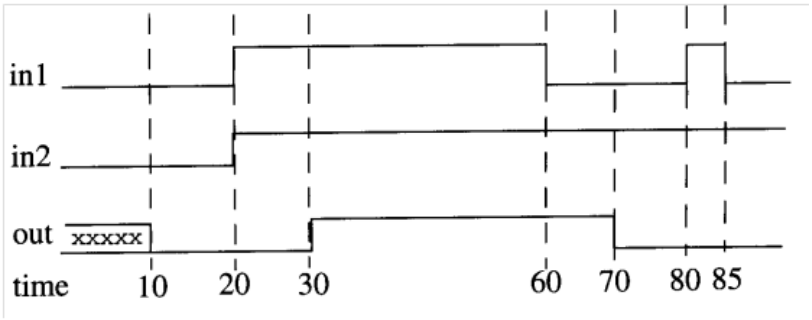
10. In a test bench, all outputs are of type
    a) wire
    b) reg
    c) variable
    d) any of the above

11. Find the final value of s, z and i in the following code?

```
module iloop(z,a);
input [31:0] a;
output z;
reg [4:0] i;
reg s, z;
initial begin
    s = 0;
    for(i=0; i<32; i=i+1)
    s = ~s;
    z = !s;
end
endmodule

a. i = 0, s = 0, z = 1
b. i = 32, s = 0, s = 1
c. i = 31, s = 1, s = 0
d. Infinite loop
e. None of the above
```

12. Write a single expression for figure below. in1 and in2 are input and are of type reg, and out is output of type wire.



13. What would be simulation time in below code when rval=10

```
`timescale 1 ns / 1 ps
module timescale_check2;
reg[31:0] rval;

initial begin
    rval = 20;
    #10.567 rval = 10;
  end

initial begin
    $monitor("TimeScale 1ns/1ps : Time=%0t,  rval = %d",$realtime,rval);
    #100 ;
  end
endmodule
```

Part B

14. Given values of *a*, *b*, and *c* as shown, write the result of expressions shown below. (2 Marks)
    Assume: a is [3:0], b is [3:0], c is [5:0]
    Assume: a = 4'b0010 , b = 4'b1010 , c = 6'b001101
    Evaluate the following expressions:

i.	a & b = ?	v.	a || b = ?
ii.	a && b = ?	vi.	a | b = ?
iii.	a - b = ?	vii.	a = c , a = ?
iv.	&b = ?	viii.	c = b , c = ?

15. Write a Verilog Code for a Mealy machine which detects an overlapping sequence of 10011. (5 Marks)

16. Draw the output waveforms for y1 to y6 for the input 'a' shown below (5 Marks)

a. always @ (a)
   y1 = a;
b. always @ (a)
   y2 = #5 a;
c. always @ (a)
   #5 y3 = a;
d. always @ (a)
   y4 <= a;
e. always @ (a)
   y5 <= #5a;
f. always @ (a)
   #5 y6 <= a;

17. Write a Verilog task to compare 2 numbers (5 Marks)