Started on	Friday, 28 January 2022, 4:30 PM
State	Finished
Completed on	Friday, 28 January 2022, 5:15 PM
Time taken	44 mins 50 secs
Grade	**17.00** out of 20.00 (**85**%)

Question **1**

Incorrect

Mark 0.00 out of 1.00

```
The value of o1 and o2 after simulation of following lines is
    wire [3:0] o1,o2;
    assign o1=(a==b)?1:0;
    assign o2=(a===b)?1:0;
    assume initial values of a=4'b1z0z;b=4'b1z0z;
```

- 4'bzzzz,4'bzzzz
- 4'b0000,4'b0000
- 4'bxxxx,4'bxxxx ✖
- 4'b0001,4'b0001

The correct answer is:
4'b0001,4'b0001

Question **2**

Correct

Mark 1.00 out of 1.00

Find the final value of 'r' considering the code below:

```
integer p, q, r;
initial
begin
p = 55; q = 20; r = 3;
p = q * r;
q = p - 25;
r = p + q;
end
```

- 35
- 75
- 90
- 95 ✔

The correct answer is:
95

Question **3**

Correct

Mark 1.00 out of 1.00

The system task '$time' returns the current simulation time as a

- 32 bit integer
- real number
- 64 bit integer ✔
- 16 bit integer

The correct answer is:
64 bit integer

Question **4**

Correct

Mark 1.00 out of 1.00

In verilog h'1234 is a

- 16 bit hexadecimal number
- It is invalid notation ✔
- 32 bit hexadecimal number
- 4 bit hexadecimal number

The correct answer is: It is invalid notation

Question **5**

Correct

Mark 1.00 out of 1.00

Consider 'p = 1011_0100' , what will be the result of p << 3 ?

- 1010_0000 ✔
- 1001_1000
- 1111_0110
- 1010_1000

The correct answer is:
1010_0000

Question **6**

Correct

Mark 1.00 out of 1.00

When does the $monitor statement in a Verilog test bench displays the specified values?

- at the beginning of the simulation
- at the end of the simulation
- when the $monitor statement is first encountered
- whenever the value of any of the specified variables change ✔

The correct answer is:
whenever the value of any of the specified variables change

Question **7**

Incorrect

Mark 0.00 out of 1.00

What does the construct "#12" indicate in simulation?

- Give a delay of 12 before executing the next statement.
- Pause execution of the statements that follow after time 12. ✖
- Unit of delay is 12.
- Execute the next statement at time 12.

The correct answer is:
Give a delay of 12 before executing the next statement.

Question **8**

Correct

Mark 1.00 out of 1.00

```
For the following code, what value is assigned to variable 'r'?
  wire[2:0] p = 3b'01;
  wire[2:0] q = 3b'101;
  wire[4:0] r ;
  assign r = { 1'b1,2{p} };
```

- 11110
- 01010
- 00001
- 10101 ✔

The correct answer is:
10101

Question **9**

Correct

Mark 1.00 out of 1.00

```
Assume that signal s0 changes value from 0 to 1 after 10 time units. Find the value of
variable 'count' at 15 time units after the execution of code below.
 reg [7:0] count = 8'b11010110;
 always @(s0 or s1)
 begin
 count = count << 1;
 count[0] = count[7];
 end
```

- 8'b10101101 ✔
- 8'b01001100
- 8'b11001101
- 8'b01010010

The correct answer is:
8'b10101101

Question **10**

Correct

Mark 1.00 out of 1.00

```
The value of o1 after simulation of following lines
    wire [7:0]o1;
    assign o1=a+b+c;
    assume initial values of a=4'b1110;b=4'b1z00;c=4'b0001
```

- 8'bxxxxxxxx ✔
- 8'b00010z11
- 8'b00000000
- none of the given choices

The correct answer is:
8'bxxxxxxxx

Question **11**

Correct

Mark 1.00 out of 1.00

```
Consider the following Verilog code fragment:
 wire [7:0] P;
 wire Q;
 assign Q = ^P;

if the value of P is 8'b10000011, what will be the value of {P[4:3], 3{Q}}
```

- 5'b00000
- 5'b00111 ✔
- Syntax error
- 5'b10111

The correct answer is:
5'b00111

Question **12**

Correct

Mark 1.00 out of 1.00

```
Find the values of a and b
    wire [3:0] u = 4'bz001;
    wire [3:0] v = 4'b1x1z;
    wire [3:0] a = u & v;
    wire [3:0] b = u | v;
```

- 1x11, x000
- 1x00, x111
- x00x, 1x11 ✔
- z00z, 1x11

The correct answer is: x00x, 1x11

Question **13**

Not answered

Marked out of 1.00

If A = 3'b11x and B = 3'b11x, What are the results of A==B and A===B?

- 1,0
- 0,0
- 1,X
- X,1

The correct answer is:
X,1

Question **14**

Correct

Mark 1.00 out of 1.00

```
The value of o1 and o2 after simulation of following lines
    integer i=-76;
    wire [7:0]o1,o2;
    assign o1=i>>3;
    assign o2=i>>>3;
```

- 8'h16,8'hF6
- 8'hF6,8'hF6 ✔
- 8'h16,8'hf16
- none of the given choices

The correct answer is:
8'hF6,8'hF6

Question **15**

Correct

Mark 1.00 out of 1.00

```
What function do the following Verilog module implement?
    module guess (f, a, b, c);
    input a,b,c; output f,
    wire t1, t2;
    and #1 G1 (t1,a,b);
    and #1 G2 (t2,b,c);
    or #1 G3 (f,t1,t2);
    endmodule
```

- f = a'.b + b'.c + c'.a
- f = a.b'.c' + a'.b.c
- f = a.b + b.c ✔
- None of the given choices

The correct answer is: f = a.b + b.c

Question **16**

Correct

Mark 1.00 out of 1.00

What does the declaration 'reg [13:0] mem[15:0]" indicate?

- an array of 14 words each containing 16 bits.
- an array of 16 elements each containing 14 bits. ✔
- none of the given choices
- 2 dimensional array with 14 rows and 16 columns, where every element is 1 bit.

The correct answer is:
an array of 16 elements each containing 14 bits.

Question **17**

Correct

Mark 1.00 out of 1.00

Consider p = 4'b1011. What is the result of ^p ?

- 1'b1 ✔
- 1'b0
- 1'bx
- 4'b1

The correct answer is:
1'b1

Question **18**

Correct

Mark 1.00 out of 1.00

If time scale is defined as `timescale 10ns/1ns and #15.55 a = b; then 'a' gets 'b' after

- 15.5ns
- 155.5ns
- 150ns
- 156ns ✔
- None of the given choices

The correct answer is:
156ns

Question **19**

Correct

Mark 1.00 out of 1.00

An AND gate with two inputs a and b has a delay of 3 units. Which among the following verilog statements describe its behaviour?

- AND #3 a1(out,a,b); ✔
- #3 AND a1(out,a,b)
- #3 assign out = a&b;
- AND a1 #3(out,a,b);

The correct answer is:
AND #3 a1(out,a,b);

Question **20**

Correct

Mark 1.00 out of 1.00

From the following code snippet, what values of A are displayed after $display and $strobe respectively?

```
initial begin
A = 1;
$display(A);
$strobe(A);
A = 0;
end
```

- 1,0 ✔
- 0,0
- 0,1
- 1,1

The correct answer is:
1,0

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Jump to...