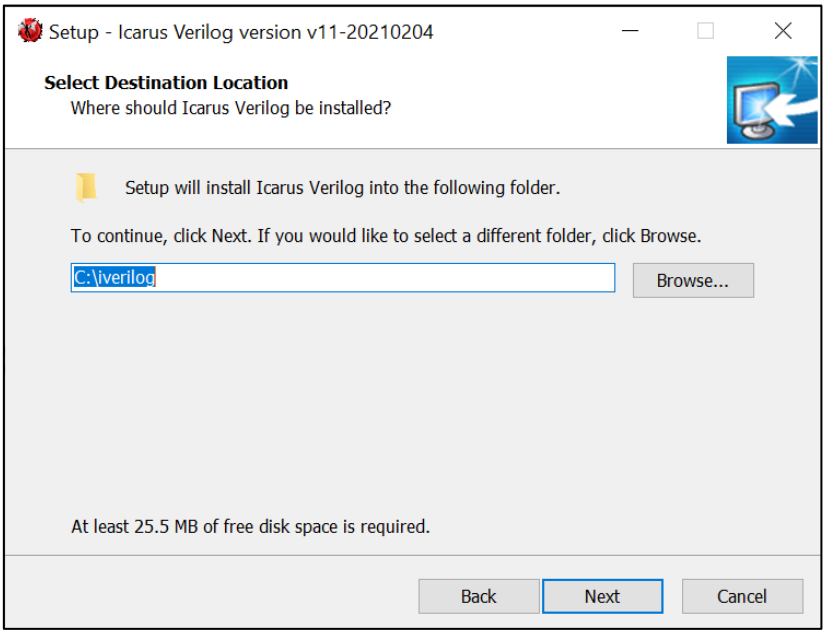
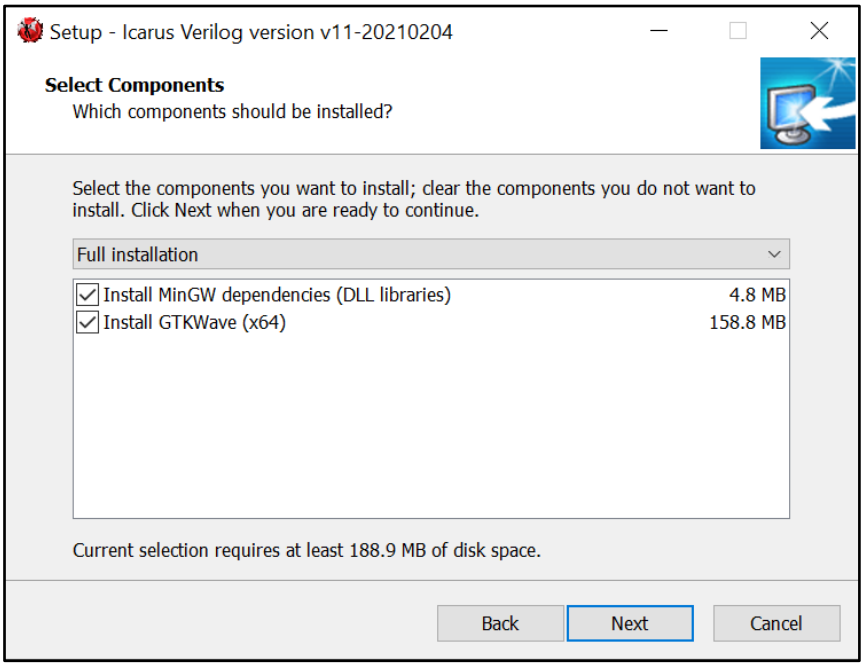
Installation of Icarus Verilog and gtkwave

Windows

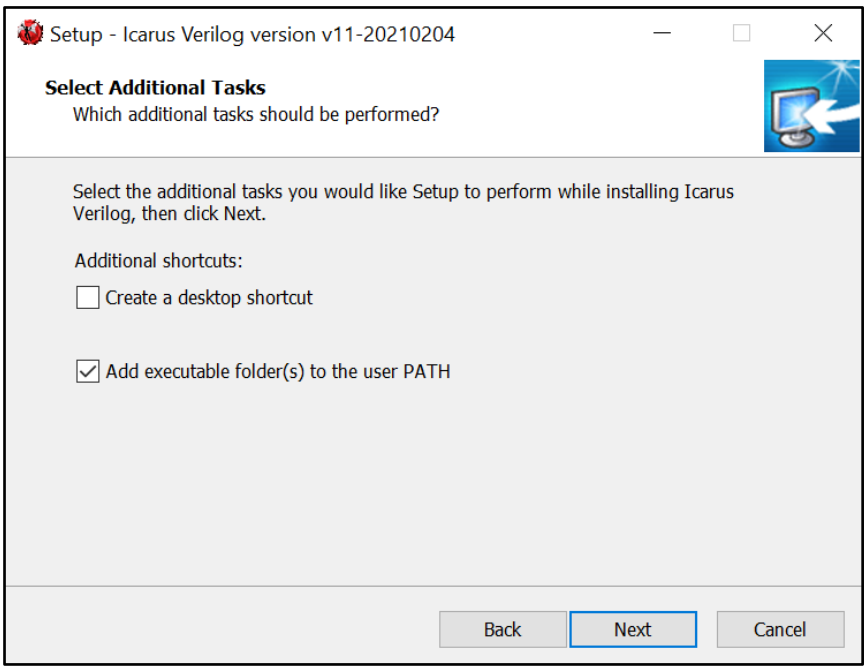
- The latest version of Icarcus Verilog for Windows can be downloaded from http://bleyer.org/icarus/
- When installing, use the same installation locaion - C:\iverilog or if you want to install in a different location, use a location path with “no blank spaces”.



- Make sure Full Installation, MinGW & GTKWave are selected.



- Check the “Add executable folder(s) to the user PATH” checkbox to add the required paths to environmental path.



- Keep the defaults for the remaining options and press NEXT till you reach the Finish step.

- The tool will be installed in **c:\ iverilog folder**.

Compilation Procedure:

- Create the Verilog source files and save it. (Example: HalfAdder.v and HalfAdder_tb.v)
- Open the command prompt and navigate to the location where the source files are available.
- To compile enter the following command

  c:\iverilog\code\iverilog -o mydesign HalfAdder_tb.v HalfAdder.v
- To simulate

  c:\iverilog\code\vvp mydesign
- To view the waverform using gtkwave

  c:\iverilog\code\gtkwave HalfAdder.vcd
- It will open a Gtkwave window: Now select the Top module name "Top",
- It will show Signals in the browser window.
- Now Select All the signals and Press "INSERT button" or add the signals into the waveform viewer by double clicking the signals.
- It will show the signals in the wave form window.

NOTE:
To get Waveform in the GTKwave, you have to add the following two lines in the Testbench code ("HalfAdder_tb.v")

$dumpfile("HalfAdder.vcd"); //Specify the file where all the variables will be dumped.
$dumpvars; // Dump all the varilables' value changes in to file.

EDITOR:
You can use

- Wordpad
- Notepad
- Notepad++ (preferred since it highlights the keywords in Verilog)
- Gvim, etc.,

Incase notepad is used then Save the file as "HalfAdder.v"
Double quotes will accepts as fileName.v rather taking as a fileName.v.txt.

Design: HalfAdder.v

```
module HalfAdder (a,b,sum, ca);
input a, b;
output sum, ca;
    assign sum = a ^ b;
    assign ca  = a & b;
endmodule
```

Testbench: HalfAdder_tb.v

```
module top;

reg ta, tb;
wire tsum, tca;

HalfAdder HA_0(ta,tb,tsum,tca);

initial
begin
        ta=0; tb=0;
    #10 ta=0; tb=1;
    #10 ta=1; tb=0;
    #10 ta=1; tb=1;
end

initial
begin
    $monitor($time, "a = %b, b = %b, Sum = %b, ca = %b",ta,tb,tsum,tca);
    $dumpfile("HalfAdder.vcd");
    $dumpvars;
    #40 $finish;
end

endmodule
```