Adwait Jog

Dept. of Computer Science, William & Mary

Biography

Adwait Jog is an Assistant Professor of Computer Science (CS) at William & Mary (W&M). He earned his Ph.D. from the Pennsylvania State University, University Park in 2015 and B.Tech from the National Institute of Technology (NIT) Rourkela, India in 2009. His research interests lie in the broad area of computer architecture with a high-level goal of architecting next-generation computers. Specifically, his research is focused on designing capable, energy-efficient, reliable, and secure general-purpose Graphics Processing Units (GPUs) and other accelerators, which have become an integral part of almost every computing system. Results of his research regularly appear in the top IEEE/ACM computer architecture conferences such as International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), International Symposium on Micro-Architecture (MICRO), International Symposium on Computer Architecture (ISCA), International Symposium on High-Performance Computer Architecture (HPCA), and other premier inter-disciplinary conferences. He is the recipient of the NSF CAREER Award (2018), NSF CRII award (2017), and Penn State Outstanding Graduate Research Assistant Award (2014).

Academic Positions

Fall 2015– **Assistant Professor**, *William & Mary (W&M)*, Williamsburg, VA.
Leading Insight Computer Architecture Group: `https://insight-cal.github.io`

Education

2009–2015 **Ph.D.**, *Pennsylvania State University (Penn State)*, University Park, PA, USA.
Computer Science and Engineering, Advisor: Chita R. Das

2005–2009 **B.Tech**, *National Institute of Technology (NIT)*, Rourkela, Orissa, India.
Electronics and Instrumentation Engineering

Professional Experience

2009–2015 **Research Assistant**, *Dept. of Computer Science and Engineering*, Penn State, PA.

Summer 2013 **Graduate Research Intern**, *NVIDIA Research*, Santa Clara, CA.

Summer 2012 **Graduate Research Intern**, *Intel Labs*, Hillsboro, OR.

Summer 2011 **Graduate Technical Intern**, *Intel*, Hillsboro, OR.

Research Funding

I am the principal investigator (PI) for the following grants totaling over 1 million USD.

NSF **Faculty Early Career Development Program (CAREER)**, *CCF/SHF: Addressing Scalability Challenges in Designing Next-generation GPU-based Heterogeneous Architectures*, Award Amount: $450,000, PI, Duration: 2018-2023.

NSF **Computing Research Initiation Initiative (CRII)**, *CCF/SHF: Design and Analysis of Processing-Near-Memory Enabled GPU Architecture*, Award Amount: $175,000, PI, Duration: 2017-2020.

NSF **CORE Program**, *CCF/SHF: Small: Enabling and Analyzing Accuracy-aware Reliable GPU Computing*, Award Amount: $449,999, PI: Jog with co-PI: Smirni, Duration: 2017-2021.

NVIDIA **Equipment Donation**, *NVIDIA K20, Jetson TX1, and NVIDIA P6000 Equipment.*

W&M **Summer Research Award**, *Award amount: $4,300 each year (2019,2018).*

W&M **Reves Faculty International Conference Travel Grant**, *Award amount each year: $400 each year (2018,2017,2015).*

Publications

Note In my research area of computer architecture, conference publication is preferred to journal publication, and the premier conferences are generally more selective than the premier journals.[1]The premier conferences in the field of computer architecture are: ASPLOS, MICRO, ISCA, HPCA. Other highly-selective inter-disciplinary conferences are: SIGMETRICS, DSN, ICS, PACT. The acceptance rate of all these conferences is ~20%. In addition, some of my works have appeared in conferences such as IISWC, ISVLSI, VLSID, which have relatively higher acceptance rates (~30%) but consistently attract established researchers.

All publications and related material (e.g., presentation slides, artifacts, videos) are available on my publication web page: `http://adwaitjog.github.io/pubs.html`. **As per Google Scholar, total citations: 1800+, h-index: 17**

Underlined Students are from W&M. My advisees are marked with *.

Peer-Reviewed Publications

[1] Mohamed Assem Ibrahim*, Onur Kayiran, Yasuko Eckert, Gabriel H. Loh, and Adwait Jog. Analyzing and Leveraging Decoupled L1 Caches in GPUs. In *the Proceedings of 27th International Symposium on High Performance Computer Architecture **(HPCA)**, Seoul, South Korea*, pages TBD–TBD, *Acceptance rate: 63/258 ~24%*, Feb 2021.

[2] Mohamed Assem Ibrahim*, Onur Kayiran, Yasuko Eckert, Gabriel H. Loh, and Adwait Jog. Analyzing and Leveraging Shared L1 Caches in GPUs. In *the Proceedings of 29th International Conference on Parallel Architectures and Compilation Techniques **(PACT)**, Atlanta, GA*, pages 161–173, *Acceptance rate: 35/135 ~25%*, Oct 2020.

[3] Bin Nie, Adwait Jog, and Evgenia Smirni. Characterizing Accuracy-Aware Resilience of GPGPU Applications. In *the Proceedings of 20th International Symposium on Cluster, Cloud and Internet Computing **(CCGgrid)**, Melbourne, Victoria, Australia*, pages 111–120, *Acceptance rate: 66/234 ~28%*, May 2020.

[1]Computing Research Association (CRA) Memo Available Here: `https://cra.org/resources/best-practice-memos/evaluating-computer-scientists-and-engineers-for-promotion-and-tenure/`

[4] Hongyuan Liu*, Sreepathi Pai, and Adwait Jog. Why GPUs are Slow at Executing NFAs and How to Make them Faster. In *the Proceedings of 23rd International Conference on Architectural Support for Programming Languages and Operating Systems **(ASPLOS)**, Lausanne, Switzerland*, pages 251–265, *Acceptance rate: 86/479 ~18%*, March 2020.

[5] Gurunath Kadam*, Danfeng Zhang, and Adwait Jog. BCoal: Bucketing-based Memory Coalescing in GPUs. In *the Proceedings of 26th International Symposium on High Performance Computer Architecture **(HPCA)**, San Diego, CA*, pages 570–581, *Acceptance rate: 48/248 ~19%*, Feb 2020.

[6] Lishan Yang, Bin Nie, Adwait Jog, and Evgenia Smirni. Practical resilience analysis of gpgpu applications in the presence of single- and multi-bit faults. *IEEE Transactions on Computers, **(TC)***, pages 1–14, 2020.

[7] Mohamed Assem Ibrahim*, Hongyuan Liu*, Onur Kayiran, and Adwait Jog. Enhancing Bandwidth Utilization via Efficient Inter-core Communication in GPUs. In *the Proceedings of 28th International Conference on Parallel Architectures and Compilation Techniques **(PACT)**, Seattle, WA*, pages 258–271, *Acceptance rate: 26/126 ~21%*, Sept 2019.

[8] Haonan Wang* and Adwait Jog. Exploiting Latency and Error Tolerance of GPGPU Applications for an Energy-efficient DRAM. In *the Proceedings of 49th International Conference on Dependable Systems and Networks **(DSN)**, Portland, OR*, pages 362–374, *Acceptance rate: 54/252 ~21%*, June 2019.

[9] Haonan Wang*, Mohamed Assem Ibrahim*, Sparsh Mittal, and Adwait Jog. Address-Stride Assisted Approximate Value Prediction in GPUs. In *the Proceedings of 33rd International Conference on Super Computing **(ICS)**, Phoenix, Arizona*, pages 184–194, *Acceptance rate: 45/193 ~23%*, June 2019.

[10] Ashutosh Pattnaik, Xulong Tang, Onur Kayiran, Adwait Jog, Asit Mishra, Mahmut T. Kandemir, Anand Sivasubramaniam, and Chita R. Das. Opportunistic Computing in GPU Architectures. In *the Proceedings of 46th International Symposium on Computer Architecture **(ISCA)**, Phoenix, Arizona*, pages 210–223, *Acceptance rate: 62/365 ~17%*, June 2019.

[11] Xulong Tang, Ashutosh Pattnaik, Onur Kayiran, Adwait Jog, Mahmut Taylan Kandemir, and Chita R. Das. Quantifying Data Locality in Dynamic Parallelism in GPUs. In *POMACS Journal of the ACM on Measurement and Analysis of Computing Systems **(SIGMETRICS)**, Phoenix, Arizona*, pages 39:1–39:24, *Acceptance rate: 50/317 ~15%*, June 2019.

[12] Hongyuan Liu*, Mohamed Assem Ibrahim*, Onur Kayiran, Sreepathi Pai, and Adwait Jog. Architectural Support for Efficient Large-Scale Automata Processing. In *the Proceedings of 51st International Conference on Micro-Architecture **(MICRO)**, Fukuoka, Japan*, pages 908–920, *Acceptance rate: 74/351 ~21%*, Oct 2018.

[13] Bin Nie, Lishan Yang, Evgenia Smirni, and Adwait Jog. Fault Site Pruning for Practical Reliability Analysis of GPGPU Applications. In *the Proceedings of 51st*

International Conference on Micro-Architecture ***(MICRO)****, Fukuoka, Japan*, pages 749–761, *Acceptance rate: 74/351 ~21%*, Oct 2018.

[14] Rachata Ausavarungnirun, Vance Miller, Joshua Landgraf, Saugata Ghose, Jayneel Gandhi, Adwait Jog, Christopher J. Rossbach, and Onur Mutlu. MASK: Redesigning the GPU Memory Hierarchy to Support Multi-application Concurrency. In *the Proceedings of 23rd International Conference on Architectural Support for Programming Languages and Operating Systems* ***(ASPLOS)****, Williamsburg, VA*, pages 503–518, *Acceptance rate: 56/319 ~17%*, March 2018.

[15] Haonan Wang*, Fan Luo*, Mohamed Assem Ibrahim*, Onur Kayiran, and Adwait Jog. Efficient and Fair Multi-programming in GPUs via Effective Bandwidth Management. In *the Proceedings of 24th International Symposium on High Performance Computer Architecture* ***(HPCA)****, Vienna, Austria*, pages 247–258, *Acceptance rate: 54/260 ~20%*, Feb 2018.

[16] Gurunath Kadam*, Danfeng Zhang, and Adwait Jog. RCoal: Mitigating GPU Timing Attack via Subwarp-based Randomized Coalescing Techniques. In *the Proceedings of 24th International Symposium on High Performance Computer Architecture* ***(HPCA)****, Vienna, Austria*, pages 156–167, *Acceptance rate: 54/260 ~20%*, Feb 2018.

[17] Hengyu Zhao, Colin Weinshenker*, Mohamed Assem Ibrahim*, Adwait Jog, and Jishen Zhao. Layer-wise performance bottleneck analysis of deep neural networks. *Architectures for Intelligent Machines* ***(AIM)*** *Workshop in conjunction with International Conference on Parallel Architectures and Compilation Techniques (PACT), Hillsboro, OR*, Sep 2017.

[18] Nandita Vijaykumar, Gennady Pekhimenko, Adwait Jog, Saugata Ghose, Abhishek Bhowmick, Rachata Ausavarangnirun, Chita Das, Mahmut T Kandemir, Todd C Mowry, and Onur Mutlu. A Framework for Accelerating Bottlenecks in GPU Execution with Assist Warps. *Advances in GPU Research and Practice*, pages 373–415, Sept 2017.

[19] Sparsh Mittal, Rajendra Bishnoi, Fabian Oboril, Haonan Wang*, Mehdi Tahoori, Adwait Jog, and Jeffrey Vetter. Architecting SOT-RAM Based GPU Register File. In *the Proceedings of IEEE Computer Society Annual Symposium on VLSI* ***(ISVLSI)****, Bochum, Germany*, pages 38–44, *Acceptance rate: 67/212 ~32%*, July 2017.

[20] Xulong Tang, Ashutosh Pattnaik, Huaipan Jiang, Onur Kayiran, Adwait Jog, Sreepathi Pai, Mohamed Assem Ibrahim*, Mahmut Kandemir, and Chita Das. Controlled Kernel Launch for dynamic parallelism in GPUs. In *the Proceedings of 23rd International Symposium on High Performance Computer Architecture* ***(HPCA)****, Austin, TX*, pages 649–660, *Acceptance rate: 50/224 ~22%*, Feb 2017.

[21] Sparsh Mittal, Haonan Wang*, Adwait Jog, and Jeffrey Vetter. Design and Analysis of Soft-Error Resilience Mechanisms for GPU Register File. In *the Proceedings of 30th International Conference on VLSI design and 16th International Conference on Embedded Systems* ***(VLSID)****, Hyderabad, India*, pages 409–414, *Acceptance rate: 71/292 ~24%*, Jan 2017.

[22] Nandita Vijaykumar, Kevin Hsieh, Gennady Pekhimenko, Samira Khan, Ashish Shrestha, Saugata Ghose, Adwait Jog, Phillip B Gibbons, and Onur Mutlu. Zorua: A Holistic Approach to Resource Virtualization in GPUs. In *the Proceedings of 49th International Symposium on Micro Architecture **(MICRO)**, Taipei, Taiwan*, pages 1–14, *Acceptance rate: 61/288 ~21%*, Oct 2016.

[23] Robert Risque* and Adwait Jog. Characterization of Quantum Workloads on SIMD Architectures. In *the Proceedings of International Symposium on Workload Characterization **(IISWC)**, Providence, RI*, pages 1–9, *Acceptance rate: 21/71 ~29%*, Oct 2016.

[24] Ashutosh Pattnaik, Xulong Tang, Adwait Jog, Onur Kayiran, Asit K Mishra, Mahmut T Kandemir, Onur Mutlu, and Chita R Das. Scheduling Techniques for GPU Architectures with Processing-in-Memory Capabilities. In *the Proceedings of 25th International Conference on Parallel Architectures and Compilation Techniques **(PACT)**, Haifa, Israel*, pages 31–44, *Acceptance rate: 31/139 ~22%*, Sept 2016.

[25] Onur Kayiran, Adwait Jog, Ashutosh Pattnaik, Rachata Ausavarungnirun, Xulong Tang, Mahmut T Kandemir, Gabriel H Loh, Onur Mutlu, and Chita R Das. μC-States: Fine-grained GPU Datapath Power Management. In *the Proceedings of 25th International Conference on Parallel Architectures and Compilation Techniques **(PACT)**, Haifa, Israel*, pages 17–30, *Acceptance rate: 31/139 ~22%*, Sept 2016.

[26] Adwait Jog, Onur Kayiran, Ashutosh Pattnaik, Mahmut T Kandemir, Onur Mutlu, Ravishankar Iyer, and Chita R Das. Exploiting Core Criticality for Enhanced GPU Performance. In *the Proceedings of 42nd International International Conference on Measurement and Modeling of Computer Systems **(SIGMETRICS)**, Antibes Juan-Les-Pins, France*, pages 351–363, *Acceptance rate: 28/208 ~13%*, June 2016.

[27] Adwait Jog, Onur Kayiran, Tuba Kesten, Ashutosh Pattnaik, Evgeny Bolotin, Niladrish Chatterjee, Stephen W Keckler, Mahmut T Kandemir, and Chita R Das. Anatomy of GPU Memory System for Multi-application Execution. In *the Proceedings of 1st International Symposium on Memory Systems **(MEMSYS)**, Washington, DC*, pages 223–234, Oct 2015.

[28] Nandita Vijaykumar, Gennady Pekhimenko, Adwait Jog, Abhishek Bhowmick, Rachata Ausavarungnirun, Chita Das, Mahmut T Kandemir, Todd C Mowry, and Onur Mutlu. A Case for Core-assisted Bottleneck Acceleration in GPUs: Enabling Flexible Data Compression with Assist Warps. In *the Proceedings of 42nd International Symposium on Computer Architecture **(ISCA)**, Portland, OR*, pages 41–53, *Acceptance rate: 58/305 ~19%*, June 2015.

[29] Evgeny Bolotin, Zvi Guz, Adwait Jog, Steve Keckler, and Michael Parker. Approach to Adaptive Allocation of Shared Resources in Computer Systems, June 2015. US Patent 2015/0163324 A1.

[30] Onur Kayiran, Nachiappan Chidambaram Nachiappan, Adwait Jog, Rachata Ausavarungnirun, Mahmut T Kandemir, Gabriel H Loh, Onur Mutlu, and Chita R Das.

Managing GPU Concurrency in Heterogeneous Architectures. In *the Proceedings of 47th International Symposium on Micro Architecture* ***(MICRO)***, *Cambridge, UK*, pages 114–126, *Acceptance rate: 53/273 ~19%*, Dec 2014.

[31] Wei Ding, Mahmut Kandemir, Diana Guttman, Adwait Jog, Chita R Das, and Praveen Yedlapalli. Trading Cache Hit Rate for Memory Performance. In *the Proceedings of 23rd International Conference on Parallel Architectures and Compilation Techniques* ***(PACT)***, *Edmonton, Alberta, Canada*, pages 357–368, *Acceptance rate: 37/144 ~25%*, August 2014.

[32] Adwait Jog, Evgeny Bolotin, Zvika Guz, Mike Parker, Stephen W Keckler, Mahmut T Kandemir, and Chita R Das. Application-aware Memory System for Fair and Efficient Execution of Concurrent GPGPU Applications. In *the Proceedings of 7th Workshop on General Purpose Computing using GPUs* ***(GPGPU)***, *co-located with 19th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Salt Lake City, UT*, pages 1–10, *Acceptance rate: 12/27 ~44%*, March 2014.

[33] Onur Kayıran, Adwait Jog, Mahmut T Kandemir, and Chita Ranjan Das. Neither More Nor Less: Optimizing Thread-level Parallelism for GPGPUs. In *the Proceedings of 22nd International Conference on Parallel Architectures and Compilation* ***(PACT)***, *Edinburgh, Scotland*, pages 157–166, *Acceptance rate: 36/208 ~19%*, Sept 2013.

[34] Adwait Jog, Onur Kayiran, Asit K Mishra, Mahmut T Kandemir, Onur Mutlu, Ravishankar Iyer, and Chita R Das. Orchestrated Scheduling and Prefetching for GPGPUs. In *the Proceedings of 40th International Symposium on Computer Architecture* ***(ISCA)***, *Tel Aviv, Israel*, pages 332–343, *Acceptance rate: 56/288 ~19%*, June 2013.

[35] Adwait Jog, Onur Kayiran, Nachiappan Chidambaram Nachiappan, Asit K Mishra, Mahmut T Kandemir, Onur Mutlu, Ravishankar Iyer, and Chita R Das. OWL: Cooperative Thread Array Aware Scheduling Techniques for Improving GPGPU Performance. In *the Proceedings of 18th International Conference on Architectural Support for Programming Languages and Operating Systems* ***(ASPLOS)***, *Houston, TX*, pages 395–406, *Acceptance rate: 44/191 ~23%*, March 2013.

[36] Adwait Jog, Asit K Mishra, Cong Xu, Yuan Xie, Vijaykrishnan Narayanan, Ravishankar Iyer, and Chita R Das. Cache Revive: Architecting Volatile STT-RAM Caches for Enhanced Performance in CMPs. In *the Proceedings of 49th Design Automation Conference* ***(DAC)***, *San Francisco, CA*, pages 243–252, *Acceptance rate: 168/741 ~22%*, June 2012.

Invited Scholarly Talks

Breaking the Memory Wall in Current and Emerging Accelerators.

- IBM T.J. Watson Research Center, NY, USA, March 2019
- Microsoft Research, India, Dec 2018
- Intel Labs, India, Dec 2018
- Indian Institute of Science, Bangalore, India Dec 2018
- University of Pittsburgh, PA, Oct 2018

Understanding and Addressing Throughput and Security Trade-offs in GPU-based Systems.

- HPCA SechArch workshop 2019, Washington DC, Feb 2019
- Intel, Hillsboro, May 2018
- Cisco (via WebEx), April 2018

Memory Bandwidth Management for Enhanced Throughput and Security in GPUs.

- North Carolina State University, April 2018
- George Washington University, April 2018

Breaking the Memory Bandwidth Wall in GPUs.

- Virginia Commonwealth University (VCU), Feb 2016
- Indian Institute of Science, Bangalore, India, Dec 2015

The Future of Parallel Computing with GPUs.

- William & Mary, Feb 2015
- University of Utah, Mar 2015
- Temple University, Mar 2015
- AMD Research, Mar 2015
- UC Riverside, Apr 2015
- Intel Labs, Apr 2015

W&M News Articles

Computer science: As Moore's Law slows down, the Insight Architecture Lab accelerates: `https://www.wm.edu/news/stories/2020/computer-science-as-moores-law-slows-down,-the-insight-architecture-lab-accelerates.php`

Using a CAREER award to advance the Insight Computer Architecture Lab: `https://www.wm.edu/news/stories/2018/using-a-career-award-to-advance-the-insight-computer-architecture-lab.php`

Software Distribution

– Artifact for ASPLOS 2020 paper: Why GPUs are Slow at Executing NFAs and How to Make them Faster. It is a fast NFA Engine for GPUs. This framework can be found here: `https://github.com/insight-cal/gpunfa-artifact`. This artifact is evaluated by the ASPLOS 2020 evaluation committee and received all possible validation badges.

– Multiple Application Framework for GPU Architectures (MAFIA) is developed for supporting multiple application execution on GPUs. Currently, it supports 25 benchmarks from various benchmark suites (e.g., CUDA, Parboil, SHOC and Rodinia). From these benchmarks, one can construct 300 2-application workloads and 2300 3-application workloads. This framework can be found here: `https://github.com/adwaitjog/mafia`

Courses Taught

Course syllabi and class-by-class schedule information is available here: `http://adwaitjog.github.io/teaching.html`

Spring 2020	CSCI 674 – GPU Architectures (upper-level graduate course)
Fall 2019	CSCI 424/524 – Computer Architecture (upper-level undergraduate course)
Spring 2019	CSCI 674 – GPU Architectures (upper-level graduate course)
Fall 2018	CSCI 424/524 – Computer Architecture (upper-level undergraduate course)
Spring 2018	CSCI 680 – GPU Architectures (upper-level graduate course)
Fall 2017	CSCI 424/524 – Computer Architecture (upper-level undergraduate course)
Spring 2017	CSCI 680 – Parallel Computer Architecture (upper-level graduate course)
Fall 2016	CSCI 424/524 – Computer Architecture (upper-level undergraduate course)
Spring 2016	CSCI 780 – GPU Architectures (seminar graduate course)
Fall 2015	CSCI 780 – Topics in Computer Architecture (seminar graduate course)

The following two courses are scheduled for the academic year 2020-21:

Spring 2021	CSCI 424/524 – Computer Architecture (upper-level undergraduate course)
Fall 2020	CSCI 780 – Topics in Computer Architecture (seminar graduate course)

Student Advising

Ph.D. Students

2016–2020 **Haonan Wang (graduated in Aug 2020; now tenure-track Assistant Professor at San Jose State University)**, *Topic: Design and Analysis of Memory Management Techniques for Next-generation GPUs*, Internship at PNNL.
Defended (July 2020), Passed Oral Exam (Aug 2019)

Spring 2016– **Mohamed Assem Ibrahim**, *Topic: Rethinking Cache Hierarchy and Interconnect Design for Next-generation GPUs*, Internship at AMD Research (twice).
Passed Oral Exam (Dec 2019), Expected Graduation: Spring 2021

Fall 2016– **Gurunath Kadam**, *Topic: Low-overhead Techniques for Improving GPU Security and Reliability*, Internship at Intel Labs.
Passed Oral Exam (Oct 2020), Expected Graduation: Spring 2021

Spring 2017– **Hongyuan Liu**, *Topic: Techniques for Accelerating Large-scale Automata Processing*, Internship at Intel Labs.
Passed Oral Exam (Sep 2020), Expected Graduation: Spring 2022

Fall 2020– **Ying Li**, *Topic: Machine Learning for GPU Architecture Design*.
Expected Graduation: Spring 2025

M.S. Students

Summer 2016 **Fan Luo**, *Topic: Parallelism Management in GPUs*, MS Project, graduated.

Spring 2017 **Corey Ames**, *Topic: DRAM Row-hammer Analysis*, MS Project, graduated.

Spring 2017 **Rongdong Chai**, *Topic: DRAM Locality Analysis*, MS Project, graduated.

Spring 2017 **Haonan Wang**, *Topic: Value Approximation*, MS Project, graduated.

Fall 2019 **Robert Xing**, *Topic: GPU Cache Management with Machine Learning*, MS Project, graduated.

Undergraduate Students

Summer 2020 **Alex Chung**, *Topic: RISC-V Simulation with Python*, Monroe Scholar.

Summer 2018 **Sungbum Hong**, *Topic: GPU Security*, Charles Center Summer Research Scholar, graduated.

2016–17 **Colin Weinshenker**, *Topic: Chiplet-based Systems*, Honors thesis, graduated.

2015–16 **Robert Risque**, *Topic: Quantum Architectures*, Senior's thesis, graduated.

Professional Service

Funding Panel Reviewing

NSF Panelist: 2020 (once), 2019 (once), 2018 (two times), 2017 (four times), 2016 (once)

Organizing Committees

2020 ACM Student Research Competition (SRC) Chair, PACT 2020

2020 Workshop co-chair, 13th Workshop on General Purpose Processing Using GPU (GPGPU 2020) @ PPoPP 2020

2020 Publicity co-chair, International Conference on Networking, Architecture and Storage (NAS)

2019 Workshop co-chair, 12th Workshop on General Purpose Processing Using GPU (GPGPU 2019) @ ASPLOS 2019

2019 Publicity co-chair, International Symposium on Micro-architecture (MICRO)

2019 Publicity chair, International Symposium on Code Generation and Optimization (CGO)

2018 Local arrangements co-chair, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)

2018 Workshop co-chair, 2nd Workshop on Minimizing Data Movement (Min-Move) @ASPLOS 2018

2017 Workshop co-chair, 1st Workshop on Minimizing Data Movement (Min-Move) @PACT 2017

2015 Proceedings Chair, International Symposium on Architectures for Networking and Communications Systems (ANCS)

Program Committees

2021 Program Committee Member, International Symposium on Computer Architecture (ISCA)

2021 Program Committee Member, International Conference on Dependable Systems and Networks (DSN)

2021 Program Committee Member, International Symposium on High Performance Computer Architecture (HPCA)

2020 Program Committee Member, International Symposium on High Performance Computer Architecture (HPCA)

2020 External Program Committee Member, International Symposium on Micro-Architecture (MICRO)

2020 External Program Committee Member, International Symposium on Computer Architecture (ISCA)

2020 External Program Committee Member, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)

2019 Program Committee Member, International Symposium on Micro-Architecture (MICRO)

2019 Program Committee Member, International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS)

2019, 2017 Program Committee Member, International Symposium on High-Performance Parallel and Distributed Computing (HPDC)

2019, 2018 Program Committee Member, International Conference on Computer Design (ICCD)

2018 Program Committee Member, International Symposium on Performance Analysis of Systems and Software (ISPASS)

2018 Program Committee Member, International Symposium on High-Performance Computer Architecture (HPCA)

2017 External Program Committee Member, International Symposium on Micro-Architecture (MICRO)

2017 Program Committee Member, International Conference on Dependable Systems and Networks (DSN)

2016-2018 Program Committee Member, Workshop on General Purpose Processing Using GPU (GPGPU)

2016 Program Committee Member, International Conference on Parallel and Distributed Systems (ICPADS)

2016 Program Committee Member, International Conference on Supercomputing (ICS)

2016 Program Committee Member, International Conference on Parallel Processing (ICPP)

2016–2020 Program Committee Member, International Conference on Networking, Architecture and Storage (NAS)

Journal Reviewing

I have reviewed 50+ journal papers across the following journals:

IEEE Transactions on Computers (TC)

IEEE Computer Architecture Letters (CAL)

ACM Architecture and Code Optimization (TACO)

IEEE Transactions on Parallel and Distributed Systems (TPDS)

IEEE Transactions on Dependable and Secure Computing (TDSC)

ACM Transactions on Embedded Computing (TECS)

ACM Transactions on Design Automation of Electronic Systems (TODAES)

Departmental and College Service

Service to the Department

2020–now Faculty Hiring Committee Member

2020–now Graduate Admissions Committee Member

Jan 2020 Outreach Talk at University of Mary Washington

2019–now Graduate Curriculum Committee Member

2016–now Colloquium Committee Member

2018–2019 Colloquium Committee Chair

2018–2019 Awards and Prizes Committee Member

2017-18 Graduate Curriculum Committee Member

2015–now Ph.D. Thesis Committee Member: Nancy Carter, Lele Ma, Bin Nie, Zheng Peng, Probir Roy, Tao Zhang

2017 Awards and Prizes Committee Chair

2015-16 Graduate Admissions, Retention, and Financial Aid Committee

Service to the College

2020–now Parking Appeals Committee Member

Fall 2019 T. Jefferson Prize in Natural Philosophy, Committee Member

Spring 2019 Graduate Research Symposium, Judge

Spring 2018 Graduate Research Symposium, Session Chair

2016–now Pre-major Undergraduate Advising

2016–2017 Sanderson Award Committee Member for Undergraduate Mentoring

Other Activities

Spring 2019 Hybrid Instructional Training (HIT), W&M, Spring 2019; URL: `https://sites.google.com/email.wm.edu/elearningsamples/adwait-jog`

Summer 2018 Taught in a very popular summer school (held annually at Fiuggi, Italy) for Computer Architects (ACACES 2018). Around 100 students took my GPU class (over 5 days); URL: `http://acaces.hipeac.net/2018/index.php?page=courseinfo&lecturer=jog`

2017–18 Represented W&M at Center for Automata Processing, University of Virginia. W&M Membership was sponsored by VMEC.

2017–18 University Teaching Project, Participant

2018,2017 Keynote Speaker, Focus on Future (FOF) Conference, Camp Launch, School of Education, W&M