Adwait Jog

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RESEARCH INTERESTS

My research interests lie in all aspects of computer architecture and systems, especially in memory systems and scheduling techniques for new computing systems.

PROFESSIONAL EXPERIENCE

- **The College of William and Mary** **Fall 2015 – Present**
  Assistant Professor **Williamsburg, VA**
  Leading a new computer architecture research group.

- **The Pennsylvania State University, Ph.D. Candidate** **Fall 2009 – Summer 2015**
  Advisor: Prof. Chita Das, High Performance Computing Lab (HPCL) **University Park, PA**
  - Proposed techniques for efficient execution of multiple applications on next generation GPUs.
  - Proposed criticality-aware memory system for GPUs.
  - Proposed a coordinated scheduling and prefetching mechanism to improve GPU performance.
  - Proposed warp scheduling policies to mitigate contention in GPU memory system.
  - Traded-off non-volatility of STT-RAM for lower write latency and energy.

- **NVIDIA Research, Graduate Research Intern** **Summer 2013**
  Manager: Steve Keckler **Santa Clara, CA**
  Mentors: Evgeny Bolotin, Zvika Guz, Mike Parker
  Researched on efficient execution of multiple contexts/applications on next generation GPUs. The results of this work are published in GPGPU 2014 (co-located with ASPLOS 2014).

- **Intel Labs, Graduate Research Intern** **Summer 2012**
  Managers: Srihari Makineni, Ravi Iyer **Hillsboro, OR**
  Mentors: Xiaowei Jiang, Li Zhao
  Implemented and evaluated micro-architecture techniques for Intel's ultra-low power core (*Siskiyou*). This infrastructure is released to universities to perform research on energy-efficient architectures.

- **Intel Corp., Graduate Technical Intern** **Summer 2011**
  Manager: Sridhar Lakshmanmoorthy **Hillsboro, OR**
  Mentor: Ramadass Nagarajan
  Performed detailed studies and proposed techniques for designing a QoS aware interconnect fabric for the Intel's next generation heterogeneous SoCs.

EDUCATION

The Pennsylvania State University, University Park *Fall 2009 - Summer 2015*
Ph.D. Candidate in Computer Science and Engineering
Advisors: Chita Das and Mahmut Kandemir

National Institute of Technology, Rourkela, India *Fall 2005 - Spring 2009*
Bachelor of Technology *(Hons.)* in Electronics and Instrumentation Engineering

AWARDS and HONORS

- Outstanding Graduate Research Assistant Award, CSE, Penn State, 2014
- NVIDIA Graduate Fellowship 2013, Finalist
- Best Paper Nomination, PACT 2013
- Student Travel Grants for attending ASPLOS (2014, 2013), ISCA (2015, 2013), MICRO 2014
- College of Engineering Fellowship, Penn State University, 2009
- Summer Research Fellowship, School of Computing, National University of Singapore, 2008
- Summer Research Fellowship, Indian Academy of Sciences, 2007
- Undergraduate Scholarship for being in Top 1% in All India Engineering Entrance Exam, 2005

PUBLICATIONS

[**MEMSYS 2015**] **Adwait Jog**, Onur Kayiran, Tuba Kesten, Ashutosh Pattnaik, Evgeny Bolotin, Niladrish Chatterjee, Stephen W. Keckler, Mahmut T. Kandemir, Chita R. Das, *Anatomy of GPU Memory System for Multi-Application Execution*, In the Proceedings of 1st International Symposium on Memory Systems (MEMSYS), Washington, DC, Oct 2015

[**ISCA 2015**] Nandita Vijaykumar, Gennady Pekhimenko, **Adwait Jog**, Abhishek Bhowmick, Rachata Ausavarungnirun, Onur Mutlu, Chita Das, Mahmut Kandemir, Todd Mowry, *A Case for Core-Assisted Bottleneck Acceleration in GPUs: Enabling Efficient Data Compression*, In the Proceedings of 42^{nd} International Symposium on Computer Architecture (ISCA), Portland, OR, June, 2015

[**MICRO 2014**] Onur Kayiran, Nachiappan CN, **Adwait Jog**, Rachata Ausavarungnirun, Mahmut Kandemir, Gabriel Loh, Onur Mutlu, Chita Das, *Managing GPU Concurrency in Heterogeneous CPU-GPU Architectures*, In the Proceedings of 47^{th} International Symposium on Micro Architecture (MICRO), Cambridge, UK, Dec 2014

[**GPGPU 2014**] **Adwait Jog**, Evgeny Bolotin, Zvika Guz, Mike Parker, Steve Keckler, Mahmut Kandemir, Chita Das, *Application-aware Memory System for Fair and Efficient Execution of Concurrent GPGPU Applications*, In the Proceedings of General-Purpose Computation on Graphics Processing Unit (GPGPU-7), co-located with ASPLOS, Salt Lake City, UT, USA, March, 2014

[**PACT 2014**] Wei Ding, Mahmut Kandemir, Diana Guttman, **Adwait Jog**, Chita Das, Praveen Yedlapalli, *Trading Cache Hit Rate for Memory Performance*, In the Proceedings of 23^{rd} International Conference on Parallel Architectures and Compilation Techniques (PACT), Edmonton, Canada, August, 2014

[**ASPLOS 2013**] **Adwait Jog**, Onur Kayiran, Nachiappan CN, Asit Mishra, Mahmut Kandemir, Onur Mutlu, Ravi Iyer, Chita Das, *OWL: Cooperative Thread Array Aware Scheduling Techniques for Improving GPGPU performance*, In the Proceedings of 18^{th} International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Houston, TX, USA, March, 2013

[**ISCA 2013**] **Adwait Jog**, Onur Kayiran, Asit Mishra, Mahmut Kandemir, Onur Mutlu, Ravi Iyer, Chita Das, *Orchestrated Scheduling and Prefetching for GPGPUs*, In the Proceedings of 40^{th} International Symposium on Computer Architecture (ISCA), Tel Aviv, Israel, June, 2013

[**PACT 2013, Best Paper Nominee**] Onur Kayiran, **Adwait Jog**, Mahmut Kandemir, Chita Das, *Neither More Nor Less: Optimizing Thread-Level Parallelism for GPGPUs*, In the Proceedings of 22^{nd} International Conference on Parallel Architectures and Compilation Techniques (PACT), Edinburgh, Scotland, September, 2013

[**DAC 2012**] **Adwait Jog**, Asit Mishra, Cong Xu, Yuan Xie, Vijaykrishnan Narayanan, Ravi Iyer, Chita Das, *Cache Revive: Architecting Volatile STT-RAM Caches for Enhanced Performance in CMPs*, In the Proceedings of 49^{th} Design Automation Conference (DAC), San Francisco, USA, June 2012

PATENTS

[**US Patent**] Evgeny Bolotin, Zvika Guz, **Adwait Jog**, Stephen W. Keckler, Mike Parker, Approach to Adpative Allocation of Shared Resources in Computer Systems, United States Patent Application US20150163324 A1

TEACHING EXPERIENCE

- **Instructor**, CS780, Topics in Computer Architecture **Fall 2015**
- **Co-Instructor**, CMPEN 331, Computer Organization and Design **Fall 2014**
- **Co-Instructor**, CMPEN 331, Computer Organization and Design **Spring 2014**
- **Teaching Assistant**, CMPEN 431, Introduction to Computer Architecture **Spring 2010**
- **Teaching Assistant**, CMPEN 471, Logic Design of Digital Systems **Fall 2009**

TALKS AND POSTER SESSIONS

- The Future of Parallel Computing with GPUs
  – The College of William and Mary, Feb 2015
  – University of Utah, Mar 2015
  – Temple University, Mar 2015
  – AMD Research, Mar 2015
  – UC Riverside, Apr 2015
  – Intel Labs, Apr 2015
- Application-aware Memory System for Fair and Efficient Execution of Concurrent GPU Applications,
  – GPGPU-7 Workshop (co-located with ASPLOS 2014), Salt Lake City, UT, March 2014
  – Intern Talk, NVIDIA Research, Santa Clara, CA, Sept 2013
- Mitigating and Masking the Limitations of GPU Memory Systems,
  – Intern Talk, NVIDIA Research, Santa Clara, CA, June 2013
- Orchestrated Scheduling and Prefetching for GPGPUs,
  – ISCA 2013, Tel Aviv, Israel, June 2013
- OWL: Cooperative Thread Array Aware Scheduling Techniques for Improving GPGPU performance,
  – ASPLOS 2013, Houston, TX, March 2013
- Cache Revive: Architecting Volatile STT-RAM Caches for Enhanced Performance in CMPs,
  – DAC 2012, San Francisco, CA, June 2012
  – Poster presentation at IUCRC NEXYS Workshop, Pittsburgh, PA

PROFESSIONAL SERVICE AND MEMBERSHIPS

- Proceedings and Submission Chair, ANCS 2015
- Reviewer (Conferences): I was on External Review Committee for DAC 2013, HPCA 2013, MICRO 2012, and ICCD (2014, 2013)
- On-Behalf Reviewer (Conferences): ASPLOS, ISCA, HPCA, MICRO, DATE, DAC, PACT, IPDPS

- Reviewer (Journals): IEEE Transactions on Computers (TC), ACM Transactions on Embedded Computing (TECS), ACM Transactions on Design Automation of Electronic Systems (TODAES), IEEE Journal on Computer Architecture Letters (CAL)
- Student Member of ACM, IEEE, ACM SIGARCH