Adwait Jog

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RESEARCH INTERESTS

My research interests lie in all aspects of computer hardware architecture, including memory system architecture, data-parallel architectures (e.g., GPUs), and hardware scheduling.

EDUCATION

Pennsylvania State University, University Park, PA — *Fall 2009 - Summer 2015*
Ph.D. in Computer Science and Engineering

National Institute of Technology (NIT), Rourkela, India — *Fall 2005 - Spring 2009*
Bachelor of Technology *(Hons.)* in Electronics and Instrumentation Engineering

PROFESSIONAL EXPERIENCE

- **College of William and Mary (W&M)** — **Aug 2015 – Present**
  Assistant Professor — **Williamsburg, VA**
  • Leading a new computer hardware architecture research group.

- **Pennsylvania State University, Research Assistant** — **Fall 2009 – Summer 2015**
  Advisor: Prof. Chita Das, High Performance Computing Lab (HPCL) — **University Park, PA**
  • Proposed various techniques to improve the performance and energy efficiency of GPU hardware.

- **NVIDIA Research, Graduate Research Intern** — **Summer 2013**
  Manager: Steve Keckler — **Santa Clara, CA**
  Mentors: Evgeny Bolotin, Zvika Guz, Mike Parker
  Researched on efficient execution of multiple contexts/applications on next generation GPUs. The results of this work are published in GPGPU 2014 (co-located with ASPLOS 2014).

- **Intel Labs, Graduate Research Intern** — **Summer 2012**
  Managers: Srihari Makineni, Ravi Iyer — **Hillsboro, OR**
  Mentors: Xiaowei Jiang, Li Zhao
  Implemented and evaluated micro-architecture techniques for Intel's ultra-low power core (*Siskiyou*). This infrastructure is released to universities to perform research on energy-efficient architectures.

- **Intel Corp., Graduate Technical Intern** — **Summer 2011**
  Manager: Sridhar Lakshmanmoorthy — **Hillsboro, OR**
  Mentor: Ramadass Nagarajan
  Performed detailed studies and proposed techniques for designing a QoS aware interconnect fabric for the Intel's next generation heterogeneous SoCs.

AWARDS, GRANTS, and HONORS

- NSF SHF Award 2017 (PI, Award Amount: $449,999)
- NSF CRII Award 2017 (sole PI, Award Amount: $175,000)
- NVIDIA Hardware Grant (Jetson TX1), 2017

- NVIDIA Hardware Grant (Tesla K40), 2016
- Reves Faculty International Conference Travel Grant, 2015
- Outstanding Graduate Research Assistant Award, CSE, Penn State, 2014
- NVIDIA Graduate Fellowship 2013, Finalist
- Best Paper Nomination, PACT 2013 (One of the four papers nominated for the Best Paper Award)
- Student Travel Grants for attending: ASPLOS (2014, 2013), ISCA (2015, 2013), MICRO 2014
- College of Engineering Fellowship, Penn State University, 2009

PUBLICATIONS

Note: In my sub-discipline (computer hardware architecture) of computer science, conference publication is preferred to journal publication, and the premier conferences are generally more selective than the premier journals. The premier conferences in computer hardware architecture and related areas (not in any particular order) are: MICRO, ISCA, HPCA, ASPLOS, PACT, SIGMETRICS, DAC. The acceptance rate of all these premier conferences is around 20%.

Underlined students are advised by me.

[**HPCA 2017**] Xulong Tang, Ashutosh Pattnaik, Huaipan Jiang, Onur Kayiran, `Adwait Jog`, Sreepathi Pai, Mohamed Ibrahim, Mahmut Kandemir, Chita Das, *Controlled Kernel Launch for Dynamic Parallelism in GPUs*, In the Proceedings of 23^{rd} International Symposium on High-Performance Computer Architecture (HPCA), Austin, USA, Feb, 2017 ***Acceptance rate: 50/224 ≈ 22%***

[**VLSID 2017**] Sparsh Mittal, Haonan Wang, `Adwait Jog`, Jeffrey Vetter *Design and Analysis of Soft-Error Resilience Mechanisms for GPU Register File* In the Proceedings of 30^{th} International Conference on VLSI design and 16^{th} International Conference on Embedded Systems, Hyderabad, India, Jan 2017 ***Acceptance rate: 71/292 ≈ 24%***

[**MICRO 2016**] Nandita Vijaykumar, Kevin Hsieh, Gennady Pekhimenko, Samira Khan, Ashish Shrestha, Saugata Ghose, `Adwait Jog`, Phillip B. Gibbons, Onur Mutlu, *Zorua: A Holistic Approach to Resource Virtualization in GPUs*, In the Proceedings of 49th International Symposium on Micro Architecture (MICRO), Taipei, Taiwan, October 2016 ***Acceptance rate: 61/288 ≈ 21.5%***

[**IISWC 2016**] Robert Risque, `Adwait Jog`, *Characterization of Quantum Workloads on SIMD Architectures*, In the Proceedings of International Symposium on Workload Characterization (IISWC), Providence, RI, September 2016 ***Acceptance rate: 21/71 ≈ 29%***

[**PACT 2016**] Ashutosh Pattnaik, Xulong Tang, `Adwait Jog`, Onur Kayiran, Asit K. Mishra, Mahmut T. Kandemir, Onur Mutlu, Chita R. Das, *Scheduling Techniques for GPU Architectures with Processing-In-Memory Capabilities*, In the Proceedings of 25^{th} International Conference on Parallel Architectures and Compilation Techniques (PACT), Haifa, Israel, September 2016 ***Acceptance rate: 31/139 ≈ 22.3%***

[**PACT 2016**] Onur Kayiran, `Adwait Jog`, Ashutosh Pattnaik, Rachata Ausavarungnirun, Xulong Tang, Mahmut T. Kandemir, Gabriel H. Loh, Onur Mutlu, Chita R. Das, *μC-States: Fine-grained GPU Datapath Power Management*, In the Proceedings of 25^{th} International Conference on Parallel Architectures and Compilation Techniques (PACT), Haifa, Israel, September 2016 ***Acceptance rate: 31/139 ≈ 22.3%***

[**SIGMETRICS 2016**] `Adwait Jog`, Onur Kayiran, Ashutosh Pattnaik, Mahmut T. Kandemir, Onur Mutlu, Ravi Iyer, Chita R. Das, *Exploiting Core-Criticality for Enhanced Performance in GPUs*, In the Proceedings of 42nd ACM International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), Antibes Juan-Les-Pins, France, June 2016 ***Acceptance rate: 28/208 ≈ 13.4%***

[**MEMSYS 2015**] `Adwait Jog`, Onur Kayiran, Tuba Kesten, Ashutosh Pattnaik, Evgeny Bolotin, Niladrish Chatterjee, Stephen W. Keckler, Mahmut T. Kandemir, Chita R. Das, *Anatomy of GPU Memory System for Multi-Application Execution*, In the Proceedings of 1st International Symposium on Memory Systems (MEMSYS), Washington, DC, Oct 2015
The associated code is open-source: https://github.com/adwaitjog/mafia

[**Ph.D. Thesis 2015**] `Adwait Jog`, *Design and Analysis of Scheduling Techniques for Throughput Processors*, Ph.D. Thesis, The Pennsylvania State University, University Park, PA, 2015

[**ISCA 2015**] Nandita Vijaykumar, Gennady Pekhimenko, `Adwait Jog`, Abhishek Bhowmick, Rachata Ausavarungnirun, Onur Mutlu, Chita Das, Mahmut Kandemir, Todd Mowry, *A Case for Core-Assisted Bottleneck Acceleration in GPUs: Enabling Efficient Data Compression*, In the Proceedings of 42^{nd} International Symposium on Computer Architecture (ISCA), Portland, OR, June, 2015 ***Acceptance rate: 58/305 ≈ 19.1%***

[**MICRO 2014**] Onur Kayiran, Nachiappan CN, `Adwait Jog`, Rachata Ausavarungnirun, Mahmut Kandemir, Gabriel Loh, Onur Mutlu, Chita Das, *Managing GPU Concurrency in Heterogeneous CPU-GPU Architectures*, In the Proceedings of 47^{th} International Symposium on Micro Architecture (MICRO), Cambridge, UK, Dec 2014 ***Acceptance rate: 53/273 ≈ 19.4%***

[**PACT 2014**] Wei Ding, Mahmut Kandemir, Diana Guttman, `Adwait Jog`, Chita Das, Praveen Yedlapalli, *Trading Cache Hit Rate for Memory Performance*, In the Proceedings of 23^{rd} International Conference on Parallel Architectures and Compilation Techniques (PACT), Edmonton, Canada, August, 2014 ***Acceptance rate: 37/144 ≈ 25.7%***

[**GPGPU 2014**] `Adwait Jog`, Evgeny Bolotin, Zvika Guz, Mike Parker, Steve Keckler, Mahmut Kandemir, Chita Das, *Application-aware Memory System for Fair and Efficient Execution of Concurrent GPGPU Applications*, In the Proceedings of General-Purpose Computation on Graphics Processing Unit (GPGPU-7), co-located with ASPLOS, Salt Lake City, UT, USA, March, 2014 ***Acceptance rate: 12/27 ≈ 44.4%***

[**PACT 2013**] Onur Kayiran, `Adwait Jog`, Mahmut Kandemir, Chita Das, *Neither More Nor Less: Optimizing Thread-Level Parallelism for GPGPUs*, In the Proceedings of 22^{nd} International Conference on Parallel Architectures and Compilation Techniques (PACT), Edinburgh, Scotland, September, 2013 ***Acceptance rate: 36/208 ≈ 17.3%, Best Paper Nomination***

[**ISCA 2013**] `Adwait Jog`, Onur Kayiran, Asit Mishra, Mahmut Kandemir, Onur Mutlu, Ravi Iyer, Chita Das, *Orchestrated Scheduling and Prefetching for GPGPUs*, In the Proceedings of 40^{th} International Symposium on Computer Architecture (ISCA), Tel Aviv, Israel, June, 2013 ***Acceptance rate: 56/288 ≈ 19.4%***

[**ASPLOS 2013**] `Adwait Jog`, Onur Kayiran, Nachiappan CN, Asit Mishra, Mahmut Kandemir, Onur Mutlu, Ravi Iyer, Chita Das, *OWL: Cooperative Thread Array Aware Scheduling Techniques for Improving GPGPU performance*, In the Proceedings of 18^{th} International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Houston, TX, USA, March, 2013 ***Acceptance rate: 44/191 ≈ 23.0%***

[**DAC 2012**] `Adwait Jog`, Asit Mishra, Cong Xu, Yuan Xie, Vijaykrishnan Narayanan, Ravi Iyer, Chita Das, *Cache Revive: Architecting Volatile STT-RAM Caches for Enhanced Performance in CMPs*, In the Proceedings of 49^{th} Design Automation Conference (DAC), San Francisco, USA, June 2012 ***Acceptance rate: 168/741 ≈ 23%***

PATENTS & BOOK CHAPTERS

[**Book Chapter**] Nandita Vijaykumar, Gennady Pekhimenko, `Adwait Jog`, Saugata Ghose, Abhishek Bhowmick, Rachata Ausavarungnirun, Chita Das, Mahmut Kandemir, Todd C. Mowry, and Onur Mutlu, A Framework for Accelerating Bottlenecks in GPU Execution with Assist Warps, Book Chapter in Advances in GPU Research and Practice, Elsevier, to be published in 2016.

[**US Patent**] Evgeny Bolotin, Zvika Guz, `Adwait Jog`, Stephen W. Keckler, Mike Parker, Approach to Adpative Allocation of Shared Resources in Computer Systems, United States Patent Application US20150163324 A1

STUDENTS CURRENTLY ADVISING

- **Ph.D. Students:** Mohamed Ibrahim, Haonan Wang, Gurunath Kadam, Hongyuan Liu
- **Undergraduate Students:** Colin Weinshenker (Honors)

STUDENTS GRADUATED

- **MS Students:** Fan Luo, Haonan Wang
- **Undergraduate Students:** Robert Risque

TEACHING EXPERIENCE

- **Instructor@W&M**, CSCI 680, Parallel Computer Architecture (graduate course) **Spring 2017** (In-progress)
- **Instructor@W&M**, CSCI 424/524, Computer Architecture (undergraduate course) **Fall 2016** (Rating: 4.06/5.0)
- **Instructor@W&M**, CSCI 680/780, GPU Architectures (graduate course) **Spring 2016** (Rating: 4.28/5.0)
- **Instructor@W&M**, CSCI 680/780, Topics in Computer Architecture (graduate course) **Fall 2015** (Rating: 4.43/5.0)
- **Co-Instructor@PSU**, CMPEN 331, Computer Organization and Design (undergraduate course) **Fall 2014**
- **Co-Instructor@PSU**, CMPEN 331, Computer Organization and Design (undergraduate course) **Spring 2014**
- **Teaching Assistant@PSU**, CMPEN 431, Introduction to Computer Architecture (undergraduate course) **Spring 2010**
- **Teaching Assistant@PSU**, CMPEN 471, Logic Design of Digital Systems (undergraduate course) **Fall 2009**

INVITED TALKS

- Breaking the Memory Bandwidth Wall in GPUs
  – Virginia Commonwealth University (VCU), Feb 2016
  – Indian Institute of Science, Bangalore, India, Dec 2015
- Anatomy of GPU Memory System for Multi-Application Execution,
  – MEMSYS 2015, Washington, DC, Oct 2015
- The Future of Parallel Computing with GPUs
  – The College of William and Mary, Feb 2015
  – University of Utah, Mar 2015
  – Temple University, Mar 2015
  – AMD Research, Mar 2015
  – UC Riverside, Apr 2015
  – Intel Labs, Apr 2015

- Application-aware Memory System for Fair and Efficient Execution of Concurrent GPU Applications,
  – GPGPU-7 Workshop (co-located with ASPLOS 2014), Salt Lake City, UT, March 2014
  – Intern Talk, NVIDIA Research, Santa Clara, CA, Sept 2013
- Mitigating and Masking the Limitations of GPU Memory Systems,
  – Intern Talk, NVIDIA Research, Santa Clara, CA, June 2013
- Orchestrated Scheduling and Prefetching for GPGPUs,
  – ISCA 2013, Tel Aviv, Israel, June 2013
- OWL: Cooperative Thread Array Aware Scheduling Techniques for Improving GPGPU performance,
  – ASPLOS 2013, Houston, TX, March 2013
- Cache Revive: Architecting Volatile STT-RAM Caches for Enhanced Performance in CMPs,
  – DAC 2012, San Francisco, CA, June 2012
  – Poster presentation at IUCRC NEXYS Workshop, Pittsburgh, PA

SERVICE AT W&M

- Pre-major advising, Aug 2016 - Present
- Departmental Awards and Prizes Committee, 2017 - Present
- Departmental Colloquium Committee, Aug 2016 - Present
- Departmental Admissions Committee, Aug 2015 - July 2016

EXTERNAL PROFESSIONAL SERVICE AND MEMBERSHIPS

- NSF Panelist: 2017 (thrice), 2016 (once)
- External Program Committee Member, MICRO 2017
- Program Committee Member, NAS 2017
- Program Committee Member, HPDC 2017
- Program Committee Member, DSN 2017
- Program Committee Member, ICPADS 2016
- Program Committee Member, ICS 2016
- Program Committee Member, NAS 2016
- Program Committee Member, ICPP 2016
- Program Committee Member, GPGPU (2017, 2016)
- Proceedings and Submission Chair, ANCS 2015
- Invited Reviewer (Journals):
  – ACM Transactions on Architecture and Code Optimization (TACO)
  – IEEE Transactions on Computers (TC)
  – IEEE Journal on Computer Architecture Letters (CAL)
  – ACM Transactions on Parallel Computing (TOPC)
  – ACM Transactions on Embedded Computing (TECS)
  – IEEE Transactions on Parallel and Distributed Systems (TPDS)
  – ACM Transactions on Design Automation of Electronic Systems (TODAES)

- Invited External Reviewer (Conferences): DAC 2013, HPCA 2013, MICRO 2012, and ICCD (2014, 2013)
- Member of ACM, IEEE, ACM SIGARCH