PROTOTYPE **Display Class C Medium** **Rev B**

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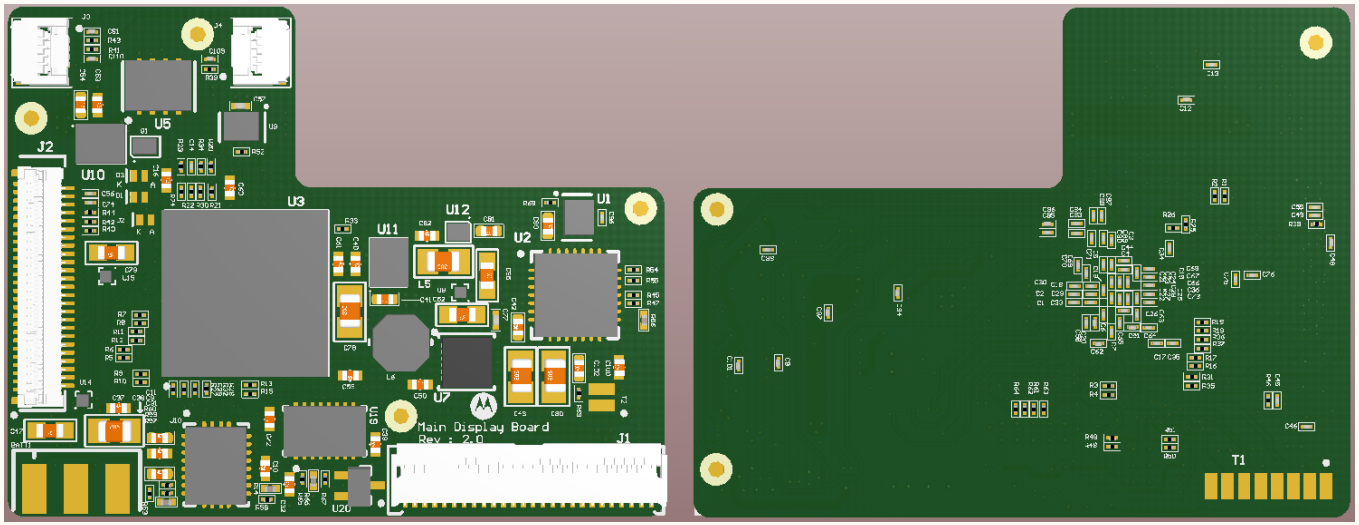
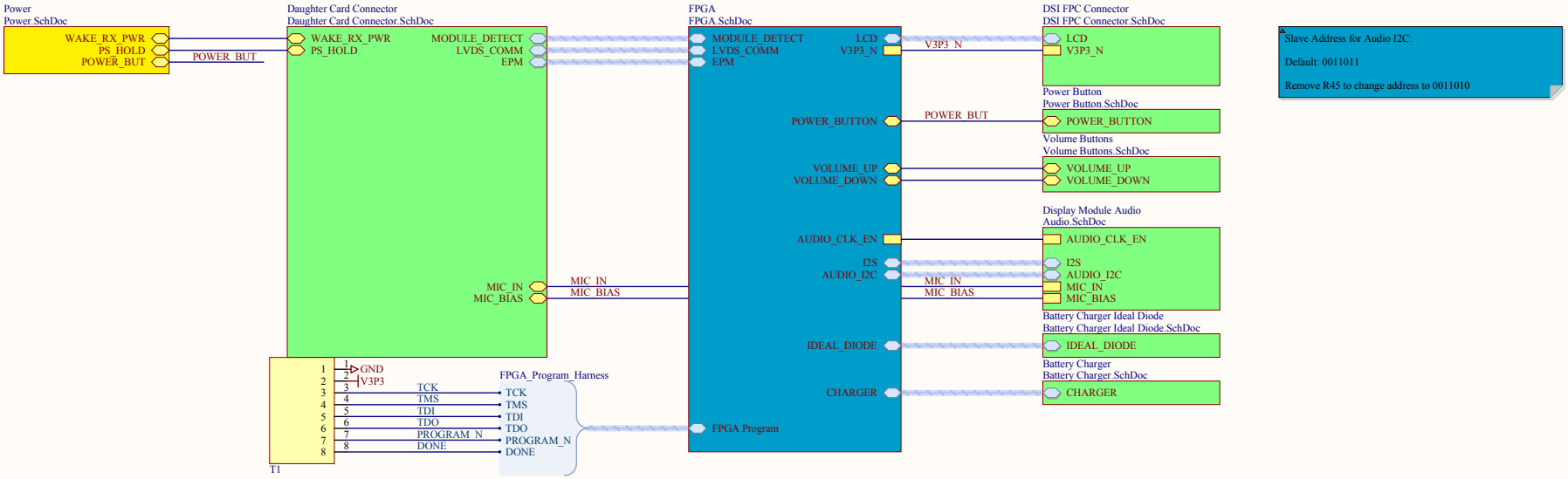


Block Diagram
Block Diagram.SchDoc

Display Module Main Board:
FPGA
DSI Connector
Audio IC
Charge Controller
Flex Cable (to daughter board)

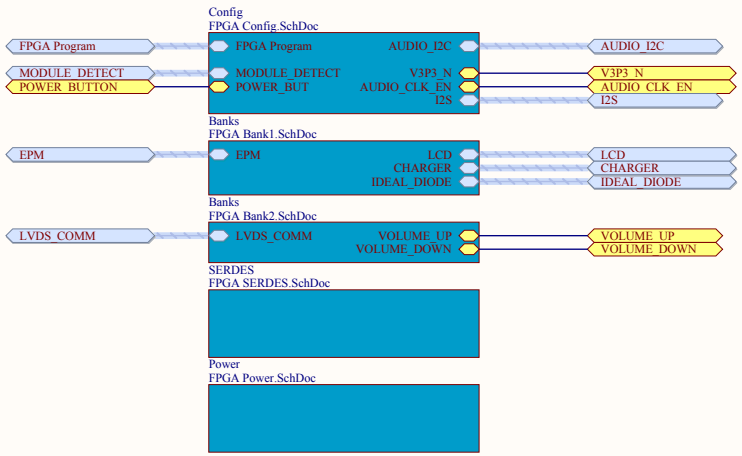


Slave Address for Audio I2C:

Default: 0011011

Remove R45 to change address to 0011010

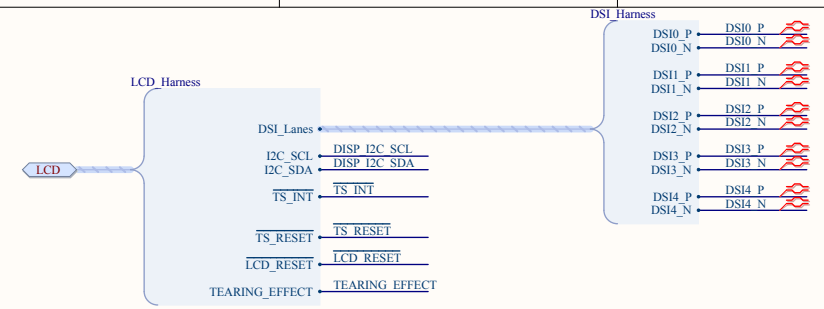
Title:	Block Diagram			
Project:	Prototype Display Main Class I Rev B.PrjPCB			
Document:	Block Diagram.SchDoc			
Engineer:	David McCoy (Cospan Design)			
Drawn By:	David McCoy			
Approved By:	*	Revision:	B	
Date:	12/18/2013	Number:	2 of 16	



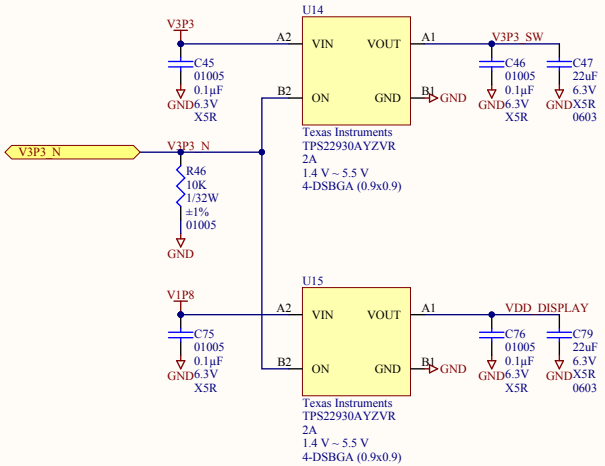
Layout Guidlines:

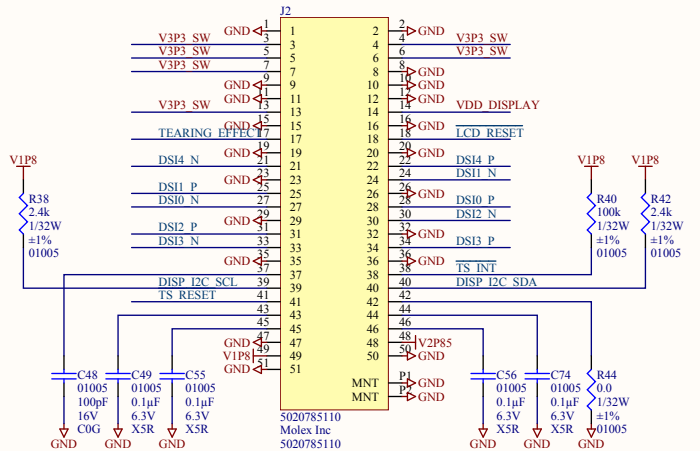
4 Layer Stackup
3-mil trace
5-mil via

Title:	FPGA		
Project:	Prototype Display Main Class I Rev B.PrjPCB		
Document:	FPGA.SchDoc		
Engineer:	David McCoy (Cospan Design)		
Drawn By:	David McCoy		
Approved By:	*	Revision:	B
Date:	12/18/2013	Number:	3 of 16



Switchable Power Supply Controller (Default On)





Pin Number	Signal Name	Function	Notes
G1	GND	Ground	Mechanical connection
1	GND	Ground	
2	GND	Ground	
3	VBAT_DISP	3.0V - 4.35V	Switchable from Common 3.3V rail
4	VBAT_DISP	3.0V - 4.35V	Switchable from Common 3.3V rail
5	VBAT_DISP	3.0V - 4.35V	Switchable from Common 3.3V rail
6	VBAT_DISP	3.0V - 4.35V	Switchable from Common 3.3V rail
7	VBAT_DISP	3.0V - 4.35V	Switchable from Common 3.3V rail
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	GND	Ground	
12	GND	Ground	
13	VCI_DISP	2.85V	Switchable from TOUCH_VCI
14	VDD_DISP	1.8V	Switchable from Common 1.8V rail
15	GND	Ground	
16	GND		
17	DISP_TE	Display Tearing	1.8V Display Tearing (from display)
18	DISP_RST_N	Display Reset	1.8V Display Reset (to display)
19	GND		
20	GND		
21	DSI_DATA3-	MIPI DSI Data 3 Negative	MIPI M-Phy DSI
22	DSI_DATA3+	MIPI DSI Data 3 Positive	MIPI M-Phy DSI
23	GND	Ground	
24	DSI_DATA0-	MIPI DSI Data 0 Negative	MIPI M-Phy DSI
25	DSI_DATA0+	MIPI DSI Data 0 Positive	MIPI M-Phy DSI
26	GND	Ground	
27	DSI_CLK-	MIPI DSI Clock Negative	MIPI M-Phy DSI
28	DSI_CLK+	MIPI DSI Clock Positive	MIPI M-Phy DSI
29	GND	Ground	
30	DSI_DATA1-	MIPI DSI Data 1 Negative	MIPI M-Phy DSI
31	DSI_DATA1+	MIPI DSI Data 1 Positive	MIPI M-Phy DSI
32	GND	Ground	
33	DSI_DATA2-	MIPI DSI Data 2 Negative	MIPI M-Phy DSI
34	DSI_DATA2+	MIPI DSI Data 2 Positive	MIPI M-Phy DSI
35	GND	Ground	
36	GND	Ground	
37	REF	Reference	Tie 100pF to this pin and ground
38	TOUCH_INT_N	Touch Interrupt	1.8V Touch Interrupt Active Low (from touch) (100K Pullup to 1.8V)
39	TOUCH_I2C_SCL	Touch I2C Clock	Open Drain I2C Clock (2.2K Pullup to 1.8V)
40	TOUCH_I2C_SDA	Touch I2C Data	Open Drain I2C Data (2.2K Pullup to 1.8V)
41	TOUCH_RST_N	Touch Reset	1.8V Touch Reset Active Low (to touch)
42	TX14	??	Tie 0 Ohm to this pin and ground
43	RX28_A4	??	Tie 0.1uF to this pin and ground
44	A4_RX28	??	Tie 0.1uF to this pin and ground
45	RX27	??	Tie 0.1uF to this pin and ground
46	RX26	??	Tie 0.1uF to this pin and ground
47	GND	Ground	
48	TOUCH_VCI	2.85V	2.85V dedicated LDO
49	VDD_TOUCH	1.8V	1.8V from Common 1.8V rail
50	GND	Ground	
51	GND	Ground	
G2	GND	Ground	Mechanical connection

V2P85 is NOT CONNECTED ANYTHING

Programmers Note: The signals

VCI_DISP_EN (Inverted)
VDD_DISP_EN

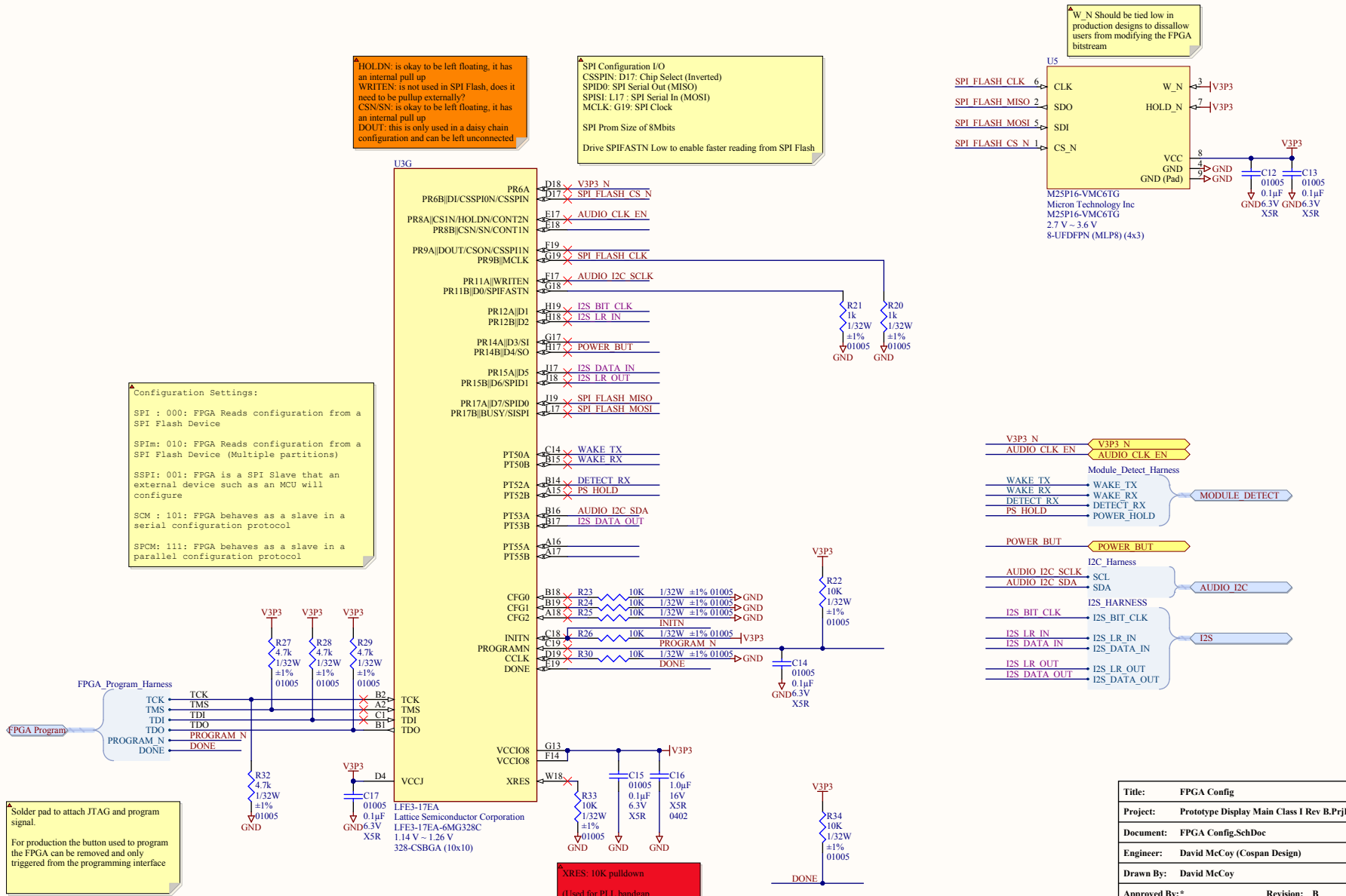
Are used to disable and enable the touch interface (respectively)

It is okay to leave these unconnected. The LCD and the touch interface will be default on.

OMAP4460 VDDIO is at 1.8V. This Power switch will enable the output voltage with a value above 1.6V but just barely. The extra NFET pulldown is in case the 1.8V is not enough and can be removed if 1.8V does enable the power switch with a 2.85V input.

This also inverts the input signal

Title:	FPC Connector
Project:	Prototype Display Main Class I Rev B.PrjPCB
Document:	DSI FPC Connector.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By:	* Revision: B
Date:	10/10/2013 Number: 4 of 16


W_N Should be tied low in production designs to dissallow users from modifying the FPGA bitstream
U5
SPI_FLASH_CLK
SPI_FLASH_MISO
SPI_FLASH_MOSI
SPI_FLASH_CS_N
CLK
SDO
SDI
CS_N
W_N
HOLD_N
VCC
GND
GND (Pad)
V3P3
M25P16-VMC6TG
Micron Technology Inc
M25P16-VMC6TG
2.7 V ~ 3.6 V
8-UFDFPN (MLP8) (4x3)
C12
C13
01005
0.1µF
6.3V
X5R
HOLDN: is okay to be left floating, it has an internal pull up
WRITEN: is not used in SPI Flash, does it need to be pullup externally?
CSN/SN: is okay to be left floating, it has an internal pull up
DOUT: this is only used in a daisy chain configuration and can be left unconnected
SPI Configuration I/O
CSSPIN: D17: Chip Select (Inverted)
SPID0: SPI Serial Out (MISO)
SPISI: L17 : SPI Serial In (MOSI)
MCLK: G19: SPI Clock
SPI Prom Size of 8Mbits
Drive SPIFASTN Low to enable faster reading from SPI Flash
U3G
PR6A
PR6B||DI/CSSPI0N/CSSPIN
PR8A||CS1N/HOLDN/CONT2N
PR8B||CSN/SN/CONT1N
PR9A||DOUT/CSON/CSSPI1N
PR9B||MCLK
PR11A||WRITEN
PR11B||D0/SPIFASTN
PR12A||D1
PR12B||D2
PR14A||D3/SI
PR14B||D4/SO
PR15A||D5
PR15B||D6/SPID1
PR17A||D7/SPID0
PR17B||BUSY/SISPI
PT50A
PT50B
PT52A
PT52B
PT53A
PT53B
PT55A
PT55B
CFG0
CFG1
CFG2
INITN
PROGRAMN
CCLK
DONE
VCCJ
VCCIO8
VCCIO8
XRES
V3P3_N
SPI_FLASH_CS_N
AUDIO_CLK_EN
SPI_FLASH_CLK
AUDIO_I2C_SCLK
I2S_BIT_CLK
I2S_LR_IN
POWER_BUT
I2S_DATA_IN
I2S_LR_OUT
SPI_FLASH_MISO
SPI_FLASH_MOSI
WAKE_TX
WAKE_RX
DETECT_RX
PS_HOLD
AUDIO_I2C_SDA
I2S_DATA_OUT
PROGRAM_N
DONE
R21
R20
1k
1/32W
±1%
01005
GND
Configuration Settings:
SPI : 000: FPGA Reads configuration from a SPI Flash Device
SPIm: 010: FPGA Reads configuration from a SPI Flash Device (Multiple partitions)
SSPI: 001: FPGA is a SPI Slave that an external device such as an MCU will configure
SCM : 101: FPGA behaves as a slave in a serial configuration protocol
SPCM: 111: FPGA behaves as a slave in a parallel configuration protocol
R23
R24
R25
R26
R30
10K
INITN
R22
C14
0.1µF
6.3V
X5R
V3P3_N
AUDIO_CLK_EN
Module_Detect_Harness
MODULE_DETECT
POWER_BUT
I2C_Harness
AUDIO_I2C
I2S_HARNESS
I2S
FPGA_Program_Harness
FPGA Program
TCK
TMS
TDI
TDO
PROGRAM_N
DONE
R27
R28
R29
4.7k
B2
A2
C1
B1
R32
D4
C17
LFE3-17EA
Lattice Semiconductor Corporation
LFE3-17EA-6MG328C
1.14 V ~ 1.26 V
328-CSBGA (10x10)
Solder pad to attach JTAG and program signal.
For production the button used to program the FPGA can be removed and only triggered from the programming interface
R33
C15
C16
1.0µF
16V
X5R
0402
XRES: 10K pulldown
(Used for PLL bandgap configuration)
R34
Your use of this Module Developer's Kit is expressly subject to the terms set out in the MDK License Agre
Title: FPGA Config
Project: Prototype Display Main Class I Rev B.PrjPCB
Document: FPGA Config.SchDoc
Engineer: David McCoy (Cospan Design)
Drawn By: David McCoy
Approved By: * Revision: B
Date: 12/18/2013 Number: 5 of 16

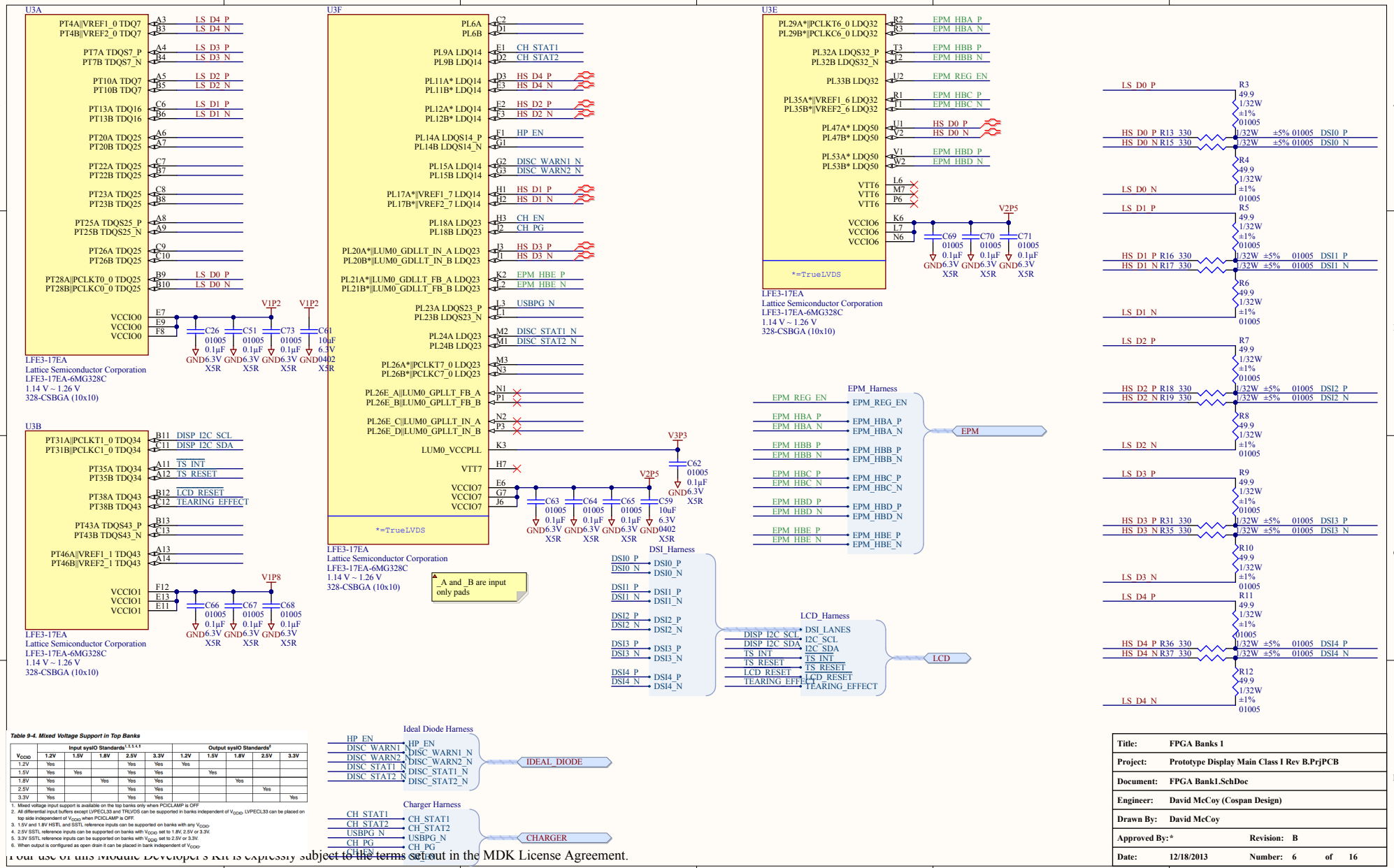
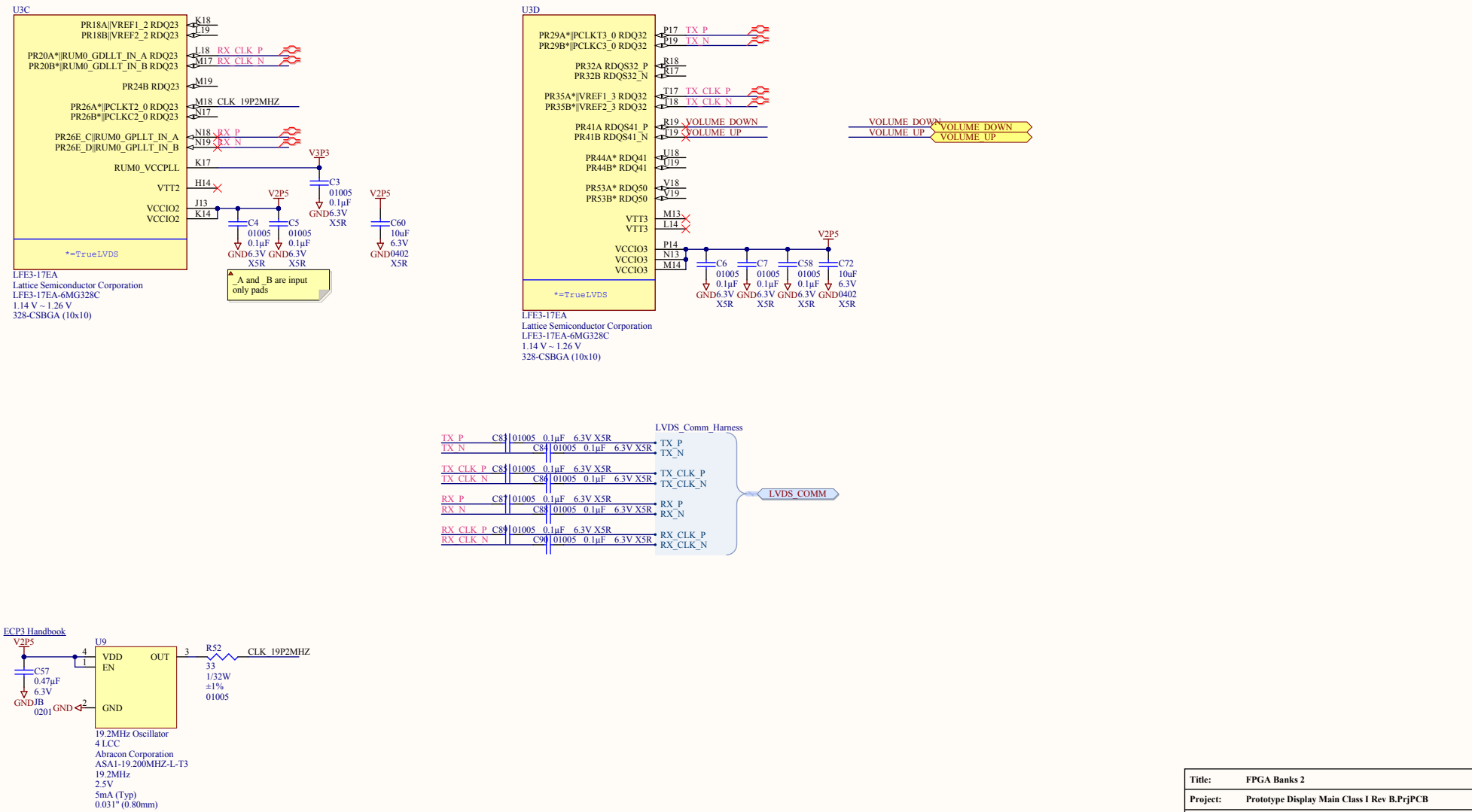


Table 9-4. Mixed Voltage Support in Top Banks

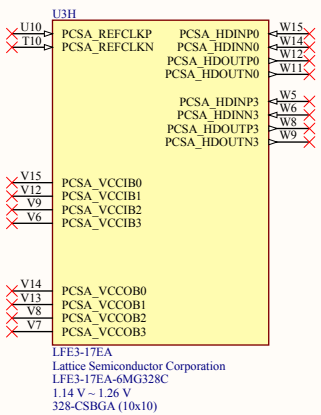
V_{CCIO}	Input sysIO Standards[1,2,3,4,5]					Output sysIO Standards[6]				
	1.2V	1.5V	1.8V	2.5V	3.3V	1.2V	1.5V	1.8V	2.5V	3.3V
1.2V	Yes			Yes	Yes	Yes				
1.5V	Yes	Yes		Yes	Yes		Yes			
1.8V	Yes		Yes	Yes	Yes			Yes		
2.5V	Yes			Yes	Yes				Yes	
3.3V	Yes			Yes	Yes					Yes

1. Mixed voltage input support is available on the top banks only when PCICLAMP is OFF
2. All differential input buffers except LVPECL33 and TRLVDS can be supported in banks independent of V_{CCIO}. LVPECL33 can be placed on top side independent of V_{CCIO} when PCICLAMP is OFF.
3. 1.5V and 1.8V HSTL and SSTL reference inputs can be supported on banks with any V_{CCIO}.
4. 2.5V SSTL reference inputs can be supported on banks with V_{CCIO} set to 1.8V, 2.5V or 3.3V.
5. 3.3V SSTL reference inputs can be supported on banks with V_{CCIO} set to 2.5V or 3.3V.
6. When output is configured as open drain it can be placed in bank independent of V_{CCIO}.

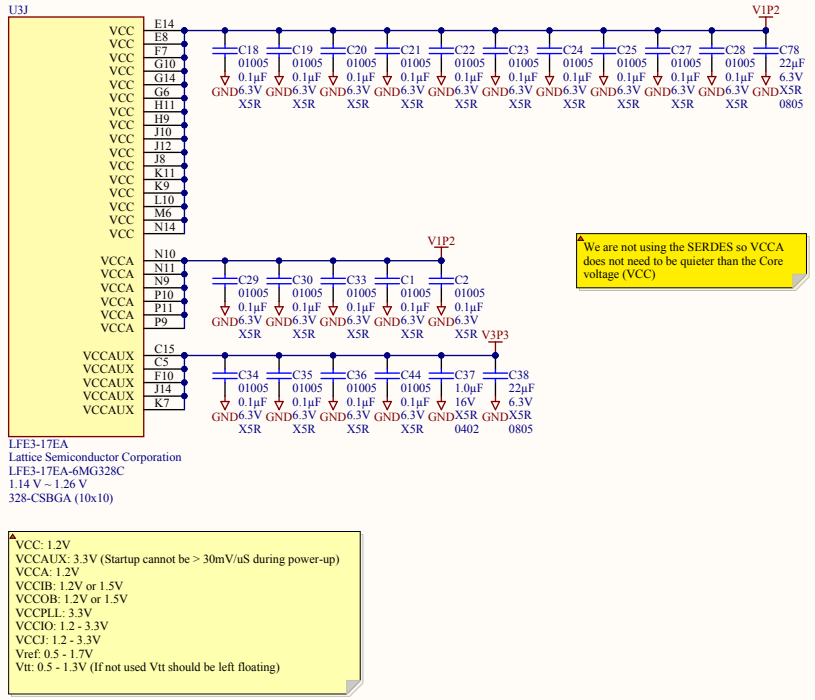
Title:	FPGA Banks 1
Project:	Prototype Display Main Class I Rev B.PrjPCB
Document:	FPGA Bank1.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By:	* Revision: B
Date:	12/18/2013 Number: 6 of 16



Title:	FPGA Banks 2		
Project:	Prototype Display Main Class I Rev B.PrjPCB		
Document:	FPGA Bank2.SchDoc		
Engineer:	David McCoy (Cospan Design)		
Drawn By:	David McCoy		
Approved By:	*	Revision:	B
Date:	2/6/2014	Number:	7 of 16

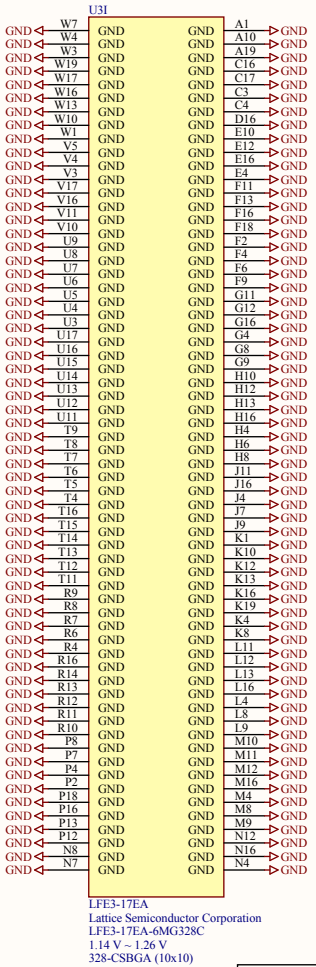


Title:	FPGA SERDES			
Project:	Prototype Display Main Class I Rev B.PrjPCB			
Document:	FPGA SERDES.SchDoc			
Engineer:	David McCoy (Cospan Design)			
Drawn By:	David McCoy			
Approved By:	*	Revision:	B	
Date:	12/18/2013	Number:	8 of 16	

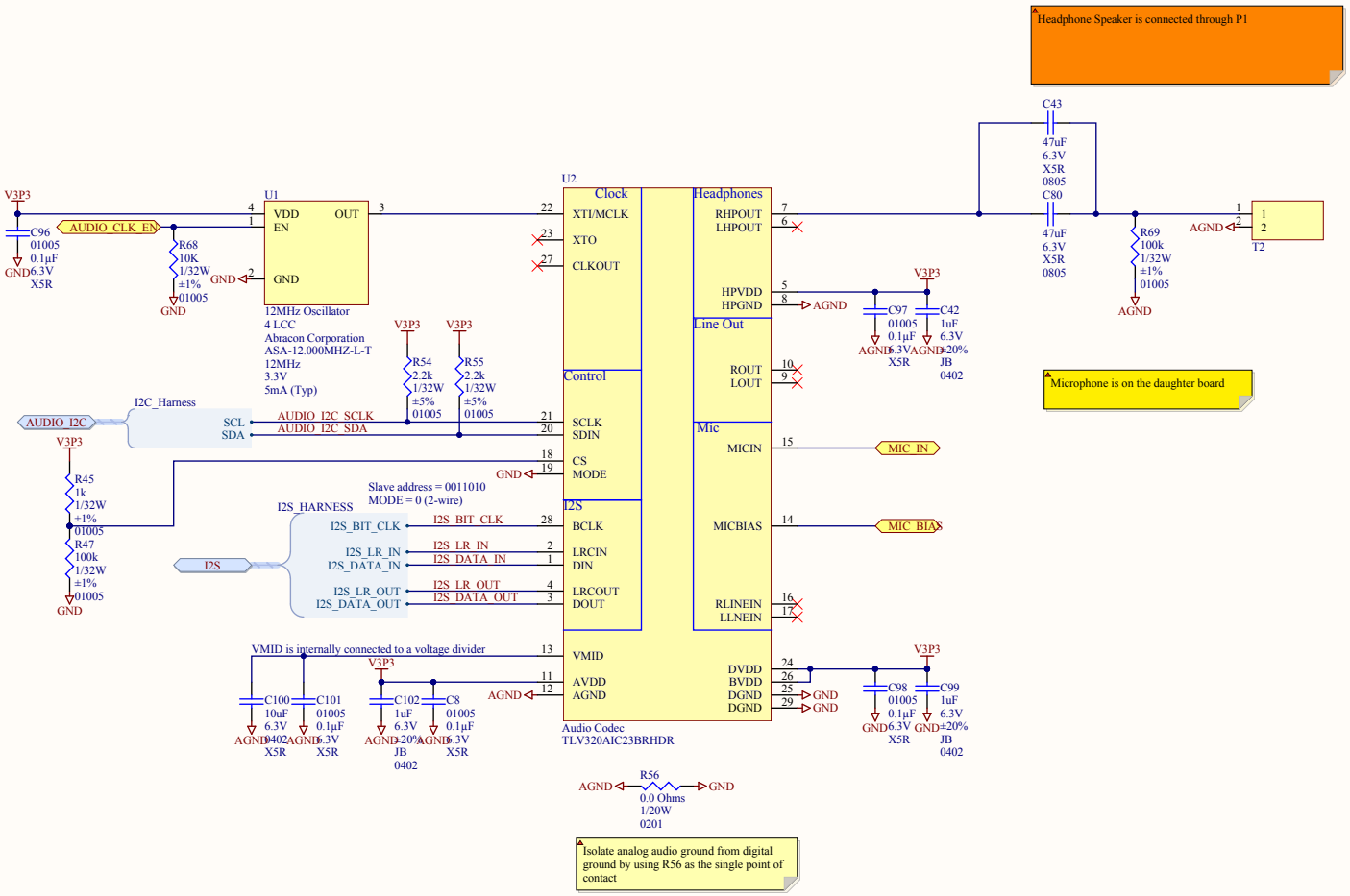


We are not using the SERDES so VCCA does not need to be quieter than the Core voltage (VCC)

VCC: 1.2V
VCCAUX: 3.3V (Startup cannot be > 30mV/uS during power-up)
VCCA: 1.2V
VCCIB: 1.2V or 1.5V
VCCOB: 1.2V or 1.5V
VCCPLL: 3.3V
VCCIO: 1.2 - 3.3V
VCCJ: 1.2 - 3.3V
Vref: 0.5 - 1.7V
Vtt: 0.5 - 1.3V (If not used Vtt should be left floating)



Title:	FPGA Power
Project:	Prototype Display Main Class I Rev B.PrjPCB
Document:	FPGA Power.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By: *	Revision: B
Date: 12/18/2013	Number: 9 of 16



Title:	Audio
Project:	Prototype Display Main Class I Rev B.PrjPCB
Document:	Audio.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By:	* Revision: B
Date:	2/6/2014 Number: 10 of 16

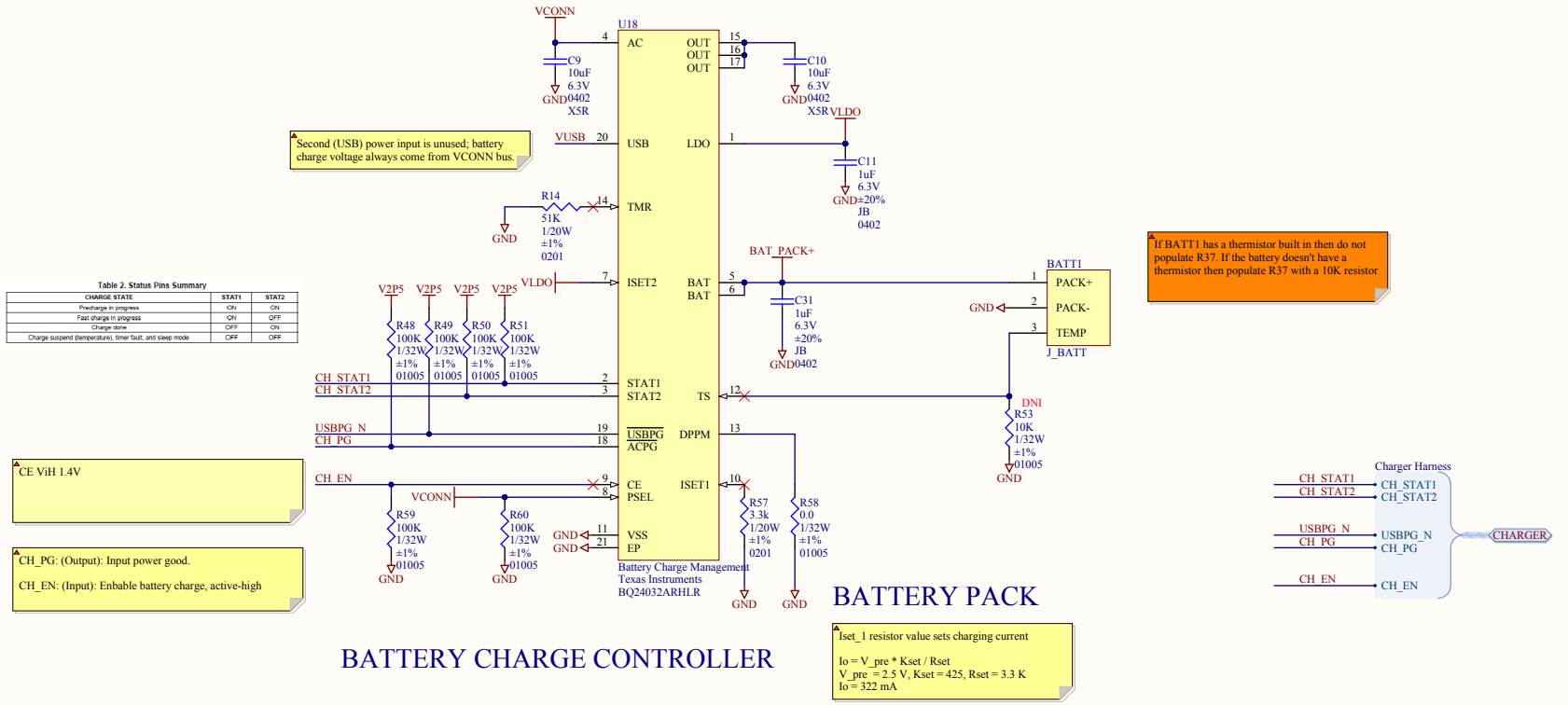
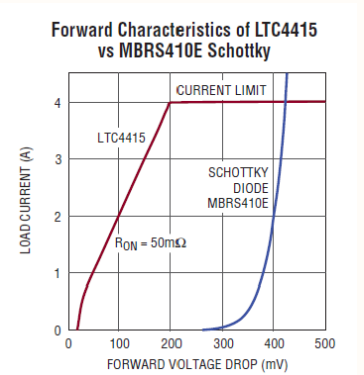
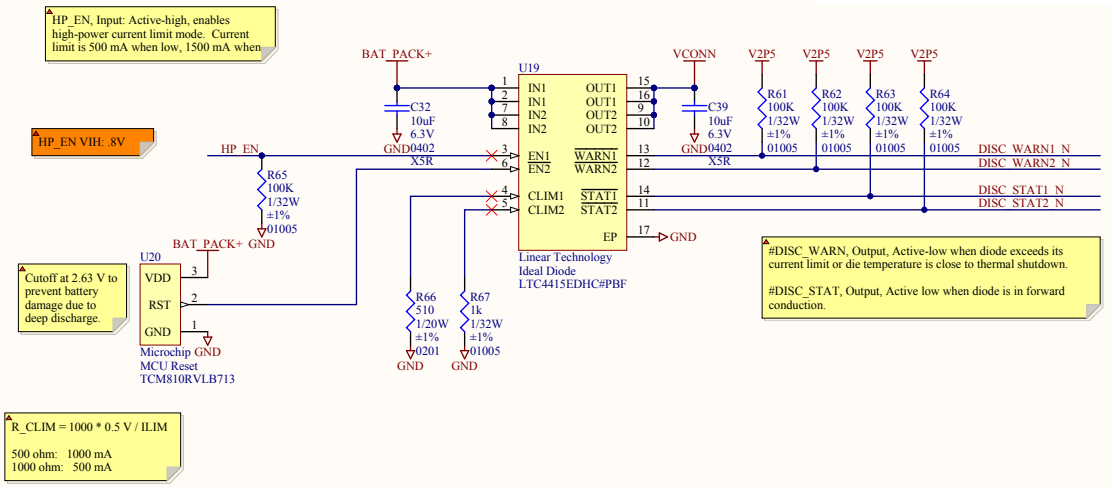


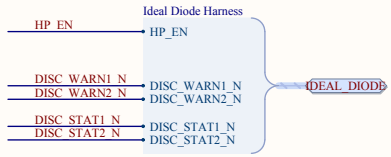
Table 2. Status Pins Summary

CHARGE STATE	STAT1	STAT2
Precharge in progress	ON	ON
Fast charge in progress	ON	OFF
Charge done	OFF	ON
Charge suspend (temperature), timer fault, and sleep mode	OFF	OFF

Title:	Battery Charger
Project:	Prototype Display Main Class I Rev B.PrjPCB
Document:	Battery Charger.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By: *	Revision: B
Date: 2/6/2014	Number: 11 of 16

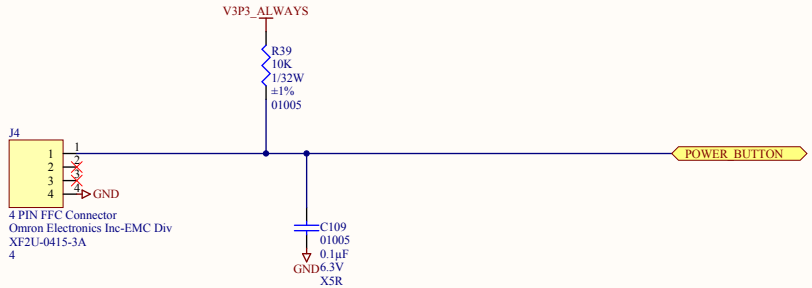




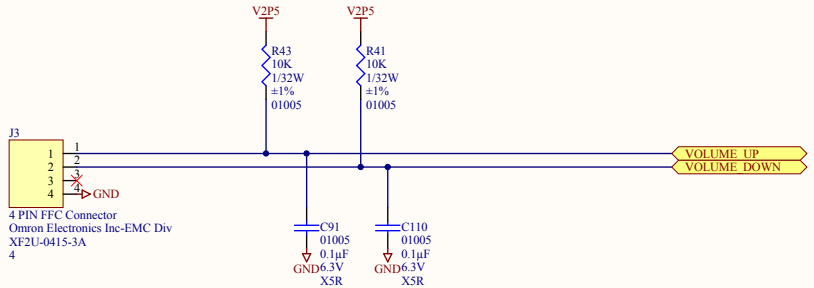


CURRENT-LIMITING DUAL IDEAL DIODE

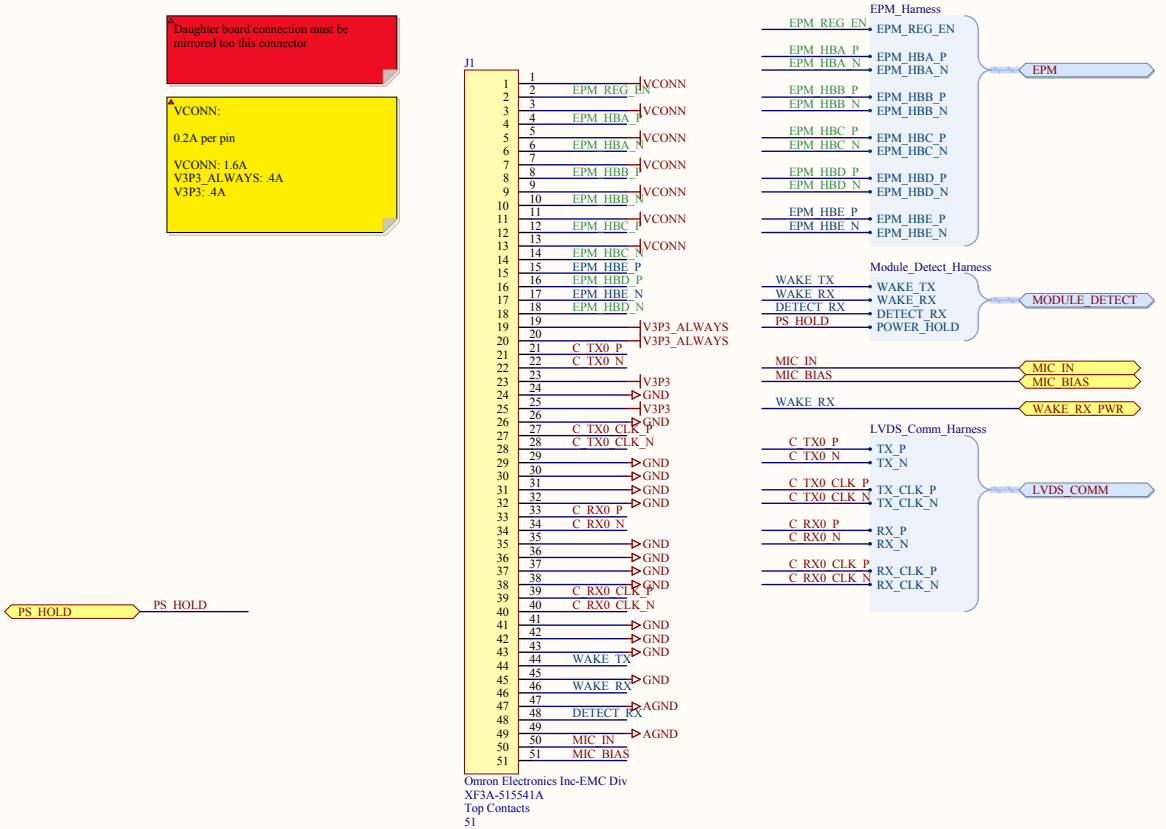
Title:	Ideal Diode		
Project:	Prototype Display Main Class I Rev B.PrjPCB		
Document:	Battery Charger Ideal Diode.SchDoc		
Engineer:	David McCoy (Cospan Design)		
Drawn By:	David McCoy		
Approved By:	*	Revision:	B
Date:	2/6/2014	Number:	12 of 16



Title:	Power Button Connector
Project:	Prototype Display Main Class I Rev B.PrjPCB
Document:	Power Button.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By:	* Revision: B
Date:	2/6/2014 Number: 13 of 16



Title:	Volume Button Connector		
Project:	Prototype Display Main Class I Rev B.PrjPCB		
Document:	Volume Buttons.SchDoc		
Engineer:	David McCoy (Cospan Design)		
Drawn By:	David McCoy		
Approved By:	*	Revision:	B
Date:	2/6/2014	Number:	14 of 16



Title:	Daughter Card Connector
Project:	Prototype Display Main Class I Rev B.PrjPCB
Document:	Daughter Card Connector.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By: *	Revision: B
Date: 2/6/2014	Number: 15 of 16