PROTOTYPE ARA 1 X 2 Template Project Alpha

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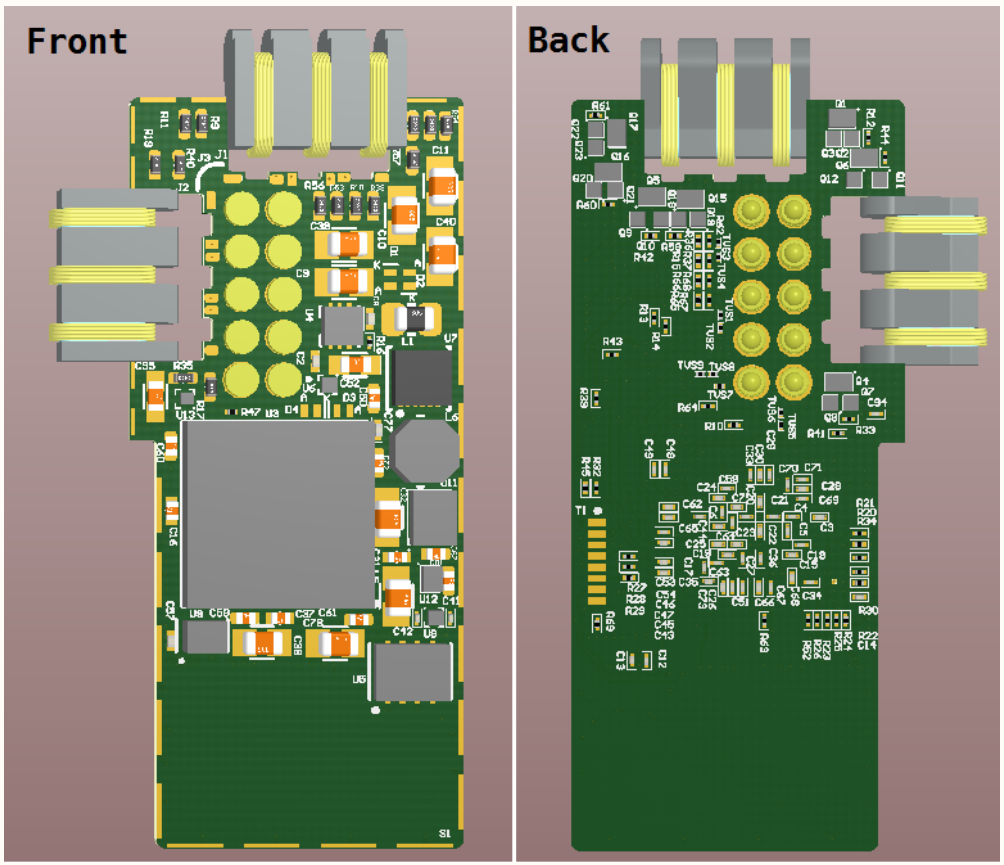
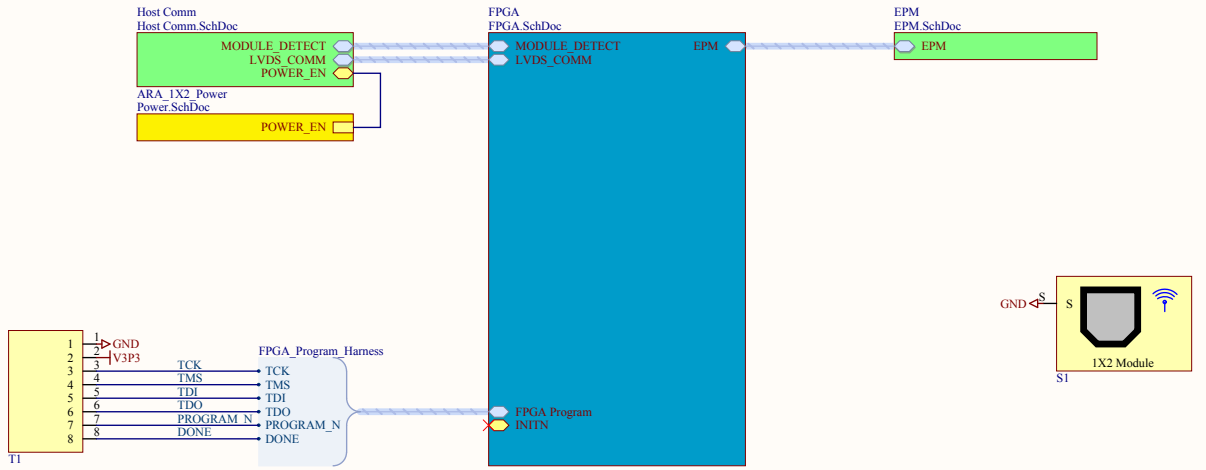
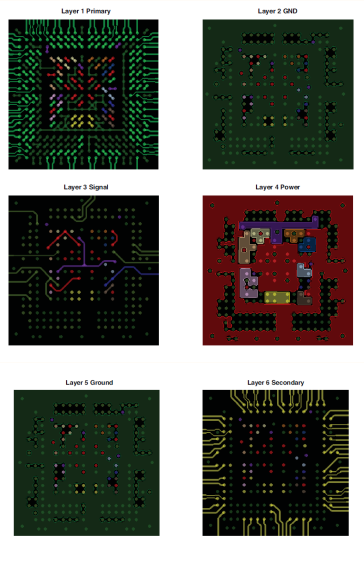
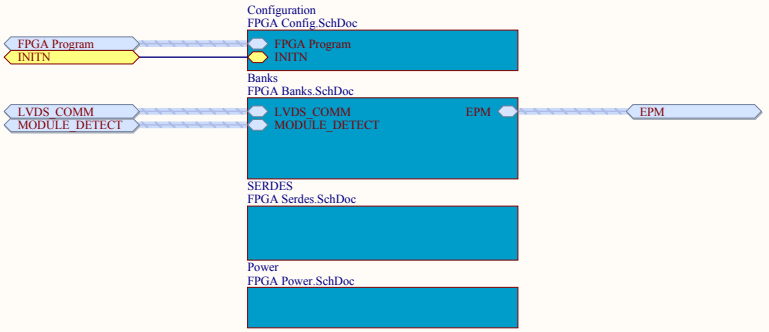


Block Diagram
Block Diagram.SchDoc



Title:	Block Diagram				
Project:	Prototype Module Template 1x2 Alpha.PrjPCB				
Document:	Block Diagram.SchDoc				
Engineer:	David McCoy (Cospan Design)				
Drawn By:	David McCoy				
Approved By:	*	Revision:	A		
Date:	10/29/2013	Number:	2	of	10



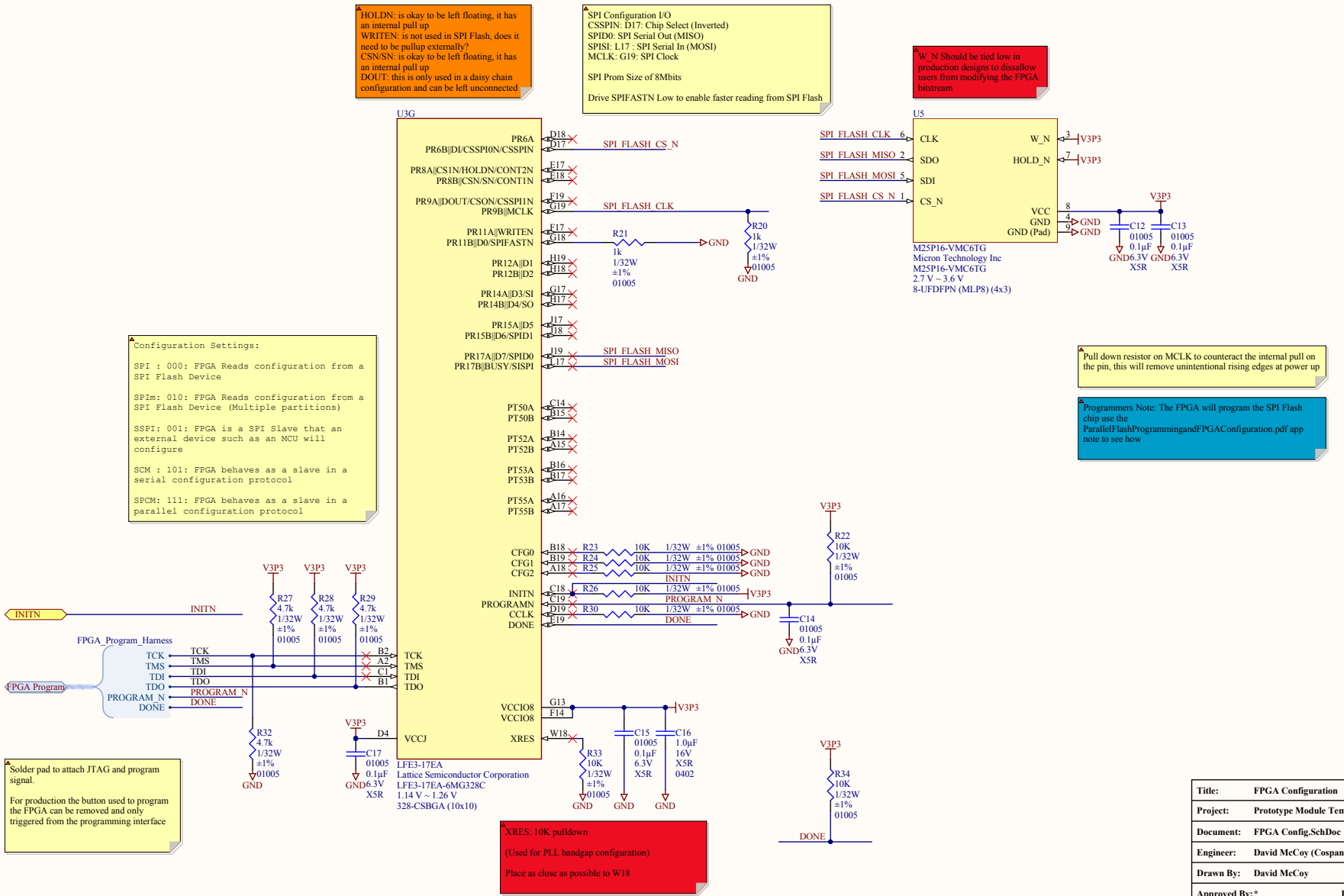


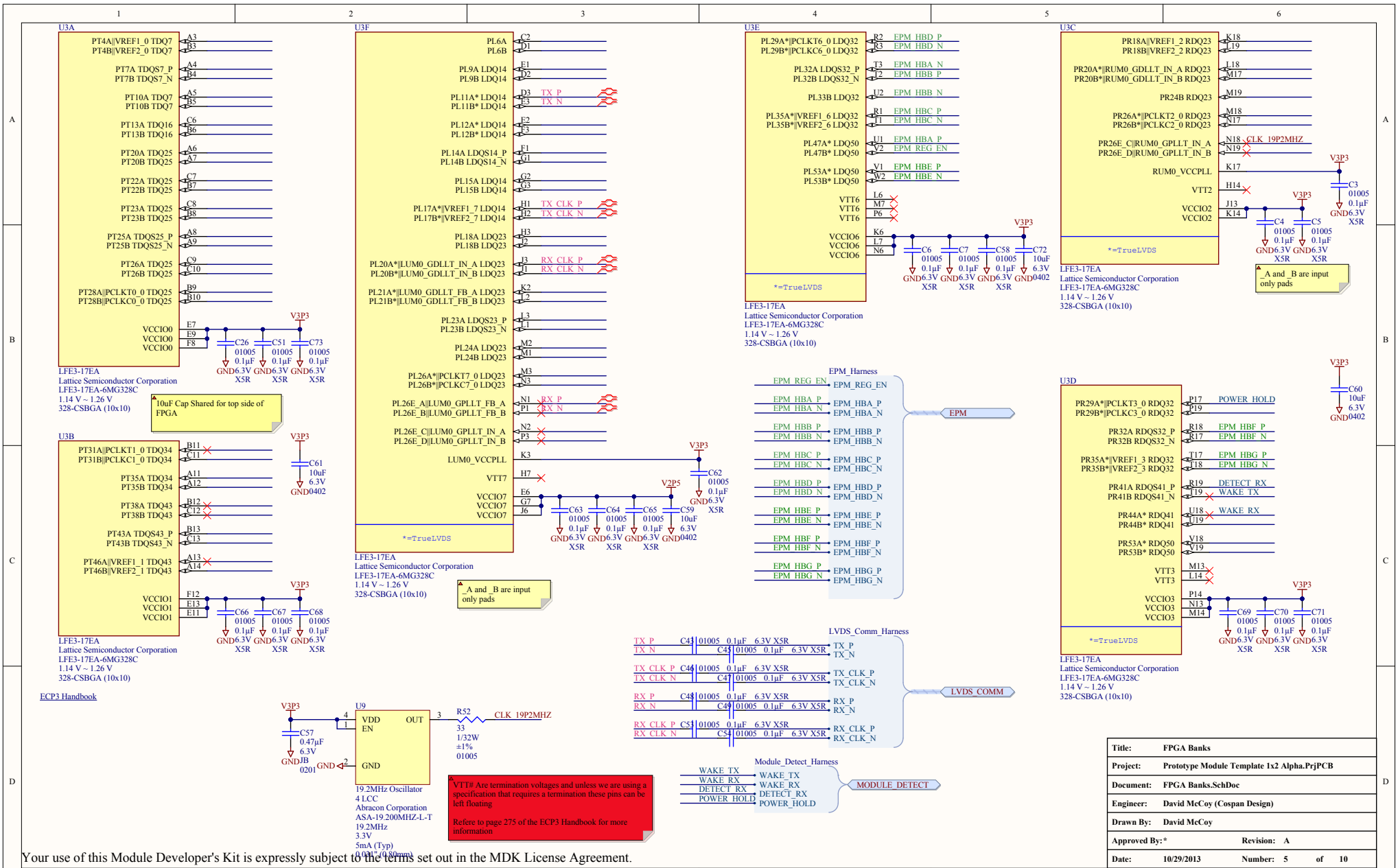
Layout Guidlines:

6 Layer Stackup
3-mil trace
5-mil via

PCB Layout Recommendations

Title:	FPGA				
Project:	Prototype Module Template 1x2 Alpha.PrjPCB				
Document:	FPGA.SchDoc				
Engineer:	David McCoy (Cospan Design)				
Drawn By:	David McCoy				
Approved By:	*	Revision:	A		
Date:	10/29/2013	Number:	3	of	10





Title:	FPGA Banks
Project:	Prototype Module Template 1x2 Alpha.PrjPCB
Document:	FPGA Banks.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By:	*
Revision:	A
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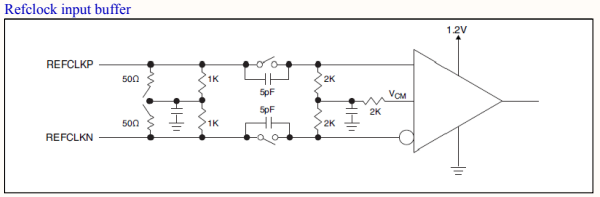
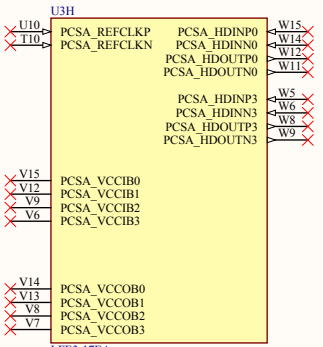
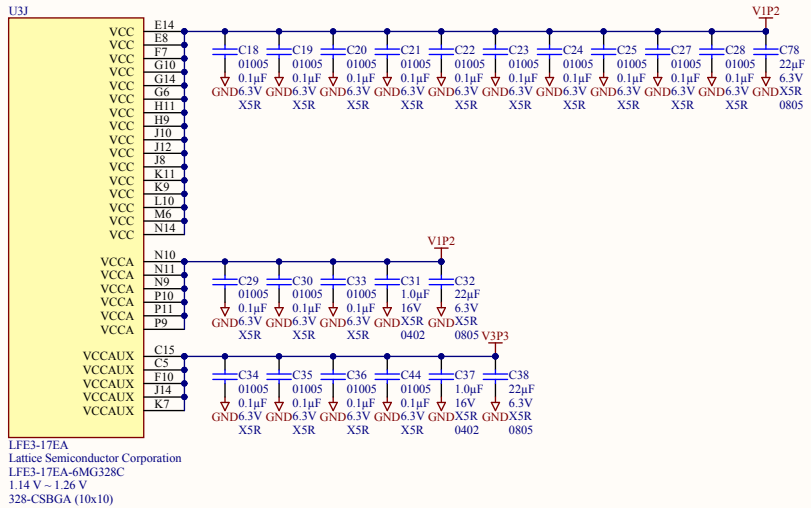
Number:	5 of 10

Refclock input buffer

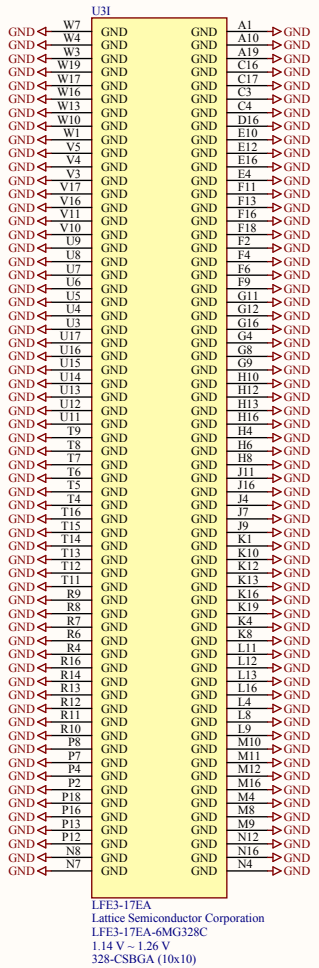




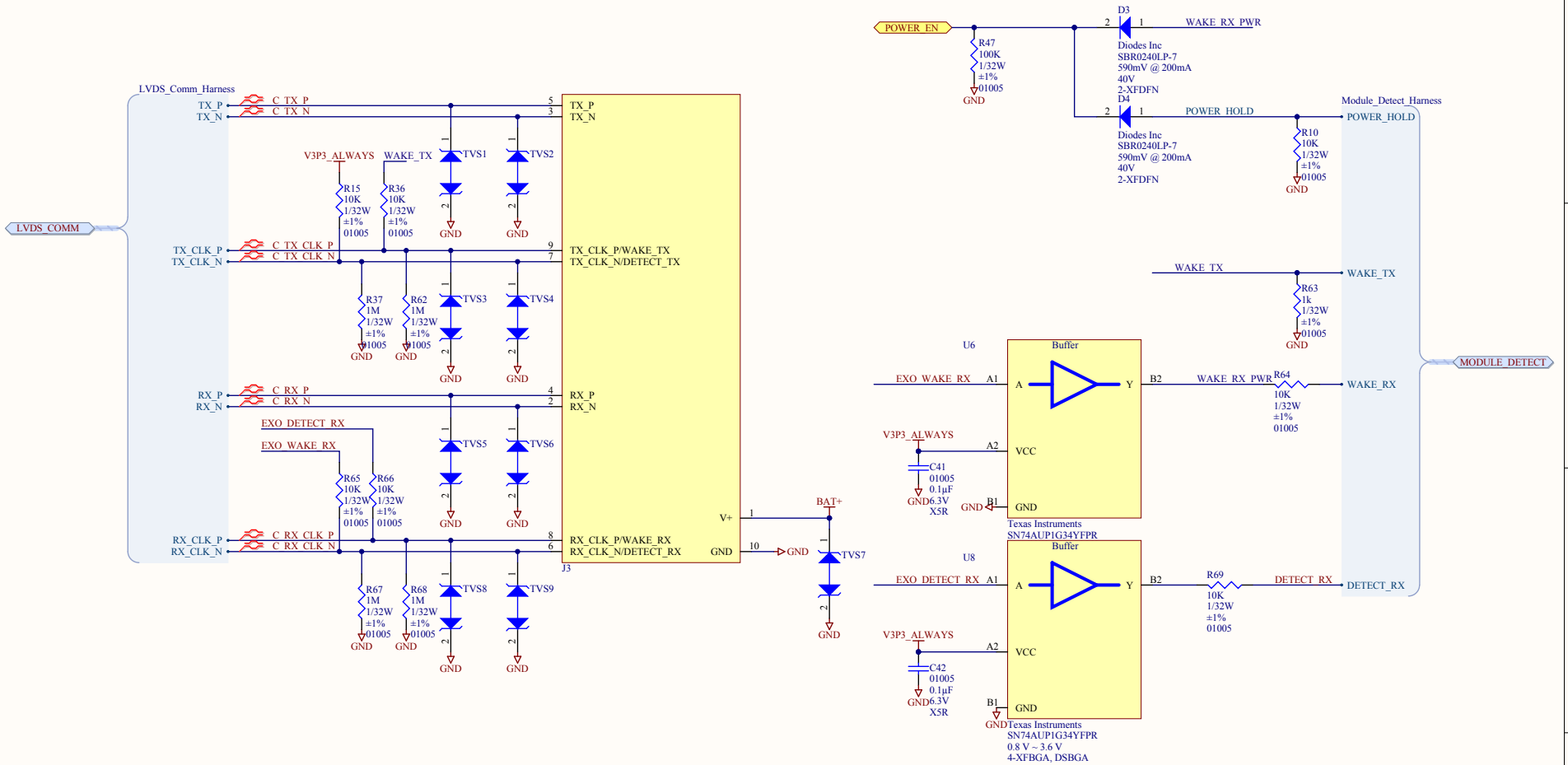
Title:	FPGA SERDES			
Project:	Prototype Module Template 1x2 Alpha.PrjPCB			
Document:	FPGA Serdes.SchDoc			
Engineer:	David McCoy (Cospan Design)			
Drawn By:	David McCoy			
Approved By:	*	Revision:	A	
Date:	10/29/2013	Number:	6 of 10	



VCC: 1.2V
VCCAUX: 3.3V (Startup cannot be > 30mV/uS during power-up)
VCCA: 1.2V
VCCIB: 1.2V or 1.5V
VCCOB: 1.2V or 1.5V
VCCPLL: 3.3V
VCCIO: 1.2 - 3.3V
VCCJ: 1.2 - 3.3V
Vref: 0.5 - 1.7V
Vtt: 0.5 - 1.3V (If not used Vtt should be left floating)



Title:	FPGA Power		
Project:	Prototype Module Template 1x2 Alpha.PrjPCB		
Document:	FPGA Power.SchDoc		
Engineer:	David McCoy (Cospan Design)		
Drawn By:	David McCoy		
Approved By:	*	Revision:	A
Date:	10/29/2013	Number:	7 of 10



Title:	Host Comm			
Project:	Prototype Module Template 1x2 Alpha.PrjPCB			
Document:	Host Comm.SchDoc			
Engineer:	David McCoy (Cospan Design)			
Drawn By:	David McCoy			
Approved By:	*	Revision:	A	
Date:	10/29/2013	Number:	8 of 10	

EPM_Harness

EPM_REG_EN
EPM_HBA_P
EPM_HBA_N
EPM_HBB_P
EPM_HBB_N
EPM_HBC_P
EPM_HBC_N
EPM_HBD_P
EPM_HBD_N
EPM_HBE_P
EPM_HBE_N
EPM_HBF_P
EPM_HBF_N
EPM_HBG_P
EPM_HBG_N

EPM

Vout = 1.255V (1 + R1/R2)
Vout = 1.255V (1 + 100K / 4.7K)
Vout = 27.9V

PFET:

Maximum VGS: -12V

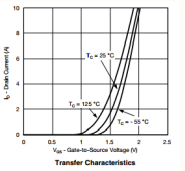
Gate 28V - 12V: 16V

For safety VGate: 20V

Resistor Divider
VGate/Vin = Rtop/Rbot+Rtop

Vout = 28 * (270 / 270 + 100)
Vout = 20.48V

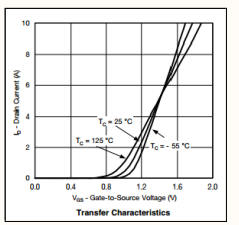
PFET VGS Characteristics



Pulse width of 300uS @ 100 mA and 28V will increase both resistors < .432 degrees (fahrenheit)

4nS turn on time for PFET
12nS turn off time for PFET

NFET Transfer Characteristics



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Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By:	* Revision: A
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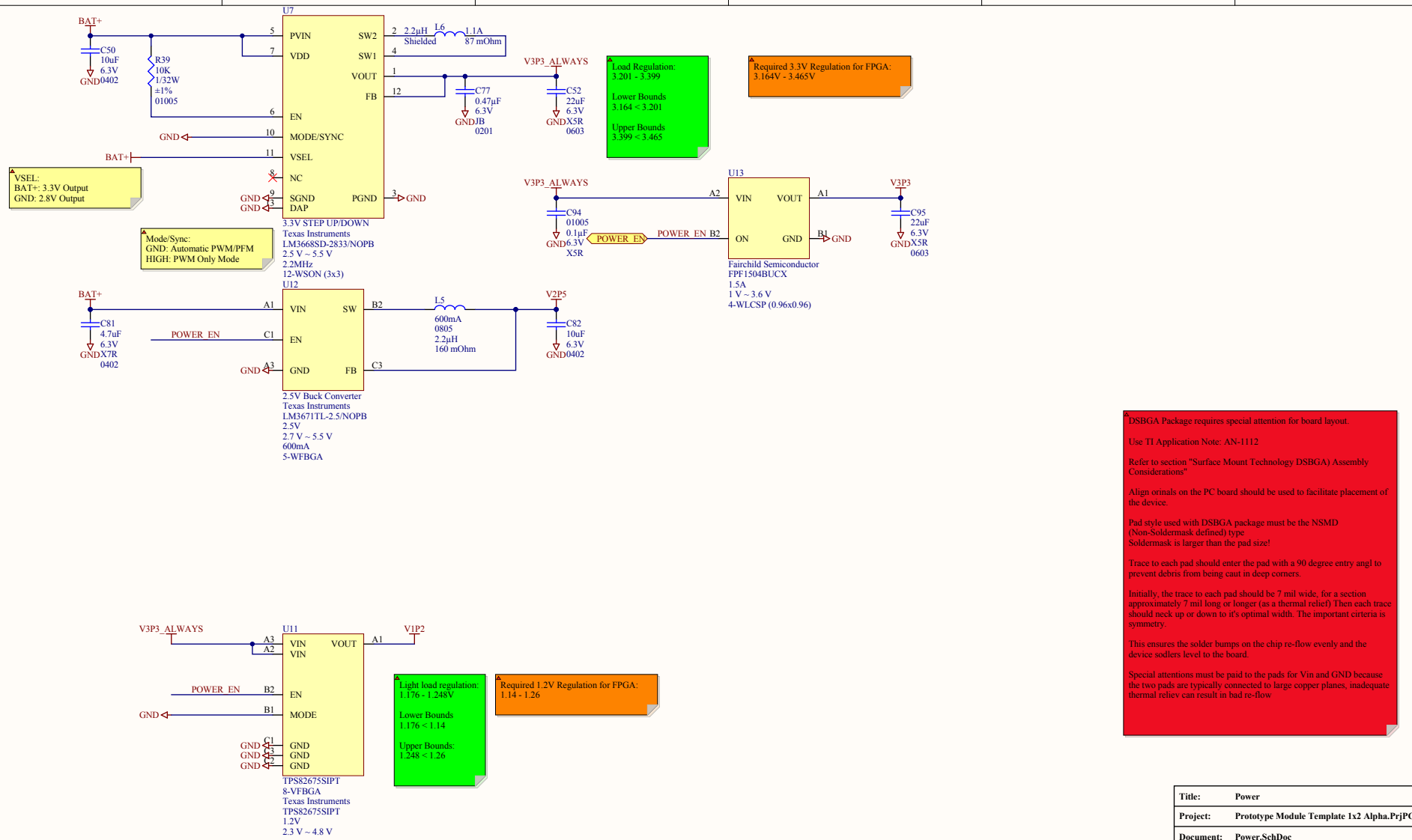

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Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By: *	Revision: A
Date: 10/29/2013	Number: 10 of 10