PROTOTYPE **Battery Charger Module** **Alpha**

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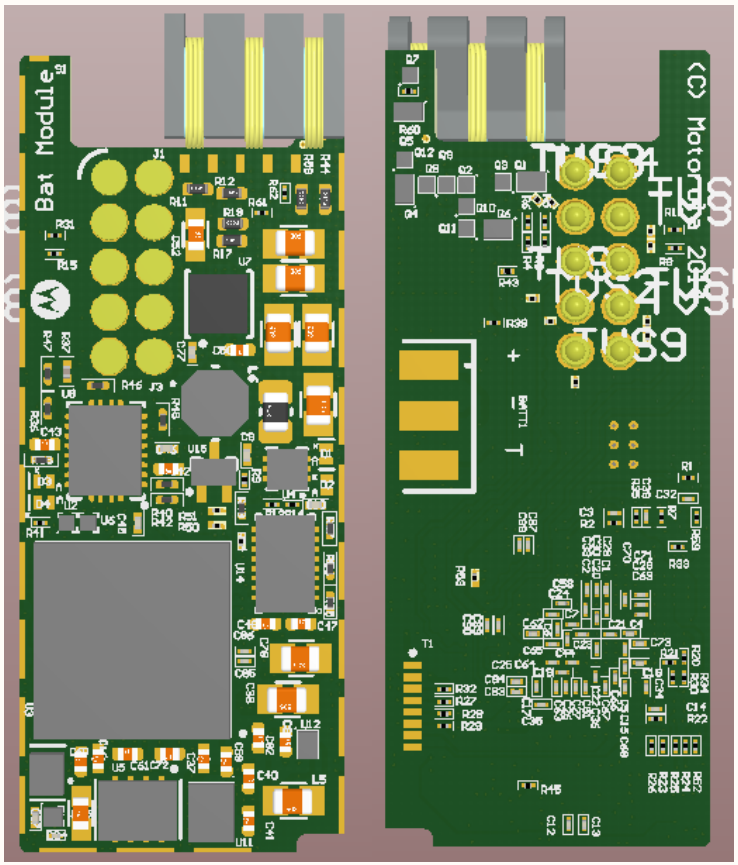
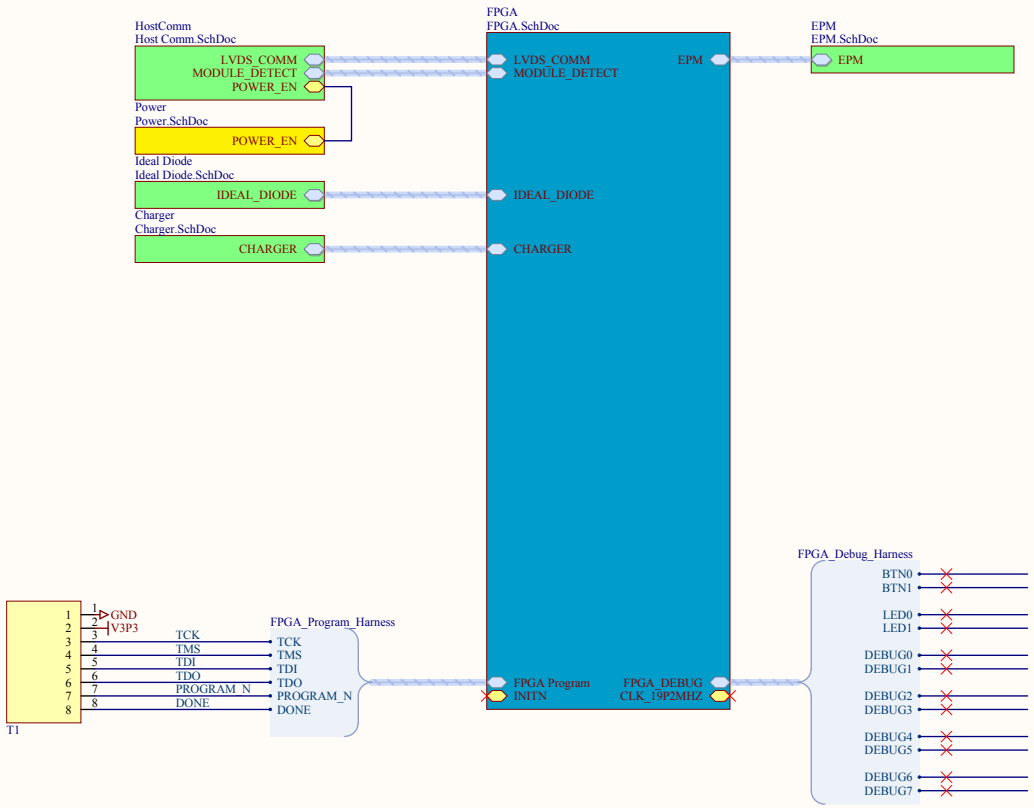
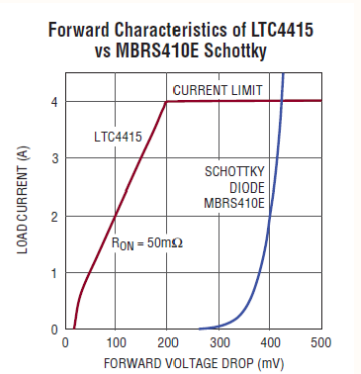
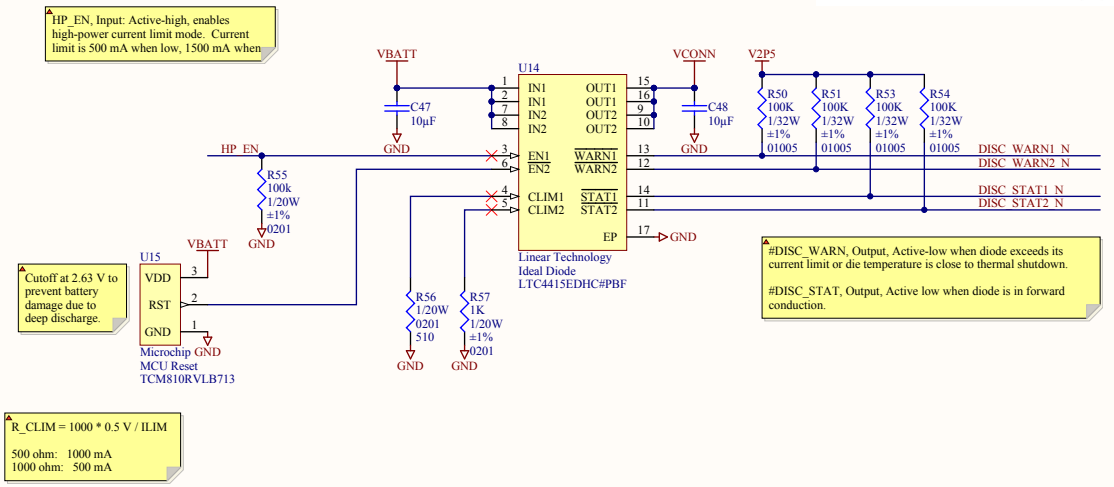


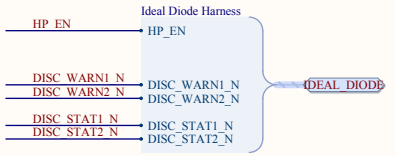
Block Diagram
Block Diagram.SchDoc



Title:	Block Diagram				
Project:	Prototype Battery Module 2x2 Alpha.PrjPCB				
Document:	Block Diagram.SchDoc				
Engineer:	David McCoy (Cospan Design)				
Drawn By:	David McCoy				
Approved By:	*	Revision:	C		
Date:	12/18/2013	Number:	2	of	13







CURRENT-LIMITING DUAL IDEAL DIODE

Title:	Ideal Diode
Project:	Prototype Battery Module 2x2 Alpha.PrjPCB
Document:	Ideal Diode.SchDoc
Engineer:	Ara Knaian
Drawn By:	Ara Knaian
Approved By:	* Revision: C
Date:	12/17/2013 Number: 4 of 13

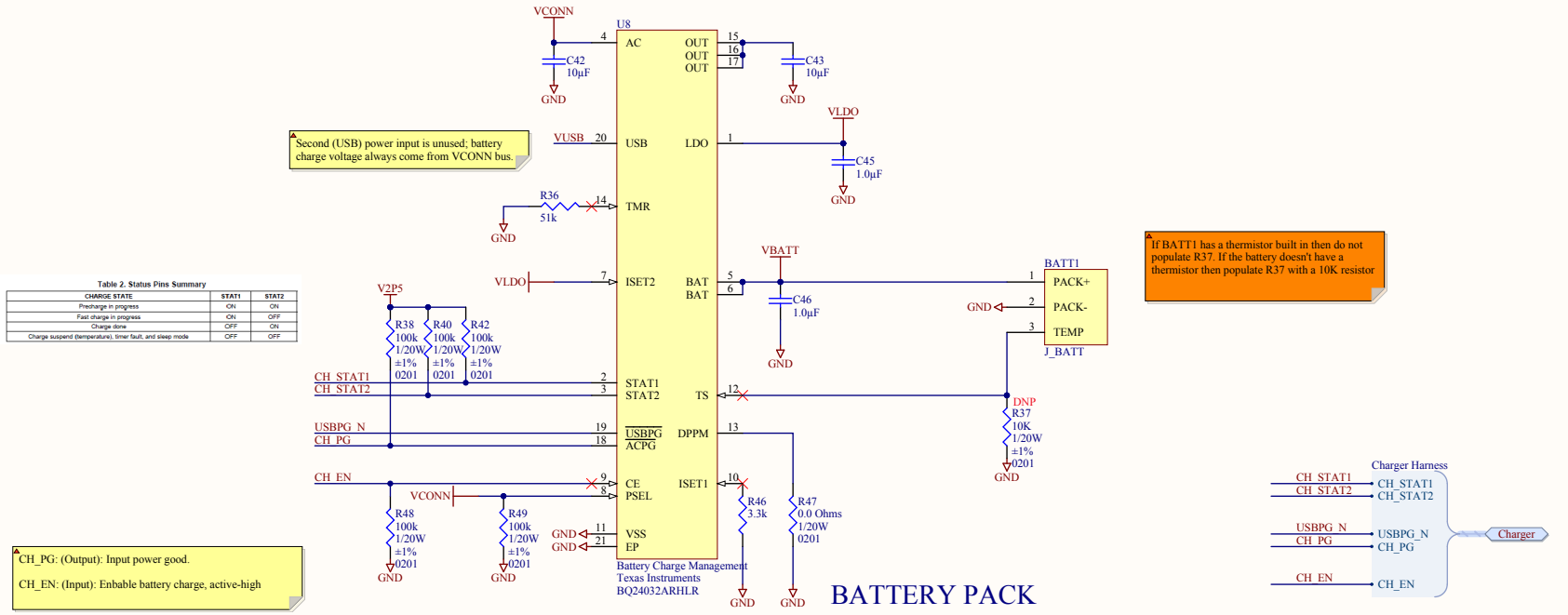


Table 2. Status Pins Summary		
CHARGE STATE	STAT1	STAT2
Precharge in progress	ON	ON
Fast charge in progress	ON	OFF
Charge done	OFF	ON
Charge suspend (temperature), timer fault, and sleep mode	OFF	OFF

CH_PG: (Output): Input power good.

CH_EN: (Input): Enbable battery charge, active-high

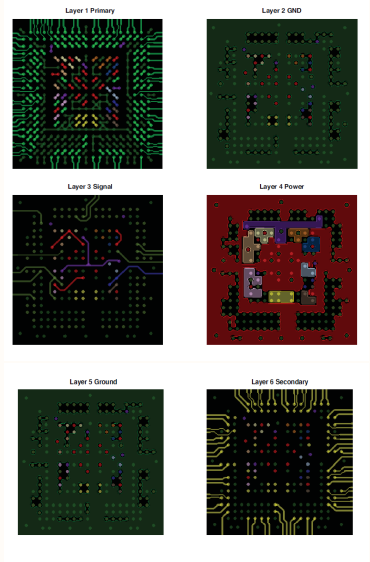
BATTERY CHARGE CONTROLLER

BATTERY PACK

Iset_1 resistor value sets charging current

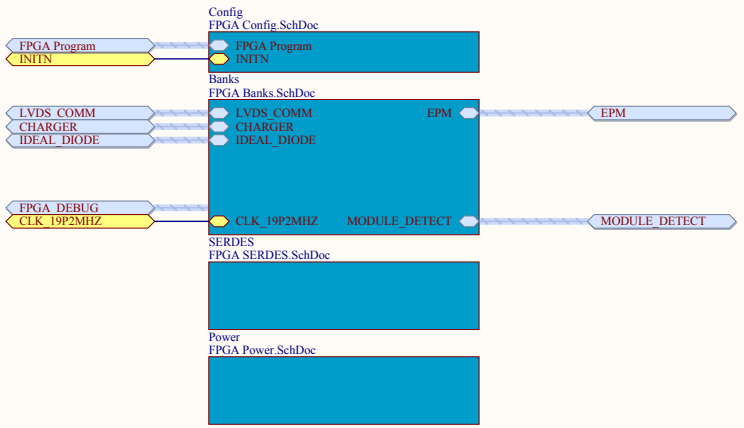
Io = V_pre * Kset / Rset
V_pre = 2.5 V, Kset = 425, Rset = 3.3 K
Io = 322 mA

Title:	Charger		
Project:	Prototype Battery Module 2x2 Alpha.PrjPCB		
Document:	Charger.SchDoc		
Engineer:	Ara Knaian		
Drawn By:	Ara Knaian		
Approved By:	*	Revision:	C
Date:	12/17/2013	Number:	5 of 13

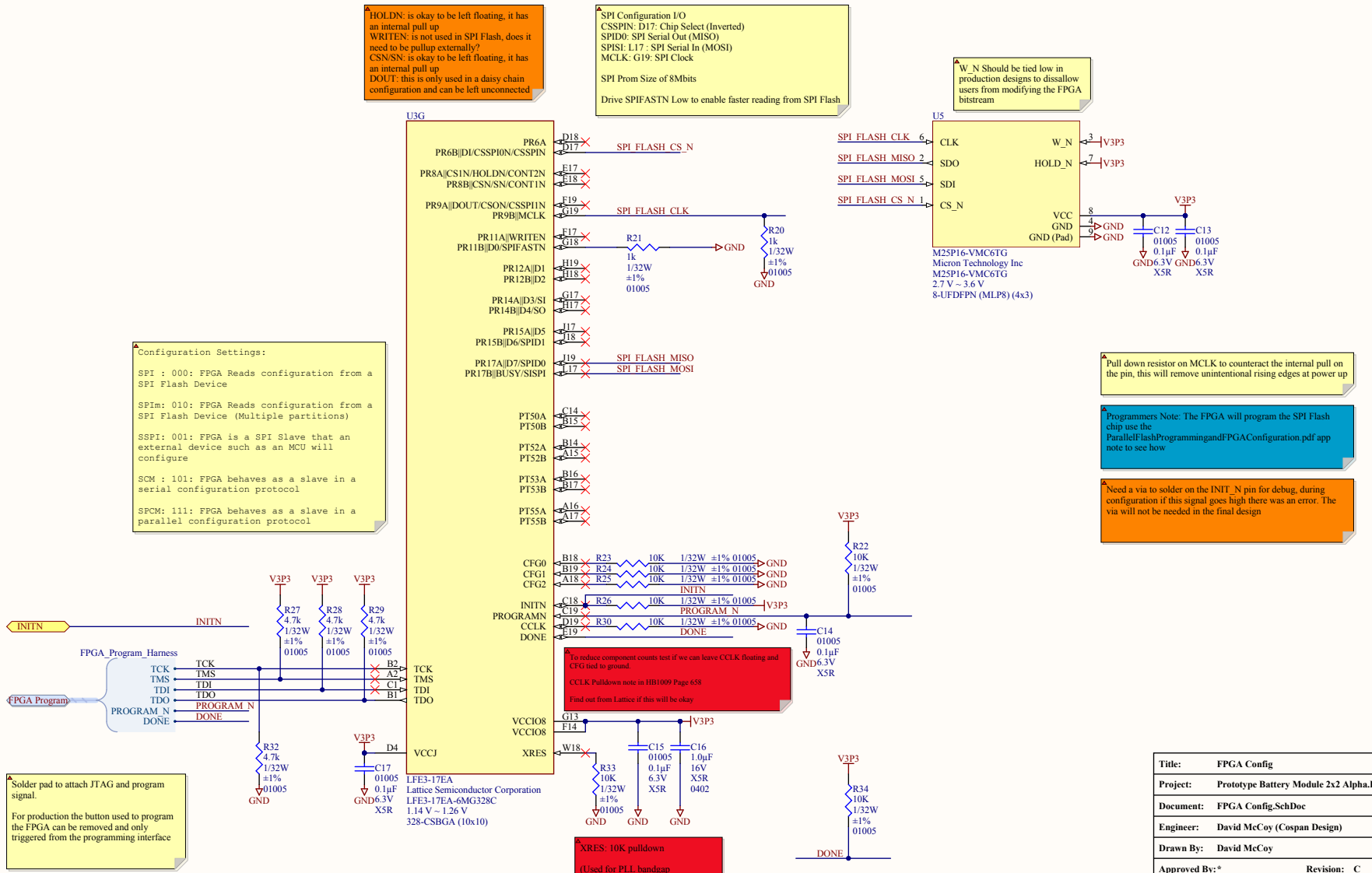


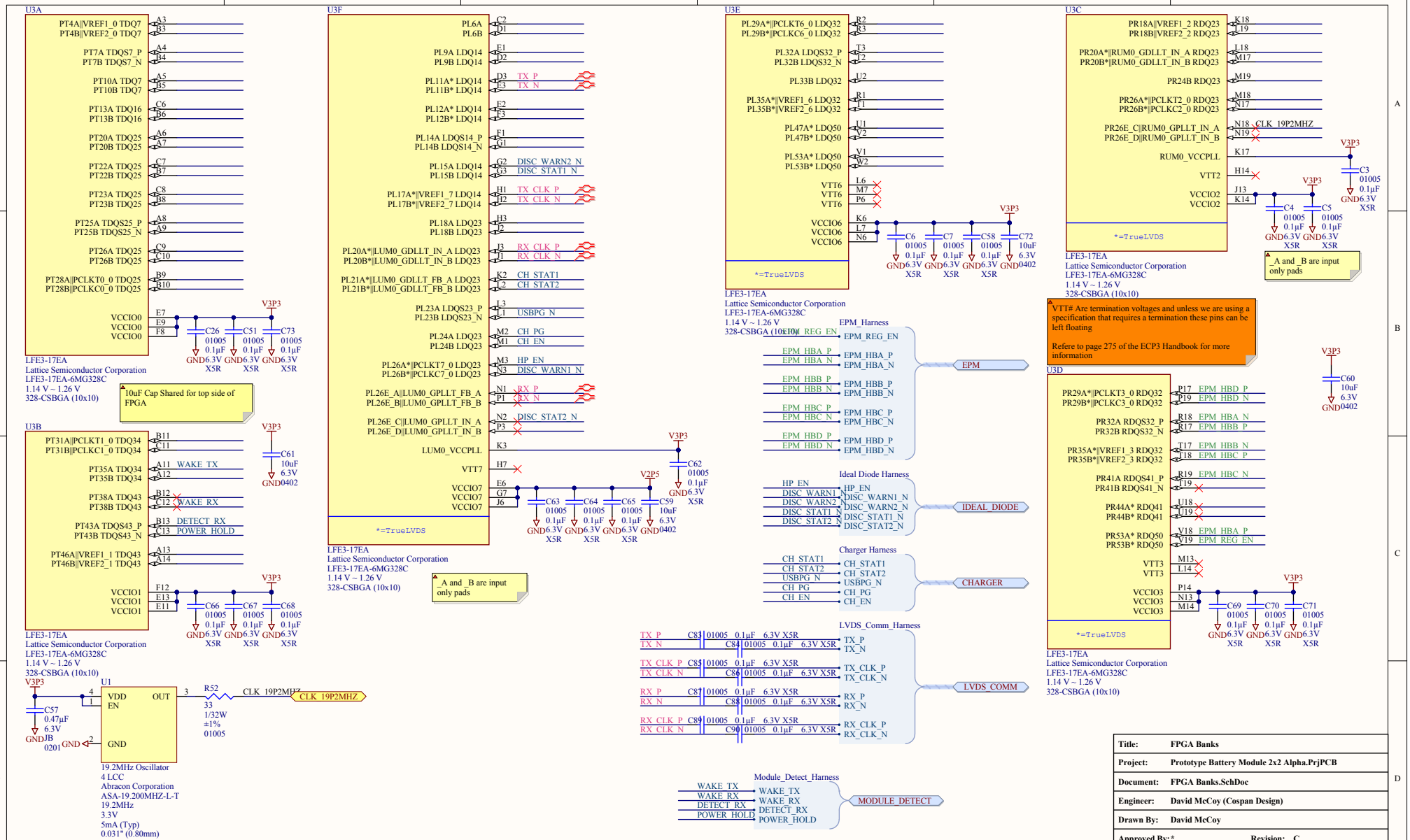
Layout Guidlines:

6 Layer Stackup
3-mil trace
5-mil via



Title:	**FPGA**				
Project:	**Prototype Battery Module 2x2 Alpha.PrjPCB**				
Document:	**FPGA.SchDoc**				
Engineer:	**David McCoy (Cospan Design)**				
Drawn By:	**David McCoy**				
Approved By:	*****	**Revision:**	**C**		
Date:	**12/18/2013**	**Number:**	**6**	**of**	**13**





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Title:	FPGA Banks
Project:	Prototype Battery Module 2x2 Alpha.PrjPCB
Document:	FPGA Banks.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By: *	Revision: C
Date: 12/18/2013	Number: 8 of 13

Vout = 1.255V (1 + R1/R2)
Vout = 1.255V (1 + 100K / 4.7K)
Vout = 27.9V

PFET:

Maximum VGS: -12V

Gate 28V - 12V: 16V

For safety VGate: 20V

Resistor Divider
VGate/Vin = Rtop/Rbot+Rtop

Vout = 28 * (270 / 270 + 100)
Vout = 20.48V

Pulse width of 300uS @ 100 mA and 28V will increase both resistors < .432 degrees (fahrenheit)

4nS turn on time for PFET
12nS turn off time for PFET

L2
240mA
0806
22µH
1.8 Ohm

U4
Linear Technology
LT3460EDC-1#TRPBF
1.255 V ~ 36 V
2.5 V ~ 16 V
650kHz
180mA
6-DFN (2x2)

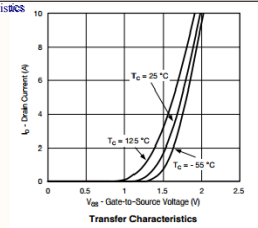
D1
Diodes Inc
SBR0240LP-7
590mV @ 200mA
40V
2-XFDFN

D2
Diodes Inc
SBR0240LP-7
590mV @ 200mA
40V
2-XFDFN

V3P3
V28P0
GND

C9 0.1µF 6.3V X5R 0201
C10 22pF 50V C0G, NP0 0201
C8 C11 C31 C49 C53 22µF 35V JB 0805
R13 100K 1/32W ±1% 01005
R14 4.7k 1/32W ±1% 01005
R9 1k 1/32W ±1% 01005
EPM_REG_EN

PFET VGS Characteristics



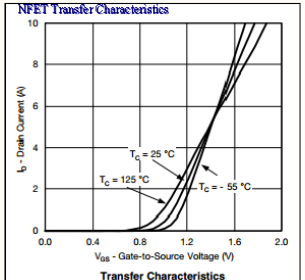
R11 100 1/5W 0402 ±1% Pulse Withstanding
R12 270 1/5W 0402 ±1% Pulse Withstanding
Q1 1.1V @ 250µA 53 mOhm @ 1.5A, 4.5V 30V
Q2 900mV @ 250µA 95 mOhm @ 1A, 4.5V 30V 1.8A (Ta) 10nC @ 8V 4-UFBGA
R59 1k 1/32W ±1% 01005
EPM_HBA_P
EPM_HBA_N
EPMA

J1
EPM0_P EPM0_N EPM1_P EPM1_N EPM2_P EPM2_N
EPMA EPMB EPMC EPMD
EPM

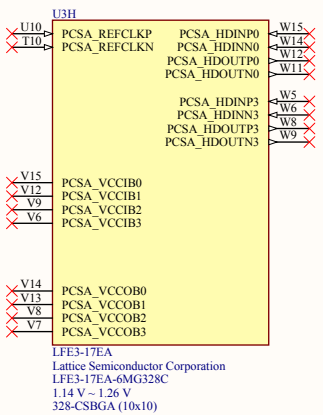
EPM_Harness
EPM_REG_EN
EPM_HBA_P EPM_HBA_N
EPM_HBB_P EPM_HBB_N
EPM_HBC_P EPM_HBC_N
EPM_HBD_P EPM_HBD_N

R16 R18 R17 R19 R44 R58 100 1/5W 0402 ±1% Pulse Withstanding
R60 R61 R62 1k 1/32W ±1% 01005
Q5 Q6 Q4 1.1V @ 250µA 53 mOhm @ 1.5A, 4.5V 30V 5.9A (Ta), 13A (Tc) 49nC @ 10V 6-UFBGA
Q7 Q8 Q10 Q11 Q9 Q12 900mV @ 250µA 95 mOhm @ 1A, 4.5V 30V 1.8A (Ta) 10nC @ 8V 4-UFBGA
EPMB EPMC EPMD

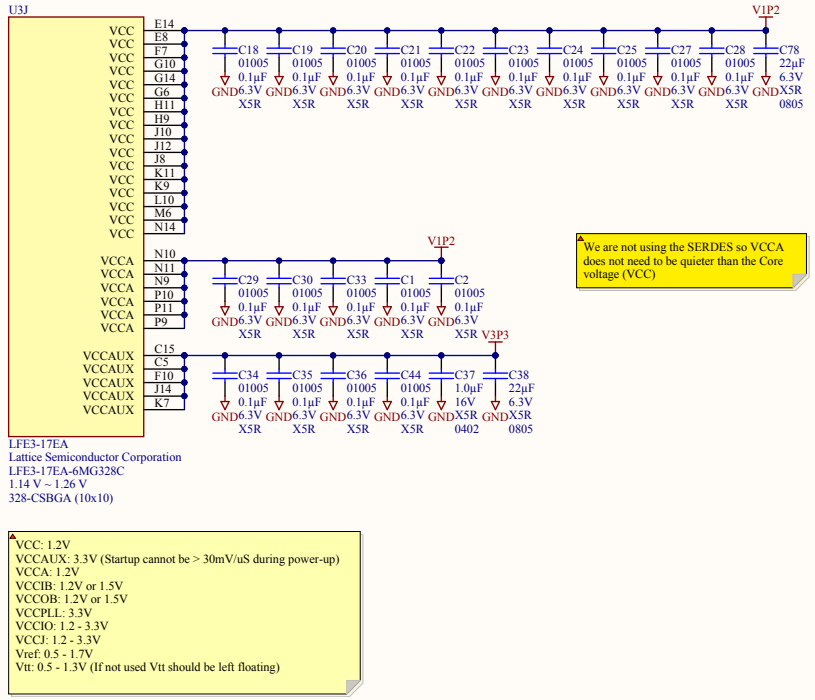
NFET Transfer Characteristics



Title:	EPM		
Project:	Prototype Battery Module 2x2 Alpha.PrjPCB		
Document:	EPM.SchDoc		
Engineer:	David McCoy (Cospan Design)		
Drawn By:	David McCoy		
Approved By:	*	Revision:	C
Date:	12/18/2013	Number:	9 of 13

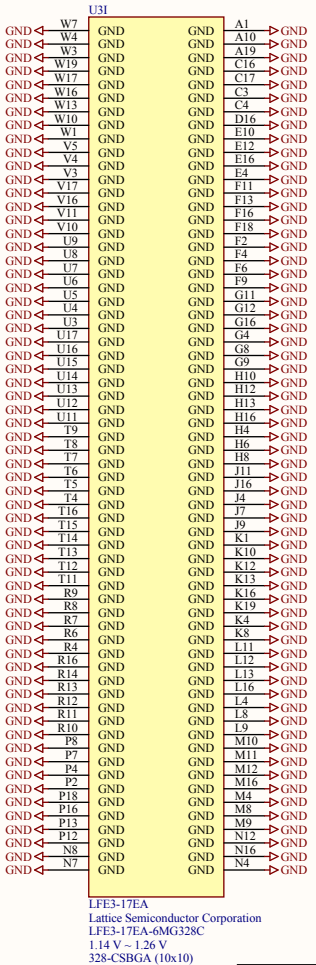


Title:	FPGA SERDES			
Project:	Prototype Battery Module 2x2 Alpha.PrjPCB			
Document:	FPGA SERDES.SchDoc			
Engineer:	David McCoy (Cospan Design)			
Drawn By:	David McCoy			
Approved By:	*	Revision:	C	
Date:	12/18/2013	Number:	10 of 13	

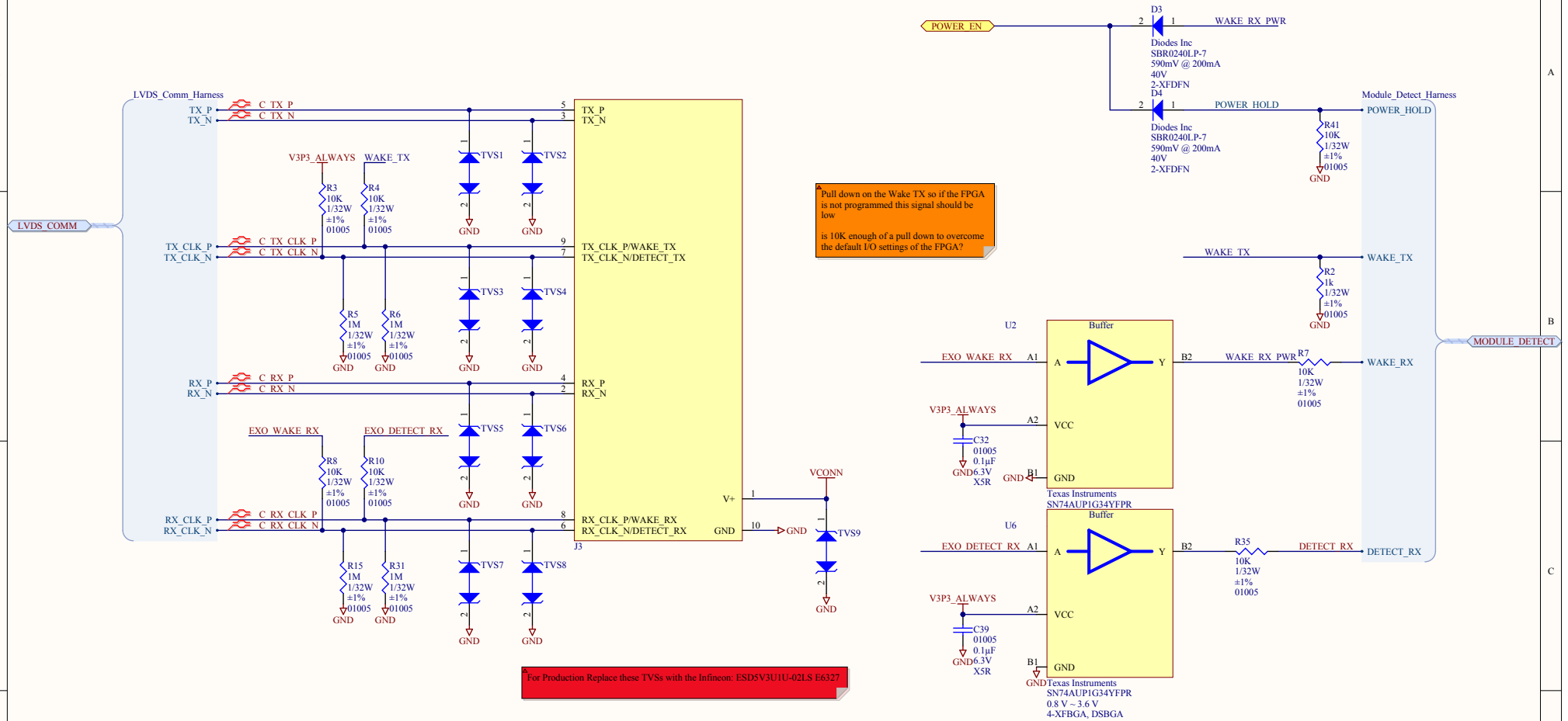


We are not using the SERDES so VCCA does not need to be quieter than the Core voltage (VCC)

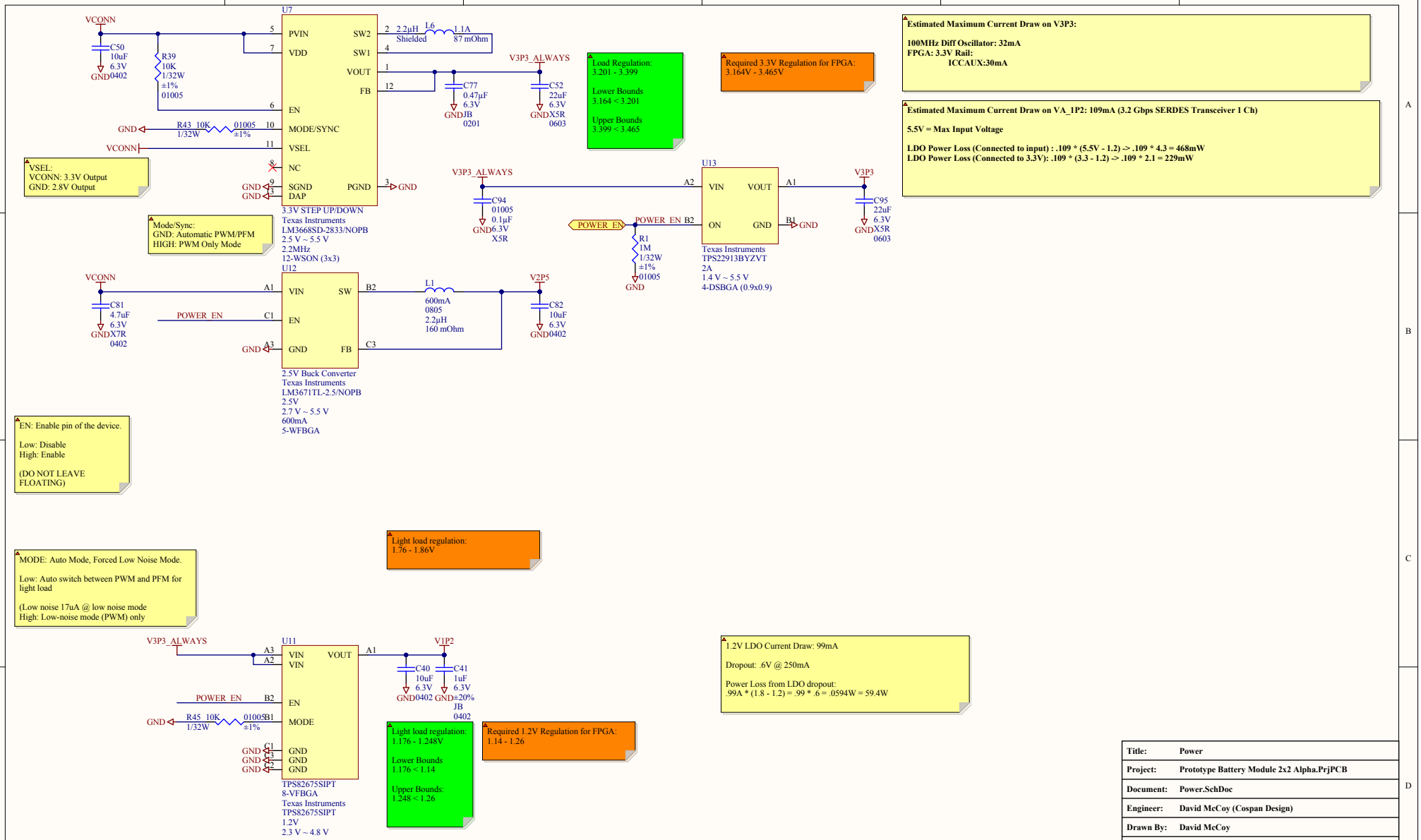
VCC: 1.2V
VCCAUX: 3.3V (Startup cannot be > 30mV/uS during power-up)
VCCA: 1.2V
VCCIB: 1.2V or 1.5V
VCCOB: 1.2V or 1.5V
VCCPLL: 3.3V
VCCIO: 1.2 - 3.3V
VCCJ: 1.2 - 3.3V
Vref: 0.5 - 1.7V
Vtt: 0.5 - 1.3V (If not used Vtt should be left floating)



Title:	FPGA Power		
Project:	Prototype Battery Module 2x2 Alpha.PrjPCB		
Document:	FPGA Power.SchDoc		
Engineer:	David McCoy (Cospan Design)		
Drawn By:	David McCoy		
Approved By:	*	Revision:	C
Date:	12/18/2013	Number:	11 of 13



Title:	Host Communication			
Project:	Prototype Battery Module 2x2 Alpha.PrjPCB			
Document:	Host Comm.SchDoc			
Engineer:	David McCoy (Cospan Design)			
Drawn By:	David McCoy			
Approved By:	*	Revision:	C	
Date:	12/18/2013	Number:	12 of 13	



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Title:	Power
Project:	Prototype Battery Module 2x2 Alpha.PrjPCB
Document:	Power.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By: *	Revision: C
Date: 12/18/2013	Number: 13 of 13