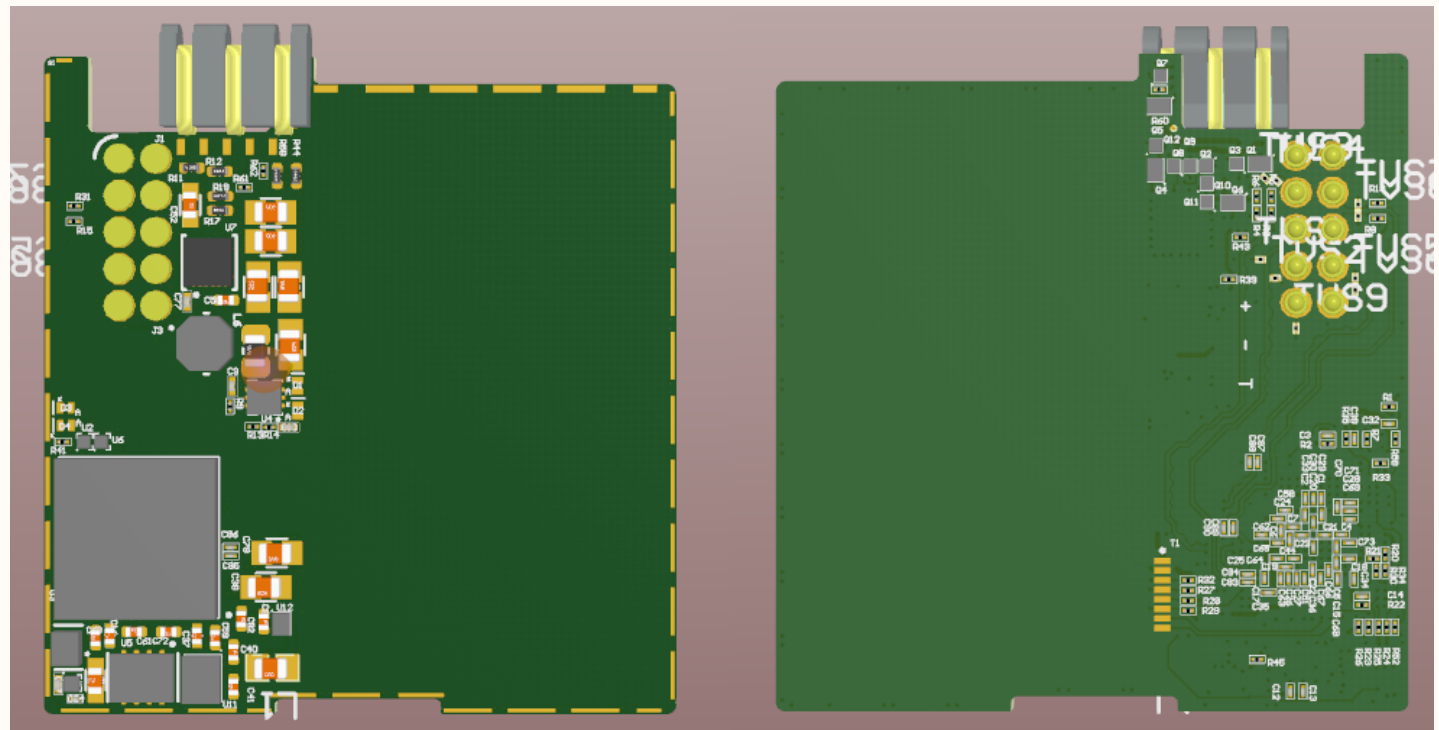
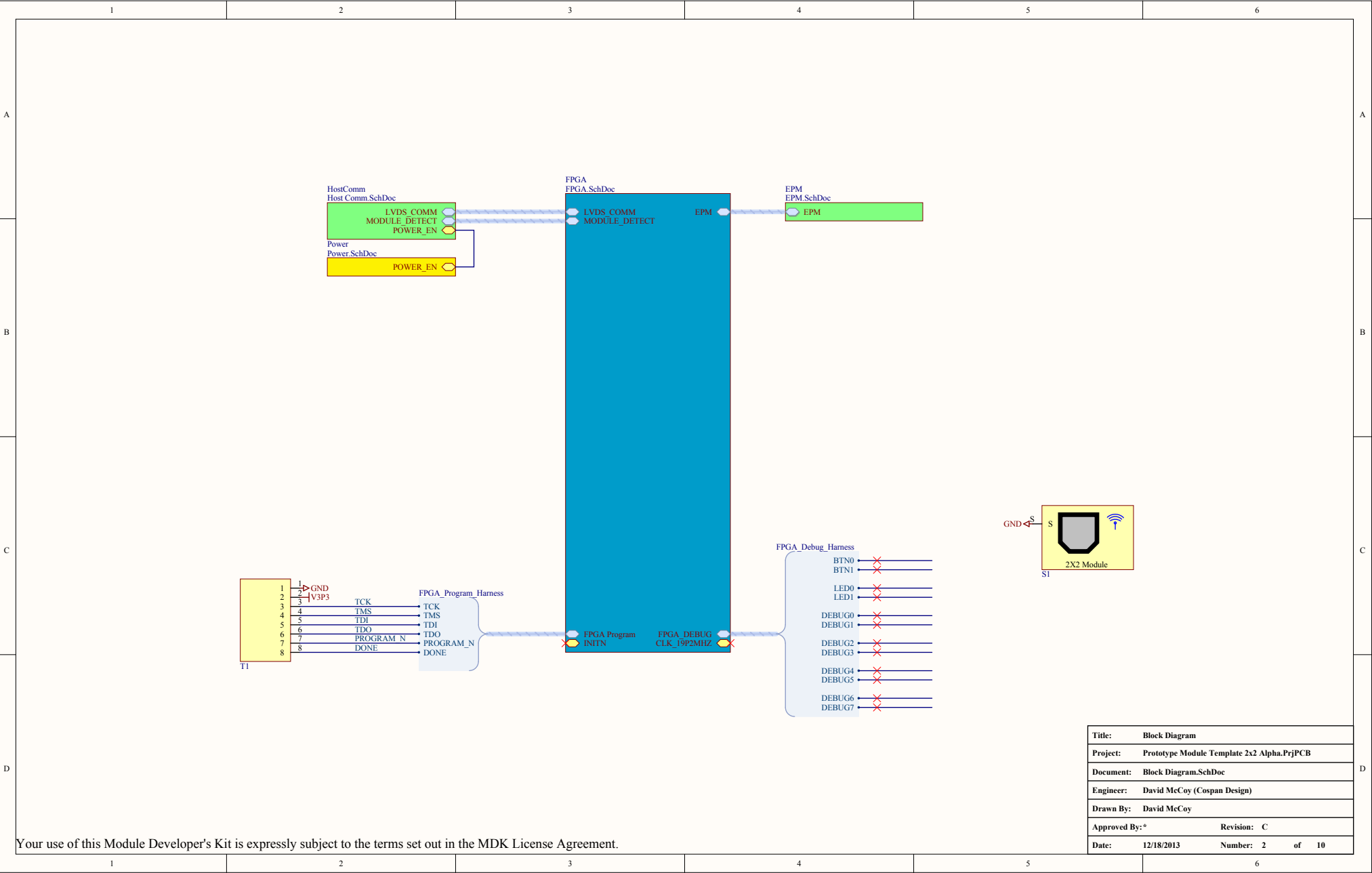


PROTOTYPE **ARA 2X2 Template Project** **Alpha**

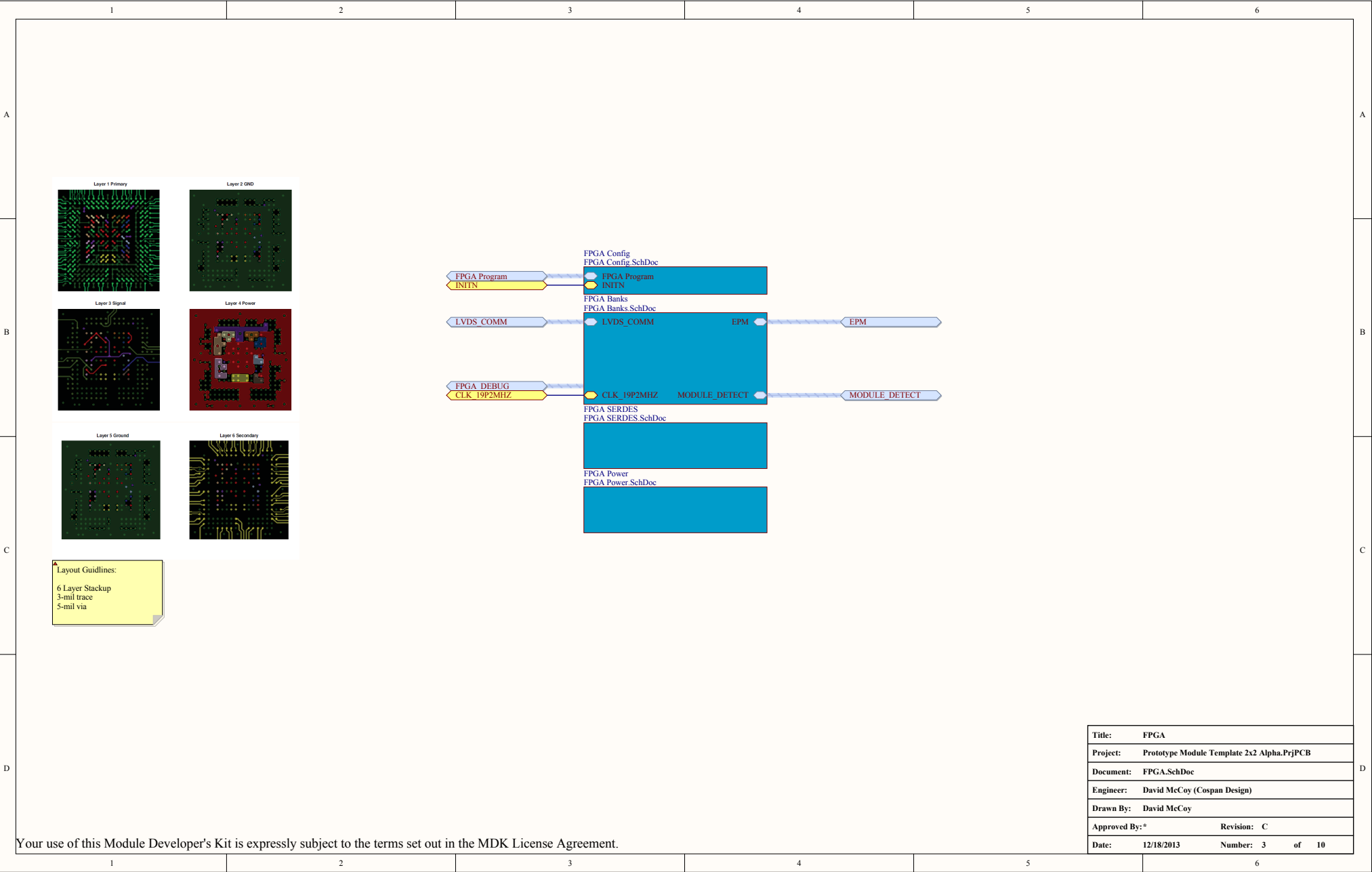
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Block Diagram
Block Diagram.SchDoc



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HOLDN: is okay to be left floating, it has an internal pull up
WRITEN: is not used in SPI Flash, does it need to be pullup externally?
CSN/SN: is okay to be left floating, it has an internal pull up
DOUT: this is only used in a daisy chain configuration and can be left unconnected

SPI Configuration I/O
CSSPIN: D17: Chip Select (Inverted)
SPID0: SPI Serial Out (MISO)
SPISL L17: SPI Serial In (MOSI)
MCLK: G19: SPI Clock
SPI Prom Size of 8Mbits
Drive SPIFASTN Low to enable faster reading from SPI Flash

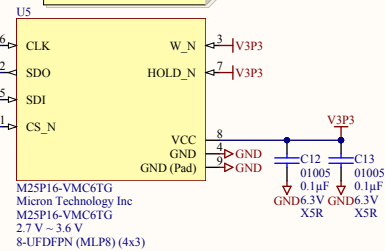
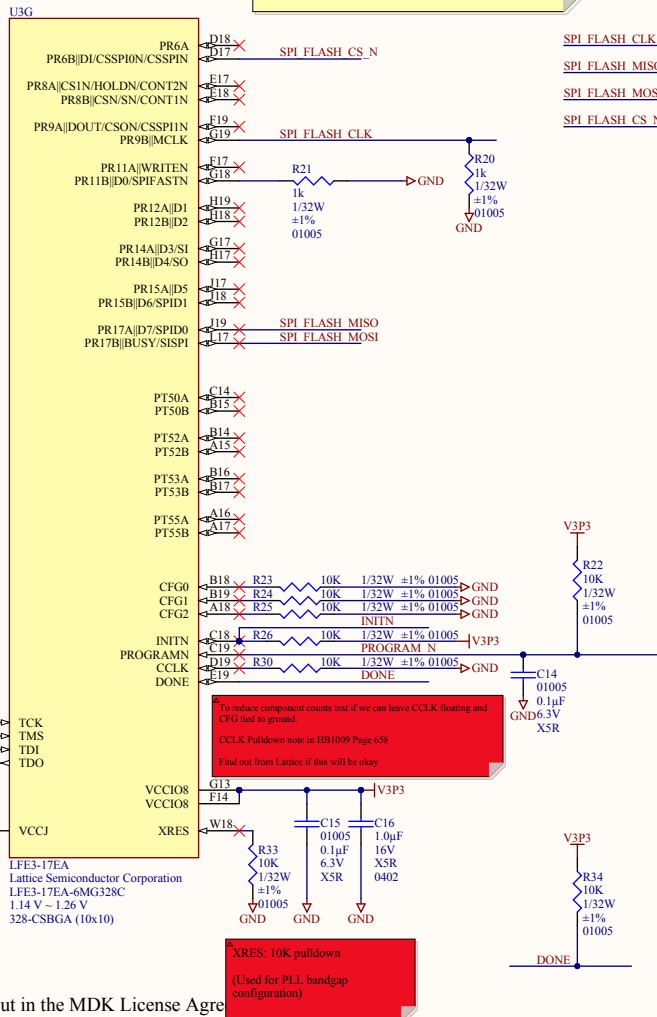
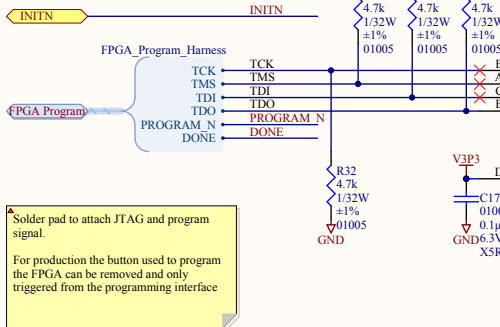
W_N Should be tied low in production designs to disallow users from modifying the FPGA bitstream

Configuration Settings:
SPI : 000: FPGA Reads configuration from a SPI Flash Device
SPIm: 010: FPGA Reads configuration from a SPI Flash Device (Multiple partitions)
SSPI: 001: FPGA is a SPI Slave that an external device such as an MCU will configure
SCM : 101: FPGA behaves as a slave in a serial configuration protocol
SPCM: 111: FPGA behaves as a slave in a parallel configuration protocol

Pull down resistor on MCLK to counteract the internal pull on the pin, this will remove unintentional rising edges at power up

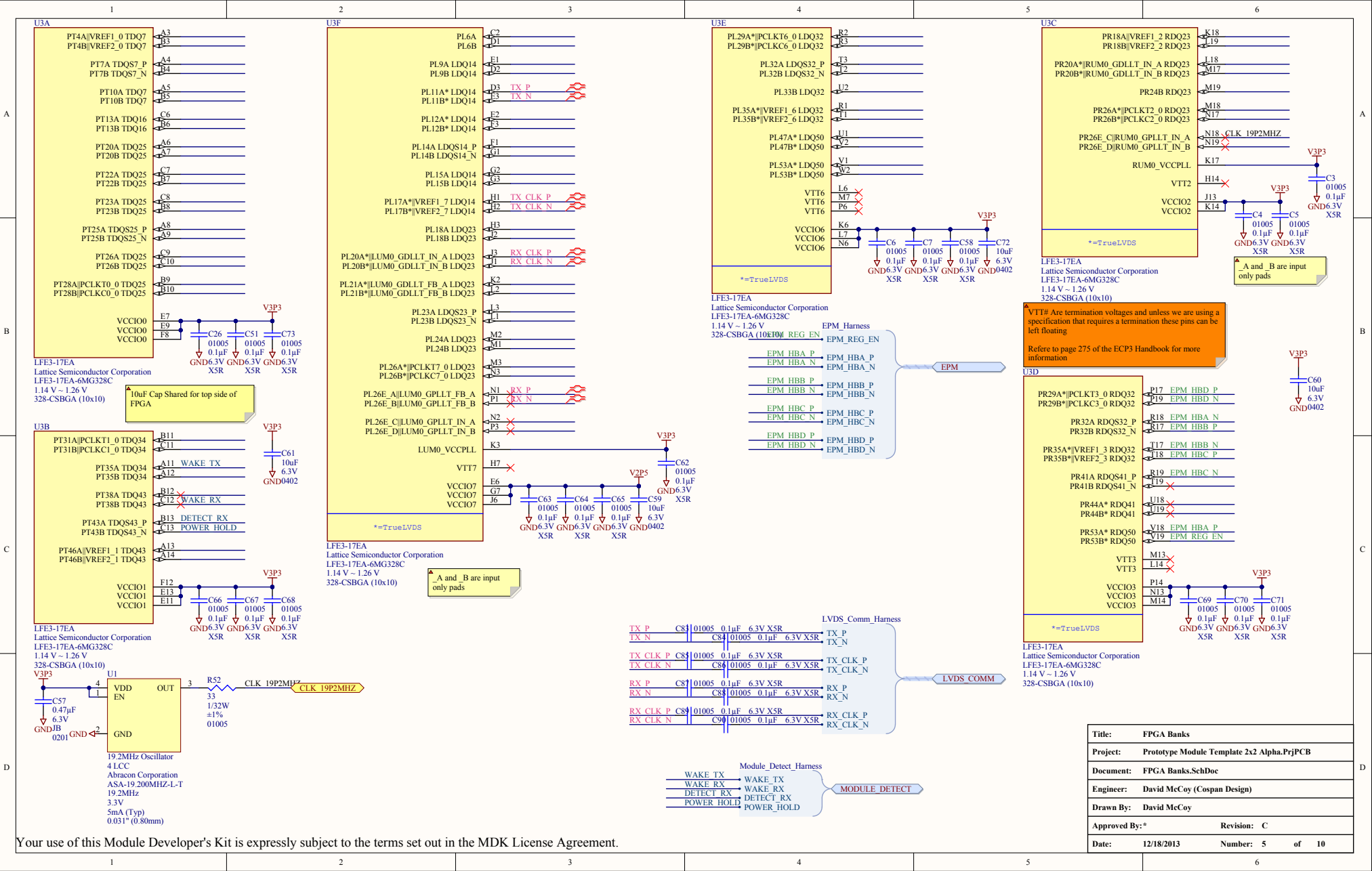
Programmers Note: The FPGA will program the SPI Flash chip use the ParallelFlashProgrammingandFPGAConfiguration pdf app note to see how

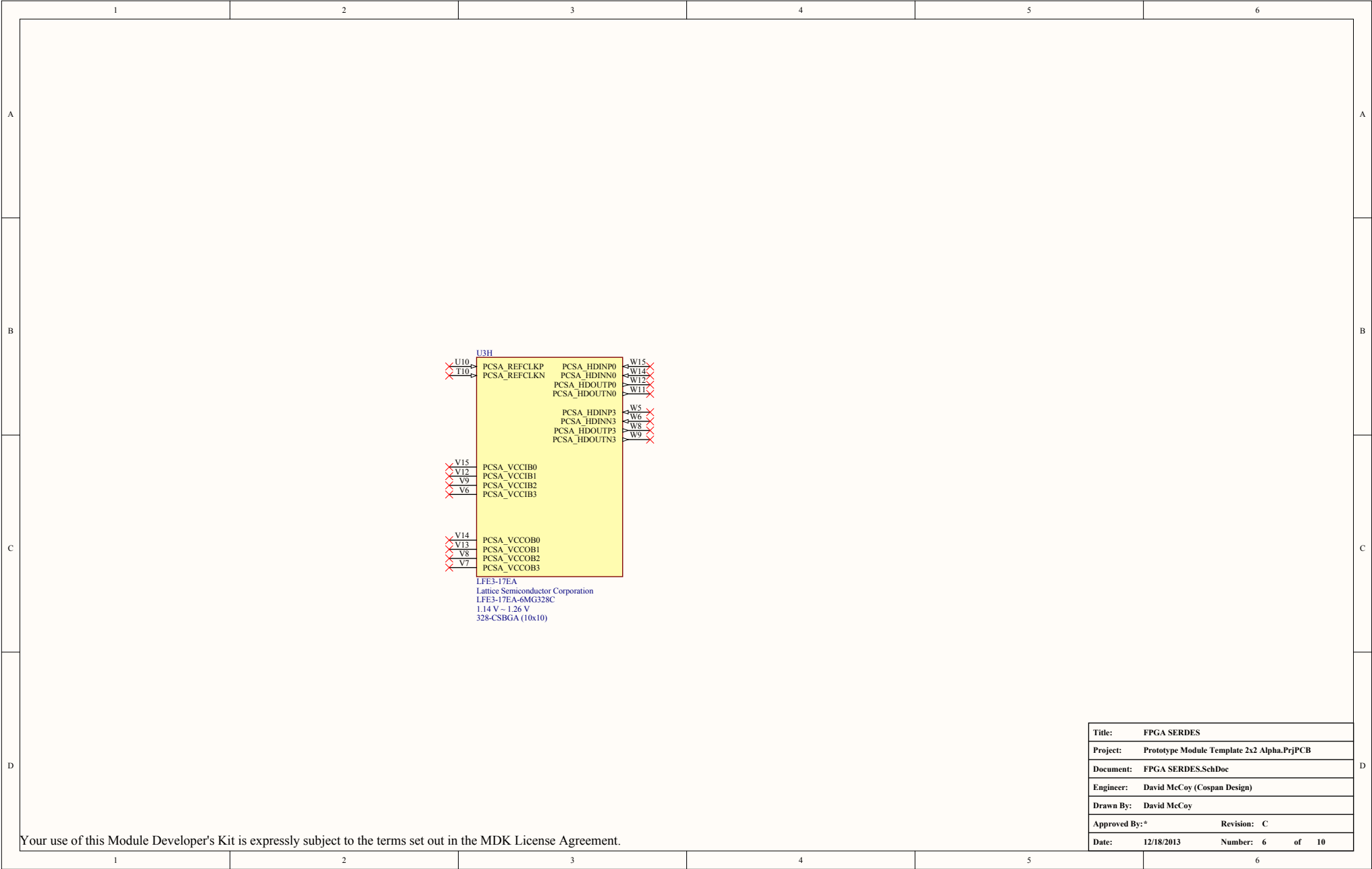
Need a via to solder on the INIT_N pin for debug, during configuration if this signal goes high there was an error. The via will not be needed in the final design



Title:	FPGA Config
Project:	Prototype Module Template 2x2 Alpha.PrjPCB
Document:	FPGA Config.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By:*	Revision: C
Date:	12/18/2013
Number:	4 of 10

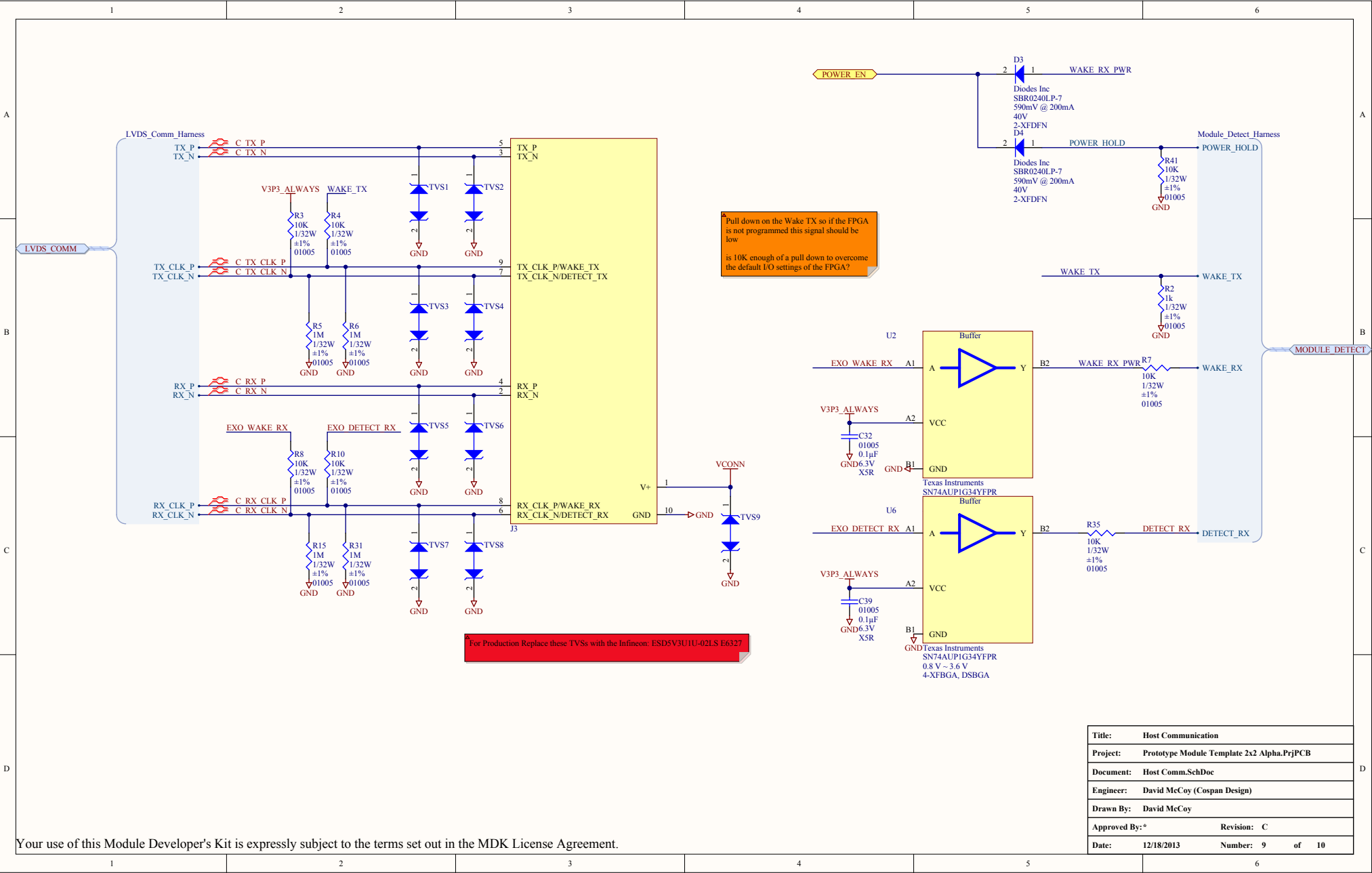
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