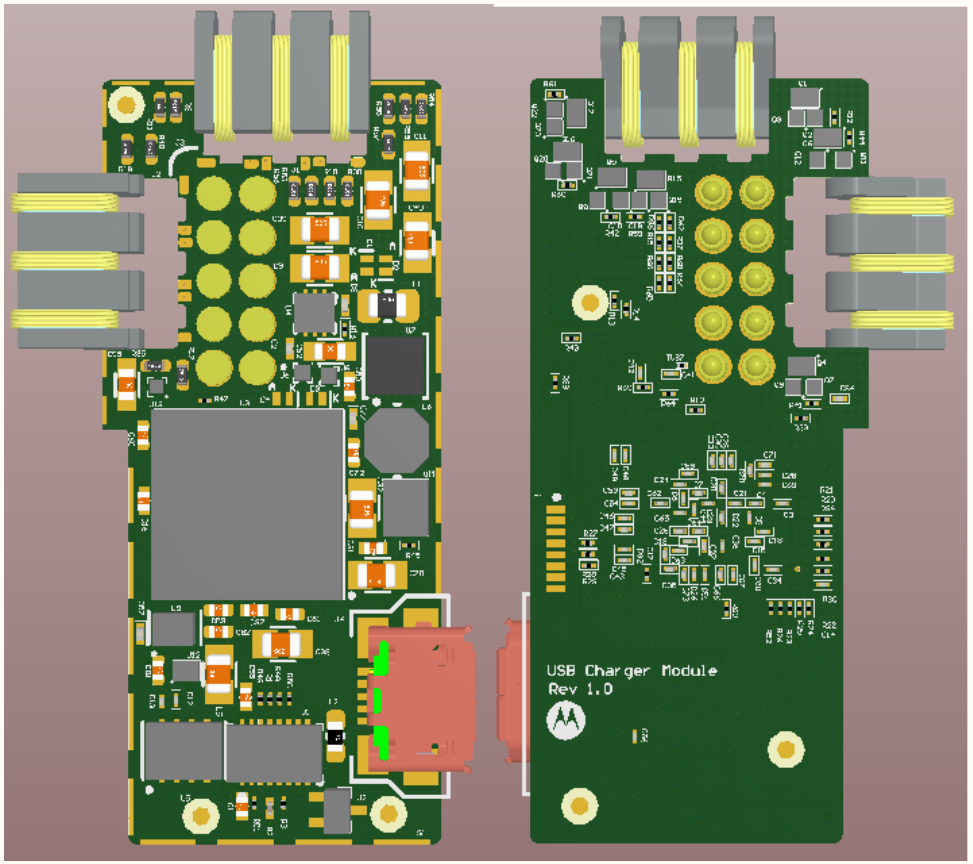
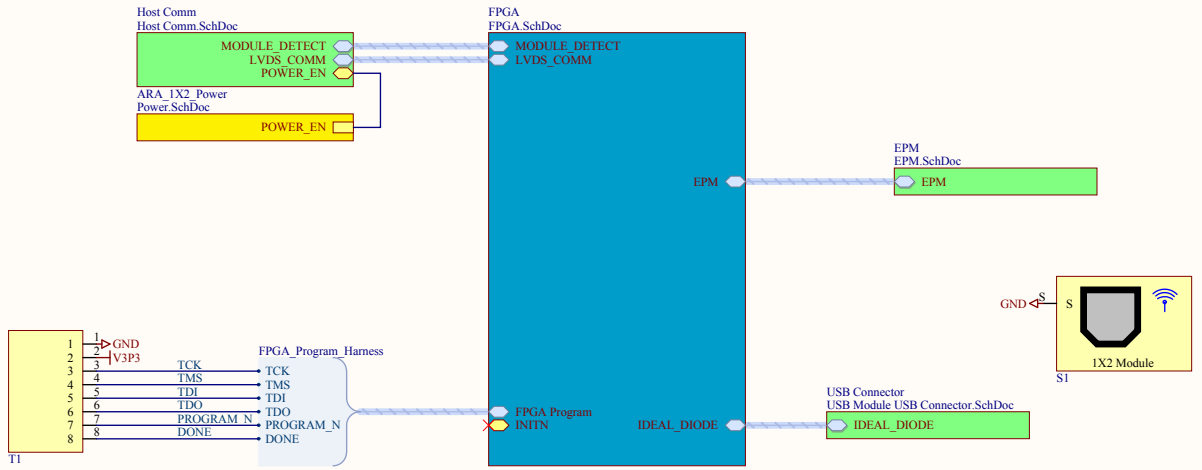
PROTOTYPE USB Charger Module Rev A

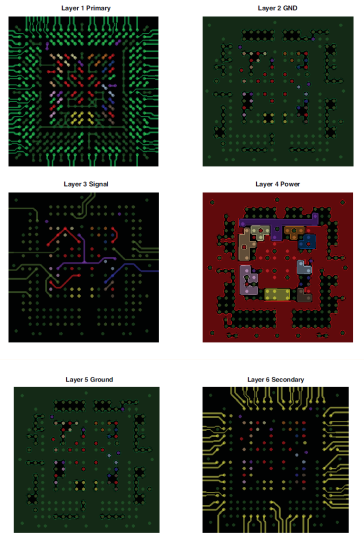
Your use of this Module Developer's Kit is expressly subject to the terms set out in the **MDK License Agreement.**



Block Diagram
Block Diagram.SchDoc

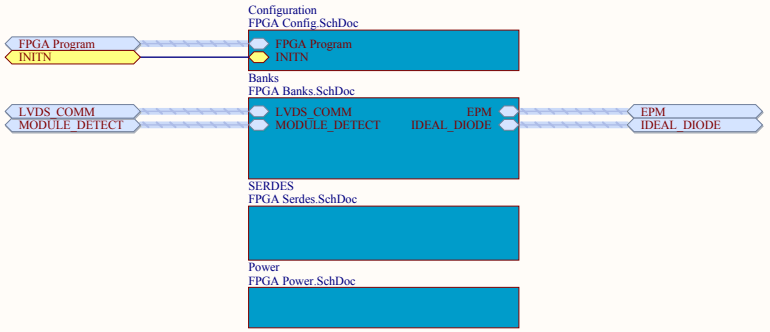


Title:	Block Diagram			
Project:	Prototype USB Charger Module 1x2 Alpha.PrjPcb			
Document:	Block Diagram.SchDoc			
Engineer:	David McCoy (Cospan Design)			
Drawn By:	David McCoy			
Approved By:	*	Revision:	A	
Date:	10/29/2013	Number:	2 of 11	



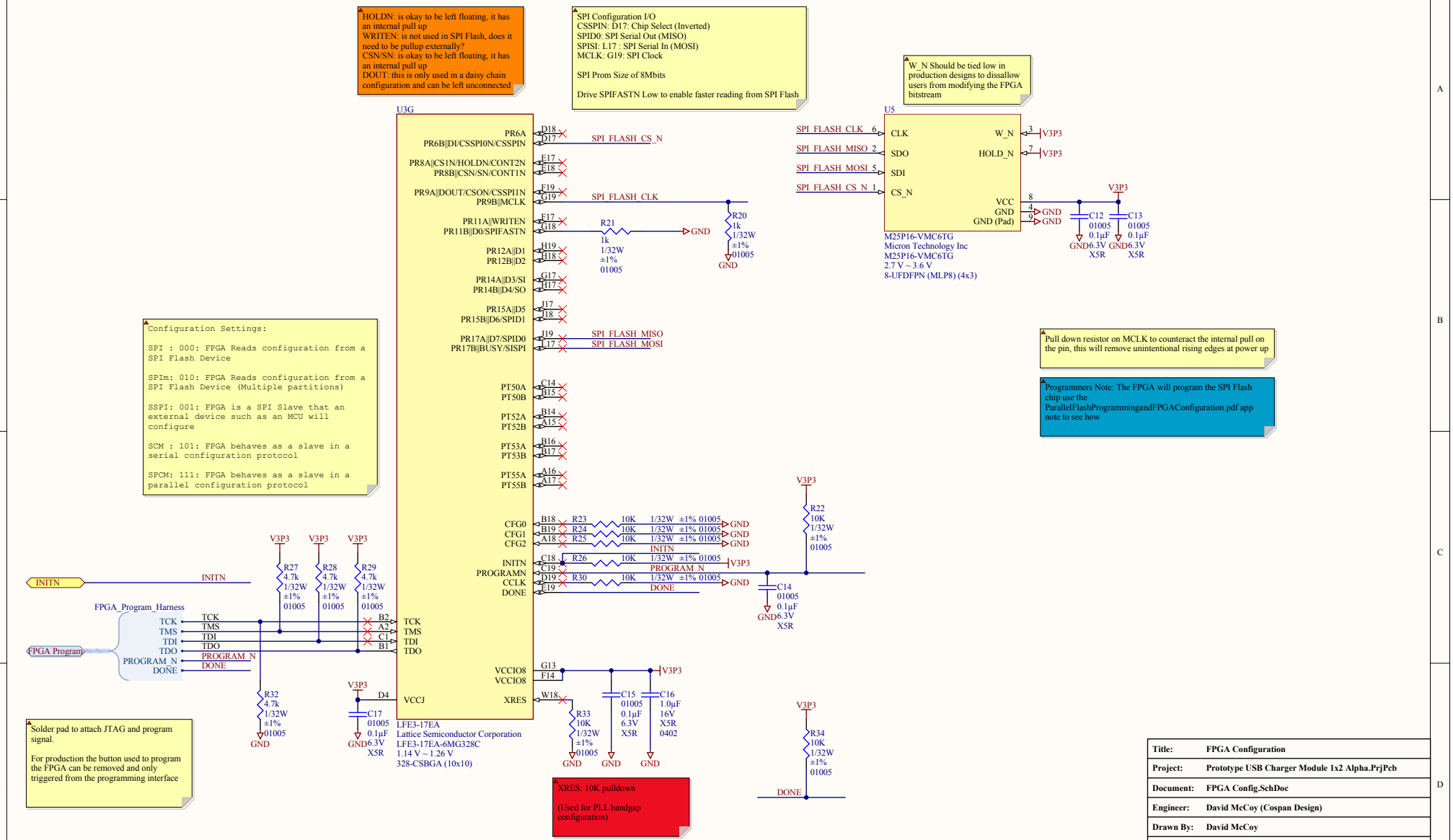
Layout Guidlines:

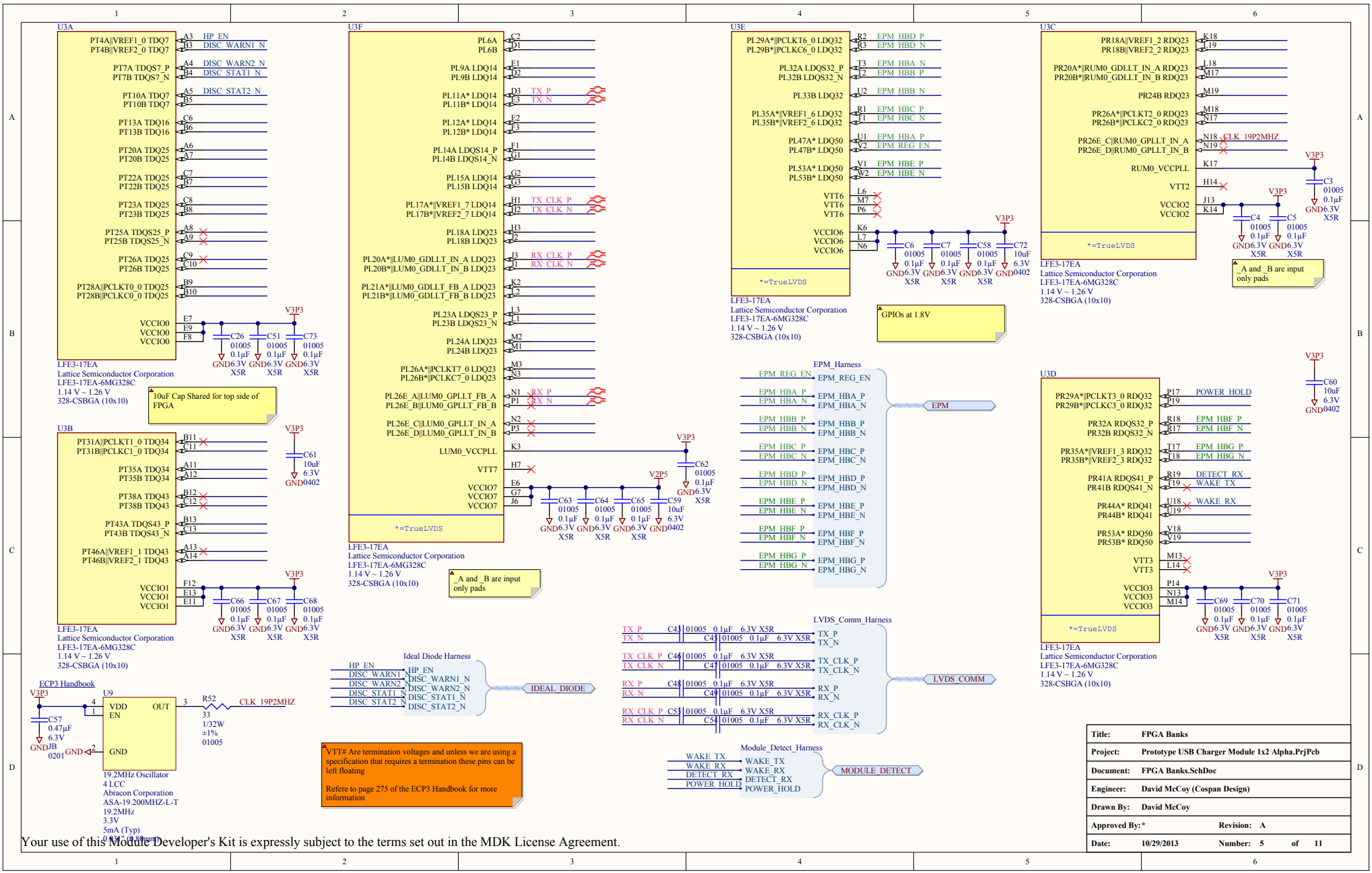
6 Layer Stackup
3-mil trace
5-mil via

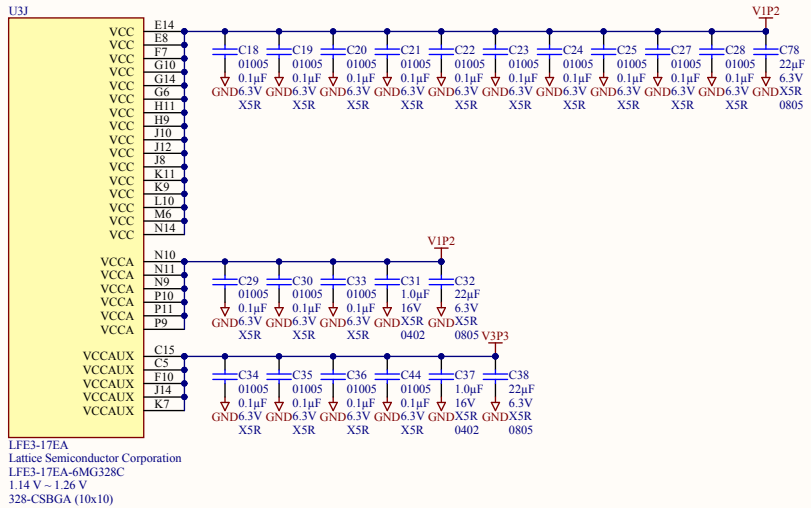


PCB Layout Recommendations

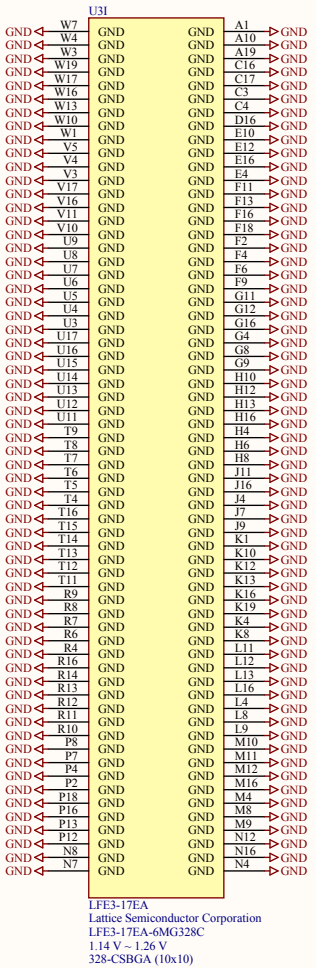
Title:	FPGA		
Project:	Prototype USB Charger Module 1x2 Alpha.PrjPcb		
Document:	FPGA.SchDoc		
Engineer:	David McCoy (Cospan Design)		
Drawn By:	David McCoy		
Approved By:	*	Revision:	A
Date:	10/29/2013	Number:	3 of 11





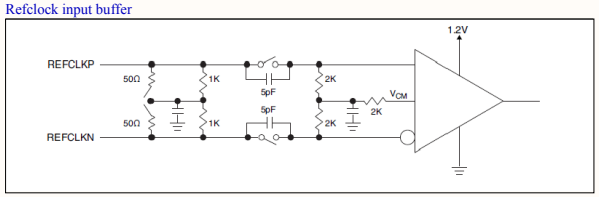


VCC: 1.2V
VCCAUX: 3.3V (Startup cannot be > 30mV/uS during power-up)
VCCA: 1.2V
VCCIB: 1.2V or 1.5V
VCCOB: 1.2V or 1.5V
VCCPLL: 3.3V
VCCIO: 1.2 - 3.3V
VCCJ: 1.2 - 3.3V
Vref: 0.5 - 1.7V
Vtt: 0.5 - 1.3V (If not used Vtt should be left floating)



Title:	FPGA Power		
Project:	Prototype USB Charger Module 1x2 Alpha.PrjPcb		
Document:	FPGA Power.SchDoc		
Engineer:	David McCoy (Cospan Design)		
Drawn By:	David McCoy		
Approved By:	*	Revision:	A
Date:	10/29/2013	Number:	6 of 11

Refclock input buffer



We only need to supply power for the BIAS resistors on the channel we are using, the other channels can be left floating

We can use chokes instead of active voltage regulator to mitigate noise for the reference termination voltages

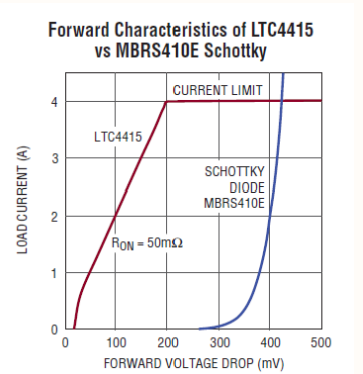
Do not use passive filters (ferrite bead) to power the VCC core for the SERDES

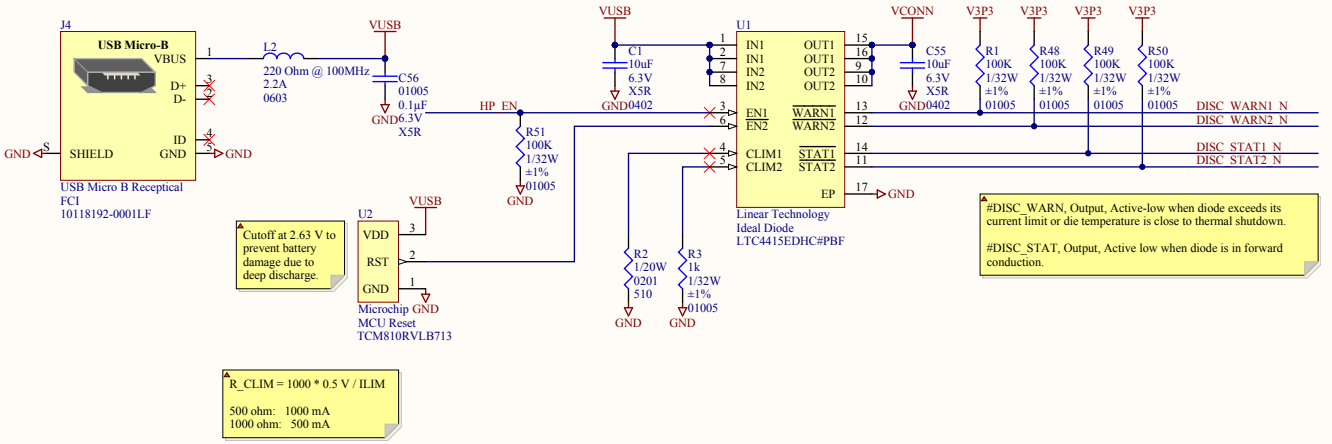
U3H

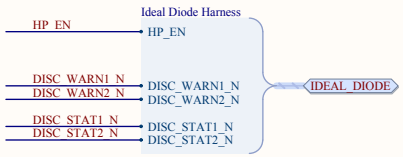
U10	PCSA_REFCLKP	PCSA_HDINP0	W15
T10	PCSA_REFCLKN	PCSA_HDINN0	W14
		PCSA_HDOUTP0	W12
		PCSA_HDOUTN0	W11
		PCSA_HDINP3	W5
		PCSA_HDINN3	W6
		PCSA_HDOUTP3	W8
		PCSA_HDOUTN3	W9
V15	PCSA_VCCIB0		
V12	PCSA_VCCIB1		
V9	PCSA_VCCIB2		
V6	PCSA_VCCIB3		
V14	PCSA_VCCOB0		
V13	PCSA_VCCOB1		
V8	PCSA_VCCOB2		
V7	PCSA_VCCOB3		

LFE3-17EA
Lattice Semiconductor Corporation
LFE3-17EA-6MG328C
1.14 V ~ 1.26 V
328-CSBGA (10x10)

Title:	FPGA SERDES				
Project:	Prototype USB Charger Module 1x2 Alpha.PrjPcb				
Document:	FPGA Serdes.SchDoc				
Engineer:	David McCoy (Cospan Design)				
Drawn By:	David McCoy				
Approved By:	*	Revision:	A		
Date:	10/29/2013	Number:	7	of	11

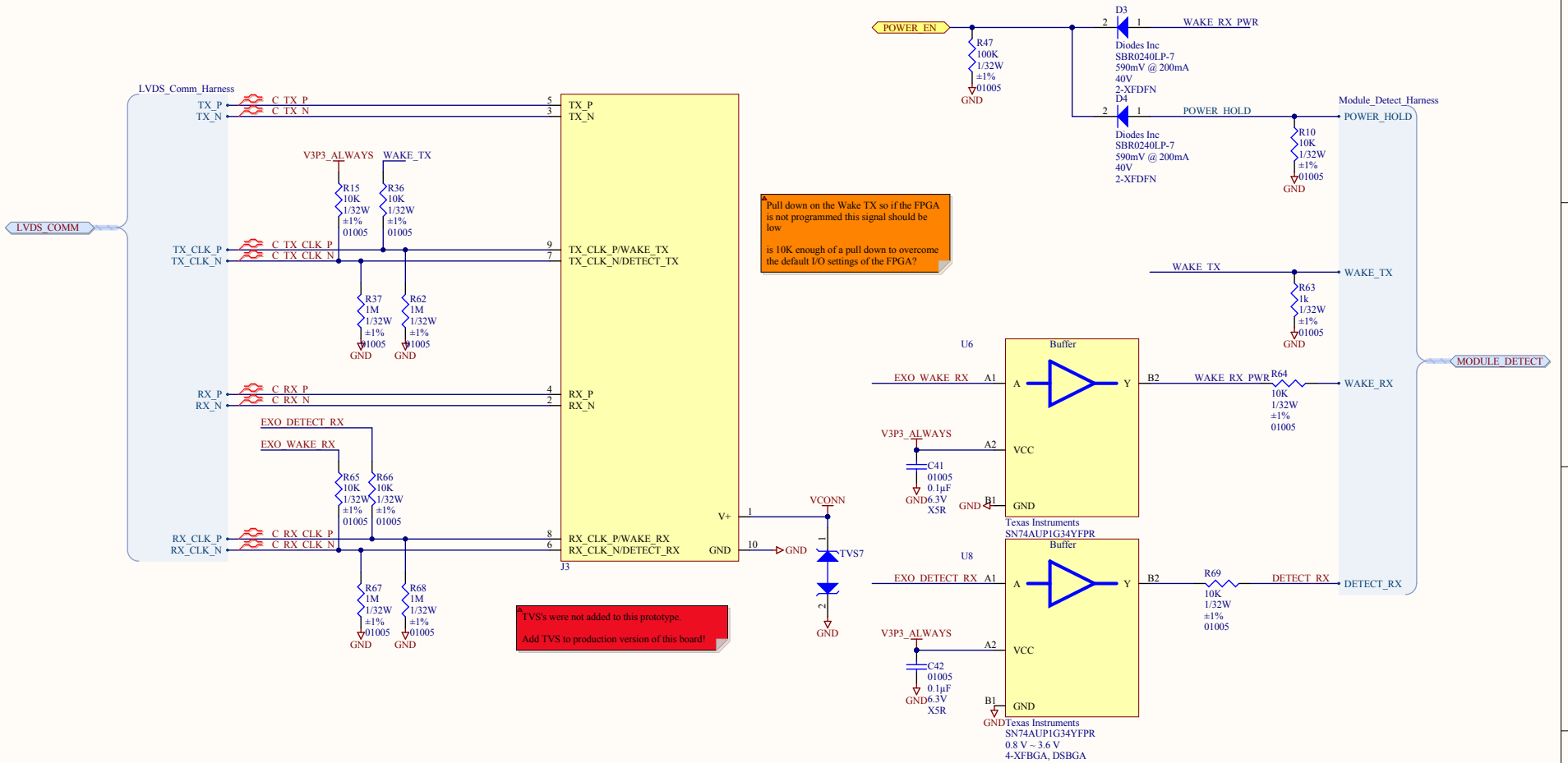




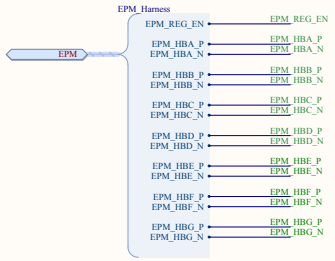


CURRENT-LIMITING DUAL IDEAL DIODE

Title:	USB
Project:	Prototype USB Charger Module 1x2 Alpha.PrjPcb
Document:	USB Module USB Connector.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By: *	Revision: A
Date: 12/18/2013	Number: 8 of 11



Title:	Host Comm			
Project:	Prototype USB Charger Module 1x2 Alpha.PrjPcb			
Document:	Host Comm.SchDoc			
Engineer:	David McCoy (Cospan Design)			
Drawn By:	David McCoy			
Approved By:	*	Revision:	A	
Date:	10/29/2013	Number:	9 of 11	



Vout = 1.255V (1 + R1/R2)
Vout = 1.255V (1 + 100K / 4.7K)
Vout = 27.9V

PFET:

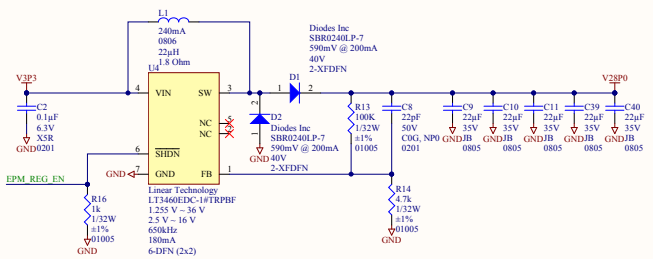
Maximum VGS: -12V

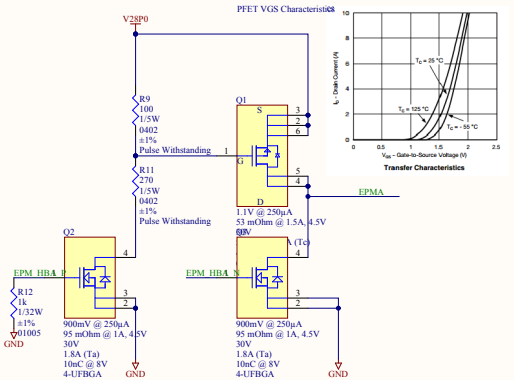
Gate 28V - 12V: 16V

For safety VGate: 20V

Resistor Divider
VGate/Vin = Rtop/Rbot+Rtop

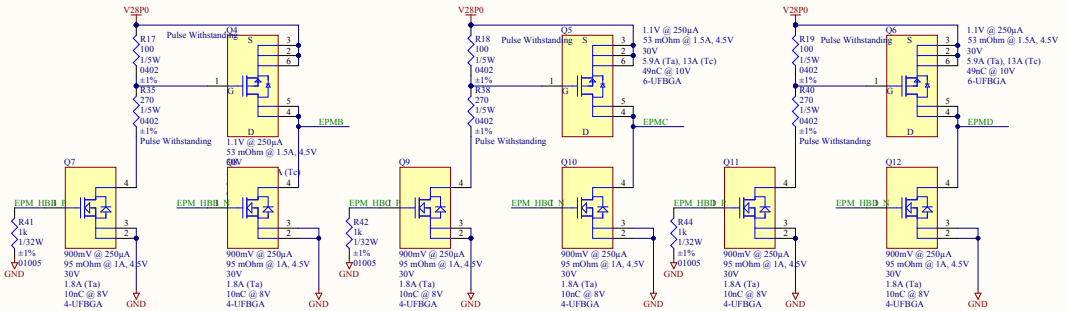
Vout = 28 * (270 / 270 + 100)
Vout = 20.48V

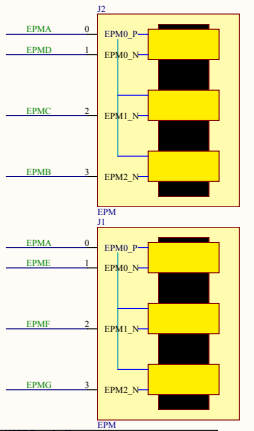


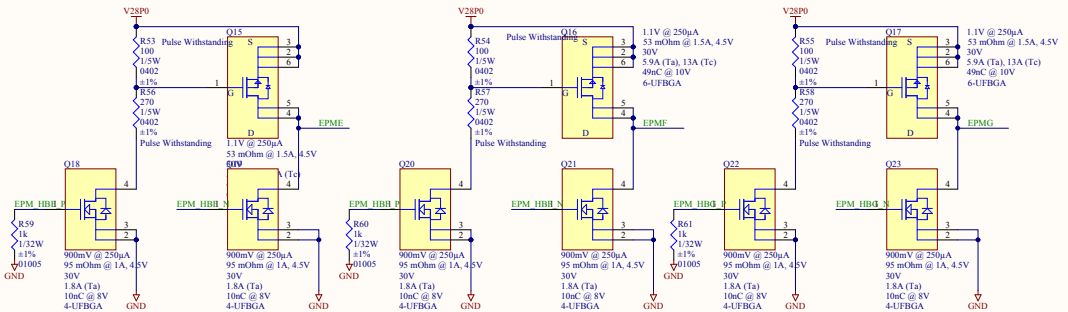


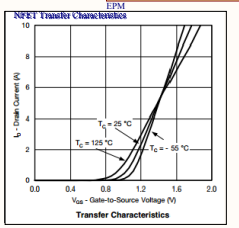
Pulse width of 300uS @ 100 mA and 28V will increase both resistors < .432 degrees (fahrenheit)

4nS turn on time for PFET
12nS turn off time for PFET

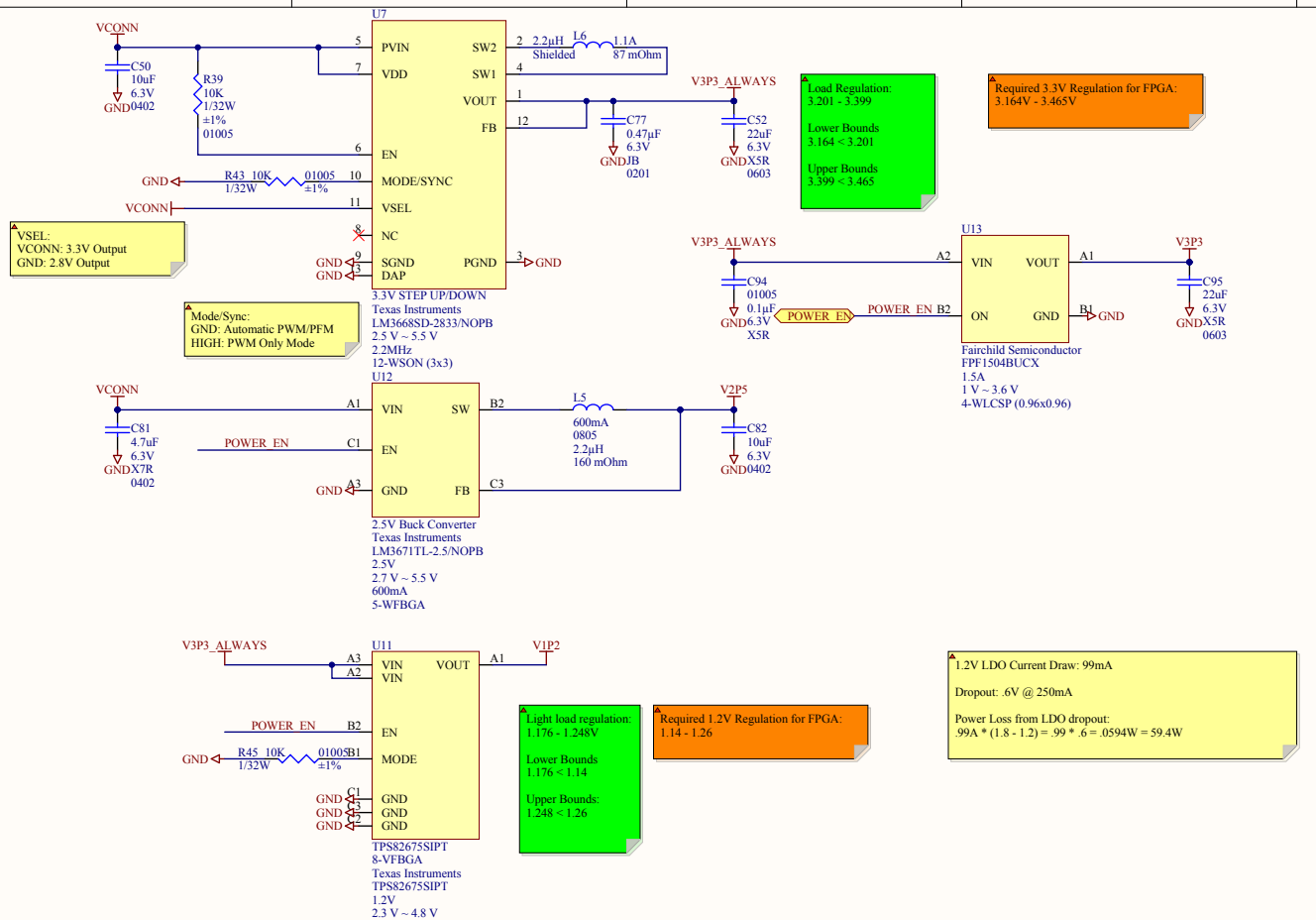








Title:	EPM
Project:	Prototype USB Charger Module 1x2 Alpha.PrjPcb
Document:	EPM.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By: *	Revision: A
Date: 10/29/2013	Number: 10 of 11



Title:	Power
Project:	Prototype USB Charger Module 1x2 Alpha.PrjPcb
Document:	Power.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By: *	Revision: A
Date: 10/29/2013	Number: 11 of 11