PROTOTYPE **Murata WIFI Module** **Rev A**

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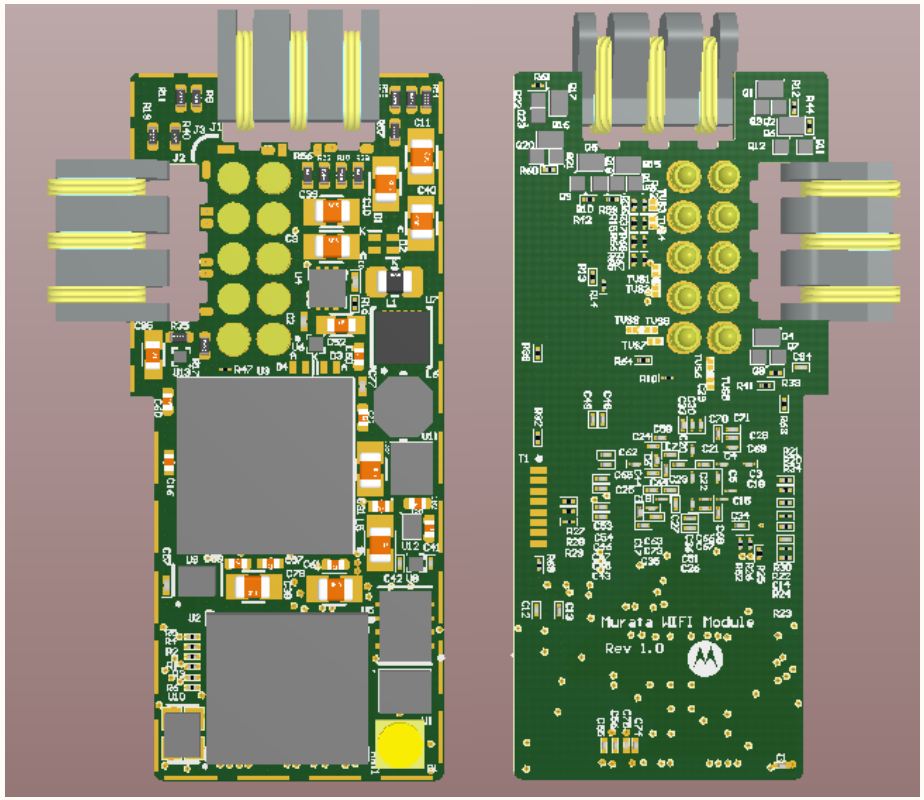
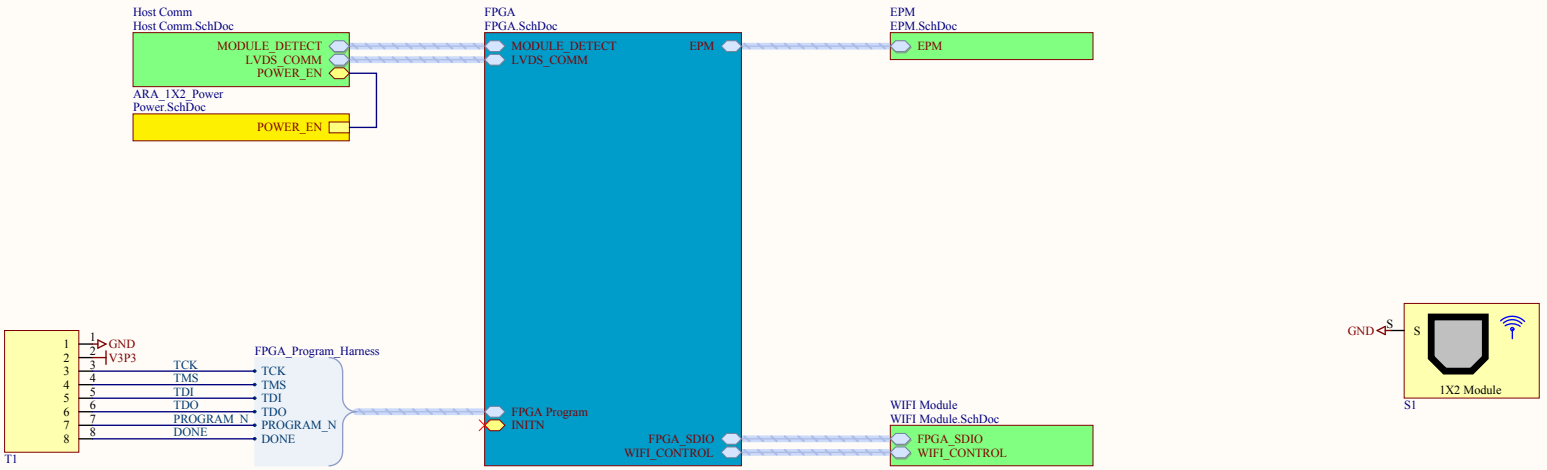
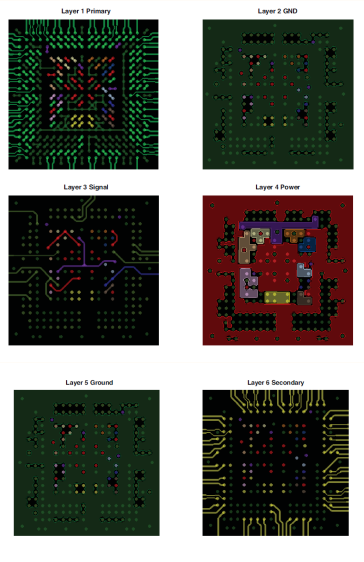
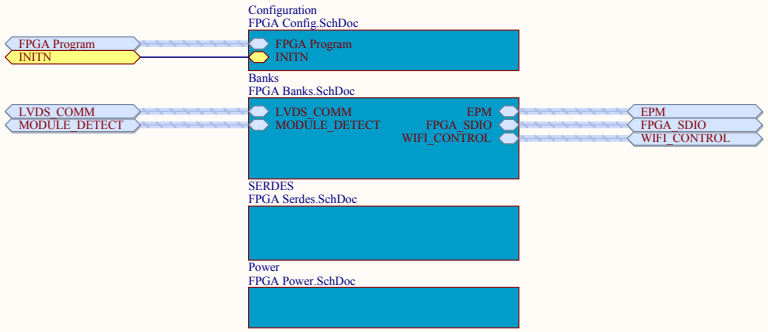


Block Diagram
Block Diagram.SchDoc



Title:	Block Diagram
Project:	Prototype Murata WIFI Module 1x2 Alpha.PrjPCB
Document:	Block Diagram.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By:	* Revision: A
Date:	10/29/2013 Number: 2 of 11



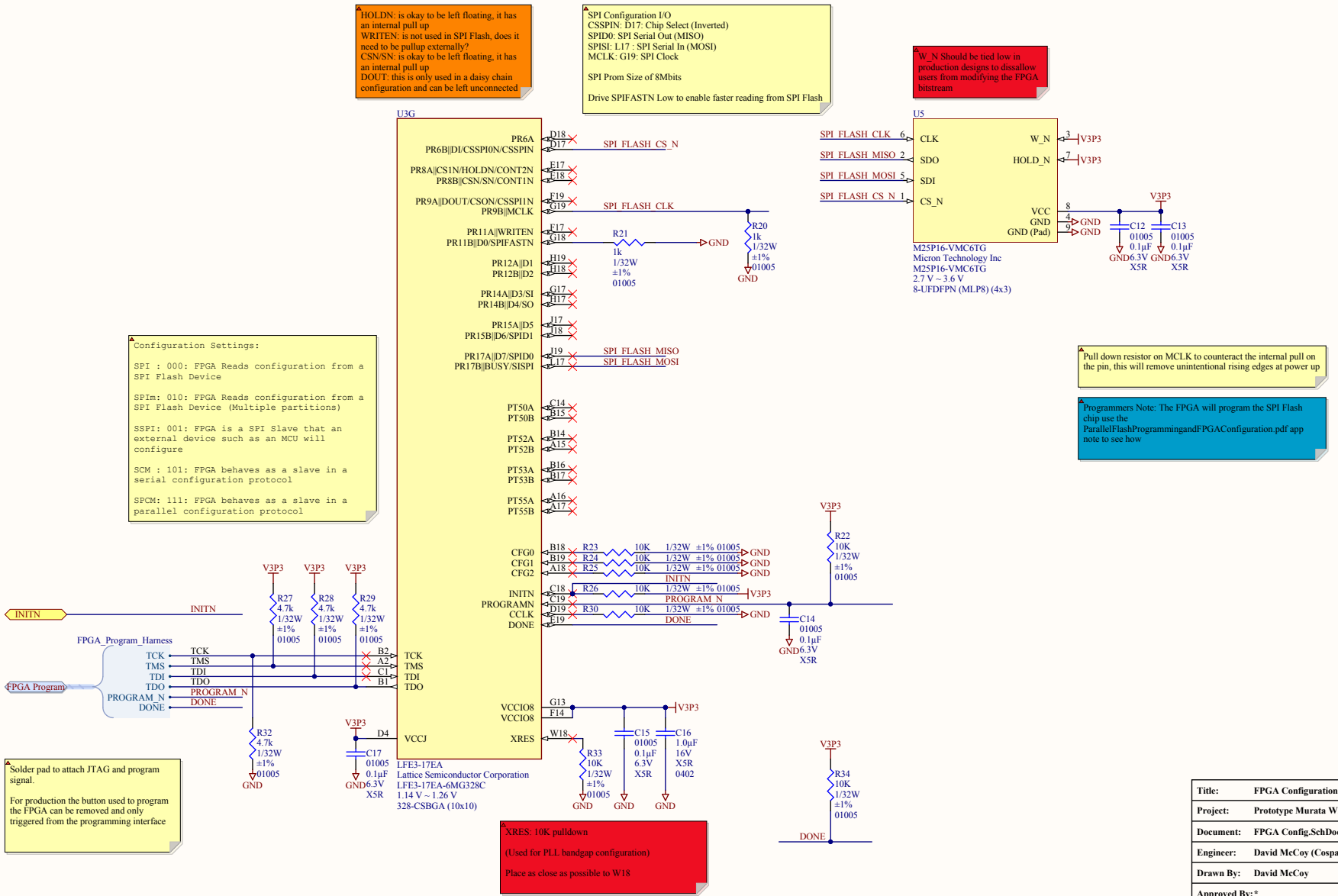


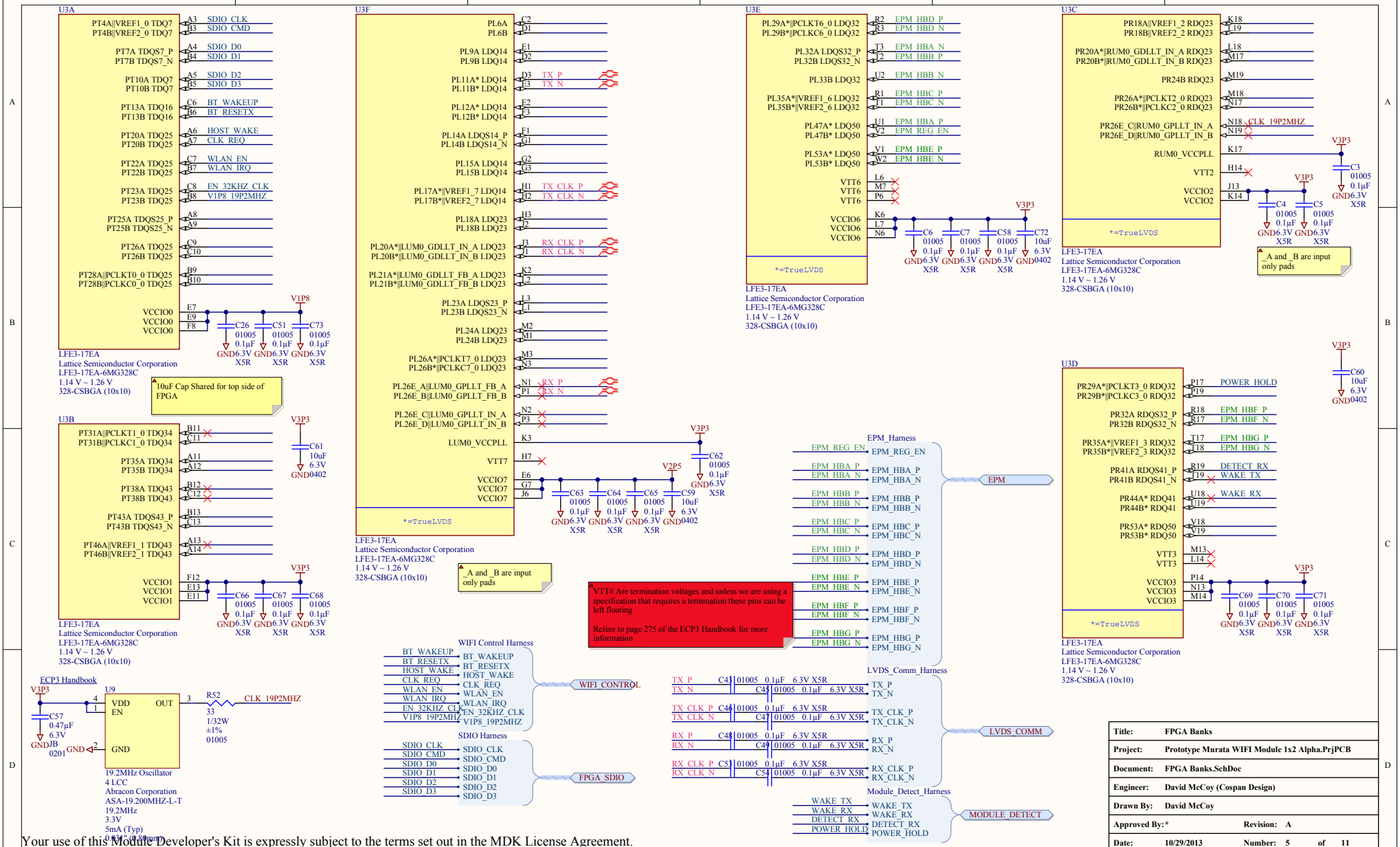
Layout Guidlines:

6 Layer Stackup
3-mil trace
5-mil via

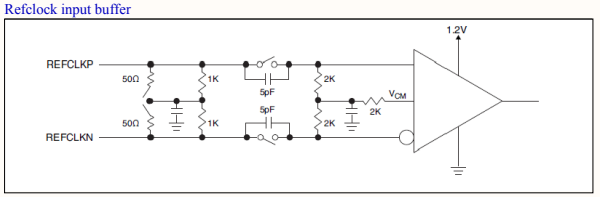
PCB Layout Recommendations

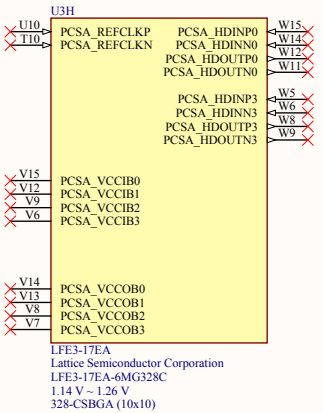
Title:	FPGA			
Project:	Prototype Murata WIFI Module 1x2 Alpha.PrjPCB			
Document:	FPGA.SchDoc			
Engineer:	David McCoy (Cospan Design)			
Drawn By:	David McCoy			
Approved By:	*	Revision:	A	
Date:	10/29/2013	Number:	3 of 11	



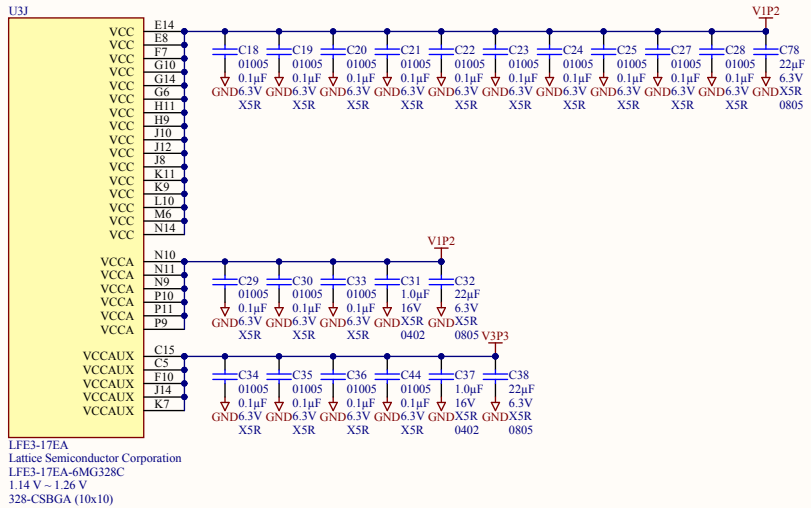

U3A
PT4A||VREF1_0 TDQ7
PT4B||VREF2_0 TDQ7
PT7A TDQS7_P
PT7B TDQS7_N
PT10A TDQ7
PT10B TDQ7
PT13A TDQ16
PT13B TDQ16
PT20A TDQ25
PT20B TDQ25
PT22A TDQ25
PT22B TDQ25
PT23A TDQ25
PT23B TDQ25
PT25A TDQS25_P
PT25B TDQS25_N
PT26A TDQ25
PT26B TDQ25
PT28A||PCLKT0_0 TDQ25
PT28B||PCLKC0_0 TDQ25
SDIO_CLK
SDIO_CMD
SDIO_D0
SDIO_D1
SDIO_D2
SDIO_D3
BT_WAKEUP
BT_RESETX
HOST_WAKE
CLK_REQ
WLAN_EN
WLAN_IRQ
EN_32KHZ_CLK
V1P8_19P2MHZ
VCCIO0
V1P8
LFE3-17EA
Lattice Semiconductor Corporation
LFE3-17EA-6MG328C
1.14 V ~ 1.26 V
328-CSBGA (10x10)
10uF Cap Shared for top side of FPGA
U3B
PT31A||PCLKT1_0 TDQ34
PT31B||PCLKC1_0 TDQ34
PT35A TDQ34
PT35B TDQ34
PT38A TDQ43
PT38B TDQ43
PT43A TDQS43_P
PT43B TDQS43_N
PT46A||VREF1_1 TDQ43
PT46B||VREF2_1 TDQ43
VCCIO1
V3P3
U3F
PL6A
PL6B
PL9A LDQ14
PL9B LDQ14
PL11A* LDQ14
PL11B* LDQ14
PL12A* LDQ14
PL12B* LDQ14
PL14A LDQS14_P
PL14B LDQS14_N
PL15A LDQ14
PL15B LDQ14
PL17A*||VREF1_7 LDQ14
PL17B*||VREF2_7 LDQ14
PL18A LDQ23
PL18B LDQ23
PL20A*||LUM0_GDLLT_IN_A LDQ23
PL20B*||LUM0_GDLLT_IN_B LDQ23
PL21A*||LUM0_GDLLT_FB_A LDQ23
PL21B*||LUM0_GDLLT_FB_B LDQ23
PL23A LDQS23_P
PL23B LDQS23_N
PL24A LDQ23
PL24B LDQ23
PL26A*||PCLKT7_0 LDQ23
PL26B*||PCLKC7_0 LDQ23
PL26E_A||LUM0_GPLLT_FB_A
PL26E_B||LUM0_GPLLT_FB_B
PL26E_C||LUM0_GPLLT_IN_A
PL26E_D||LUM0_GPLLT_IN_B
LUM0_VCCPLL
VTT7
VCCIO7
V2P5
TX_P
TX_N
TX_CLK_P
TX_CLK_N
RX_CLK_P
RX_CLK_N
RX_P
RX_N
*=TrueLVDS
A and _B are input only pads
U3E
PL29A*||PCLKT6_0 LDQ32
PL29B*||PCLKC6_0 LDQ32
PL32A LDQS32_P
PL32B LDQS32_N
PL33B LDQ32
PL35A*||VREF1_6 LDQ32
PL35B*||VREF2_6 LDQ32
PL47A* LDQ50
PL47B* LDQ50
PL53A* LDQ50
PL53B* LDQ50
VTT6
VCCIO6
EPM_HBD_P
EPM_HBD_N
EPM_HBA_N
EPM_HBB_P
EPM_HBB_N
EPM_HBC_P
EPM_HBC_N
EPM_HBA_P
EPM_REG_EN
U3C
PR18A||VREF1_2 RDQ23
PR18B||VREF2_2 RDQ23
PR20A*||RUM0_GDLLT_IN_A RDQ23
PR20B*||RUM0_GDLLT_IN_B RDQ23
PR24B RDQ23
PR26A*||PCLKT2_0 RDQ23
PR26B*||PCLKC2_0 RDQ23
PR26E_C||RUM0_GPLLT_IN_A
PR26E_D||RUM0_GPLLT_IN_B
RUM0_VCCPLL
VTT2
VCCIO2
CLK_19P2MHZ
U3D
PR29A*||PCLKT3_0 RDQ32
PR29B*||PCLKC3_0 RDQ32
PR32A RDQS32_P
PR32B RDQS32_N
PR35A*||VREF1_3 RDQ32
PR35B*||VREF2_3 RDQ32
PR41A RDQS41_P
PR41B RDQS41_N
PR44A* RDQ41
PR44B* RDQ41
PR53A* RDQ50
PR53B* RDQ50
VTT3
VCCIO3
POWER_HOLD
EPM_HBF_P
EPM_HBF_N
EPM_HBG_P
EPM_HBG_N
DETECT_RX
WAKE_TX
WAKE_RX
_A and _B are input only pads
VTT# Are termination voltages and unless we are using a specification that requires a termination these pins can be left floating
Refere to page 275 of the ECP3 Handbook for more information
EPM_Harness
EPM
LVDS_Comm_Harness
LVDS_COMM
WIFI Control Harness
WIFI_CONTROL
SDIO Harness
FPGA_SDIO
Module_Detect_Harness
MODULE_DETECT
ECP3 Handbook
U9
VDD
EN
OUT
GND
R52
33
1/32W
±1%
01005
CLK_19P2MHZ
19.2MHz Oscillator
4 LCC
Abracon Corporation
ASA-19.200MHZ-L-T
19.2MHz
3.3V
5mA (Typ)
0.01uF (Optional)
Your use of this Module Developer's Kit is expressly subject to the terms set out in the MDK License Agreement.
Title: FPGA Banks
Project: Prototype Murata WIFI Module 1x2 Alpha.PrjPCB
Document: FPGA Banks.SchDoc
Engineer: David McCoy (Cospan Design)
Drawn By: David McCoy
Approved By:* Revision: A
Date: 10/29/2013 Number: 5 of 11

Refclock input buffer

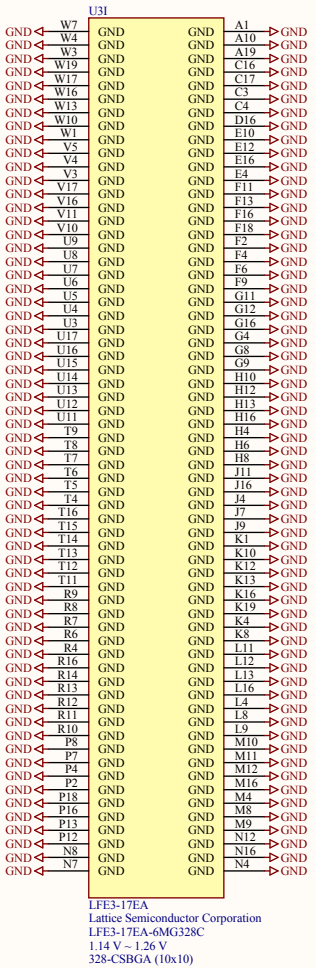




Title:	FPGA SERDES
Project:	Prototype Murata WIFI Module 1x2 Alpha.PrjPCB
Document:	FPGA Serdes.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By:	* Revision: A
Date:	10/29/2013 Number: 6 of 11



VCC: 1.2V
VCCAUX: 3.3V (Startup cannot be > 30mV/uS during power-up)
VCCA: 1.2V
VCCIB: 1.2V or 1.5V
VCCOB: 1.2V or 1.5V
VCCPLL: 3.3V
VCCIO: 1.2 - 3.3V
VCCJ: 1.2 - 3.3V
Vref: 0.5 - 1.7V
Vtt: 0.5 - 1.3V (If not used Vtt should be left floating)



Title:	FPGA Power		
Project:	Prototype Murata WIFI Module 1x2 Alpha.PrjPCB		
Document:	FPGA Power.SchDoc		
Engineer:	David McCoy (Cospan Design)		
Drawn By:	David McCoy		
Approved By:	*	Revision:	A
Date:	10/29/2013	Number:	7 of 11

SDIO Harness

FPGA_SDIO

SDIO_CLK
SDIO_CMD
SDIO_D0
SDIO_D1
SDIO_D2
SDIO_D3

R1 33 1/32W ±1% 01005 — WIFI_SDIO_CLK 19
R2 33 1/32W ±1% 01005 — WIFI_SDIO_CMD 18
R3 33 1/32W ±1% 01005 — WIFI_SDIO_D0 20
R4 33 1/32W ±1% 01005 — WIFI_SDIO_D1 17
R5 33 1/32W ±1% 01005 — WIFI_SDIO_D2 16
R6 33 1/32W ±1% 01005 — WIFI_SDIO_D3 21

U2A

COMM/WIFI/BT/FM

SDIO_CLK
SDIO_CMD
SDIO_D0
SDIO_D1
SDIO_D2
SDIO_D3
2.4G_ANT 49

ANT1
SIG 1
GND 2
GND 3
GND 4

Ultra Miniature Coaxial
Ultra Miniature Coaxial
50 Ohm
Snap-On

UART_CTS 43
UART_RTS 44
UART_RX 46
UART_TX 45

FM_I2S_CLK/PCM_CLK 52
FM_I2S_FSYNC/PCM_FSYNC 50
FM_I2S_DI/PCM_IN 48
FM_I2S_DO/PCM_OUT 47

No Signals are Allowed on the IO pins if no IO power supplied because the IOs are not 'fail safe', exceptions are CLK_REQ_OUT, SLOWCLK, XTALP and AUD_xxx

WIFI Control Harness

WIFI_CONTROL

BT_WAKEUP
BT_RESETX
HOST_WAKE
CLK_REQ
WLAN_EN
WLAN_IRQ
EN_32KHZ_CLK
V1P8_19P2MHZ

BT_WAKEUP 33
BT_RESETX 5
HOST_WAKE 3
CLK_REQ 4
WLAN_EN 14
WLAN_IRQ 6

1V8_PRE_REG 39
VDD_LDO_IN_CLASS1P5 40

V1P8
C1 01005 0.1µF GND 6.3V X5R

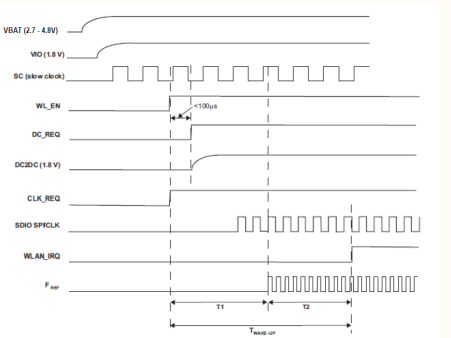
U10
VCC 4
OUTPUT 3
GND 2
EOH 1

32.768kHz
Pericom
KX2513G0032.768000
1.8V

32KHZ_CLK — SLEEP_CLK 23
V1P8_19P2MHZ — XTALP 35 / XTALM 36
GND — XTALP 35

SLEEP_CLK
WL_UART_DBG 66
BT_UART_DBG 69
XTALP
XTALM
WL_RS232_TX 12
WL_RS232_RX 13

Murata
LBEH59XUHC-TEMP



U2B

POWER

V3P3
C55 01005 0.1µF GND 6.3V X5R
C56 01005 0.1µF GND 6.3V X5R

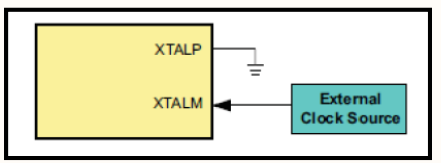
VBAT 41
VIO 38

V1P8
C74 01005 0.1µF GND 6.3V X5R
C75 01005 0.1µF GND 6.3V X5R

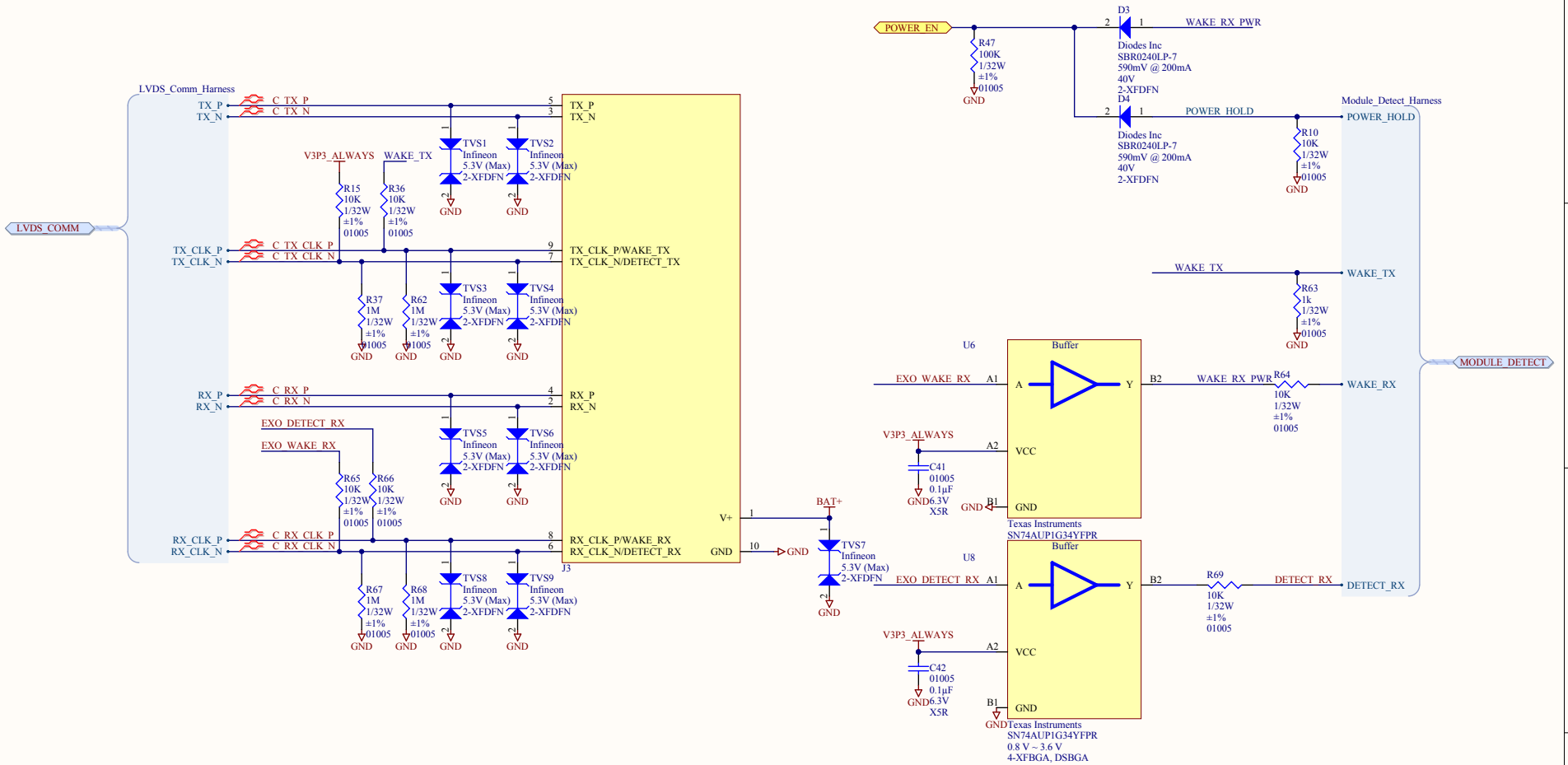
GND 7, 15, 22, 24, 26, 27, 28, 29, 30, 31, 32, 34, 37, 42, 45, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 70

NC 8, 10, 11, 53, 67, 68

Murata
LBEH59XUHC-TEMP



Title:	WIFI Module		
Project:	Prototype Murata WIFI Module 1x2 Alpha.PrjPCB		
Document:	WIFI Module.SchDoc		
Engineer:	David McCoy (Cospan Design)		
Drawn By:	David McCoy		
Approved By:	*	Revision:	A
Date:	3/12/2014	Number:	8 of 11



Title:	Host Comm				
Project:	Prototype Murata WIFI Module 1x2 Alpha.PrjPCB				
Document:	Host Comm.SchDoc				
Engineer:	David McCoy (Cospan Design)				
Drawn By:	David McCoy				
Approved By:	*	Revision:	A		
Date:	10/29/2013	Number:	9	of	11

EPM_Harness

EPM_REG_EN
EPM_HBA_P
EPM_HBA_N
EPM_HBB_P
EPM_HBB_N
EPM_HBC_P
EPM_HBC_N
EPM_HBD_P
EPM_HBD_N
EPM_HBE_P
EPM_HBE_N
EPM_HBF_P
EPM_HBF_N
EPM_HBG_P
EPM_HBG_N

EPM

Vout = 1.255V (1 + R1/R2)
Vout = 1.255V (1 + 100K / 4.7K)
Vout = 27.9V

PFET:

Maximum VGS: -12V

Gate 28V - 12V: 16V

For safety VGate: 20V

Resistor Divider
VGate/Vin = Rtop/Rbot+Rtop

Vout = 28 * (270 / 270 + 100)
Vout = 20.48V

L1
240mA
0806
22µH
1.8 Ohm

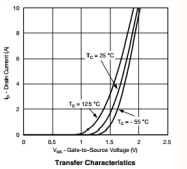
U4
Linear Technology
LT3460EDC-1#TRPBF
1.255 V – 36 V
2.5 V – 16 V
650kHz
180mA
6-DFN (2x2)

D1
D2
Diodes Inc
SBR0240LP-7
590mV @ 200mA
40V
2-XFDFN

V3P3
V28P0
EPM_REG_EN
GND

C2 0.1µF 6.3V X5R 0201
R16 1k 1/32W ±1% 01005
R13 100K 1/32W ±1% 01005
R14 4.7k 1/32W ±1% 01005
C8 22pF 50V C0G, NP0 0201
C9 22pF 35V JB 0805
C10 22pF 35V JB 0805
C11 22pF 35V JB 0805
C39 22pF 35V JB 0805
C40 22pF 35V JB 0805

PFET VGS Characteristics



V28P0
R9 100 1/5W 0402 ±1% Pulse Withstanding
R11 270 1/5W 0402 ±1% Pulse Withstanding
Q1 Q2
1.1V @ 250µA
53 mOhm @ 1.5A, 4.5V
60V
5.9A (Ta), 13A (Tc)
49nC @ 10V
6-UFBGA
EPMA
EPM_HBA_P
EPM_HBA_N
R12 1k 1/32W ±1% 01005
900mV @ 250µA
95 mOhm @ 1A, 4.5V
30V
1.8A (Ta)
10nC @ 8V
4-UFBGA
GND

Pulse width of 300uS @ 100 mA and 28V will increase both resistors < .432 degrees (fahrenheit)

4nS turn on time for PFET
12nS turn off time for PFET

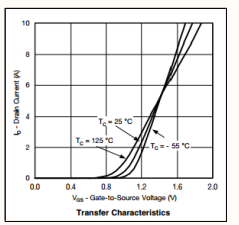
J2
EPMA 0
EPMD 1
EPMC 2
EPMB 3
EPM0_P
EPM0_N
EPM1_N
EPM2_N
EPM

J1
EPMA 0
EPME 1
EPMF 2
EPMG 3
EPM0_P
EPM0_N
EPM1_N
EPM2_N
EPM

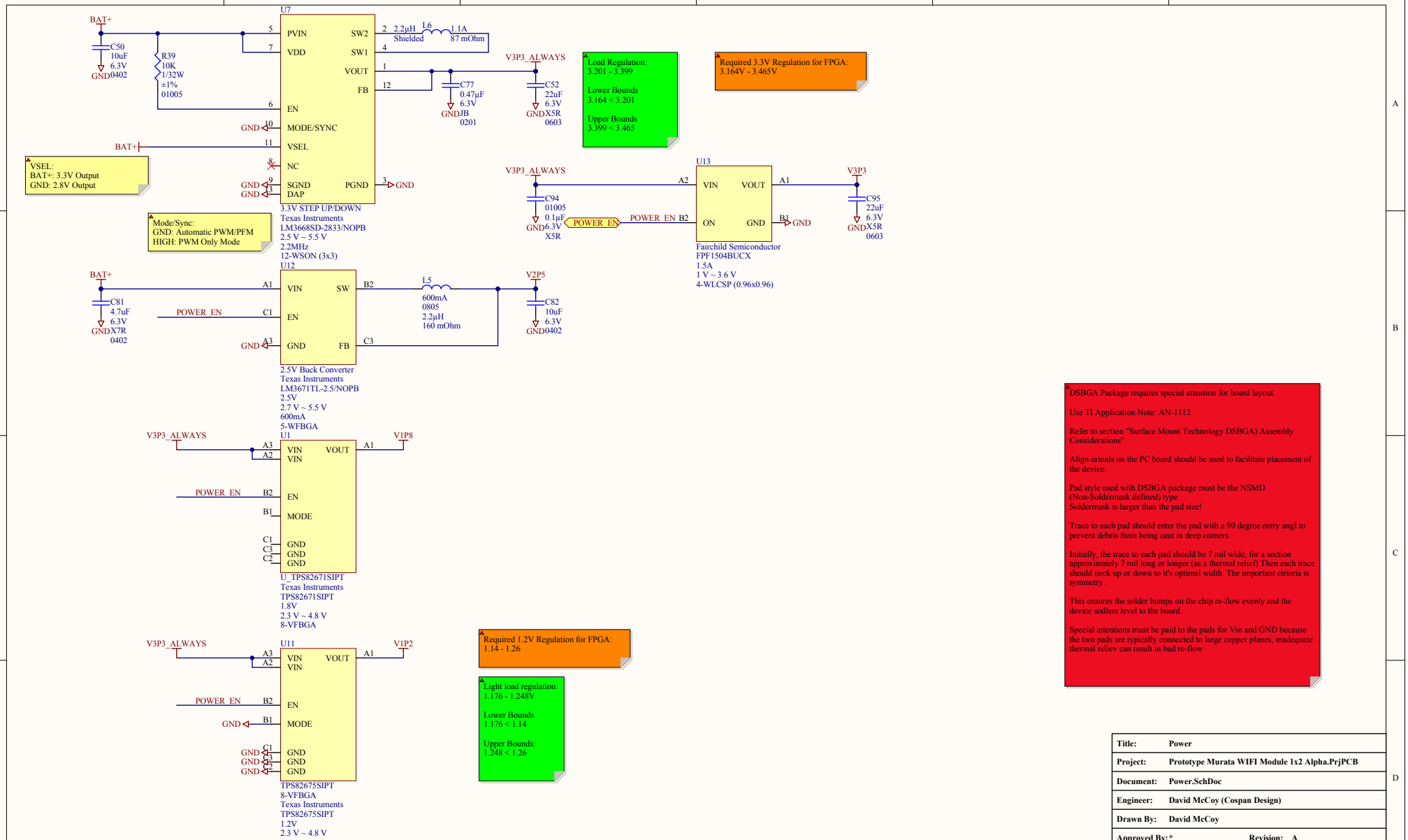
NFET Transfer Characteristics

R17 R35 Q4 EPMB
R18 R38 Q5 EPMC
R19 R40 Q6 EPMD
Q7 Q9 Q10 Q11 Q12
R41 R42 R44
EPM_HBB_P EPM_HBB_N EPM_HBC_P EPM_HBC_N EPM_HBD_P EPM_HBD_N

R53 R56 Q15 EPME
R54 R57 Q16 EPMF
R55 R58 Q17 EPMG
Q18 Q20 Q21 Q22 Q23
R59 R60 R61
EPM_HBE_P EPM_HBE_N EPM_HBF_P EPM_HBF_N EPM_HBG_P EPM_HBG_N



Title:	EPM		
Project:	Prototype Murata WIFI Module 1x2 Alpha.PrjPCB		
Document:	EPM.SchDoc		
Engineer:	David McCoy (Cospan Design)		
Drawn By:	David McCoy		
Approved By:	*	Revision:	A
Date:	10/29/2013	Number:	10 of 11



Title:	Power
Project:	Prototype Murata WIFI Module 1x2 Alpha.PrjPCB
Document:	Power.SchDoc
Engineer:	David McCoy (Cospan Design)
Drawn By:	David McCoy
Approved By: *	Revision: A
Date: 10/29/2013	Number: 11 of 11