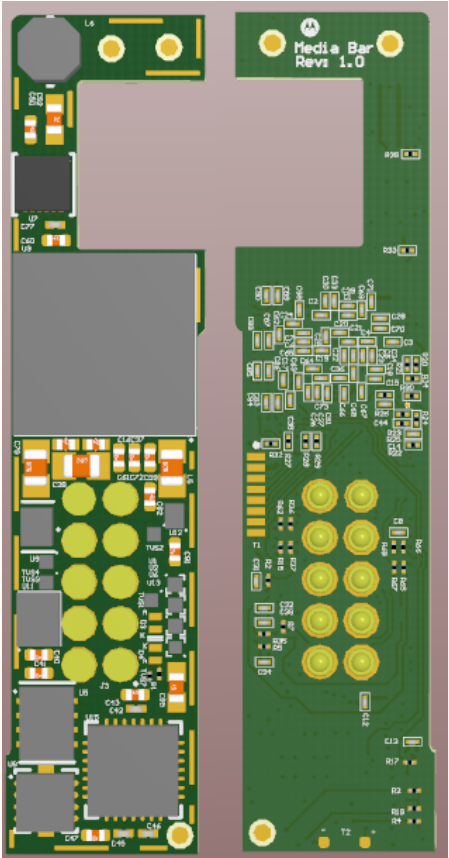
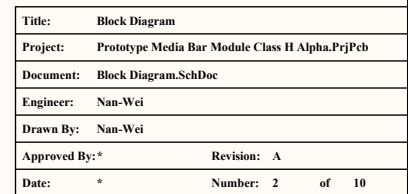


**PROTOTYPE   Media Bar Class B Medium   Alpha**

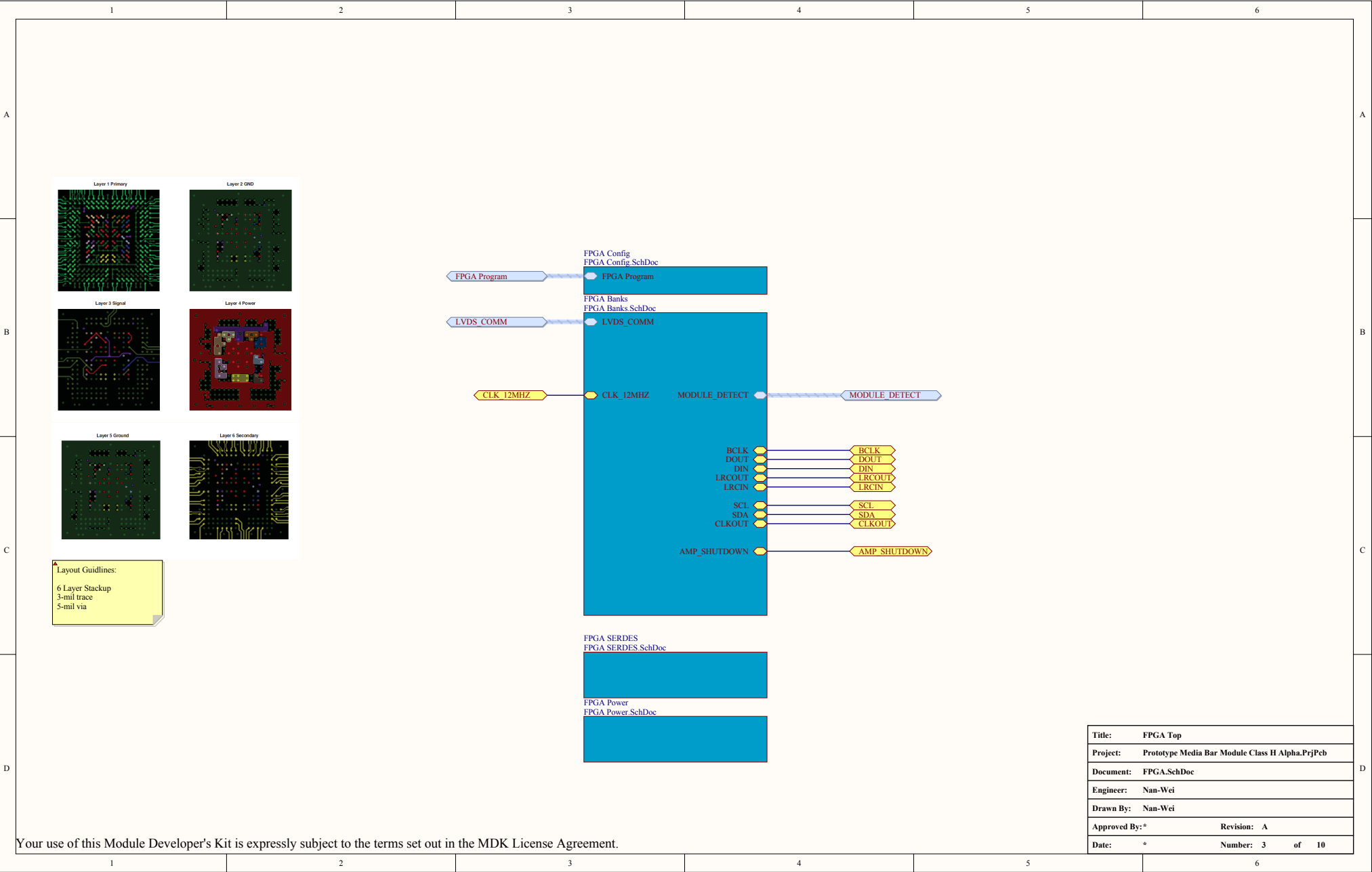
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Block Diagram  
Block Diagram SchDoe



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HOLDN: is okay to be left floating, it has an internal pull up  
WRITEN: is not used in SPI Flash, does it need to be pullup externally?  
CSN/SN: is okay to be left floating, it has an internal pull up  
DOUT: this is only used in a daisy chain configuration and can be left unconnected

SPI Configuration I/O  
CSSPIN: D17: Chip Select (Inverted)  
SPID0: SPI Serial Out (MISO)  
SPISL L17: SPI Serial In (MOSI)  
MCLK: G19: SPI Clock  
SPI Prom Size of 8Mbits  
Drive SPIFASTN Low to enable faster reading from SPI Flash

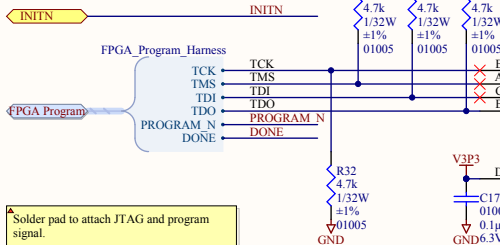
W\_N Should be tied low in production designs to disallow users from modifying the FPGA bitstream

Configuration Settings:  
SPI : 000: FPGA Reads configuration from a SPI Flash Device  
SPIm: 010: FPGA Reads configuration from a SPI Flash Device (Multiple partitions)  
SSPI: 001: FPGA is a SPI Slave that an external device such as an MCU will configure  
SCM : 101: FPGA behaves as a slave in a serial configuration protocol  
SPCM: 111: FPGA behaves as a slave in a parallel configuration protocol

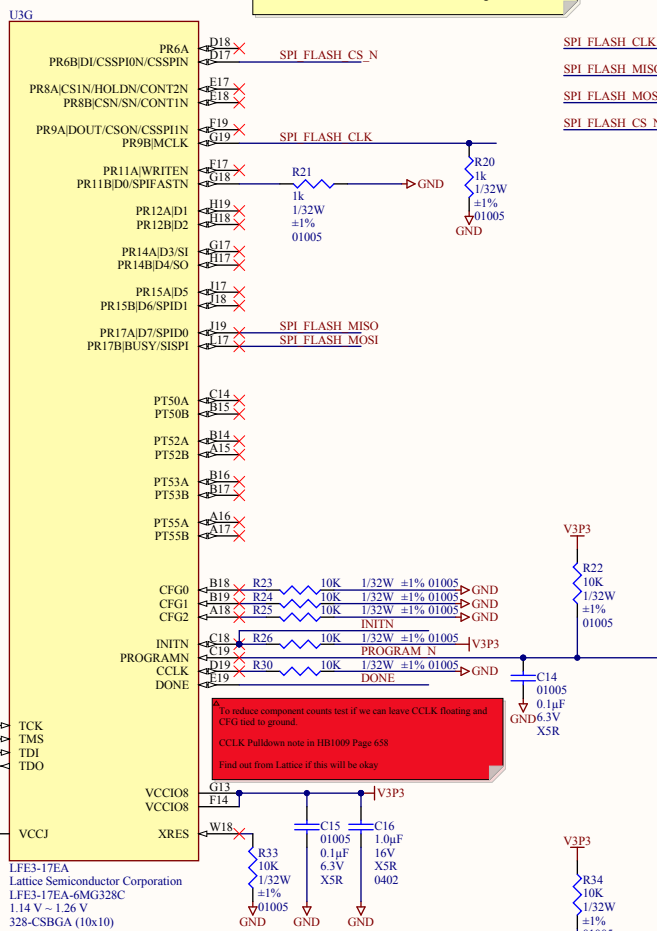
Pull down resistor on MCLK to counteract the internal pull on the pin, this will remove unintentional rising edges at power up

Programmers Note: The FPGA will program the SPI Flash chip use the ParallelFlashProgrammingandFPGAConfiguration pdf app note to see how

Need a via to solder on the INIT\_N pin for debug, during configuration if this signal goes high there was an error. The via will not be needed in the final design



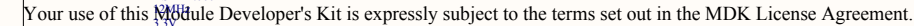
Solder pad to attach JTAG and program signal.  
For production the button used to program the FPGA can be removed and only triggered from the programming interface

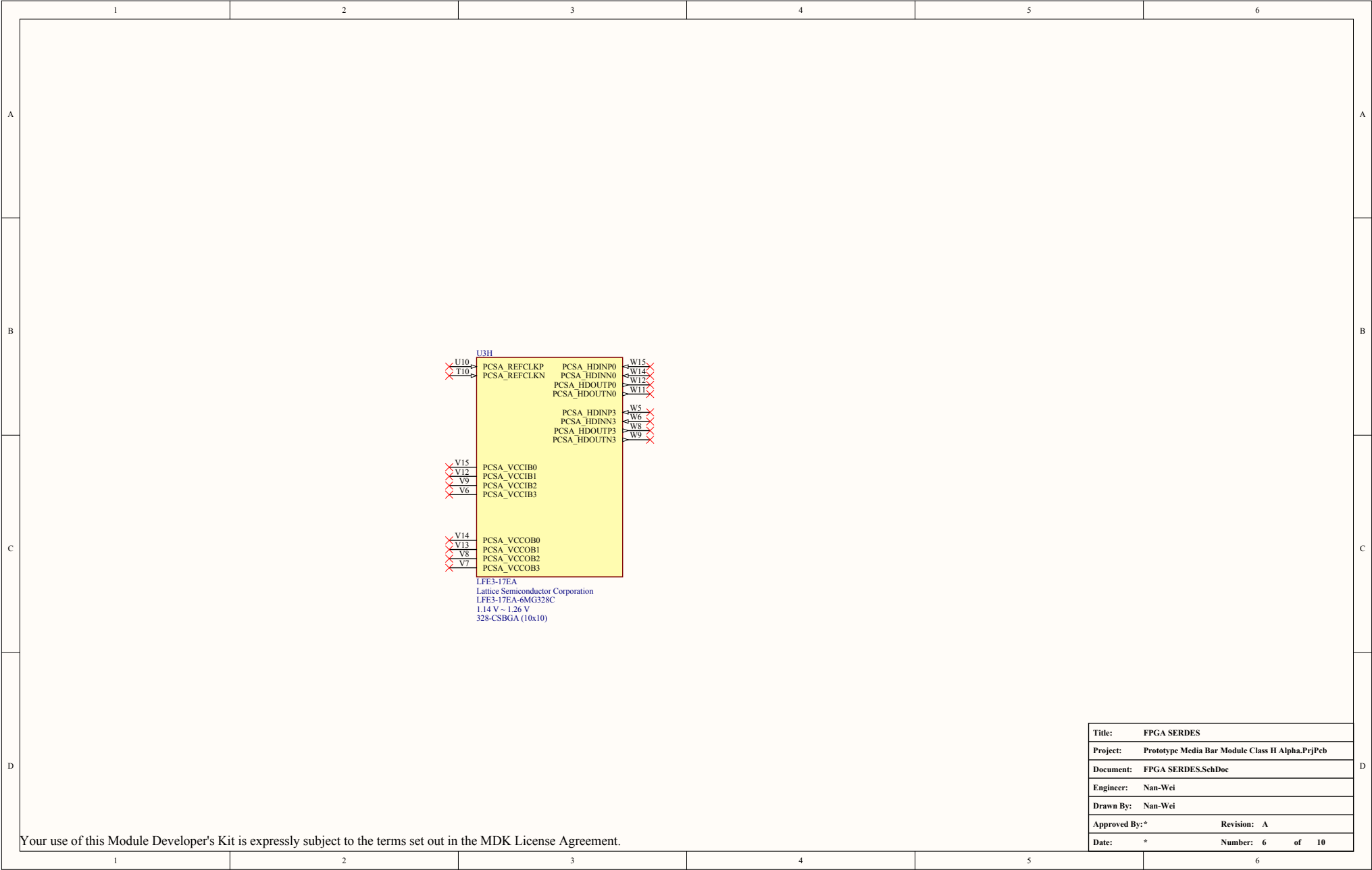


To reduce component counts test if we can leave CCLK floating and CFG test to ground.  
CCLK Pulldown note in HBI009 Page 658  
Find out from Lattice if this will be okay

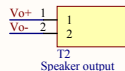
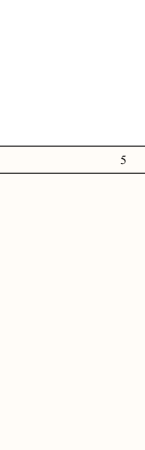
XRES: 10K pulldown  
(Used for PLL bandgap configuration)

Title:	FPGA Config
Project:	Prototype Media Bar Module Class H Alpha.PrjPcb
Document:	FPGA Config.SchDoc
Engineer:	Nan-Wei
Drawn By:	Nan-Wei
Approved By:*	Revision: A
Date:	* Number: 4 of 10









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A

B

C

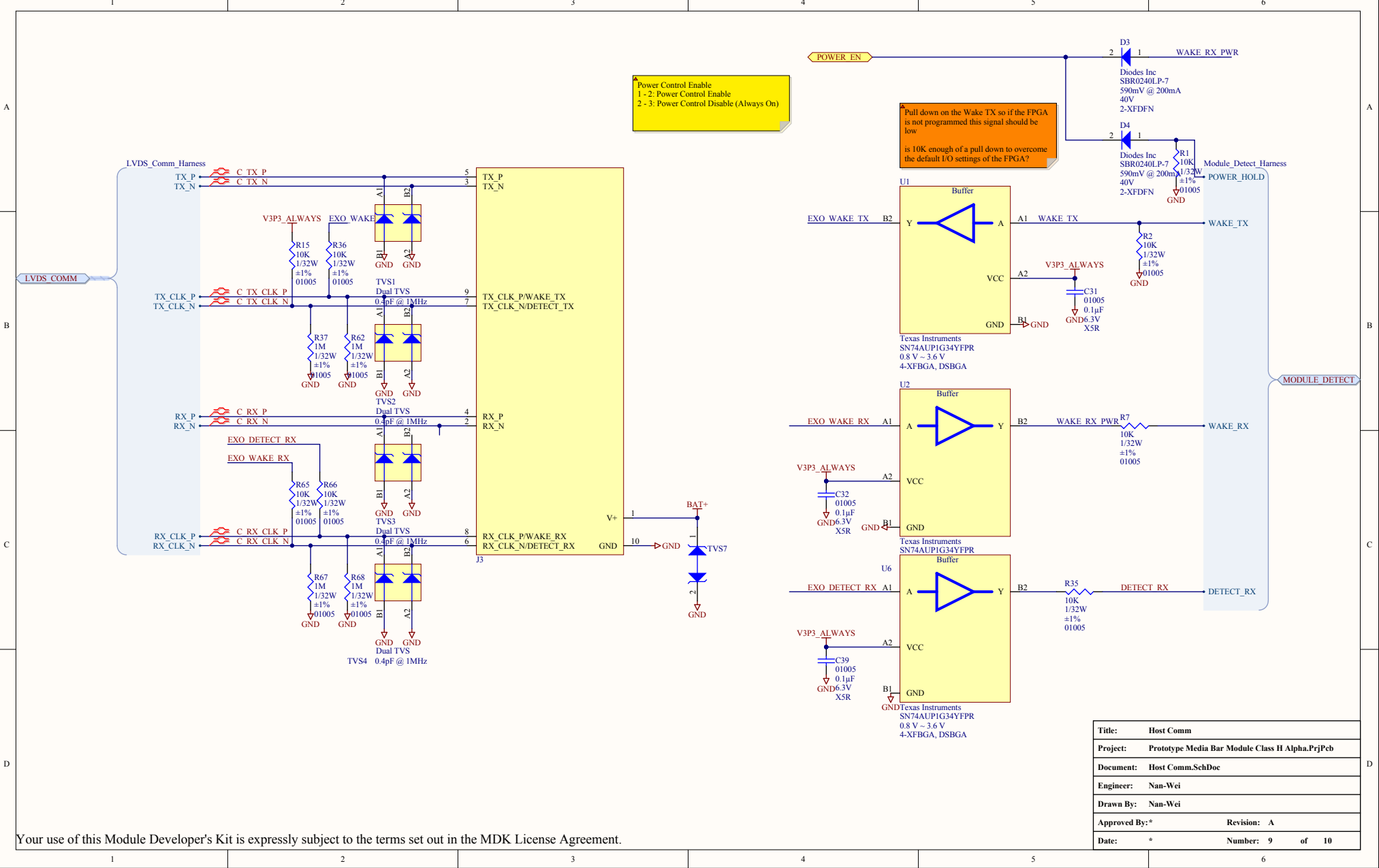
D

A

B

C

D



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