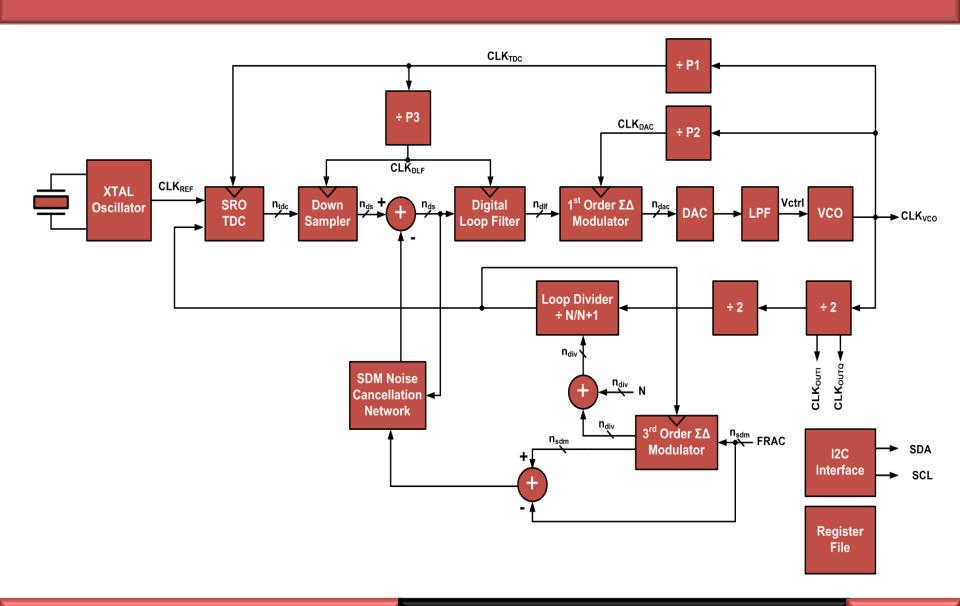


# All Digital Phase Locked Loop

#### **Digital Blocks**

Mohamed Atef March 2015

# **System Block Diagram**

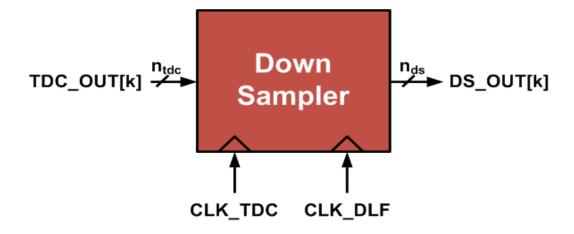


### **Digital Blocks**

- Down Sampler (CIC Filter)
- Digital Loop Filter
- MASH 1-1-1 Sigma Delta Modulator
- Sigma Delta Cancellation Network
- Register File
- SPI interface

# Down Sampler

## **Block Diagram**



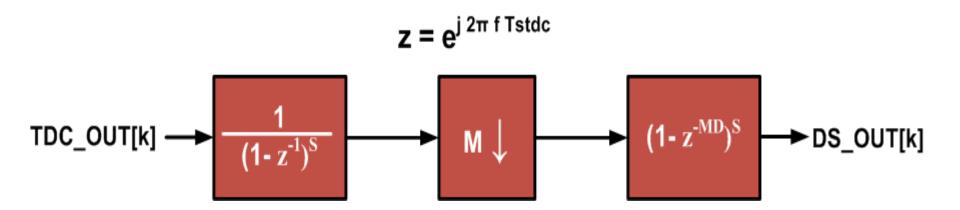
- Down Sampler is used to down sample the time-to-digital converter (TDC\_OUT) output code from TDC sampling clock (CLK\_TDC) rate to the digital loop filter clock (CLK\_DLF) rate.
- The decimation factor of TDC is given by:

$$M = \frac{f_{sTDC}}{f_{sDLF}}$$

Where  $f_{STDC}$ : TDC sampling frequency

 $f_{SDLF}$ : DLF sampling frequency

### **Transfer Function**



The Transfer function is given as:

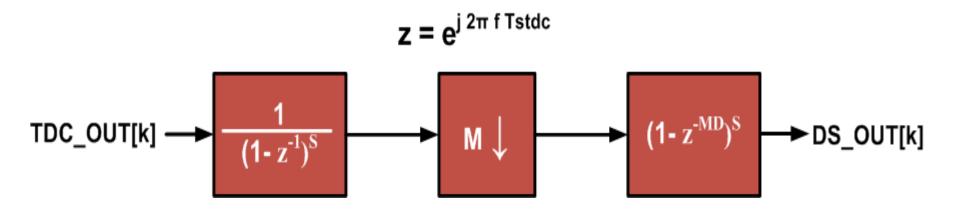
$$H(z) = \frac{(1 - z^{-MD})^{s}}{(1 - z^{-1})^{s}}$$

Where M: Decimation Factor

**D: Number of Differential Delay Units** 

**S: Number of CIC stages** 

### **Transfer Function**



The bandwidth of this filter is given as:

$$f_{BW} = \frac{f_{STDC}}{D M}$$

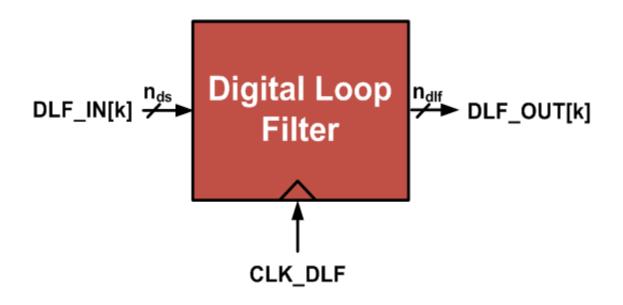
# **Specifications**

Design Parameter	Symbol	Min. Value	Typ. Value	Max. Value	Unit
TDC Sampling Frequency	$f_{sTDC}$	600	-	625	MHz
DLF Sampling Frequency	$f_{\text{sDLF}}$	37.5	-	39.0625	MHz
CIC Filter Bandwidth	$f_{BW}$	-	19.53125	-	MHz
TDC Number of Output Bits	$n_{tdc}$	-	5	-	Bits
Down Sampling Factor	M	-	16	-	-
CIC Number of Stages	S	-	3	-	-
CIC Number of Differential Delay Units	D	-	2	-	-
CIC Number of Output Bits	n <sub>cic</sub>	-	20	-	Bits
Down Sampler Number of Output Bits	$N_{ds}$	-	15	-	Bits

Discard the last five least significant bits of CIC word to get the downsampler word

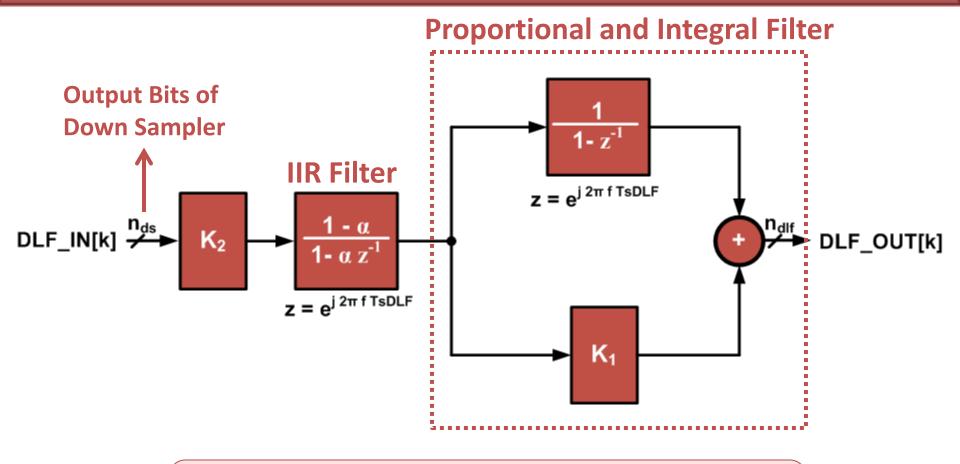
# Digital Loop Filter

### **Block Diagram**



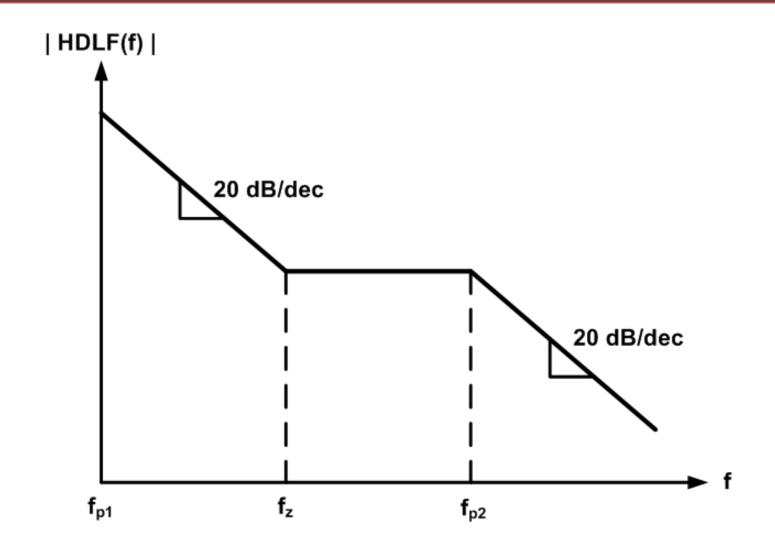
- Second-Order digital filter
- IIR Filter + Proportional and Integral Filter

#### **Transfer Function**



$$H_{DLF}(z) = K_2 \times \frac{1-\alpha}{1-\alpha z^{-1}} \times \frac{(K_1+1)-K_1z^{-1}}{1-z^{-1}}$$

# Ideal Magnitude Response

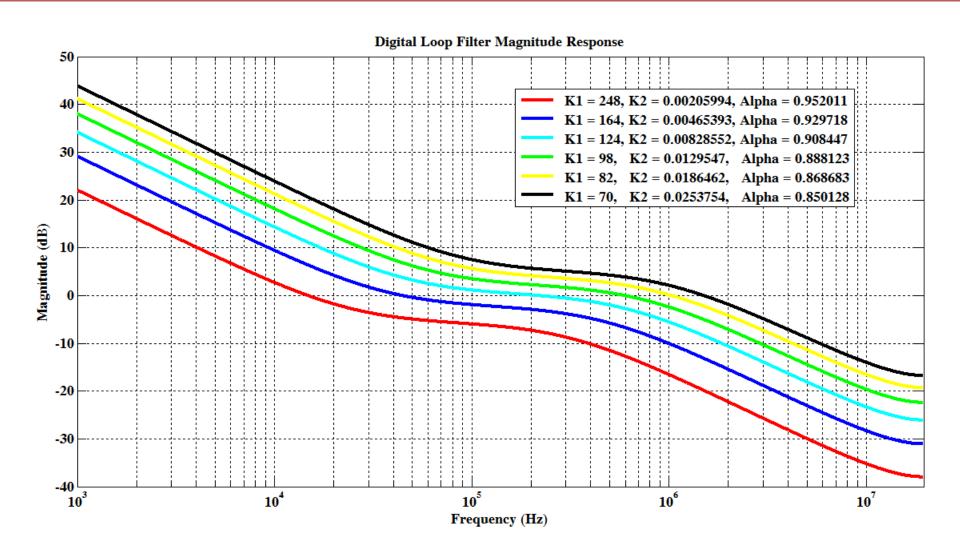


## **Specifications**

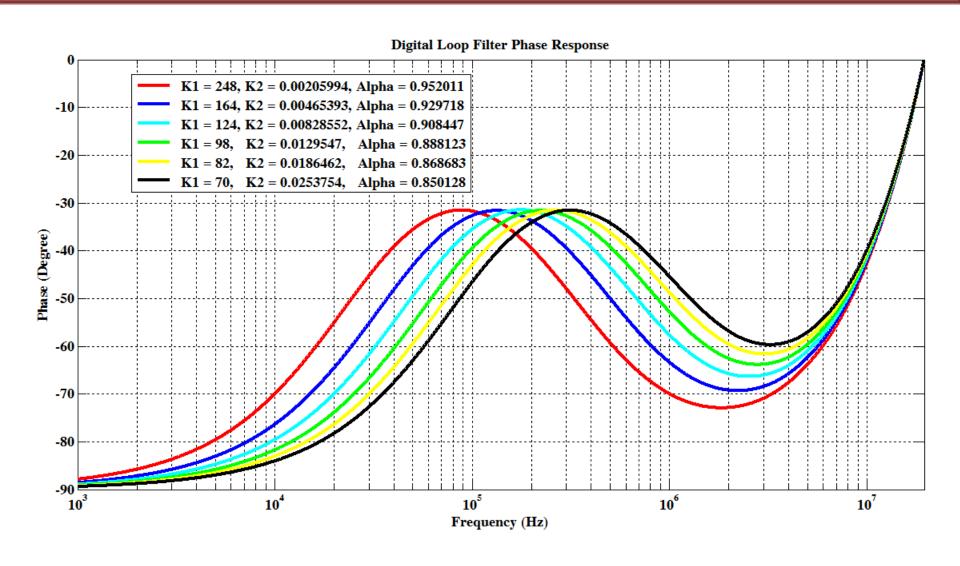
Design Parameter	Symbol	Min. Value	Max. Value	Unit
DLF Sampling Frequency	f <sub>sDLF</sub>	37.5	39.0625	MHz
Coefficients	K <sub>1</sub>	70	248	-
	K <sub>2</sub>	0.00205994	0.0253754	-
	α	0.850128	0.952011	-

 The DLF coefficients is needed to be programmable so it is need to be saved in the register file.

## Magnitude Response



### **Phase Response**



# Thank You!