APR FOLDER STRUCTURE

Layout Team

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APR files should be prepared at the beginning of any APR process, And to start APR process you should be supplied by two main file (Verilog file – SDC file), In the path */Project/digital/APR/topModule/vx_date/* you should create a structure as showen in figure 1, We are going to refer to the top level module as "TopModule" and the cell name and version as "VX_date".

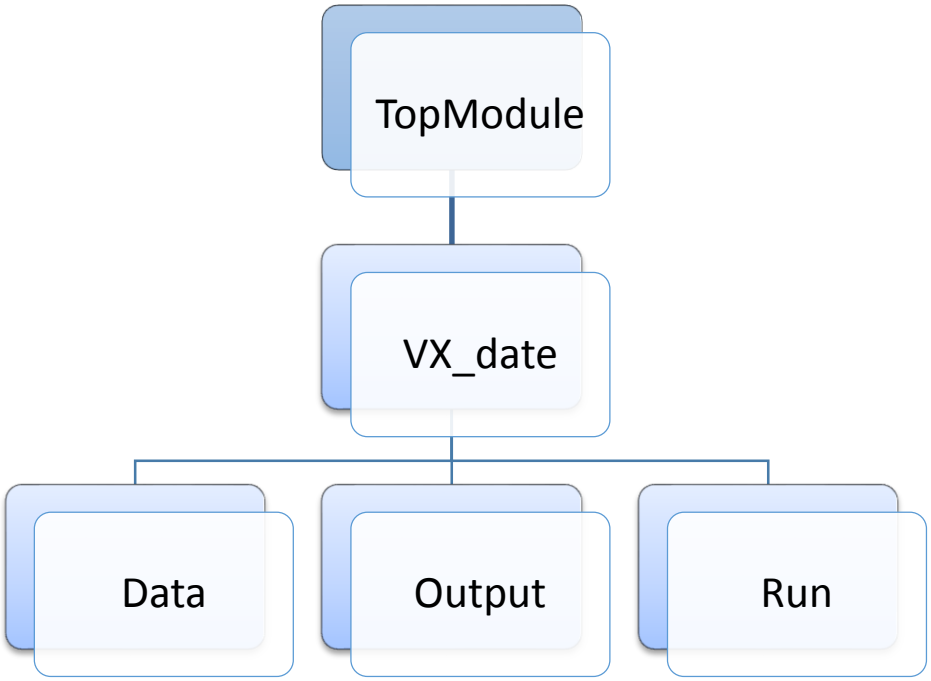

Figure 1 APR folder structure

- **Data Folder**

Data folder contain some input file and some files generated once during the run and use for all upcoming runs in the APR process, and these files are divided in to the folders as following:

Configuration file

This file contain the declaration of all the timing variables that will be used in check the timing of the design after layout, All these variables are declared as global variables and it should contain the declaration of the LEF[1] files used in the design. It should contain also some inputs like: (Net list name – net list type – top cell name - VSS and VDD names - …)

CTS (Clock Tree Synthesis)

This file contain the Clock tree routs that used to distribute the clock inside your design this file is generated once at the beginning and then use it for the upcoming runs

Floor-plan

This file contain the intial floor plan for the top level module and there are some steps to generate this floor plan (.def file) at the beginning of the APR process.

1- Initially you export the icon view from Cadence and this file contains the name of the pins and its location using the script (getpins)

[1] LEF file is the file that contains all the information about the standard cells (Pins – Metals ….)

2- Open encounter and export the initial floor plan with the required area but the pins not properly allocated
3- Use the script (iconto def) to transfer the pins co-ordinates to the initial def file to generate anew .def file contains the right area and shape of the top level with a properly allocated pins on the boundary
4- This step is done only one time at the beginning of the APR process and it should be done again if the floor plan has area changes or pin changes

Map
This file contain the name of the metal layers and VIA layers and its corresponding number in the technology and it is used to transfer the output of the encounter to real GDS II that could be fabricated.

Procedure
This file contain the typical commands used in the encounter tool to do the process through using terminal not the GUI and you can get it at the beginning of the process from its template

SDC
This file is supplied before the beginning of the APR process and it mainly contains the delays used in the design the do not touch signals the parasitic capacitance.

Source me file
In this file you should set the value of the variables that are declared in the configuration file to be used in the APR process

Verilog
This is also a supplied file before the beginning of the APR process that contain the main design after the synthesis

- # Output Folder

Output folder contain all the final output that should be used after finishing the APR, and these files are divided in to the folders as following:

CMD log directory
It contains the *command file (.cmd file)* used to run the APR and the *log file* (encounter.log) generated while running the APR showing the warnings and the errors (if found).

ENC directory
It contains the final design saved when using the command: saveDesign ../output/enc/*cellname*_top.enc

GDS directory
It contains the output gds file (gds.gz) generated after the APR, can be directly imported to Cadence to be used in the integration.

SDF auto directory
It contains the sdf files at all the process corners generated after running the script *create_enc.pl* and sourcing the file *enc_commands*.

Timing Reports directory[2]

It contains all the timing reports at all the process corners generated after running the script *create_enc.pl* and sourcing the file *enc_commands*. And it is categorized as:

reg2reg – reg2out – in2reg – in2out – clkgate	Files classified by its type contain the timing for each path in the setup mode and in hold mode (each in separate file)
Hold .slk - .slk	Contain the slack times for all the paths for hold mode and setup mode respectively
Hold.summary - .summary	Contain a summary table for the violating paths for hold mode and setup mode
.cap - .fanout - .trans	Contain the electrical violations for driving capacitance and fanout and transotions
all.tarpt – all_hold.tarpt	Contain the detailed information for the violating paths

VG directory

It contains the logical netlist that doesn't include filler cells nor power supply data (Cellname.log.vg) and the physical netlist that includes filler cells and power supply data (Cellname.phys.vg).

- # Run Folder

This is the folder that you should point at when you are running the APR process and it will contain many files like the:

- Encounter .cmd file contain the commands used in the encounter too.
- Encounter.log and this is a log file contain the warnings and errors through the process.
- Some .enc files saved through the process run.
- Verification reports like (LVS – DRC – Antenna - …)
- Some clock reports generated through the optimization.

[2] For more details refer to the APR Timing document