All Digital Phase Locked Loop

Digital Blocks

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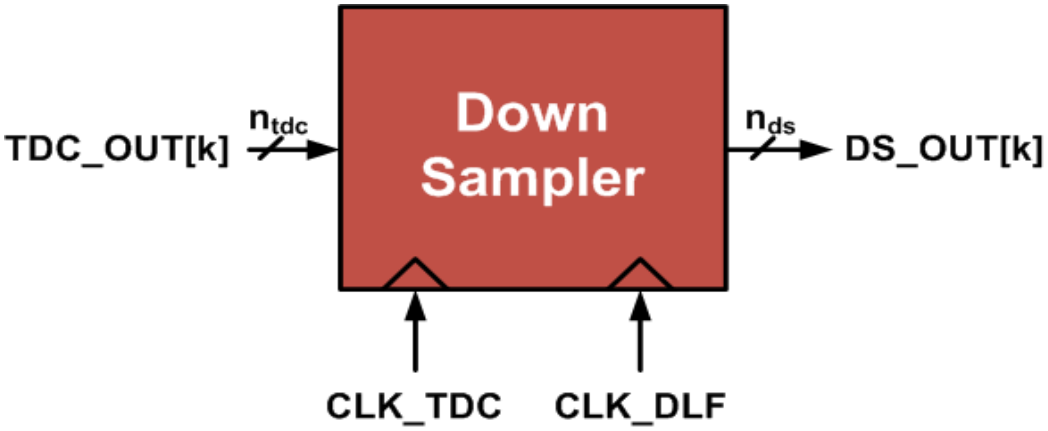
Digital Blocks

- Down Sampler
- Digital Loop Filter
- Sigma Delta Cancellation Network
- Register File
- I^2C interface

Down Sampler

Block Diagram



- Down Sampler is used to down sample the time-to-digital converter (TDC_OUT) code from TDC sampling clock (CLK_TDC) rate to the digital loop filter clock (CLK_DLF) rate.
- The decimation factor of TDC is given by:

$$M_{TDC} = \frac{f_{sTDC}}{f_{sDLF}}$$

Where f_{sTDC}: TDC sampling frequency

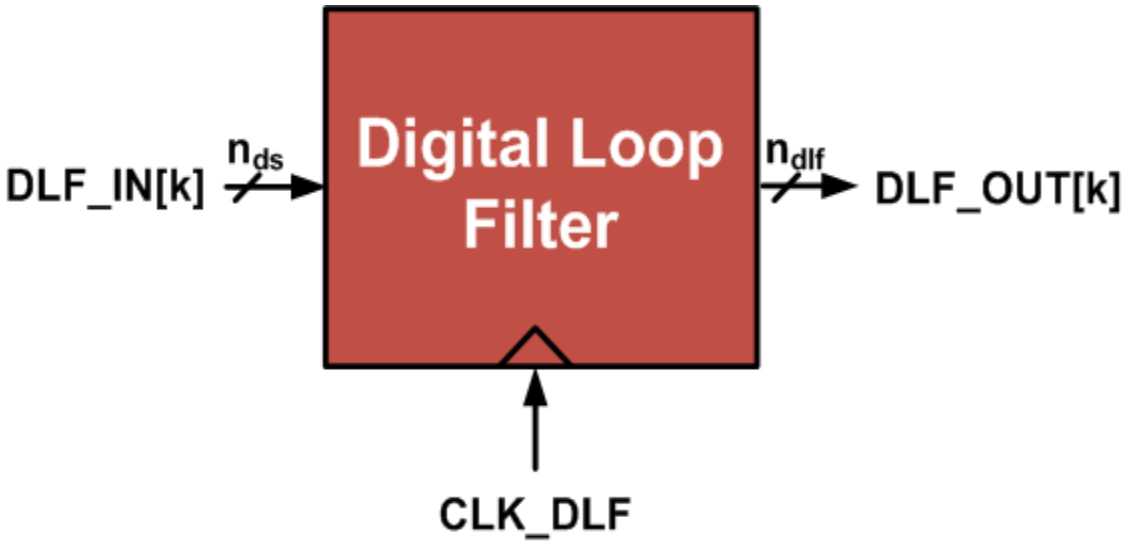
f_{sDLF}: DLF sampling frequency

Specifications

Design Parameter	Symbol	Value	Unit
TDC Sampling Frequency	f_{sTDC}	625	MHz
DLF Sampling Frequency	f_{sDLF}	78.125	MHz
Down Sampling Factor	M_{TDC}	8	-
TDC Number of Bits	n_{tdc}	5	Bits

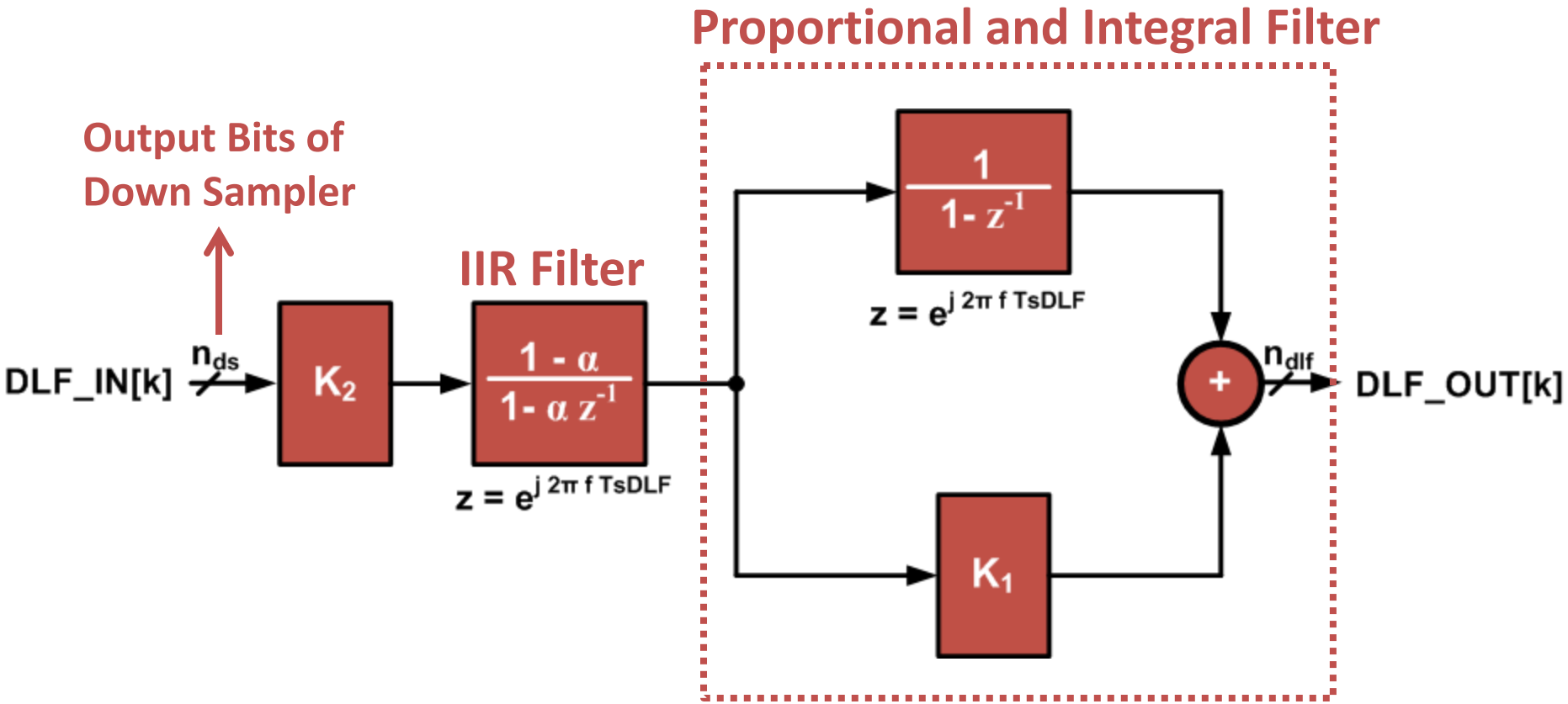
Digital Loop Filter

Block Diagram



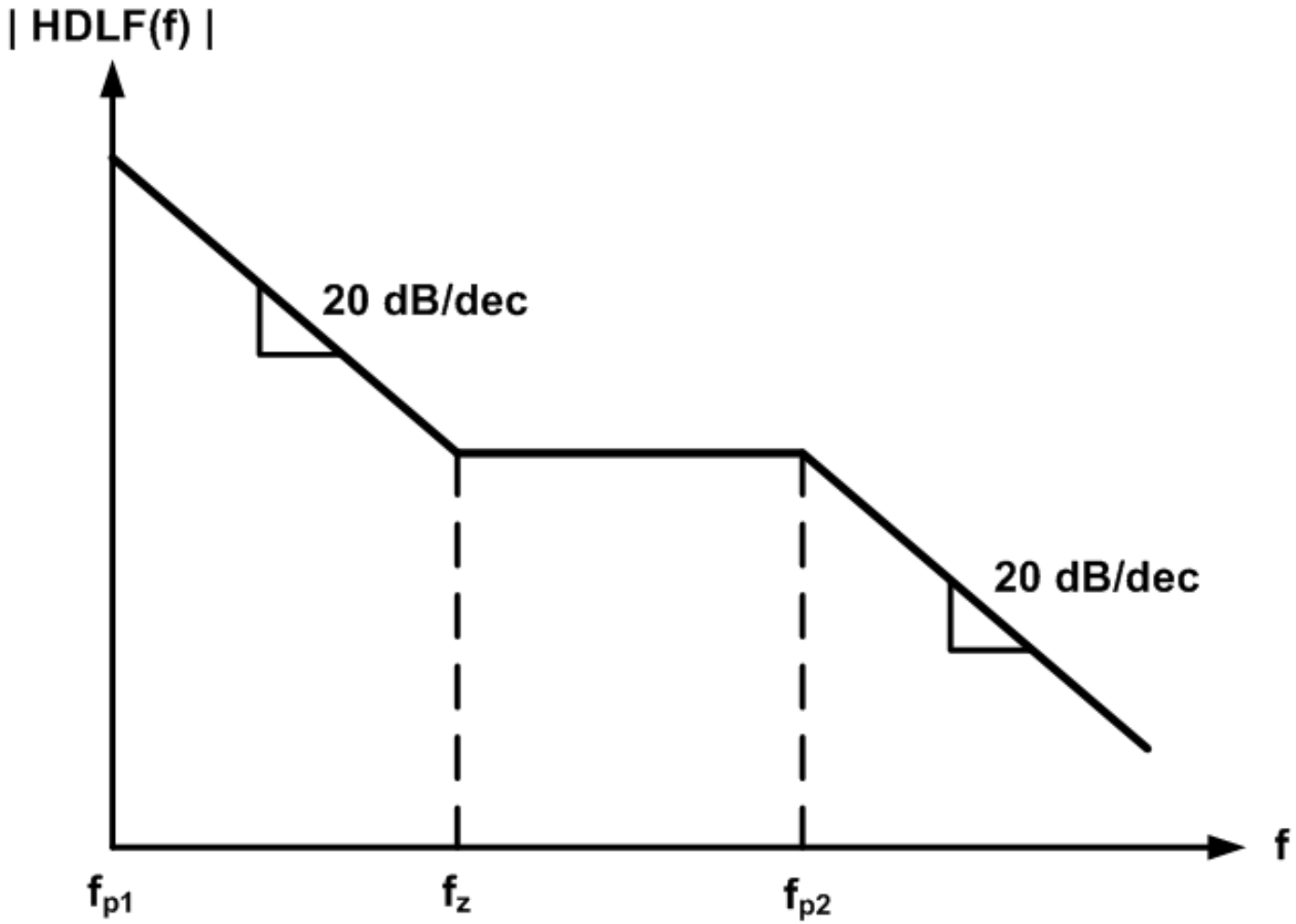
- Second-Order digital filter

Transfer Function



$$H_{DLF}(z) = K_2 \times \frac{1-\alpha}{1-\alpha\, z^{-1}} \times \frac{(K_1+1) - K_1 z^{-1}}{1-z^{-1}}$$

Ideal Magnitude Response

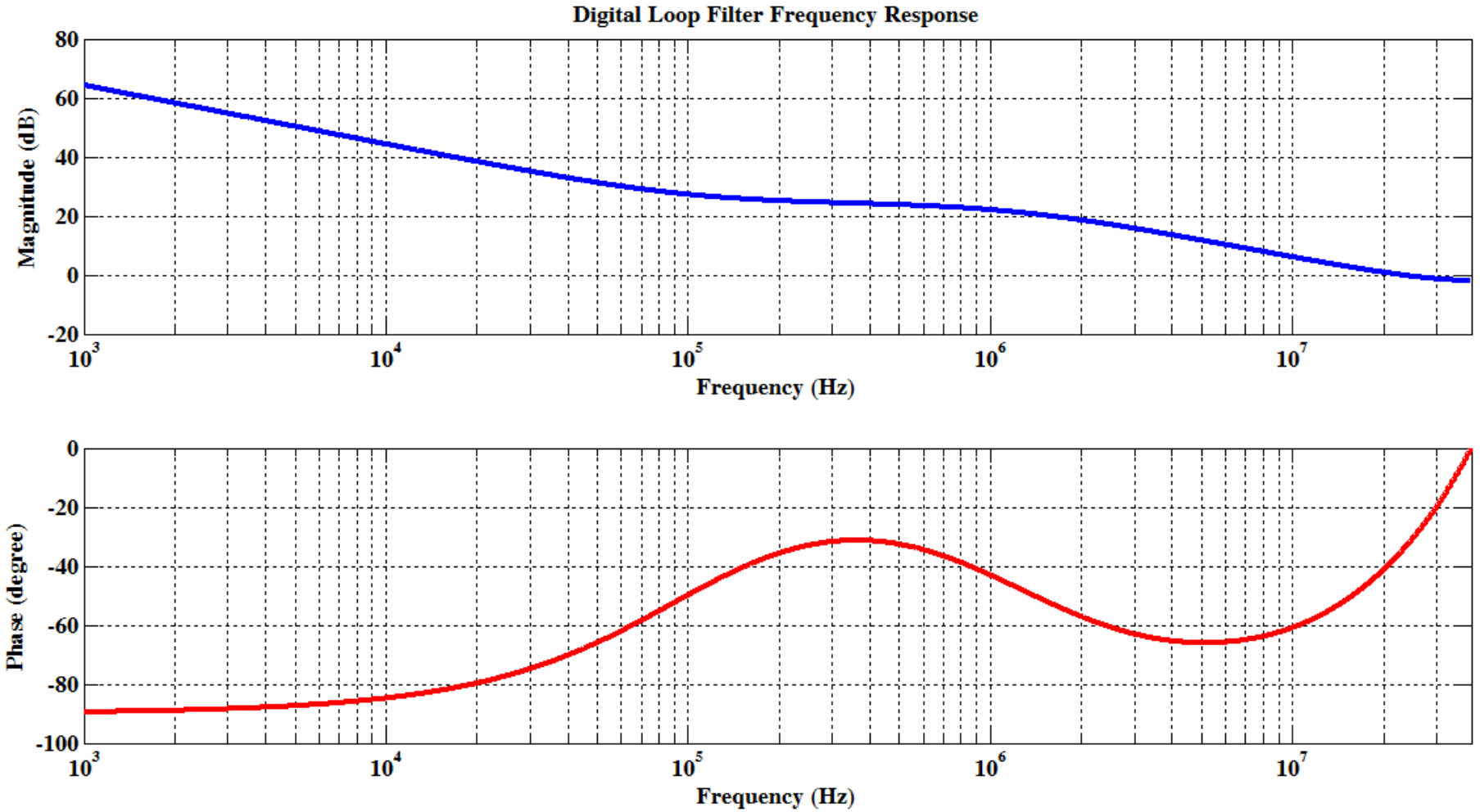


Specifications

Design Parameter	Symbol	Value	Unit
DLF Sampling Frequency	f_{sDLF}	78.125	MHz
DLF Coefficients	K_1	122	-
	K_2	0.132813	-
	α	0.90625	-

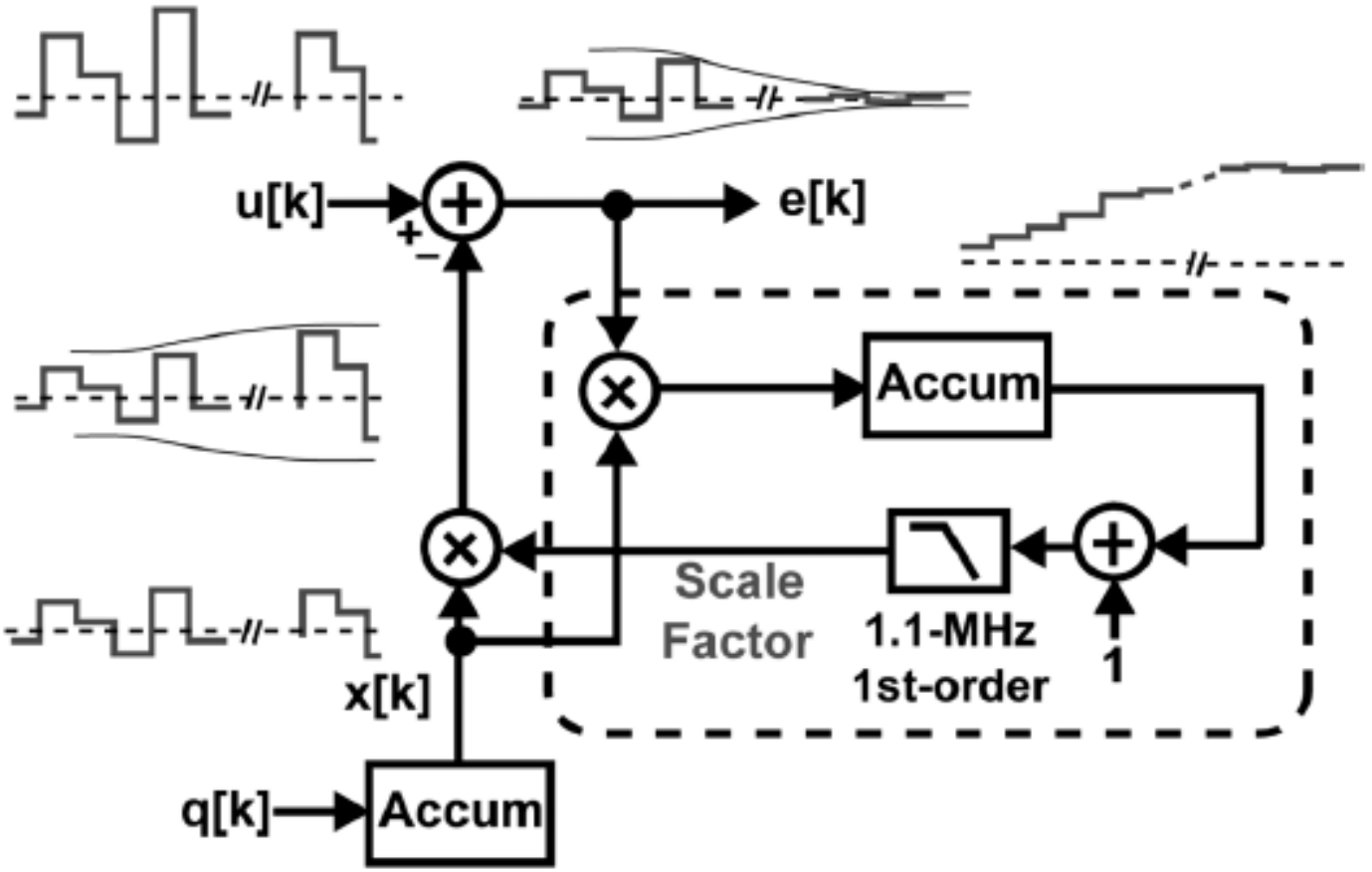
- The DLF coefficients is needed to be programmable so it is need to be saved in the register file.

Frequency Response



Sigma Delta Cancellation Network

Block Diagram



Block Diagram

- The quantization noise q[k] is fed into an accumulator (to convert from frequency to phase) and then subtracted from the TDC output after being properly scaled.
- The scale factor is easily computed by a simple digital correlator (a 16-bit digital multiplier) and accumulator circuit.
- In the case where the quantization noise is completely cancelled, the correlation will become zero and the accumulator will hold its value at the proper scale factor.
- An IIR low pass filter with cutoff frequency of 1.1 MHz is used to further smooth the scale factor signal.

Signals Mapping

Signal	Mapping	Number of Bits
u[k]	Output of Down Sampler Signal DS_OUT[k]	n_{ds}
e[k]	DLF input signal DLF_IN[k]	n_{ds}
q[k]	Quantization noise signal of MASH 1-1-1 SDM	$n_{sdm} = 11$

Register File

Register File

- Register file contains trimmer control lines for analog blocks and control bits for digital blocks.

I^2C Interface

I^2C Communications

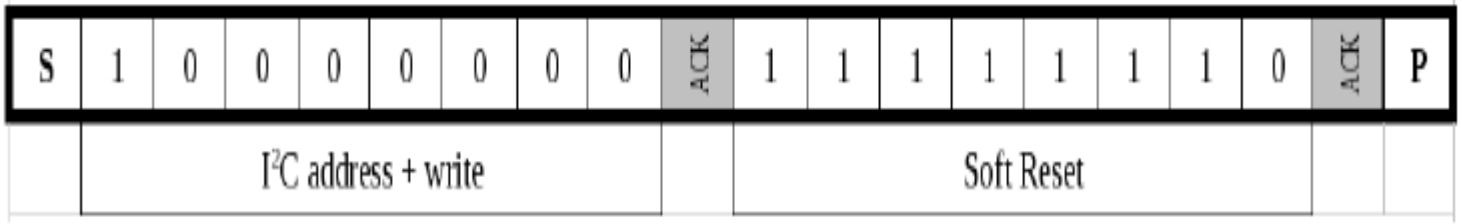
- I^2C bus is a bidirectional open drain bus, the bus is pulled high when there is no activity.
- The data line “SDA” must go low while the clock line “SCL” is still high to indicate a start of communication.
- SDA must go from low to high while SCL is high to indicate stop of communication.
- After the start condition, the master controller sends the device address in 7 bits and the direction of communication on the eight's bit if its read '1' or write '0', the addressed device must pull down the SDA line on the ninth bit to proceed in the communication, other wise the communication will stop at this point.

I²C Communications

- After the address is fetched correctly, any of the following commands can be sent to the device.

1) Soft Reset

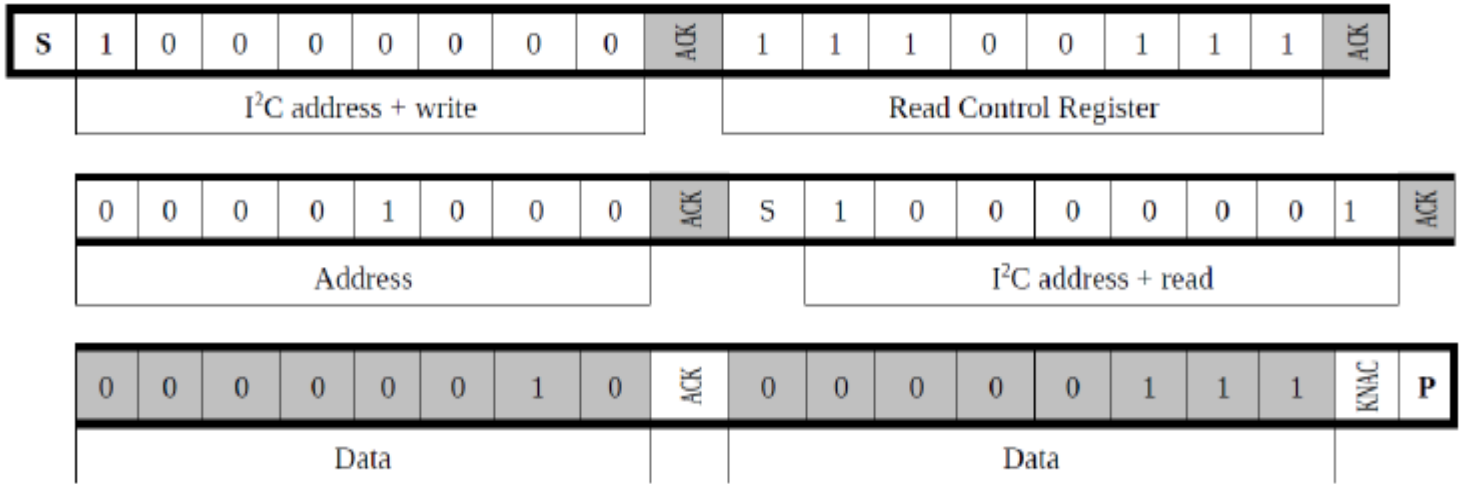
- Used for rebooting the system without switching off the power.
- Upon reception of this command, the system reinitialize and starts operation according to the default setting.



I²C Communications

2) Read Control Register

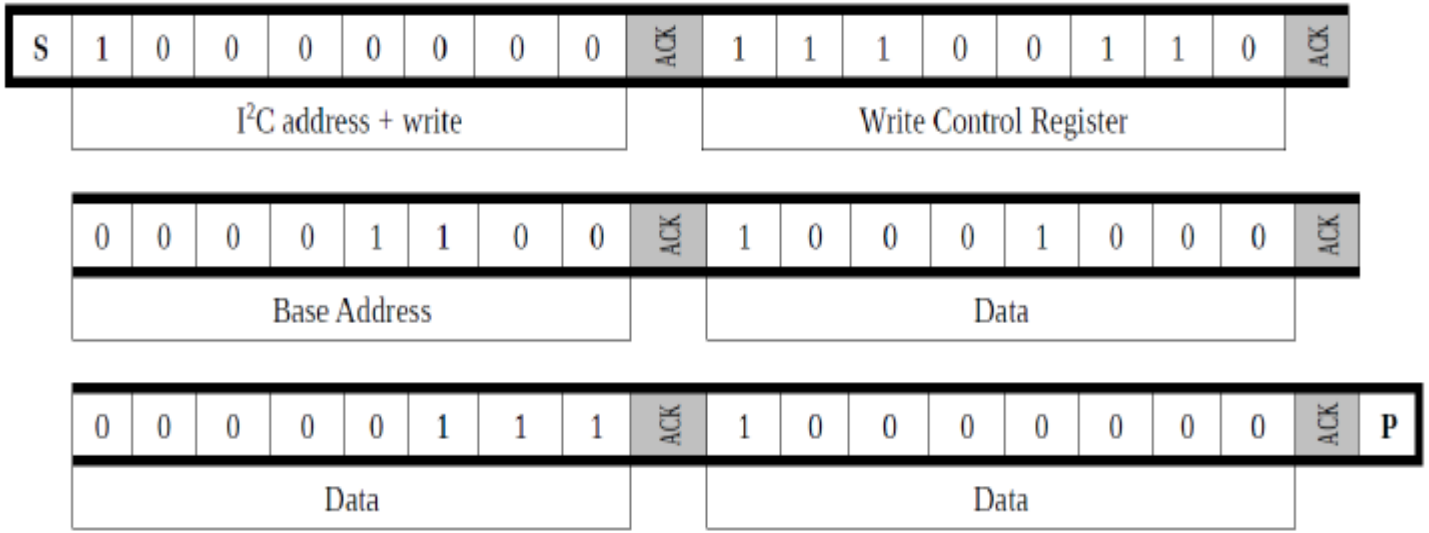
- Used to read values from the register map.
- Master controller sends the base address to start reading from.
- Upon completion, master sends an NACK & stop condition.



I²C Communications

3) Write Control Register

- Used to write values in the control register
- Master controller sends the base address followed by the data bytes followed by stop at write completion



Thank You!