Silicon Vision
Innovative IC Solutions

APR TIMING

Layout Team

Haitham Ghoniem

May 2014
Version 1.0

• Introduction

Our designs are limited by getting data between FFs, Combinational Logic delay, Routing delay, and FF parameters dictate the maximum speed. The flip-flops shown are positive edge triggered, i.e. on the positive edge of the clock, they takes the value of the signal at its input and send it to the flip-flop's output after a small delay called the $t_{clock\text{-}to\text{-}Q}$

The flip-flops do their job correctly only if the signal at their inputs does not change for some time before the clock edge (t_{setup}) and a time after the clock edge (t_{hold}) as shown in the figure below. In addition, the clock signal, which flows around the system on a separate set of wires called the clock tree, has its own variability, called skew.

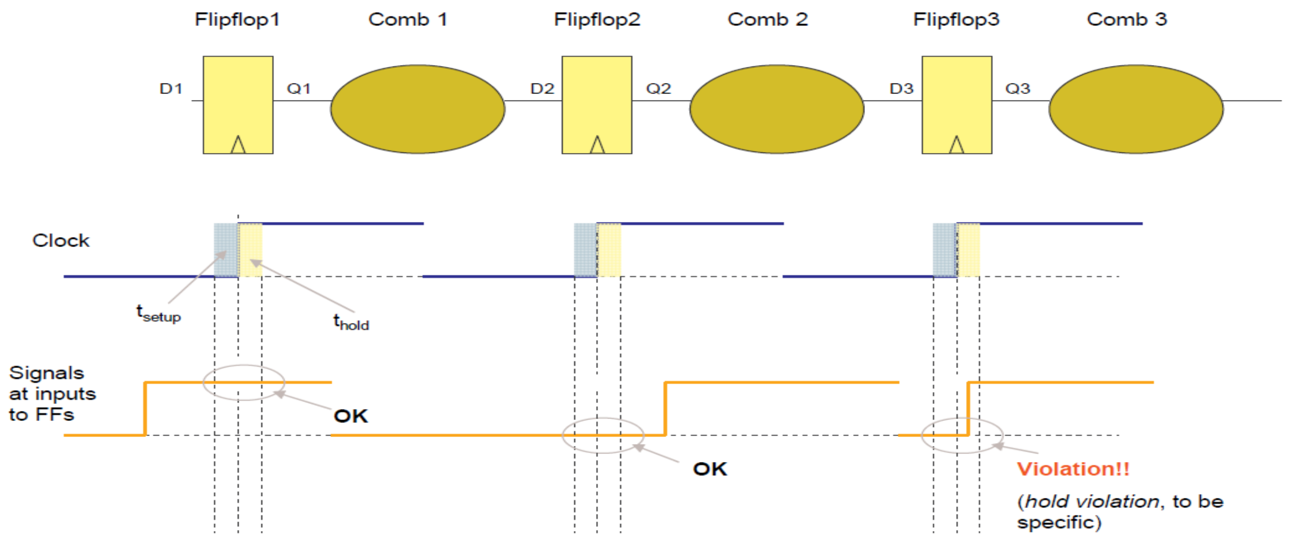


Figure 1 Setup and Hold times

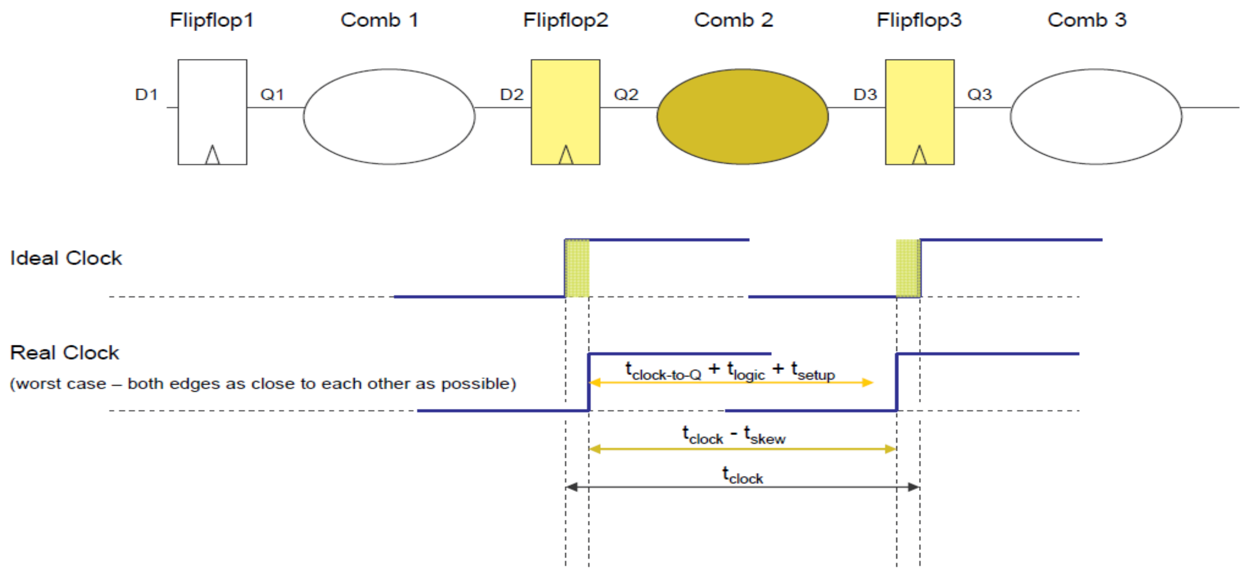


Figure 2 Setup explanation

Time to propagate a valid (no violations) signal at D2, to D3, counting from the clock edge at flip-flop2, is invariably = $t_{clock\text{-}to\text{-}Q} + t_{logic}$. And for flipflop3 to latch it, this signal has to be maintained at D3 for t_{setup} time before the clock tree sends the next positive edge of the clock to Flipflop3.

Therefore, to make sure the signal is SETUP at the input of Flipflop3 far enough ahead of the clock edge.

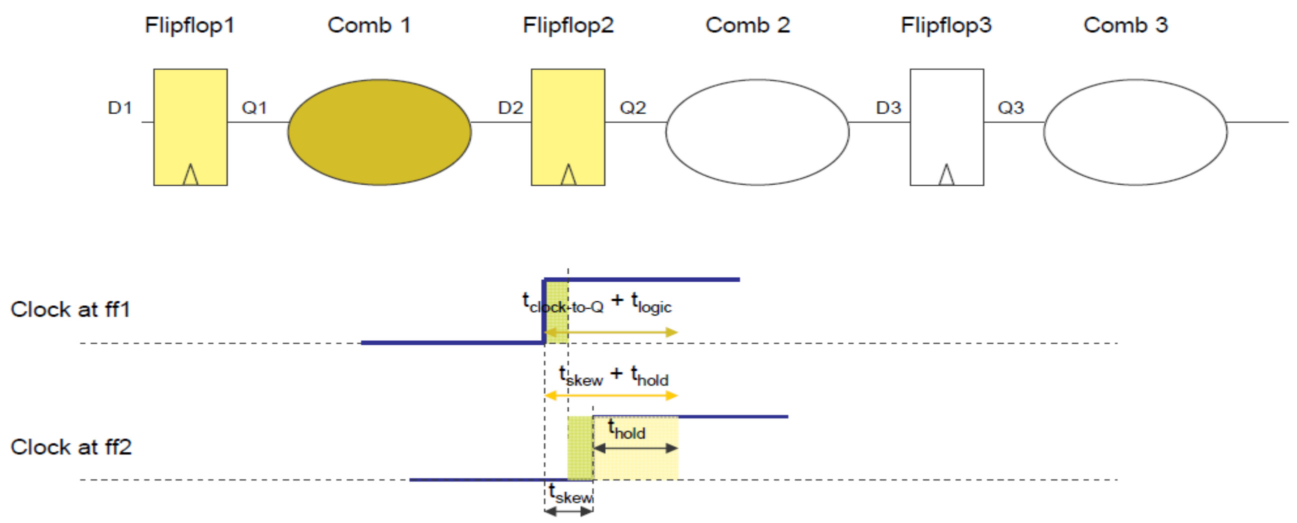


Figure 3 Hold explanation

For D2 to be able to send its signal to Q2, it must be left unchanged for t_{hold} time after a clock edge. That is, during this time, a signal from D1 should not be able to race through the combinational logic Comb1 and make it to D2.

Therefore, to make sure the signal is HELD properly at the input of Flipflop2 without the input of the previous flip-flop (D1) racing through.

So to prevent both setup and hold violation both coming relations should be followed:

to prevent setup violations …

$$\underleftrightarrow{t_{clock\text{-}to\text{-}Q\_max} + t_{logic\_max} + t_{setup\_max}} \quad \substack{<\\=} \quad \underleftrightarrow{t_{clock} - t_{skew}}$$

to prevent hold violations …

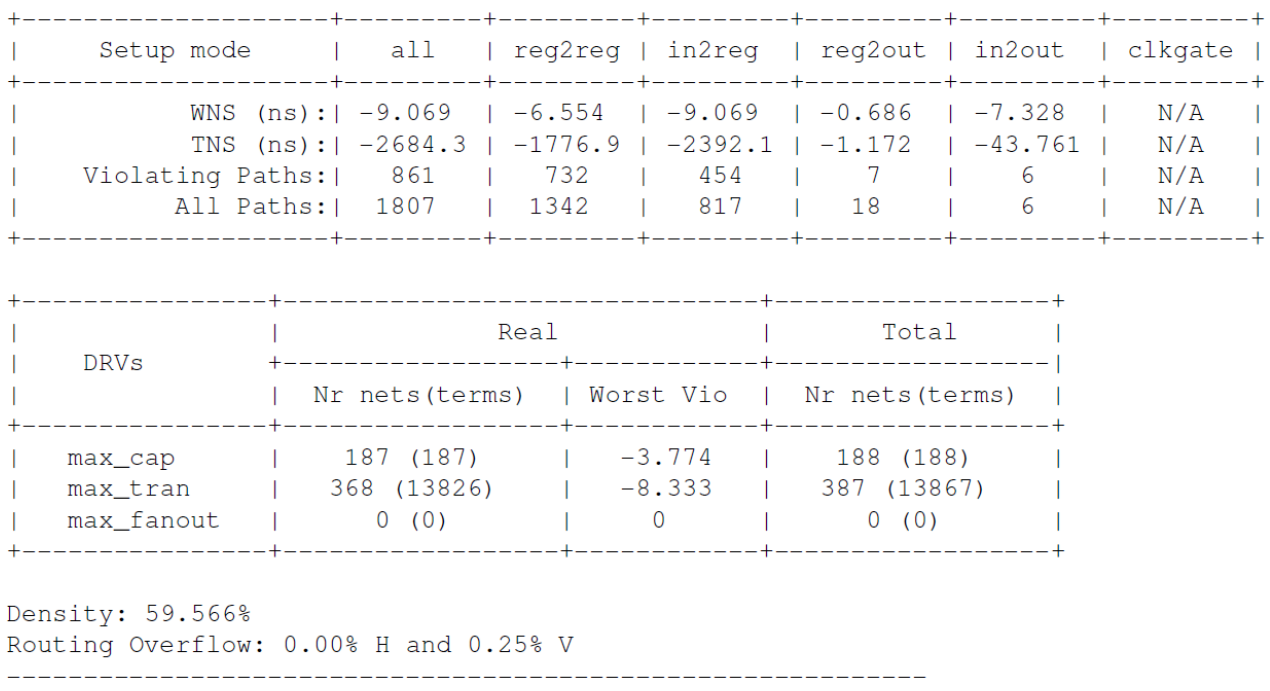
$$\underleftrightarrow{t_{skew} + t_{hold\_max}} \quad \substack{<\\=} \quad \underleftrightarrow{t_{clock\text{-}to\text{-}Q\_min} + t_{logic\_min}}$$

- **Analysis**

CADENCE SOC ENCOUNTER has a practical timing analysis function, where you only have to specify the state of the design (as shown below)[1] and the ANALYSIS TYPE (Setup or Hold) you want to run.
Pre-Place design is not placed
Pre-CTS design is placed but clock tree is not yet inserted
Post-CTS design is placed and the clock tree is inserted
Post-Route design is placed and routed
Sign-Off will use extra tools for even more precise analysis

The Accuracy and reality of the violations depends on the state you are using in the analysis. After the analysis a short summary will be displayed on the console as shown below:

For Setup type:



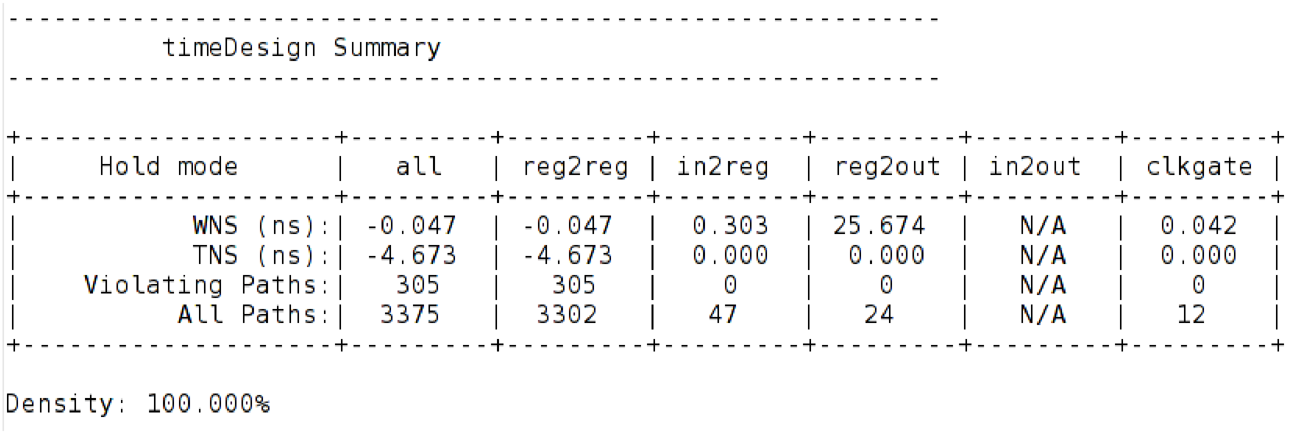
```
+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):| -9.069  | -6.554  | -9.069  | -0.686  | -7.328  |   N/A   |
|           TNS (ns):| -2684.3 | -1776.9 | -2392.1 | -1.172  | -43.761 |   N/A   |
|    Violating Paths:|   861   |   732   |   454   |    7    |    6    |   N/A   |
|          All Paths:|  1807   |  1342   |   817   |   18    |    6    |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |    187 (187)     |   -3.774   |    188 (188)     |
|   max_tran     |   368 (13826)    |   -8.333   |   387 (13867)    |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 59.566%
Routing Overflow: 0.00% H and 0.25% V
------------------------------------------------------------
```

Figure 4 Setup time violation

[1] All the analyses before the routing, the tool trial route (a very simple, but fast routing) and/or parasitic extraction might be run automatically prior to the timing analysis



```
-----------------------------------------------------------
          timeDesign Summary
-----------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):| -0.047  | -0.047  |  0.303  | 25.674  |   N/A   |  0.042  |
|           TNS (ns):| -4.673  | -4.673  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|   305   |   305   |    0    |    0    |   N/A   |    0    |
|          All Paths:|  3375   |  3302   |   47    |   24    |   N/A   |   12    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 100.000%
```

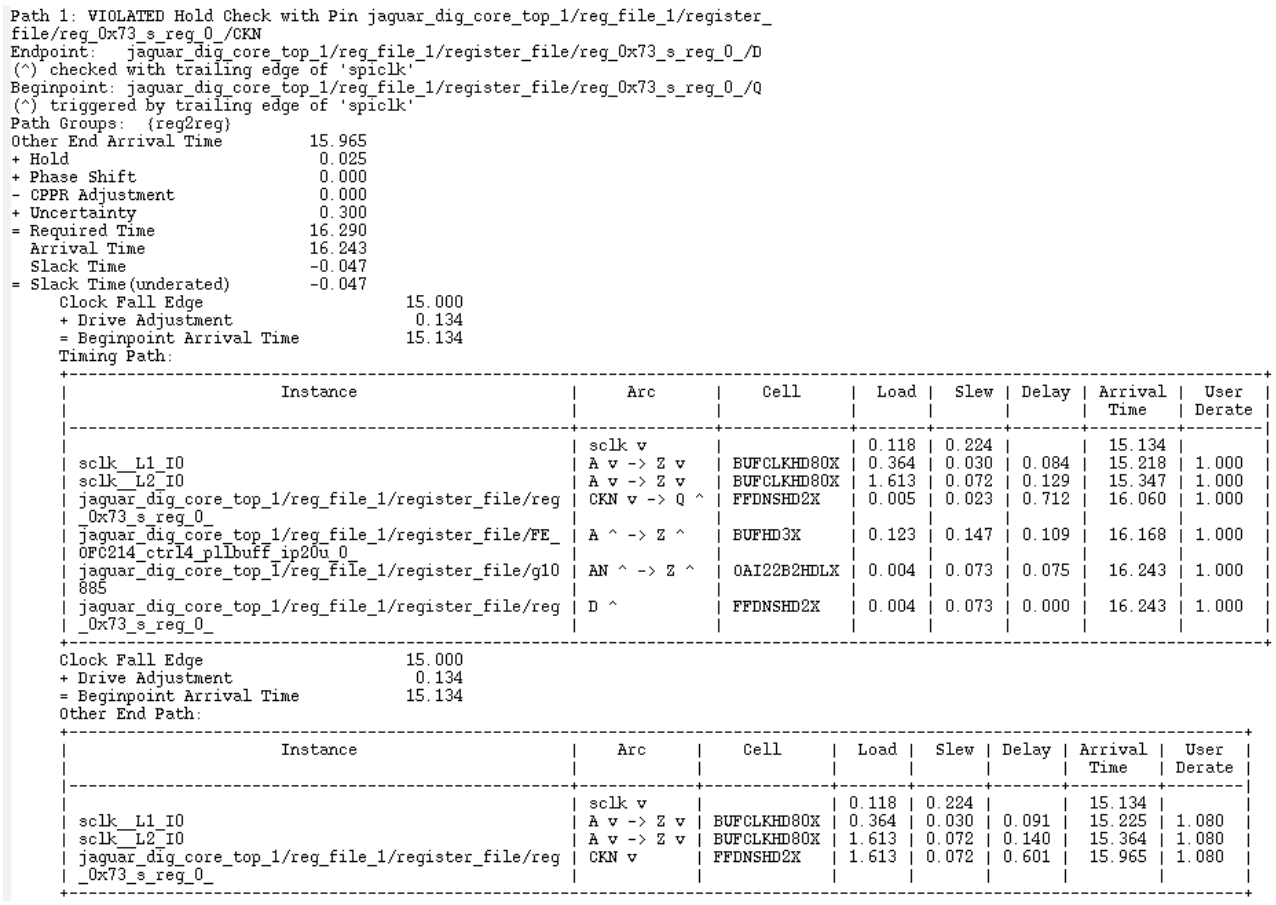
Figure 5 Hold time violations

The summary gives a very good overview of the current design timing. Some explanations:

- The analysis was run in setup mode or in hold mode as written in the first cell in the table i.e. setup time checks were performed but no hold time checks or vice versa.
- The columns contain numbers for all path in the design (ALL) or for specific path groups, e.g. reg2reg for all register to register paths.
- Worst negative slack (WNS) reports the slack for the most critical path. Negative numbers mean that the constraints are violated by this value.
- Total negative slack (TNS) is the sum of WNS for all violating paths. Together with the number of violating paths this figure helps to see how severe the violations are.
- Real/Total DRV in the setup time violation show (electrical) design rule violations, some libraries have a maximum transition time for all nets. The report above shows that 368 nets have a transition violation (the signal takes too long to change from logic-1 to logic-0 or vice versa). In addition 187 nets have a maximum capacitance violation (the total amount of capacitance driven by a net exceeds the limit set by the design library). These violations are mostly related to excessive parasitic capacitance due to interconnections, and generally cause timing violations as well. However, even if a DRV does not cause a timing violation it needs to be fixed.
- DENSITY and ROUTING OVERFLOW show the placement utilization and routing resources, i.e. are a measure for the feasibility of the current floor-plan/placement.

As shown in the figure below the detailed timing report for a violation path in the design and it has:

- End point and Begin point which describe the full path
- The triggering clock that drive the path sequential gates
- The required time for no violation the arrival time
- The difference between them which is the slack time (negative slack time mean a real violation).
- The slack time underated which is the slack time minus the a margin set by the user
- A timing table contain the detailed delays added by each gate in the path
- Other End path table describe the clock timing from the nearest common point to each flip-flop at the beginning and the end of the path.



```
Path 1: VIOLATED Hold Check with Pin jaguar_dig_core_top_1/reg_file_1/register_
file/reg_0x73_s_reg_0_/CKN
Endpoint:   jaguar_dig_core_top_1/reg_file_1/register_file/reg_0x73_s_reg_0_/D
(^) checked with trailing edge of 'spiclk'
Beginpoint: jaguar_dig_core_top_1/reg_file_1/register_file/reg_0x73_s_reg_0_/Q
(^) triggered by trailing edge of 'spiclk'
Path Groups:  {reg2reg}
Other End Arrival Time         15.965
+ Hold                          0.025
+ Phase Shift                   0.000
- CPPR Adjustment               0.000
+ Uncertainty                   0.300
= Required Time                16.290
  Arrival Time                 16.243
  Slack Time                   -0.047
= Slack Time(underated)        -0.047
     Clock Fall Edge                     15.000
     + Drive Adjustment                   0.134
     = Beginpoint Arrival Time           15.134
     Timing Path:
     +-----------------------------------------------------------------------------------------------------------------------------+
     |                        Instance                        |      Arc       |    Cell     |  Load |  Slew | Delay | Arrival |  User  |
     |                                                        |                |             |       |       |       |  Time   | Derate |
     |--------------------------------------------------------+----------------+-------------+-------+-------+-------+---------+--------|
     |                                                        | sclk v         |             | 0.118 | 0.224 |       |  15.134 |        |
     | sclk__L1_I0                                            | A v -> Z v     | BUFCLKHD80X | 0.364 | 0.030 | 0.084 |  15.218 | 1.000  |
     | sclk__L2_I0                                            | A v -> Z v     | BUFCLKHD80X | 1.613 | 0.072 | 0.129 |  15.347 | 1.000  |
     | jaguar_dig_core_top_1/reg_file_1/register_file/reg     | CKN v -> Q ^   | FFDNSHD2X   | 0.005 | 0.023 | 0.712 |  16.060 | 1.000  |
     | _0x73_s_reg_0_                                         |                |             |       |       |       |         |        |
     | jaguar_dig_core_top_1/reg_file_1/register_file/FE_     | A ^ -> Z ^     | BUFHD3X     | 0.123 | 0.147 | 0.109 |  16.168 | 1.000  |
     | OFC214_ctrl4_pllbuff_ip20u_0_                          |                |             |       |       |       |         |        |
     | jaguar_dig_core_top_1/reg_file_1/register_file/g10     | AN ^ -> Z ^    | OAI22B2HDLX | 0.004 | 0.073 | 0.075 |  16.243 | 1.000  |
     | 885                                                    |                |             |       |       |       |         |        |
     | jaguar_dig_core_top_1/reg_file_1/register_file/reg     | D ^            | FFDNSHD2X   | 0.004 | 0.073 | 0.000 |  16.243 | 1.000  |
     | _0x73_s_reg_0_                                         |                |             |       |       |       |         |        |
     +-----------------------------------------------------------------------------------------------------------------------------+
     Clock Fall Edge                     15.000
     + Drive Adjustment                   0.134
     = Beginpoint Arrival Time           15.134
     Other End Path:
     +-------------------------------------------------------------------------------------------------------------------------+
     |                        Instance                        |     Arc    |    Cell     |  Load |  Slew | Delay | Arrival |  User  |
     |                                                        |            |             |       |       |       |  Time   | Derate |
     |--------------------------------------------------------+------------+-------------+-------+-------+-------+---------+--------|
     |                                                        | sclk v     |             | 0.118 | 0.224 |       |  15.134 |        |
     | sclk__L1_I0                                            | A v -> Z v | BUFCLKHD80X | 0.364 | 0.030 | 0.091 |  15.225 | 1.080  |
     | sclk__L2_I0                                            | A v -> Z v | BUFCLKHD80X | 1.613 | 0.072 | 0.140 |  15.364 | 1.080  |
     | jaguar_dig_core_top_1/reg_file_1/register_file/reg     | CKN v      | FFDNSHD2X   | 1.613 | 0.072 | 0.601 |  15.965 | 1.080  |
     | _0x73_s_reg_0_                                         |            |             |       |       |       |         |        |
     +-------------------------------------------------------------------------------------------------------------------------+
```

Figure 6 Violating path report

- ## Optimization

In order to (better) meet the constraints, CADENCE SOC ENCOUNTER can try to optimize the design at every stage of the design process. Although the netlist delivered by the synthesis tool had no timing violations. This is due to differences in interconnect parasitics between the two tools. While the synthesis tool relies on an estimate (statistical model based) CADENCE SOC ENCOUNTER can use the real placement and (trialrouting) at hand.

During optimization CADENCE SOC ENCOUNTER can select different drive strengths for cells, add/remove buffers and inverters, move instances or even restructure part of the logic (just like synthesis does).

Optimization is done using iterations of timing analysis, optimization, trial-route and parasitic extraction.

As a last step CADENCE SOC ENCOUNTER performs a timing analysis on the optimized design, prints the summary to the console and writes the detailed reports to the timingReports directory.

But what happens if we cannot fix the violations with optimization? First make sure to understand what your constraints are and why they are violated. Often there are errors in converting the design specifications to constraints (e.g. is the input delay really 3.5 ns? Also for this pin?) and describing them properly with the commands available. If you still have problems, there are three levels where you can reach a solution:

○ Optimization during backend design (CADENCE SOC ENCOUNTER)

CADENCE SOC ENCOUNTER can optimize the design at every stage of the design process. In general, the earlier the stage, the more changes can be done, e.g. PRE-CTS optimization has much more flexibility than POST-ROUTE optimization. At the PRE-CTS stage registers can be moved and resized, this will no longer be possible after clock tree insertion. On the other hand, the parasitic interconnect information is much more accurate with later stages of design, so the timing information (and hence the optimization goals) will be more accurate.

We can (re)run the optimization at various stages, try a new placement or even start with a new floor-plan. It is impossible to give general guidelines, you will have to see what works best for your design. If you are far from meeting your target (e.g. for a 10 ns clock, if after all optimizations you still have a timing violation of 2 ns), you may need to go back to synthesis.

○ Optimization during synthesis

Once you have tried to place and route a netlist you will get a better idea about the relationship between synthesis results and back-end results (area and timing wise). You may use this information to adjust the timing constraints and re-synthesize the circuit.

○ Architectural optimizations

If nothing else helps, you will have to modify your architecture. During this iteration you will have a much better idea about what is critical for your circuit.

If all of the above fails, you will have to see if the specifications could be changed