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Fault Tolerant Computing and VLSI Testing

Lab 1

1.

Circuit name	Number of stuck-at faults	No of test patterns	Test coverage
C432	812	35	90.59
C499	1130	61	100
C880	1376	32	100
C1355	1294	75	100
C1908	892	34	100

Note with C1908 that two faults were undetected. The 100% coverage is due to the fact that Tetramax rounds to two decimal places.

2.

Circuit name (combinational logic only)	Number of stuck-at faults	No of test patterns	Test coverage
Full adder	32	5	100
4 bit	116	8	100
8 bit	228	11	100
16 bit	452	12	100
32 bit	900	17	100
64 bit	1796	22	100

3.

Circuit name	Number of stuck-at faults	No of test patterns	Test coverage
s298	510	21	97.04
s344	634	13	97.3
s349	634	13	97.3
s382	756	38	95.61
s386	576	15	79.37

4.

Command	Example
read_netlist	read_netlist ./verilog_simulation_models/*.v
run_build_model	run_build_model s27
add_clocks	add_clocks 0 CK
write_drc_file	write_drc_file ./s27.spf -replace
run_drc	run_drc ./s27.spf
set_atpg	set_atpg -merge medium
set_faults	set_faults -model stuck
add_faults	add_faults -all
run_atpg	run_atpg full_sequential_only
report_summaries	report_summaries
report_faults	report_faults -all
report_patterns	report_patterns -all
write_patterns	write_patterns s27_ATPG.wgl -format WGL