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Fault Tolerant Computing and VLSI Testing

Lab 1

1. Above questions:

   - How many scan cells do you have? 3
   - How many rule violations do you have? 0
   - How many scan chains will you have? 1
   - How much is the area overhead of scan? 23.4%
   - How much is the timing overhead of scan? 4.7%
   - What type of DFF before dft_compiler? reg
   - What type of DFF after dft_compiler? HDSDFPQ1
   - What two pins did dft_compiler add? test_si, test_se

2.

Circuit name	Area without scan chain	Area with scan chain
s298	1380.55	1483.78
s344	1509.57	1664.41
s349	1509.57	1664.41
s382	1899.87	2170.83
s386	1077.34	1154.76

3.

Circuit name (registered inputs and outputs)	Area without scan chain	Area with scan chain
Full adder	280.63	332.24
4 bit	503.20	496.75
8 bit	825.75	941.88
16 bit	1599.90	1819.25
32 bit	3148.19	3573.98
64 bit	6244.76	7083.46

4.

Command	Example
create_clock	create_clock -period 10 CK
current_design	current_design s27
compile	compile -scan
set_dft_signal	set_dft_signal -view existing_dft -type ScanClock -port CK -timing [list 40 60]
create_test_protocol	create_test_protocol
dft_drc	dft_drc
set_scan_configuration	set_scan_configuration -chain_count 1
insert_dft	insert_dft
write	write -format verilog -hierarchy -output s27_dft.v
report_area	report_area
report_timing	report_timing
report_power	report_power