Fault Tolerant Computing Individual Project
Modeling and Synthesis of a Fault Tolerant RISC CPU

Objectives: Model a fault tolerant block in RISC processor (MIPS) and synthesize it using Synopsis tools.

Given: Complete description of the processor including test bench in Verilog.

Report

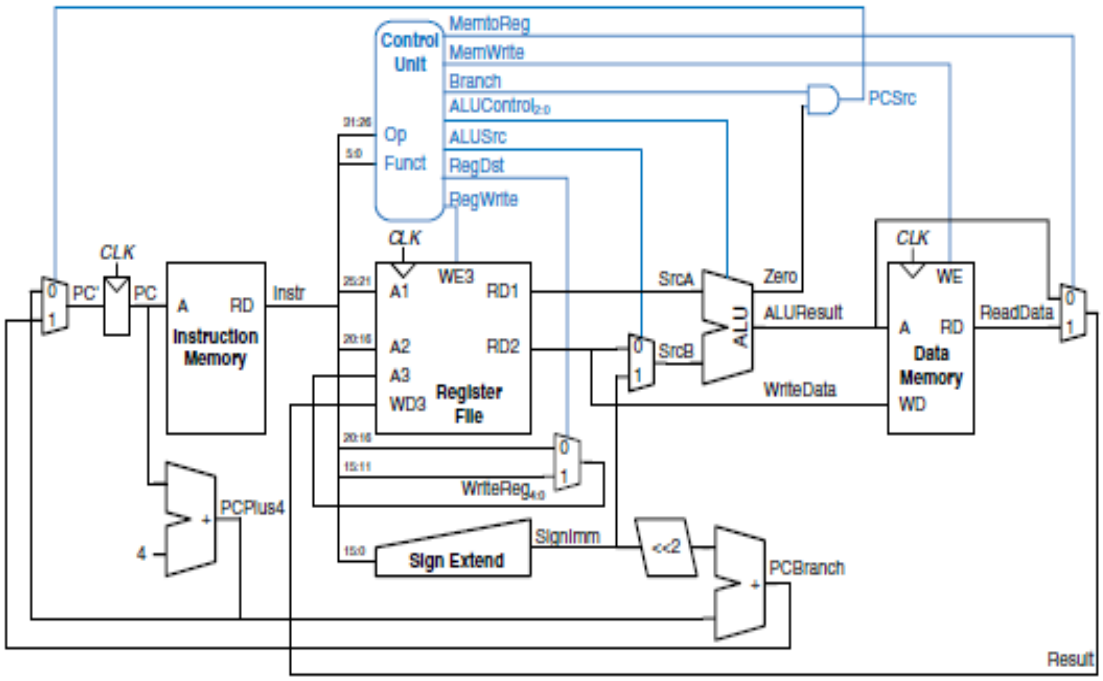
The report should be a comprehensive document of what you have done.

Your final report should include

(1) Minimum and maximum slack of your design (compare with original)
(4) Area/Time and power overhead
(5) Your script
(6) Lessons learned from the project
(7) Conclusion

Your submission must contain:

- The source code of your design/testbench) - reasonably well documented.


MemtoReg
MemWrite
Branch
ALUControl2:0
ALUSrc
RegDst
RegWrite
Control Unit
Op
Funct
31:26
5:0
PCSrc
CLK
PC'
PC
A
RD
Instruction Memory
Instr
25:21
20:16
A1
A2
A3
WD3
WE3
RD1
RD2
Register File
SrcA
SrcB
ALU
Zero
ALUResult
WriteData
WE
Data Memory
WD
ReadData
15:11
WriteReg4:0
PCPlus4
4
15:0
Sign Extend
SignImm
<<2
PCBranch
Result