Analog Circuits Course Project

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Submitted to
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Aim

Design of cascode amplifier and cascode current mirror in schematic and layout using LTspice and Magic tools in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier, and cascode current mirror in 22 nm (supply 1 V) technology node to see the effect of lowering the technology node.

Circuit Diagrams

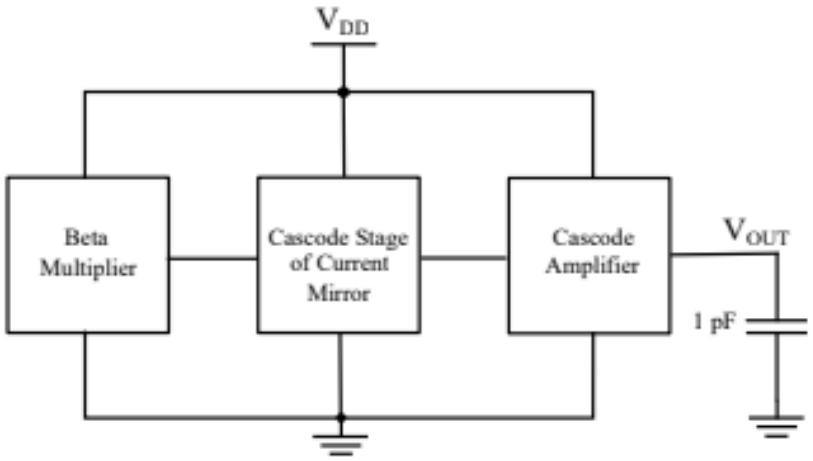


Figure 1: Block diagram of cascode amplifier with other blocks

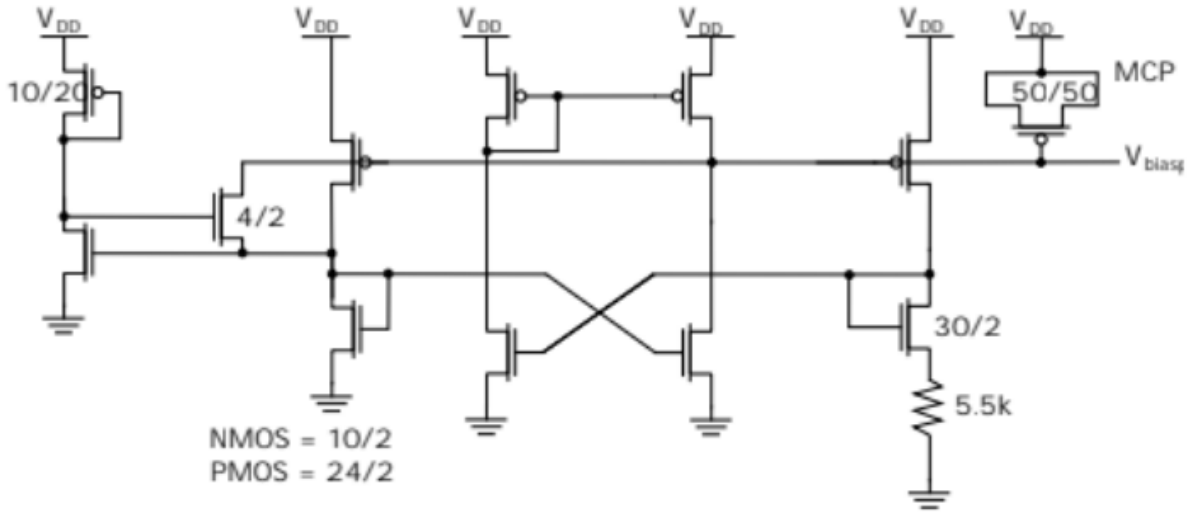


Figure 2: Circuit for beta multiplier circuit

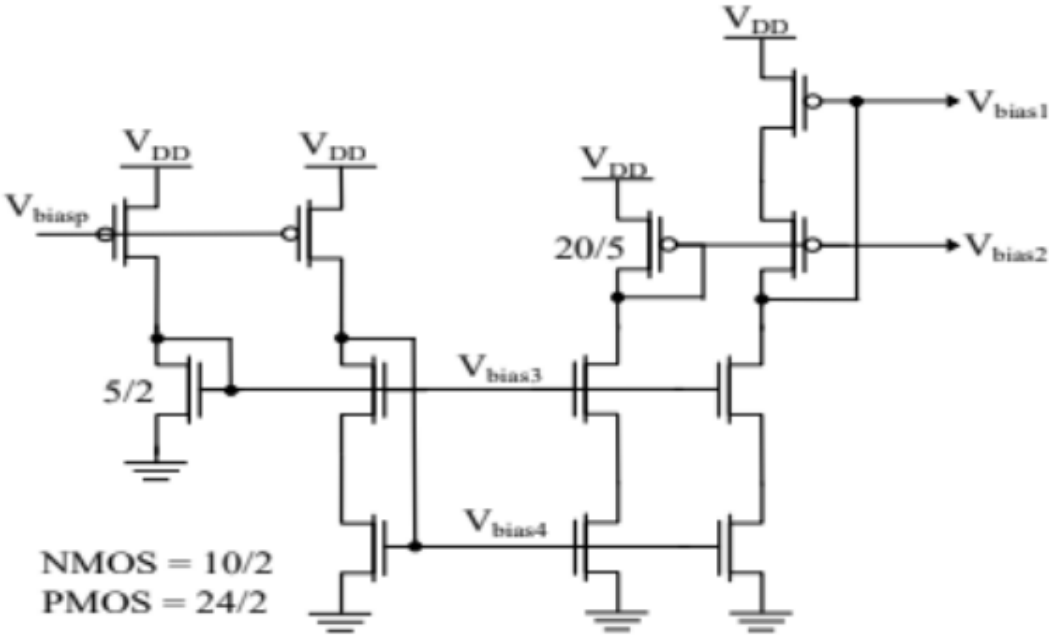


Figure 3: Circuit for cascode current mirror

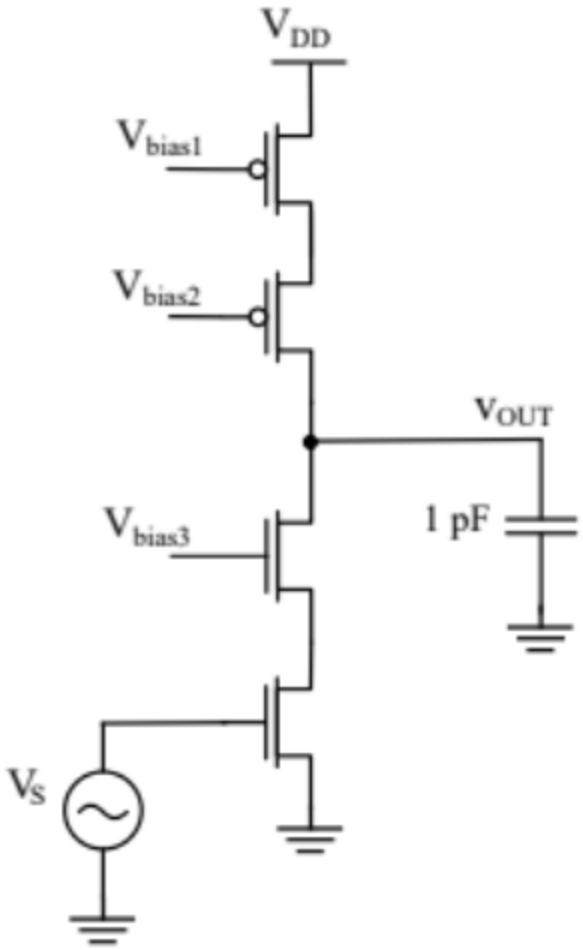
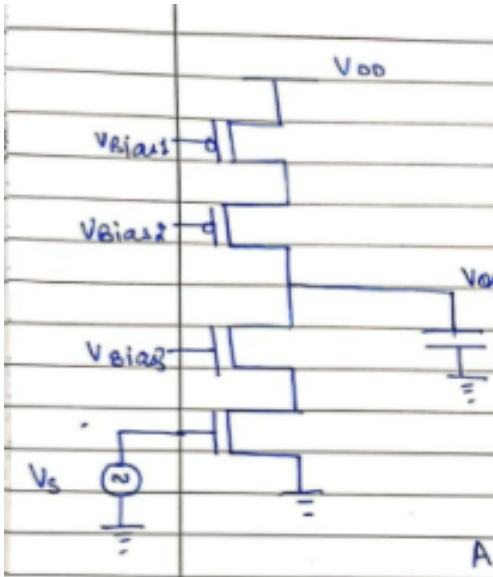


Figure 4: Circuit for cascode amplifier

Hand Calculations

For 180nm



let frequency → 1.25MHz

$f = \frac{1}{2\pi RC}$

$1.25M \Rightarrow \frac{1}{2\pi R_{out}(10^{-12})}$

$R_{out} \Rightarrow 127323.954$

V_{TH} (given) $\Rightarrow 0.6\,V$

$A_V = 20$

$A_v = g_m R_{out}$ —(i)

$\frac{20}{127323.954} = g_m$

$g_m = 0.000157\,07$ —(ii)

$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_{TH})$ —(iii)

$\frac{\mu_n C_{ox}}{2} = 175.4\,\mu$

$\frac{\mu_p C_{ox}}{2} = 35.6\,\mu$

$V_{GS} - V_{TH} \leq V_{DS}$ (saturation)

$V_{GS} - 0.6 \leq 0.2$

$V_{GS} \leq 0.8\,V$

let $V_{GS} = 0.7\,V$ —(iv)

put (iv) in (iii)

$0.000157\,07 = (175.4)(2)\left(\frac{W}{L}\right)(0.7 - 0.6)$

$\frac{W}{L} = \frac{0.000157\,07}{350.8 \times 10^{6} \times 0.1} =$

$\left(\frac{W}{L}\right)_{NMOS} \Rightarrow 4.48 \longrightarrow (1)$

$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{Tn})^2$

$= (175.4)(4.48)(0.1)^2 \times 10^{-6}$

$\boxed{I_D = 7.85\,\mu A}$

Now, for PMOS2,

$V_{SG} - V_{Tn} \geq V_{DS}$ (saturation)

$V_G - V_S - V_{Tn} \geq V_{DS}$

$V_G - (1.6) - (-0.6) \geq -0.1$

$V_{Bias2} - 1 \geq -0.1$

$\boxed{V_{Bias2} = 0.9V}$

Now (PMOS1)

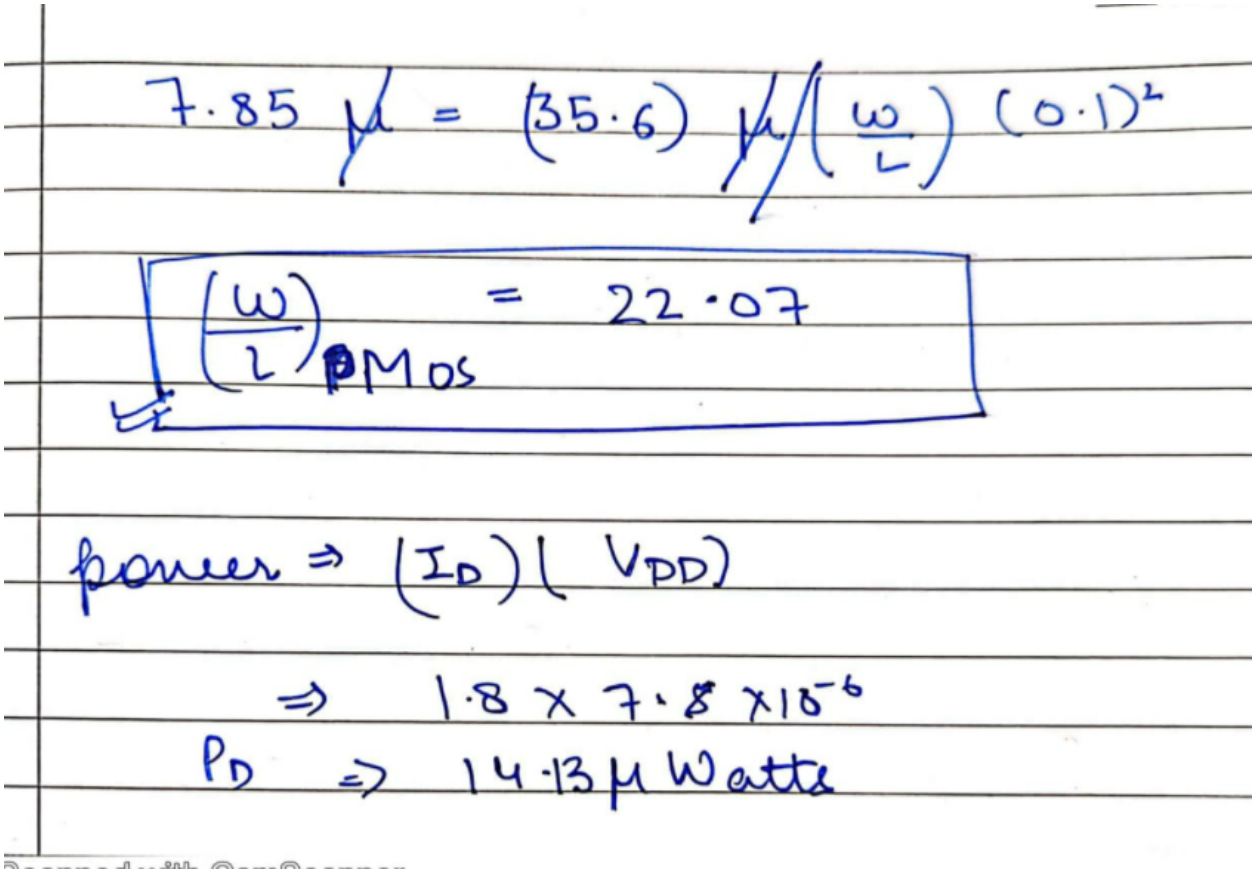
$V_G - V_S - V_{Tn} \geq V_{DS}$

$V_{Bias1} - 1.8 - (-0.6) \geq -0.1$

$\boxed{V_{Bias1} \Rightarrow 1.1V}$

Since, I_D is same for all, $I_D = \frac{1}{2}\mu_p C_{ox}(V_{SG} - V_{Tn})^2$ eq (1)

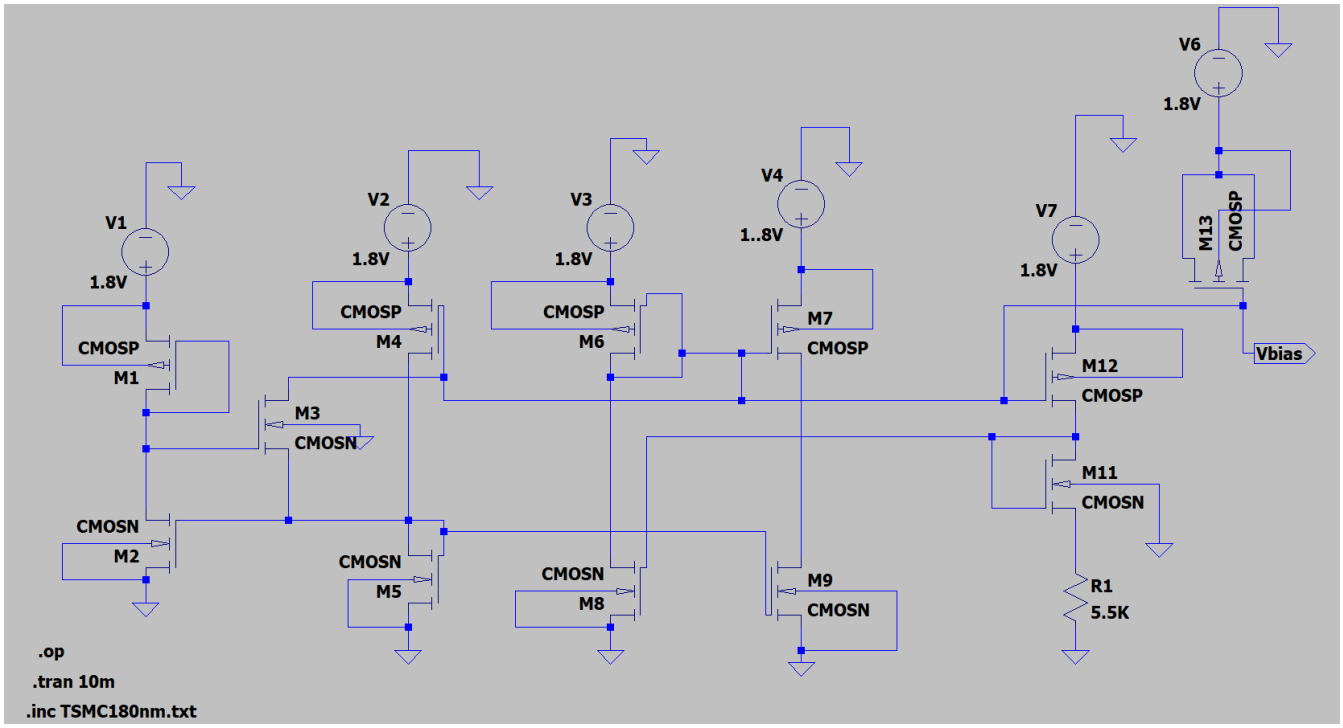
$7.85\,\mu = \frac{1}{2}(\mu_p C_{ox})\left(\frac{W}{L}\right)(V_{SG} - V_{Tn})^2$



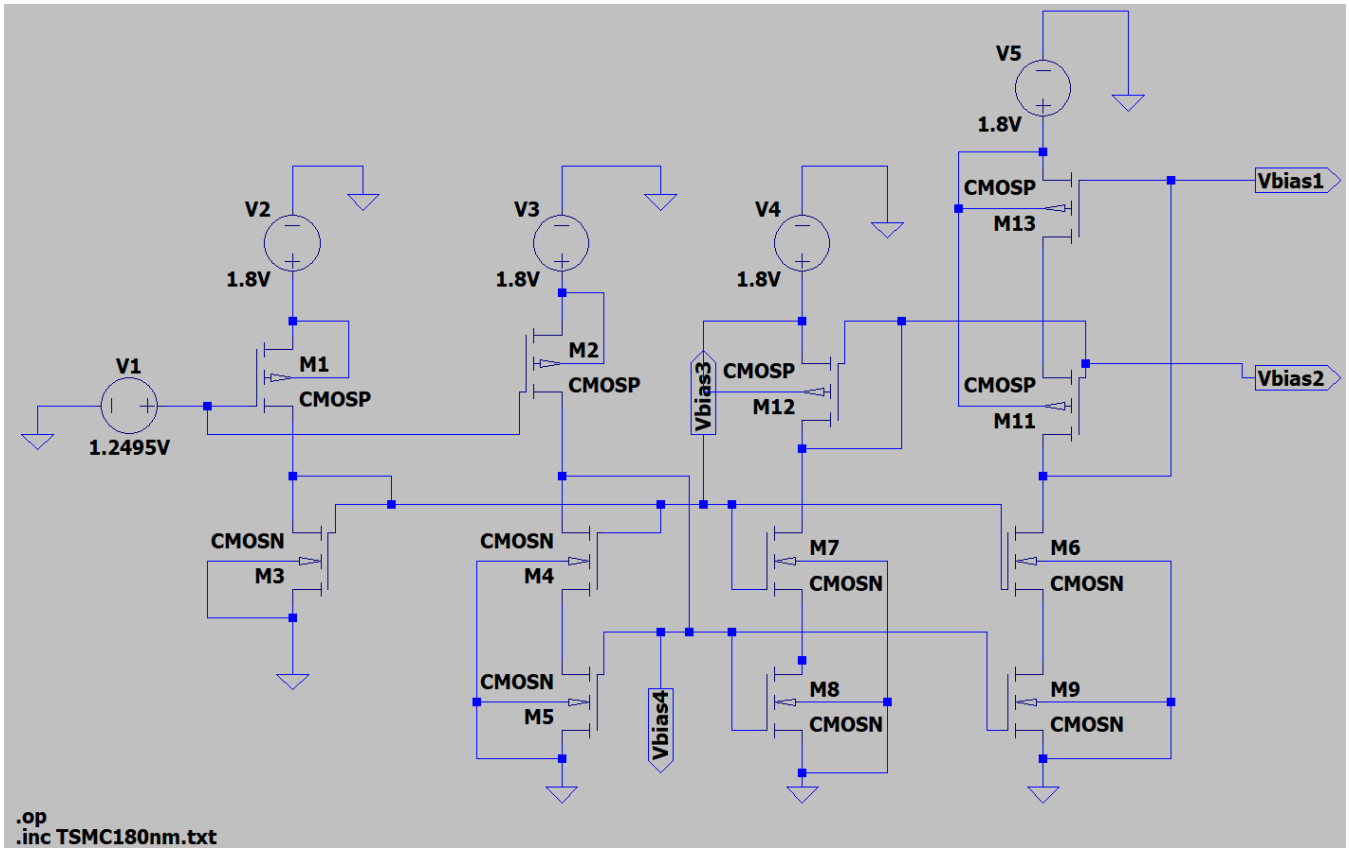
Schematic (LTSpice)

I. 180nm

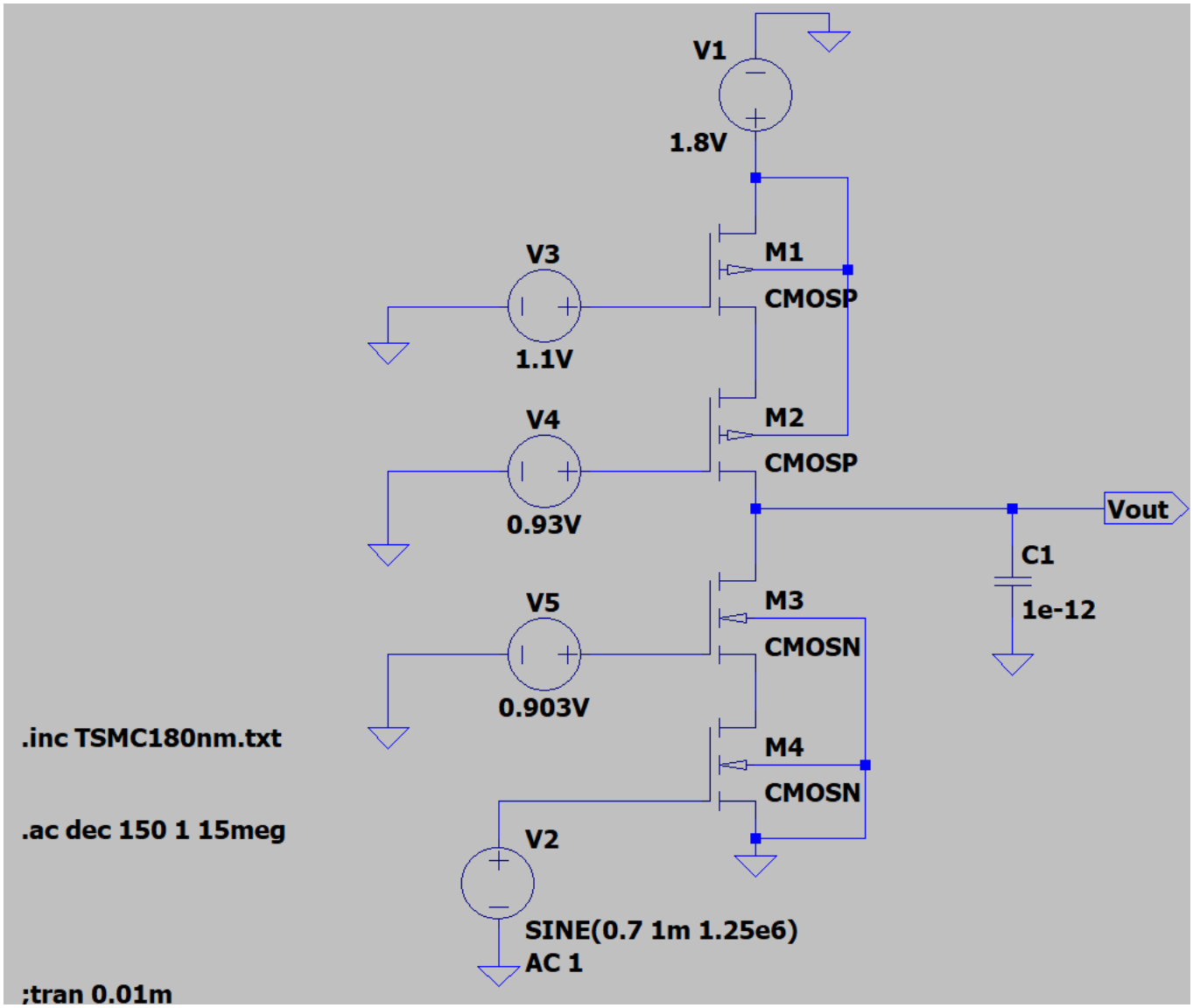
A. Diagrams



Beta Multiplier

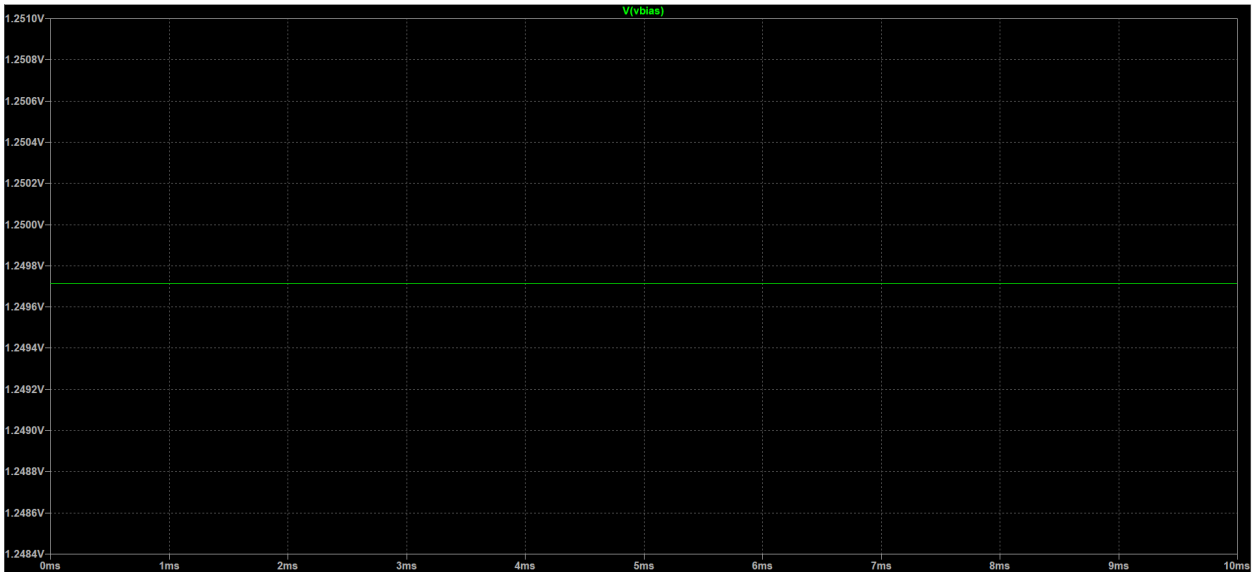


Current Mirror



Cascode Amplifier

B. Graphs



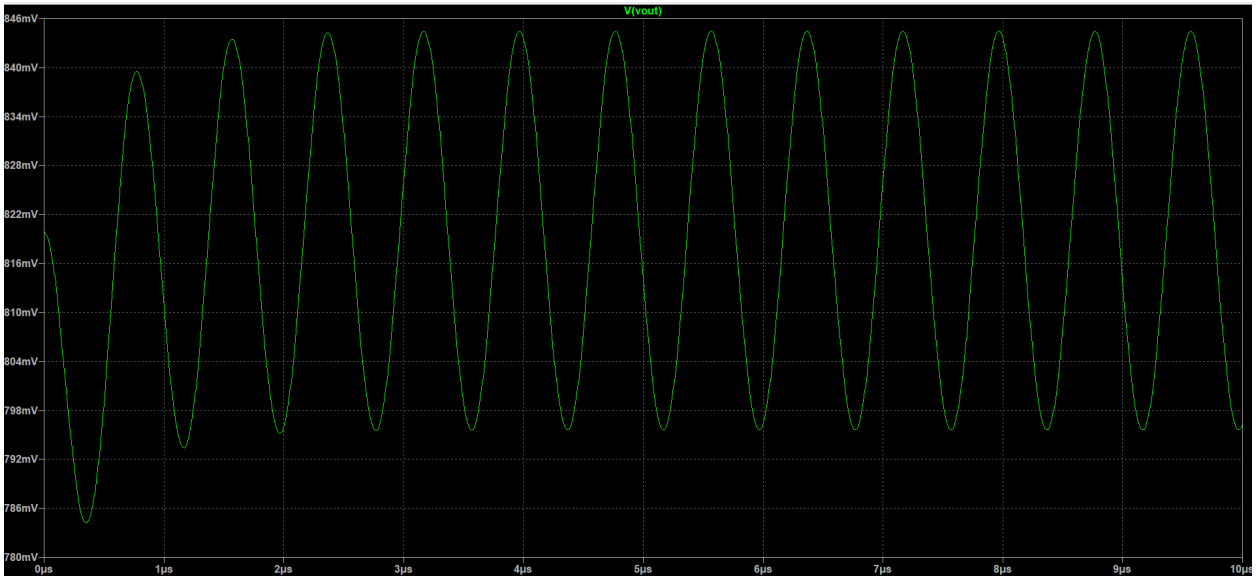
The result of beta multiplier resulted in a value of nearly 1.25Volts.

Tuned values of Vbias1, Vbias2 and Vbias3 on the current mirror circuit using the values from the amplifier circuit being displayed here. We calculated the Vbias1, Vbias2 and Vbias3 in the hand calculations, using a frequency of 1.25MHz. Through this, we used the saturation conditions to find the respective voltages and finally calculated the (W/L) ratios of PMOS and NMOS.

The voltages we calculated from this we used as reference voltages to what we wanted in this circuit. We did this by varying the (W/L) figurines and managed to get the desired voltages.

* C:\Users\AENA\Dropbox\My PC (DESKTOP-9EOALJ3)\Desktop\analog project\2nd.asc

```
      --- Operating Point ---

V(n006):        1.2495          voltage
V(n003):        1.8             voltage
V(n002):        1.8             voltage
V(vbias3):      0.900378        voltage
V(n007):        0.284085        voltage
V(vbias4):      0.541365        voltage
V(vbias2):      0.926934        voltage
V(n008):        0.288282        voltage
V(vbias1):      1.10367         voltage
V(n009):        0.289764        voltage
V(n005):        1.55514         voltage
V(n001):        1.8             voltage
V(n004):        1.8             voltage
Id(M2):         5.5484e-006     device_current
Ig(M2):         -0              device_current
Ib(M2):         1.26864e-012    device_current
Is(M2):         -5.5484e-006    device_current
Id(M1):         5.31099e-006    device_current
Ig(M1):         -0              device_current
Ib(M1):         9.09622e-013    device_current
Is(M1):         -5.31099e-006   device_current
Id(M13):        -5.55871e-006   device_current
Ig(M13):        -0              device_current
Ib(M13):        2.54862e-013    device_current
Is(M13):        5.55871e-006    device_current
Id(M12):        -5.55604e-006   device_current
Ig(M12):        -0              device_current
```



Vout of the Cascode Amplifier

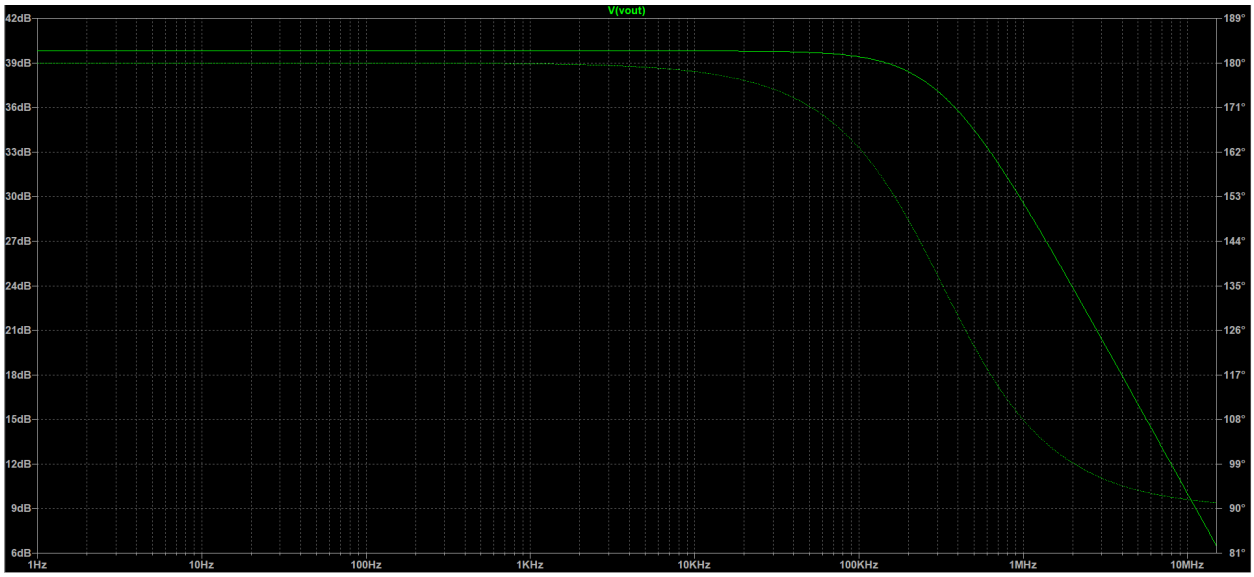
Frequency took: 1.25MHz

$Av = (Vout)/(Vin)$

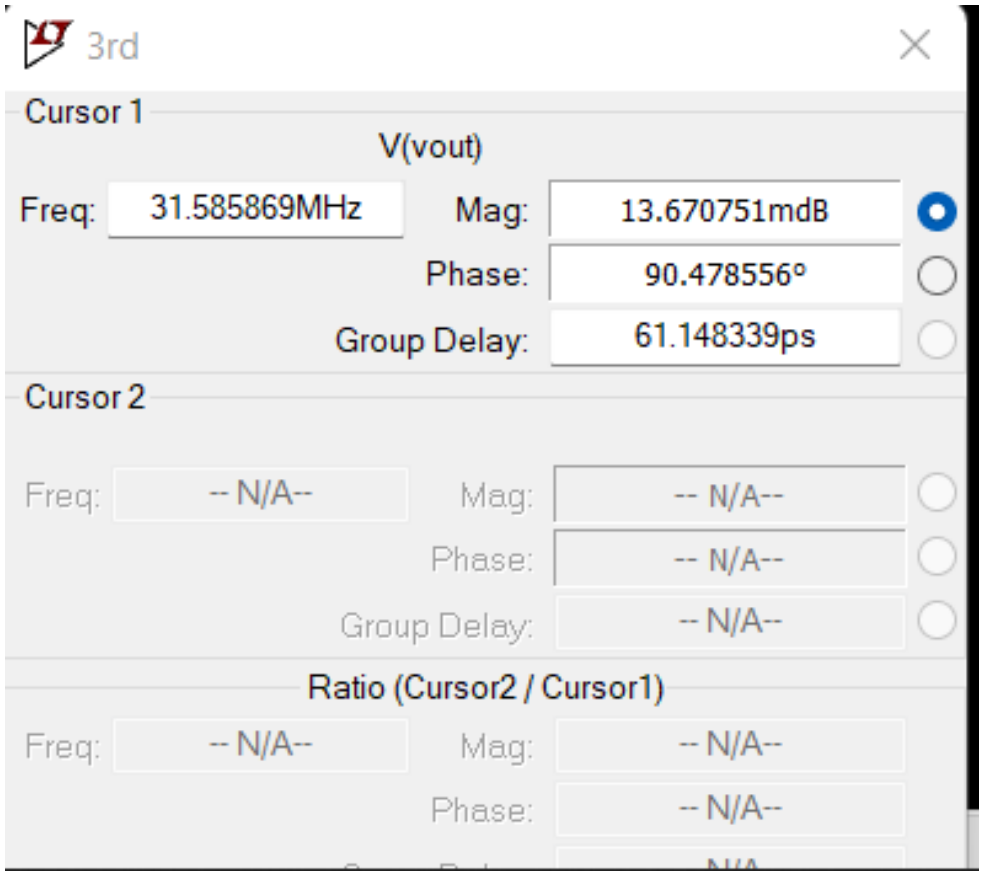
$Av = (845mV - 795mV)/(0.002)$

$Av = 25$ *(nearly)*

Current in the cascode amplifier(180nm) as came in the LTSpice results is 31.4 microamperes, which is a tad bit higher than the one calculated.



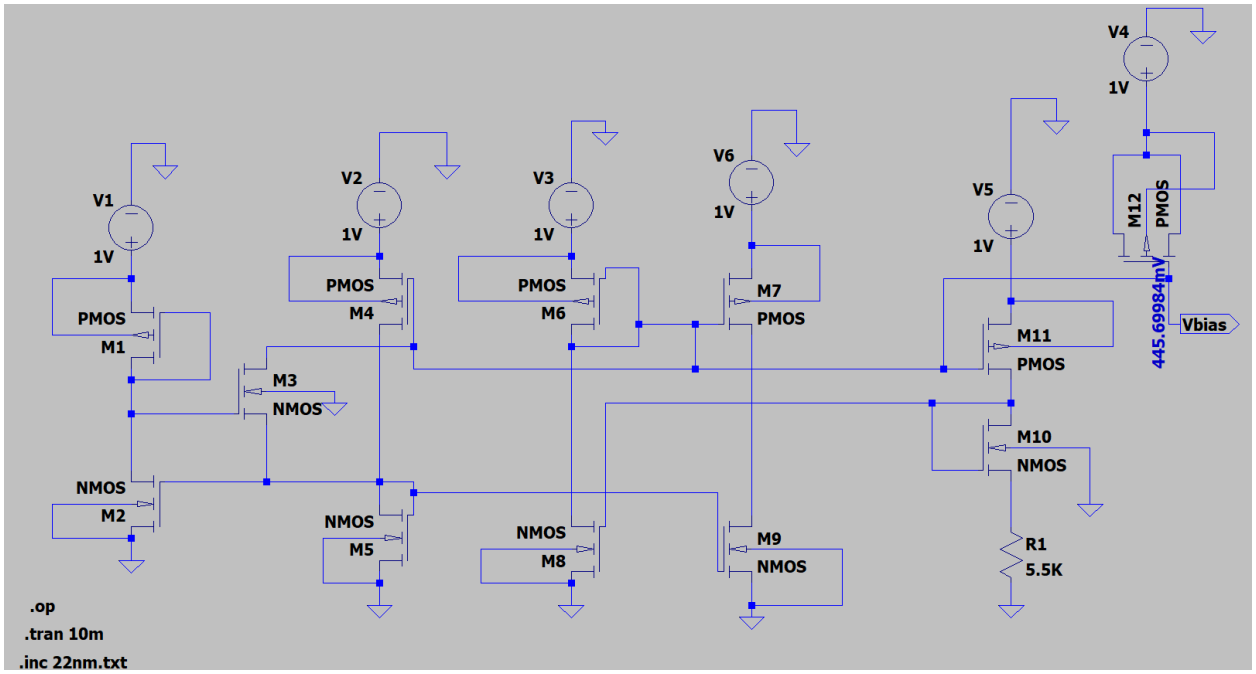
Bode plot(180nm)



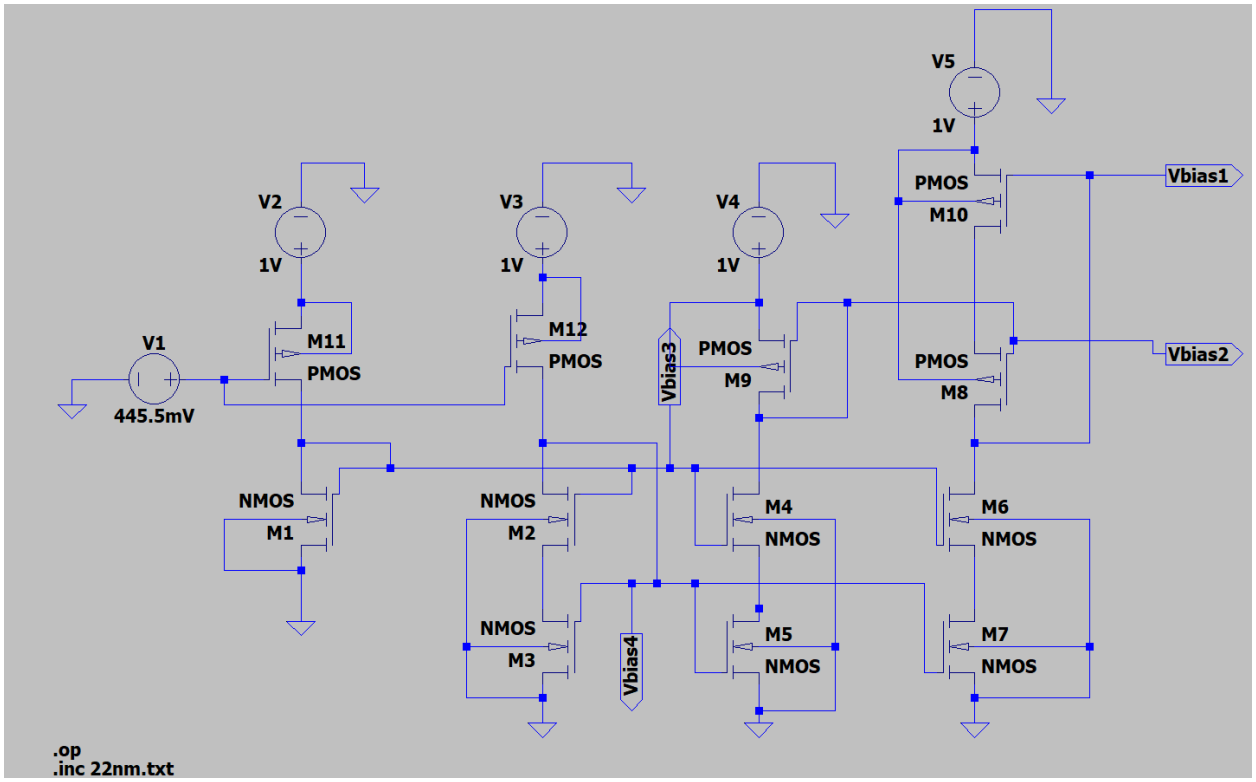
Zero dB frequency for 180nm bode plot

II. 22nm

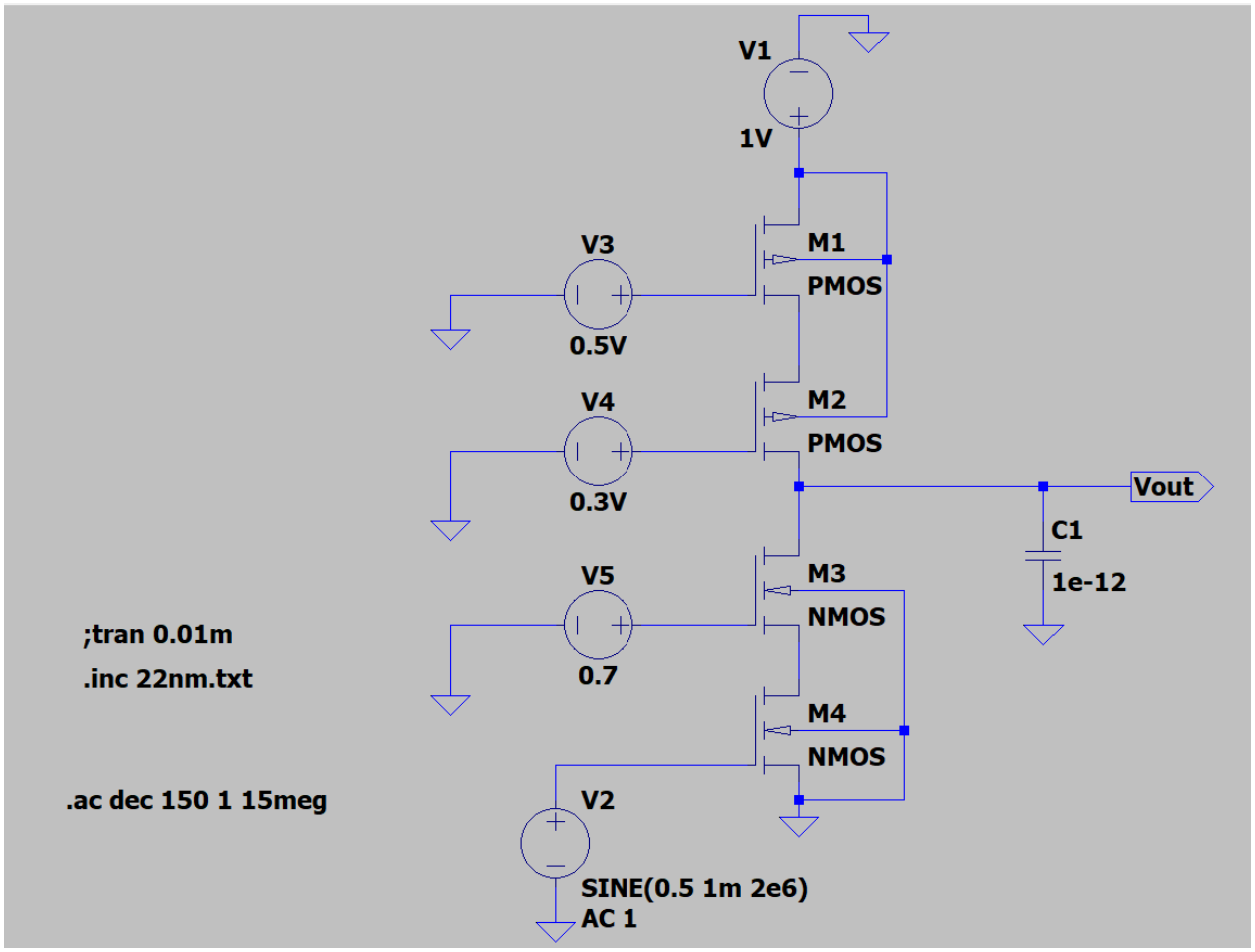
A. Diagrams



Beta multiplier circuit, showing the value of Vbias in 22nm.

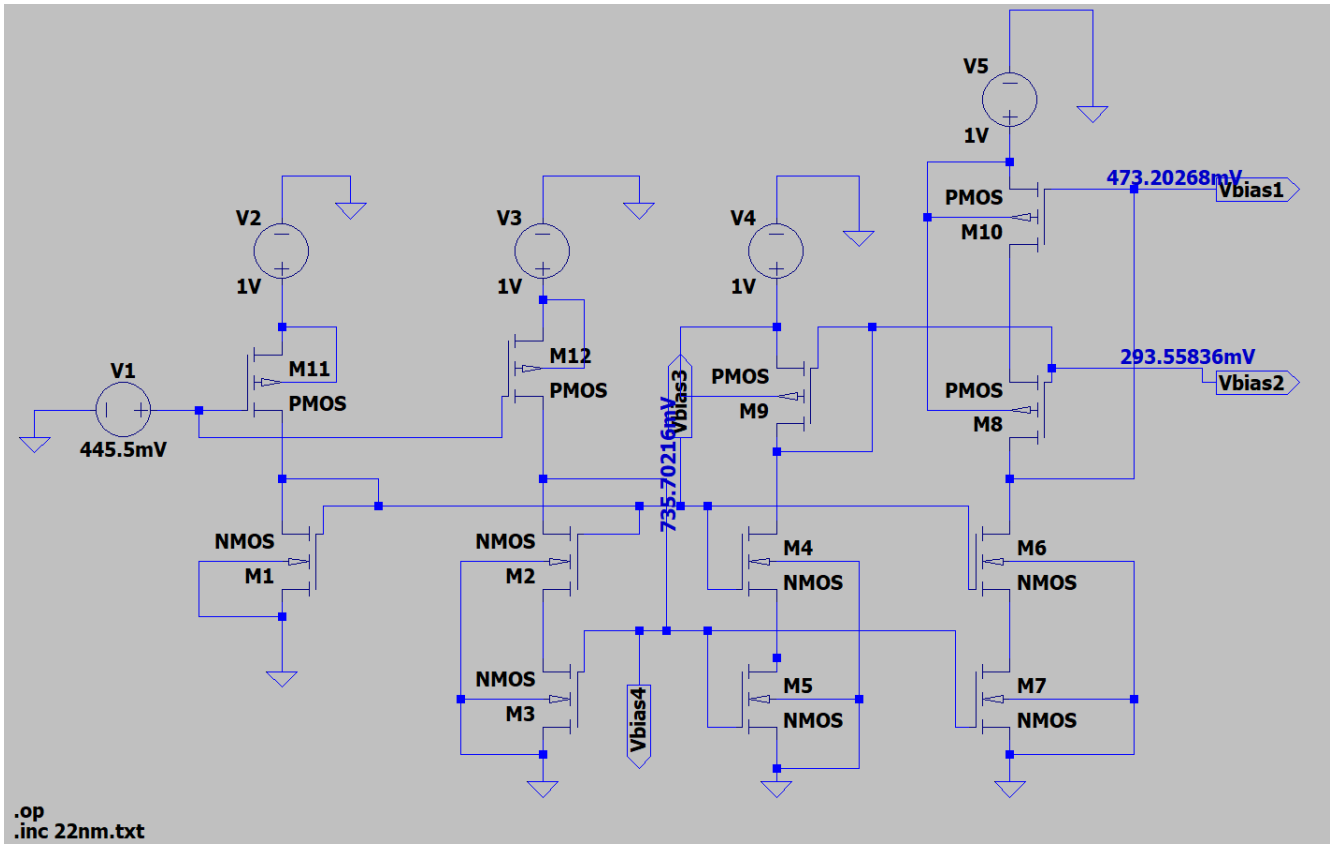


Circuit diagram of Current Mirror in 22nm



Circuit diagram of Cascode Amplifier (22nm)

B. Graphs

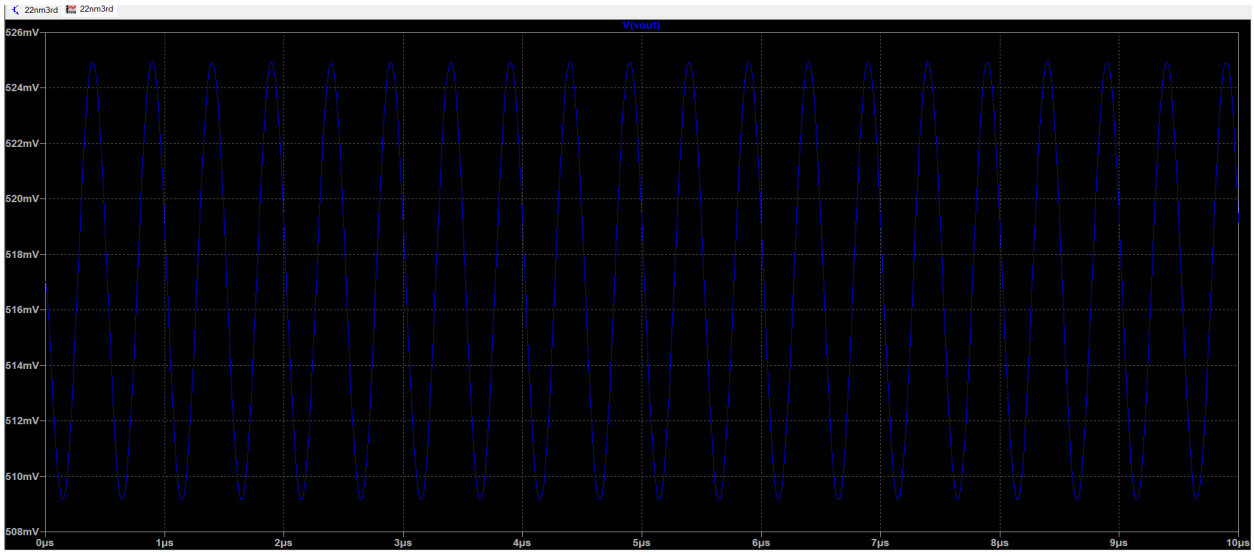


Circuit diagram showing the values of Vbias1, Vbias2 and Vbias3 after tuning them by varying their (W/L) ratios.

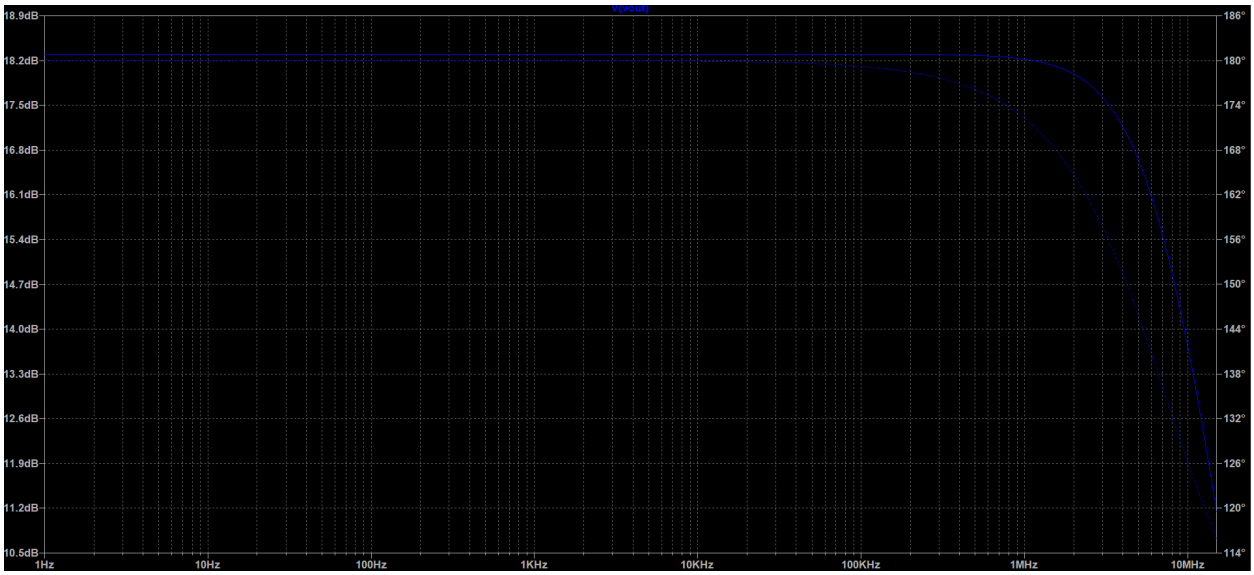
Frequency taken: 2 MHz

* C:\Users\AENA\Dropbox\My PC (DESKTOP-9EOALJ3)\Desktop\analog project\22nm2nd.asc

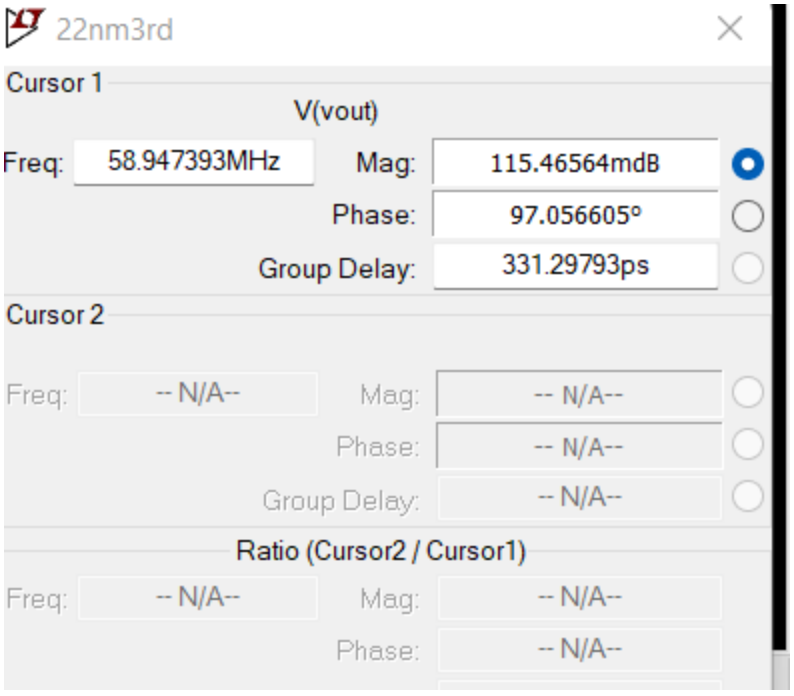
```
      --- Operating Point ---

V(n006):        0.4455          voltage
V(n003):        1               voltage
V(n002):        1               voltage
V(vbias3):      0.735702        voltage
V(n007):        0.0684897       voltage
V(vbias4):      0.909835        voltage
V(vbias2):      0.293558        voltage
V(n008):        0.0618369       voltage
V(vbias1):      0.473203        voltage
V(n009):        0.0340441       voltage
V(n005):        0.999997        voltage
V(n001):        1               voltage
V(n004):        1               voltage
V(m12#dbody):   1               voltage
V(m12#sbody):   1               voltage
V(m11#dbody):   1               voltage
V(m11#sbody):   1               voltage
V(m10#dbody):   0.999998        voltage
V(m10#sbody):   0.999998        voltage
V(m9#dbody):    1               voltage
V(m9#sbody):    1               voltage
V(m8#dbody):    1               voltage
V(m8#sbody):    1               voltage
V(m7#dbody):    1.77945e-010    voltage
V(m7#sbody):    1.77635e-010    voltage
V(m6#dbody):    6.075e-012      voltage
V(m6#sbody):    2.70645e-012    voltage
```



The current in the cascode amplifier(22nm), as in the LTSpice results, is 37.5 microampere.



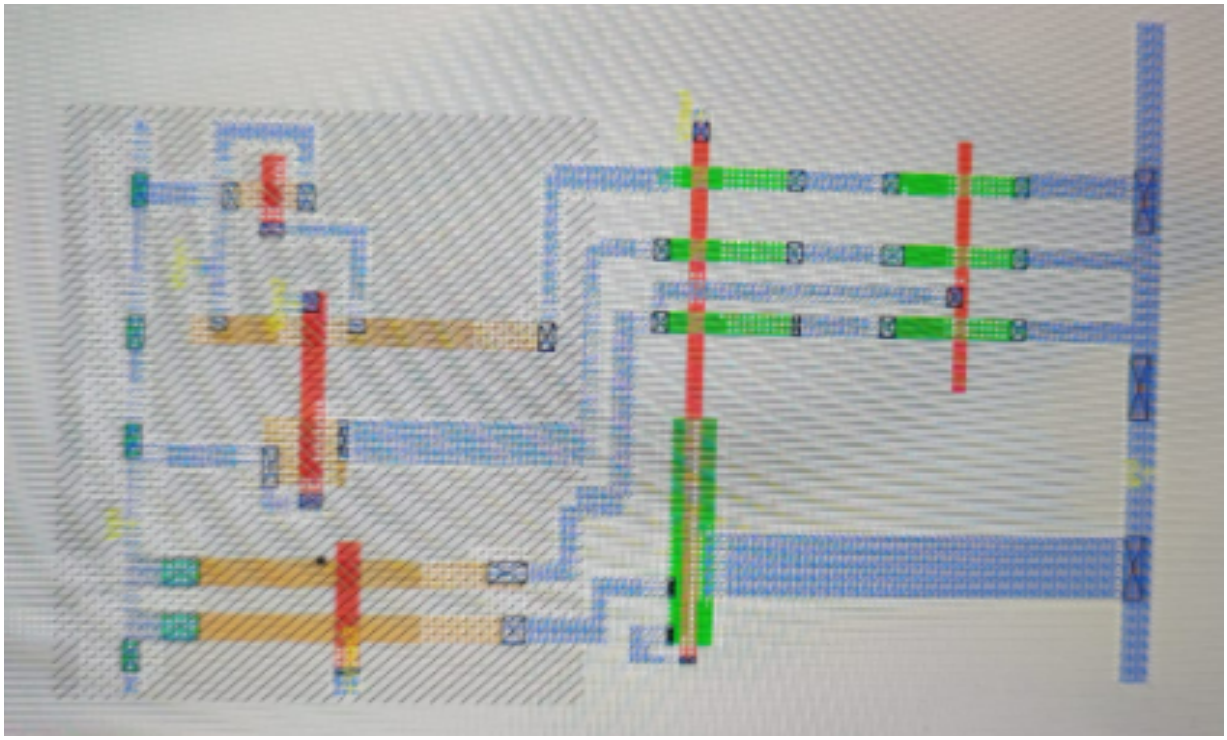
Bode Plot

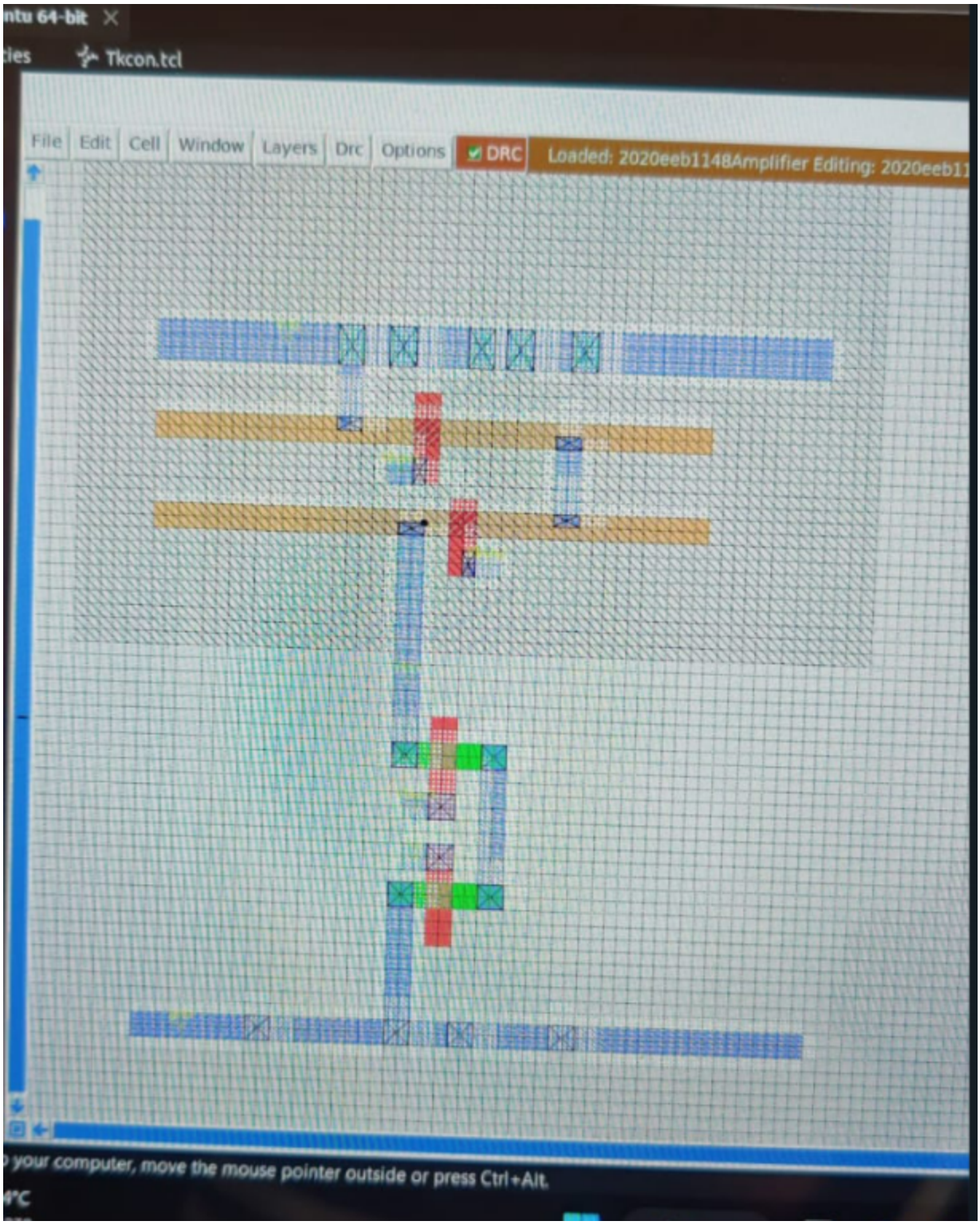


The Zero dB frequency

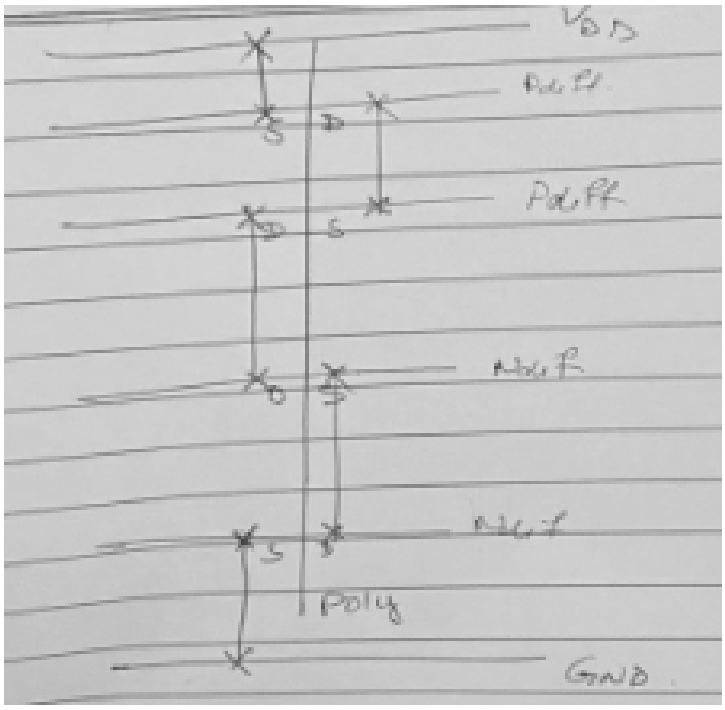
Layout (Magic)

Made the stick diagrams, using which finally made the layout using the Magic tool, through which also extracted a spice file attached in the compressed folder along with the report submitted.





Cascode Amplifier



Stick Diagram

Conclusion

From the observations and calculations above, we observe that Cascode Amplifier acts as a **Low pass Filter.**

We could successfully implement and make the layout and schematic of the cascode amplifier, current mirror and schematic of the beta multiplier in both the 22nm and 180nm technology files in LTSpice and using the Magic Tools.