AEP227 Github Name

November 27, 2019

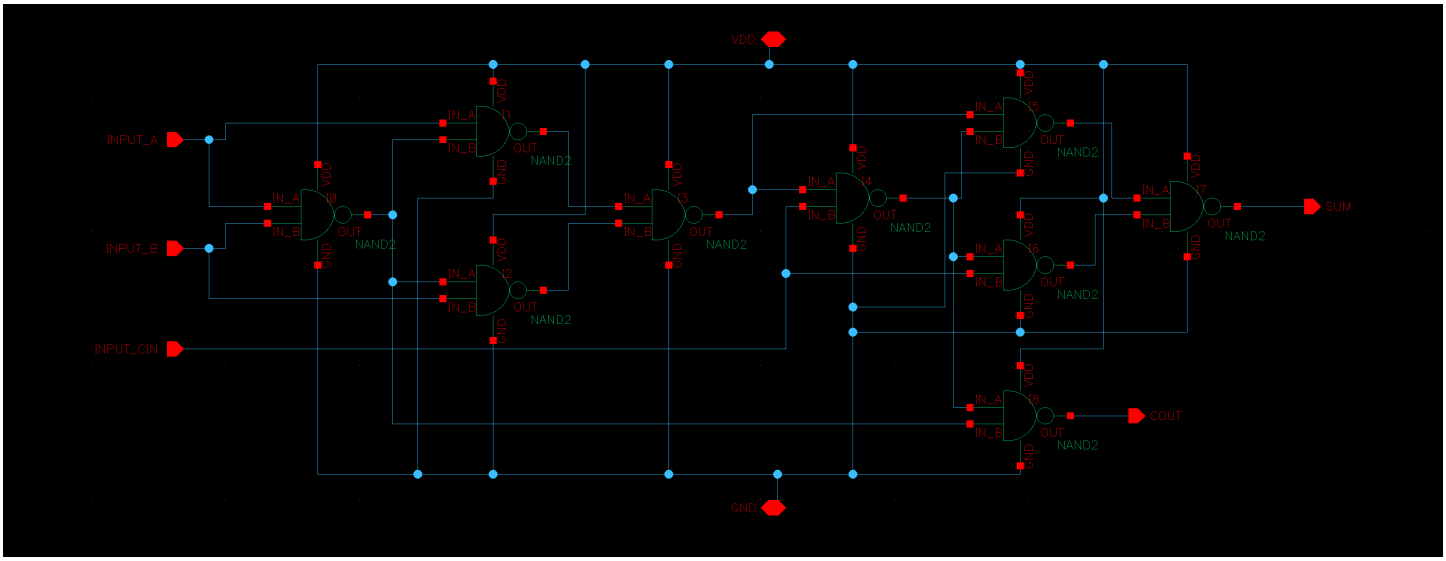
ECE 4540: VLSI Circuit Design

Lab 4 Report

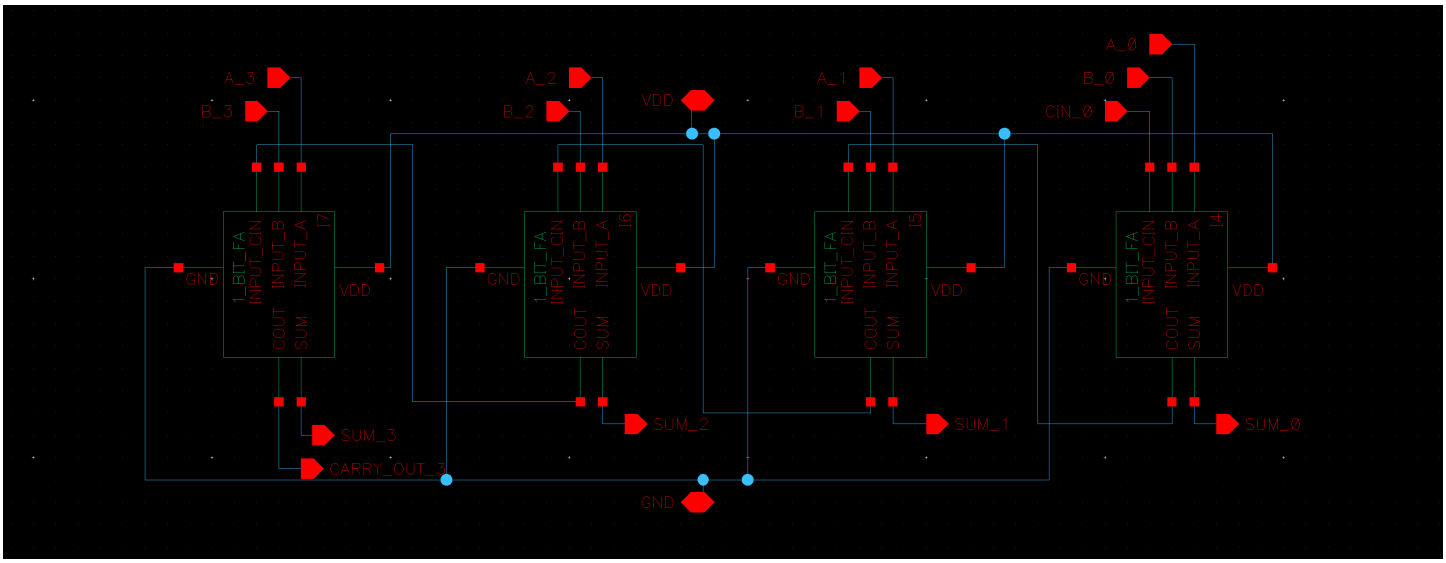
Contents

Part I: Pre-Layout Design

Schematics of 4-bit Ripple Carry Adder and Sub-Components

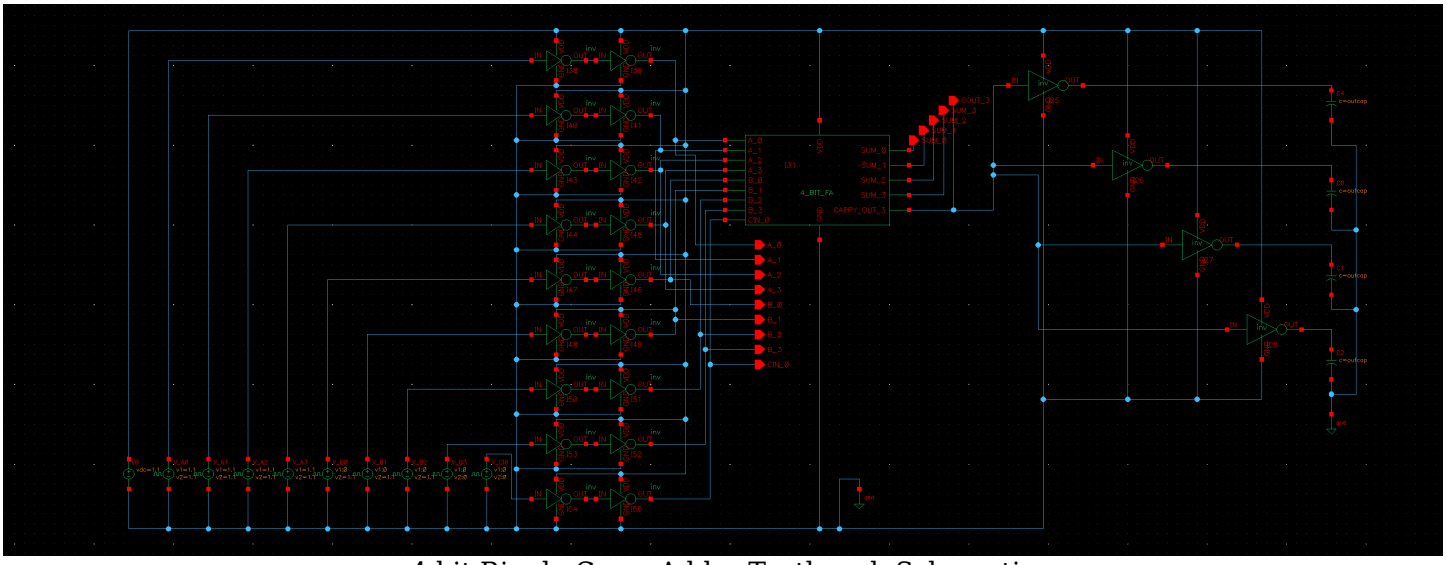


1-bit Full Adder Schematic

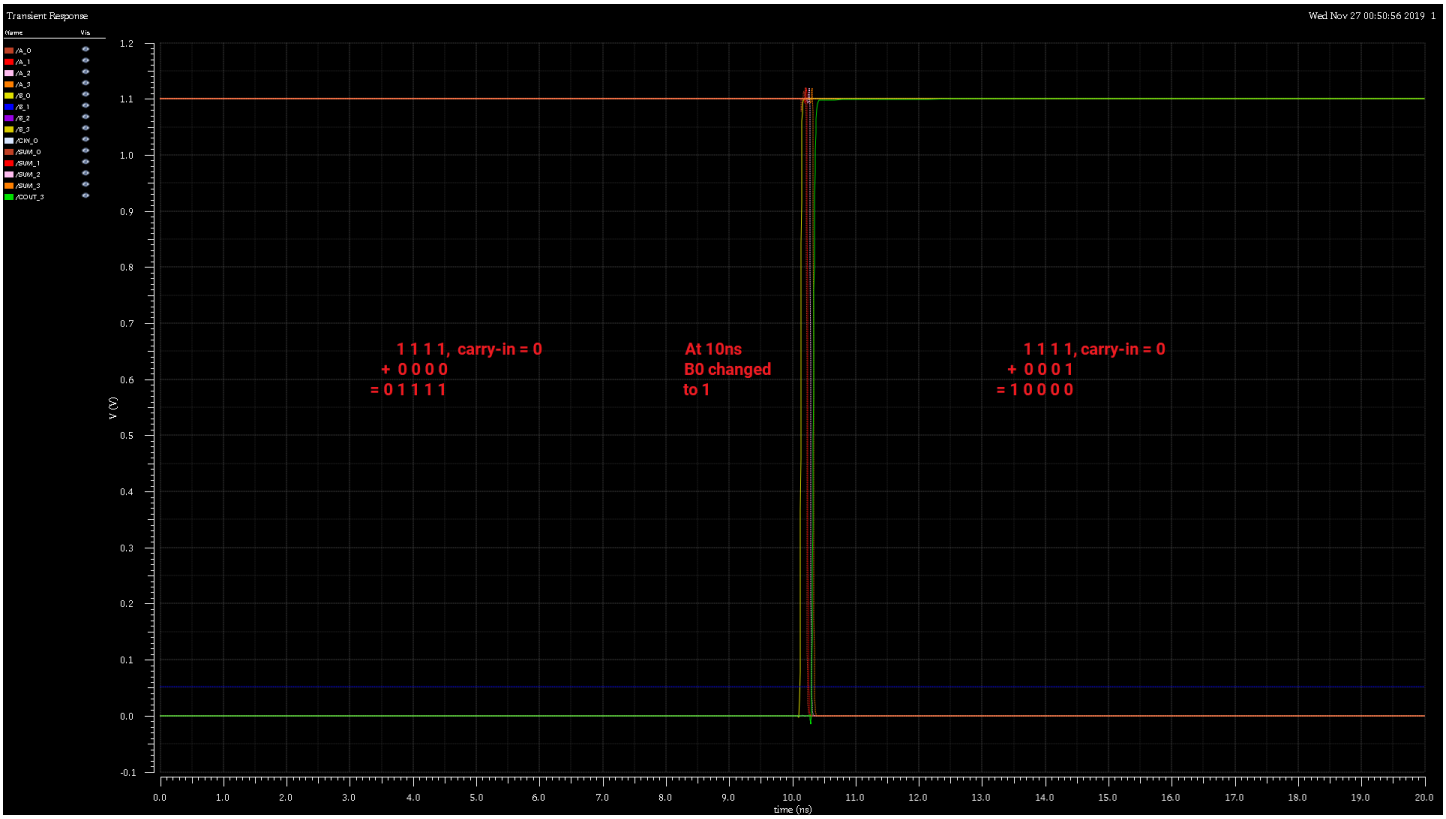


4-bit Ripple Carry Adder Schematic

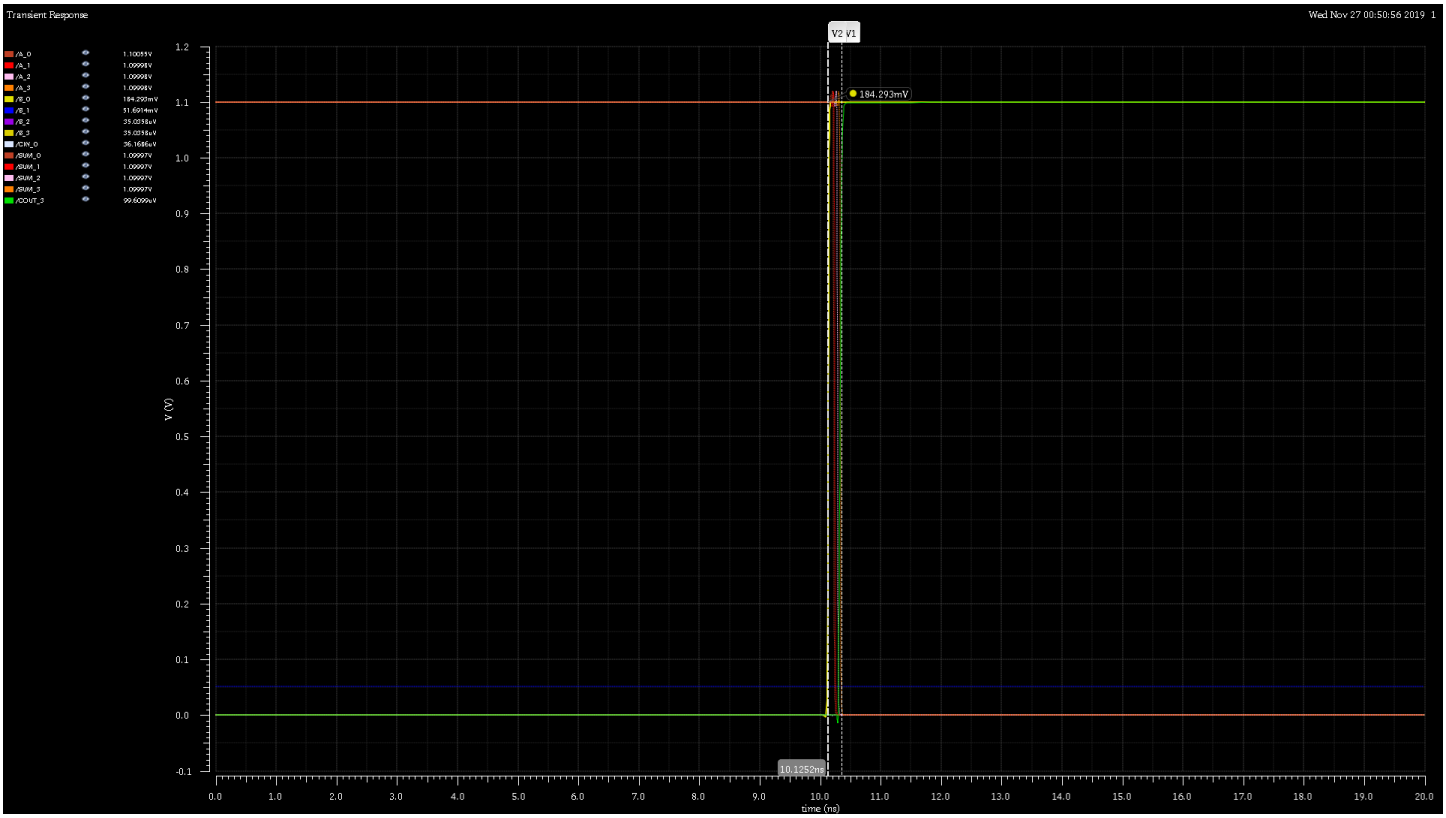
Test Bench, Pre-Layout Simulation

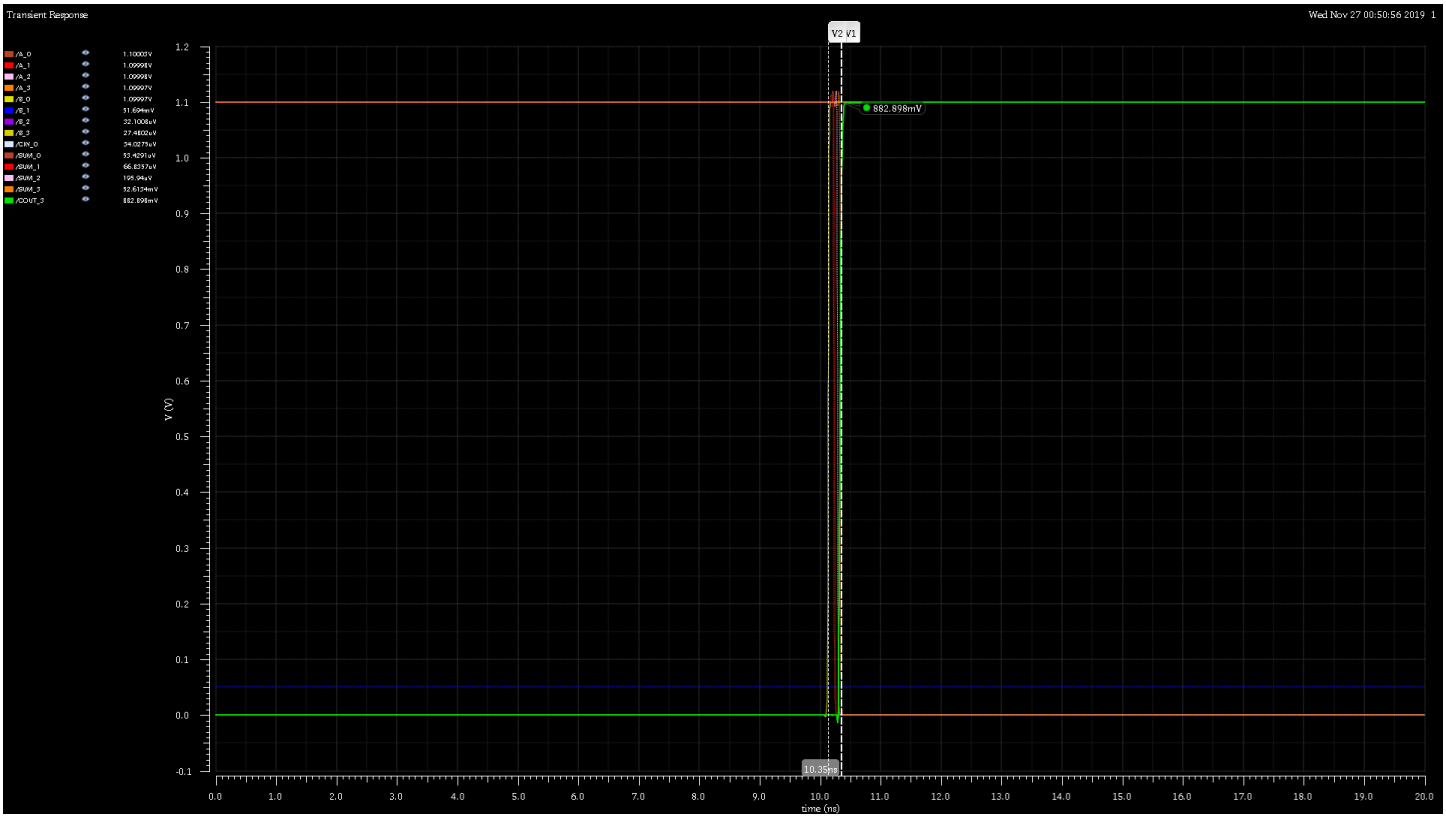


4-bit Ripple Carry Adder Testbench Schematic



Simple addition case to test functionality of the circuit and determine pre-layout worst-case delay
Initially, A = 1111, B = 0000, and the carry-in was 0. This resulted in the correct output of 01111
At 10ns, B was changed to 0001, resulting in the correct output of 10000

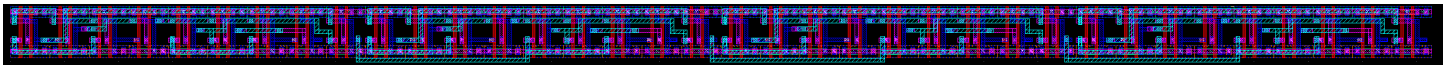




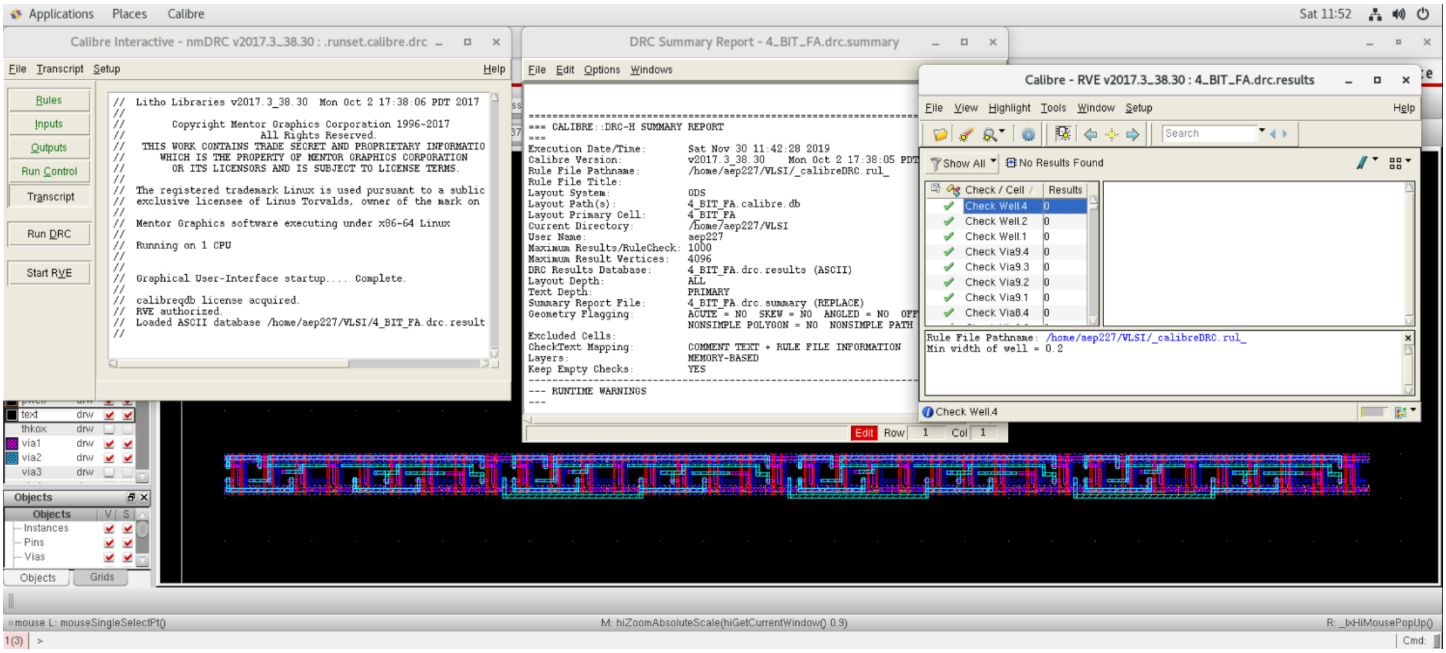
B0 changed to 1 at 10.1252ns. The carryout of the 4-bit adder updated to 1 at 10.35ns
Worst-case propagation time = 0.2248ns

Part II: Layout, Post-Layout Simulations, Adder Characteristics

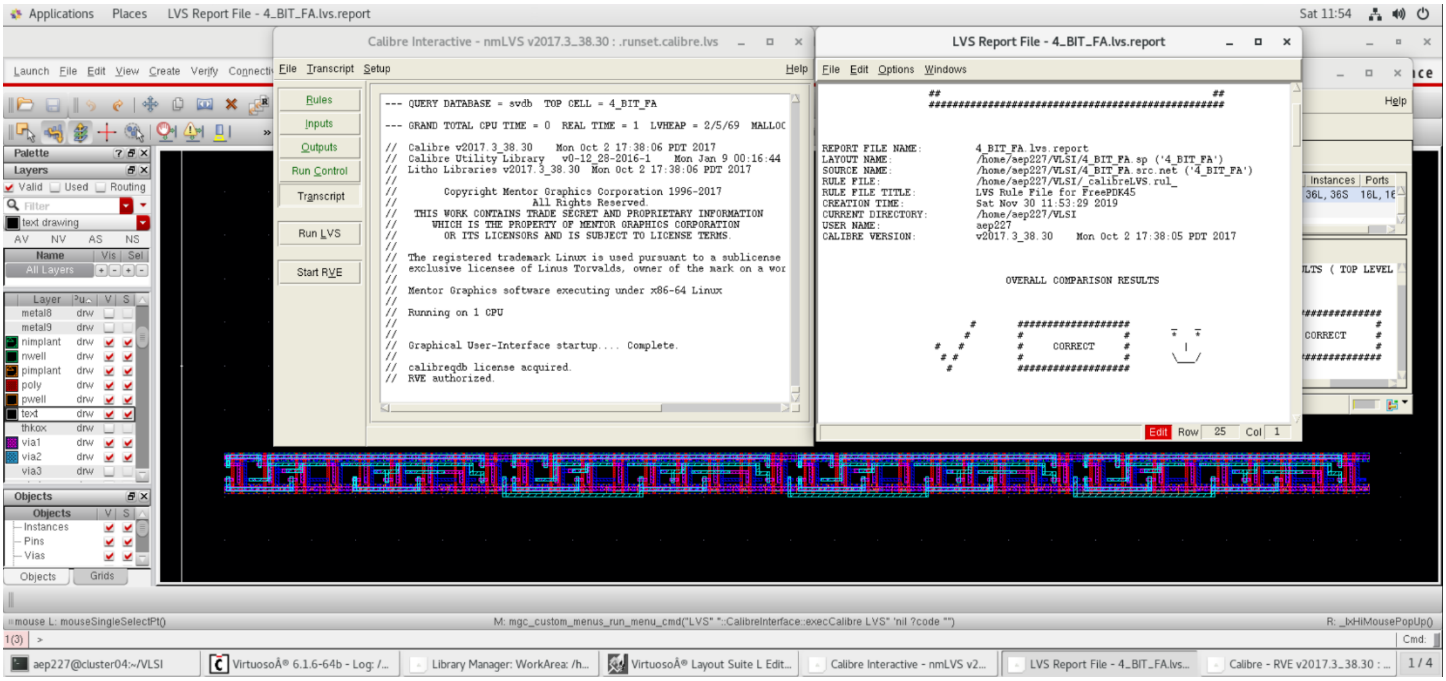
Adder Layout



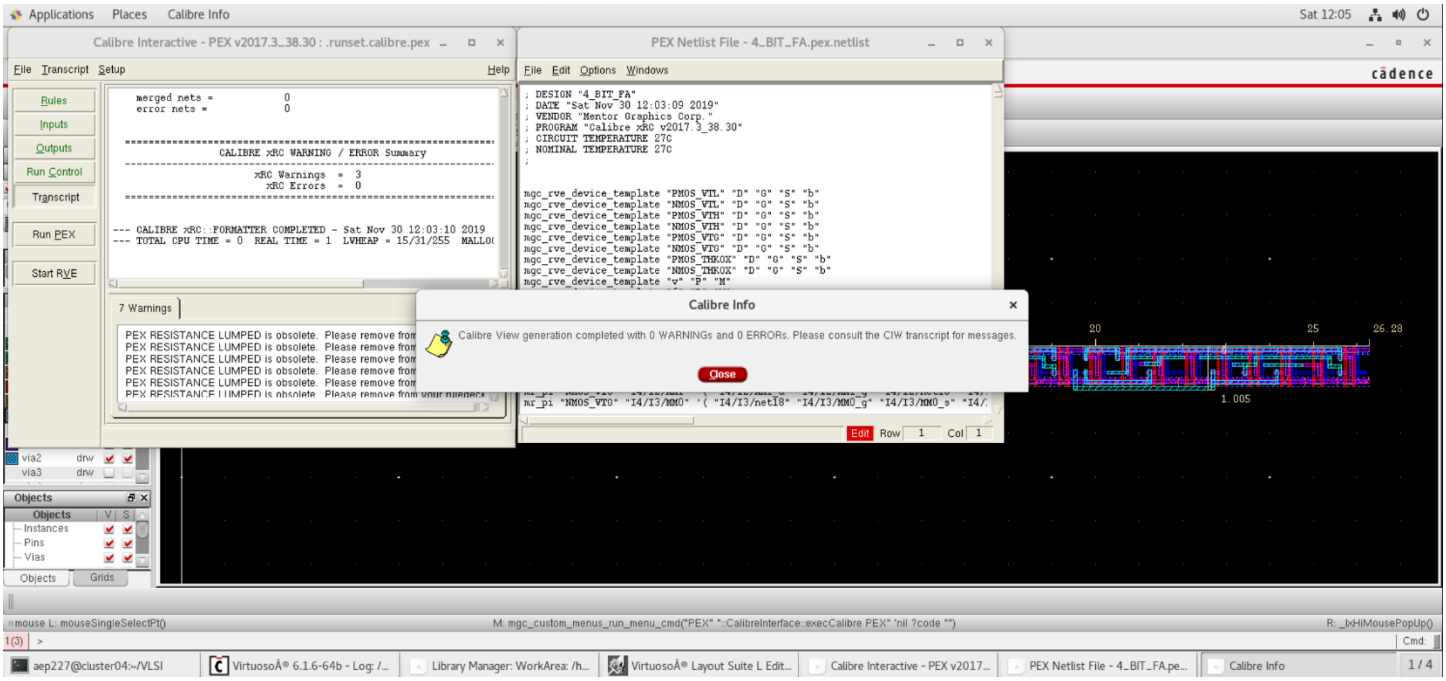
Layout of the 4-bit Ripple Carry Adder
Bounding Box Dimensions: 26.28um x 1.005um



4-bit Ripple Carry Adder DRC Pass



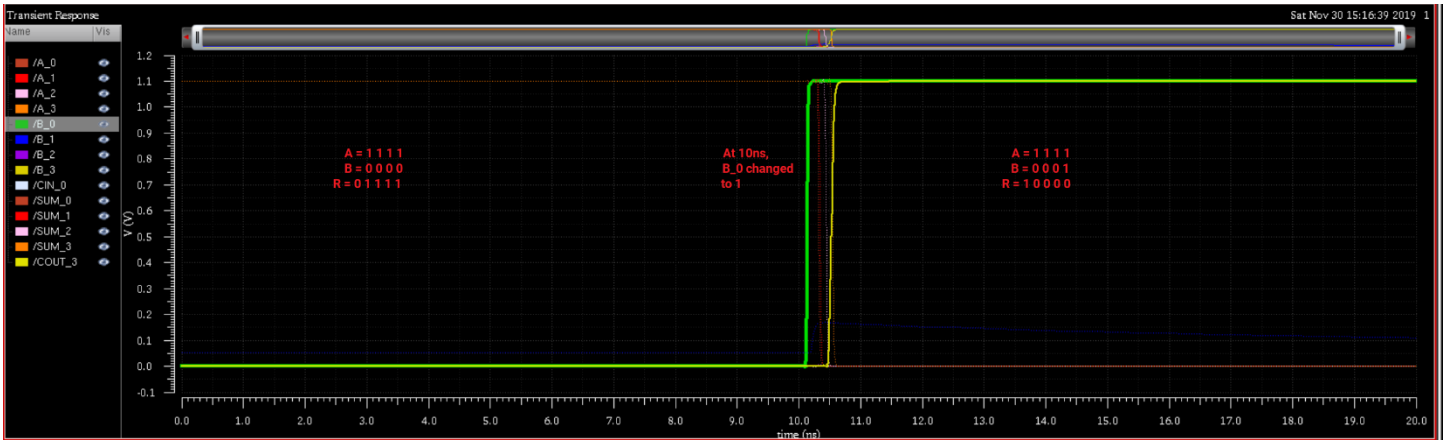
4-bit Ripple Carry Adder LVS Pass

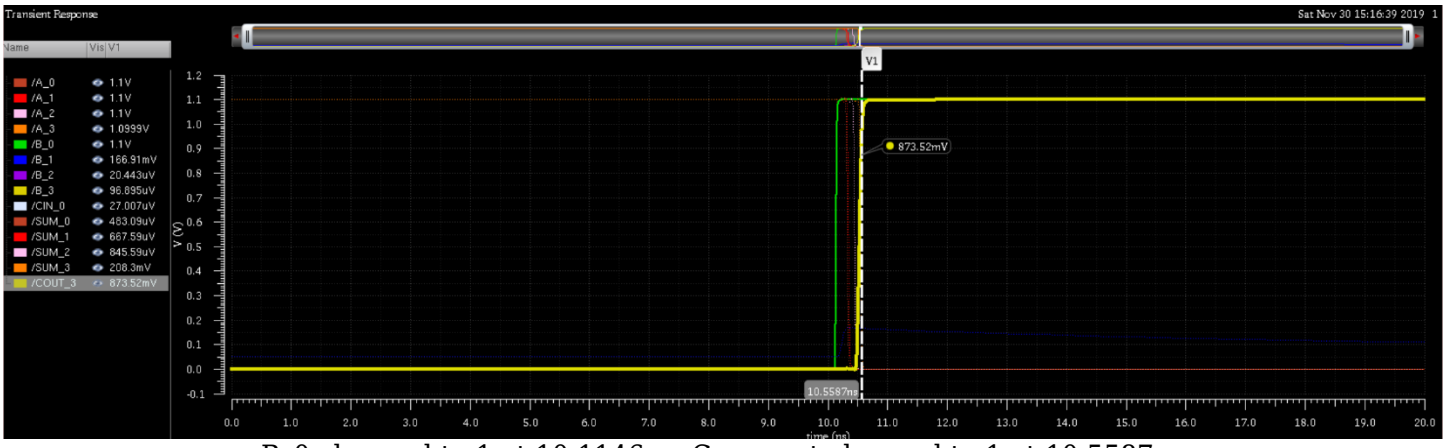


4-bit Ripple Carry Adder PEX Pass

Post-Layout Simulation, Worst-Case Propagation Delay

Post-Layout simulations used the same inputs, timings, and testbench as before

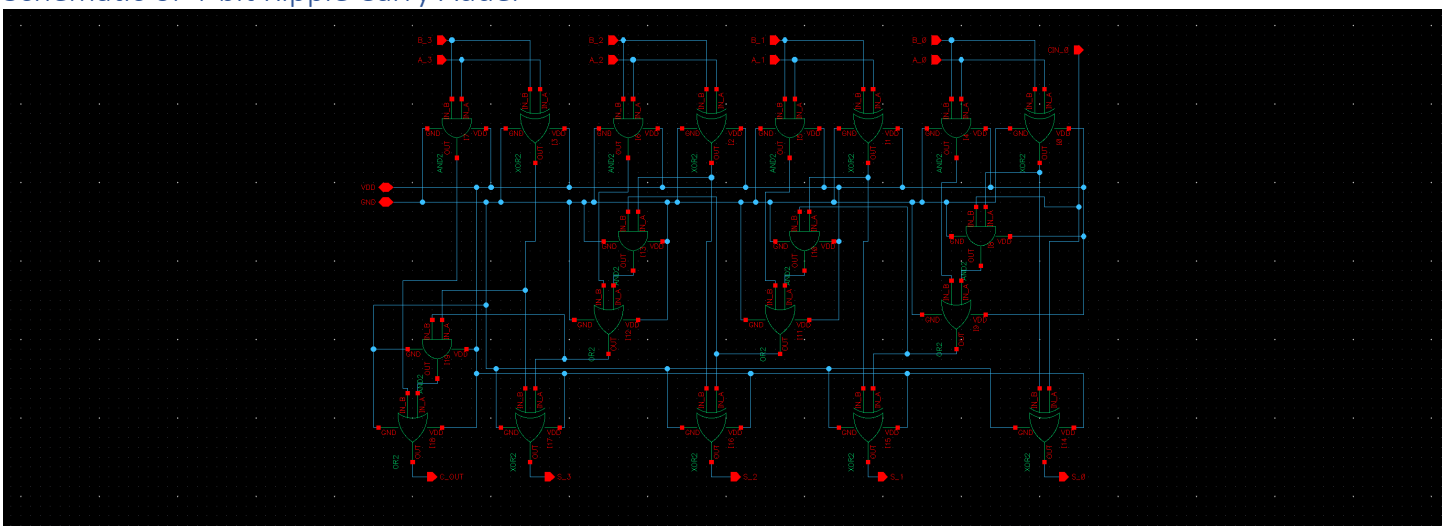




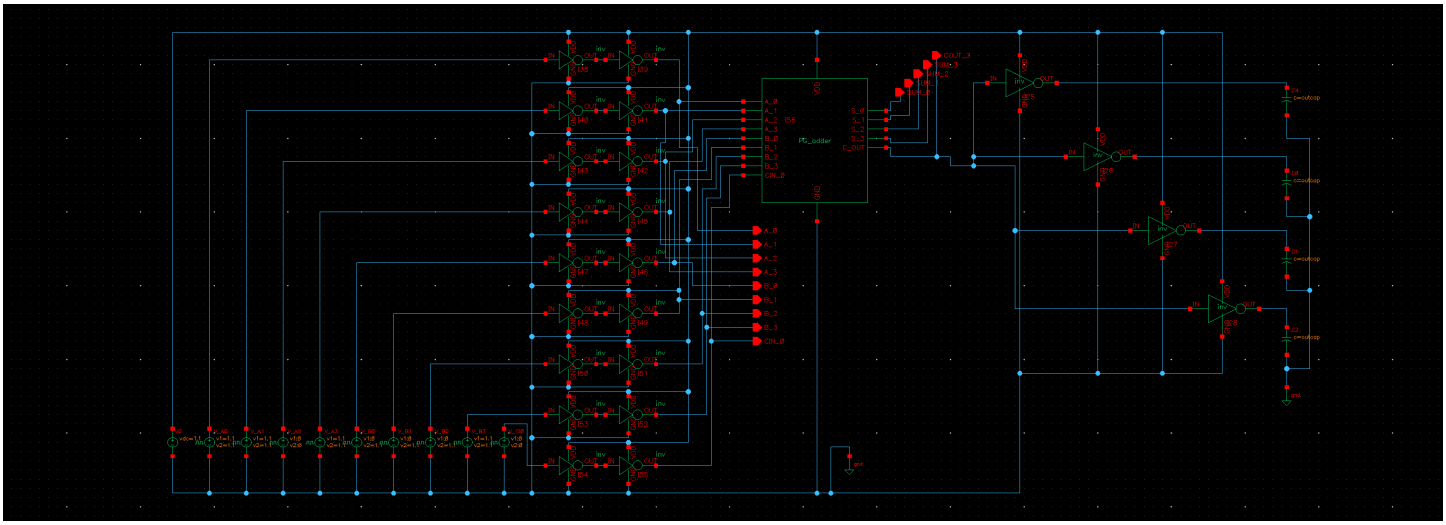
B_0 changed to 1 at 10.1146ns, Carry-out changed to 1 at 10.5587ns
Worst-case propagation delay: 0.4441ns

Part III: Bonus 4-bit PG Ripple Carry Adder

Schematic of 4-bit Ripple Carry Adder

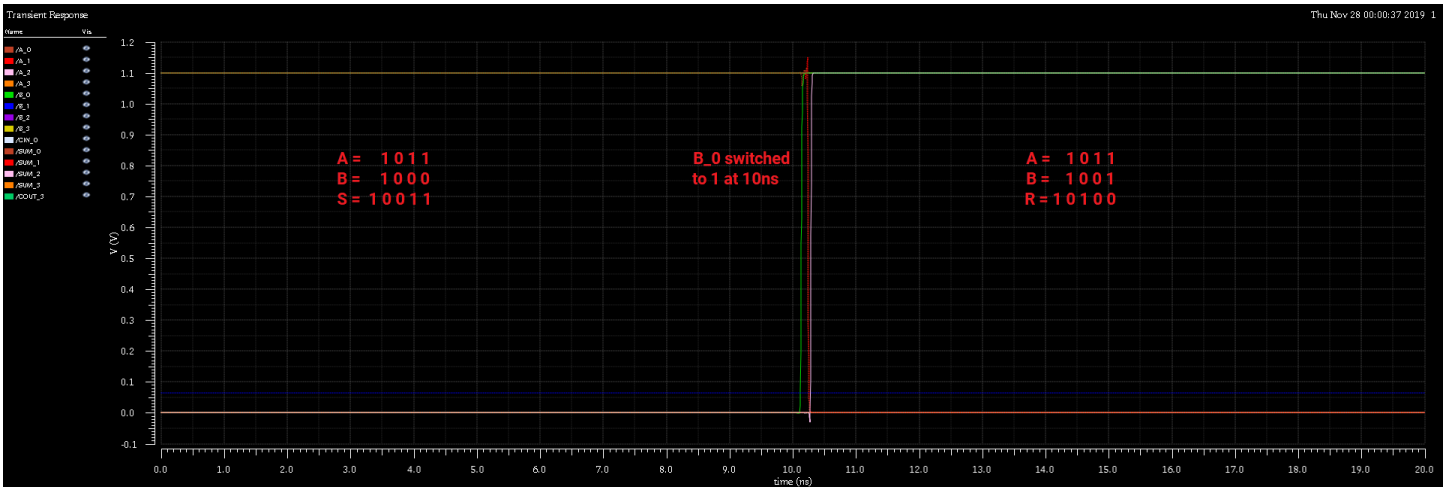


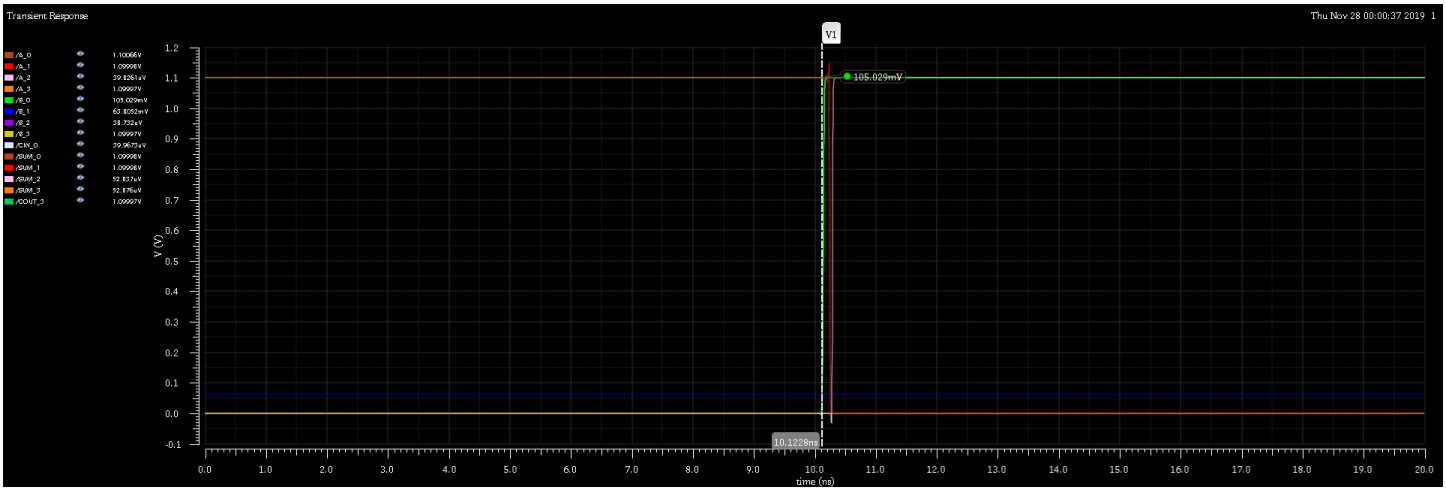
Schematic of the 4-bit PG Ripple Carry Adder

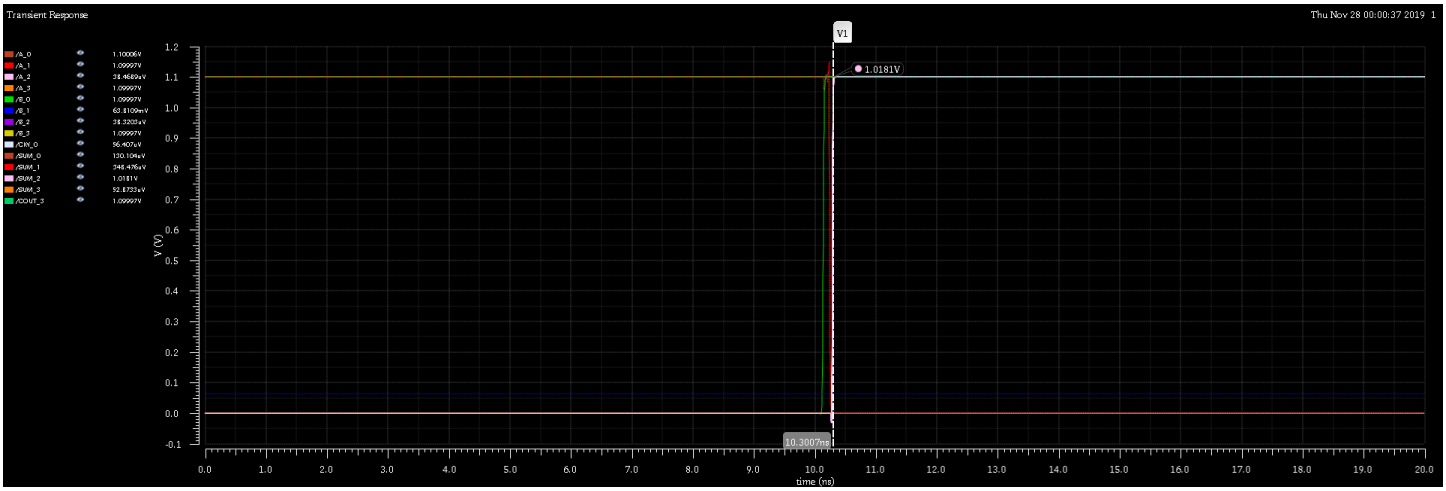


Testbench for 4-bit PG Ripple Carry Adder

Test bench and Pre-Layout Simulation







B_0 switched to 1 at 10.1228ns, output S_2 updated at 10.3007ns.
“Average” propagation delay: 0.1779ns