AEP227 Github Name
October 9, 2019
ECE 4540: VLSI Circuit Design
Lab 1 Report

Part 1 – CMOS Manufacturing Process

1. What is Oxidation? Why?

Oxidation (in regards to IC fabrication) is the process of converting a thin layer of the silicon wafer into silicon dioxide. This silicon dioxide layer is used as an insulator or as a mask for ion implantation.

2. Ion implantation / Diffusion

Ion implantation is the process of inserting impurities (such as phosphorous or boron) into the silicon wafer via an electric field. Diffusion is the movement of these impurity elements throughout a silicon wafer. Both of these processes serve to give the silicon wafer particular electrical properties.

3. Deposition

There are many different deposition steps in IC fabrication. In general, deposition is the process of depositing a material onto the silicon wafter. The two most common methods of this are physical vapor deposition (PVD) and chemical vapor deposition (CVD). PVD involves taking the material to be deposited as a solid or liquid, evaporating the material, and allowing it to solidify on the water in a vacuum. CVD is instead a chemical reaction of a gaseous form of the material to be deposited with the substrate. CVD allows for a more uniform thickness across the target but requires high temperatures to perform.

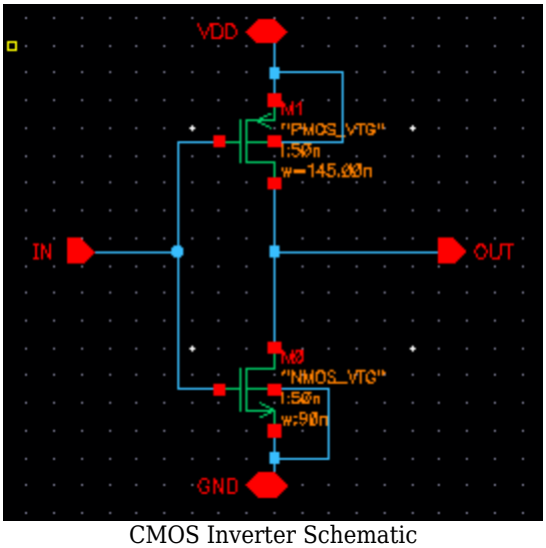
4. Photolithography & Etching

Lithography and etching are “patterning” processes, which is the changing of the deposited layers into their desired shapes. First a photoresist layer is applied to the substrate. Etching is a process in which this layer is selectively removed to create a pattern on the wafer. Lithography is the use of light of varying wavelengths and a mask to selectively change the properties of this photoresist layer.

What is the purpose of the well/substrate taps? With what voltage do they have to be applied?

The tap cells are used to wire the body of a PMOS transistor to Vdd and the body of an NMOS transistor to ground. This is done to avoid leakage into the substrate and ensures that the electric potential for a given material (whether it’s n-type or p-type) is held constant. This is done to prevent latchup, which is essentially a type of short circuit/positive feedback loop that continues until the CMOS is powered off or burns itself out.

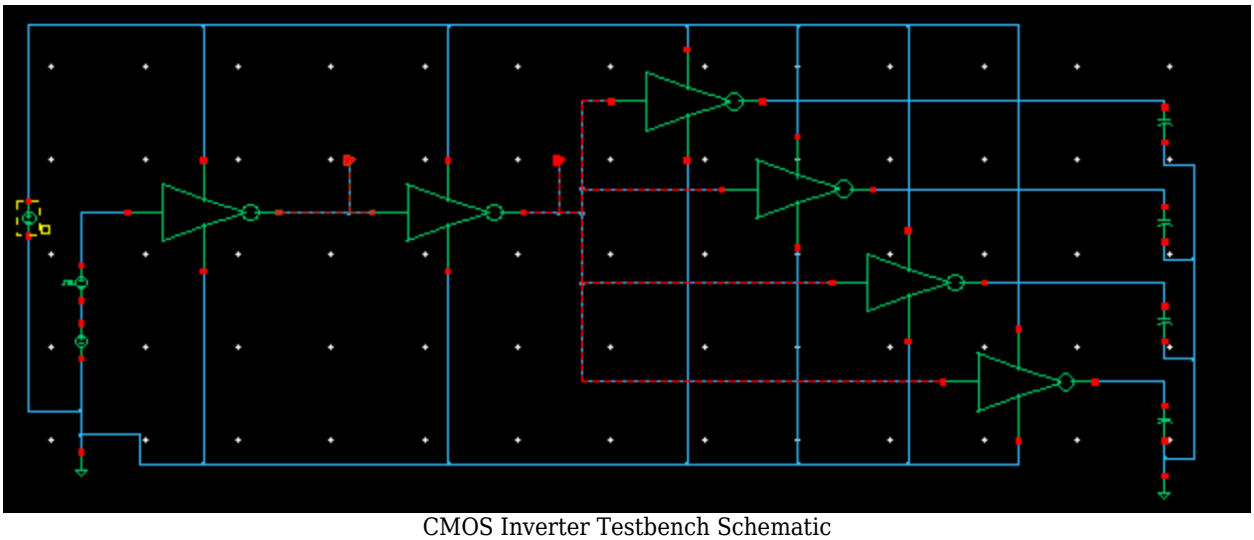
Part 2 – Inverter Symbol and Schematics



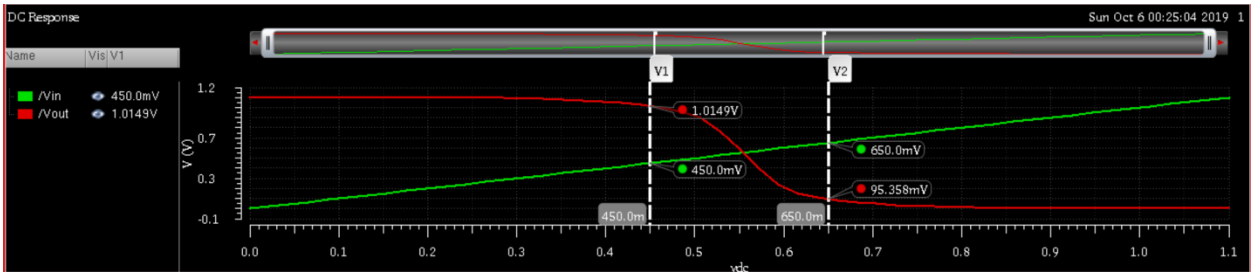
CMOS Inverter Schematic

Through research (http://classweb.ece.umd.edu/enee359a.S2008/enee359a-sizing.pdf; slide 23 of the Lecture 12 slides), I found out that symmetric performance comes from a PMOS/NMOS width ratio of around 2.4. Reducing the width of the PMOS increases the speed due to less parasitic capacitance in the PMOS. My attempt to play with the equations myself didn't lead to a definitive ratio, so using the pdf above and the slides in our lecture notes, I tested the initial ratio of 2.0 in the Lab 1 tutorial, the ideal of 2.4, as well as ratios of 1.6 to 1.9, to see how performance increases while keep the performance relatively symmetric. From there, several other ratios were simulated to find the best results. The results can be found in the table below. The ratio of 1.6 was chosen based on these results. This led to an NMOS with a length of 50nm and a width of 90nm, and a PMOS with a length of 50nm and a width of 145nm.

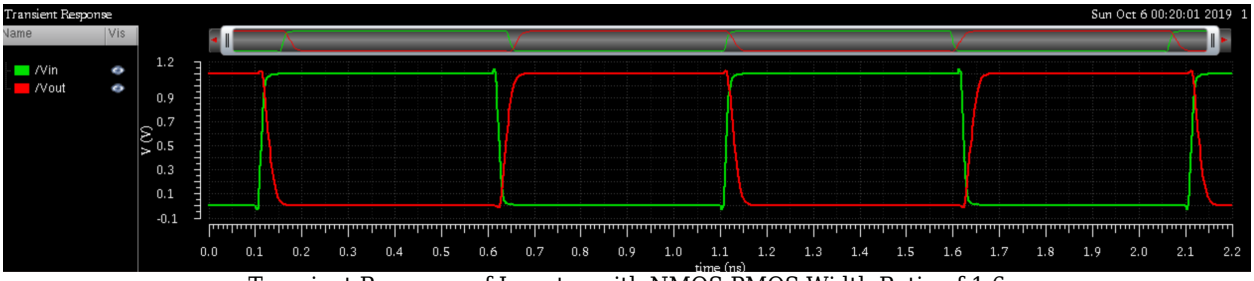
Part 3 – Schematic Simulation


CMOS Inverter Testbench Schematic

Using the DC response graph of the inverter, I determined the Vin thresholds were 0.45V and 0.65V. This leads to the following values: VIL = 450mV; VIH = 650mV; VOL = 95.358mV; VOH = 1.0149V. Using these values, the two noise margins are calculated as NMH = 364.9mV, and NML = 354.642mV.



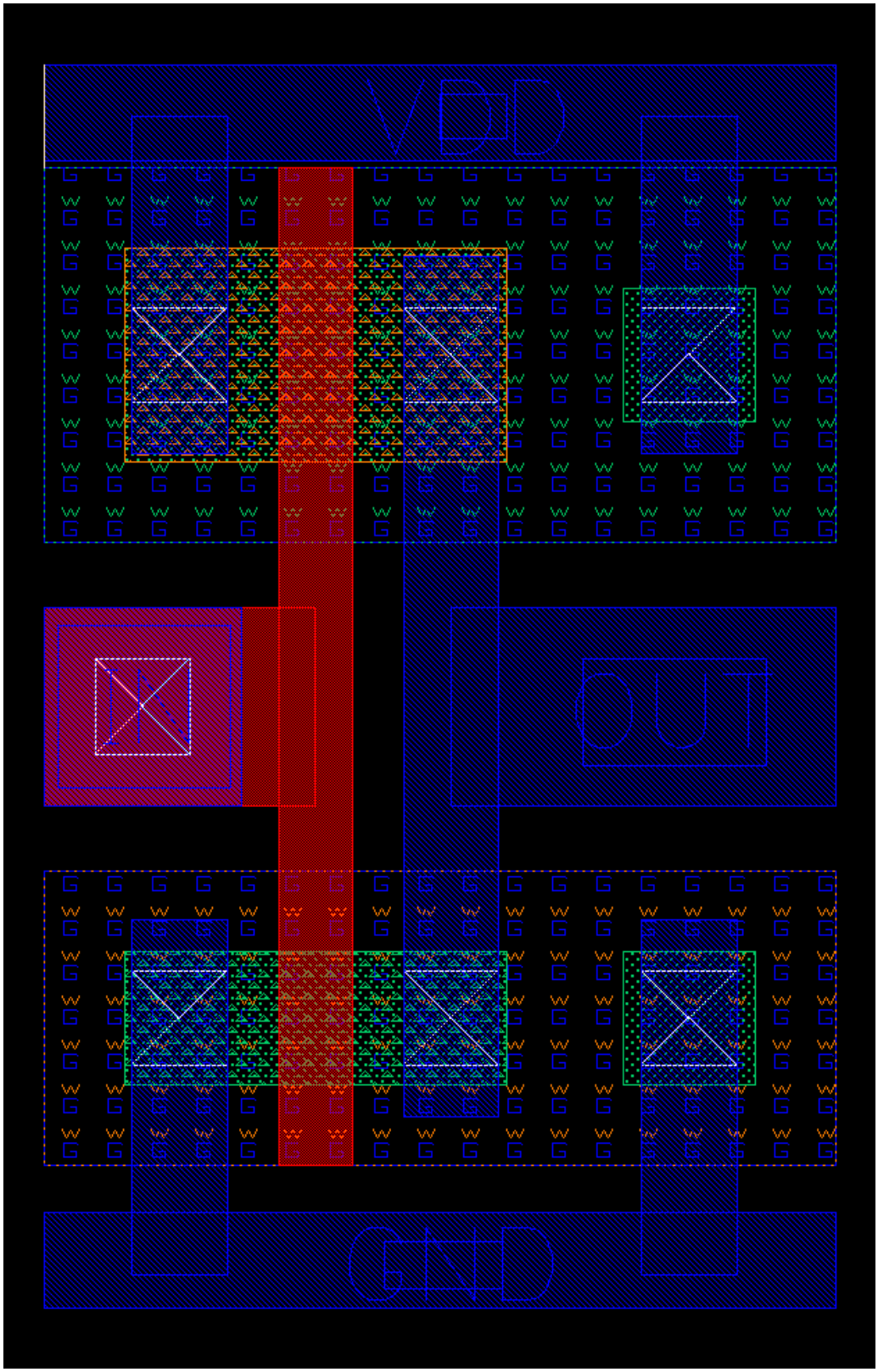
DC Response of Inverter with NMOS-PMOS Width Ratio of 1.6



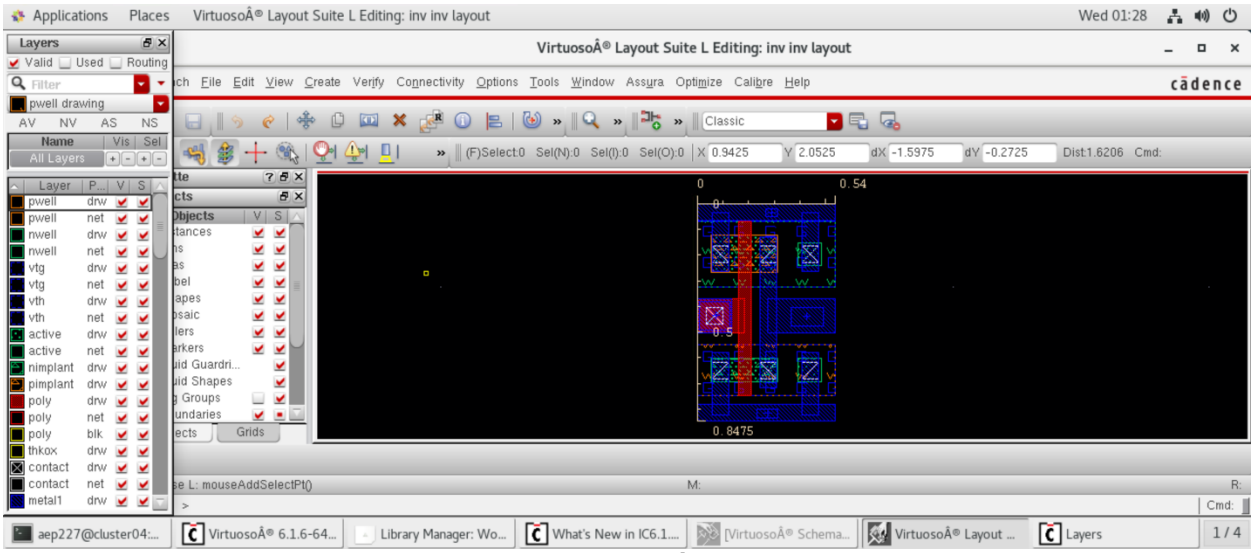
Transient Response of Inverter with NMOS-PMOS Width Ratio of 1.6

PMOS Width to NMOS Width Ratio	Propagation Delay (picoseconds)	Vout Max Rise Time(ps)	Vout Max Fall Time(ps)	Percentage Different
2.8	20.305	15.21	25.54	50.70%
2.4	18.949	15.689	22.62	36.18%
2.0	17.67	16.66	20.3	19.70%
1.9	17.265	16.86	19.531	14.68%
1.75	16.76	17.39	18.875	8.19%
1.6	16.147	17.94	17.97	0.17%
1.589	16.27	18.05	17.98	0.39%
1.583	16.27	18.07	17.89	1.00%
1.5	16.73	18.51	17.731	4.30%

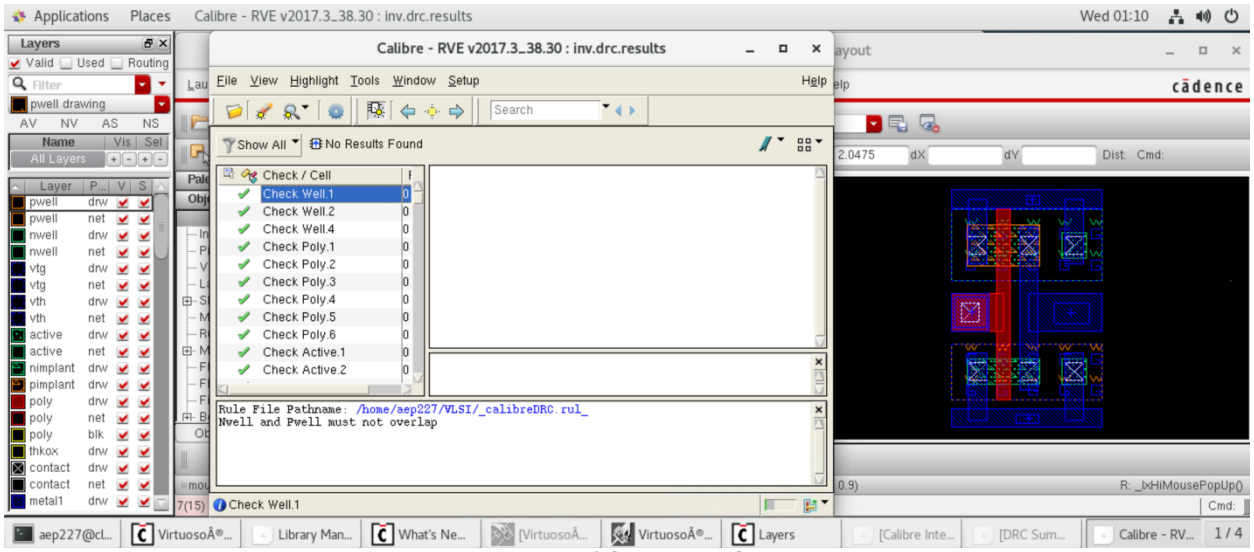
Part 4 – Inverter Layout



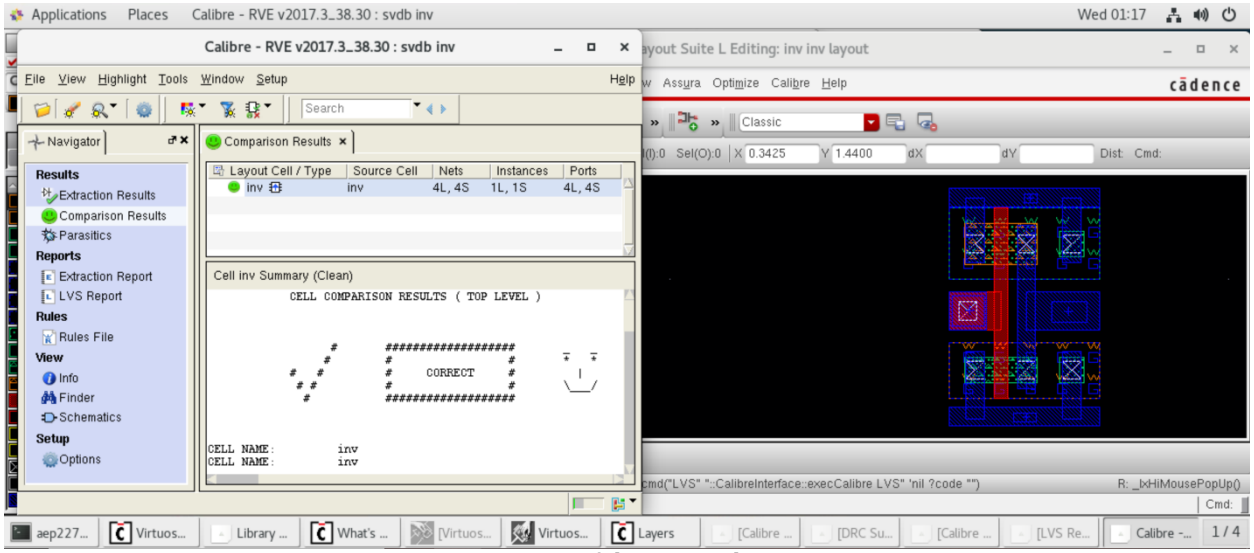
CMOS Inverter Layout
PMOS W/L: 145nm/50nm
NMOS W/L: 90nm/50nm
Bounding Box Dimensions: 847.5nm x 540nm
Area: 457,650 nm^2



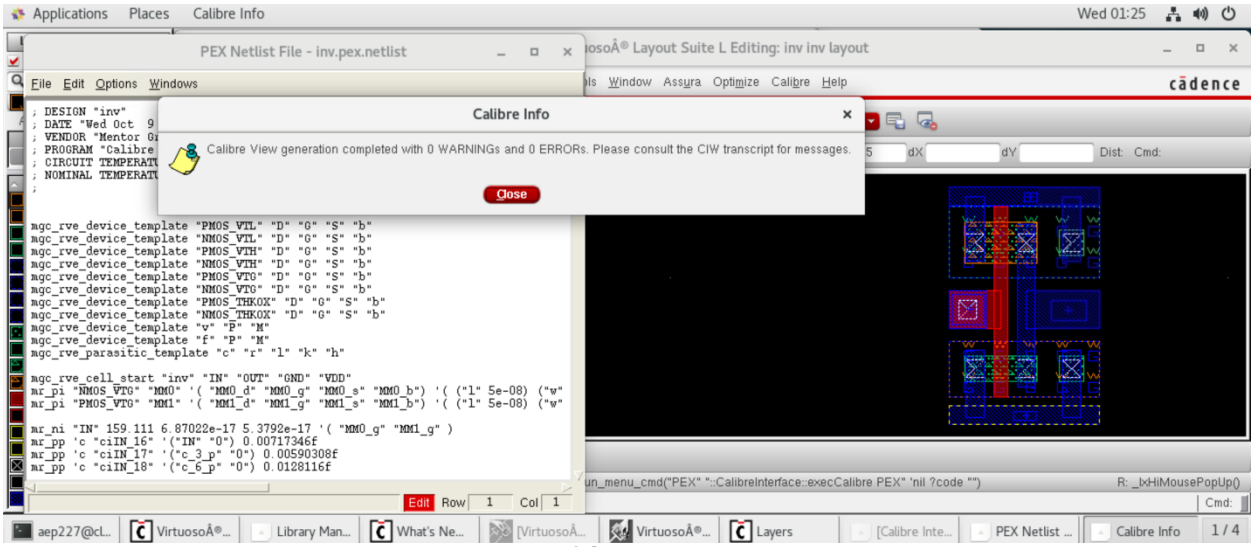
CMOS Inverter Layout with Measurements



Successful DRC Result

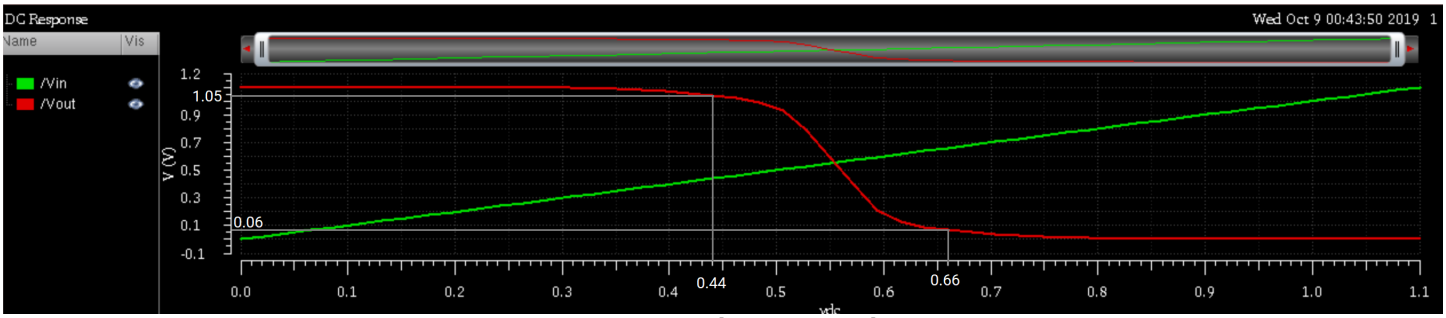


Successful LVS Result

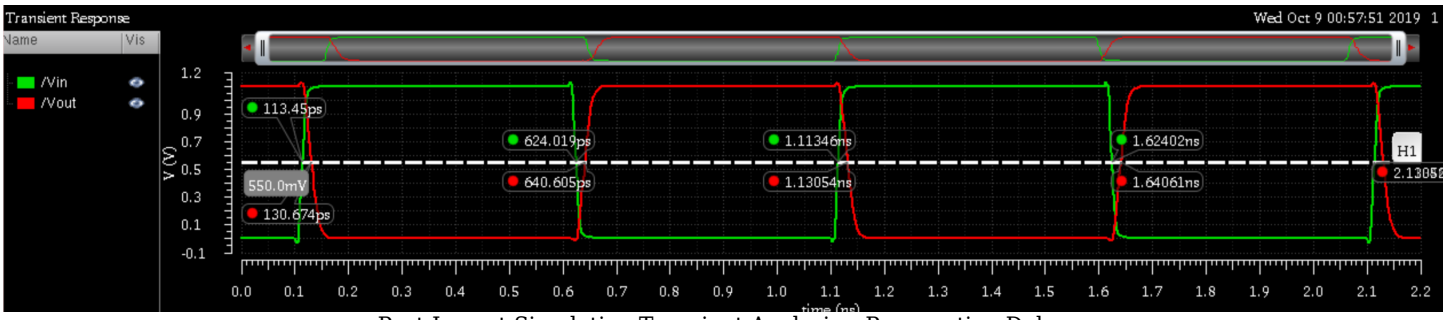


Successful PEX Extraction

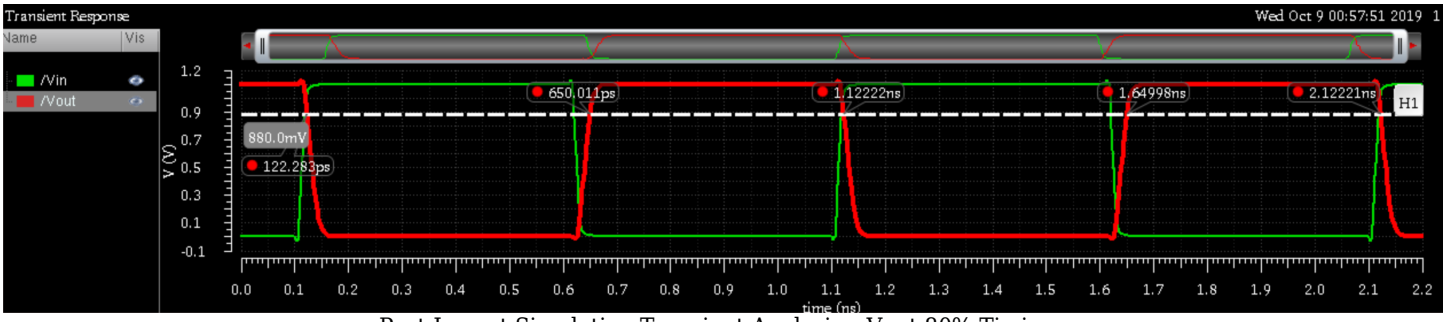
Part 5 – Layout Simulation



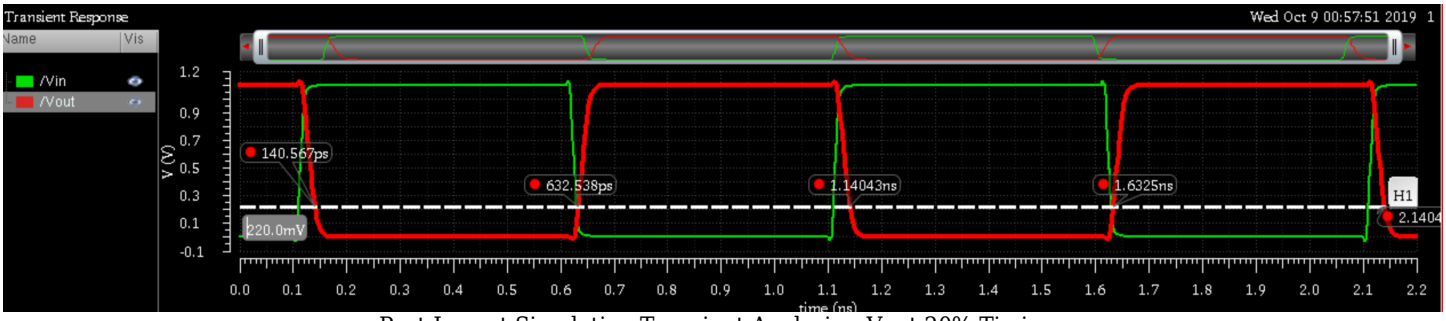
Post-Layout Simulation DC Analysis



Post-Layout Simulation Transient Analysis – Propagation Delay



Post-Layout Simulation Transient Analysis – Vout 80% Timings



Post-Layout Simulation Transient Analysis – Vout 20% Timings

Using the data above, the post-layout DC and transient response were calculated and tabulated below.

Value	Pre-Layout Simulation	Post-Layout Simulation	Percentage Difference Pre- vs Post-Layout
VIL	0.450V	0.440V	2.25%
VIH	0.650V	0.660V	1.53%
VOL	0.095V	0.060V	45.16%
VOH	1.015V	1.050V	3.39%
NMH	0.365V	0.450V	20.86%
NML	0.355V	0.380V	6.80%
Max Propagation Delay	16.147ps	17.224ps	6.45%
Max Rise Time	17.940ps	17.480ps	2.60%
Max Fall Time	17.970ps	18.284ps	1.73%

Due to the changes in rise and fall times, the inverter behaves slightly differently. The pre-layout simulation showed almost exactly symmetrical performance between rise/fall times with a difference of only 0.03ps / 0.17%. By contrast, the post-layout simulation showed a faster rise time, but a slower fall time, leading to a difference in 0.804ps / 4.5%.

Finally, with the layout complete and an average propagation delay, the Area-Product Delay was calculated for the circuit. With an area of 457,650 nm^2 and an average propagation delay of 16.905ps (obtaining by averaging the first two propagation delays), this inverter has an area-product delay of 7,736,573.25 $nm^{2*}ps$.

Most of the differences between these two simulations are slight but have large effects. As stated above, the decrease in rise times and the increase in fall times led to a significant decrease in the symmetrical performance of the device. The maximum propagation delay also increased by a full picosecond. However, there was one improvement, and that's that the noise margins were significantly improved.

These differences are likely caused by the parasitic capacitances that the pre-layout simulations don't take into consideration. While this only a single data point, it's safe to say that when included in the simulation, these capacitances will increase the propagation delay and modify the rise and fall times in

some manner. With further research, the exact effects of these capacitances on the propagation delay, rise, and fall timescould be determined and accounted for earlier in the design process.