

AEP227 Github Name

November 12, 2019

ECE 4540: VLSI Circuit Design

Lab 3 Report

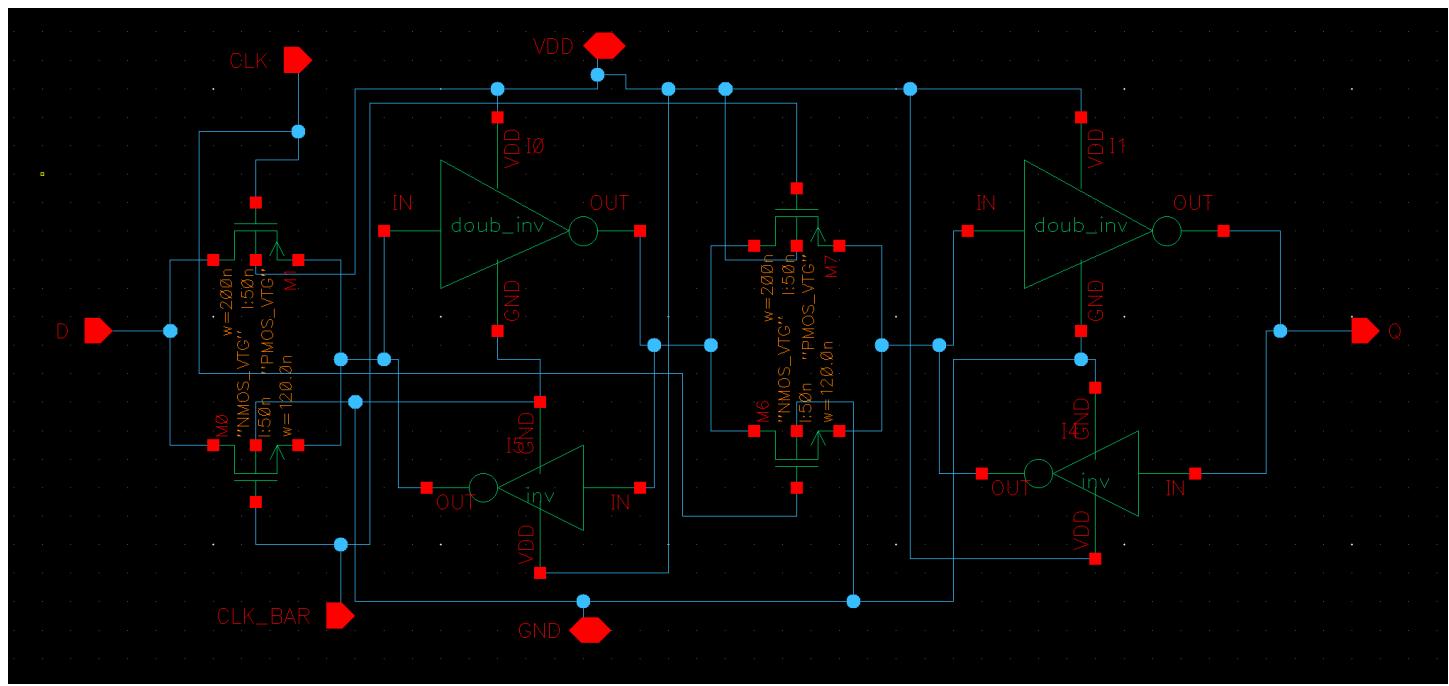
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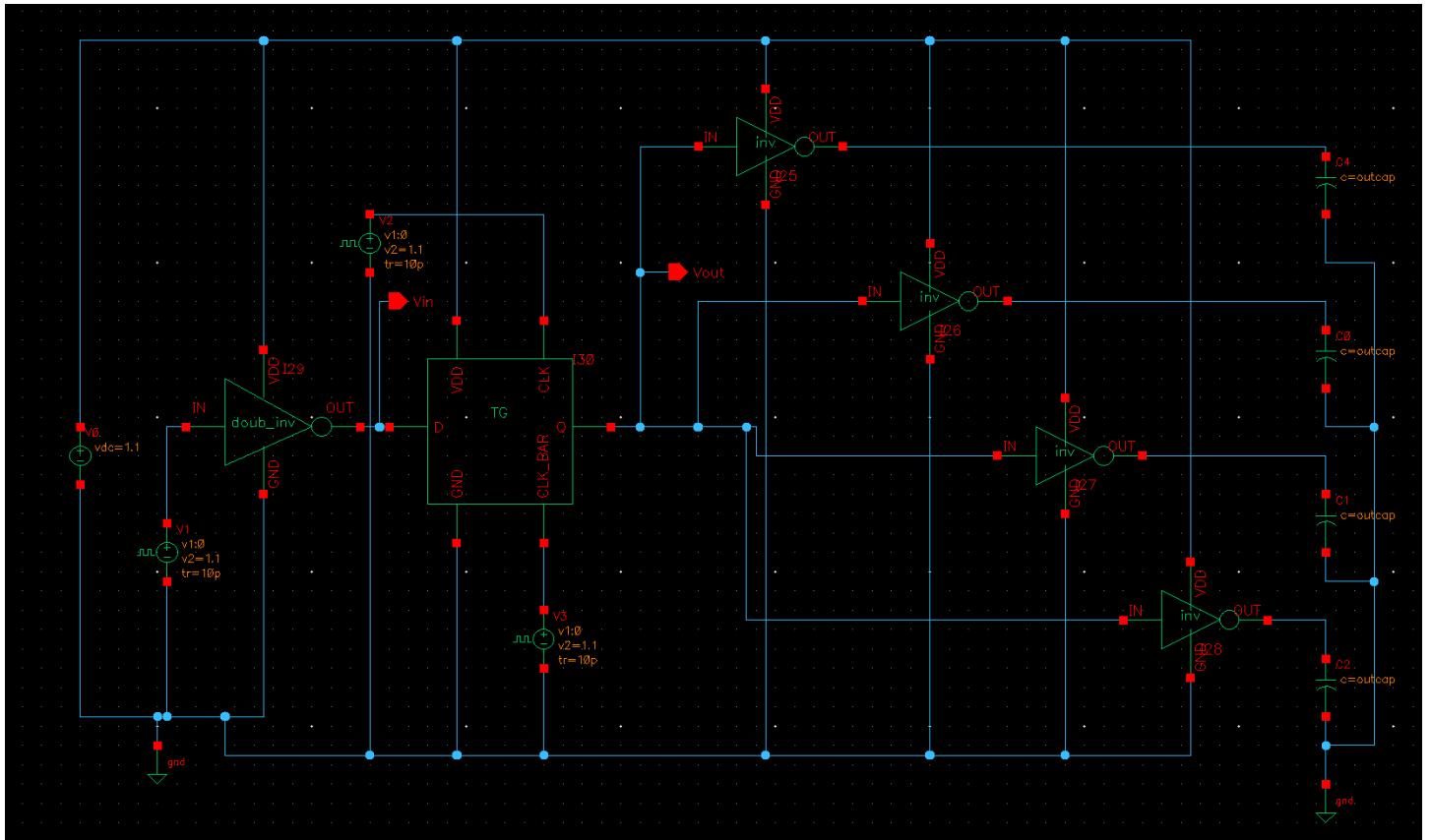
Part I: Schematics and Pre-Layout Simulation

Schematics

	PMOS	NMOS		
	Width (nm)	Length (nm)	Width (nm)	Length (nm)
Transmission Gate 1	200		120	
Inverter Loop 1 (forward)	300		180	
Inverter Loop 1 (feedback)	150		90	
Transmission Gate 2	200	50	120	
Inverter Loop 2 (forward)	300		180	
Inverter Loop 2 (feedback)	150		90	



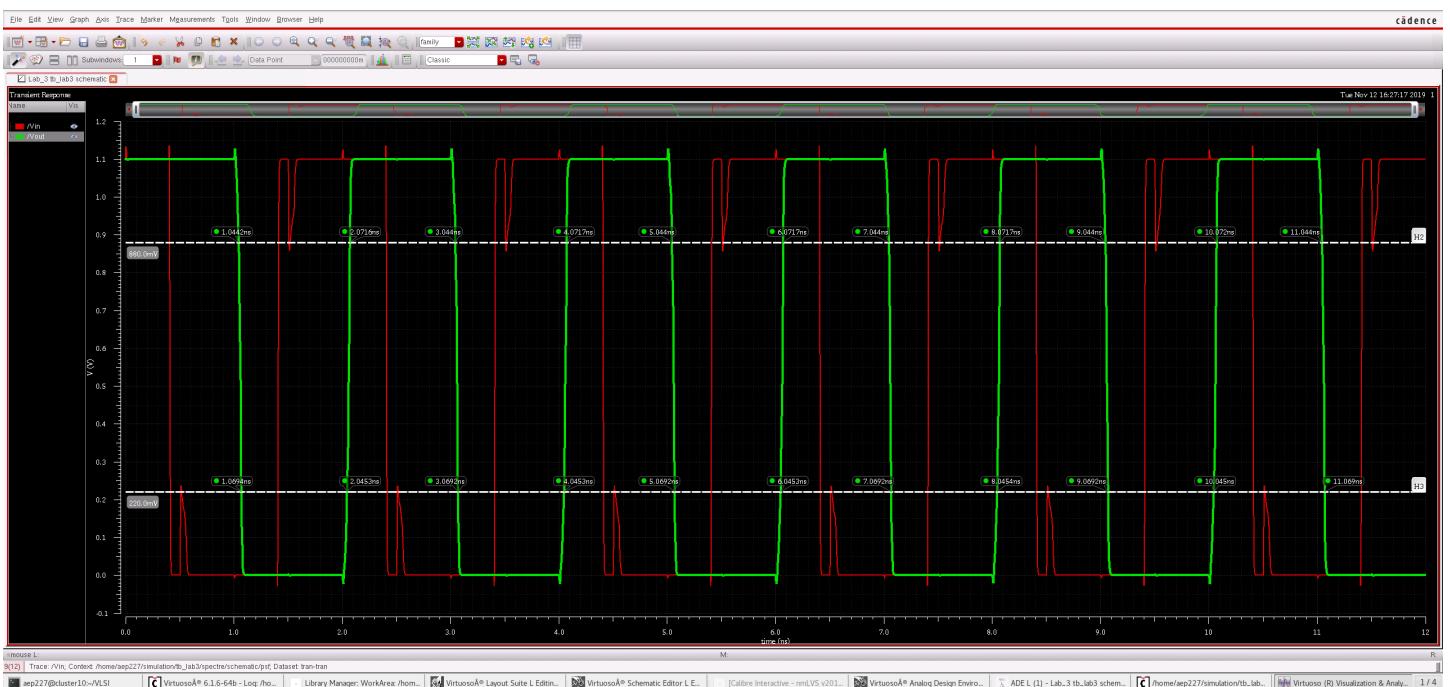
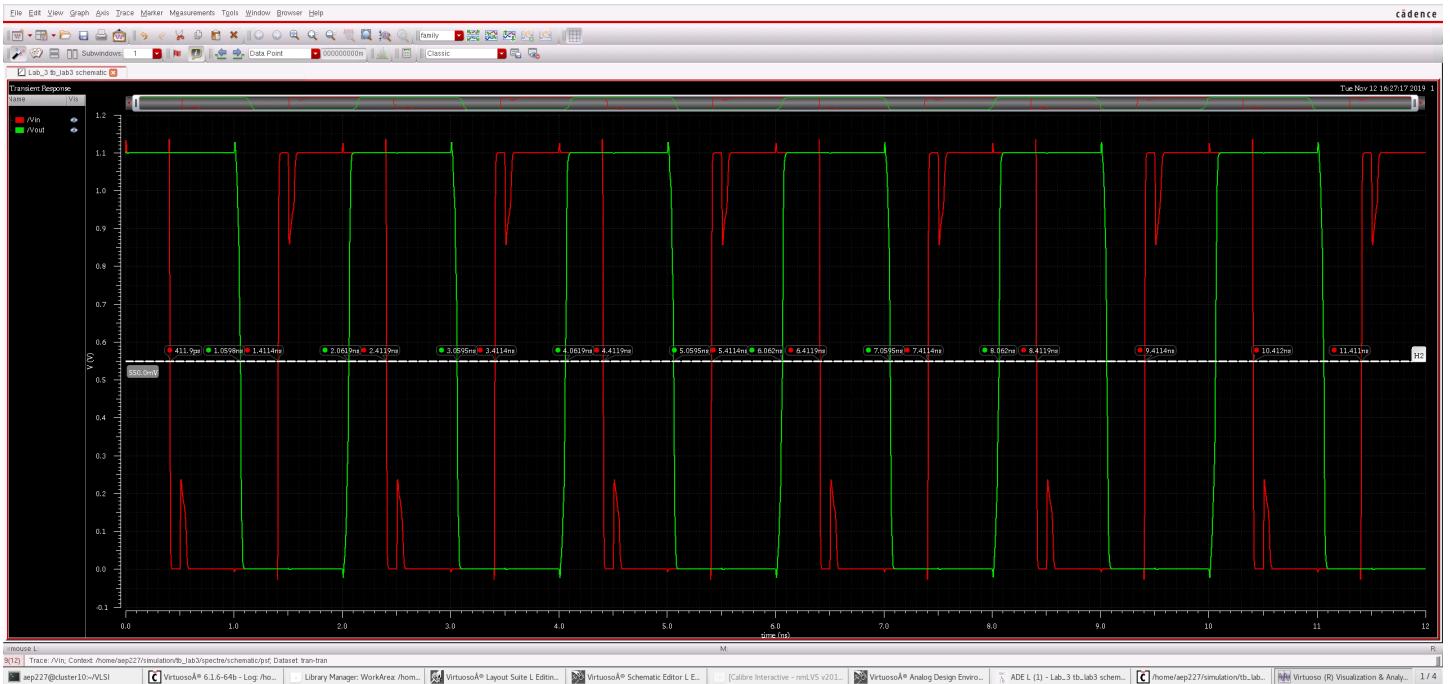
Test Bench and Pre-Layout Simulation



Testbench Schematic

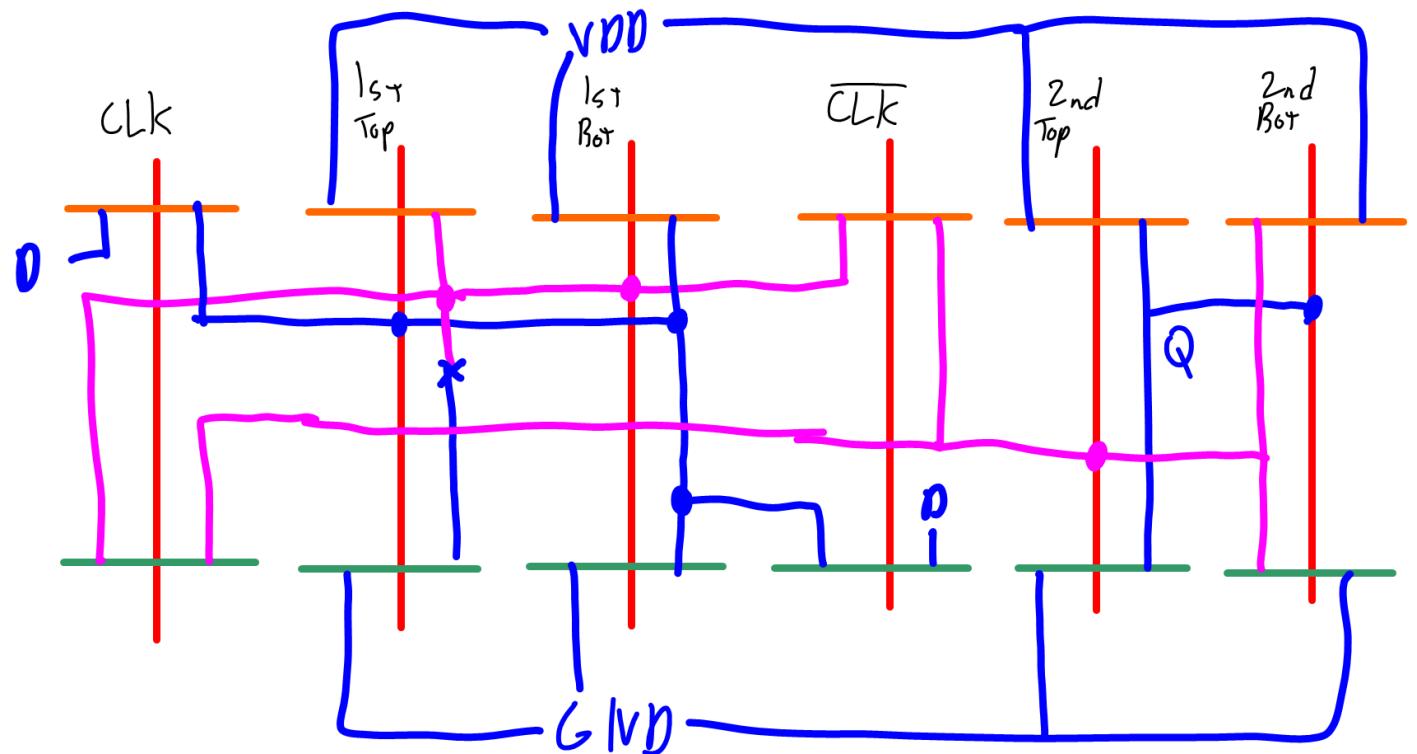


Pre-Layout Simulation Results at 85 degrees Celsius
Positive clock edges on the nanosecond, negative clock edges on the half nanosecond

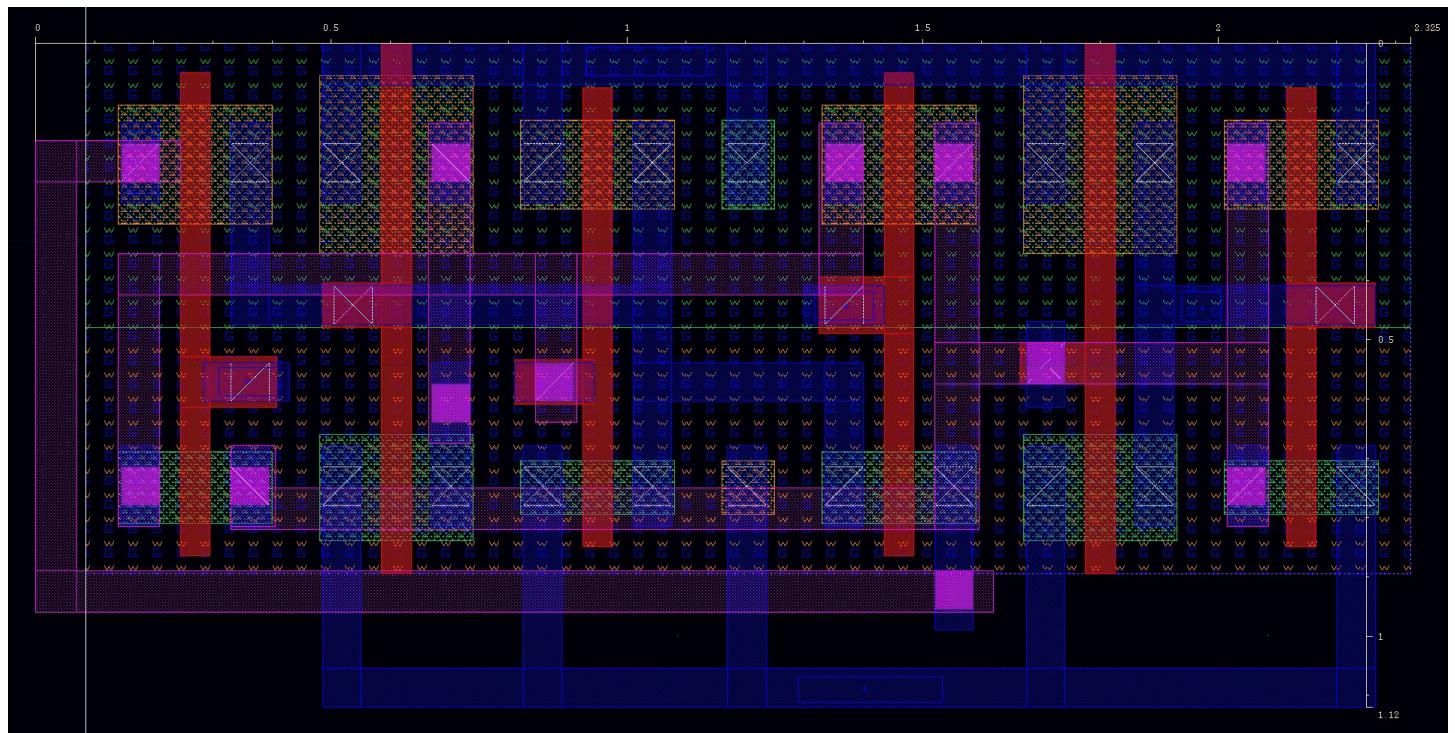


Part II: Layout, Post-Simulation, DFF Characteristics

Layout

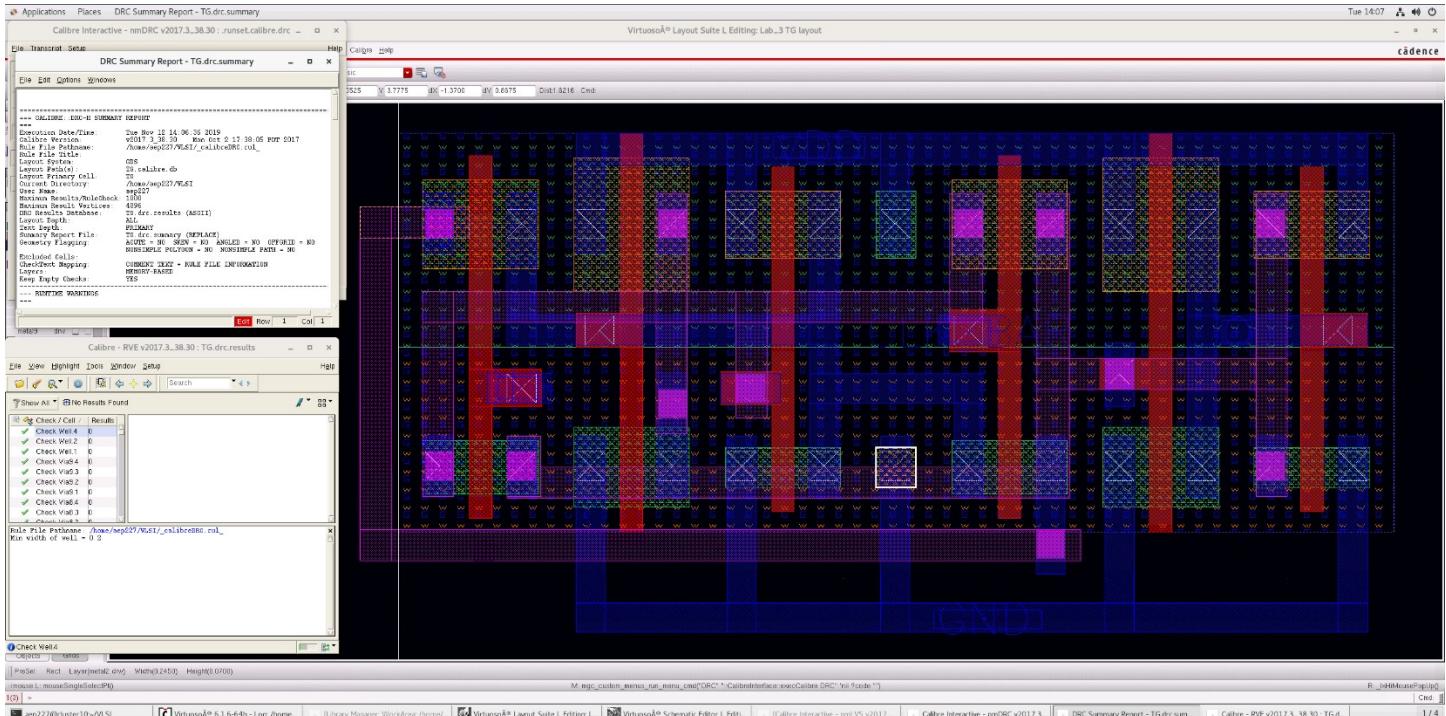


Stick Diagram

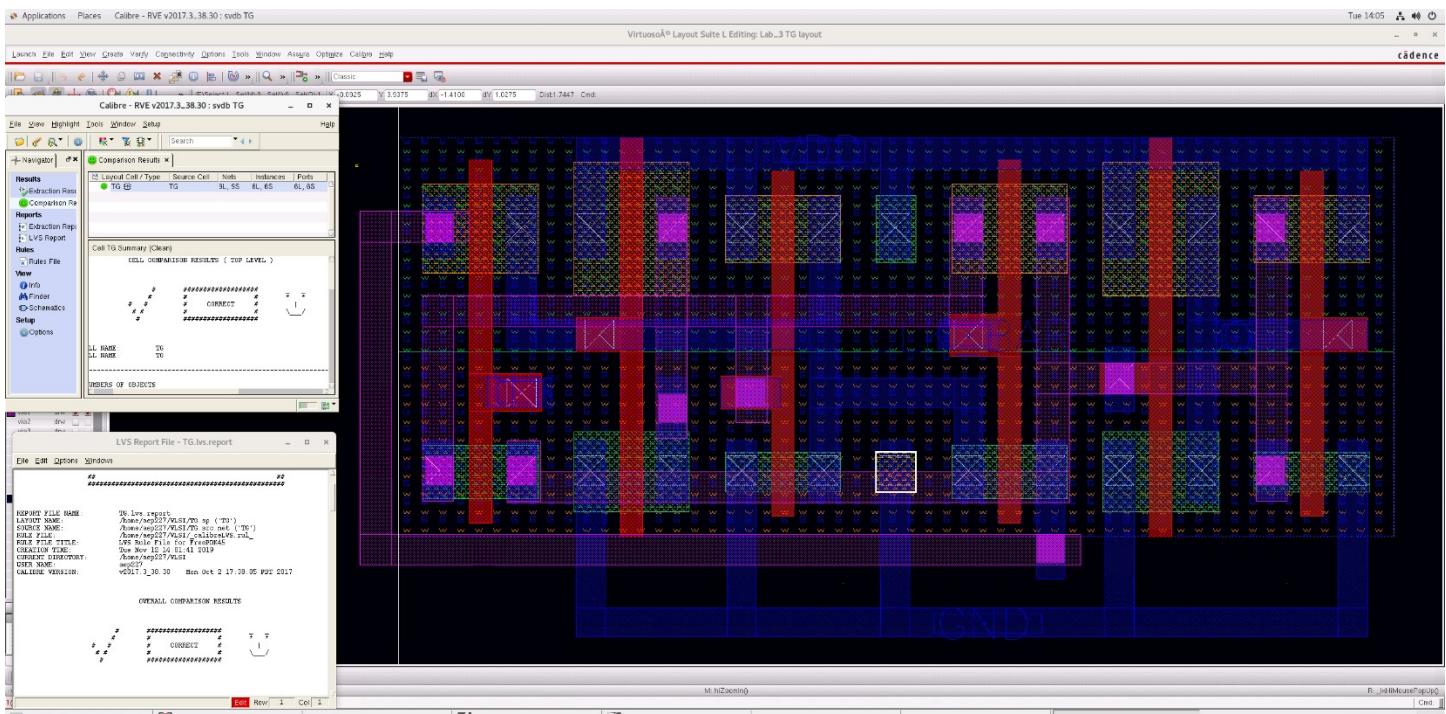


Final Device Layout

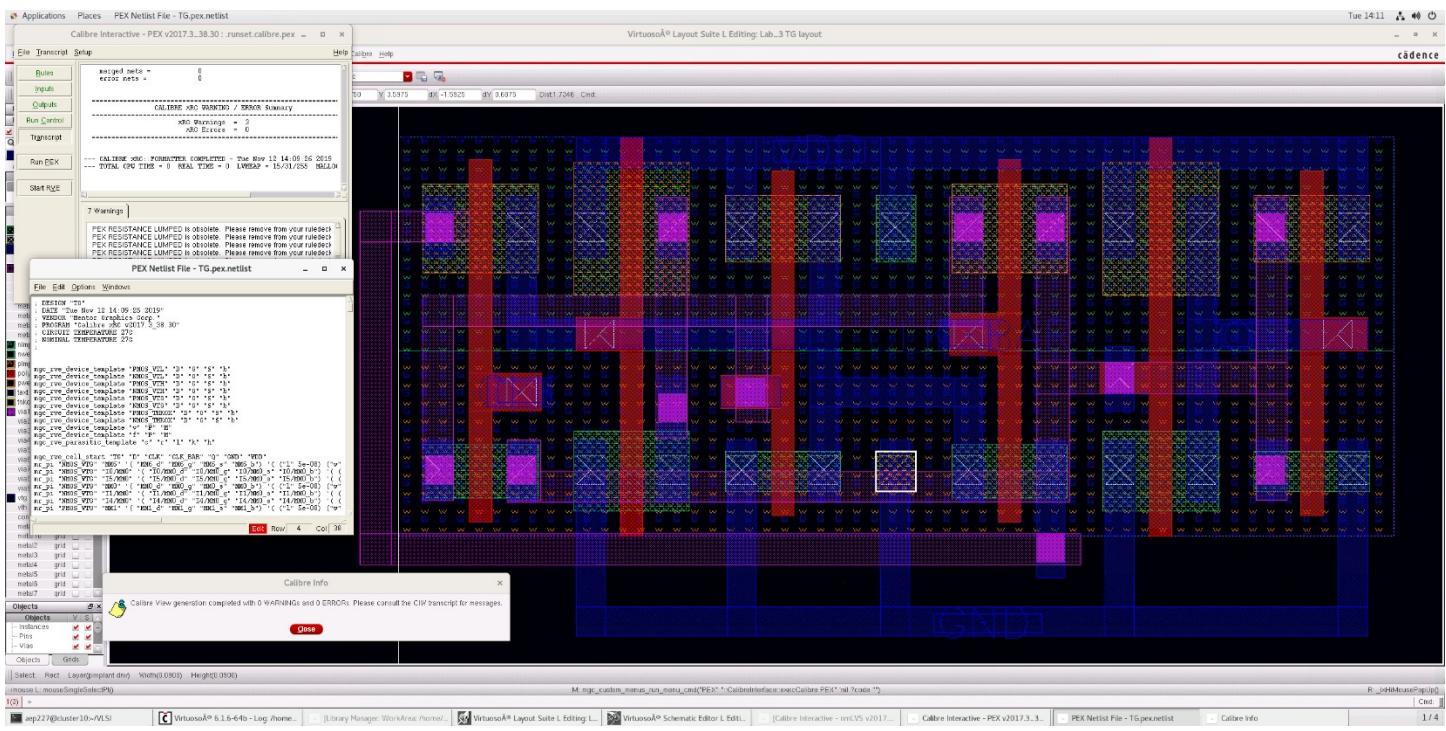
Post-Layout Simulation Results



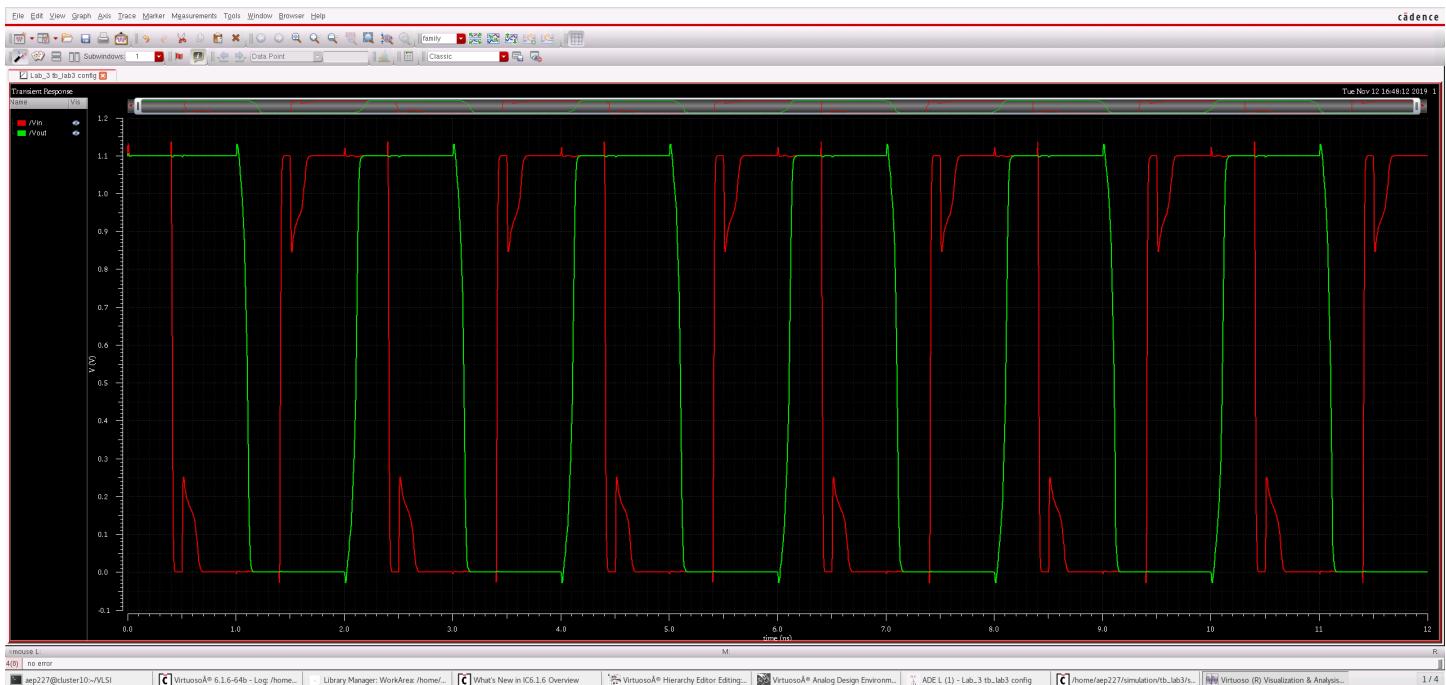
DRC Pass



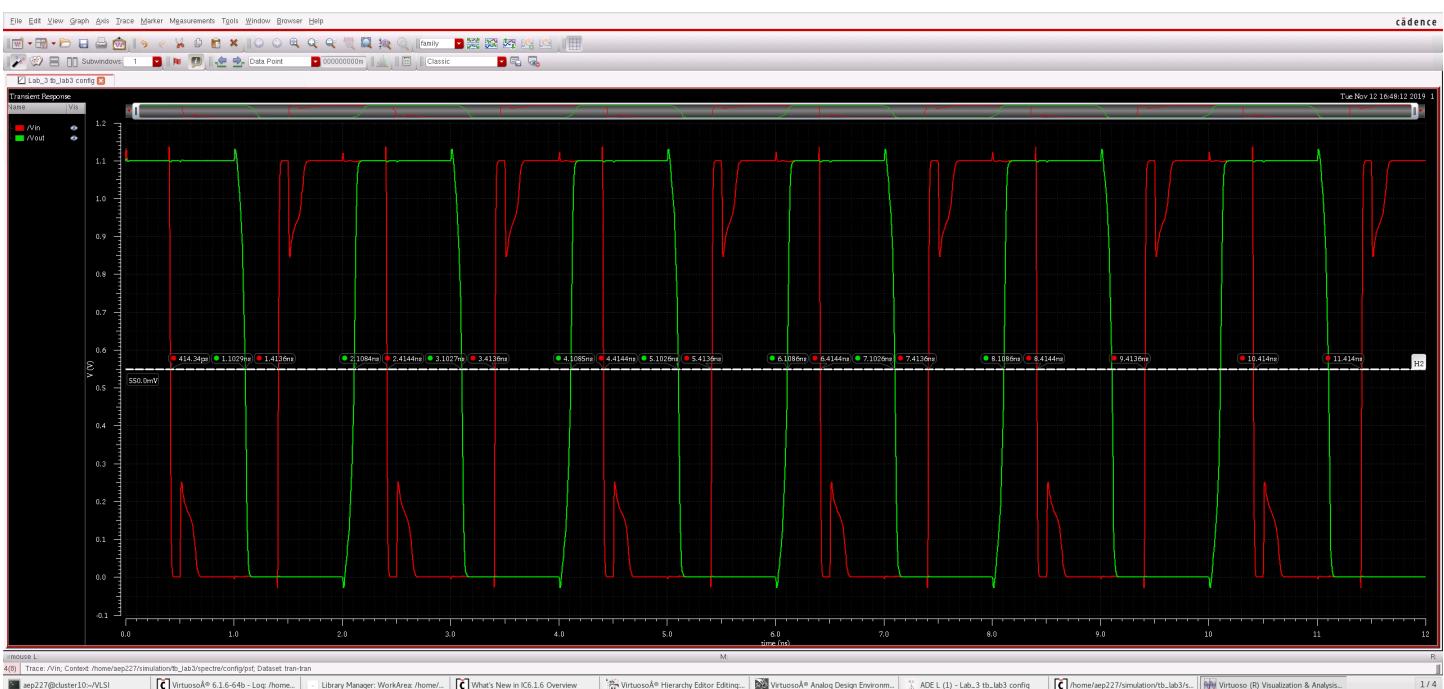
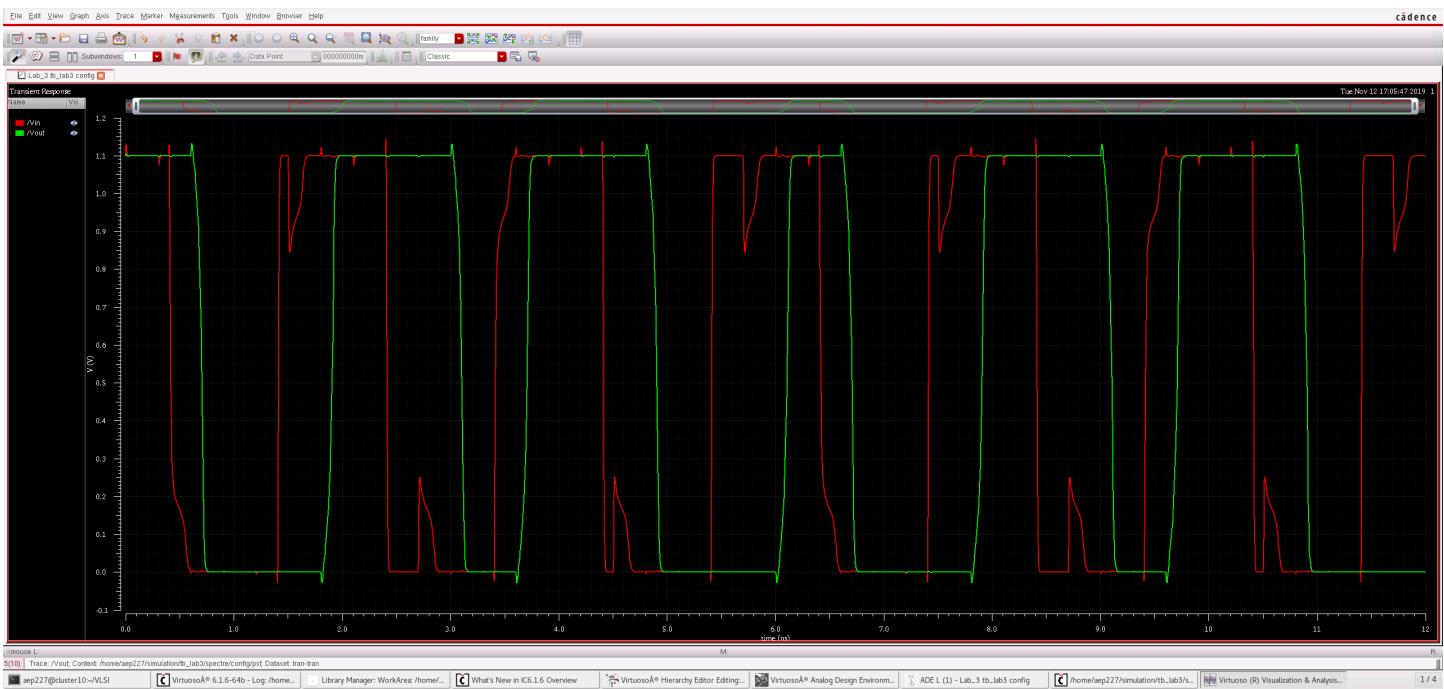
LVS Pass

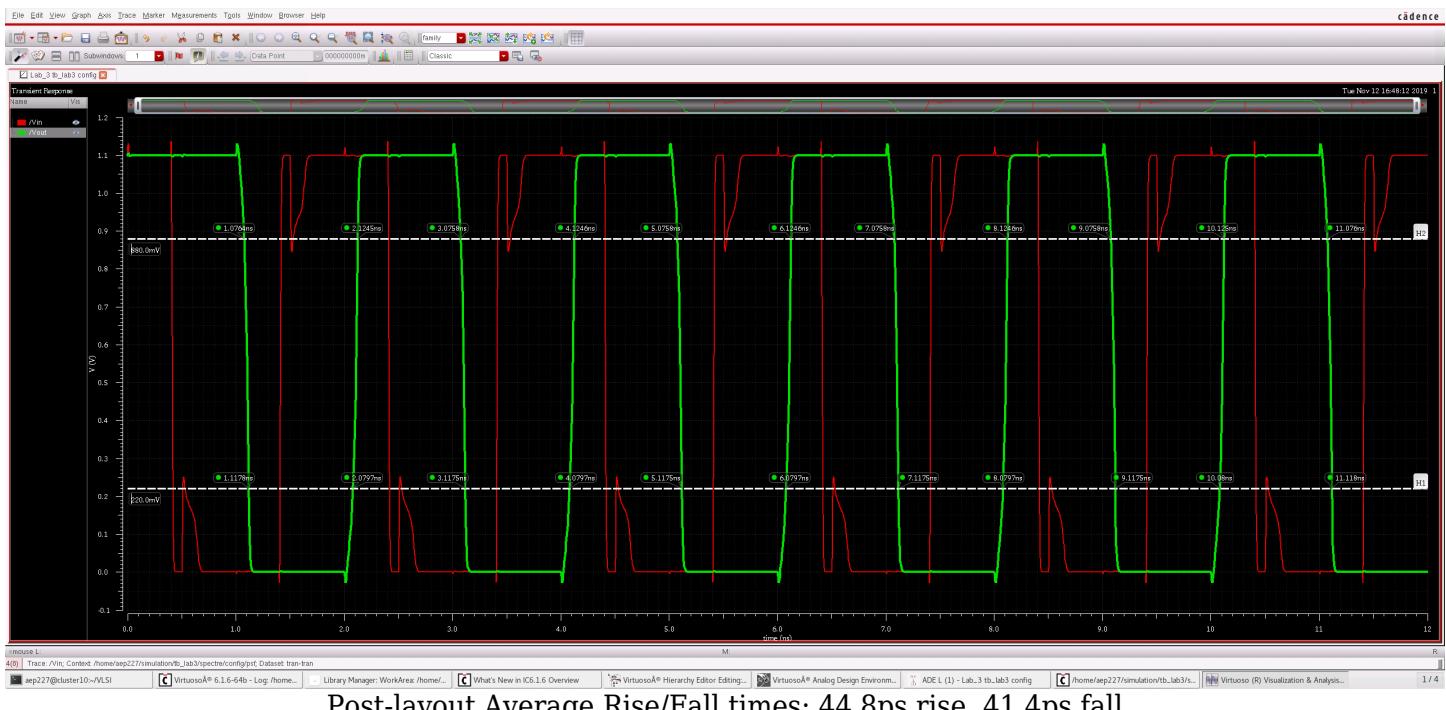


PEX Pass



Post-Layout Testbench Results at 85 degrees Celsius
1Ghz clock. Positive edges on the nanosecond, negative edges on the half nanosecond

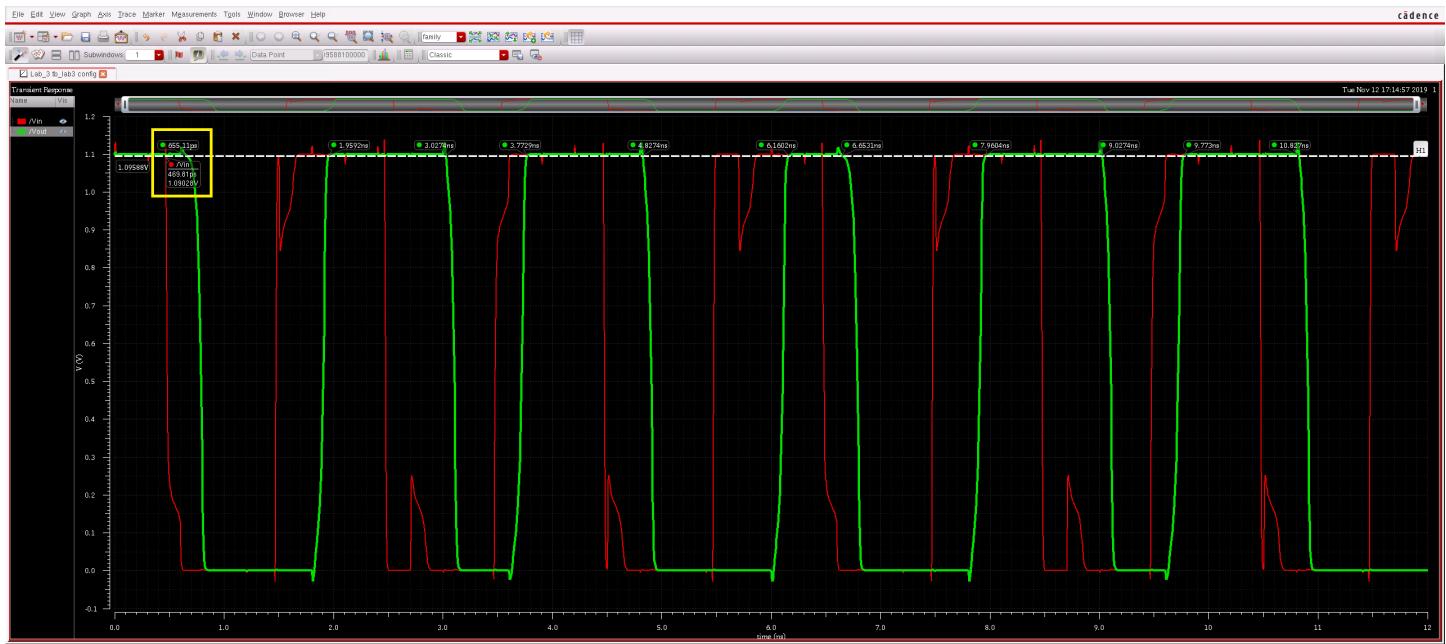




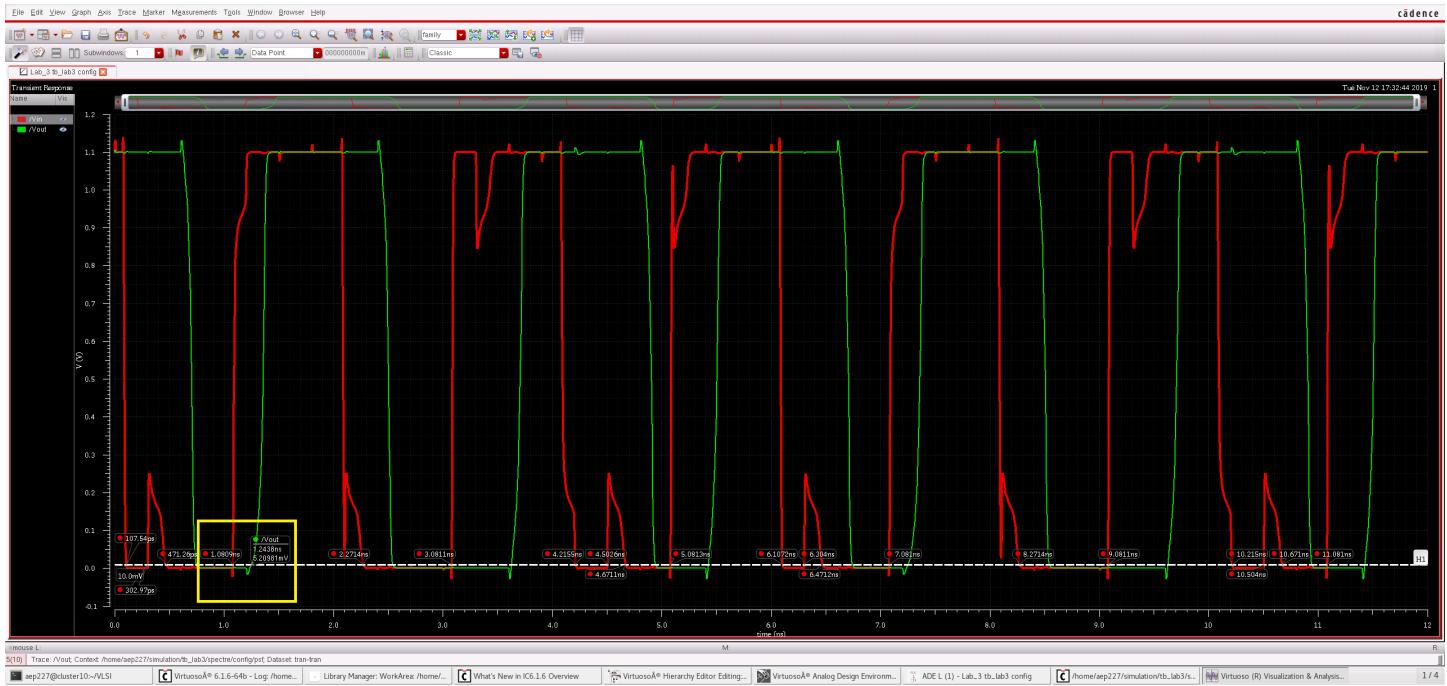
Post-layout Average Rise/Fall times: 44.8ps rise, 41.4ps fall

Setup and Hold Time Measurement

Note: All setup and hold time measurements were at the increased 1.66Ghz clock (600ps period). Positive clock edges occur at 600ps, 1.2ns, 1.8ns, etc. The setup and fall times were measured from these first two positive edges



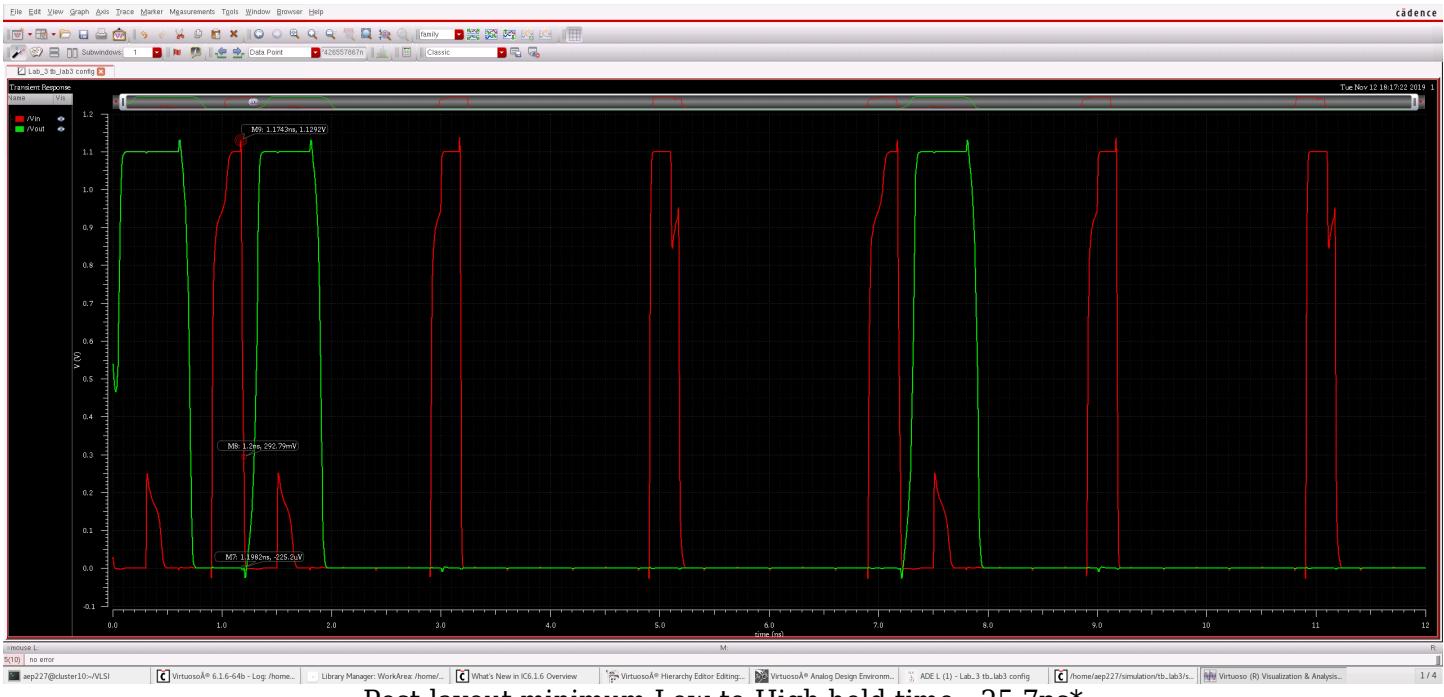
Post-layout Minimum High-to-Low setup time: 185.3ps



Post-layout Minimum Low-to-High setup time: 162.9ps



Post-layout minimum High-to-Low hold time: -20.66ps*



Post-layout minimum Low-to-High hold time: -25.7ps*

Summary of Times

	Pre-layout	Post-layout
Propagation Delay	60.76 ps	105.61 ps
Rise time	26.4 ps	44.8 ps
Fall time	25.2 ps	41.4 ps
Setup Time - High-to-Low	Not Measured	185.3 ps
Setup Time - Low-to-High	Not Measured	162.9 ps
Hold Time - High-to-Low	Not Measured	-20.66 ps*
Hold Time - Low-to-High	Not Measured	-25.7 ps*

*Having a “hold time” that came before the clock was a strange phenomenon. I was convinced there was either an error in the design of the circuit or my testing methodology, or a bug in the simulation. Upon researching the issue, I discovered that “setup” and “hold” times are relative concepts to the clock edge. Collectively they refer to a sampling window in which a device will read a value. Setup time being the earliest time of this window, while the hold time is the latest time of this window. The traditional convention is the positive setup time refers to time before the clock edge and a positive hold time refers to the time after the clock edge. Conversely, a negative setup time would be after the clock edge, while a negative hold time is before the clock edge. I discovered that it’s possible to have this sampling window be completely before the clock (positive setup, negative hold), “over” the clock (the traditional positive setup and hold), or entirely after the clock (negative setup, positive hold).

I tested as best I could to determine the value of this negative hold time, however there was a threshold where the input value was high enough that it could’ve been considered the beginning of the setup time. The values recorded here are a best guess where I felt the values could still be considered a hold time as opposed to a setup time.

**All tests were conducted at 85 degrees Celsius