

AEP227 Github Name

October 22, 2019

ECE 4540: VLSI Circuit Design

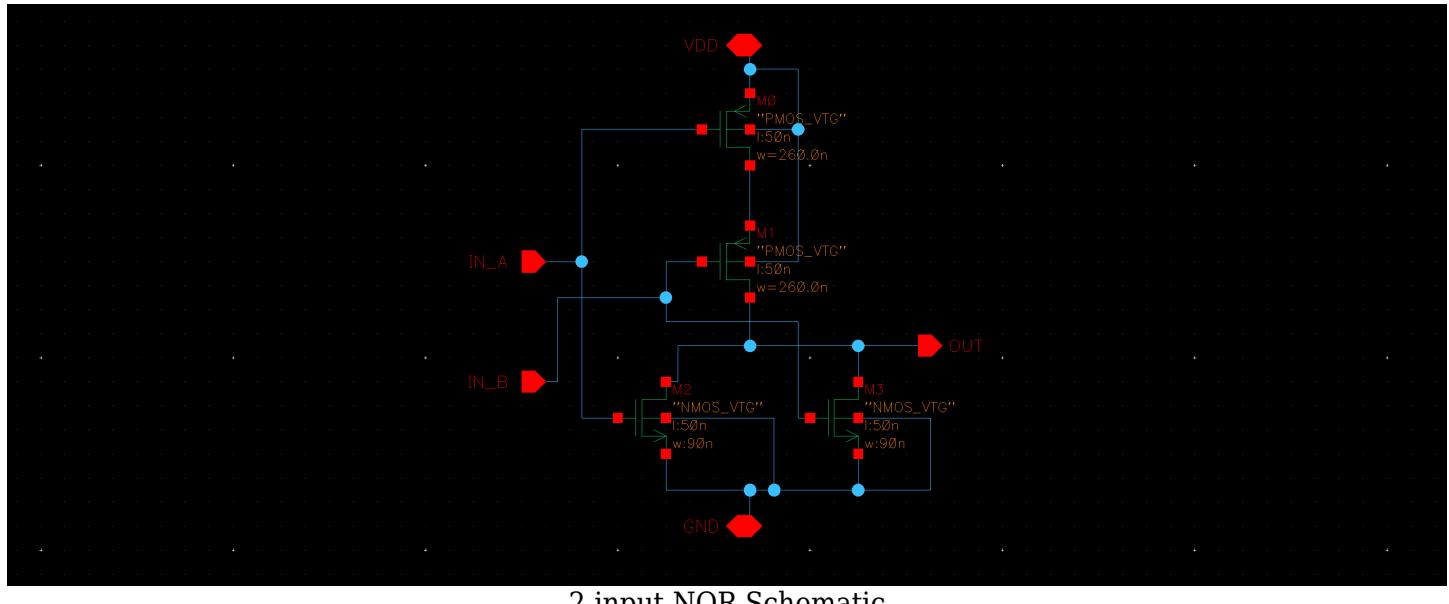
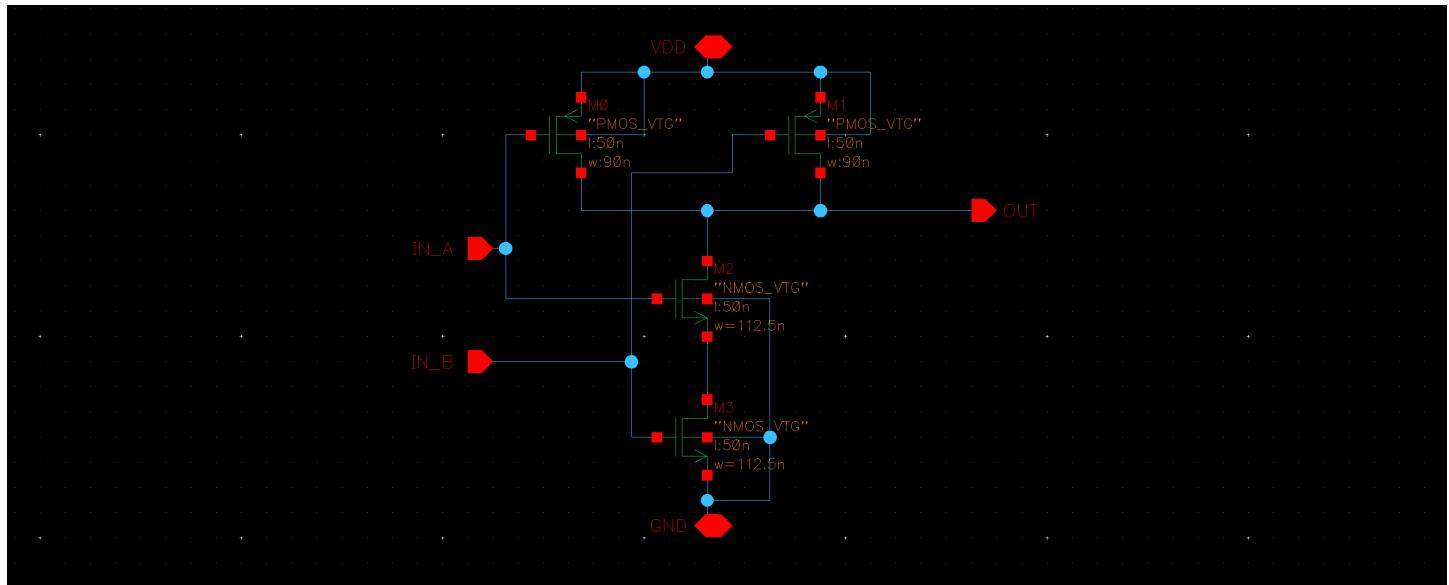
Lab 2 Report

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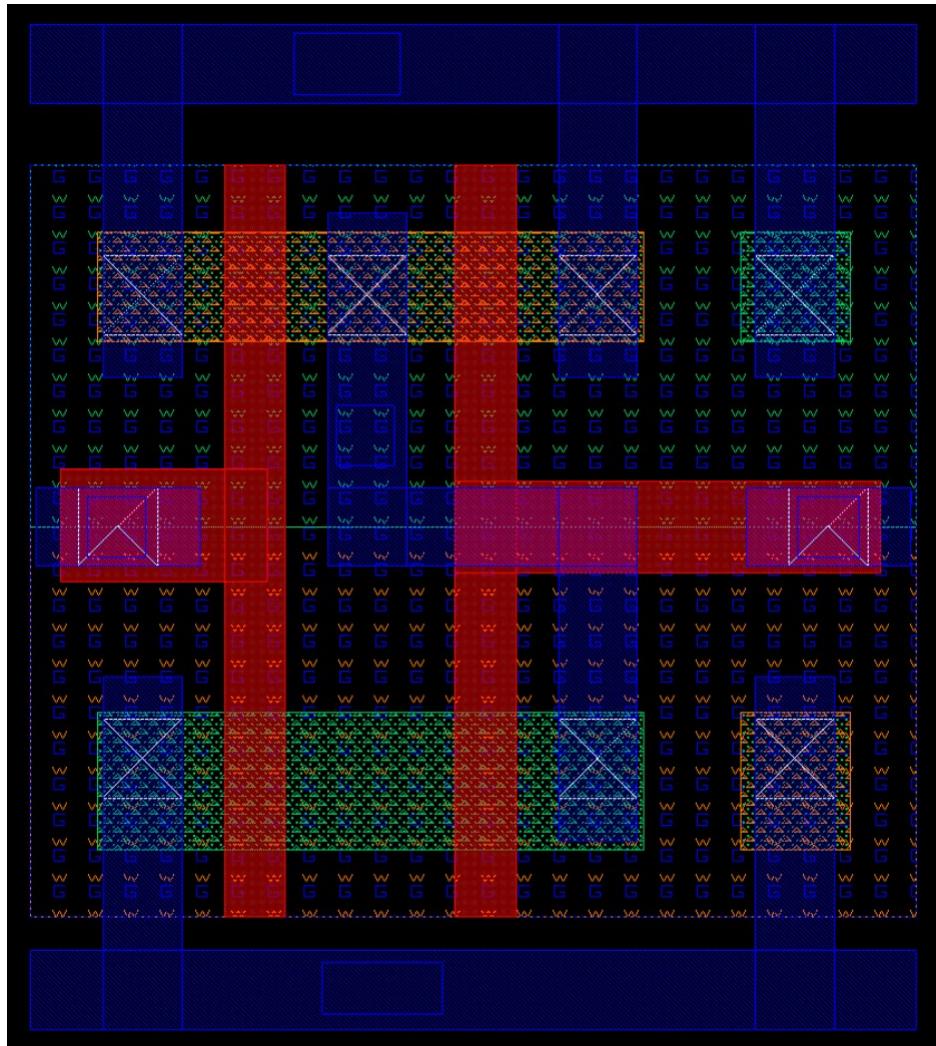
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Part 1: Symmetric NAND and NOR Gates

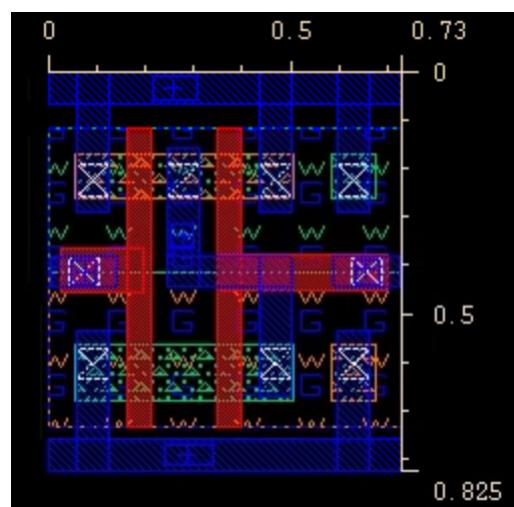
2-input NAND and 2-input NOR Schematics



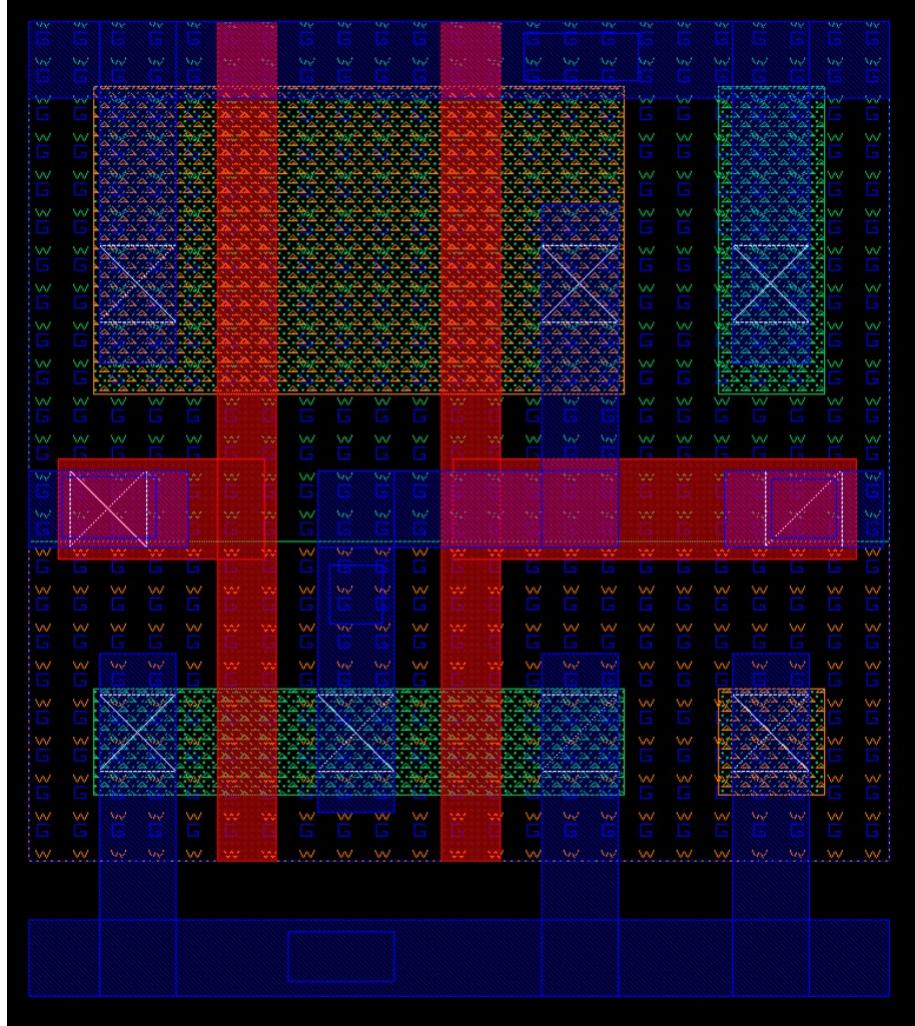
2-input NAND and 2-input NOR Layouts



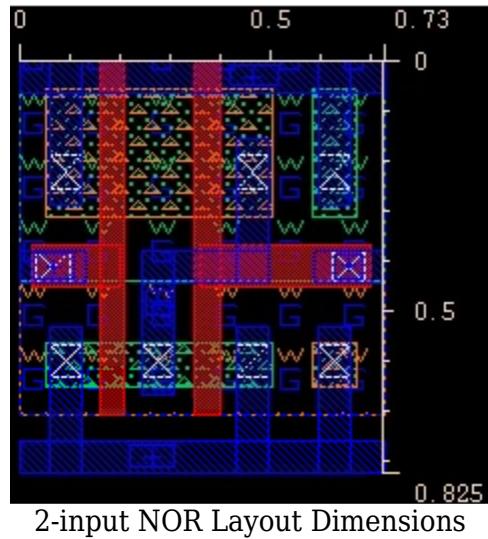
2-input NAND Layout



2-input NAND Layout Dimensions

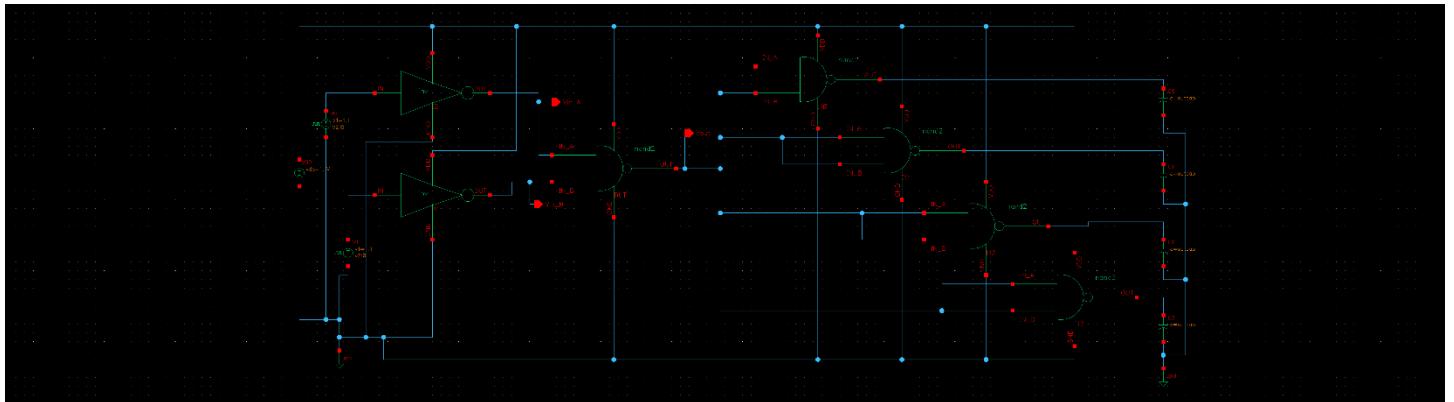


2-input NOR Layout

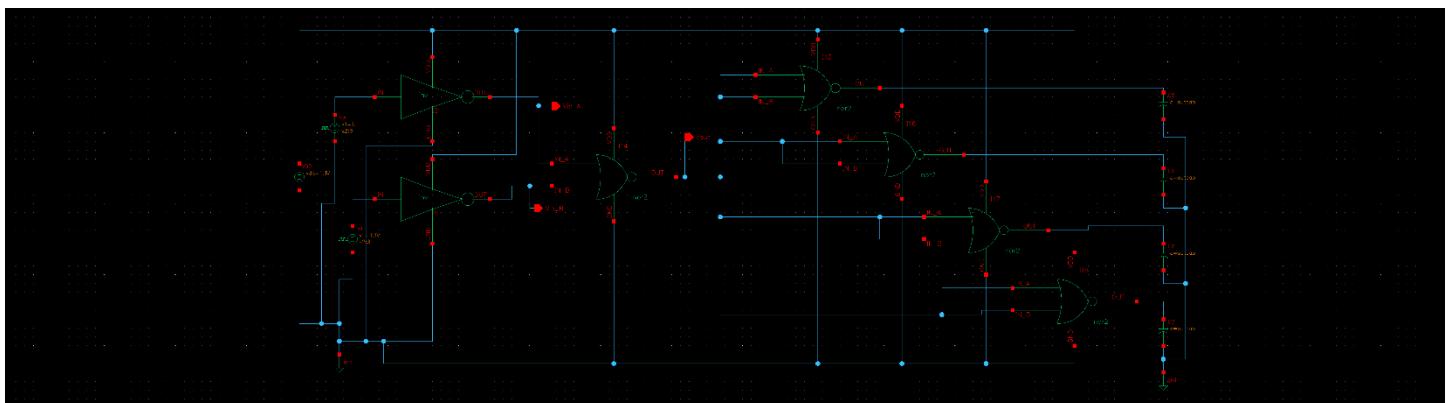


2-input NOR Layout Dimensions

Test Benches

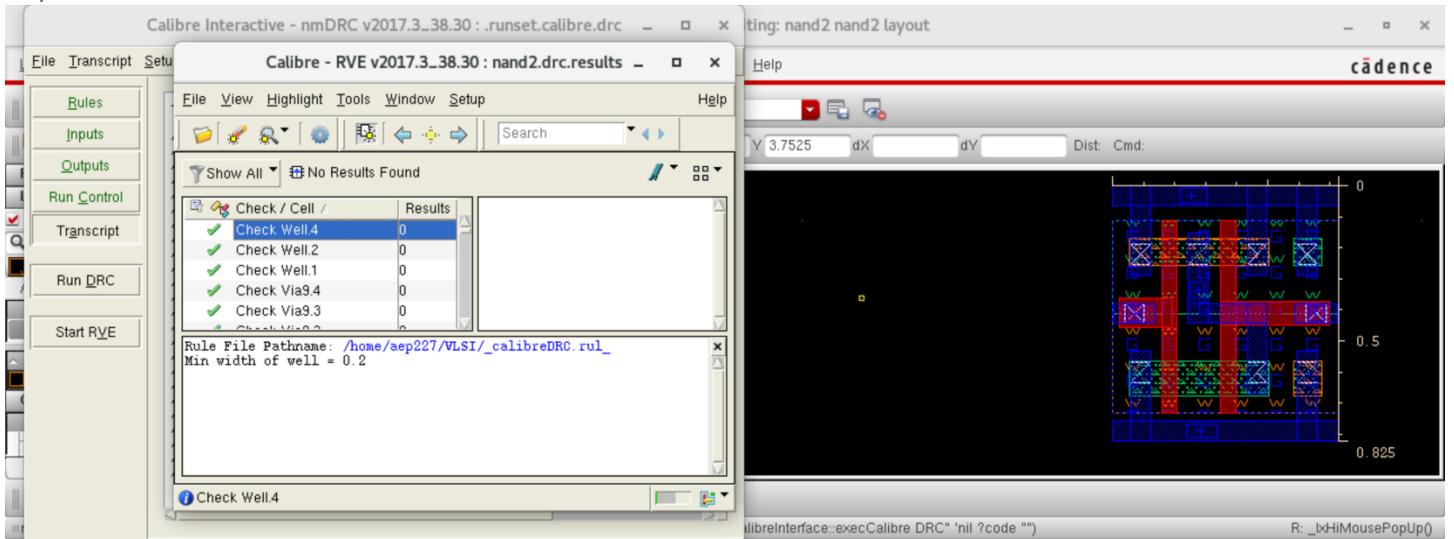


2-input NAND Test Bench

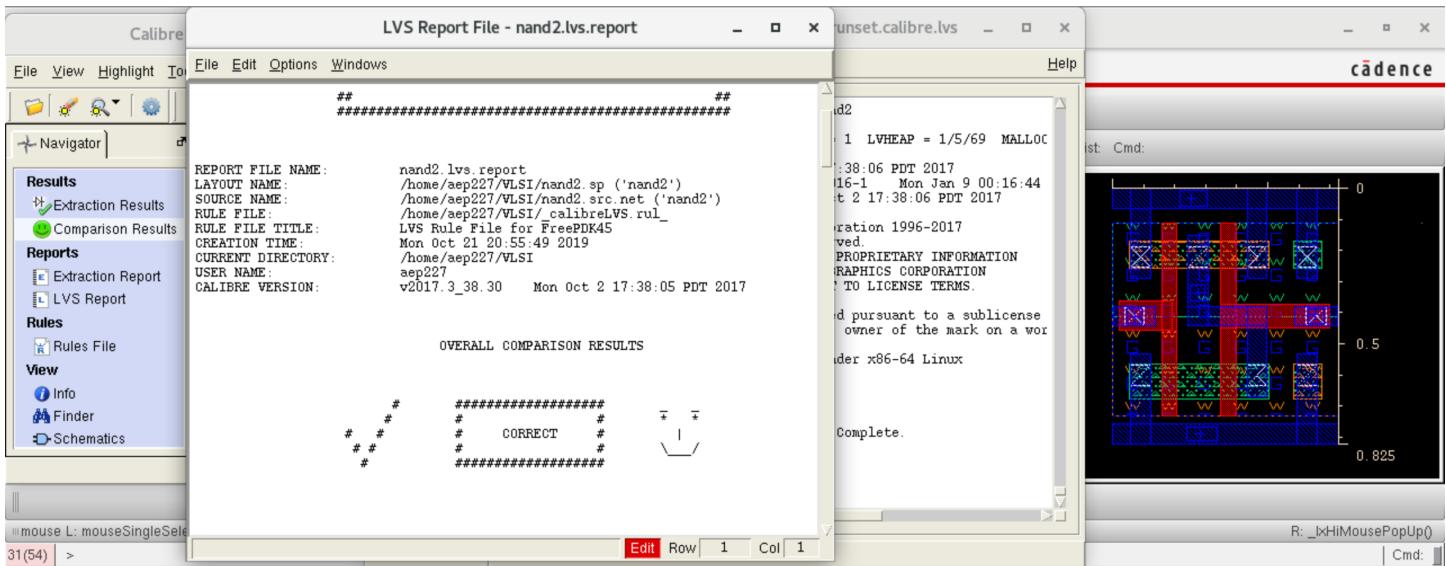


2-input NOR Test Bench

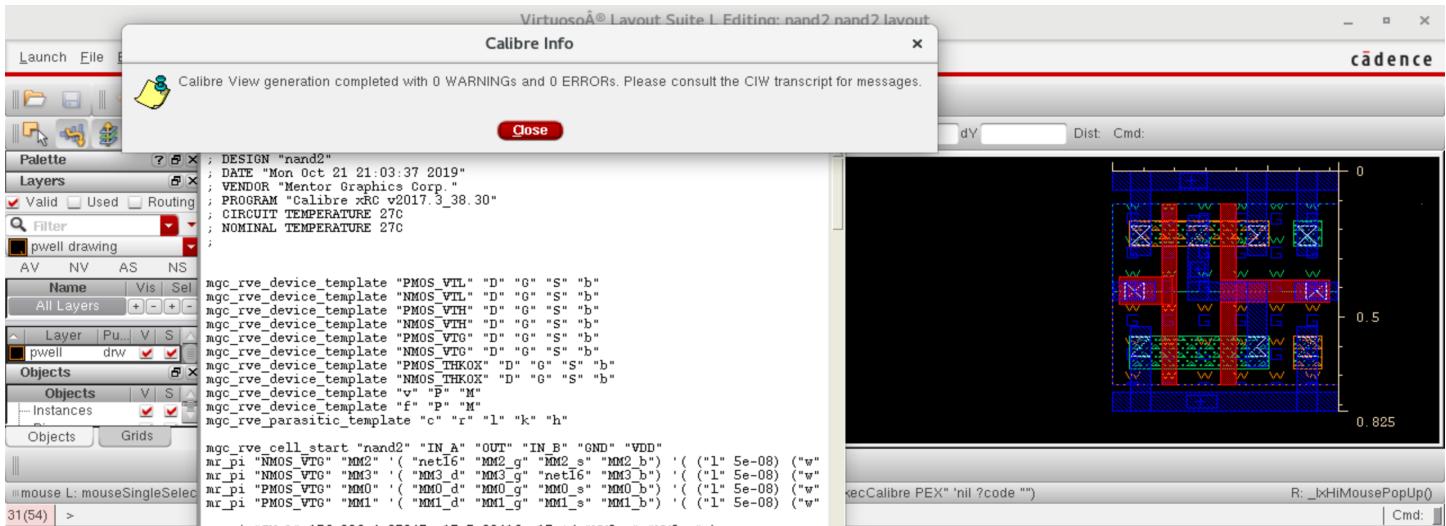
Layout Checks



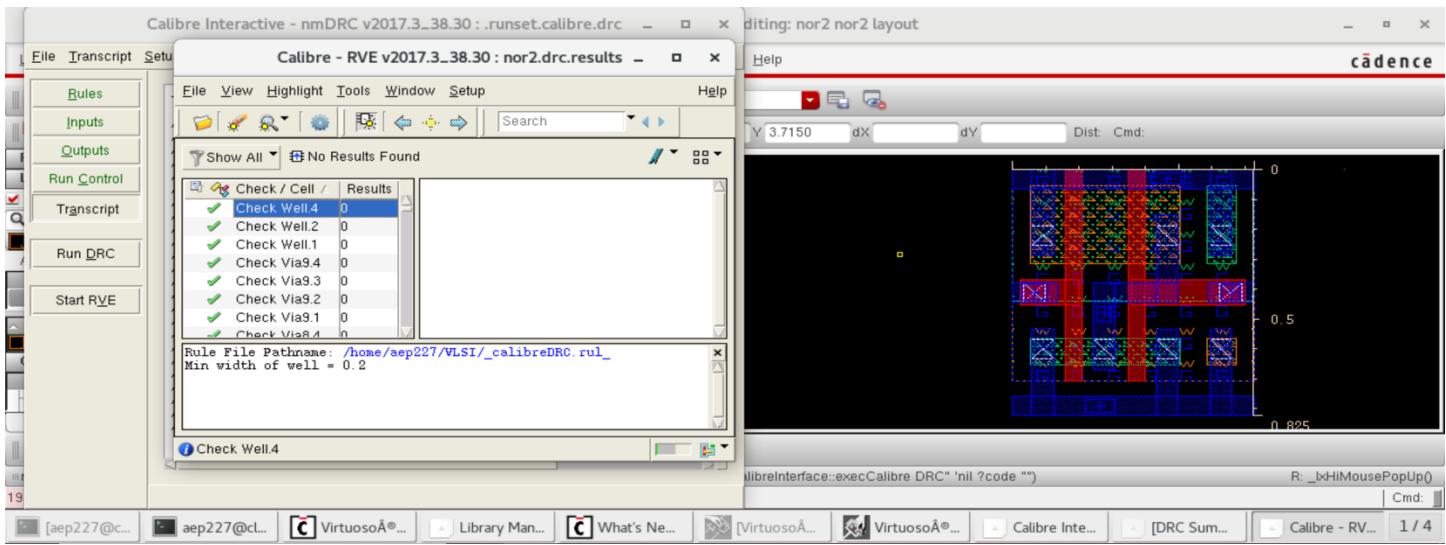
2-input NAND DRC Pass



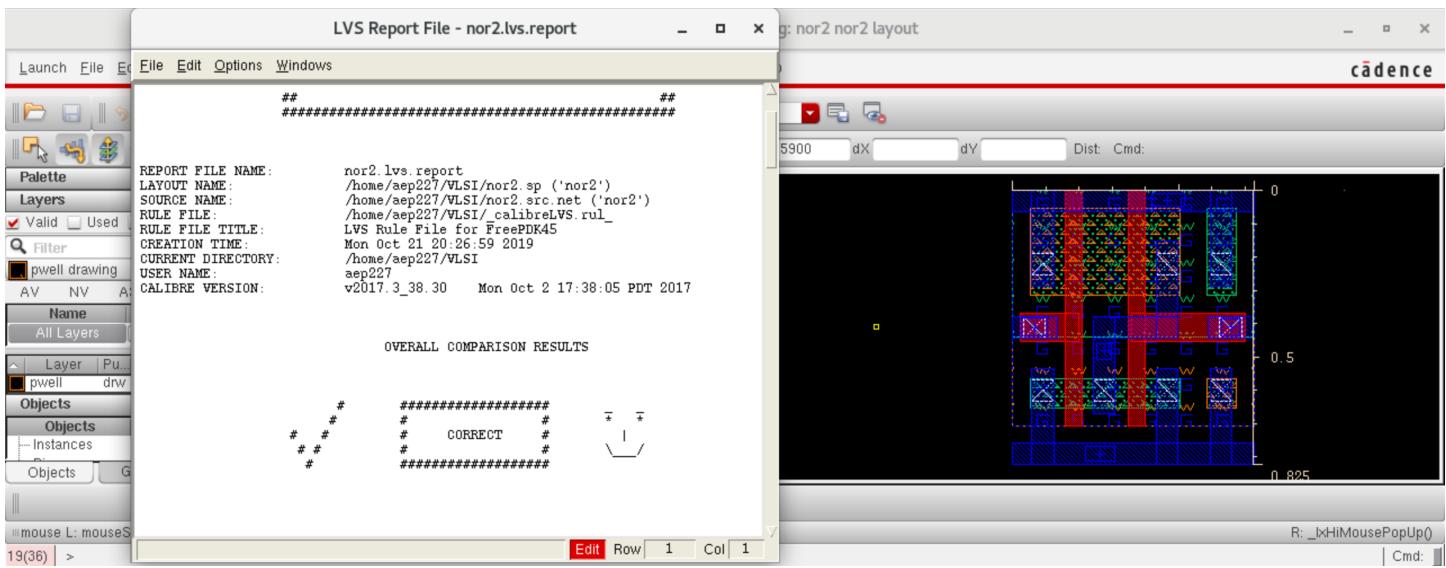
2-input NAND LVS Pass



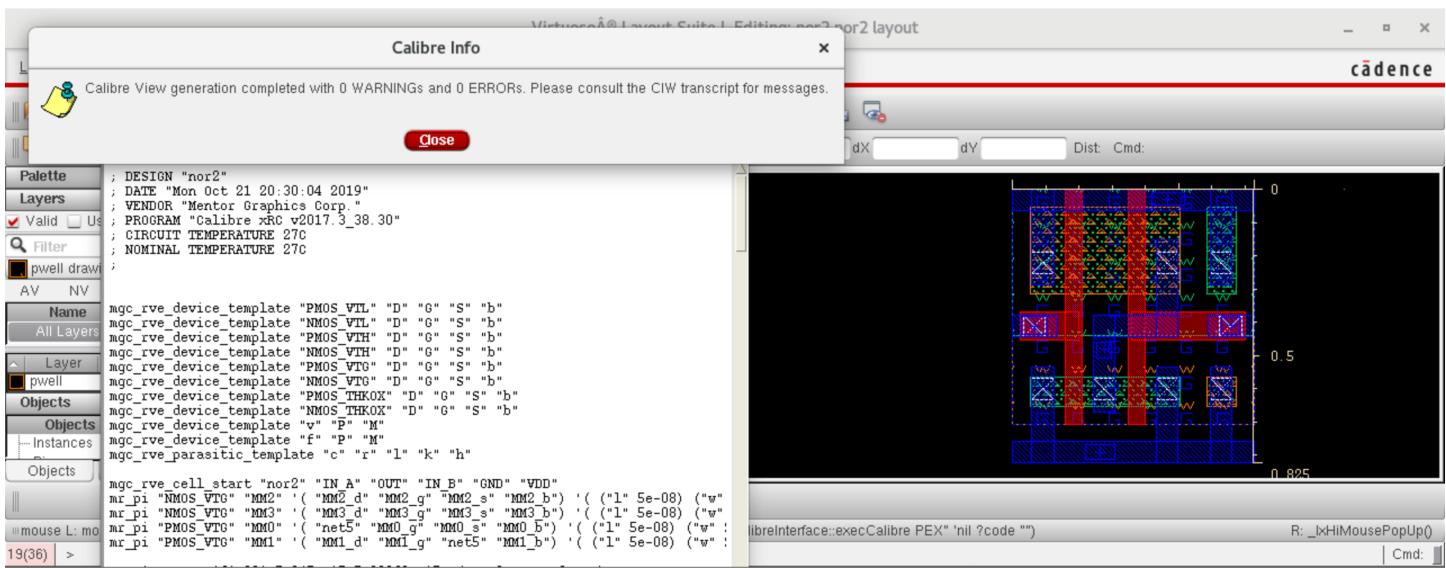
2-input NAND PEX Pass



2-input NOR DRC Pass



2-input NOR LVS Pass



2-input PEX Pass

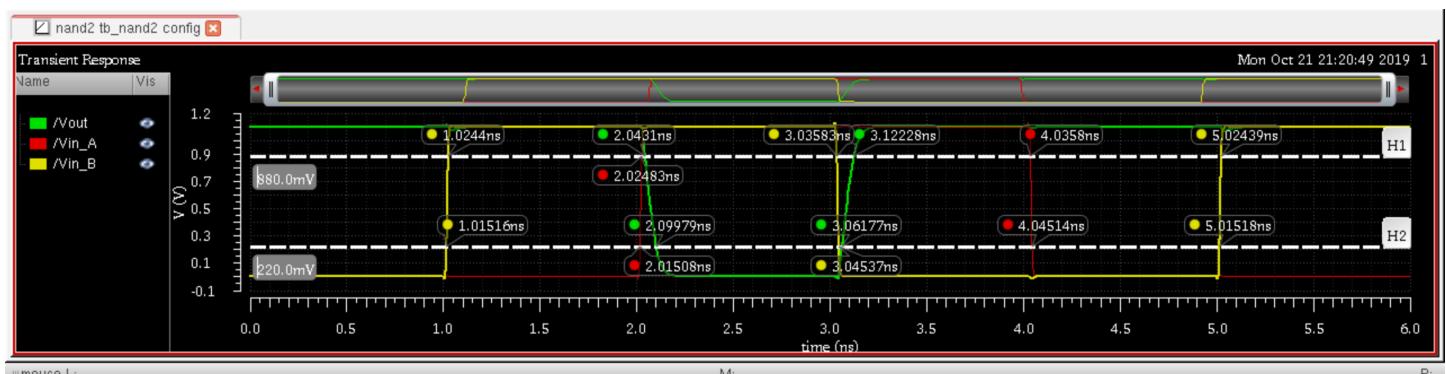
Post-Layout Characteristics



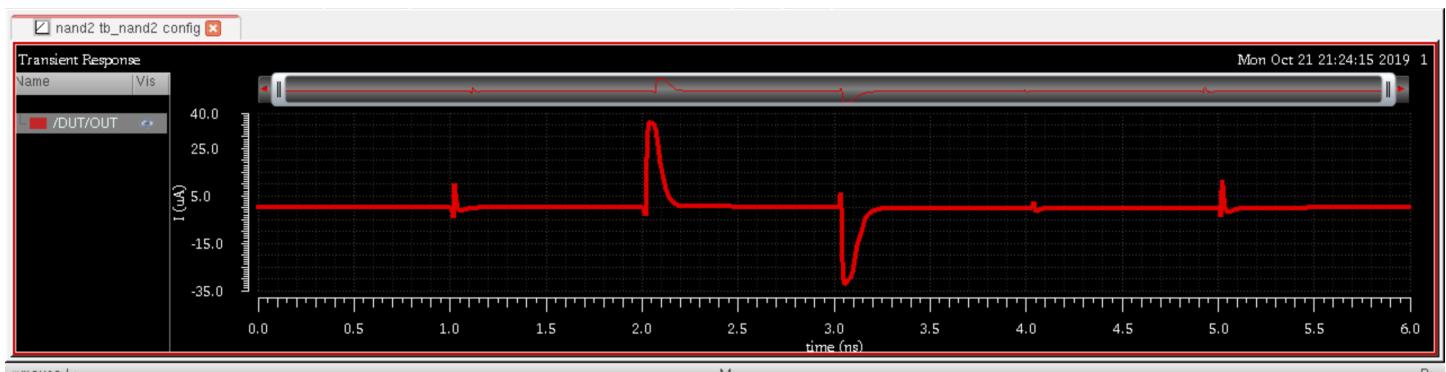
2-input NAND Output 1



2-input NAND Output 2



2-input NAND Output 3



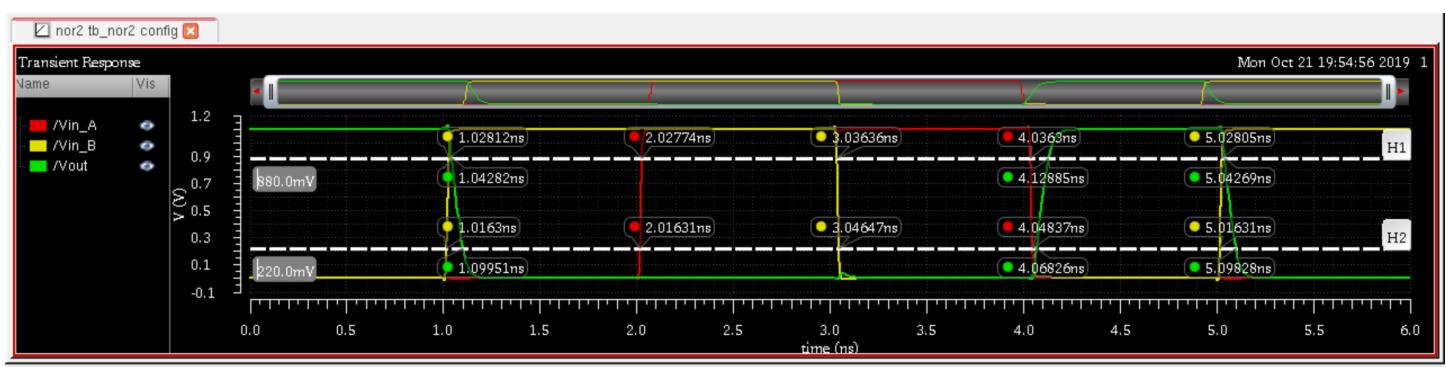
2-input NAND Output Current



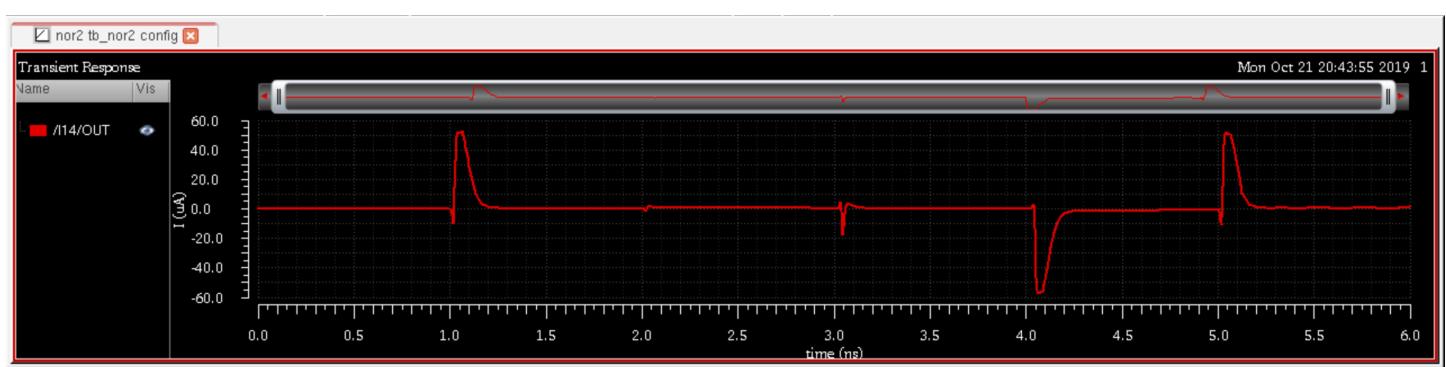
2-input NOR Output 1



2-input NOR Output 2



2-input NOR Output 3



2-input NOR Output Current

NAND2

VOH: 916.743mV	VIH: 583.122 mV
VOL: 188.747mV	VIL: 652.433 mV
Noise Margin Low-to-High: 463.686mV	
Noise Margin High-to-Low: 333.621mV	
Rise Time: 60.51ps	
Fall Time: 56.69ps	
Average Propagation Delay: 47.385ps	
Area: 602,250 nm ²	
Area-Delay Product: 28,537,616.25 ps*nm ²	
Peak Positive Power: 35.2 uA * VDD(1.1V) = 38.72 uW	
Peak Negative Power: -33.4 uA * VDD(1.1V) = -36.74 uW	

NOR2

VOH: 872.690mV	VIH: 500.253mV
VOL: 101.671mV	VIL: 582.513mV
Noise Margin Low-to-High: 480.842 mV	
Noise Margin High-to-Low: 372.437 mV	
Rise Time: 60.59ps	
Fall Time: 56.14ps	
Average Propagation Delay: 49.405ps	
Area: 602,250 nm ²	
Area-Delay Product: 29,754,161.25 ps*nm ²	
Peak Positive Power: 53.7 uA * VDD(1.1V) = 59.07 uW	
Peak Negative Power: -56.1 uA * VDD(1.1V) = -61.71 uW	

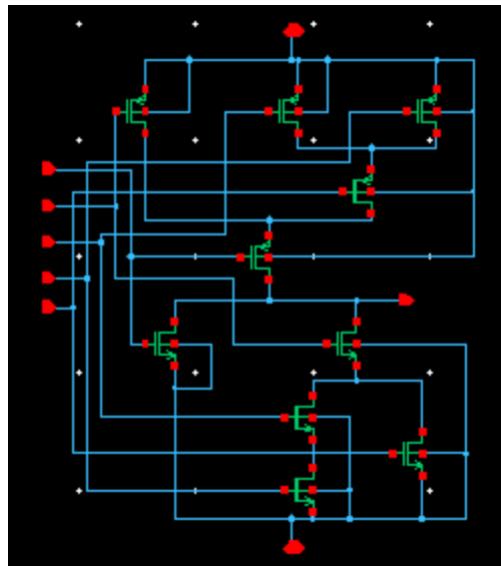
From the above data, 2-input NAND gates are more efficient than 2-input NOR gates, both in terms of ADP and power consumption. The NOR has a slight edge in noise margins, however. Overall, I'd prefer to build with just NANDs. I believe I could make my NAND layout smaller with more time, and after seeing the post-layout simulations, I believe there are some major optimizations I can make to the performance of the NAND.

I know in class we discussed how NANDs are usually faster due to the slightly wider NMOS's needed compared to much wider PMOS's needed for the NORs.

My above data has me concerned with my overall design. Pre-layout simulations showed good propagation delays with the widths I choose, even with the large decrease in PMOS width I choose in the NOR design (260nm from 300nm from what I initially calculated). Propagation delays were around 26ps for the NAND and 29ps for the NOR. I wasn't expecting that to almost double after the layout/PEX. My inverter design in the previous lab didn't see such drastic changes in performance either, so I'm left stumped as to the cause of the poor performance of my design.

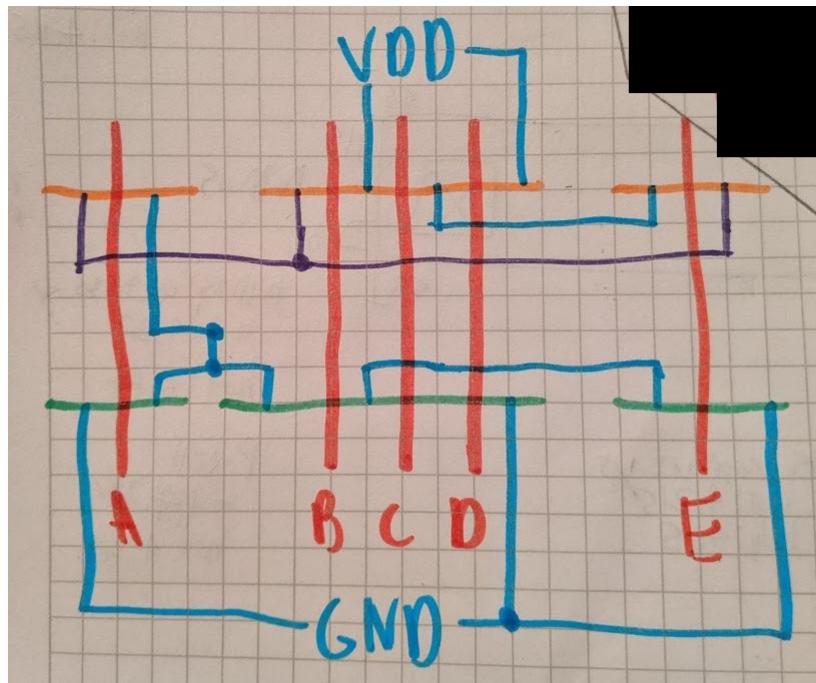
Part 2: Compound Gate

Schematic



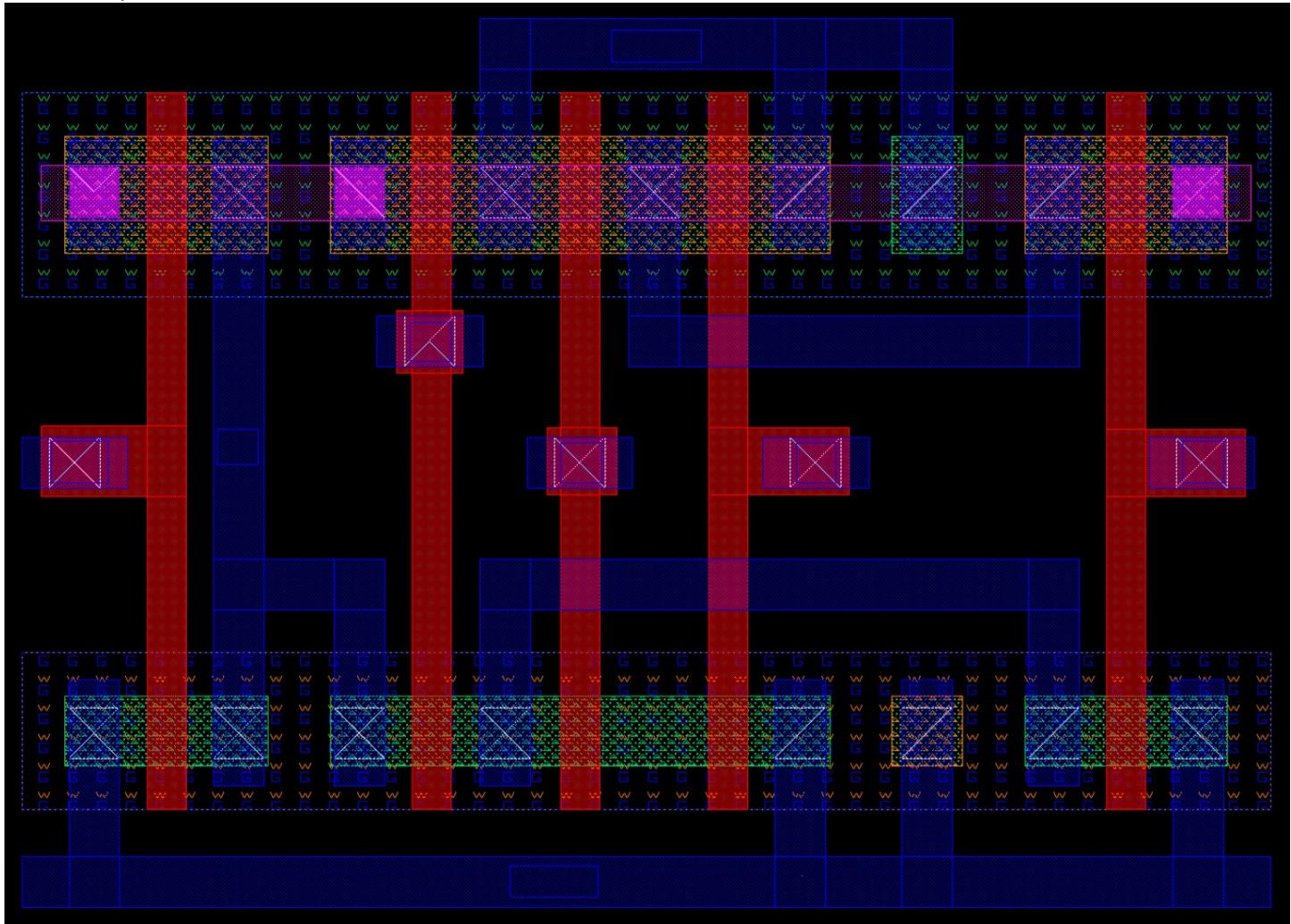
Complex Gate Schematic

Stick Diagram

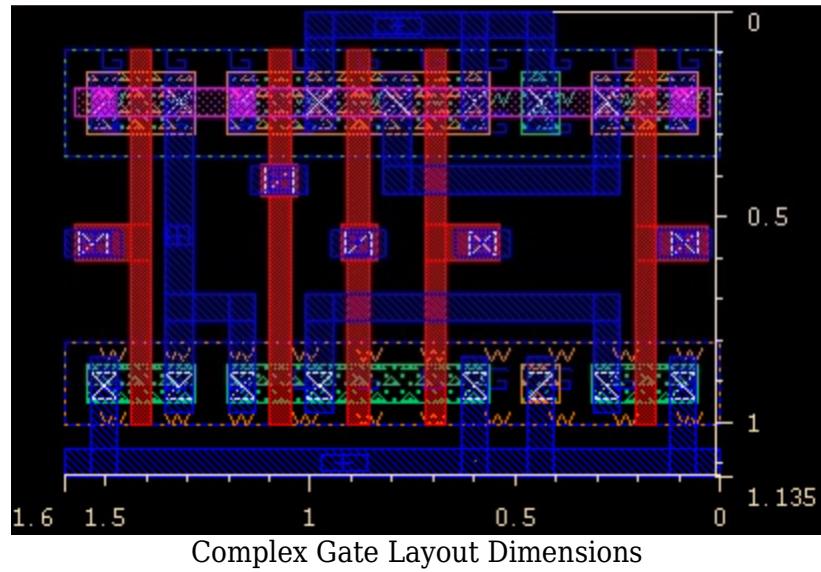


Complex Gate Stick Diagram

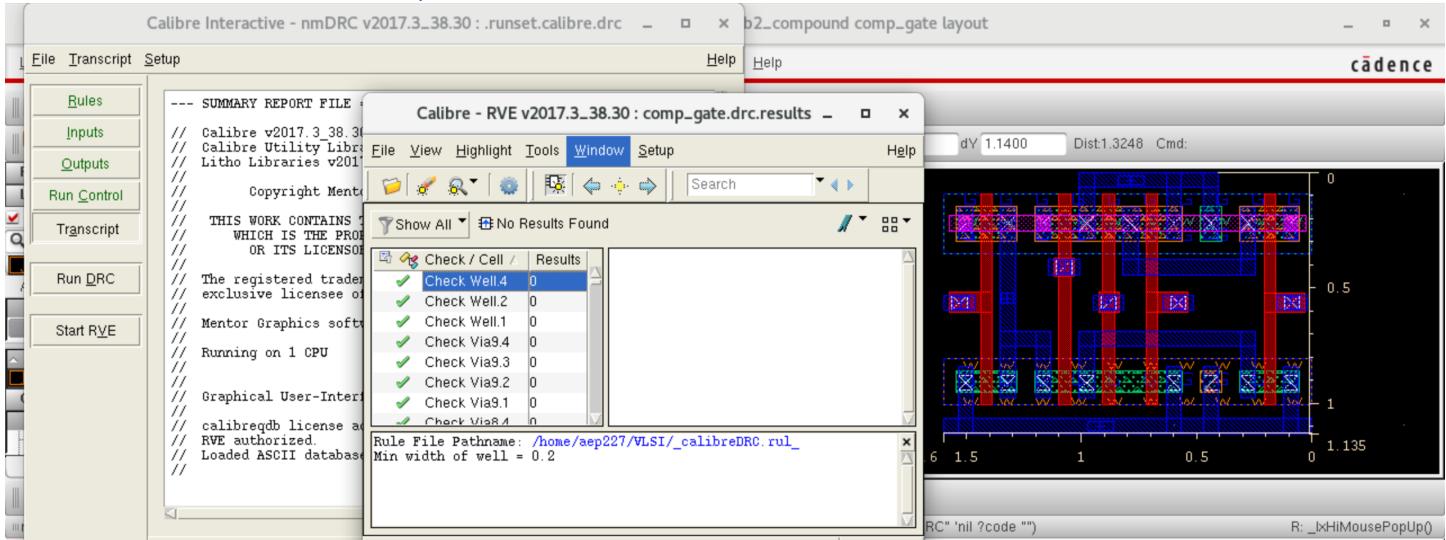
Layout



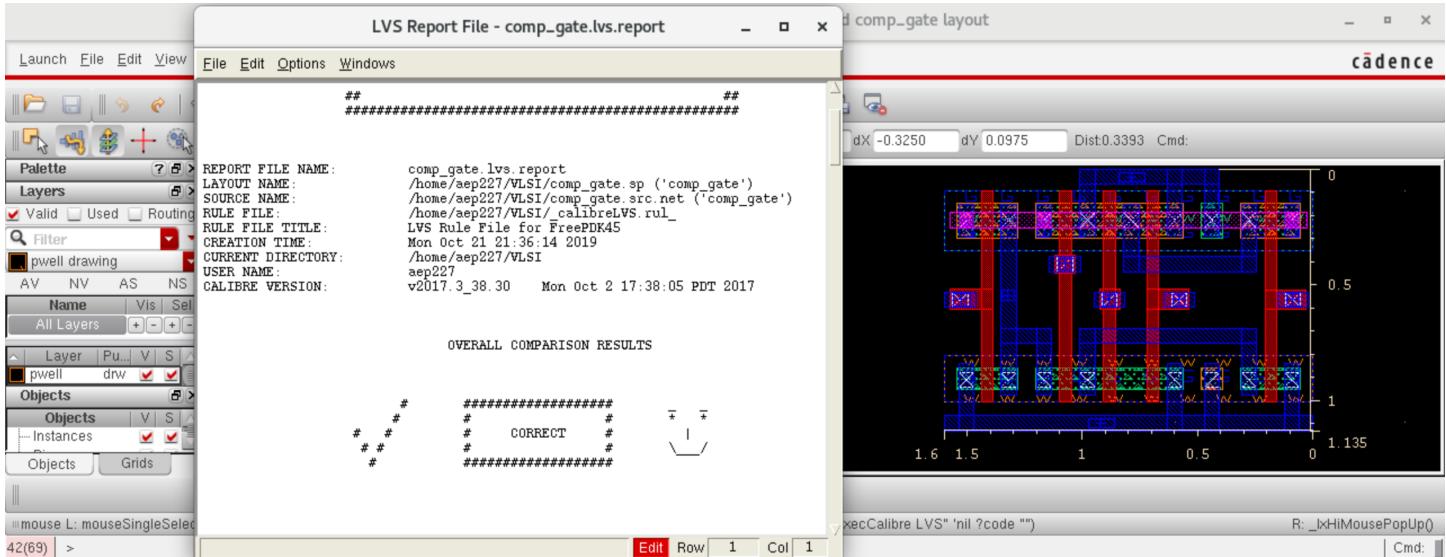
Complex Gate Layout



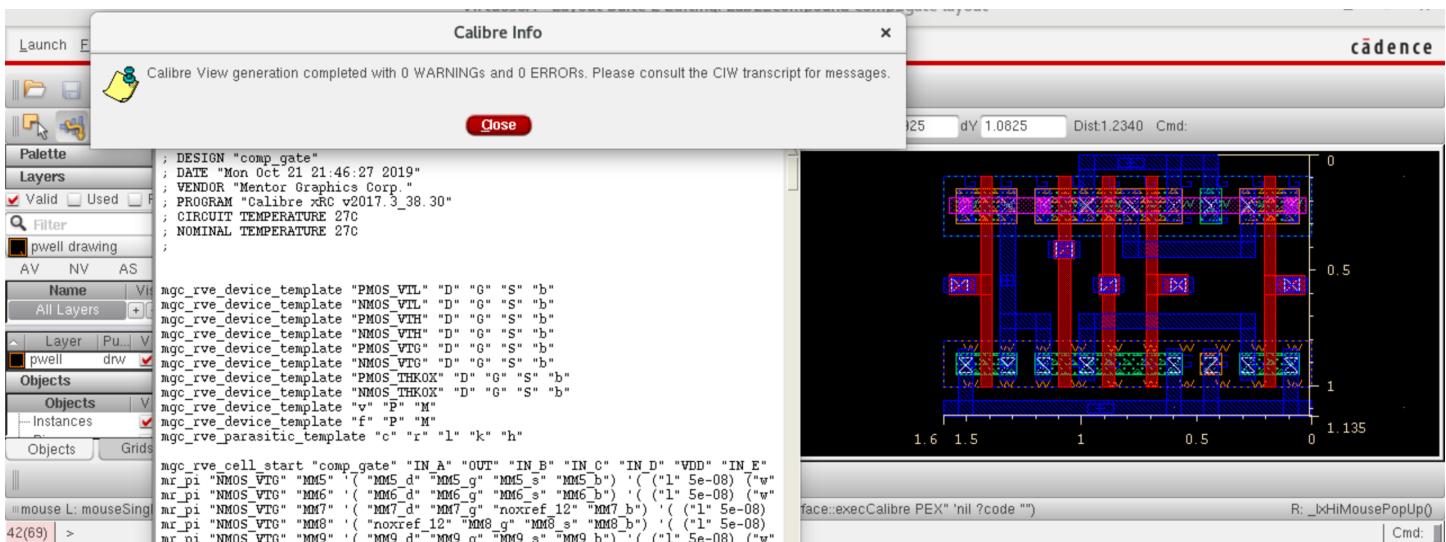
Testbench and Post-Layout Characteristics



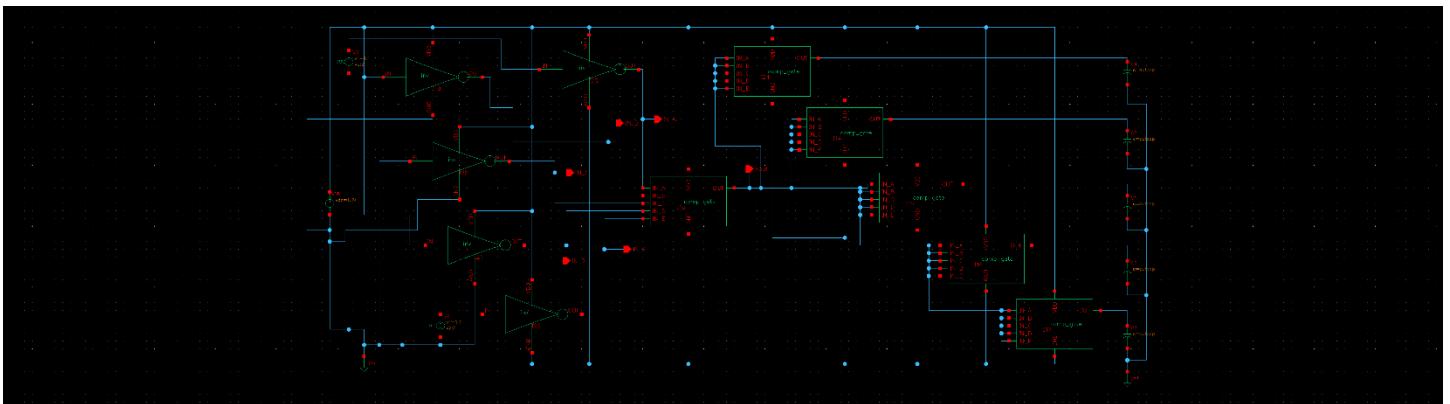
Complex Gate DRC Pass



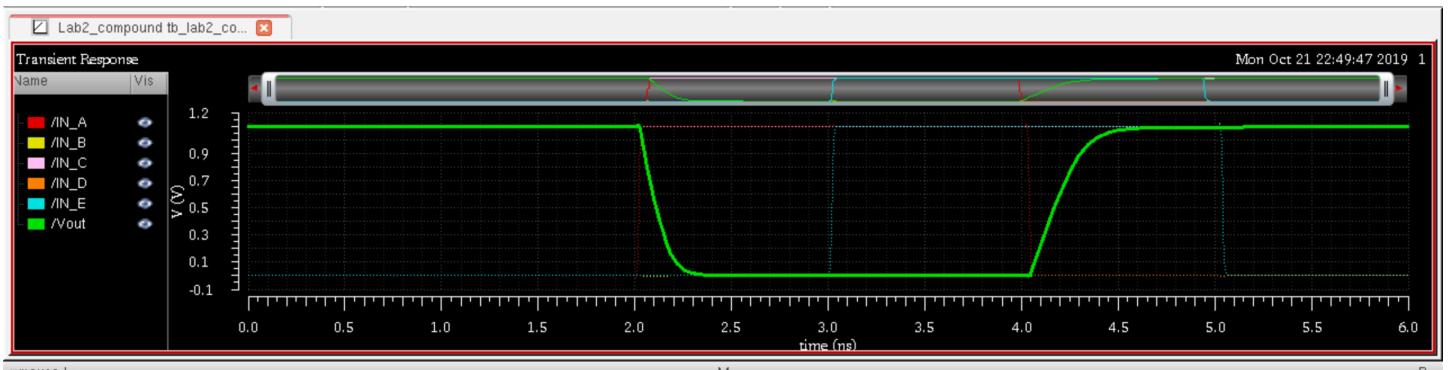
Complex Gate LVS Pass



Complex Gate PEX Pass



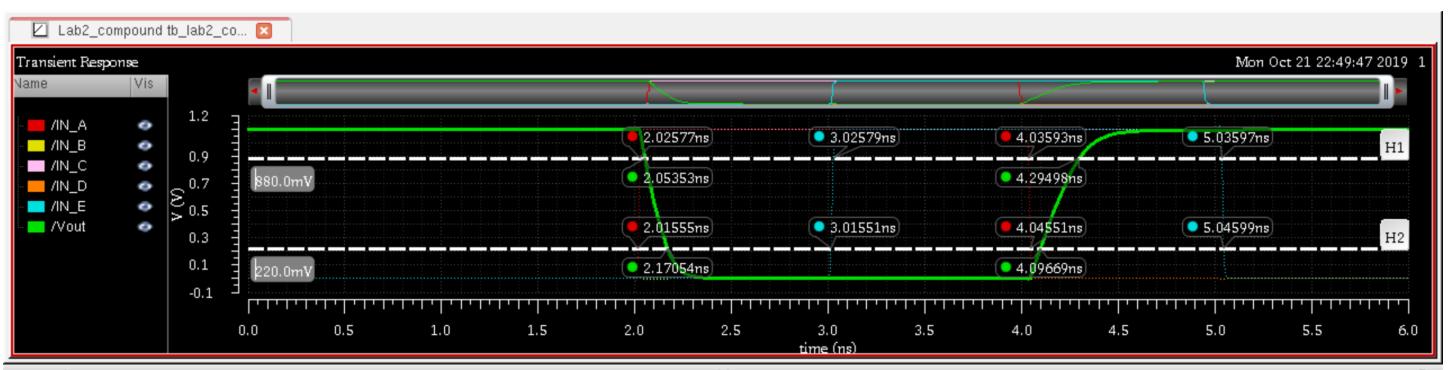
Complex Gate Test Bench



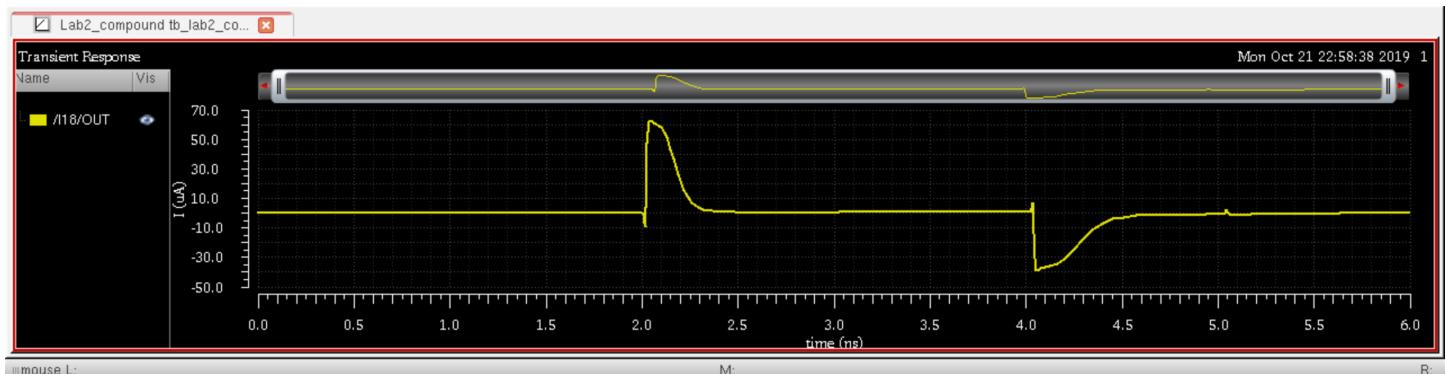
Complex Gate Output 1



Complex Gate Output 2



Complex Gate Output 3



Complex Gate Output Current

Average Propagation Delay: 112.76ps

Rise Time: 198.29ps

Fall Time: 117.01ps

Area: 1,816,000 nm²

Area Product Delay: 204,772,160 ps*nm²

Peak Positive Power: 63.1 uA * VDD(1.1V) = 69.41 uW

Peak Negative Power: -39.8 uA * VDD(1.1V) = -43.78 uW

For inputs, I choose a simple 5 input case of 00100->10100->10101->00101. This allowed for some simple testing of the proper function of the gate, as well as including a rise and fall in the output to test the times. It also allowed for a simpler testbench, with the inverter driving input C being grounded and the inverters driving inputs B and D being powered. Only two vpulse sources were needed for the changing signals in inputs A and E.