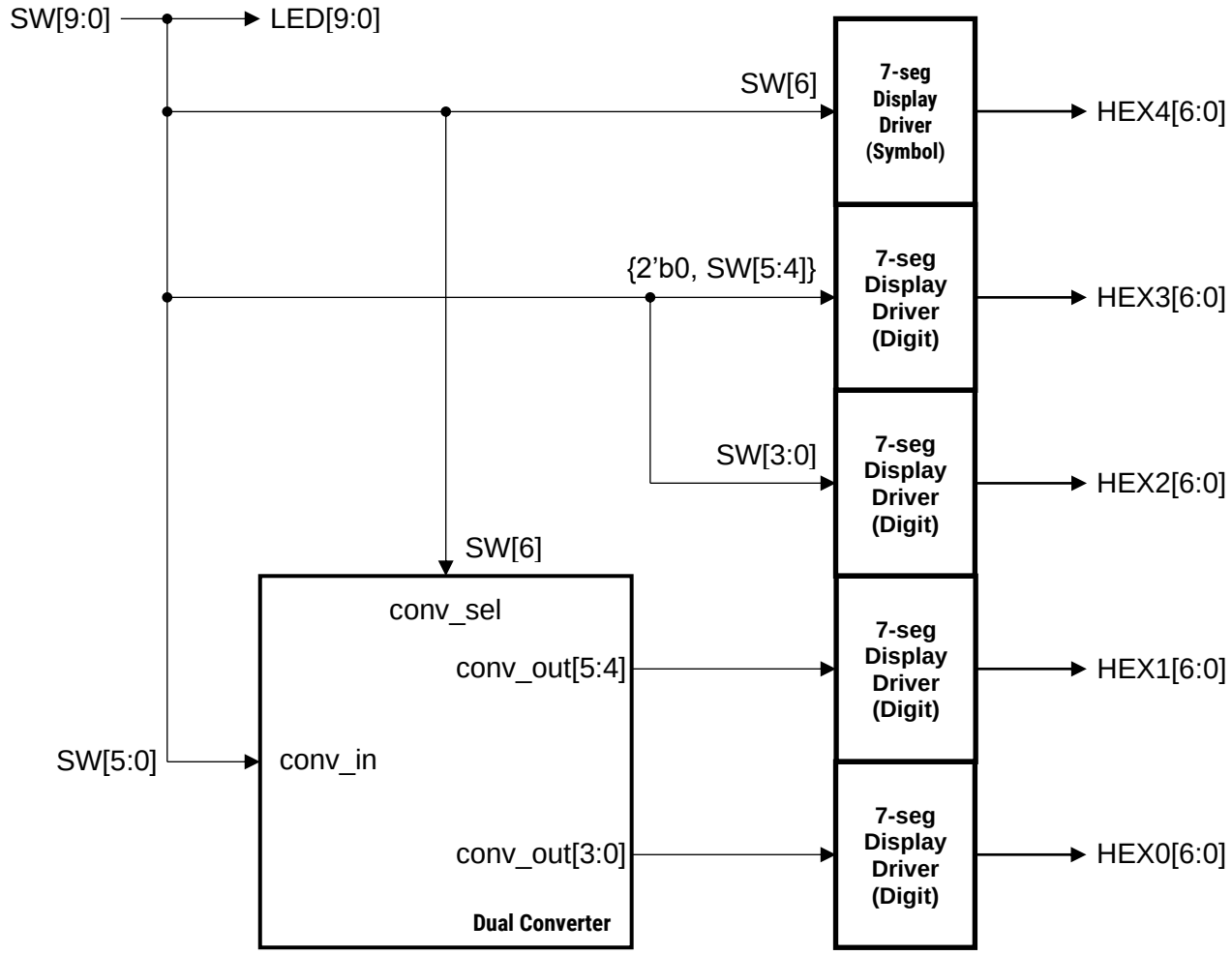
Project Objectives

Project 3A introduced the process of using Quartus to build a logic circuit and flashing it to the DE1-SoC FPGA. From the starting data files, an archived starter Quartus project was unpacked. This project was flashed to the FPGA after setting up pin declarations and other initial settings. With this circuit flashed to the FPGA, its functionality was confirmed using the switches on the board.

The second part of the project called for implementing a binary/BCD conversion circuit (shown below) using previously developed modules. Once this circuit was constructed, a testbench file was written for it and tested through Quartus via ModelSim. The waveform results from these tests appeared to show correct operation of the circuit. Due to the results from the test bench file, the Verilog circuit was flashed to the board to confirm its functionality through extensive real-world testing.



Design Process

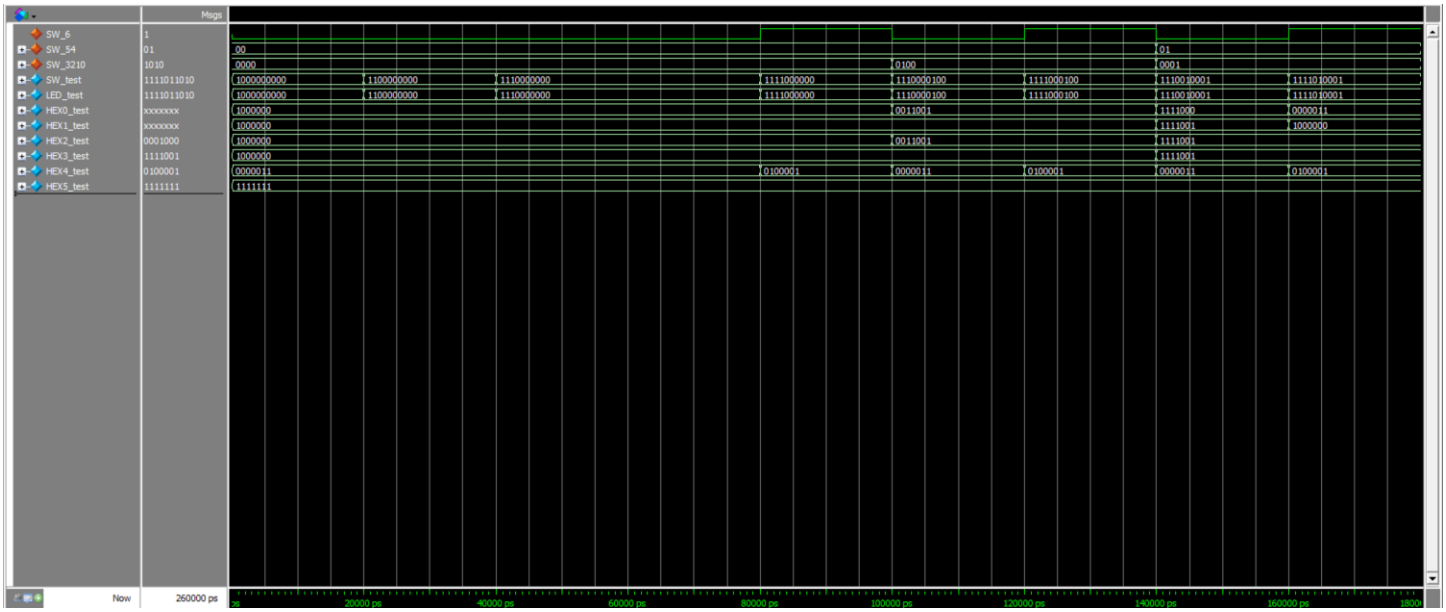
The first module that was created was the symbol 7-segment driver as it was the simplest module to create. It's essentially a 2-to-1 mux. If SW[6] is a 0, output a constant binary value. If SW[6] is a 1, output a different constant value.

After this driver was made, the 7-segment driver module from Homework 3 was instantiated 4 times for HEX3 through HEX0. After testing the circuit on the FPGA, it was discovered that the outputs from this driver module were all incorrect aside for the number 8. These outputs were fixed and then worked properly through the rest of testing.

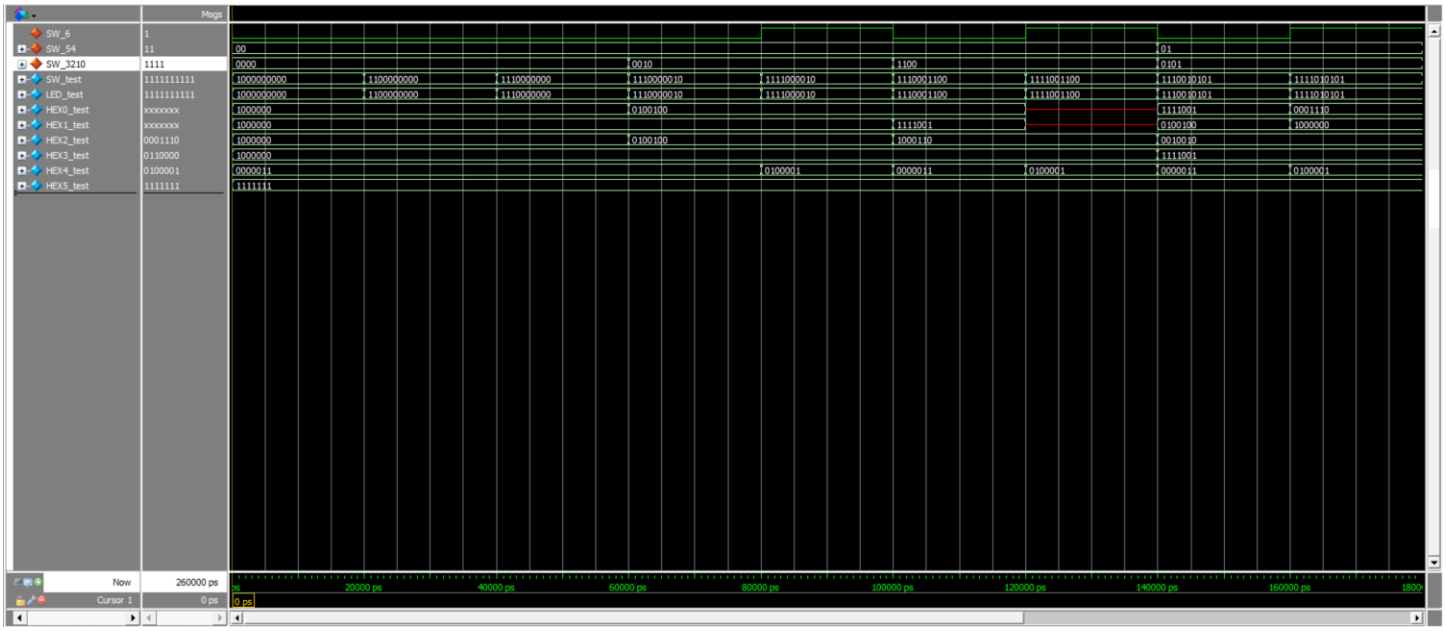
Lastly, the dual converter module was created using a SN184 and SN185 module from Project 2. SW[5:0] is used as the 6-bit input for each decoder. The outputs of each decoder were then put into another procedural 2-to-1 mux using SW[6] as the select bit to choose what is output from the dual converter module.

From here, all the instantiated modules were made and connected. A simple test bench was written to test a few input combinations and simulated in ModelSim through Quartus. The resulting waveform output looked accurate. The circuit was flashed to the FPGA and then was extensively tested on the board (especially the Don't Care results). Every valid input case was tested along with a number of invalid inputs.

Output Waveforms



First Testbench Test Results



Second Testbench Test Results

Conclusion

This was a simple but useful project. It was good practice to get re-acclimated with Quartus after a year and a half or so since ECE 2504. This project also provided some more practice designing larger systems using previously designed modules. Another lesson I learned is to be more careful designing these modules in the first place. The 7-segment display drivers I wrote in HW3 “worked correctly” but the output signals it “output correctly” were wrong (I got the MSB and LSB backwards). It wasn’t until I tested the code on an actual 7-segment display that I discovered this mistake.