Genesys Logic, Inc.

GL827L

USB 2.0 Single Slot SD/MMC/MS Card Reader Controller

Datasheet

Revision 1.03

Oct. 17, 2008

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Revision History

Revision	Date	Description
1.00	2007/11/06	First formal release
1.01	2007/12/14	1. Add QFN24 package, p.9, p. 18 2. Update absolute maximum rating and DC characteristics, p.14
1.02	2008/07/11	1. Remove Ambient Temperature in Table 6.1, p.14 2. Update QFN24 package, p.18, p.19
1.03	2008/10/17	Add QFN24 package (B), p.10,11

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CHAPTER 1 GENERAL DESCRIPTION

The GL827L is USB 2.0 SD/MMC/MS Flash Card Reader single chip. It supports USB 2.0 high-speed transmission to Secure Digital™ (SD), SDHC, Mini SD™, Micro SD™ , T-Flash , MultiMediaCard™ (MMC), RS MultiMediaCard™ (RS MMC), MMC Micro , HS-MMC, MMC-Mobile , Memory Stick™ (MS), Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick PRO™ (MS PRO), Memory Stick PRO™ Duo (MS PRO Duo), Memory Stick PRO-HG (MS PRO-HG), Memory Stick ROM, MS PRO Micro (M2) on one chip. As a single chip solution for USB 2.0 flash card reader, the GL827L complies with Universal Serial Bus specification rev. 2.0, USB Storage Class specification ver.1.0, and each flash card interface specification.

The GL827L integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and flash card interfaces. Its' pin assignment design fits to card sockets to provide easier PCB layout.
The GL827L is packaged with 28-pin SSOP (150mil) and 24-pin QFN for up to 1 LUN (SD/MMC, MS).

CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with 480Mbps Universal Serial Bus specification rev. 2.0.
  - Comply with USB Storage Class specification rev. 1.0.
  - Support 1 device address and up to 4 endpoints: Control (0)/ Bulk Read (1)/ Bulk Write (2)/Interrupt (3).
- Integrated USB building blocks
  - USB2.0 transceiver macro (UTM), Serial Interface Engine (SIE), Build-in power-on reset (POR) and low-voltage detector (LVD)
- Embedded 8051 micro-controller
  - Operate @ 60 MHz clock, 12 clocks per instruction cycle
  - Embedded 32K Byte mask ROM and internal 256 byte SRAM
  - Embedded 2K Byte external SRAM
- Secure Digital™ and MultiMediaCard™
  - Supports SD specification v1.0 / v1.1 / v2.0
  - Supports MMC specification v3.X / v4.0 / v4.1 / v4.2.
  - x1 / x4 / x8 data transmission. (For QFN24 up to x4)
  - Automatic CRC7 generation for command and CRC7 verification for response on CMD
  - Support automatic CRC16 generation and verification on DAT0:7
  - In addition to full packet transaction, optional single byte / bit operation on both CMD and DAT line / lines
  - Process data in block or byte
- Memory Stick™/ Memory Stick PRO™ / Memory Stick PRO Duo™ / Memory Stick PRO-HG/ Memory Stick Micro
  - Comply with Memory Stick specification: MS 1.43, MSPRO 1.02, MSPRO-HG 1.01 with 4-bit data bus
  - Support INS signal
  - Support automatic CRC16 generation and verification
- On board 12 MHz Crystal driver circuit or 12 MHz Clock input.
- On-Chip 5V to 3.3V regulator. No external regulator required.
- On-Chip power MOSFETs for supplying flash media card power.
- Available in 28-pin SSOP (150mil) package.
- Available in 24-pin QFN package.

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinout

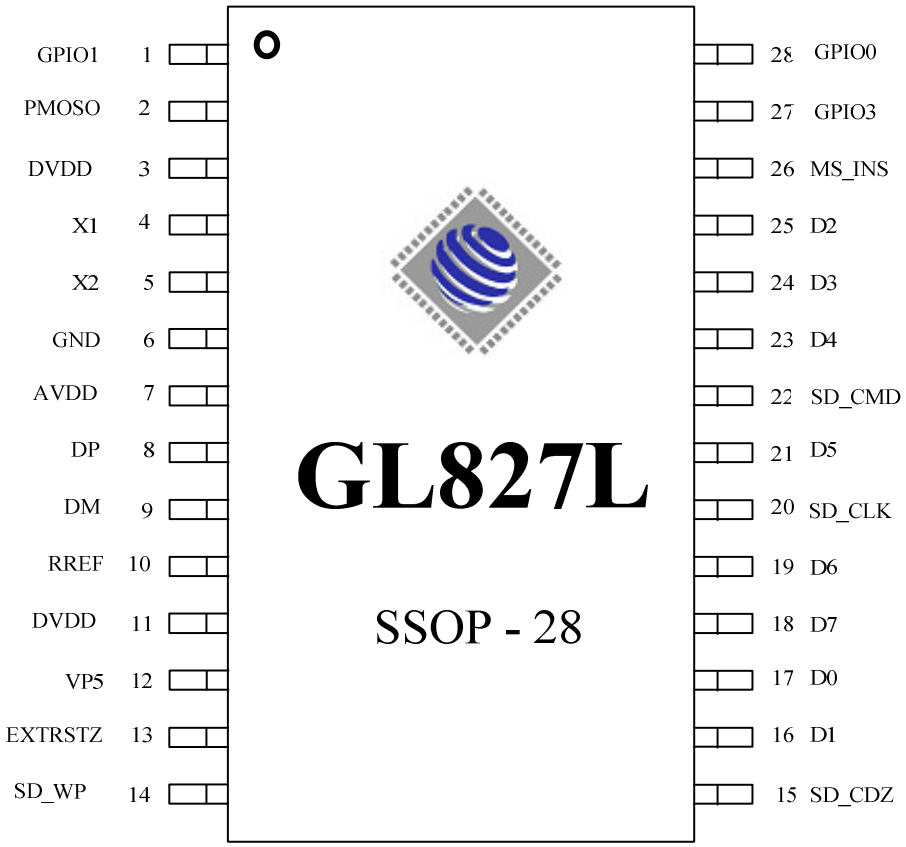


Figure 3.1 – 28 Pin SSOP Pinout Diagram

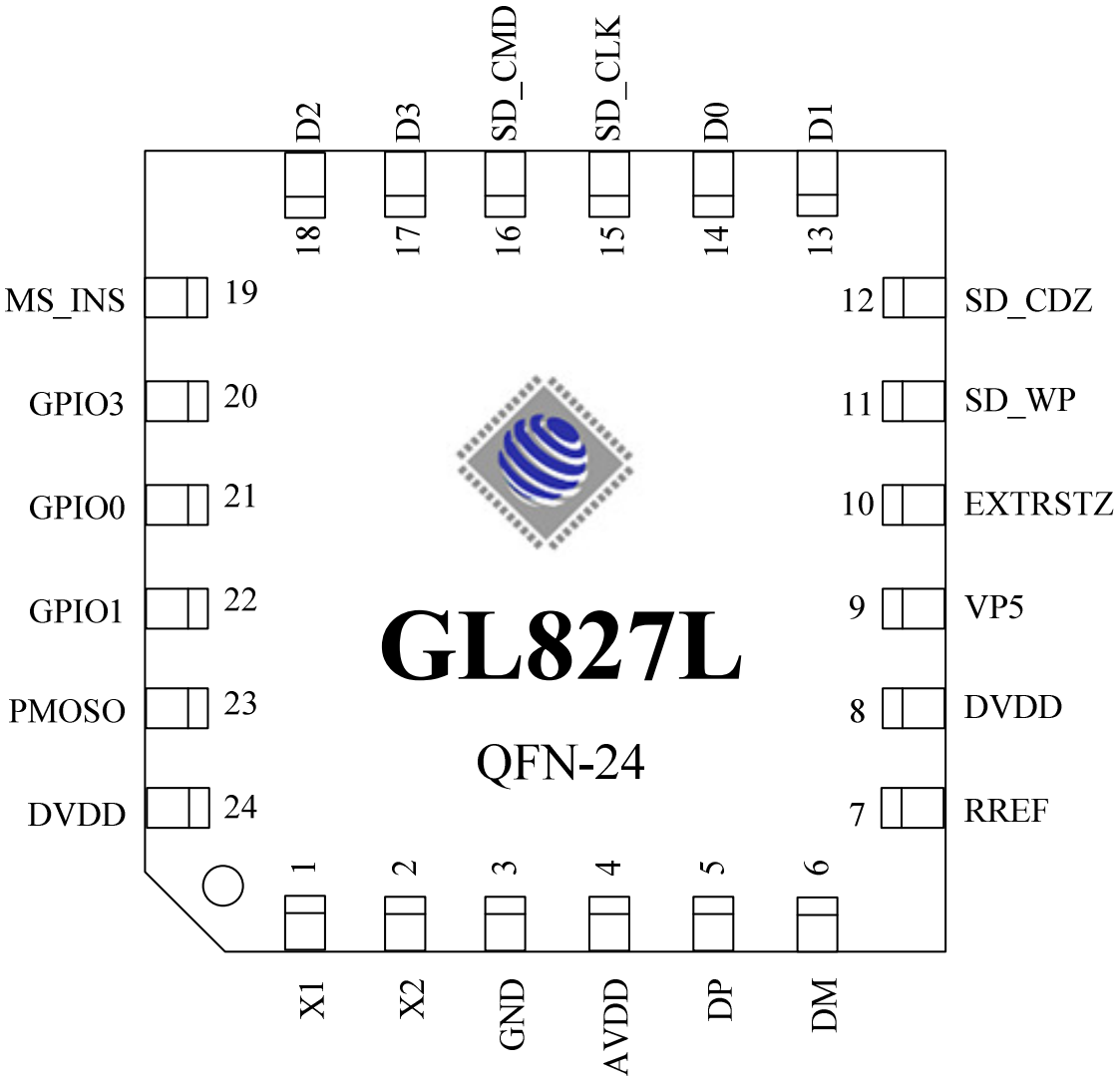


Figure 3.2 – (A) 24 Pin QFN Pinout Diagram

(No EEPROM, with Power and Access LED support)

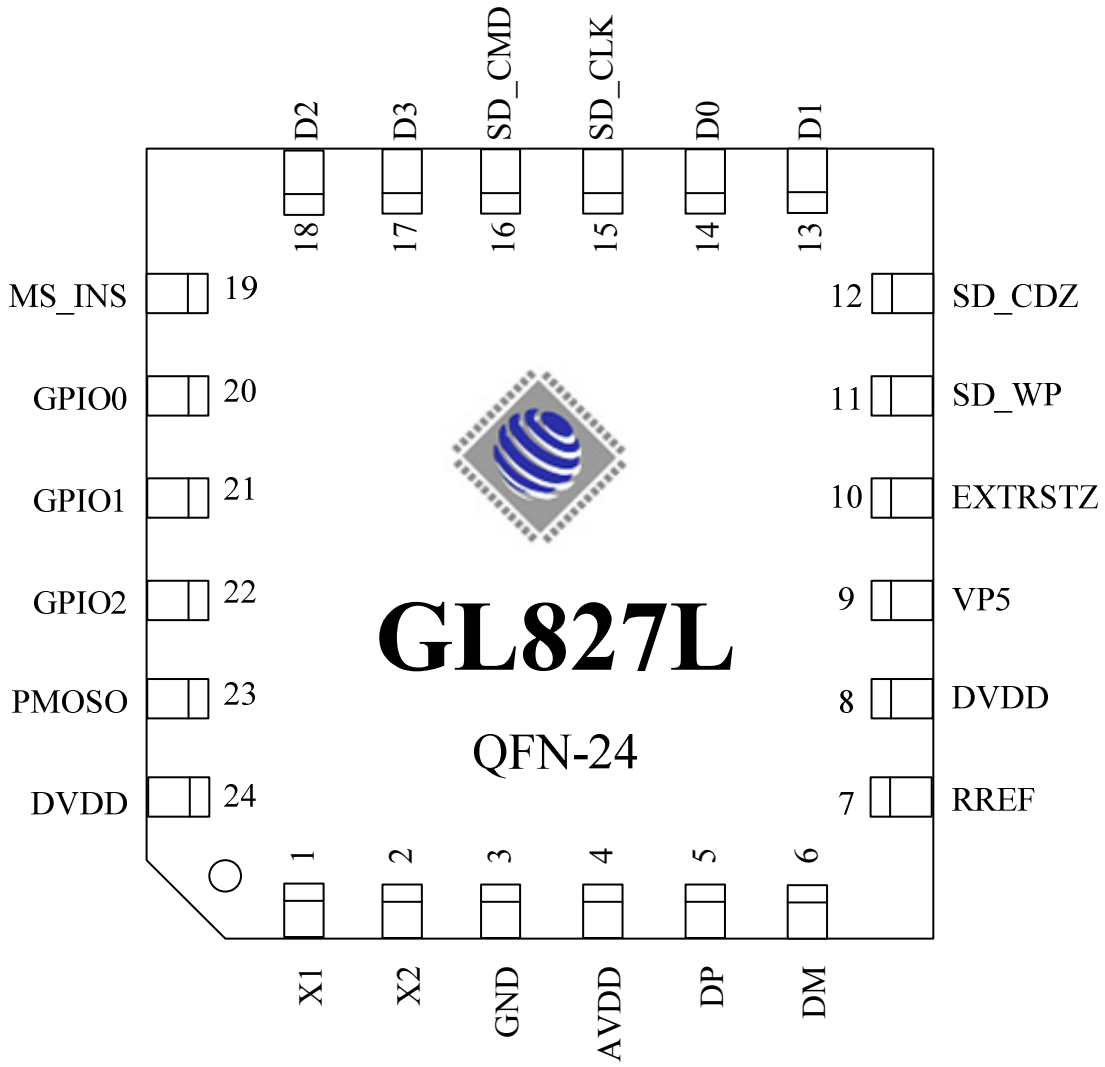


Figure 3.3 – (B) 24 Pin QFN Pinout Diagram

(No Power LED, with EEPROM and Access LED support)

3.2 Pin Descriptions

Table 3.3 - Pin Descriptions

Pin name	SSOP28	QFN 24 (A)	QFN 24 (B)	Type	Description
GND	6	3	3	P	ground
AVDD	7	4	4	P	Analog power 3.3v
DM	9	6	6	A	USB D-
DP	8	5	5	A	USB D+
RREF	10	7	7	A	Reference resistor
X1	4	1	1	I	12MHz XTAL input. It can be connected to external 12MHz clock input.
X2	5	2	2	B	12MHz output.
DVDD	3,,11	24,,8	24,,8	P	Digital power 3.3V
VP5	12	9	9	P	Regulator 5V Input
PMOSO	2	23	23	P	Card power
EXTRSTZ	13	10	10	I, pu	System reset, active low
MS_INS	26	19	19	I, pu	Memory Stick insertion detect 0: card insert 1: no card
SD_CDZ	15	12	12	I, pu	SD Card detect 0: card insert 1: no card
D0~D3	17,16,25, 24	14,13,18, 17	14,13,18, 17	B	MS data 0~3 SD data 0~3 MMC data 0~3
D4~D7	23,21, 19,18	-	-	B	MMC Data4~7 (Only for SSOP28)
SD_CLK /MS_SCLK	20	15	15	O	SD/MMC CLK/ MemoryStick SCLK
SD_WP	14	11	11	I, pd	SD Write Protect 0: write enable 1: write protect
SD_CMD/ MS_BS	22	16	16	I, pd	SD/MMC CMD/ Memory Stick BS
GPIO0	28	21	20	B	Access LED
GPIO1	1	22	21	B	SSOP28/ QFN24(A) GPIO1: NC QFN24(B) GPIO1: I2C_SCL
GPIO3	27	20		B	Power LED
GPIO2			22	B	I2C_SDA

Notation:

Type	**A**	Analog
	B	Bi-directional
	I	Input
	O	Output
	P	Power / Ground
	pd	Internal pull down
	pu	Internal pull up

CHAPTER 4 BLOCK DIAGRAM

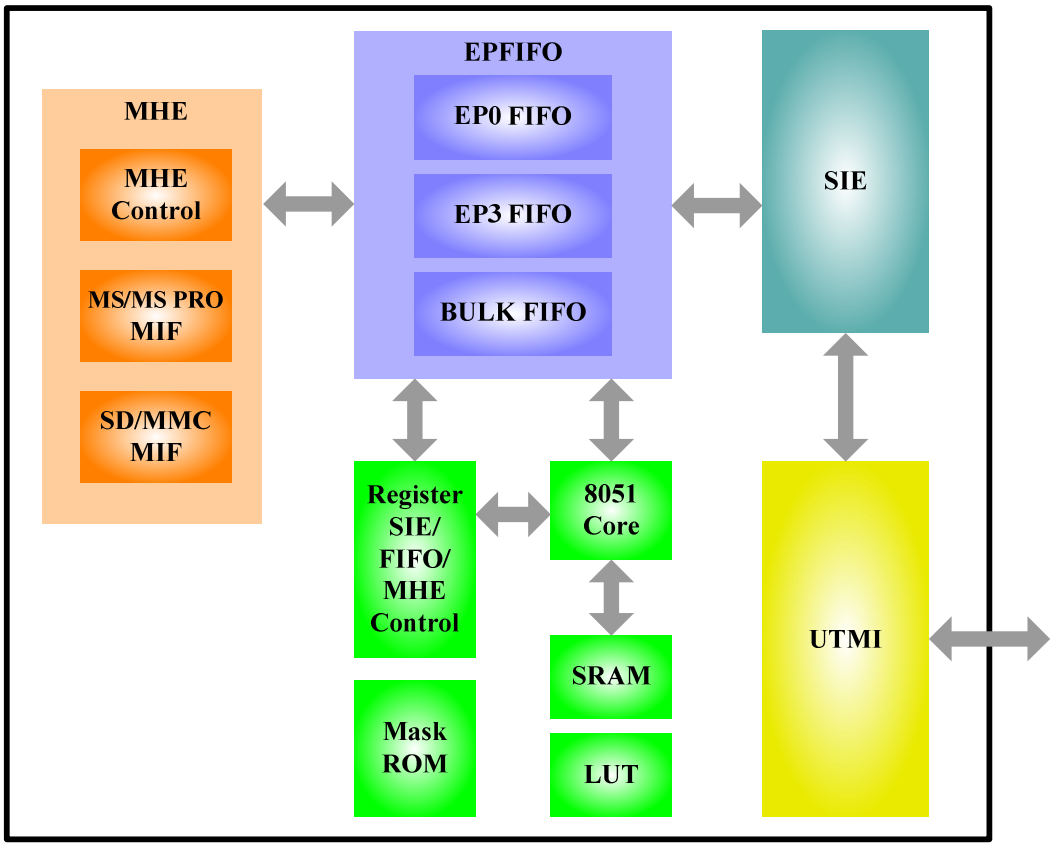


Figure 4.1 - Block Diagram

CHAPTER 5 FUNCTION DESCRIPTION

UTM

The USB 2.0 Transceiver Macrocell is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0), interrupt FIFO (FIFO3), Bulk In/Out FIFO (BULKFIFO)

- **Control FIFO** FIFO of control endpoint 0.
  It is 64-byte FIFO, and it is used for endpoint 0 data transfer.
- **Interrupt FIFO** 64-byte depth FIFO of endpoint 3 for status interrupt
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It contains ping-pong FIFO (512 bytes each bank) for transmit/receive data continuously.
  2. It can be directly accessed by Uc
  3. Automatic hardware SmartMedia ECC error correction support

MHE

It contains 2 MIFs (Media Interface)

- **MIFs**
  1. SD / MMC
  2. MemoryStick/ MemoryStick PRO
- **External reset circuit**
  Non-inverting, Schmitt input with weak pull-up using DVDD power.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 6.1 - Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-65°C to +150 °C
DC Input Voltage to Any Pin	-0.5V to +5.8V

6.2 Operating Conditions

Table 6.2 - Operating Conditions

Parameter	Value
Ta (Ambient Temperature Under Bias)	0°C to 70°C
Supply Voltage	+4.75V to +5.25V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	12 MHz ± 0.05% 12 MHz ± 0.25% (for USB full-speed only)

6.3 DC Characteristics

Table 6.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage		4.75	-	5.25	V
V_{IH}	Input High Voltage		2.0	-	-	V
V_{IL}	Input Low Voltage		-	-	0.8	V
I_I	Input Leakage current	$0 < V_{IN} < 3.3v$	-10	-	10	µA
V_{OH}	Output High Voltage		2.4	-	-	V
V_{OL}	Output Low Voltage		-	-	0.4	V
I_{OH}	Output Current High		-	8	-	mA
I_{OL}	Output Current Low			8	-	mA
C_{IN}	Input Pin Capacitance		-	5	-	pF
I_{SUSP}	Suspend current	1.5K external pull-up included	-	-	450	µA
I_{CC}	Power consumption	Connect to USB with 8051 operating without Card power consumption	-	-	60	mA

6.4 5V to 3.3V Regulator Characteristics

Table 6.4 – Regulator Output Current

Parameters	Description	Test Conditions	Typ..	Units
Iq	Quiescent current	no loading	18	uA
Io_max	Output driving capability	Vo > 2.9V	400	mA
Vo_0mA	Vo voltage without loading		3.38	V

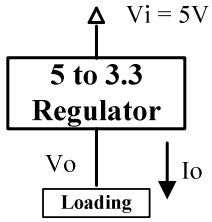


Figure 6.1 - 5V to 3.3V Regulator Architecture

6.5 PMOS Characteristics

Table 6.5 - PMOS I-V table

(IO Power=3.3V, Temperature 25 °C)

Driving Loading (mA)	Vd output voltage(V)
100mA	**3.12**
200mA	**2.94**

Note:
1. Driving strength is defined as the PMOS sinking current when Vio=3.3V

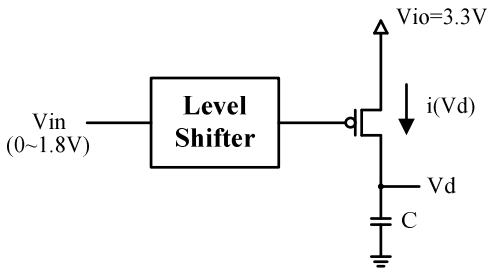


Figure 6.2 - Embedded PMOS Switch Architecture

6.6 AC Characteristics

6.6.1 UTMI Transceiver

The GL827L is fully compatible with Universal Serial Bus specification rev. 2.0 and USB 2.0 Transceiver Macercell Interface (UTMI) specification rev. 1.01. Please refer to the specification for more information.

6.6.2 Reset Timing

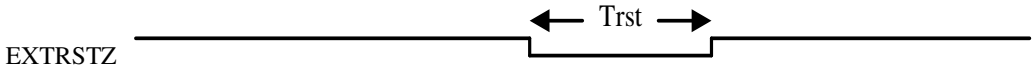


Figure 6.3 - Timing Diagram of Reset width

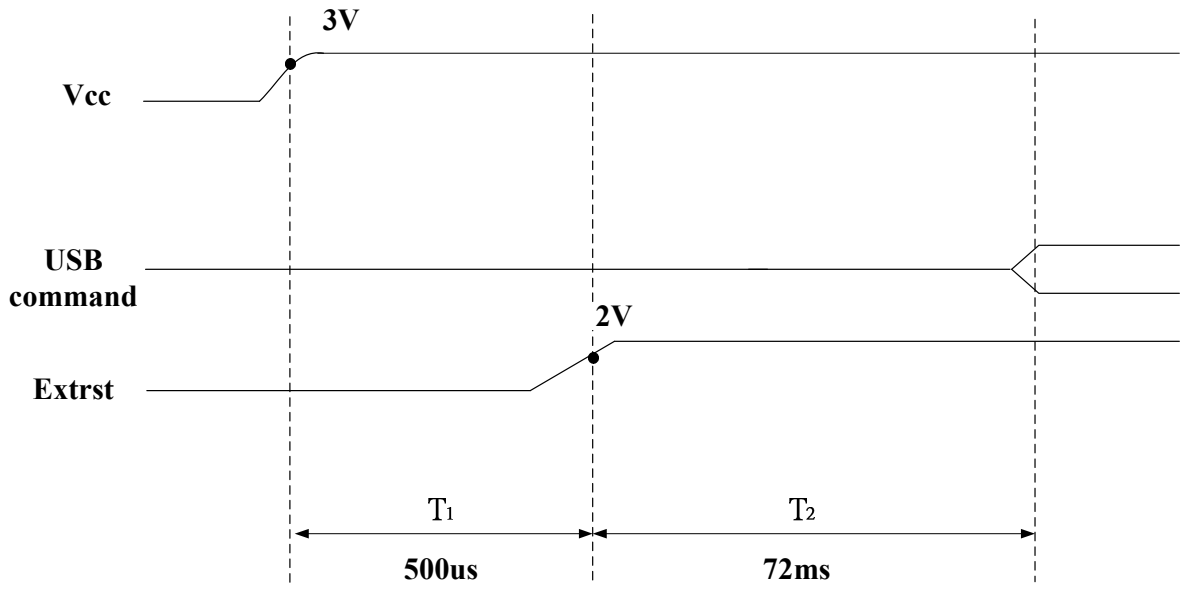
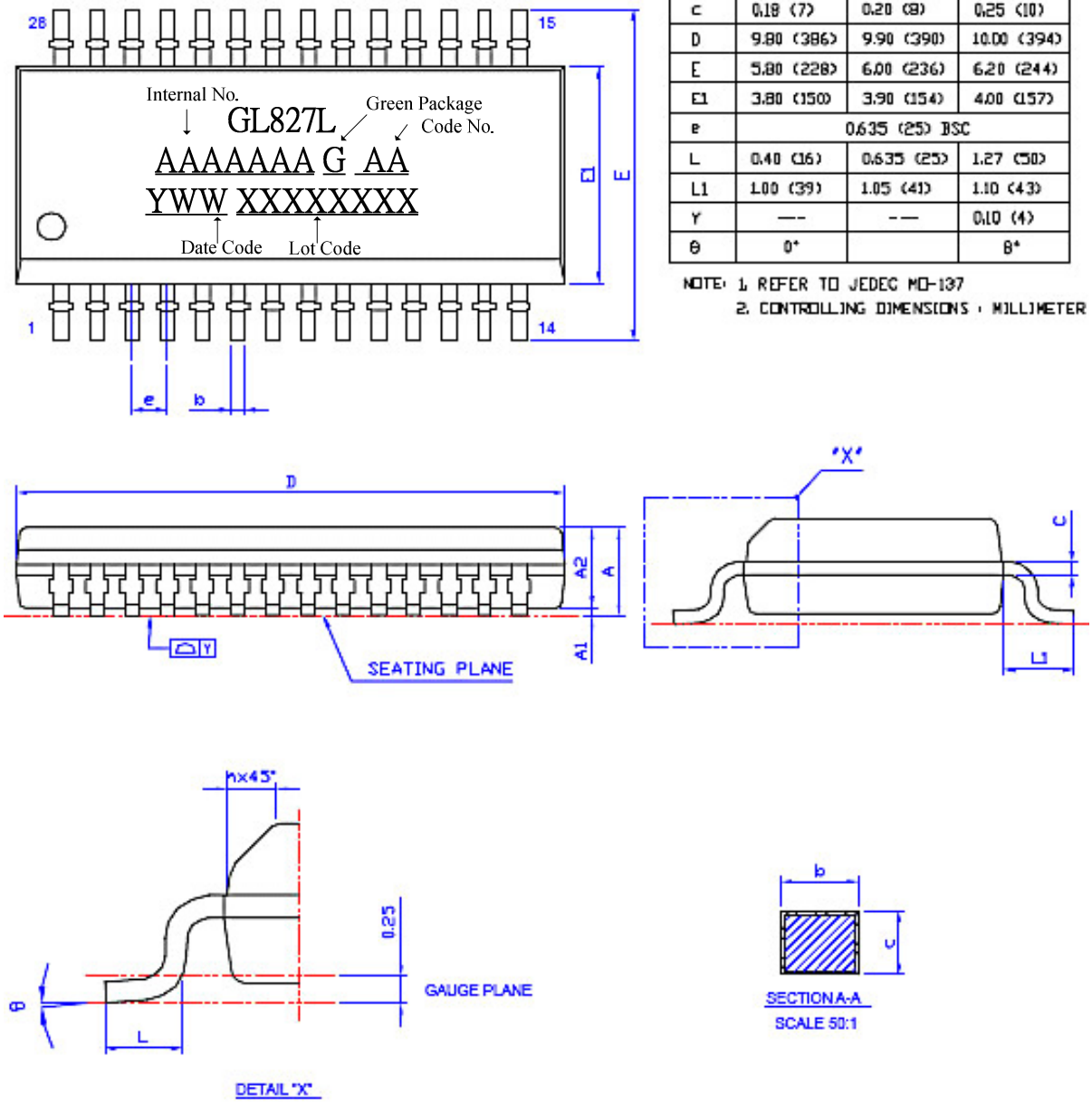


Figure 6.4 - Timing Diagram of Power Good to USB command receive ready

Parameter	Description	Min	Unit
Trst	Chip reset sense timing width	2	us
T1	External reset valid from power up to high	500	us
T2	Reset deassertion to respond USB command ready	72	ms

CHAPTER 7 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	1.35 (53)	1.60 (63)	1.75 (69)
A1	0.10 (4)	0.15 (6)	0.25 (10)
A2	1.25 (49)	1.45 (57)	1.50 (59)
b	0.20 (8)	0.25 (10)	0.30 (12)
c	0.18 (7)	0.20 (8)	0.25 (10)
D	9.80 (386)	9.90 (390)	10.00 (394)
E	5.80 (228)	6.00 (236)	6.20 (244)
E1	3.80 (150)	3.90 (154)	4.00 (157)
e	0.635 (25) BSC		
L	0.40 (16)	0.635 (25)	1.27 (50)
L1	1.00 (39)	1.05 (41)	1.10 (43)
Y	---	---	0.10 (4)
θ	0°		8°

NOTE: 1. REFER TO JEDEC MO-137
2. CONTROLLING DIMENSIONS : MILLIMETER

Figure 7.1 - GL827L 28 Pin SSOP Package

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (28)	0.75 (30)	0.80 (32)
A1	0.00 (0)	0.02 (0.8)	0.05 (2)
A3	0.20 (8) REF		
b	0.18 (7)	0.25 (10)	0.30 (12)
D	3.90 (154)	4.00 (158)	4.10 (161)
E	3.90 (154)	4.00 (158)	4.10 (161)
D2	1.90 (75)	2.00 (79)	2.10 (83)
E2	1.90 (75)	2.00 (79)	2.10 (83)
e	0.50 (20) BSC		
L	0.30 (12)	0.40 (16)	0.50 (20)
y	0.08 (3)		

NOTE: 1. REFER TO JEDEC MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

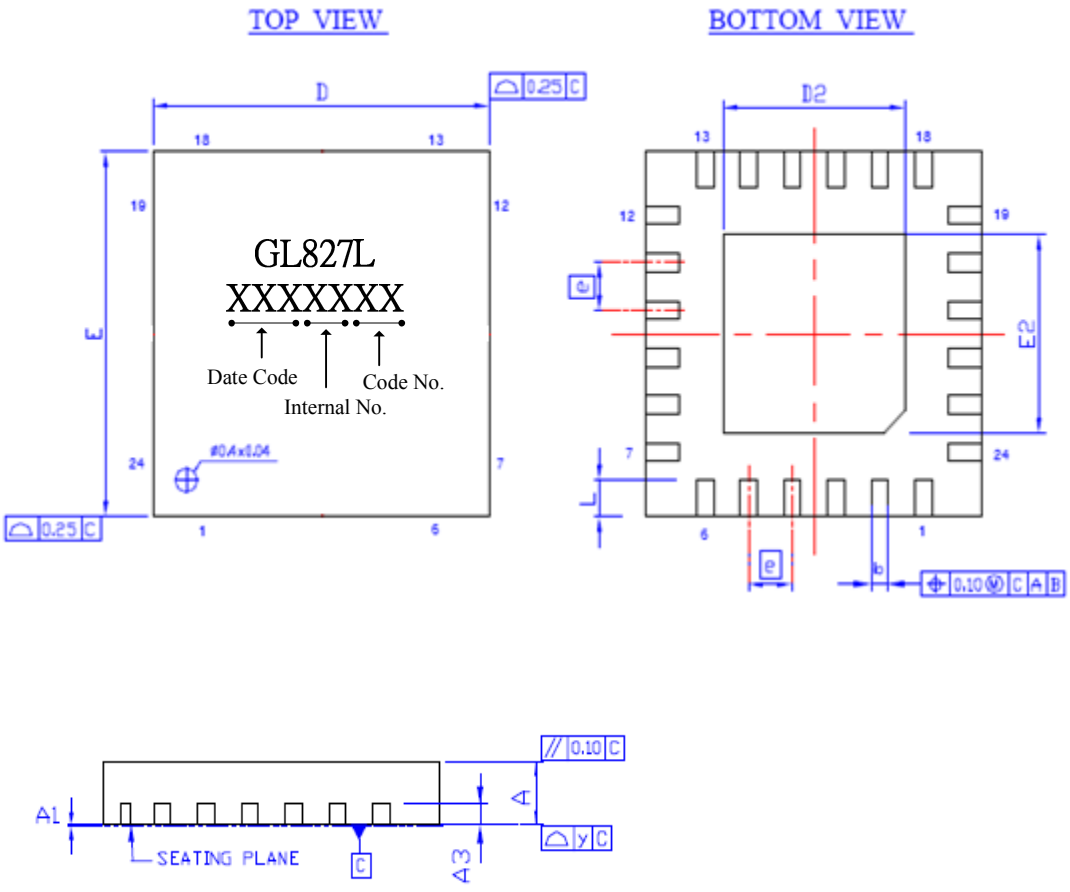


Figure 7.2 - GL827L 24 Pin QFN Package (For 827L-01 and 827L-02 version only)

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (28)	0.75 (30)	0.80 (32)
A1	0.00 (0)	0.02 (0.8)	0.05 (2)
A3	0.20 (8) REF		
b	0.18 (7)	0.25 (10)	0.30 (12)
D	3.90 (154)	4.00 (158)	4.10 (161)
E	3.90 (154)	4.00 (158)	4.10 (161)
D2	1.90 (75)	2.00 (79)	2.10 (83)
E2	1.90 (75)	2.00 (79)	2.10 (83)
e	0.50 (20) BSC		
L	0.30 (12)	0.40 (16)	0.50 (20)
y	0.08 (3)		

NOTE: 1. REFER TO JEDEC MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

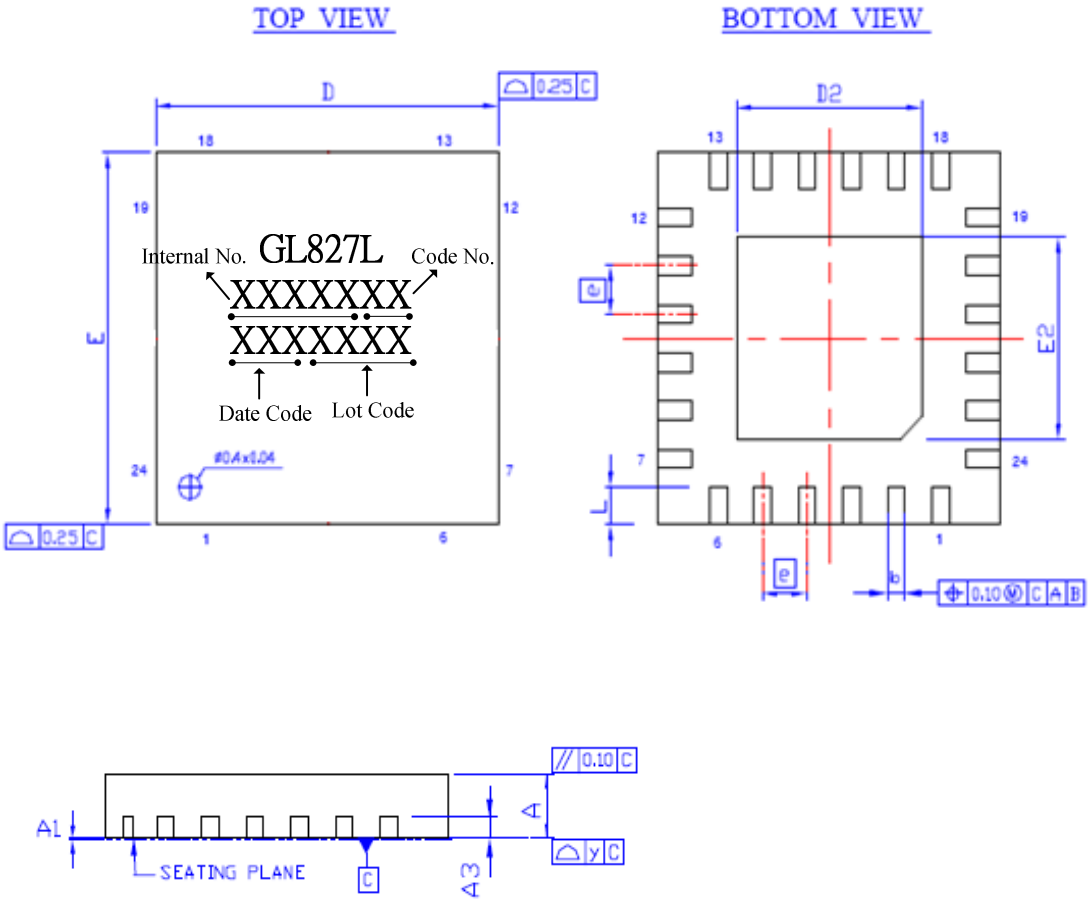


Figure 7.3 - GL827L 24 Pin QFN Package (For 827L-03 and later version)

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Normal/Green	Version	Status
GL827L -HHG	28-pin SSOP	Green Package	XX	Available
GL827L -OGG	24-pin QFN	Green Package	XX	Available