线上学习线上测试1

本次测试为线上学习部分中的线上测试。

1. The L1 cache on a high-end processor is most likely to use which technology?

单选题(5 分)

A. magnetic disk

B. DRAM

C. SRAM

D. Flash

2. What is an advantage of increasing the number of pipelines?

单选题(5 分)

A. Less complex circuit

B. Faster computation on a whole instruction

C. Increased clock period

D. Faster clock speed

3. Suppose we have made the following measurements ,
Frequency of Instruction A= 25%
Average CPI (clock cycles per instruction) of Instruction A= 4.0
Average CPI of other instructions = 1.2
Frequency of Instruction B= 2%
Average CPI of Instruction B= 20
If we decrease the CPI of Instruction B to 7, calculate the total CPI

单选题(5 分)

A. 1.64

B. 1.54

C. 1.36

D. 2.31

4. The execution of the following two instructions may have the (_____) hazard.
lw R3,0(R2)
lw R2,0(R1)

单选题(5 分)

A. RAW (Read after Write)

B. WAW (Write after Write)

C. WAR (Write after Read)

D. No hazards

5. What is the decimal of the binary real number 101.1×2^{-2} ?

单选题(5 分)

A. 1.5

B. 5.5

C. 1.375

D. 2.75

6. Increasing associativity can reduce_____

单选题(5 分)

A. Compulsory misses (cold-start misses)

B. Capacity misses

C. Conflict misses (collision misses)

D. All three misses

7. What is the content of stack pointer (SP)?

单选题(5 分)

A. address of the current instruction

B. address of the next instruction

C. size of the stack

D. address of the top element of the stack

8. What is the RISC-V assembly code for the binary?
0010010 00110 00111 010 11000 0100011

单选题(5 分)

A. sw t1, 1200(t2)

B. sw t1, 600(t2)

C. sw t2, 1200(t1)

D. sw t2, 600(t1)

9. Which type of parallel computing architecture is no longer commonly encountered in machines today?

单选题(5 分)

A. MIMD (Multiple Instruction/Multiple Data Stream)

B. MISD (Multiple Instruction/Single Data Stream)

C. SIMD (Single Instruction/Single Data Stream)

D. SISD (Single Instruction/Multiple Data Stream)

10. If we want to construct a PTE (Page Table Entry) where there are flags for Writable, Valid, and Dirty. And we have a total of 1 TB space in Main Memory. Each page also has the size of 8 KB, what is the minimum number of bits we need to fill up the PTE?

单选题(5 分)

A. 28 bits

B. 30 bits

C. 32 bits

D. 33 bits

11. The control component of the processor performs arithmetic operations.

判断题(5 分)

A. True

B. False

12. Bigger cache blocks always lead to a higher hit rate.

判断题(5 分)

A. True

B. False

13. Von Neumann architecture has data and instructions in the same memory space.

判断题(5 分)

A. True

B. False

14. The direct memory access (DMA) is worse for large transfers than interrupts due to the overhead of setting up the transfer.

判断题(5 分)

A. True

B. False

15. In virtual memory, the number of entries of a page table is equals to the physical page number.

判断题(5 分)

A. True

B. False

16. For L2 cache, reducing hit time is as important as reducing miss rate.

判断题(5 分)

A. True

B. False

17. For the following question, assume the following:

- 28-bit virtual addresses
- 16MiB Physical Memory with LRU replacement
- 4KiB Pages
- Fully associative TLB with 16 entries and an LRU replacement policy

综合题(20 分)

(1) What is the number of bits of VPN and PO (Virtual Page Number : Page Offset) for VM (Virtual Memory)?

VPN: ① , PO: ②

填空题(10 分)　(请按题目中的空缺顺序依次填写答案)

① 16

② 12

(2) What is the number of bits of PPN and PO (Physical Page Number : Page Offset) for Physical memory?

PPN: ① , PO: ②

填空题(10 分)　(请按题目中的空缺顺序依次填写答案)

① 12

② 12