总复习

2023年12月29日 11:03

导论

Moore's law: The observation that the number of transistors in a dense IC doubles approximately every two years

Characteristics of AIC:

- operational amplifiers, voltage and current circuits
- OPAMP determines the whole performance of IC(core circuits)

Challenge in AIC:

- sensitive to noise, crosstalk and other interferes
- heavy second order effects

Challenge in DIC:

- multiple levels of abstractions
- multiple and conflicting constraints: low cost and high performance
- short design time

ISSCC: IEEE international Solid-State Circuits Conference

工艺流程

operations:

- Wafer: 产生合适类型的衬底
- Photolithography（光刻）: 精确地划分各个区
- Oxidation, deposition, ion implantation（氧化、沉积、离子注入）: 给晶圆添加材料
- Etching（蚀刻）: 去除材料

CMOS Fabrication Steps

N-well Silicon-gate CMOS

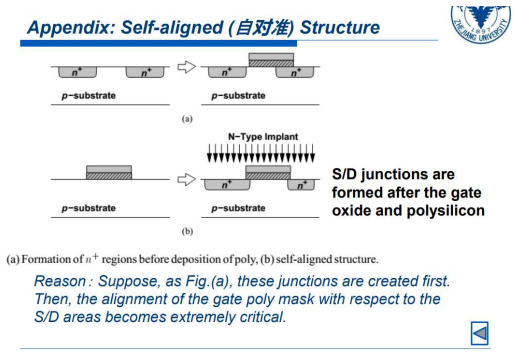
- P衬底上形成N-well
- 确定有源区(active)、场区(field)，场区隔离(isolation)
- 制备MOS管：阈值电压调节，自对准结构、LDD

- 元件互连
- 钝化

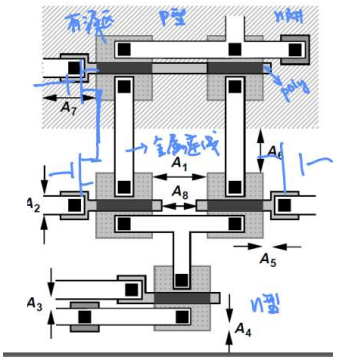
Self-aligned:

PMOS: n-well -> gate oxide and polysilicon -> source/drain junctions

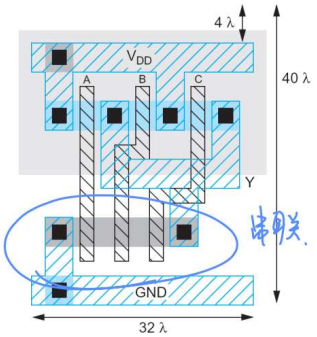
- Make S/D regions implanted at precisely the edges of gate area



layout of a PMOS电流源负载差分对



layout的串并联



器件模型

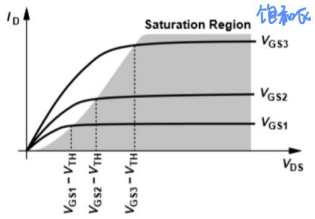
Diode

$I_D = I_S(exp(V_D/\phi_T) - 1)$

耗尽层电容：$C_j = \frac{C_{j0}}{(1-V_D/\phi_0)^m}$

Breakdown:$BV \approx \frac{\epsilon_{Si}(N_A+N_D)}{2qN_AN_D} E_{max}^2$ $E_{max} = 3 \times 10^5\ V/cm$

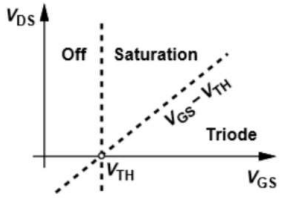
MOS



深线性区：作电阻，$R_{on} = \frac{1}{\mu_n C_{OX} W/L(V_{GS}-V_{TH})}$

饱和区：作电流源，$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$

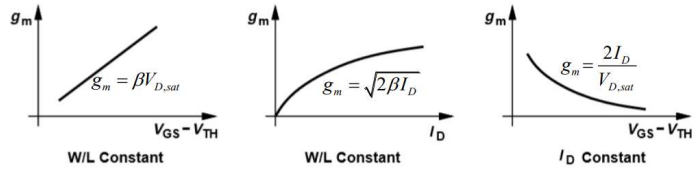
PMOS的电流驱动能力更差，$\mu_p < \mu_n$



- V_{GS}<V_{TH}: off region
- V_{DS} = V_{GS}−V_{TH} = $V_{D,sat}$: saturation and triode region
- For a given V_{DS}, V_{GS} increases: off, saturation, triode

跨导

$g_m = \frac{\partial I_D}{\partial V_{GS}}|_{V_DS=const} = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH}) = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GS}-V_{TH}} = \frac{1}{R_{on}}$



Body effect

$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|})$

参量γ与衬底浓度有关，$N \uparrow \Rightarrow \gamma \uparrow$

$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\Phi_F+V_{SB}}} = \eta g_m$

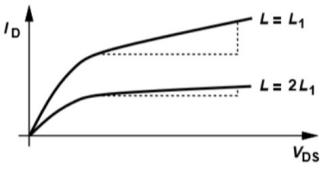
沟道调制效应

记得跨导也要 $\times(1+\lambda V_{DS})$

$r_{ds} = \frac{1}{I_{DS}\lambda}$

$L \uparrow \Rightarrow \lambda \uparrow$

Early Voltage: $V_E L = \frac{I_{ds}}{g_{ds}} = \frac{1}{\lambda}$



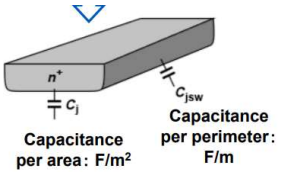
Slope is 1/4!

弱反型

当$V_{GS} < VTH$，MOSFET不会马上关断，$I_D = I_0 exp(\frac{V_GS}{\zeta V_T})$，$g_m = \frac{I_D}{\xi kT/q}$

高频电容

耗尽层（源/漏与体）：$C_j \times Area + C_{jsw} \times Perimeter$



栅-沟道电容：$C_1 = W_{eff} L_{eff} C_{ox}$

栅-源/漏交叠电容：$C_3/C_4 = CGXO \cdot W_{eff} = C_{ov} W$（$C_{ov} = LC_{ox}$）

按区域：

- 关断区：$C_{GS} = C_3$，$C_{GD} = C_4$，$C_{GB} = C_1 // C_2$
- 三极管区：$C_{GS} = C_3 + 1/2\, C_1$，$C_{GD} = C_4 + 1/2\, C_1$，C_{GB}不考虑
- 饱和区：$C_{GS} = C_3 + 2/3\, C_1$，$C_{GD} = C_4$，C_{GB}不考虑

PMOS vs. NMOS

在CMOS工艺中，PMOS劣(inferior)于NMOS：

- Lower mobility of holes
- Lower output resistance

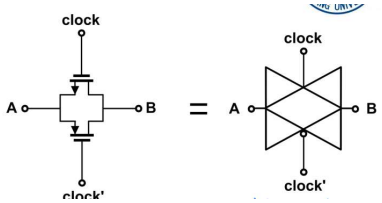
模拟基本单元

Switch

dummy管：

- 减少clock feedthrough
- 减轻沟道充电效应

CMOS Switch：

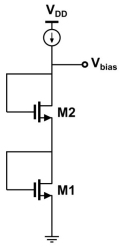


- feedthrough被抵消了
- 更大的动态范围
- 更小的r_{ON}
- 要求互补时钟
- 更大面积

二极管

$r_o = \frac{1}{g_m+g_{mb}+g_{ds}}$

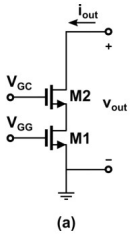
当I_D固定（接恒流源时），令$V_{ON} = \sqrt{2\,I_D/\beta}$，则$V_{DS} = V_{GS} = V_{ON} + V_{TH}$



$V_{bias} = 2V_{ON} + 2V_{TH}$

电流源

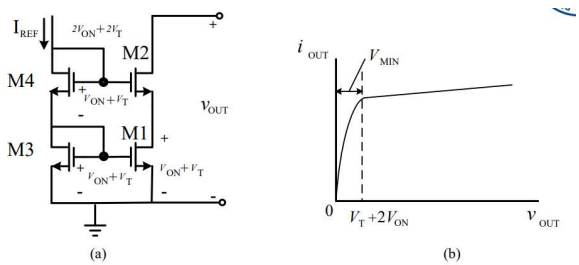
Cascode电流源：看rout时，M1管子相当于一个漏源电阻，$r_0 = (g_{m2} + g_{mb2})r_{ds2}r_{ds1}$



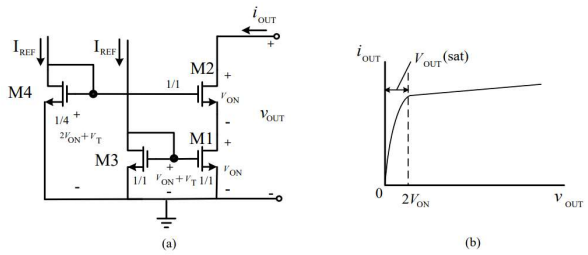
多级Cascode：把最底下的当作电阻，上面有多少级就×多少个$g_m r_o$

在电流源当中V_{ON}作为一种设计参数，已知。

1.

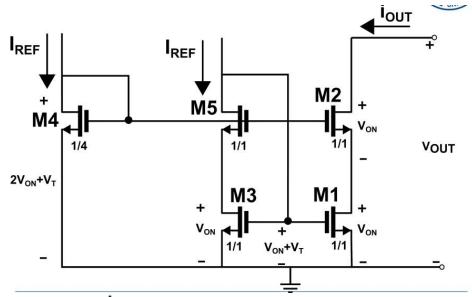


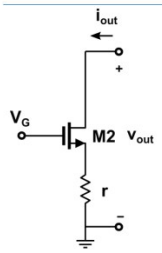
2. 上图M4和M2的源端对称，因此M1工作电压在$V_{ON} + V_T$，降低M1管的V_{DS}：



注意：M4的宽长比是1/4，因为$V_{ON4} = 2V_{ON}$

3.



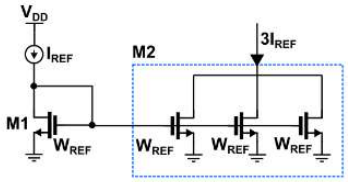


$$I_3 = \frac{1}{2}K'\frac{W}{L}(V_{GS3} - V_{TH})^2 = \frac{1}{2}K'\frac{W}{L}(V_{G3} - V_{S3} - V_{TH})^2$$
$$= \frac{1}{2}K'\frac{W}{L}(V_{TH} + 2V_{ON} - V_{S3} - V_{TH})^2$$
$$= \frac{1}{2}K'\frac{W}{L}(2V_{ON} - V_{S3})^2$$
$$= I_1 = \frac{1}{2}K'\frac{W}{L}V_{ON}^2$$

$\Rightarrow V_{S3} = V_{ON}$

电流镜与基准

倍增电流镜



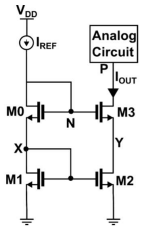
- ”Dummy“管
- Unit管

Mismatch问题

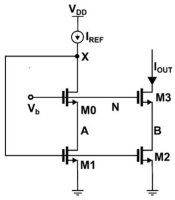
- 沟道效应调制：V_{DS2}取决于负载电路-----增大L、Cascode电流镜
- M1、M2失配
- 版图影响

Cascode电流镜

1. 见ch. 电流源（工作电压太高，但是M3的Vb不用自己设计）

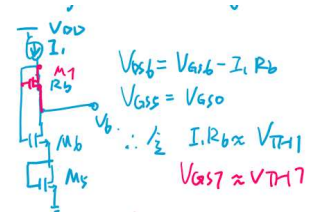


2. Low-voltage Cascode

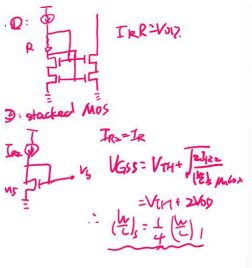


$V_b \geq V_{OD1} + V_{OD0} + V_{TH0}$

Generation of vb:



3. 现行Cascode电流镜

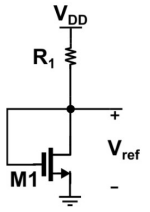


Voltage biasing

Temperature variation：$TC(V_{ref}) = \frac{1}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial T}$

Supply Rejection：$S_{V_{DD}}^{V_{ref}} = \frac{V_{DD}}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial V_{DD}}$

电阻-MOS 分压器



$$I_D=\frac{VDD-V_{ref}}{R}=\frac{\beta_1}{2}(V_{ref}-V_{THN})^2$$

$$V_{ref}=V_{THN}+\sqrt{\frac{2I_D}{\beta_1}}=V_{THN}+\sqrt{\frac{2(VDD-V_{ref})}{R\cdot\beta_1}}$$

or $$V_{ref}=V_{THN}-\frac{1}{\beta_1 R}+\sqrt{\frac{2(VDD-V_{THN})}{\beta_1 R}+\frac{1}{\beta_1^2 R^2}}$$

MOS-only 分压器

$I_{D1}=I_{D2}$,

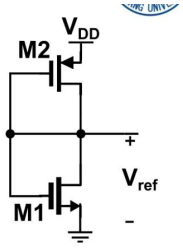
$$\frac{\beta_1}{2}(V_{ref}-VSS-V_{THN})^2=\frac{\beta_2}{2}(VDD-V_{ref}-V_{THP})^2$$

the reference voltage:

$$V_{ref}=\frac{VDD-V_{THP}+\sqrt{\beta_1/\beta_2}(VSS+V_{THN})}{\sqrt{\beta_1/\beta_2}+1}$$

or knowing the reference voltage and the power supply voltages gives

$$\frac{\beta_1}{\beta_2}=\left[\frac{VDD-V_{ref}-V_{THP}}{V_{ref}-VSS-V_{THN}}\right]^2$$

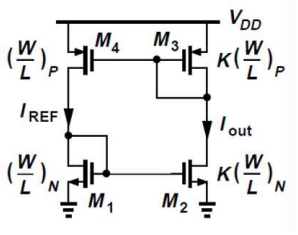


$$S_{V_{DD}}^{V_{ref}}=\frac{V_{DD}}{V_{DD}-V_{THP}+\sqrt{\beta_1/\beta_2}(V_{SS}+V_{THN})}$$

$$TC(V_{ref})=\frac{1}{V_{ref}}\cdot\frac{1}{\sqrt{\beta_1/\beta_2}+1}\cdot\left[-\frac{\partial V_{THP}}{\partial T}+\sqrt{\beta_1/\beta_2}\frac{\partial V_{THN}}{\partial T}\right]$$

Bias Current Generation

Self-biasing



$$I_{out}=KI_{REF}$$

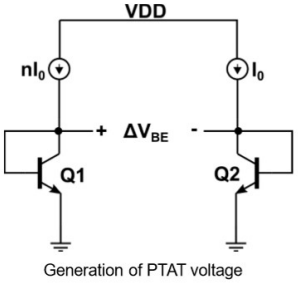
Temperature Independent Reference

Negative-TC Voltage

bjt

Positive-TC Voltage

差分对



Generation of PTAT voltage

$$\Delta V_{BE}=V_{BE1}-V_{BE2}$$
$$=V_t\ln\frac{nI_0}{I_{S1}}-V_t\ln\frac{I_0}{I_{S2}}$$
$$=V_t\ln n$$

$$\frac{\partial\Delta V_{BE}}{\partial T}=\frac{k}{q}\ln n$$

是PTAT常用电路。

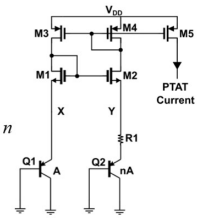
$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_t \ln\left(\frac{I_1}{I_{S1}}\right) - V_t \ln\left(\frac{I_2}{I_{S2}}\right)$$

$$\frac{A_{E2}}{A_{E1}} = n \qquad \frac{I_{S2}}{I_{S1}} = n$$

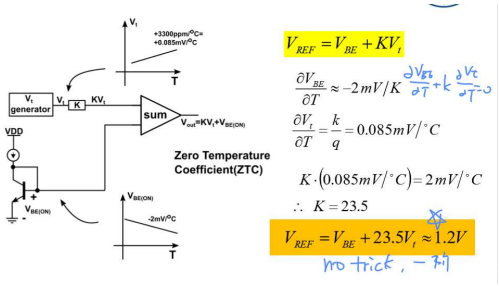
$$V_R = \Delta V_{BE} = V_t \ln\left(\frac{I_1}{I_{S1}} \cdot \frac{I_{S2}}{I_2}\right)$$

$$= V_t \ln\left(\frac{I_{S2}}{I_{S1}}\right) = V_t \ln\left(\frac{A_{E2}}{A_{E1}}\right) = V_t \ln n$$

$$I_O = I_2 = \frac{\Delta V_{BE}}{R} = \frac{V_t}{R} \ln n$$



带隙基准（BGR）



$$V_{REF} = V_{BE} + KV_t$$

$$\frac{\partial V_{BE}}{\partial T} \approx -2mV/K \quad \frac{\partial V_{BE}}{\partial T} + k \frac{\partial V_t}{\partial T} = 0$$

$$\frac{\partial V_t}{\partial T} = \frac{k}{q} = 0.085mV/°C$$

$$K \cdot (0.085mV/°C) = 2mV/°C$$

$$\therefore \ K = 23.5$$

$$V_{REF} = V_{BE} + 23.5V_t \approx 1.2V$$

no trick, - 7:1

单级运放

放大器$R_{in} \to \infty, \quad R_{out} \to 0$

Common-Source

电阻负载

$A_v = -g_m R_D = -\mu_n C_{ox} W/L \, (V_{in} - V_{TH}) R_D \, (// \, r_o)$

$R_{out} = (r_o // R_D)$; $R_{in} = \infty$

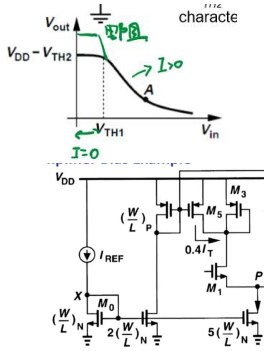
Intrinsic Gain: $R_D \to \infty, A_v = -g_m r_o$

二极管负载

二极管的等效电阻$R_D = \frac{1}{g_m} // \frac{1}{g_{mb}} // r_o$

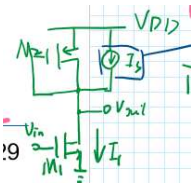
其他的就跟电阻负载一样分析就好。

Output Swing：二极管负载会牺牲一部分电压，swing减小。



注意，N管有体效应，P管一般没有。

Enhancement：电流源Is可以用PMOS实现。

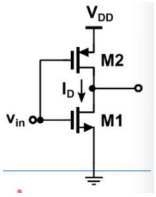


电流源负载

电流源的等效电阻是r_o，栅接交流地。

如果是理想电流源，$A_v = -g_m r_o = -\sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}\cdot\frac{1}{\lambda I_D} \propto \frac{1}{\sqrt{I_D}}$，小电流大增益（代价是低速高noise）

Push-Pull 反相器



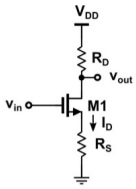
$A_v = -(g_{m1} + g_{m2})(r_{o1} // r_{o2})$

Source Degeneration

接一个源级负反馈电阻R_S，$G_m = -\frac{g_m}{1+g_m R_S}$

$R_{out} = r_o + R_S + (g_m + g_{mb})R_S r_o \approx (g_m + g_{mb})R_S r_o$

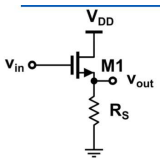
相当于本征增益乘Rs（阻抗倍增小效应）（Cascode）



Source-Follower

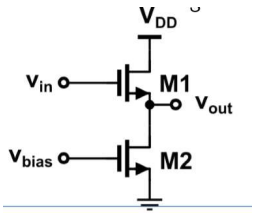
高输入阻抗、低输出阻抗，增益小于等于1

用于降低CS的高输出阻抗。



$A_v = \frac{g_m R_S}{1+(g_m+g_{mb})R_S}$

电流源负载



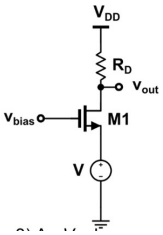
只能用N管。

$A_v = \frac{g_m}{g_m+g_{mb}}$

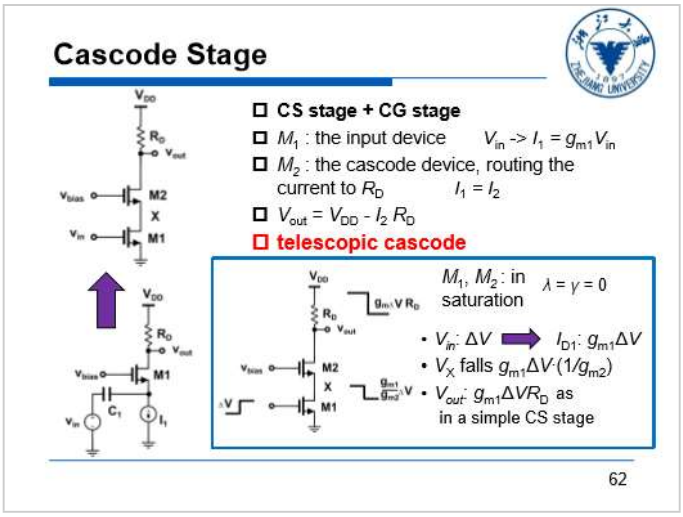
$R_{out} = \frac{1}{g_m+g_{mb}}$，联想电流源负载的CS。

Common-Gate

低输入阻抗，高输出阻抗



Cascode Stage



如果是M2输入，相当于接无穷大的源级负反馈，Vout=0。

差分放大器

差分的好处

- 提高swing
- 减少信号间耦合

- 减少coupled noise
- Rejection of supply noise
- 容易偏置
- 更高的线性度
- 更大的面积

输入范围

ICMR：$V_{GS1}+(V_{GS3}-V_{TH3})\le V_{in,CM}\le min[V_{DD}-R_D\frac{I_{SS}}{2}+V_{TH3},V_{DD}]$

Lower limit: M3 saturation region; Upper limit: M1\M2 triode region

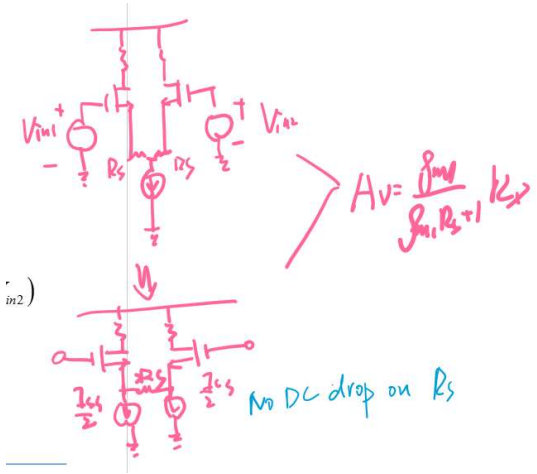
Output swing

$[max(V_{in,CM}-V_{TH},V_{DD}-I_{SS}R_D),\ V_{DD}]$

Half-Circuit

$V_X-V_Y=-g_m(R_D//r_o)(V_{in1}-V_{in2})$，无所谓是否完全差分

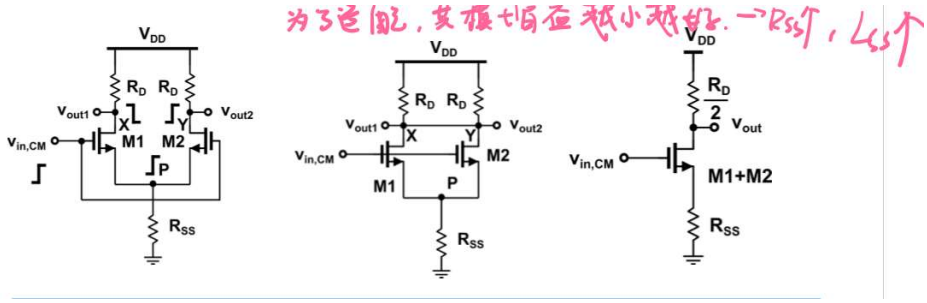
两种改进：



共模响应

差分对并不是完全对称、微电流具有有限的输出阻抗。

1. *Output Impedance* R_{SS}



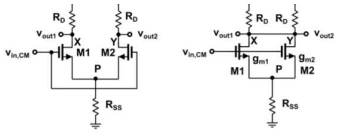
$A_{v,CM}=-\frac{R_D/2}{R_{SS}+1/(2g_m)}$，并联的管子$G_m=2g_m$

2. $g_{m1}\neq g_{m2}$

$$(g_{m1}+g_{m2})(V_{in,CM}-V_P)=I_{D1}+I_{D2}$$

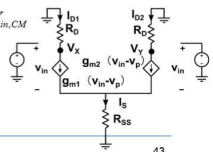
$$(g_{m1}+g_{m2})(V_{in,CM}-V_P)R_{SS}=V_P$$

$$\Rightarrow V_P=\frac{(g_{m1}+g_{m2})R_{SS}}{1+(g_{m1}+g_{m2})R_{SS}}V_{in,CM}$$



$$\Rightarrow V_X=-g_{m1}(V_{in,CM}-V_P)R_D=\frac{-g_{m1}}{(g_{m1}+g_{m2})R_{SS}+1}R_DV_{in,CM}$$

$$V_Y=-g_{m2}(V_{in,CM}-V_P)R_D=\frac{-g_{m2}}{(g_{m1}+g_{m2})R_{SS}+1}R_DV_{in,CM}$$



$$\Rightarrow V_X-V_Y=-\frac{g_{m1}-g_{m2}}{1+(g_{m1}+g_{m2})R_{SS}}R_DV_{in,CM}$$

$$A_{CM-DM}=\frac{\Delta g_m R_D}{1+2g_mR_{SS}}\quad(g_m=\frac{g_{m1}+g_{m2}}{2})$$

$$CMRR=\frac{A_{DM}}{A_{CM-DM}}=\frac{g_m}{|\Delta g_m|}(1+2g_mR_{SS})$$

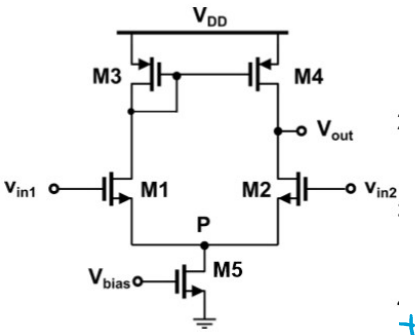
3. 二极管负载的差分对

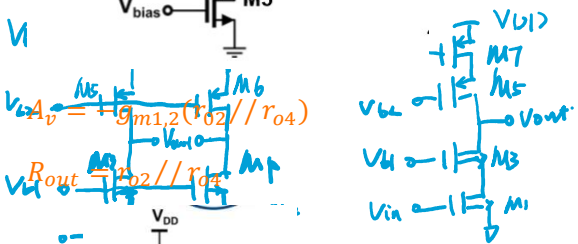
$$A_v=-g_{m1}(g_{m3}//r_{o3}//r_{o1})$$

4. Cascode负载的差分对

$$A_v=g_{m1}[(g_{m3}//r_{o3}//r_{o1})//(g_{m5}//r_{o5}//r_{o7})]$$

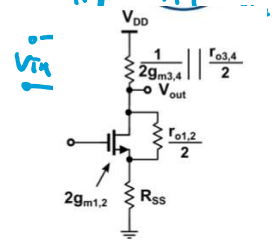
5. OTA





$$A_v=-g_{m1,2}(r_{o2}//r_{o4})$$

$$R_{out}=r_{o2}//r_{o4}$$



$$A_{CM}=\frac{1}{R_{SS}+1/(2g_{m1,2})}(1/(2g_{m3,4})//(r_{o3,4}/2)//(r_{o1,2}/2))$$

$$CMRR=(1+2g_{m1,2}R_{SS})g_{m3,4}(r_{o1,2}//r_{o3,4})$$

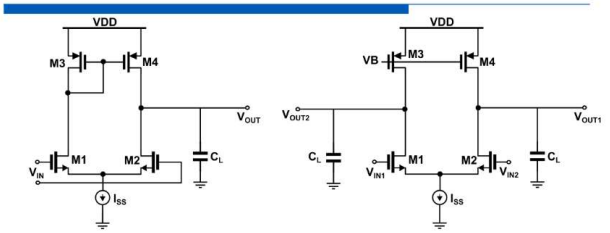
OPAMP

Ideal op-amp

- 压控电压源
- 增益无穷大
- 无限输入阻抗
- 零输出阻抗

一阶运放

Basic Topologies

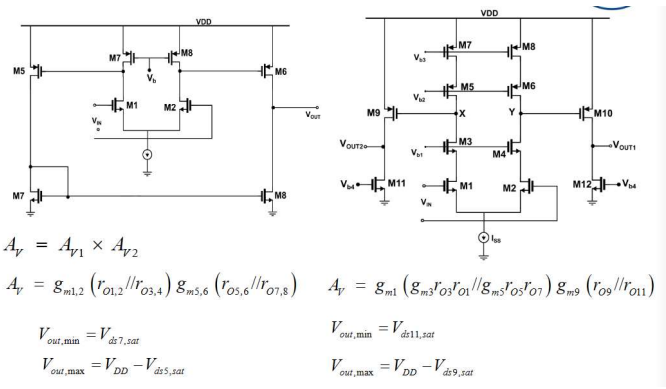


- **Low-frequency gain**: $A_O = g_{mN} r_{out} = g_{mN}\left(r_{ON} // r_{OP}\right) < g_{mN} r_O$
- **Bandwidth**: $\omega_1 = \frac{1}{C_L R_{out}} = \frac{1}{\left(r_{O2} // r_{O4}\right) C_L}$ $\omega_u = \frac{g_{mN}}{C_L}$
- **Output Swing** (single-side): V_{DD} -3V_{OV}
- **Mirror pole** in single ended

二阶运放

Stage1：High Gain

Stage2：High Swing



$A_V = A_{V1} \times A_{V2}$

$A_V = g_{m1,2}\left(r_{O1,2} // r_{O3,4}\right) g_{m5,6}\left(r_{O5,6} // r_{O7,8}\right)$

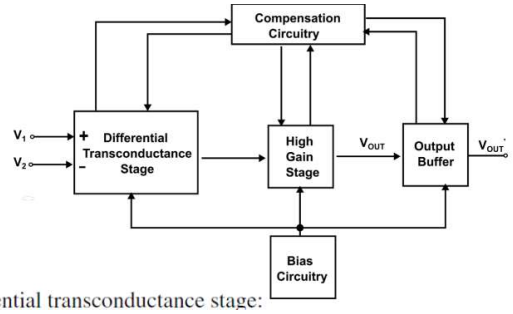
$V_{out,\min} = V_{ds7,sat}$

$V_{out,\max} = V_{DD} - V_{ds5,sat}$

$A_V = g_{m1}\left(g_{m3} r_{O3} r_{O1} // g_{m5} r_{O5} r_{O7}\right) g_{m9}\left(r_{O9} // r_{O11}\right)$

$V_{out,\min} = V_{ds11,sat}$

$V_{out,\max} = V_{DD} - V_{ds9,sat}$



ferential transconductance stage:

差分跨导级：输入，有时提供差分到单端的转换；

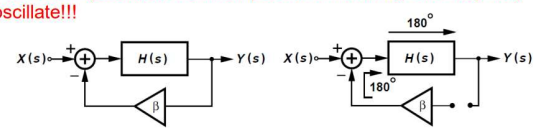
高增益级：由opamp和输入级提供电压增益

输出缓冲：如果opamp需要驱动低阻抗

compensation电路：保持OP稳定，当阻性负反馈。

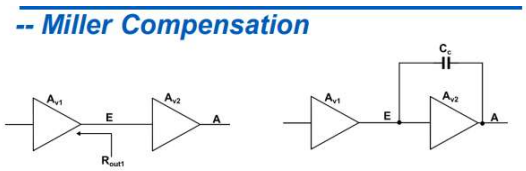
稳定性考量

- Feedback systems suffer from potential instability and they may oscillate!!!



- Closed-loop transfer function: $\frac{Y(s)}{X(s)}=\frac{H(s)}{1+\beta H(s)}$
- When $\beta H(s)=-1$, the closed-loop "gain" goes to infinity -> oscillate
- **Barkhausen's Criteria**: $|\beta H(j\omega_1)|=1$, $\angle\beta H(j\omega_1)=-180^\circ$
- **Negative feedback itself provides 180 phase shift**
- Loop transmission determines the stability issue

Miller 补偿

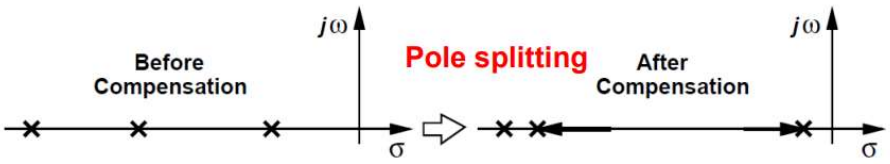


Stage 1: High output impedance

Stage 2: A moderate gain

dominanting pole：节点E的大电容

中电容导致低频极点-移除输出极点



其他问题

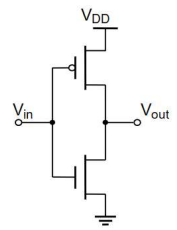
Input Range limitations

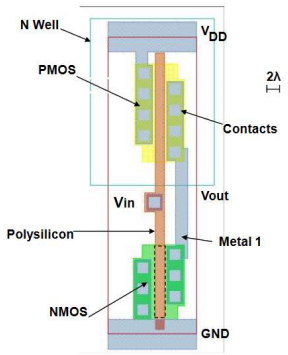
slew rate

反相器

基本结构

推挽式结构



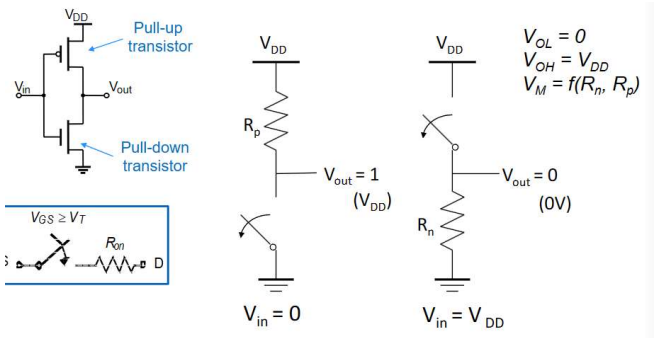


漏端相连，最小尺寸2λ

PN管的宽长比是不一样的，P更宽

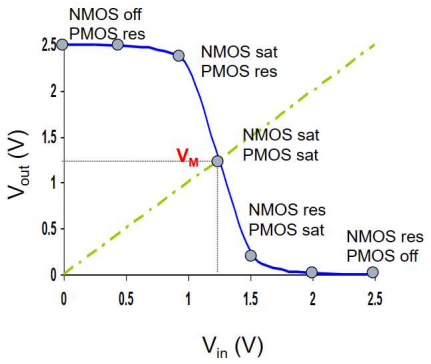
一阶直流分析

采用开关模型。（N管高于阈值电压导通，懂得都懂）

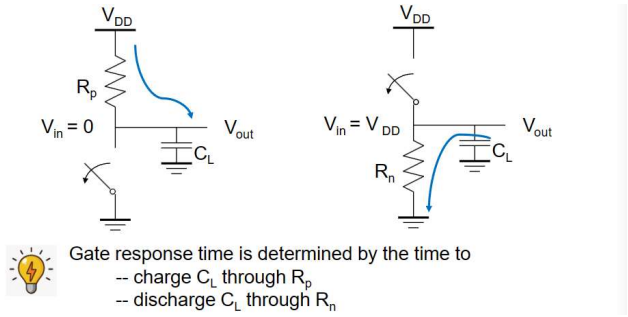


- 摆幅是rail to rail(VDD-GND)高噪声容限
- ratioless 无比电路
- 静态功耗小（VDD和GND之间没有直接通路）噪声和干扰不敏感
- 低输出阻抗
- 输入阻抗大

VTC(Voltage Transfer Characteristics)



动态特性（速度）



减小输出电容或者减小R_{on}（增大W/L）

瞬态响应主要由输出电容决定。

静态特性

开关阈值（V_M）

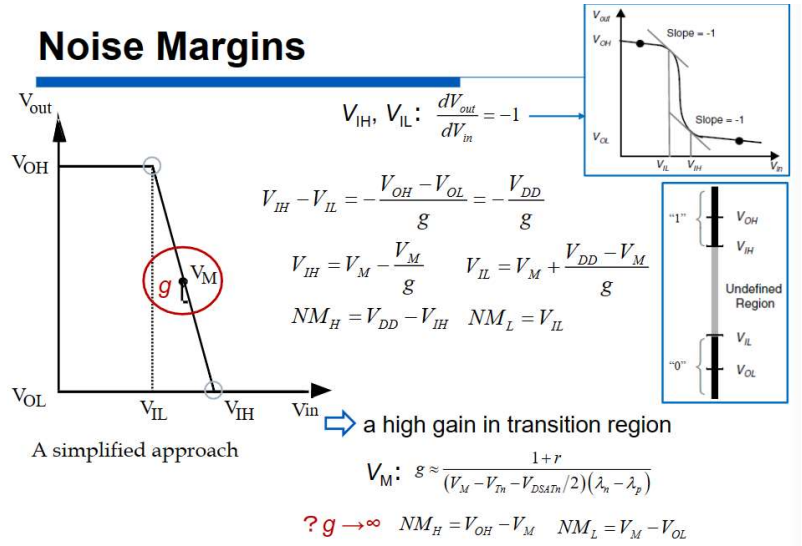
假设$V_{in} = V_{out}$，两个管子都在饱和区。

$V_M \approx r\,V_{DD}/(1+r),\quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{v_{satp} W_p}{v_{sqtn} W_n}$电子和空穴的饱和速度；$r$是相对驱动强度，基本上完全取决于宽度比。

为了让r接近1，P的宽度会做的比N大。

噪声容限

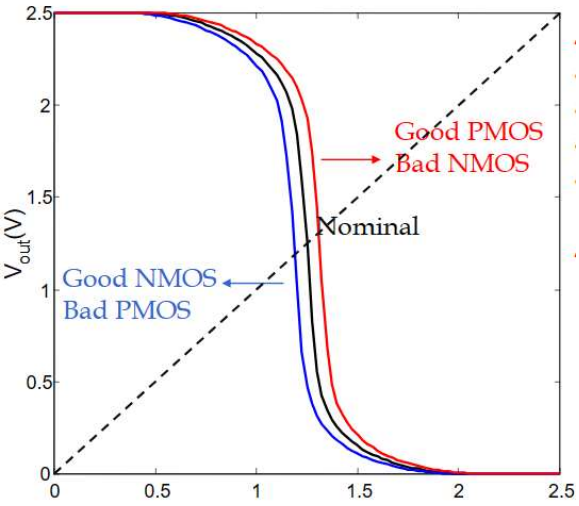
把斜率为-1的点当作截止点。



工程上是拿M点斜率作交点得到IH和IL。

$$V_M:\ g \approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

工艺的影响

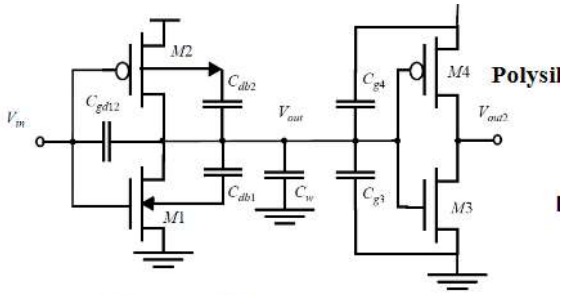


电源电压的影响

降低VDD改善增益，但$V_{DD} > (2to4)kT/q$

Dynamic Behavior

以CMOS为例，Cinc是第一级反相器的电容，包括栅漏电容和漏底电容；Cext是导线电容和第二级反相器的电容，包括两个栅源电容。

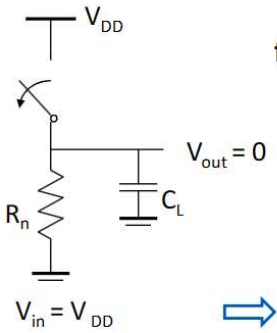


$$C_L = C_{inc} + C_{ext}$$

一阶传播延时

- Propagation delay is proportional to the time-constant of the network formed by the pull-down resistor and the load capacitance

$$t_p = \int_{v_1}^{v_2} \frac{C_L(v)}{i(v)} dv = f(R_n, C_L)$$



first-order linear RC-network:

$$t_{pHL} = \ln(2) R_{eqn} C_L = 0.69 R_{eqn} C_L$$

$$t_{pLH} = \ln(2) R_{eqp} C_L = 0.69 R_{eqp} C_L$$

$$t_p = (t_{pHL} + t_{pLH})/2 = 0.69 C_L (R_{eqn} + R_{eqp})/2$$

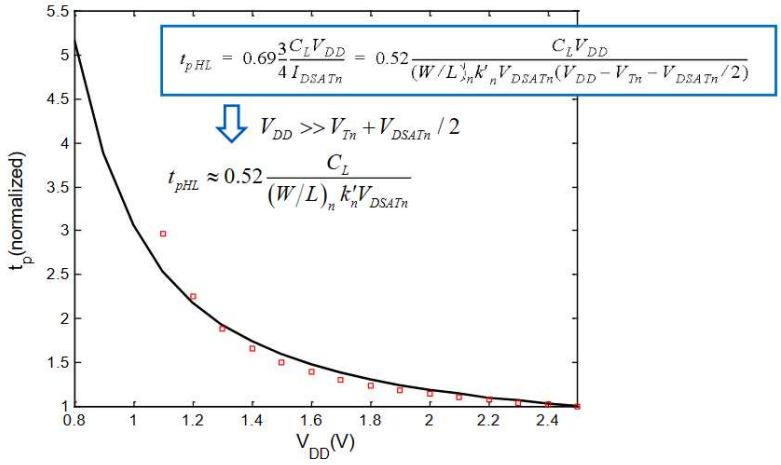
$$\Rightarrow t_{pHL} = t_{pLH} \qquad R_{eqn} = R_{eqp}$$

a symmetrical VTC

输出高到低看n，低到高看p

$t_{pHL} \approx 0.52 \frac{C_L}{(W/L)k_n V}$

? How to manipulate or optimize the delay?



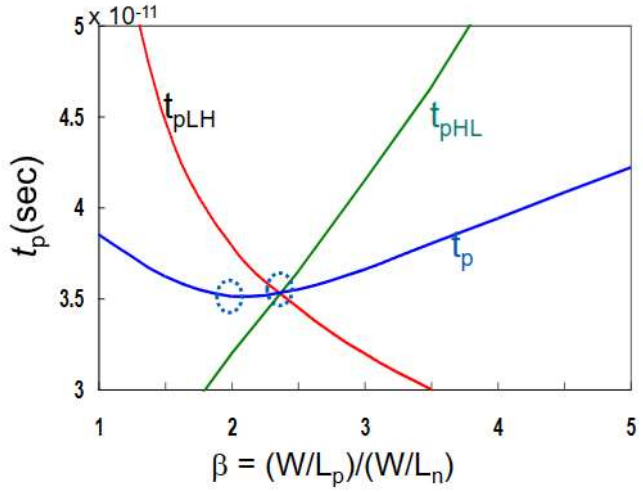
Trade-off between delay and consumption

为了减小传播延时：

1. 降低CL，keep the drain diffusion as small as possible
2. 增加宽长比
3. 增大VDD

NMOS/PMOS Ratio

- Symmetrical VTC and t_{pHL}=t_{pLH}: β = (W/L_p)/(W/L_n)=3~3.5
- If speed is the only concern, reduce the width of the PMOS device



$t_p = (t_{pHL} + t_{pLH})/2$

widening PMOS degrades t_{pHL} due to larger parasitic capacitance

$\frac{\partial t_p}{\partial \beta} = 0 \Rightarrow \beta_{opt} = \sqrt{r\left(1 + \frac{C_w}{C_{dn1} + C_{gn2}}\right)}$

$C_w \Rightarrow \beta_{opt} = \sqrt{r}$

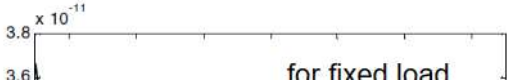
- β of 2.4 (= 31 kΩ/13 kΩ): symmetrical response
- β of 1.6 to 1.9: optimal performance

实际上最佳点的偏移：宽长比改变后不仅电阻改变，寄生电容也改变了。

- Divide capacitive load, C_L, into C_L,= C_{int}+ C_{ext}
  - C_{int}: intrinsic (self-loading) cap - diffusion and gate-drain (Miller) effect
  - C_{ext}: extrinsic load cap- wiring and fan out

  t_p = 0.69 R_{eq} C_{int} (1 + C_{ext}/C_{int}) = t_{p0} (1 + C_{ext}/C_{int})
  - intrinsic delay (unloaded, C_{ext}=0)

    t_{p0} = 0.69 R_{eq} C_{int}



- Size factor: S (reference gate)

$C_{int}=SC_{iref}$ $R_{eq}=C_{eq}/S$

$t_p = 0.69\, R_{eq}\, C_{int}\,(1 + C_{ext}/C_{int})$

$=0.69\, R_{ref}\, C_{iref}\,(1 + C_{ext}/C_{int})$

$= t_{p0}\,(1 + C_{ext}/SC_{iref})$

-- t_{p0} : the size of gate ✗
technology and layout ✓

-- S↑, t_p -> t_{p0}

反相器链

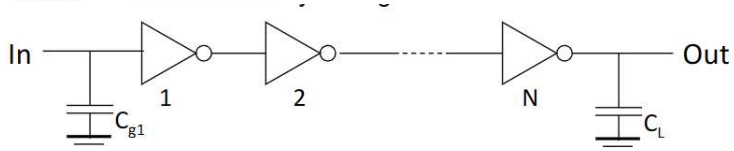
The delay of the *j*-th inverter stage:

$t_{p,j} = t_{p0}\,(1 + C_{g,j+1}/(\gamma C_{g,j})) = t_{p0}(1 + f_j/\gamma)$

and $t_p = t_{p1} + t_{p2} + \ldots + t_{pN}$ ⇨ $t_p = \Sigma t_{p,j} = t_{p0} \Sigma\,(1 + C_{g,j+1}/(\gamma C_{g,j}))$

$\frac{\partial t_p}{\partial C_{g,j}} = 0$ ⇨ $C_{g,j+1}/C_{g,j}=C_{g,j}/C_{g,j-1}$ $C_{g,j} = \sqrt{C_{g,j-1}C_{g,j+1}}$

- The optimum size of each inverter is the geometric mean of its neighbors sizes.



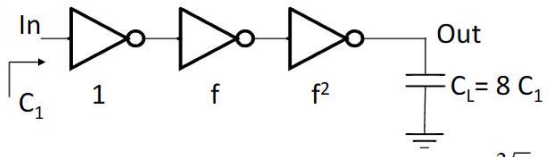
- The optimum size of each inverter will have the same effective fan-out and the same delay $f = \sqrt[N]{C_L/C_{g,1}} = \sqrt[N]{F}$

F: the overall effective fan-out of the circuit ($F= C_L/C_{g,1}$)

- The minimum delay through the inverter chain is

$t_p = Nt_{p0}\left(1+\sqrt[N]{F}/\gamma\right)$

Example



C_L/C_1 has to be evenly distributed across N = 3 stages: $f = \sqrt[3]{8} = 2$

最佳阶数N

- What is the optimal value for *N* given *F* ($=f^N$) ?

$t_p = Nt_{p0}\left(1+\sqrt[N]{F}/\gamma\right)$

  - if *N* is too large, the intrinsic delay of the stages becomes dominate
  - if *N* is too small, the effective fan-out of each stage becomes dominate

$f = e^{1+\gamma/f}$

  - **γ=0**: The optimal number of stages: ***N*=ln(*F*)** （**γ=0**）
    the effective fanout of each stage *f*=2.71828=*e*
  - **γ=1**

导线

Simplifications

- 忽略电感影响：导线电阻很大或者外加信号的上升下降时间很慢
- 导线间电容忽略，寄生电容模拟成接地电容：导线只在一段很短的距离靠在一起
- 当导线很短，截面很大或者互联材料的电阻率很低，可以采用只含电容的模型

现在的工艺通常使用Copper，但是Cu原子会扩散到硅并破坏FET；必须由diffusion barrier包围

Lumped model集总模型

要求比较短的导线

RC trees

不包含回路！

共享路径电阻$R_{ik} = \sum R_j \, j \in [path(s \to i) \cap path(s \to k)]$

Elmore delay: $\tau_{Di} = \sum C_k \, R_{ik}$

无分支RC树

$\tau_{DN} = \sum C_i \, R_{ii} = C_1 R_1 + C_2(R_1 + R_2) + \cdots + C_i(R_1 + R_2 + \cdots R_i)$

该模型可以用来近似一条电阻电容线，总长L，被分割成N段，$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}, \, R = rL, \, C = cL$

一条导线的延时是长度的二次函数。

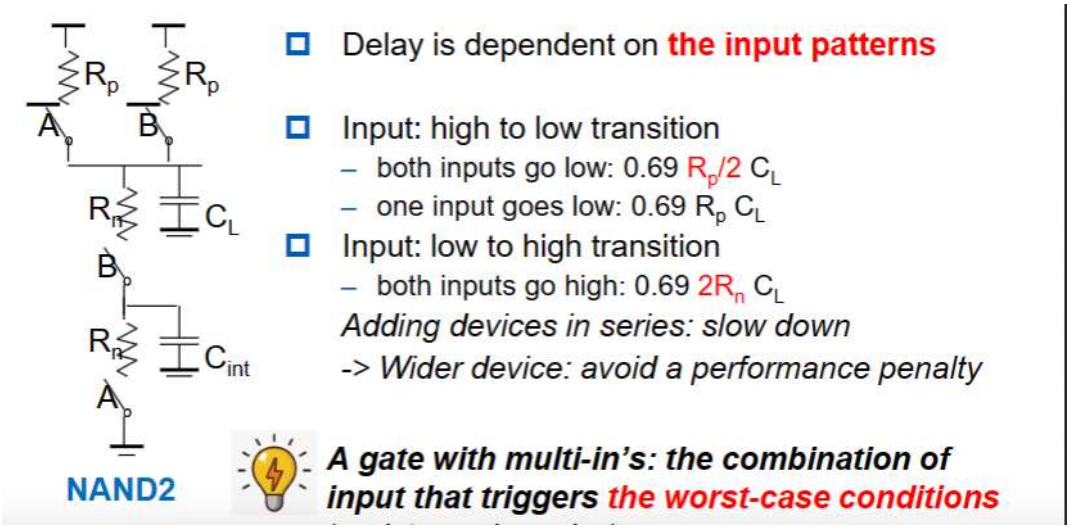
分布式rc线的延时是集总模型的一半

组合逻辑门

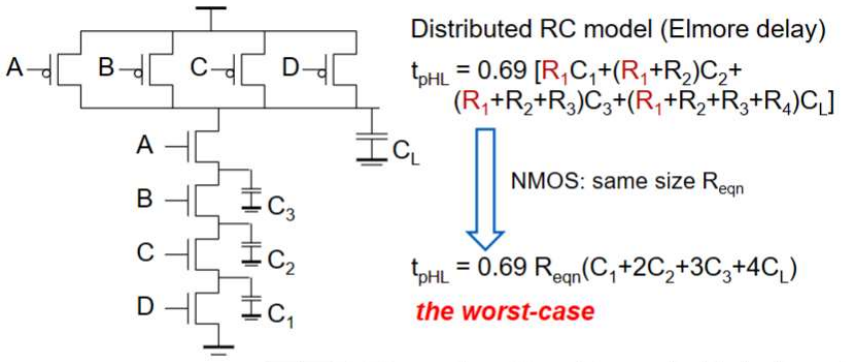
static CMOS

NMOS串联相当于AND，并联相当于OR，类似可推导出PMOS网络

根据DeMorgan定理，上拉网络和下拉网络对偶。



对这一模型的简单分析表明，与噪声容限相类似，传播延时也取决于输入模式。例如考虑由低至高的翻转。可以看到有三种可能的输入情形可以使输出充电至 V_{DD}。如果两个输入都被驱动至低电平，那么两个PMOS器件都导通。这时的延时为 $0.69\times(R_p/2)\times C_L$，因为这两个电阻并联。但这并不是最坏情形时由低至高的翻转，最坏情形发生在只有一个器件导通的时候，此时的延时为 $0.69\times R_p\times C_L$，对于下拉路径，输出只有在 A 和 B 同时切换至高电平时才放电，因此就一阶近似而言延时为 $0.69\times(2R_N)\times C_L$。换言之，增加串联的器件会使电路变慢，因而器件必须设计得较宽以避免性能下降。当确定一个多输入门的晶体管尺寸时，我们应当考虑能引起最坏情形的输入组合。



Ratioed Logic

减少晶体管数，但降低稳定性，功耗升高。

仿NMOS门：2N-N+1，降低噪声容限，引起静态功耗

Dynamic CMOS