线上学习线上测试2

本次测试为线上学习的线上测试部分。

1. Two processors A and B have clock frequencies of 700 MHz and 900 MHz, respectively. Suppose A can execute an instruction with an average of four steps and B can execute with an average of five steps. For the execution of the same instruction which processor is faster?

单选题(5 分)

A. A

B. B

C. Both take the same time

D. Insufficient information

2. The effectiveness of the cache memory is based on the property of ____.

单选题(5 分)

A. Locality of reference

B. Memory localization

C. Memory size

D. None of the above

3. The fastest data access is provided using _____

单选题(5 分)

A. Caches

B. Registers

C. DRAM's

D. SRAM's

4. Memory (____) needs to be refreshed periodically.

单选题(5 分)

A. SRAM

B. EPRAM

C. FLASH

D. DRAM

5. Interrupts can be generated in response to (_____).

单选题(5 分)

A. Detected hardware faults

B. Detected program errors such as arithmetic overflow or division by zero

C. Input/Output activities

D. All of the above.

6. What is the function of the compiler?

单选题(5 分)

A. Combines independent programs and resolves labels into an executable file.

B. Translate a high-level language into assembly language.

C. Translates source code into intermediates and immediately executes it.

D. Translates assembly language into binary instructions.

7. Which of the following statement is NOT true?

单选题(5 分)

A. The assembler translates symbolic, human-readable instruction into the binary version the machine understands.

B. The instruction set architecture of a computer is the abstraction from hardware to low-level software.

C. Register is implemented inside the main memory on computer board.

D. Von Neumann architecture has data and instructions in the same memory space.

8. The instruction set architecture of a computer specifies the vocabulary required by the program to execute instructions in the hardware.

判断题(5 分)

A. True

B. False

9. Assembly language is a symbolic representation of binary machine language.

判断题(5 分)

A. True

B. False

10. Embedded computers often have more limited power resources than general-purpose computers.

判断题(5 分)

A. True

B. False

11. To help the operating system estimate the LRU pages, some computers provide a dirty bit, which is set whenever a page is accessed.

判断题(5 分)

A. True

B. False

12. Write-through: A scheme that handles writes by updating values only to the block in the cache, then writing the modified block to the lower level of the hierarchy when the block is replaced.

判断题(5 分)

A. True

B. False

13. When meeting cache misses, “no write allocate” means only writing to main memory.

判断题(5 分)

A. True

B. False

14. If hit rates are well below 0.9, then they’re called as speedy computers.

判断题(5 分)

A. True

B. False

15. Each stage in pipelining should be completed within 5 cycles.

判断题(5 分)

A. True

B. False

16. If a data cache does not contain a dirty bit, then it must be using a write-through policy.

判断题(5 分)

A. True

B. False

17. Translate virtual address 0x18123 to physical address, given the contents of the TLB and the first 32 entries of the page table below(page size is 4KiB).

TLB

Index	Tag (Hex)	Physical page number (Hex)	Valid
0	05	13	1
	3F	15	1
1	10	0F	1
	0F	1E	0
2	1F	01	1
	11	1F	0
3	03	2B	1
	1D	23	0

Page Table

VPN(Hex)	PPN(Hex)	Valid	VPN(Hex)	PPN(Hex)	Valid
00	17	1	10	26	0
01	28	1	11	17	0
02	14	1	12	0E	1
03	0B	0	13	10	1
04	26	0	14	13	1
05	13	0	15	18	1
06	0F	1	16	31	1
07	10	1	17	12	0
08	1C	0	18	23	1
09	25	1	19	04	0
0A	31	0	1A	0C	1
0B	16	1	1B	2B	0
0C	01	0	1C	1E	0
0D	15	0	1D	3E	1
0E	0C	0	1E	27	1
0F	2B	1	1F	15	1

综合题(20 分)

(1) VPN = 0x ① , TLB tag = 0x0 ② .

TLB hit or miss(H/M) ③ , Physical Address = 0x ④ .

填空题(20 分) (请按题目中的空缺顺序依次填写答案)

① 18

② 6

③ M

④ 23123