

Design Through Verilog HDL

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Design Through Verilog HDL

T. R. Padmanabhan
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To my parents

B. Bala Tripura Sundari

To Ravi and Chandra

T.R. Padmanabhan

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PREFACE

Verilog has rapidly become a widely accepted language for VLSI design. The language is well-structured and defined to cater to the steady increase in the size of ICs to be designed without sacrificing the advantages associated with design at the “grass roots” level. A designer aspiring to master the language in its versatility should become familiar with the various constructs in it, practice their use in real applications, and use them in combinations to be successful.

Describing a design using Verilog is only half the story: Writing Test benches, testing a design for all its desired functions, and identifying the faults and removing them remain equally challenging tasks. This book is an attempt to address these issues effectively. The constructs in Verilog are discussed through apt illustrative examples. Equal importance is given to design description and test benches. The examples have been tested with popular and commonly used simulation packages and the results reproduced. In many of the cases the tested designs have been synthesized, and the synthesized circuit has also been reproduced. “Seeing is believing”: Seeing a design available as a software routine, transformed to a circuit, will add a lot to the confidence level of novices who use the book. flip-flops, counters, registers, coders, decoders, mux, demux *etc.*, have been considered at different levels of design; this should help in clarifying the perspectives regarding levels, need, and significance.

Place and significance of Verilog in VLSI design have been brought out in Chapters 1 and 2. Basics of the language, its conventions, *etc.*, are dealt with in Chapters 2 and 3. Chapters 4 and 5 form an introduction to design through Verilog. It is done at the gate level, which may be the most comfortable for the beginner. Any design, however involved it may be, can be completely realized in terms of the gate primitives of Verilog. We hope that the illustrative examples considered and the exercises at the end of the chapters, impart such a confidence to a designer. Chapter 6 is devoted to design at the data flow level. Continuous assignments using operators linking operands, which allow designs to be described more compactly but still close enough to the circuit level, form the theme of this chapter. Behavioral level design is discussed in Chapters 7 and 8. Mastery at this level – akin to the C language – is essential for a successful designer working at the system level. Functions and tasks, which facilitate structuring of designs and their orderly description, form the theme of Chapter 9. The switch primitives in Verilog constitute the link with actual VLSI implementation although their mastery is not essential to many of the designers with their higher level activities. Chapter 10 is devoted exclusively to switch level design; since it stands out from

the main text flow so far, its discussion is consciously deferred to this stage. Chapter 11 forms an introduction to the system tasks and functions in Verilog and their use in typical environments. Chapter 12 deals with design using PLDs and FSMs. Though subdued, the treatment is enough to give the necessary lead to more comprehensive designs.

All the chapters have enough exercises at the end. Some help mastery of the material in the chapter, through practice; others are structured to stimulate the users to explore avenues of their own. The step-by-step build-up of a processor in Chapter 12 is of this type.

All simulation results presented in the text as part of illustrative examples, have been obtained using the “Modelsim” software of Mentor Graphics. All synthesis results wherever presented, have been obtained using the “Leonardo Spectrum” software of Mentor Graphics. These have been reproduced by courtesy of Mentor Graphics.

Users’ views and suggestions are welcome; for this purpose, the website www.aitec.amrita.edu/publications may be accessed.

T. R. PADMANABHAN
B. BALA TRIPURA SUNDARI

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Our obeisance goes to *Mata Amritanandamayi Devi* for her commitment to societal transformation through quality education; this is a humble attempt to add another brick to the edifice being built by her.