A Front-End for a Magnetic Transmitter/Receiver

Final Report : Group 09

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Abstract

Communicating from beneath arctic ice poses significant challenges due to the complexities of sending signals through water, ice, and air. The current methods of acoustic and electromagnetic waves encounter the limitations of signal attenuation and speed constraints. This paper explores a potential solution to amplify and transmit magnetic inductance (MI) waves for underwater communication in the arctic. MI waves offer promise when crossing the medium interfaces, particularly within the frequency range of 100 Hz to 30 kHz. The proposed solution involved designing a transmitter and receiver comprising various subsystems like FPGA, H-bridge amplifier, transmission coils, receiving coils, and filters. The team delivered a PCB designed to amplify and transmit an analog input signal, and a design for a receiver which was moved out of scope during the project. The report includes supporting simulations providing a proof of concept to the purchased PCB. Results, work summaries for each subsystem, milestones, team structure, and budget are discussed. This report aims to provide an outline and conclusion to UW-Stream (the client) about the teams work on this project.

Table of Contents

Table of Figures

Table of Tables

Introduction

Communicating from below the ice in the arctic to a receiver above the water, ice, and air presents a difficult task. The most common ways for communicating are using acoustic and electromagnetic waves which are not suitable for this purpose. Acoustic waves are often used to communicate from one underwater system to another, but there are two issues presented when using acoustics to communicate through different mediums. The first issue is that the signal is greatly attenuated when crossing any interface with most of the signal being reflected towards the source. The second issue is that acoustic waves travel at approximately 1.5 km/s, which can cause delays and limit the bandwidth. Electromagnetic waves, while great for communication through air, travel much shorter distances in water. Using magnetic induction (MI) waves for transmitting offers a promising solution. Simulations and testing done by the client and presented to our team show that MI waves are attenuated the least and are most suitable for crossing the interfaces at frequencies between 100 Hz and 30 kHz. There is attenuation and noise added to the signal at these frequencies, but they are attenuated the least when travelling through different mediums. Using MI waves also has the benefit of transmitting at approximately one-ninth of the speed of light in water. This would allow for less latency and a higher bit rate when communicating in the arctic.

There are two use cases for communicating through ice that were discussed between the client and the team. The first was the ability for sensors that monitor conditions in the arctic to communicate their data for climate models. The second is communication with autonomous submarines that are trapped under ice. In both cases, the ability to communicate through ice is a significant advantage. The diagram below in Figure 1 shows the environment the system would be applicable to.

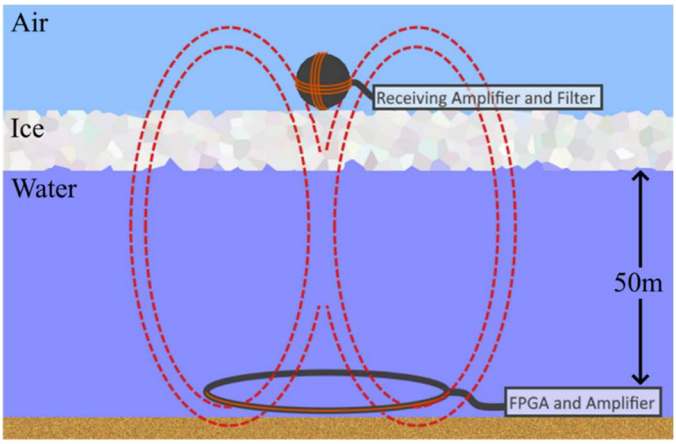

Figure 1: Project Overview Diagram

Project Objectives

The original objectives described by the client in January 2024 were a transmitter and a receiver made of the subsystems listed in Table 1. The FPGA was to be responsible for producing an analog frequency to the H-Bridge which amplified the signal to the transmission coil at 10-30 kHz, as determined by the client. The receiver was to capture the signal through its own receiving coil and using a low pass filter to amplify and isolate the transmitted signal.

Table 1: Deliverable Systems and Subsystems

System	***Subsystems***	***Purpose***
Transmitter	FPGA	Signal Generation
	H-bridge Amplifier	Signal Amplification
	Transmission Coil	MI Wave Creation
Receiver	Receiving Coil	MI Wave Receiving
	Pass Band Filter	Signal Isolation
	Amplifier	Signal Amplification

As of September 13th, a meeting with the client redefined our scope for the rest of the project period. Over the summer the client had a student working on the receiver, no longer needing it designed the client redefined our objectives to solely the amplifying transmitter.

Table 2: Changed Scope Deliverable System and Subsystems

System	***Subsystems***	***Purpose***
Transmitter	FPGA	Signal Generation
	H-bridge Amplifier	Signal Amplification
	Low Pass Filtering Circuit	Smooth output signal from Pulse Width Modulation (PWM)
	Transmission Coil	MI Wave Creation

The changes made from the technical memo represent a slightly more detailed breakdown of the requirements of the project. The changes also reduced the deliverables; although time spent on the receiver was unused, the effort will be shown in this report.

A stop work point is hit when the simulations for the amplifier are complete. The simulations must be accepted by the client before the team prints the design on a circuit board. Detailed explanations, models, and simulations will be delivered to the client to ensure nothing is overlooked and to make future work and changes easier to implement. The simulation and design of the H-bridge and receiver have been stressed as important by the client as the product continues to develop once the team has finish their capstone.

To prove what was produced is effective, testing of the finished transmitter PCB is an objective of the project. The system will initially be tested by component. The project will be testable in two components, the FPGA and the amplifier. After concluding that both components are valid, they will be combined to be tested by the full amplifier/receiver circuit. If all tests are successful, the system will be tested at Dalhousie's Aquatron, shown in the Figure 2 below.

Figure 2: Testing Environment, Dalhousie's Aquatron

Technical Requirements

This section of the report details the technical requirements for the project, specifying the desired performance and constraints of the system. These requirements ensured the project met functional, electrical, and physical design goals. Each requirement is paired with an explanation of its purpose and a defined method for verification and are shown in Table 3 below. Testing methods are further elaborated upon in the Testing section of this report.

Table 3: Technical Requirements

TECHNICAL COMPONENT	EXPLANATION	TESTING METHOD
SIGNAL GENERATION	The system shall deliver sinusoidal signals to the load. Users shall have the ability to select one of three frequency options: 100Hz, 1kHz, or 10kHz.	An oscilloscope shall be used to measure the output waveform. The frequency shall be verified by comparing the measured signal against the chosen frequency.
POWER THROUGH COIL	The system shall supply 5 amps of current and 25 volts of voltage to the load, resulting in a total power delivery of 125 watts.	Two oscilloscope measurements shall be taken, one to measure the current through the load and another to measure the voltage. Power shall be calculated and verified using $P = I * V$.

LOAD IMPEDANCE	The impedance of the load must not exceed 5 ohms. To maintain efficient power transfer, the reactance introduced by the transmission coil shall be offset using capacitors.	An ohmmeter shall be used to measure the impedance of the load.
TOTAL HARMONIC DISTORTION (THD)	The total harmonic distortion of the amplification PCB shall be less than 5%.	The output of the amplifier PCB shall be measured, and the total harmonic distortion shall be calculated with a fast Fourier transform (FFT).
SIZE	The size of the PCB system shall fit within a cylinder with a diameter of 150mm and a length of 480mm.	The PCB system shall be placed within the specified enclosure to confirm compliance with the size constraints.

These requirements provide a foundation for the system's development and serve as a reference for testing and validation. The next section, Methods, delves into the technical background and approaches considered for meeting these requirements.

Methods

Possible approaches

During the design phase of this project, we went through different approaches to the problem. There were three main components where we had choices to make in designing our solution. The first and main pivoting point of this was in the decision of how to amplify the sine wave. This brought us to a decision between two different approaches.

The first approach was to combine two half bridges from Efficient Power Conversion Semiconductors. This approach would also raise the need for an encoded Pulse Width Modulation (PWM) or Pulse Density Modulation (PDM) signal from the FPGA.

The second approach to the amplifier was to find an Integrated Circuit (IC) chip that would encode an analog sine wave and amplify the signal to twice that of the power source across its output terminals.

The choice was made to find an IC chip that met our engineering requirements for amplification and switching speed. This also solved a major design choice of how one would go about encoding a PWM vs PDM signal to the H-Bridge. This was originally a task to be done by the FPGA, however, with the approach of using the IC this no longer needed to be done.

The third decision that required a choice of design was how to balance the reactance caused by the induction coil at the load. This would be simple, with simply adding a capacitor to balance this out, however, we are working with three different frequencies therefor we need to switch between three different capacitance values. The decision we had to make was to use either a standard relay, or a solid-state relay. This decision was not difficult to make. The standard relay has a high internal impedance, while the solid-state relay has a relatively lower internal impedance. The solid-state relay also has no moving parts while the standard relay is a mechanical switch, which can be prone to mechanical error. The choice was made to go with the solid-state relay.

Technical Background

To amplify the analog signal, there are two concepts that need to be understood. The first is what control signals need to be sent to the H -Bridge, which comes in the form of a PWM signal. The second is how these signals manipulate the H-Bridge to produce a large output. In our case we utilized a class D power amplifier.

Class D power amplifiers, compared to class A, B, and AB linear power amplifiers have a much higher efficiency. The efficiency of class A, B, and AB linear amplifiers are below 75%. Class D power amplifiers can yield an efficiency of 100% in principle, but generally produce an efficiency in the range of 85-95% (Hui Feng, 2010).

To create the control signals for the internal H-Bridge we need to encode the analog input signal into a PWM signal. A PWM signal operates by encoding a sine wave within a signal. The goal is for the average voltage within the modulated signal to follow that of the input, this is done by

changing the duty cycle incrementally within each subsequent period to follow the average input voltage.

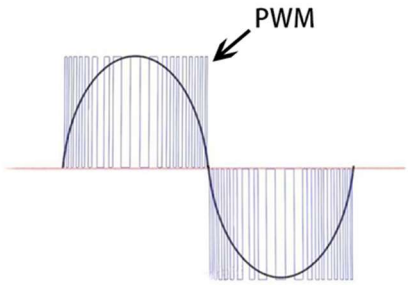

Figure 3: PWM encoded signal

As seen from the figure above, the voltage is followed by incrementally increasing then decreasing the duty cycle of the input at the high input voltage. The PWM is routed to control the Field effect transistors (FETS) in the H-bridge.

The H-bridge will output a fast-changing voltage and current over the load. The H-bridge is a circuit comprised of four FETs resembling the two edges of an H while the load resides in the 'bridge' in between the FETs. The H-bridge turns the FETs on and off to allow the current to flow across the resistor in one direction, observing Figure 4 below, in this instance the current flows through Q1 across the load and then through Q4. Through a process of changing the FETs states allows for current to flow across the load in the opposite direction, through Q3, across the load, then through Q2. This allows the H-bridge to create a sine wave across the load without putting the stress of that power through the FPGA.

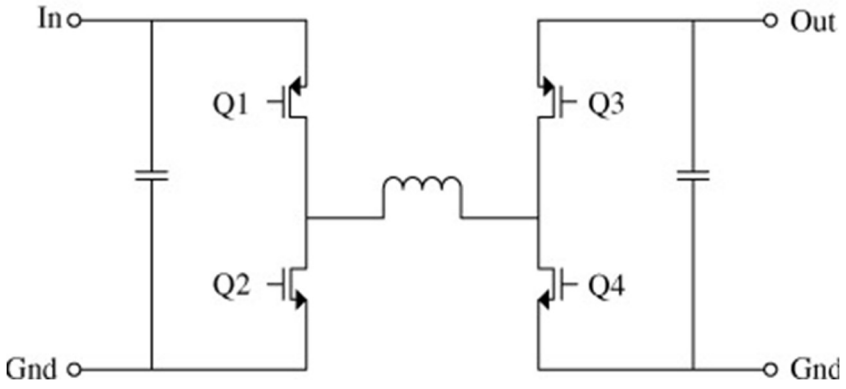

Figure 4: H-Bridge visualization

At the output of the chip the PWM voltage will be twice that as input from the high-power source. The output across the load creates a sine wave with added harmonics, which is close to our target output, a high voltage sine wave but with added high frequency harmonics.

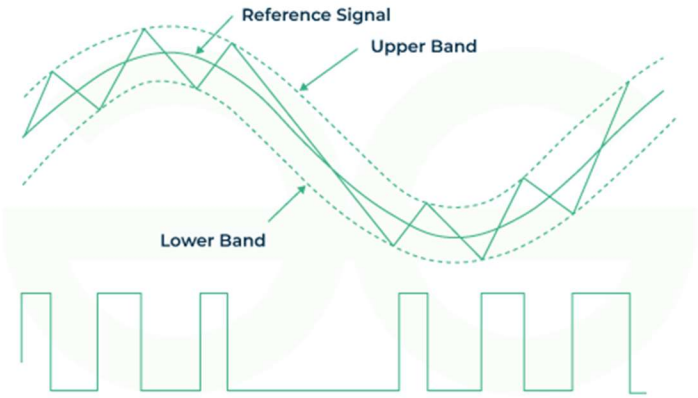

Figure 5: Harmonic distortion within Output Signal

In our case the source will initially supply 12.5 volts, to push 25 volts at the output. This voltage will be encoded in a 450-600 kHz PWM output. Sending this high frequency directly across the induction load will not produce a smooth wave as shown by the image above.

The next piece of technical background is the theory behind the low pass filter. To achieve a smooth voltage output, a low pass filter is needed to smooth out the voltage that the inductor sees. The manufacturer of the chip, TI, has a recommended filter for their load which is a 2-4 Ω resistive load. Since our inductor was a reactive load, we needed to adapt the recommended output filter to the load. A low pass filter removes the high frequencies and leaves the low ones which filtered at the end of the PWM, will produce a smooth low frequency sine wave.

To be able to successfully generate a magnetic field strong enough to carry the signal from the water into the receiver in the air, the signal needs to have a high current. Ampere's law from Maxwell's equations states that:

$$\int H.dl = I$$

The equation means that the magnetic field intensity "H" depends on the current "I" in this case going through the coils of the inductor. The client has determined based on their research that a

current of around 5A should be appropriate for the purpose of this project. To be able to generate this current, the client has communicated to the design team that they estimate the impedance of the coils will be 1.86mH, this means that the voltage needed to achieve this current would be approximately 25V.

Work Plan and Milestones

This section of the report details the work plan and milestones that the team has set to finish this project by mid December 2024.

Work Plan

The work for the project was broken down into four main sections: project set up, system design and simulation, design revision, and design assembly and testing. As of the submission of this report, the project is 87% complete according to the progress of our Gannt chart, which is in the appendices.

The first section, project set up, aimed to outline the project objectives and engineering requirements, as well as the initial research. This period lasted from when we were assigned our project in mid January to early March. In this time, we conducted literature review on all of the different components of the project, including but not limited to H-Bridges, VHDL code, receivers, and filters. Following this, the design of the first version of the receiver was completed and simulated.

The second section of our project was spend working on preliminary designs of the system. The first achievement was developing a system architecture, as well as outlining the inputs and outputs between each system. In this section we also presented our poster in the capstone poster presentations and created a progress report outlining our work and initial design. This section of the project bled into the summer, with the second version of the receiver being produced. The second version of the receiver came with improved active filtering and a higher order filter. The last thing accomplished in this section is the recommendation of using a smaller wire gauge to handle the current; by recommending a larger wire diameter, the induction coil will be able to

handle the current. This section, by the early completion of the second version of the receiver differed from the original work plan.

The following sections differed from the original workplan.

The third section started off with a change in scope, as of September our team was notified that the receiver was no longer needed, and we removed if from our scope which significantly changed the breakdown of our work. Benjamin converted to leading the hardware design with Aethan's help on the transmitter. Jake switched to working onto only the FPGA. Within this section of the work a lot was completed. The transmitting coil was remade with the suggestion of a larger wire carrying the current. Developing the transmitter on a single PCB was done in this section of the semester, including the chip selection, simulation and implementation, as well as the low pass filter design, simulation, and implementation.

The fourth section of the project is the manufacturing, assembly, and testing of the system. As of the submission of this paper, we have recently received the components and are in the assembly process. This will lead us to the testing phase to test and validate the amplifier.

Table 4: Project Progress

SYSTEM	SUBSYSTEMS	PURPOSE	COMPLETION
TRANSMITTER	FPGA	Signal Generation	40%
	H-bridge Amplifier	Signal Amplification	Complete
	Transmitter PCB (new from scope change)	Single Platform for all of Transmitter	Complete
	Transmission Coils	MI Wave Creation	Complete
RECEIVER	Receiving Coils	MI Wave Receiving	Out of scope
	Pass Band Filter	Signal Isolation	Complete (out of scope)
	Amplifier	Signal Amplification	Complete (out of scope)

Including the table of deliverables from the workplan in the technical memo, we have mostly completed the project. Note that from the scope change, the receiver that was designed with a

band pass filter and amplifier design was completed but left the scope of the client. We currently have failed to meet two deliverables still within the scope of our project, which is the FPGA, and the testing of the amplifier PCB.

The first deliverable that was not met was the coding of the FPGA. The set up to be able to code the FPGA was not simple, and the lab we work with needed to order a new computer to be able to work with the FPGA. This new computer was delivered mid semester and by the time the software lead had Linux set up to work with the FPGA, the leads workload from school distracted him from the work needed to finish the deliverable. However, to test the transmitter PCB, the main deliverable of the project, the FPGA does not need to be complete as we can use a signal generator and power sources to source the analog input and control the capacitor bank.

The amplifier PCB has not yet been tested. This is a deliverable we have not yet delivered, but plan on completing by mid December. The PCB was supposed to be printed and assembled by a PCB manufacturer. In the initial research into the manufacturing process, it was assumed that it was a quick process for assembly with the manufacturer, however, when going through the ordering process for assembly, the manufacturer did not have all the needed components to construct the PCB. Given that it was not easily assembled, the decision was made to separately purchase the PCB and components, then assemble the PCB in house. Due to this oversight, the testing of the product will be delayed by one to two weeks. The assembly and testing will be complete by December 18th.

Even with the two incomplete deliverables not being met within the course time, the team will still be able to test and validate the final amplifier PCB by December 18th.

The supporting Gantt chart to the timeline is in Appendix A.

Milestones

We hit eight major milestones during our project. These milestones outlined our progress and achievements as we progressed. The milestones ranged from developing the engineering requirements of the project, milestones that enabled us to move from theory to application, and finally milestones that hit deliverables.

The first milestone we hit was creating an engineering outline of the deliverables of our project. Working with our client to outline the deliverables of our project was a crucial step as it allowed for us to begin designing a system architecture.

The second milestone we reached was creating the second version of the receiver design. The first design of the output filter isolated and amplified the transmitted signals showed a promising result. However, even with this first design we felt that it could be improved. This second milestone was hit when we achieved improved gain and isolation of the transmitted signals, showcasing a product that was ready to be built on a PCB.

A large milestone was the change in scope of the project. This large change meant that our focus was to go from designing a transmitter and receiver, to just designing the transmitter. This milestone didn't signify an accomplishment from the team, but it did make a significant impact on the project.

The next major milestone we hit was identifying a chip that would work for both encoding the PWM signal and implementing these signals onto a H-Bridge. This step took a lot of research and data sheet validation. With the chip chosen, we were able to achieve viable simulations to get a PWM output, the goal with the chip.

The fifth milestone we hit was getting Linux working on the new lab computer. Getting this working meant that we were able to begin coding the FPGA from the computer. This was a major milestone as the FPGA is needed to output an analog signal and select the capacitors.

The next major milestone we hit was in the final design of the low pass filter. The output of the TPA3255 chip is a high frequency encoded PWM and needed to be filtered to a sine wave at one of our three frequencies. The design of the low pass filter achieved an acceptable filtering of the voltage, and with the simulations working, we were then able to move onto simulating the whole system.

The seventh milestone was achieving a working simulation of the entire Transmitter PCB system. This is a very significant milestone because it meant that we could move onto the design of the PCB in Altium.

The last major milestone up to date is having the Transmitter PCB designed and ordered. This is a huge milestone as the product that was in design for months was finally complete, and in the manufacturing stage. This will lead us to assembling the system and testing in a laboratory.

Team Structure

The team that worked on the Front-End Magnetic Transmitter/Receiver consists of three individuals in Dalhousie's Electrical and Computer Engineering program.

Aethan Cubitt – Project Manager

Aethan took on the project manager role on the team. This consisted of making sure that the group is on time with the milestones and tasks. By keeping an open line of communication between the team members Aethan delegated work to spread the load evenly and work to individual strengths. Aethan was also the external point of contact for the team and worked to keep UW-Stream up to date on the progress of the project and ensure that both the client and the team are on the same page with the development of the project. Aethan was also responsible for aiding in the design of the Transmitter PCB. This included working with ben in both chip selection and implementation, and low pass filter design, as well as the LT-Spice simulations for the low pass filter design. Aethan worked in tandem with Benjamin to generate the Gerber files, finding a manufacturer for the PCB. Aethan worked with the client in ordering and billing the parts and PCB. Aethan wrote the Abstract, Introduction, Objectives, Methods, Workplan, Gantt Charts, Simulated Results, Conclusion & Recommendations.

Benjamin Jarrin - Hardware Lead

Benjamin took on the role of hardware lead. This means that Benjamin oversaw the hardware designs and approved each design and choice in the design process. Benjamin was responsible for the design of the Transmitter PCB board. Benjamin and Aethan worked on chip selection, and low pass filter design. The Altium design of the PCB fell into Benjamins hands, using the TPA3255 datasheet, Benjamin implemented the design into a PCB. Benjamin generated the Gerber files from Altium, as well as an extensive bill of materials for the 97 components on the PCB. Benjamin was also responsible for the design of both versions of the receiver in the first half of the project, creating a validated design. Ben Wrote the Proposed Amplifier Solution.

Jacob Janson – Software Lead/Safety Manager

Jacob took on the role of software lead within the team structure. This entailed the design of the FPGA logic using VHDL software. Jacob was responsible for creating a valid output from the board that will be fed to the Transmitter PCB. This was done by working with and setting up the FPGA board within the client's lab and working with the master's students to implement VHDL code to output an analog sine wave, and control signals to the capacitor bank. Jacob also took on the role of doing the wire sizing of the transmitting and receiving coils. Lastly, Jacob took on the role of safety manager to ensure that when the team is working with low to medium power that it was done in a safe manner. Jacob wrote the Technical Requirements, Budget, Proposed FPGA solution, Testing, & Discussion.

Project Budget

The initial project budget provided by UW-Stream was one thousand dollars. The UW-Stream lab had given the team some components from previous years and projects that were used without impacting the budget. The first component that was used from previous years was the Zybo Z7-10 FPGA board. This board would cost more than $400, but since it was provided, it did not impact the budget for this project. A second item that was provided by UW-Stream was the signal generator and oscilloscope which will be used to verify parts of the transmitter.. A new computer was needed to program the Zybo Z7-10 board. This computer was provided by the lab and cost approximately $1500 plus tax. A new transmitter coil housing and wire was needed at an estimated cost of $50 from the lab's budget.

The $1000 for the team's budget was used for printing and populating the transmitter PCB. The cost of the PCB was broken into three stages. The first was components ordered through DigiKey which cost $250. The second was components ordered through Mouser Electronics which also cost $250. The third was the printing and population of the PCB which cost $60. The total cost for the PCB was $560. Components were ordered from both DigiKey and Mouser Electronics since each supplier had only some of the required parts.

A cost analysis of this project is shown in Table 5 below.

Table 5: Project Cost Analysis

Item	Cost ($)
DigiKey Components	250
Mouser Electronics Components	250
PCB Board Printing and Population	60

The total cost of the project was $560. This is 56% of the initial project budget given to our team. The estimated cost after the first semester of this project was $800 (80%). The actual cost was lower because the receiver was removed from the scope which brought down the PCB costs and the transmission coil was moved to UW-Stream's lab's budget.

Proposed Solution

Within the scope, two designs were originally undertaken as part of the project scope. These two designs consisted of the amplifier and receiver of the system.

The amplifier has six main design components to complete the task of amplifying a user input signal. The software architecture of the FPGA is a scoped in view of the FPGA design component in the amplifier. The signal input starts in the FPGA, which from observing the software architecture in the figure below, has two outputs. The first output is to the analog input of the amplifier, and the second output is to the Capacitor Bank.

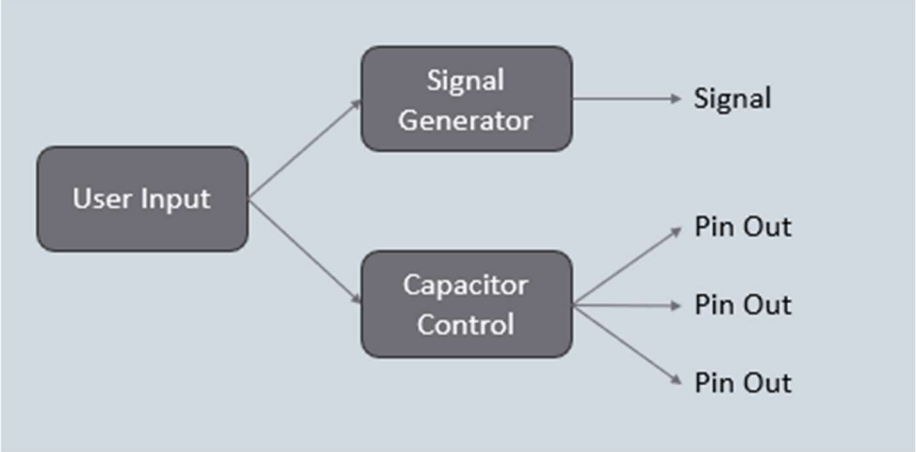

Figure 6: FPGA software architecture

The FPGA's outputs both go to the systems residing on the Transmitter PCB. The analog signal from the FPGA is routed to a chip that converts the analog signal to a PWM signal. This generated PWM signal goes to the gate drivers that control the FETS operation mode. This converts the small control signals into the high-power output of the chip.

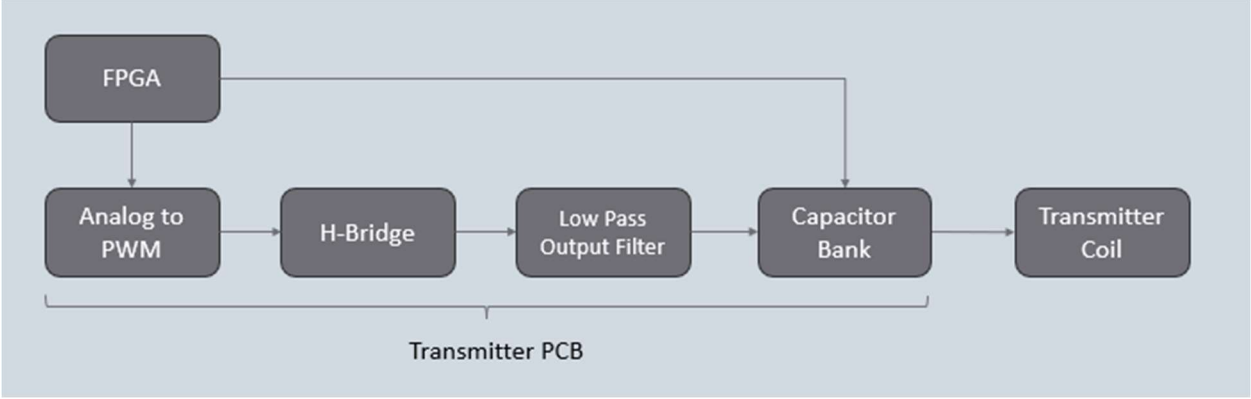

Figure 7: System Architecture

The output of the H-Bridge is pushed through the 2nd order low pass filter. The filter smooths out the PWM output and feeds the power to the load. To cancel the reactive component of the coils and achieve a higher power transfer, a capacitor was placed in series with the load. Since the coil's reactance depends on the frequency, a capacitor bank was implemented to have a different capacitor value for each of the 3 chosen frequencies to transmit.

Although the receiver was deemed out of scope during month nine of the project, extensive work had been undertaken on the project. In the first version of the receiver, a second-order Chebyshev filter was designed. After testing on software, the simulated receiver had room to be improved upon. This took us to designing a sixth-order Chebyshev active filter to isolate the received signal.

The individual proposed subsystems are explained in detail in the sections below.

FPGA

The FPGA board provided by the client is the Zybo Z7-10 shown in Figure 8 below. This board was capable of running Linux to interface with the FPGA. VHSIC hardware description language (VHDL) had been planned to be used to program the FPGA. This board was planned to be the signal generator for the project; however, this was not completed.

To act as the signal generator, three possible methods were researched. The first was using PWM. PWM would have used a pulse length of 2 nanoseconds, which would have adjusted its time spent high to generate a signal. A second strategy was to use pulse density modulation (PDM). PDM used a consistent length of pulses and controlled the delay between each pulse. The reason PWM and PDM were explored at the beginning of this project was because they could drive the H-Bridge. When the decision was made to use a chip with a built-in H-Bridge controller, the FPGA deliverable was revised to generate an analog signal. The third method involved generating an analog sine wave. This was the approach pursued the furthest since the team had access to libraries to aid in its development. For each approach, the output voltages for the signals would have been calculated on a different computer and loaded onto the board. The FPGA would then have used the file to lookup the next voltage to output, rather than calculate the next step continuously. This was intended to reduce the complexity, power consumption, and inaccuracies of the output signal. The FPGA was expected to generating sine waves at three different frequencies, 100Hz, 1kHz, and 10kHz. The FPGA was also meant to control the capacitor bank on the PCB shown in Figure 16.

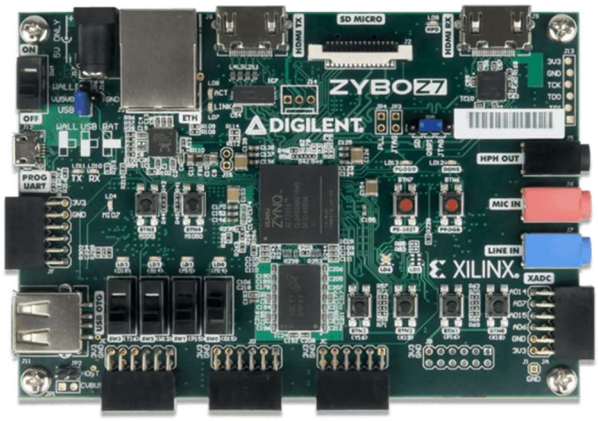

Figure 8: Zybo Z7-10 FPGA Board (Digilent, 2024)

Transmitter

The transmitter PCB is the main product that was designed. This PCB has all the components and modules necessary to amplify the signal coming from the FPGA into the final output going into the coils that generate the magnetic field responsible for the transmission of the signal.

Figure 9 below shows the main schematics created for the transmitter.

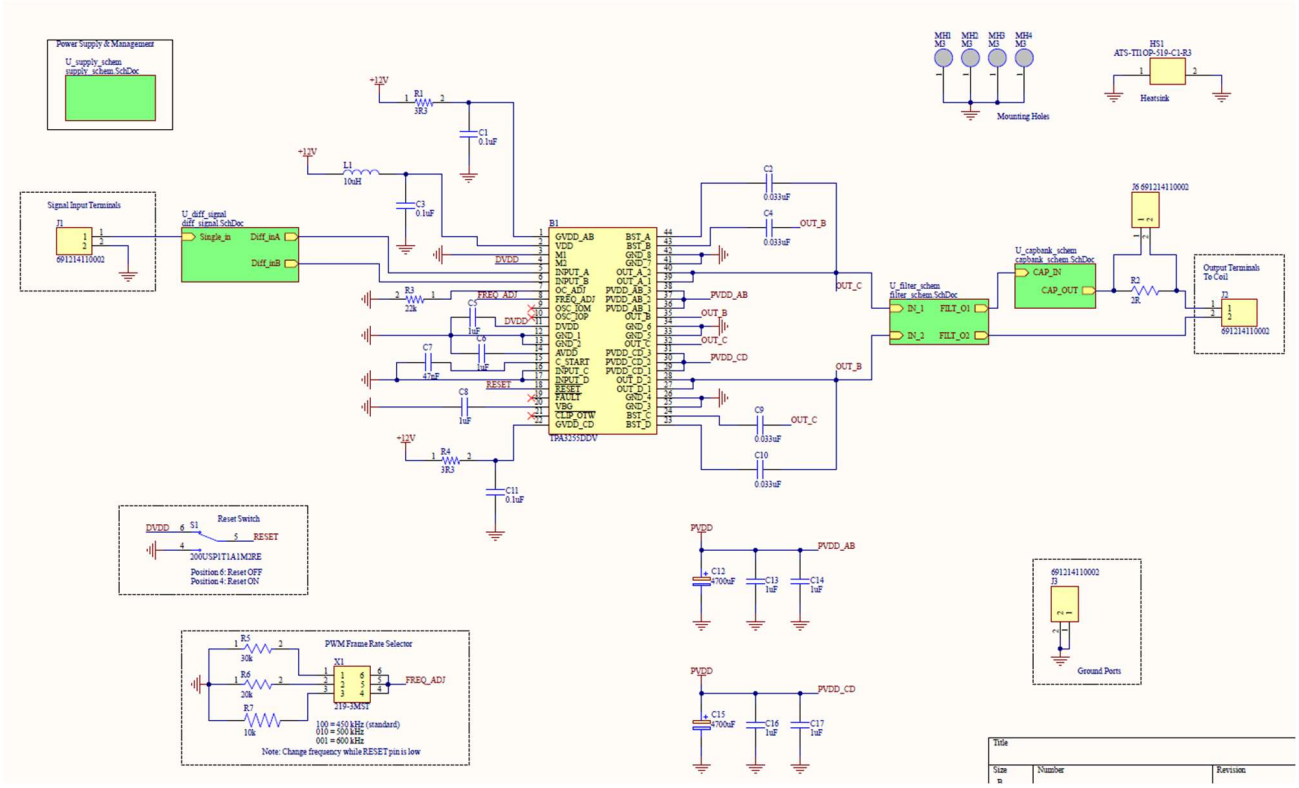

Figure 9: Transmitter PCB Main Schematics

In Figure 9, the central component “B1” is the main amplifier module. The chip chosen for this is the TPA3255 by Texas Instruments. This chip is a class-D audio amplifier that can output out to 600 Watts of power. Furthermore, this chip accepts an analog input which makes it easier to implement because this no longer must be done by the FPGA. The block diagram of the TPA3255 has been included in Figure 10 below.

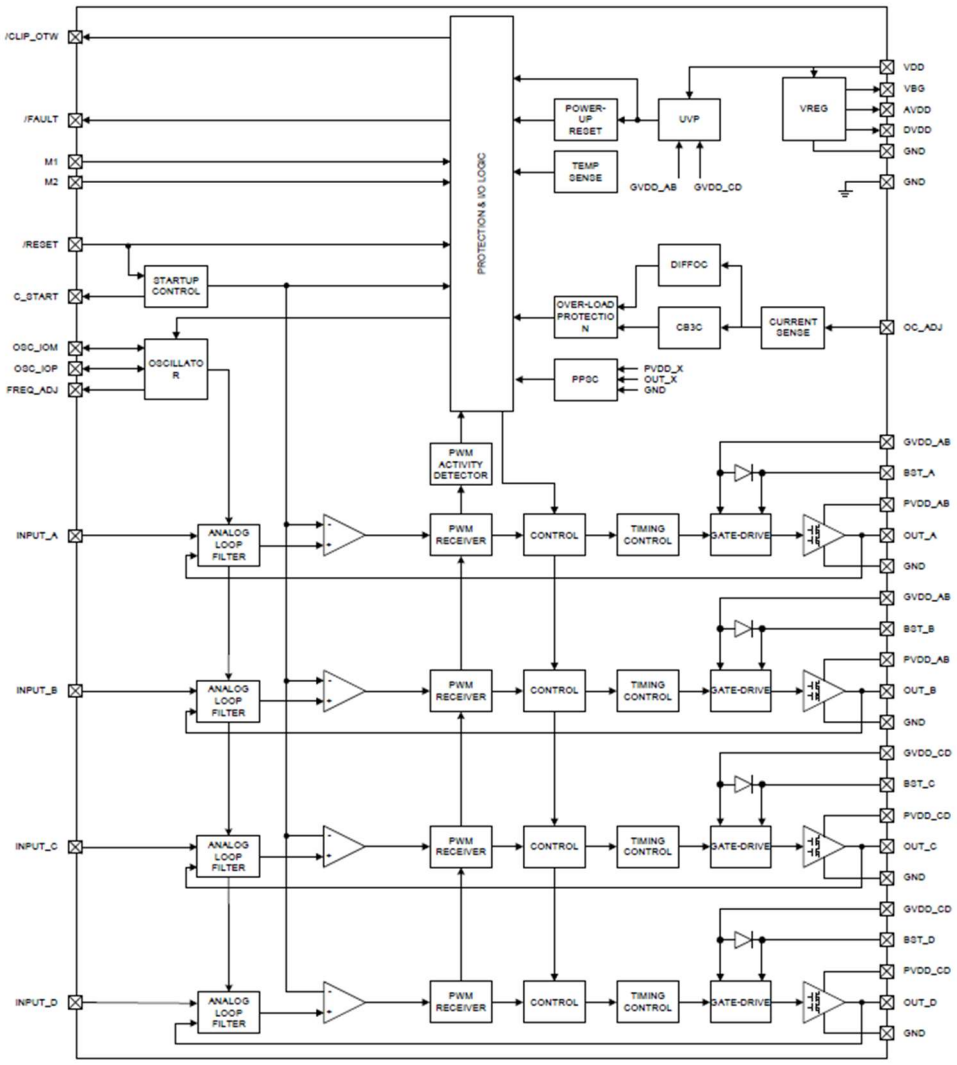

Figure 10: TPA3255 Block Diagram (Texas Instruments, 2016)

As seen in Figure 10 the TPA3255 converts the analog input to a PWM signal internally. Then, after going through additional blocks, it goes to the gate drivers that are responsible for controlling the FETs in the H-bridge with the appropriate deadtime to ensure there are no short circuits. One of the big benefits of the TPA3255 is that it incorporates the FETs internally which removes the necessity of implementing bulky power FETs as individual components.

When the schematics were being developed, the TPA3255 datasheet was consulted to ensure all pins were connected to the right components and was consulted for the values of the resistors, capacitors, and inductors. The resistance, capacitance, and inductance values of the components connected to the TPA3255 as seen in Figure 9 were stated by the datasheet based on the design requirements of our solution which incorporated a single load with a single input.

The PWM frame rate selector in Figure 9 is a submodule that allows the user to select the desired PWM frame rate. A 3-position dip switch was used to select the desired value as specified in the schematics.

The reset switch module in Figure 9 is a regular switch that allows the user to stop the amplification and reset the chip to change the frame rate.

The “single input” terminals “J1” on Figure 9 are the main input into the PCB. A 2-position terminal block was used for this. A single-ended signal is required at the input which would come from the FPGA or any other source desired.

The component “R2” in Figure 9 is a 2ohm 100 Watt resistor. This resistor is in series with the load and its purpose is to allow a precise load current reading by connecting an oscilloscope to terminal “J6”. By doing so, the voltage in the resistor can be monitored. Since the resistance value is known, the current in the coil can be calculated.

The “output terminals to coil” component in Figure 9 is a 2-position terminal block which is the main output of the system. The ends of the coil will be connected to this terminal.

The modules that are seen as green blocks in Figure 9 have their independent schematics and will be reviewed in detail in the next subsections.

Power Supply Management

The power supply management is the module that handles the power to all the components in the transmitter PCB. The schematics for this module are shown in Figure 11 below.

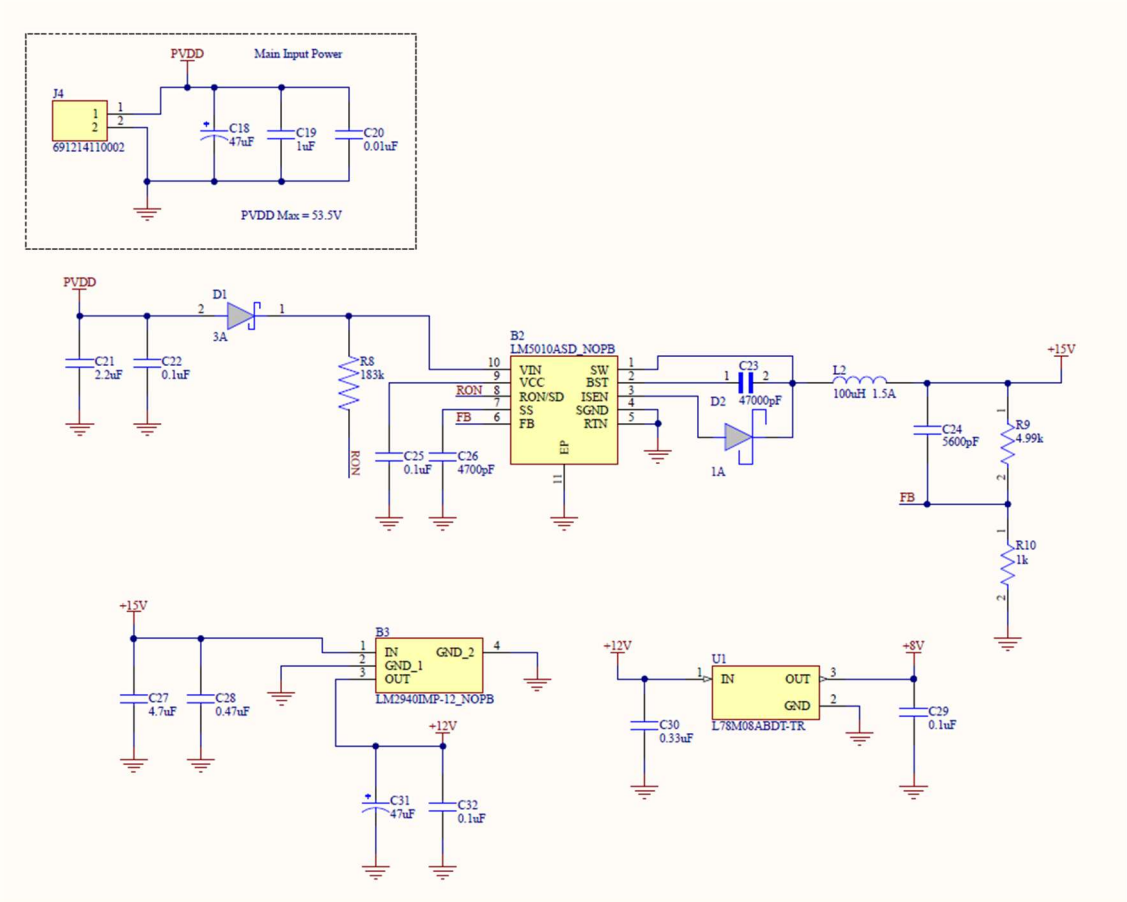

Figure 11: Power supply management schematics

The “Main input power” submodule seen in Figure 11 has the terminals where the main power source for the PCB will be connected. This is the only power source for the board and will be powering all the electronics as well as the amplification. A voltage in the range of 15 VDC to 53.5 VDC can be supplied through these terminals, with a higher voltage resulting in a higher output power from the H-bridge.

The submodule with the component “B2” as seen in Figure 11 is a step-down switching regulator. The LM5010 chip by Texas Instruments was used to perform the step-down switch regulating. This submodule is responsible for stepping down the main input power voltage to 15 VDC. A switching regulator was used in this stage to deal with the high range of input voltages in an efficient way. However, switching regulators tend to have a higher level of output ripple or noise.

To overcome the ripple in the switching regulator, a linear voltage regulator sub-module was used to further step down the 15 VDC into 12 VDC. This submodule can be seen in Figure 11

with the chip “B3” being an LM2940-12 by Texas Instruments. This linear regulator makes sure the output voltage is as clean and stable as possible. This 12VDC supplies power to the TPA3255.

The final submodule in Figure 11 with the “U1” chip is another linear voltage regulator that steps down 12VDC into 8VDC. The submodule uses the L78M08ABDT-TR chip by STMicroelectronics to supply 8VDC to the differential amplifier explained in Differential Signal subsection.

Differential Signal

The TPA3255 requires a differential input to operate the amplifier in the chip's differential PBTL mode—a single H-Bridge configuration. Since the FPGA supplies a single-ended input, a module that created a differential input was needed. The schematics of this module have been included in Figure 12 below.

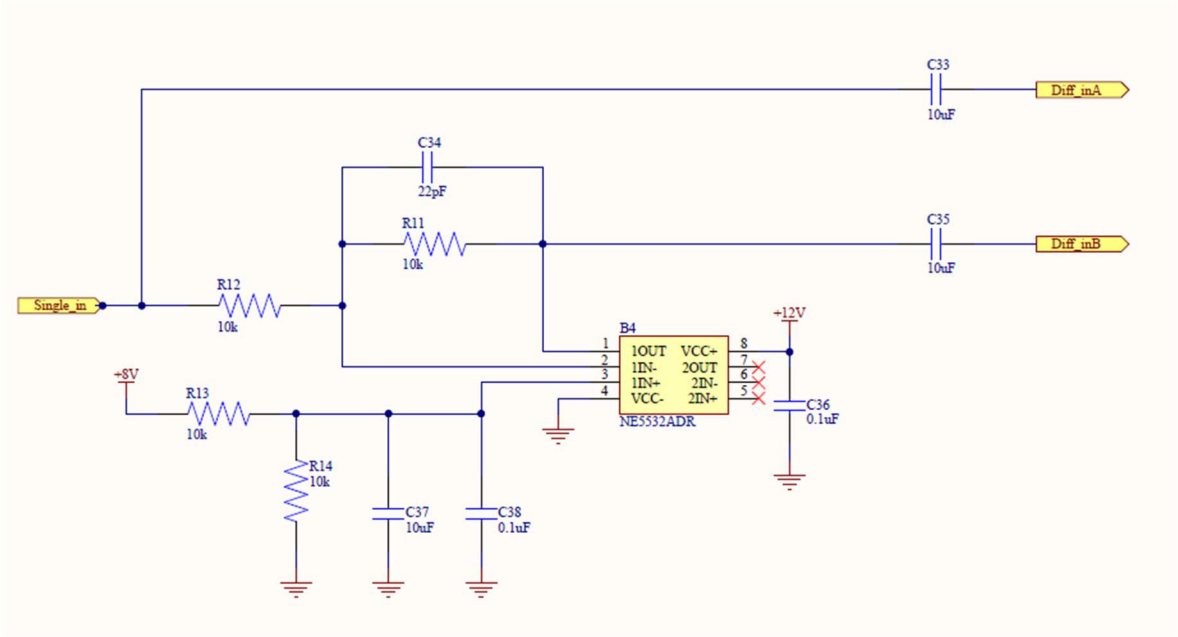

Figure 12: Differential signal module schematics

This subsystem uses a differential amplifier to generate the differential signal needed. Due to the lack of a dual power supply, the design of this amplifier had to be done as shown in Figure 12. This design uses an 8V reference voltage which is one of the inputs to a regular differential amplifier configuration. The single-ended signal is the other input to the differential amplifier configuration. This way, the main output of the amplifier is the exact opposite of the single-

ended input but with a DC offset. The DC offset was removed by using a DC blocking capacitor labeled as “C35” in Figure 12. This way the main outputs of this module are “Diff_inA” and “Diff_inB” which are the differential inputs into the TPA3255.

To ensure the right implementation, the design was first done and simulated using LT-Spice as shown in Figure 13.

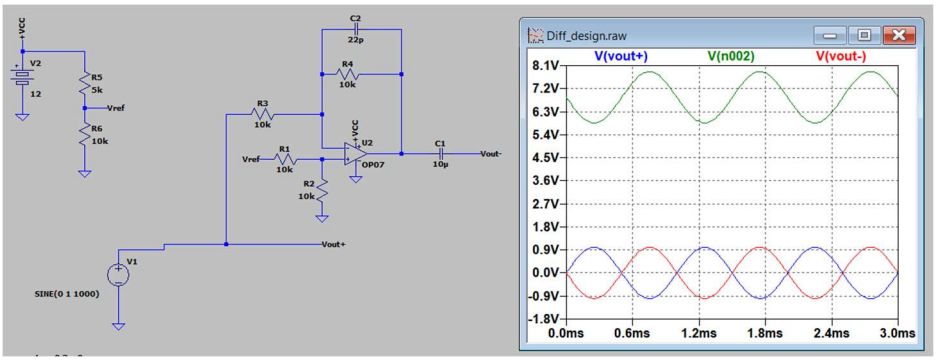

Figure 13: Differential Amplifier LTSpice

The waveforms in Figure 13 show the single-ended input signal in red, the output of the differential amplifier before the DC-blocking capacitor in green, and the final output signal in red. This shows how the outputs are differential with respect to each other. The design was then implemented into the schematics in Figure 12, using the NE5532ADR operational amplifier with additional decoupling capacitors.

Filter

The filter is an important module in the transmitter because the outputs of the H-bridge are high-frequency switching amplified signals. This means that a low-pass filter is required to filter out the high-frequency components and end up with a clean sinusoidal wave to be outputted into the load. The schematics for this module have been included in Figure 14 below.

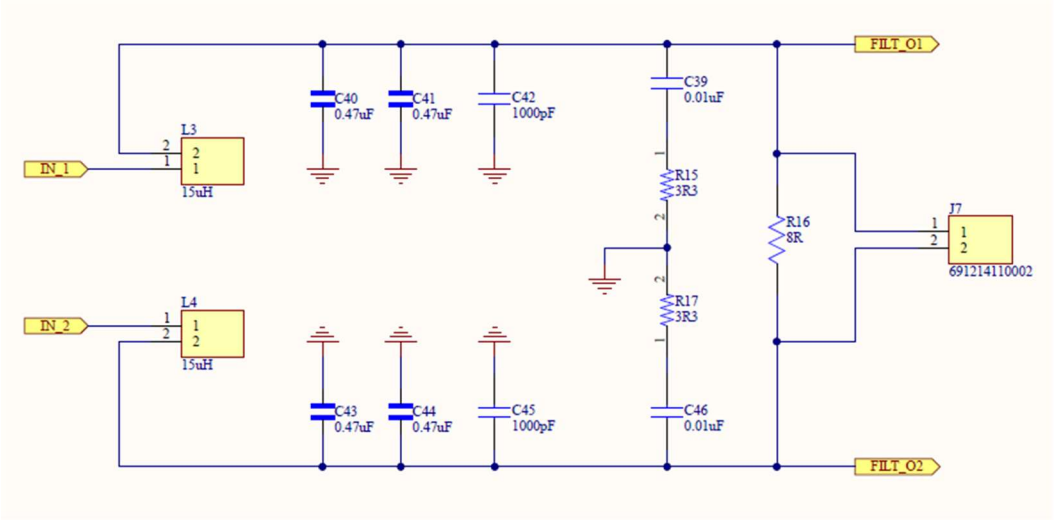

Figure 14: Low-pass filter schematics

As seen, the filter used is a second-order low-pass filter. The TPA3255 datasheet had a recommended filter design which is the one that was used for this PCB. However, because the load for this project has a coil and is not just a regular resistive load, some changes had to be made to the filter from the TPA3255 datasheet. For these changes, LT-Spice was used to simulate the frequency response of the filter as shown in Figure 15 below.

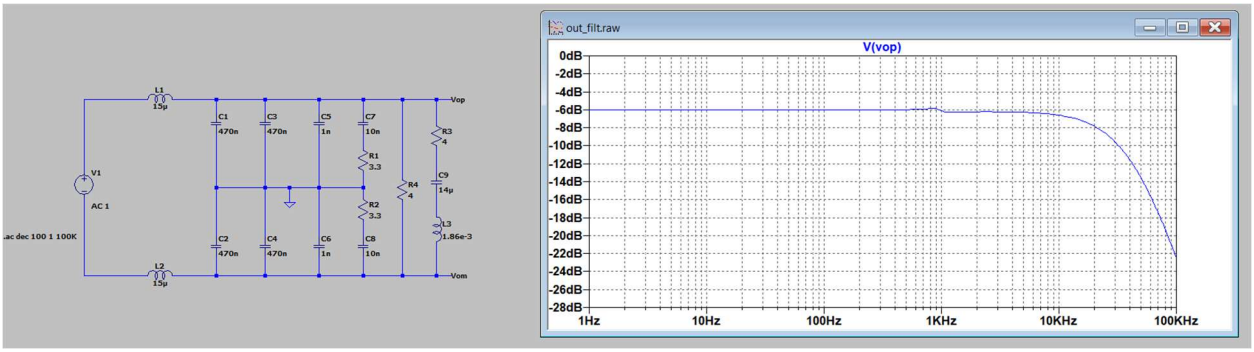

Figure 15: Filter Simulation

The values of the components were carefully reviewed until the desired frequency response was achieved. Furthermore, a shunt resistor—R16 in Figure 14 and R4 in Figure 15—was added as it was found that this greatly improved the frequency response.

After the desired frequency response was obtained through simulation, it was implemented into the schematics as shown in Figure 15.

Capacitor Bank

The capacitor bank is the module that allows the system to select the capacitor value that cancels the coil's reactance based on the frequency. The schematics for this system have been included in Figure 16 below.

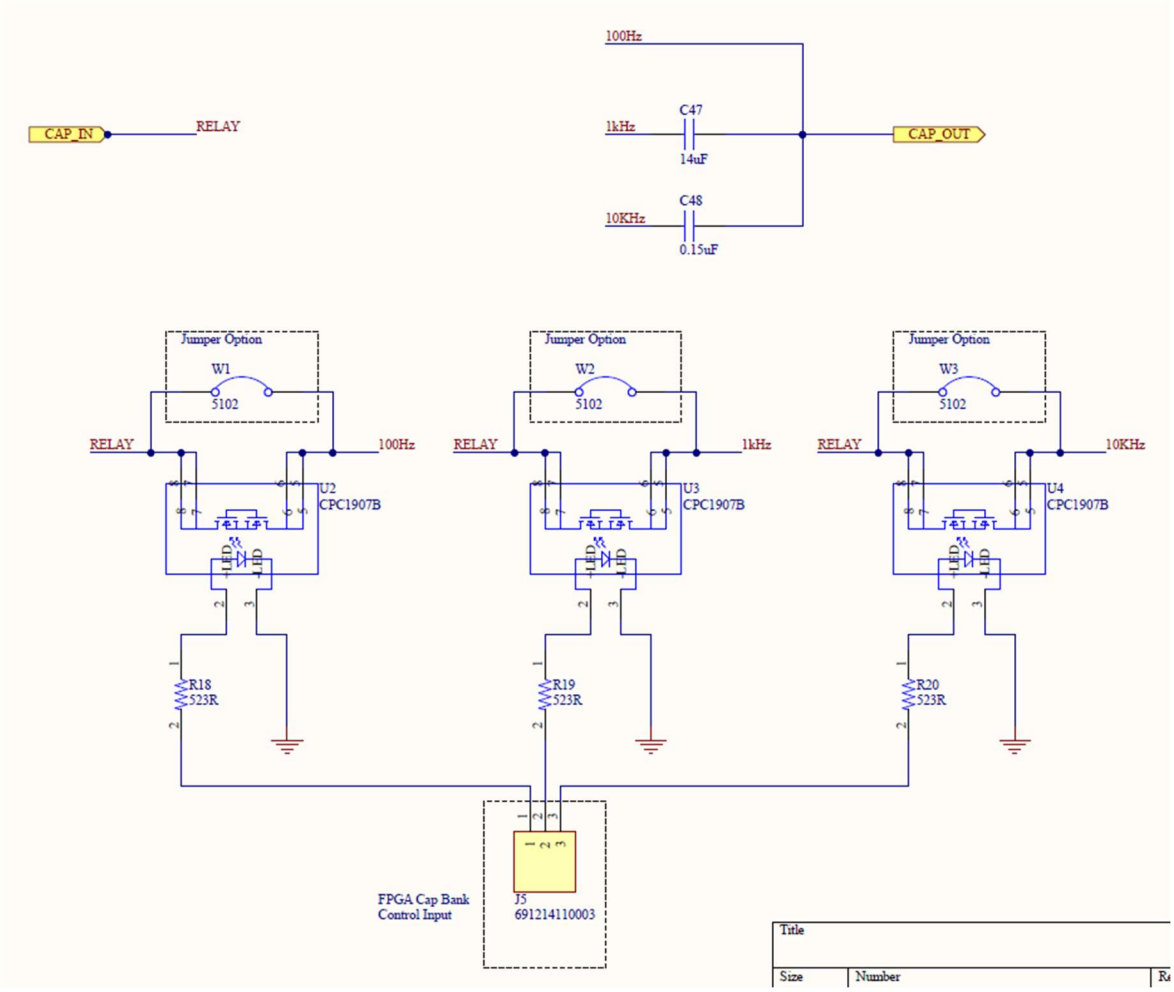

Figure 16: Capacitor Bank Schematics

For the capacitor bank, we chose to use solid-state relays as the switches because of their low series resistance. As these relays are connected in series with the load, it was crucial to not affect the load resistance as this would affect the power that reaches the load. The CPC1907B solid-state relays were used which only have a resistance of 0.06 ohms and were rated for the output power needs. The solid-state relays are controlled by a 3.3VDC signal from the FPGA that is connected to connector "J5" in Figure 16.

The initial design for the capacitor bank used three capacitors as shown in Figure 17 below.

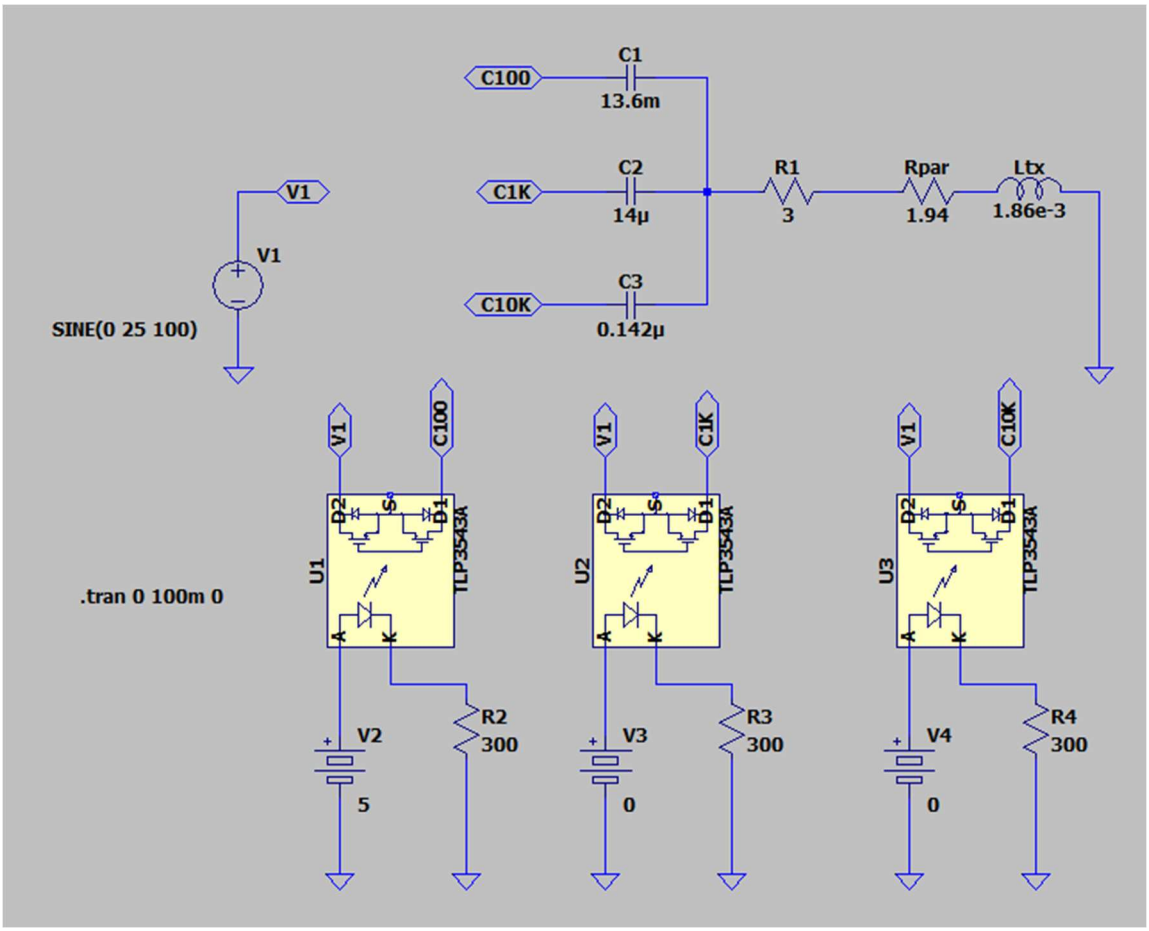

Figure 17: Capacitor bank initial design

However, in the actual PCB design, it was not possible to find a non-polarized capacitor with a capacitance value of 13.6mF that was rated for the power needs. After further consideration, it was concluded that because this capacitor was used to cancel the coil reactance at 100 Hz, this low frequency did not result in a reactive value that was considerably high. At 100 Hz, the coil only had a reactance of around 1 ohm, which could be ignored due to the inability to find a capacitor.

Transmitter PCB Layout

For the transmitter PCB layout design, the main objectives were placing the components strategically to ensure the correct operation and to ensure the PCB board was within the size constraints of the underwater enclosure it will be placed in. The client stated that the cylindrical enclosure has a diameter of 150mm and a length of 480mm. The PCB must fit within those values considering that the enclosure will also need to hold the FPGA and batteries. Therefore, it was important to make it as short as possible.

To begin, the TPA3255 datasheet was consulted as this has a section with PCB layout recommendations. This section provided key information about the placement of decoupling capacitors and the general guidelines about trace widths and grounding. After this, the datasheets of the other chips used were also consulted for similar purposes. With all the information in consideration, the PCB layout included in Appendix B was created. The traces in red are for the top layer and those in blue are for the bottom layer.

As seen in Appendix B the layout has a placement of parts that follows the path of the signal from inputs to the left to outputs at the right. Firstly, all the components were grouped together based on the schematics and function. This way, the low-power components which are part of the initial stages of the signal like the differential amplifier were placed in the left end of the PCB. This way, these components were isolated from the higher power signals at the right which can cause noise and distortion. Then, the TPA3255 was placed followed by the higher power components like the filters and capacitor bank at the right of the PCB. All the connectors were placed at the edges of the PCB to facilitate the connections.

After the components were physically placed, the traces were created. For this, a trace width calculator was used to ensure the traces had a width that could handle the amount of current going through them. All these traces can be seen in Appendix B.

Then, the silkscreen layer was created which has all the descriptive text in the PCB. It was important to place the component identifiers appropriately and the descriptive text for connectors, clearly indicating the polarities. Finally, through holes were placed for the placement of the TPA3255 heatsink and the mounts. After completing the layout, a two-layer PCB was created with a final size of the PCB achieved was 130mm by 160mm.

Transmitter PCB Manufacturing

After completing the PCB design for the transmitter PCB, the final product was obtained. A digital view of the PCB has been included in Appendix C as a reference.

Once the design was done, the manufacturing files were obtained. This includes the Gerber and drill files. The manufacturer chosen was JLC PCB because it was recommended to us. A 1.6mm thick PCB with 1oz copper thickness was ordered.

Finally, the components were ordered from Digikey and Mouser for the PCB assembly. The Bill of Materials has been included in Appendix D as a reference.

Results

As of the submission of the report, simulation results are available for the systems within the transmitter PCB. The TPA3255 chip has been validated within simulation by using a sister chip in the series of TPA3 chips. As well, the corresponding low pass filter was validated within simulation. The solid-state relay was testing in both simulation and lab tests.

To validate the TPA chip we used Tina TI software. From the technical requirements, we aimed to input an analog signal into the chip and receive an amplified PWM signal at the output. The figure below shows the output results for the input of a 1V analog signal.

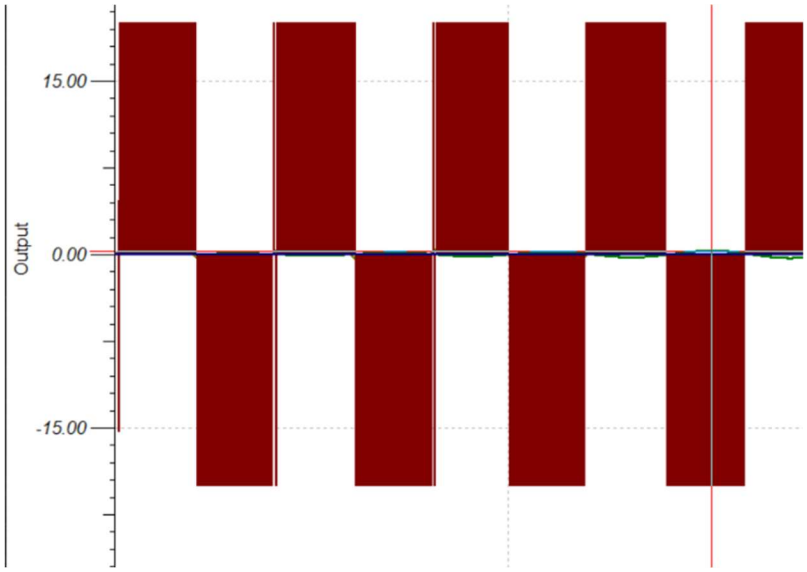

Figure 18: PWM Amplifier Output

It is important to note that although the sine wave appears in the form of blocks, the sine wave is encoded in a high frequency PWM. Investigating further into the output, we can observe the individual changing duty cycles of the PWM output in the figure below.

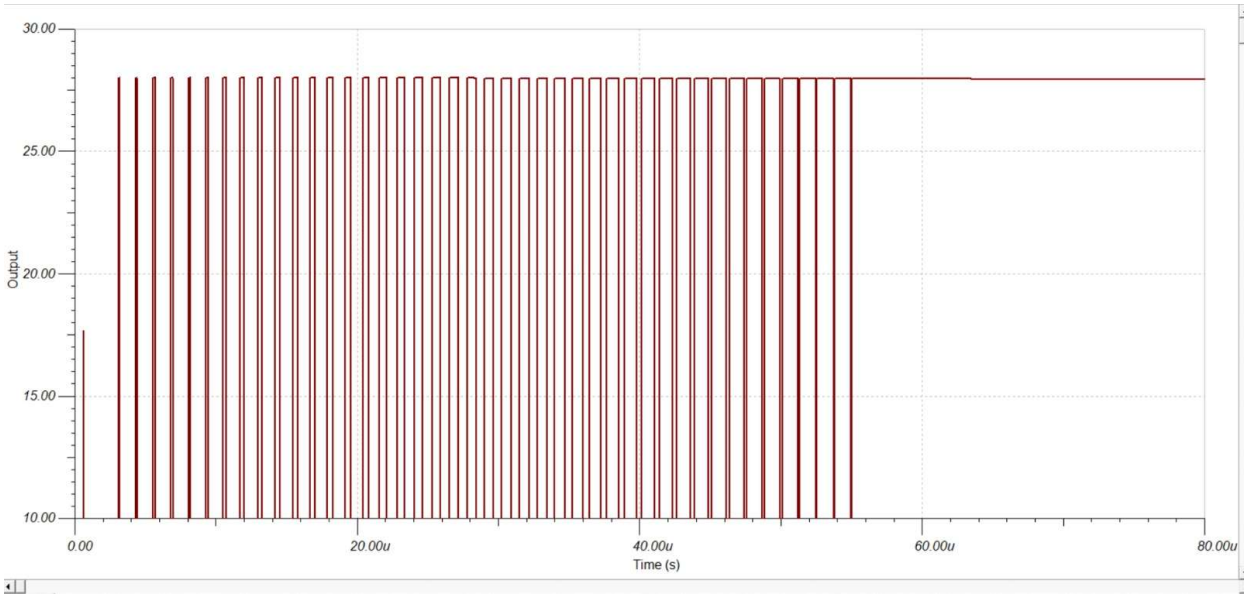

Figure 19: Changing Duty Cycle of PWM Output

Observing the changing duty cycle validates the output of the PWM and is a significant result in the project.

The next result we obtained was the output filter frequency diagram. This showed us the response of the output filters amplification to different input frequencies. An ideal low pass filter would have a straight cut off. In our project we used a 2nd order filter, garnering a cutoff response of 40dB per decade.

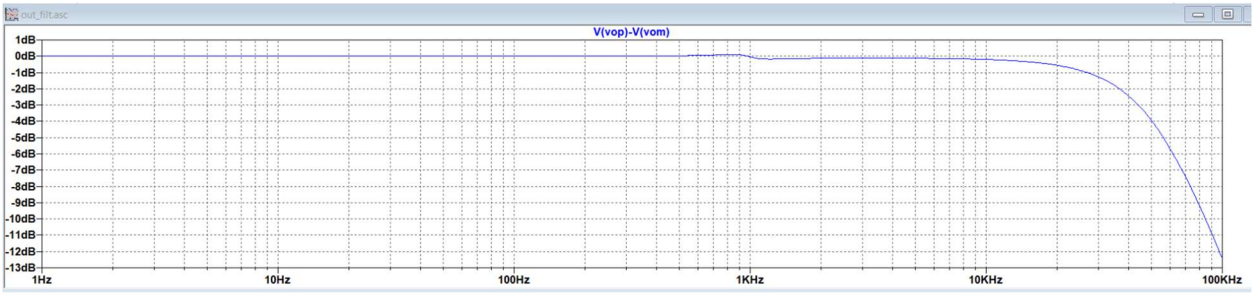

Figure 20: Low Pass Filter Frequency Plot

The output from the filter also allows for full power for each frequency we are aiming to output, 100Hz, 1kHz, and 10kHz. The 3dB cutoff, which is a common statistic to determine what signals won't be present in the output is 30kHz.

Finally, we can observe the results from the entire Transmitter PCB being simulated in the figure below.

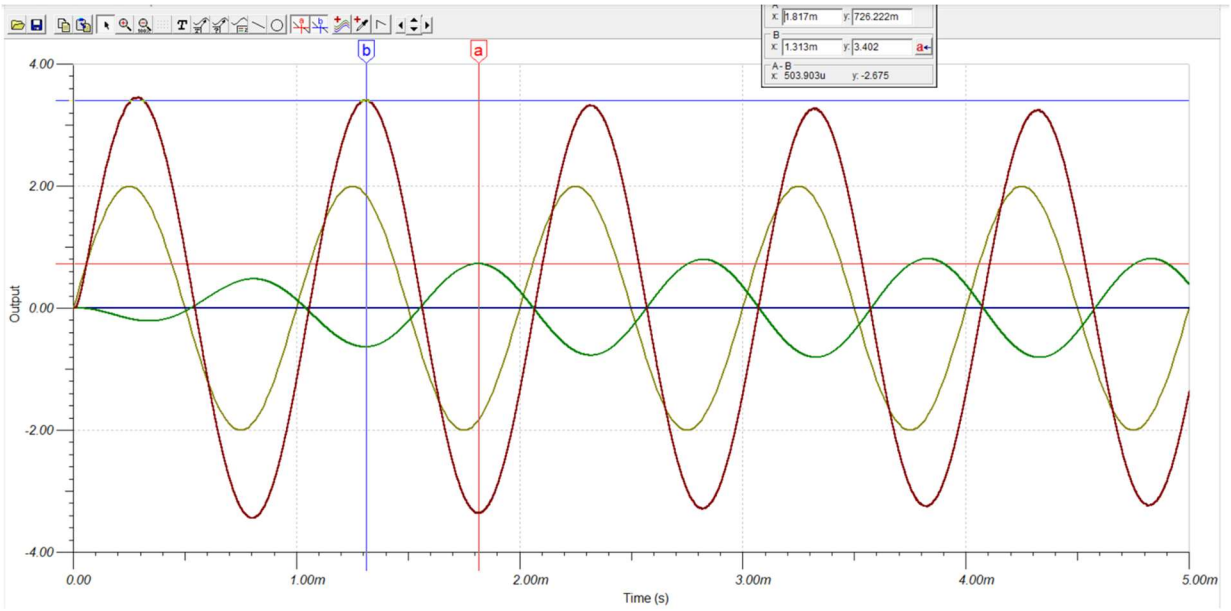

Figure 21: Filtered Output Voltage & Current Across Inductor

In the figure above, the yellow/green line is the analog input voltage, this is the small analog signal that determines the frequency that the system will produce. The red line is the amplified voltage, after being smoothed out by the low pass filter. We can observe that there is no harmonic distortion influencing the wave, proving that the outcome of the low pass filter is smoothing out our low frequency signal. Lastly, the green line is the observed current through the inductor. This current follows Ohm's Law and validates in simulation that the inductor should receive the full current.

The last validation was of the solid-state relay (SSR). The simulation results were inconclusive as if the SSR would be able to stop the higher resonant frequencies from passing through. To test this, we wanted to observe the stopping power of the solid-state relay at a high frequency in the laboratory. Five volts at 10kHz was pushed through the SSR in the off state to observe how much noise was going through. The oscilloscope results are shown below.

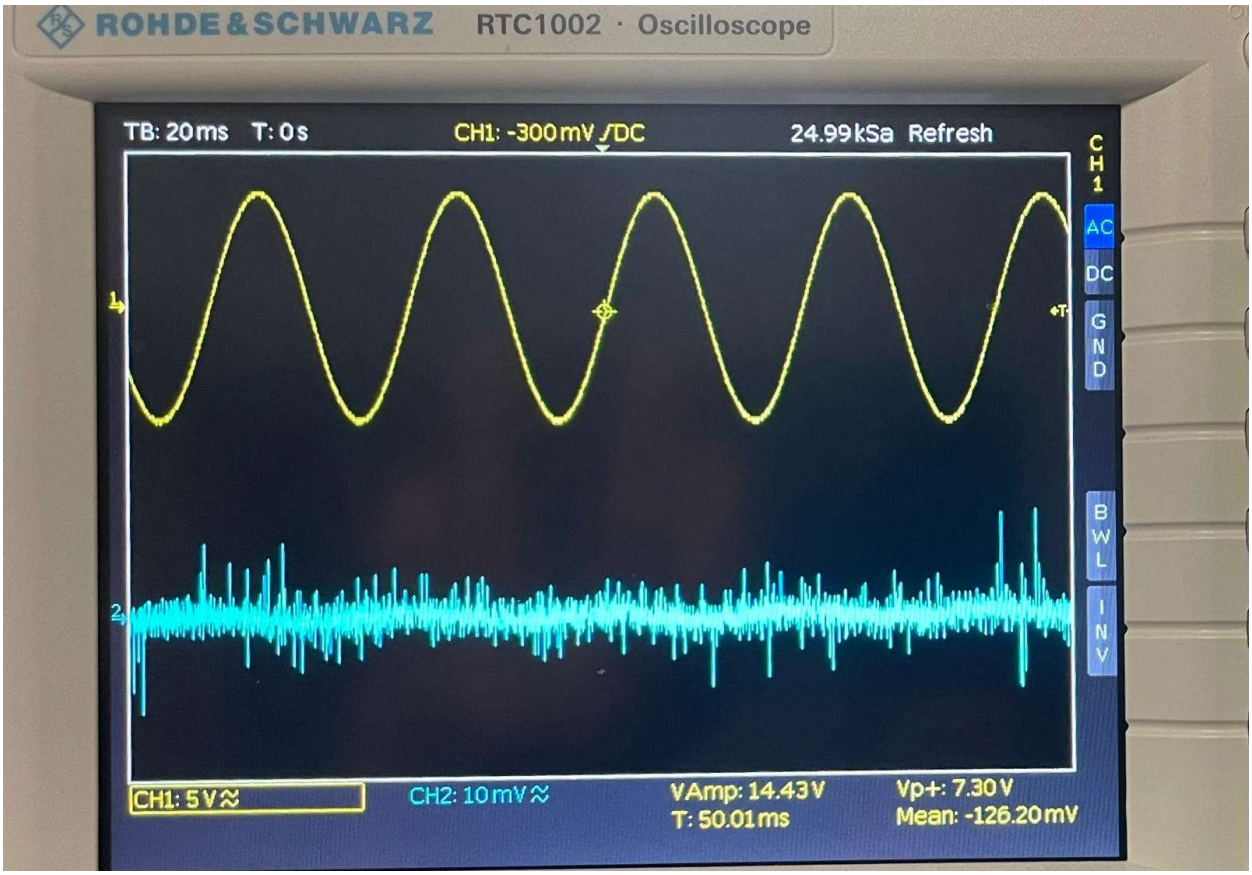

Figure 22: SSR Oscilloscope Reading

We can observe the input signal (yellow) being a five-volt 10kHz input signal. The blue output wave was observed over a resistor in series to ground from the output of the SSR. The scale is different and calculating the signal to noise ratio (SNR).

$$SNR = 20\log\left(\frac{signal}{noise}\right) = 20\log\left(\frac{5\,V}{10mV}\right) = 53.98dB$$

A SNR of 53.98 dB is impressive, for reference a high-end audio system has a dB above 60dB. This boasts an impressive performance from the SSR chip and validated it for use in the amplifier.

Testing

At the time of writing this report, the PCB was undergoing assembly, and no physical testing has been completed. From the Results section above, the board is expected to behave correctly and

meet design expectations. This section details how the system will be tested once it is fully assembled and integrated.

The first subsystem to be tested is the PCB. During assembly all connections should be checked by the manufacturer; however, it is crucial to recheck them especially when using a current of 5A. THD will be measured to confirm that the PCB does not introduce any unwanted harmonics to the signal before it is sent through the transmitter coil. The input current can be evaluated by placing an oscilloscope in series with the signal generator or FPGA to determine the cleanliness of the signal is before it is amplified. On the high current side of the PCB, the oscilloscope should only measure voltage to avoid damaging the equipment. The resistor in parallel with the transmitter coil should also be measured and the signals can then be compared to determine the system's THD.

Testing the FPGA is more theoretical than the PCB test, as the FPGA will not be completed for this project. If it were completed, a test would involve measuring the output and performing an FFT to confirm that the output has minimal harmonics. Reducing the harmonics has two purposes: to minimize the power loss when transmitting and to ensure a clearer signal for the receiver. Additionally, a test should confirm that the correct capacitor, and only the correct capacitor, is connected when each harmonic is generated.

When testing the completed transmitter system, the focus will be on efficiency. There are two resistors on the high-current side of the Transmitter PCB as shown in Figure 15 as R3 and R4. R3 is in series with the transmitter coil and capacitor bank. R4 is in parallel with R3, the transmitter coil, and the capacitor bank. From voltage measurements across both resistors, the amount of current reaching the transmitter coil can be found and the efficiency of the system can be calculated.

To test if the signal is transmitted from the transmitter coil to the receiver coil, the system will be tested in two ways. The first test involves transmitting through air by the UW-Stream lab with a five-meter distance between the transmitter and receiver. The output from the receiver amplifier will be measured with an oscilloscope to assess the noise added from the channel and the amplitude received. If this test is successful, the team plans to conduct additional testing at Dalhousie's Aquatron. Testing at the Aquatron will involve submerging the transmitter underwater with five meters between the transmitter and receiver. The test in water will help

illustrate the different attenuation distances for the frequencies when compared with each other and when compared with the amplitude received in the dry tests.

Discussion

As shown in Table 3 in the Technical Requirements section of this report, there were five main requirements that this project was supposed to meet. This section evaluates whether each of these requirements was fulfilled and discusses potential design changes to address unmet objectives.

The first technical requirement was to code an FPGA to be a signal generator. It was required that the signal generator create three frequencies of sine waves, 100Hz, 1kHz, and 10kHz. This requirement was not met. To meet this requirement, IP cores for user interface and sine wave generation must be integrated together. These cores already exist, but the output control for capacitors would also need to be developed and integrated with the user interface. For the purposes of testing the rest of the system, a signal generator from UW-Stream's lab will be used.

The second technical requirement was achieving 125 watts of power dissipation through the amplifier load. This requirement is expected to be met when the integrated system is tested. The PCB and power supply were designed to handle more than this amount of power and demonstrated the ability to deliver it to the load in simulation. However, the efficiency of the system is reduced by the resistor in parallel with the load (R4 in Figure 15). This resistor helps reduce noise, resulting in a much cleaner output, but it also diverts a significant portion of the current output from the filter. In simulation, R4 reduced system efficiency by more than 40%.

The third technical requirement was limiting the impedance of the load to 5 ohms. This was achieved by placing capacitors in series with the inductive load. For frequencies of 1kHz and 10kHz, different capacitors are added to the circuit when each frequency was sent through the coil. These capacitors kept the impedance below 5 ohms. For the 100Hz signal, a capacitor was not included due to sourcing and size limitations. Simulations showed that this omission had minimal impact because 100Hz generates relatively low reactance.

The fourth technical requirement was ensuring THD of less than 5%. This was met in simulation for the amplifier. However, physical testing may reveal additional factors that could increase distortion. These include distortion caused by the physical PCB and the leads connecting to the

load. The team anticipated these distortions to be minor and that the inductive load will filter out the highest frequencies, preventing them from being transmitted. The solid-state relay was tested physically, and the noise it introduced to the signal was minimal, as shown in Figure 22.

The fifth and final technical requirement was that the PCB fit within a cylinder with a diameter of 150mm and a length of 480mm. This requirement was met. Appendix C: Transmitter PCB shows the layout of the PCB. Larger components were placed closer to the center of the cylinder as to comply with this requirement.

Conclusion & Recommendations

This project worked on creating a transmitter for underwater to above water communication using magnetic induction. The project aimed to use an FPGA to create an analog sine wave. This sine wave was then to be amplified using pulse width modulation and an H-Bridge to 25 Volts at 5 Amps. This power was then to be delivered to the load.

The FPGA did not conclude with a resulting analog input wave; however, this will be mitigated for testing by using the combination of a signal generator and voltage supplies to the capacitor bank. The transmitter PCB was designed. Housed on the PCB is the TPA3255 chip, which modulates the input signal and controls the H-Bridge to output an amplified PWM wave. This wave was then put through a low pass filter on the PCB suppling 125 Watts of power to the output pins. The load, a new larger wire induction coil is connected to these output pins of the PCB.

The PCB board was simulated in full, yielding promising results to the extent that the client went ahead with approving a PCB to be printed. This PCB is currently in the manufacturing process and will be validated by December 18th. The project was under budget by $440.

In the next iteration of the project, we would make one major design revision. The low pass filter included a resistor in parallel to the load to achieve the desired response. In the next iteration we would re-design the low pass filter to not include this passive component.

This project aims to connect the clients underwater monitoring device with the surface, where methods such as a physical connection are not possible. The Project concludes with a physically

implemented design that is to be tested and validated to use magnetic induction to transmit sine waves through water, ice, and air.

We are grateful for advice from our internal supervisor, Dr. Jacek Ilow, whose technical advice aided in our validation and testing. We would like to extend our gratitude to our client and mentor Dr. Jean Francois-Bousquet, whose guidance provided a strong conceptual foundation to the project.

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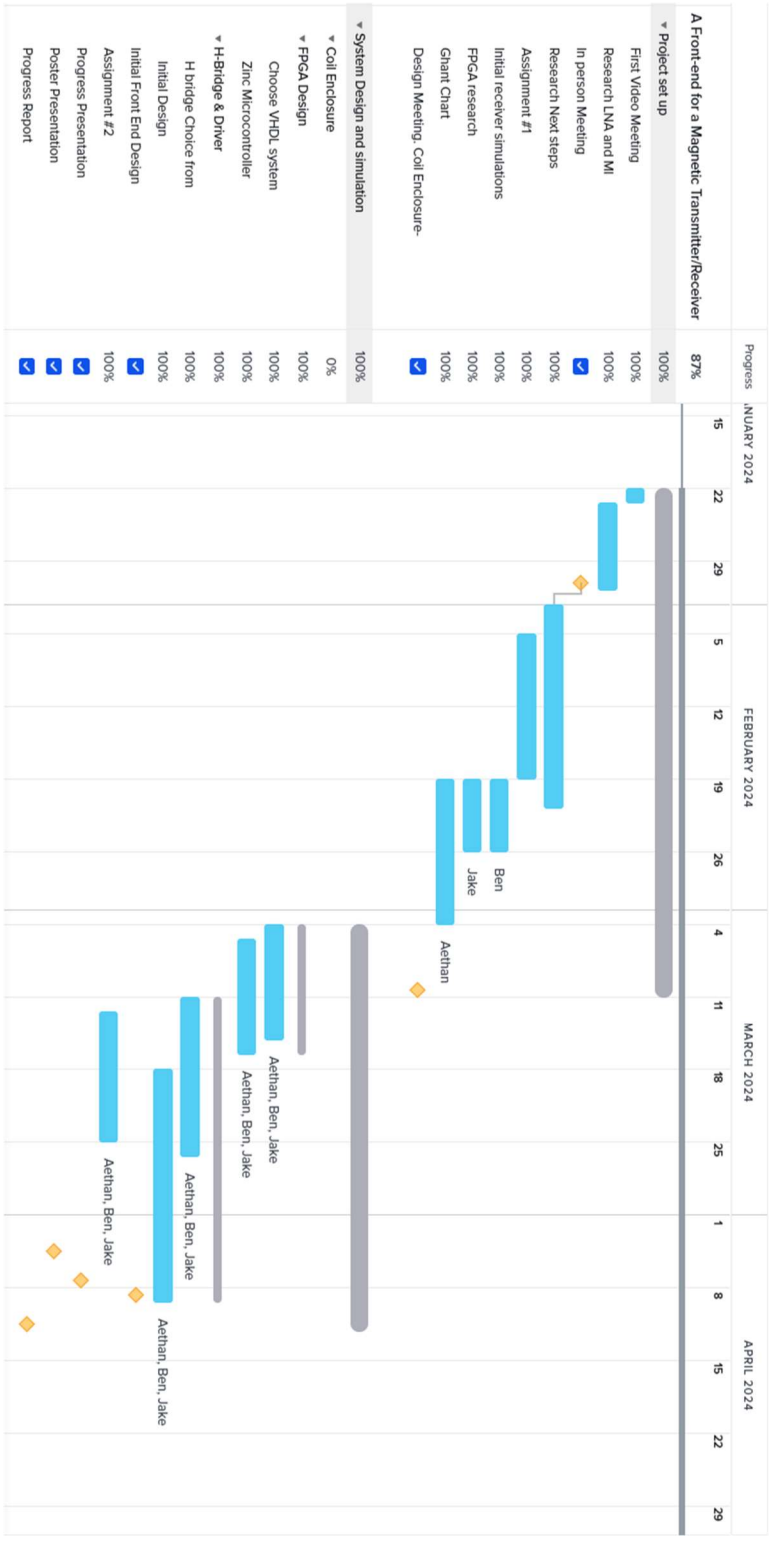
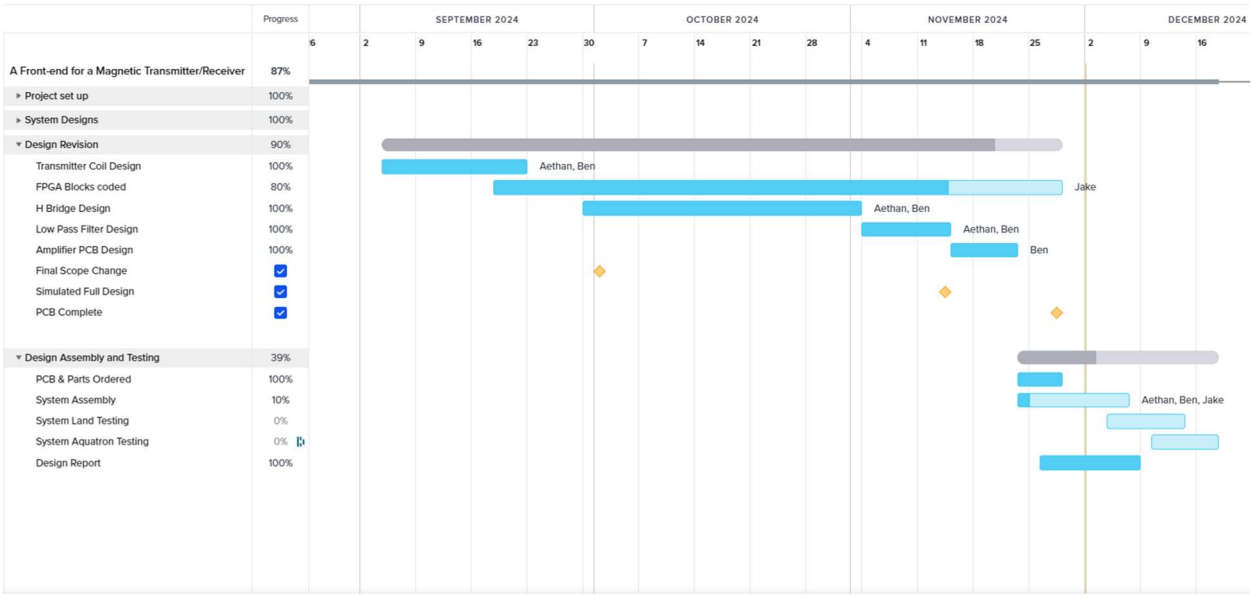
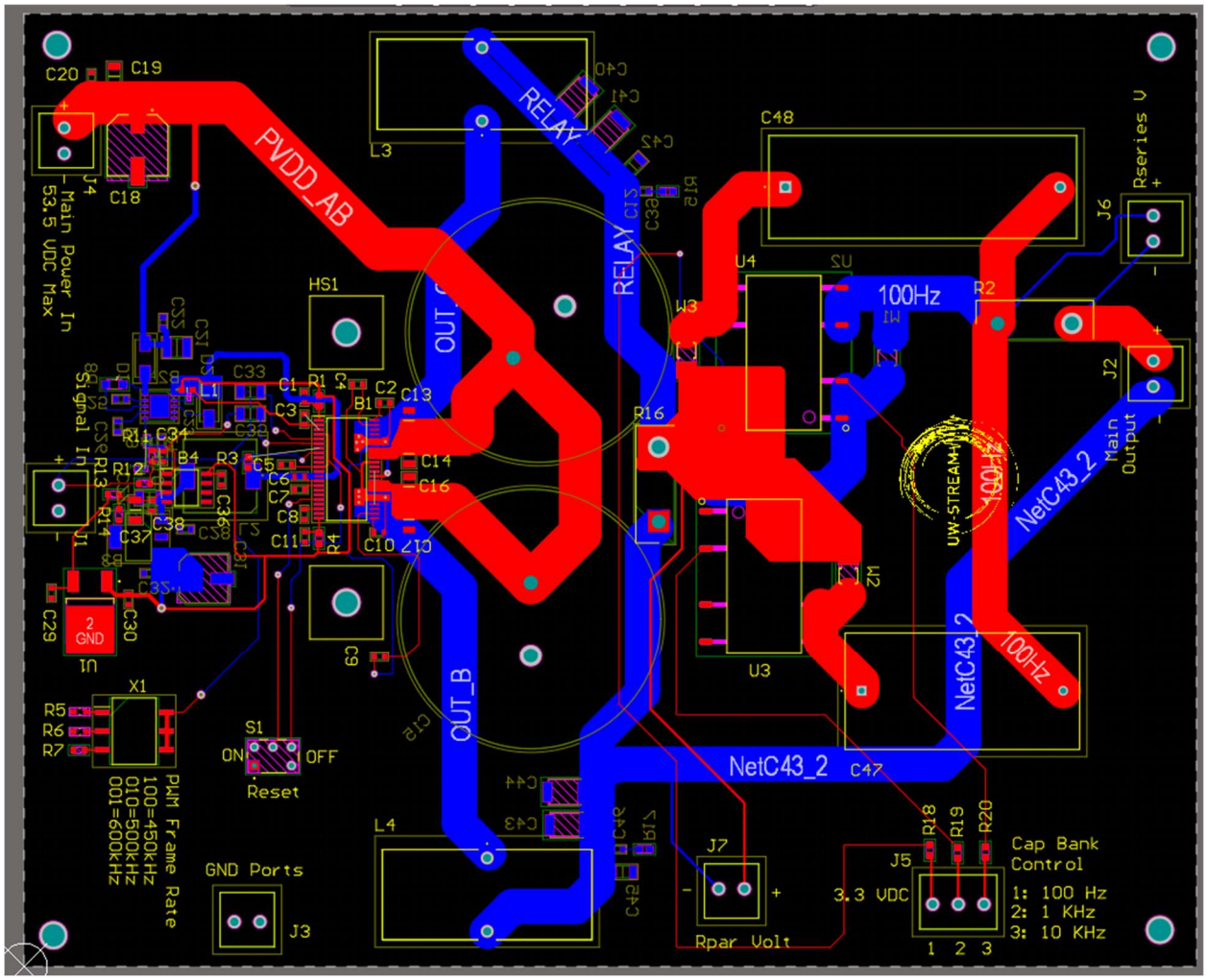
Appendices

Appendix A: Gantt chart



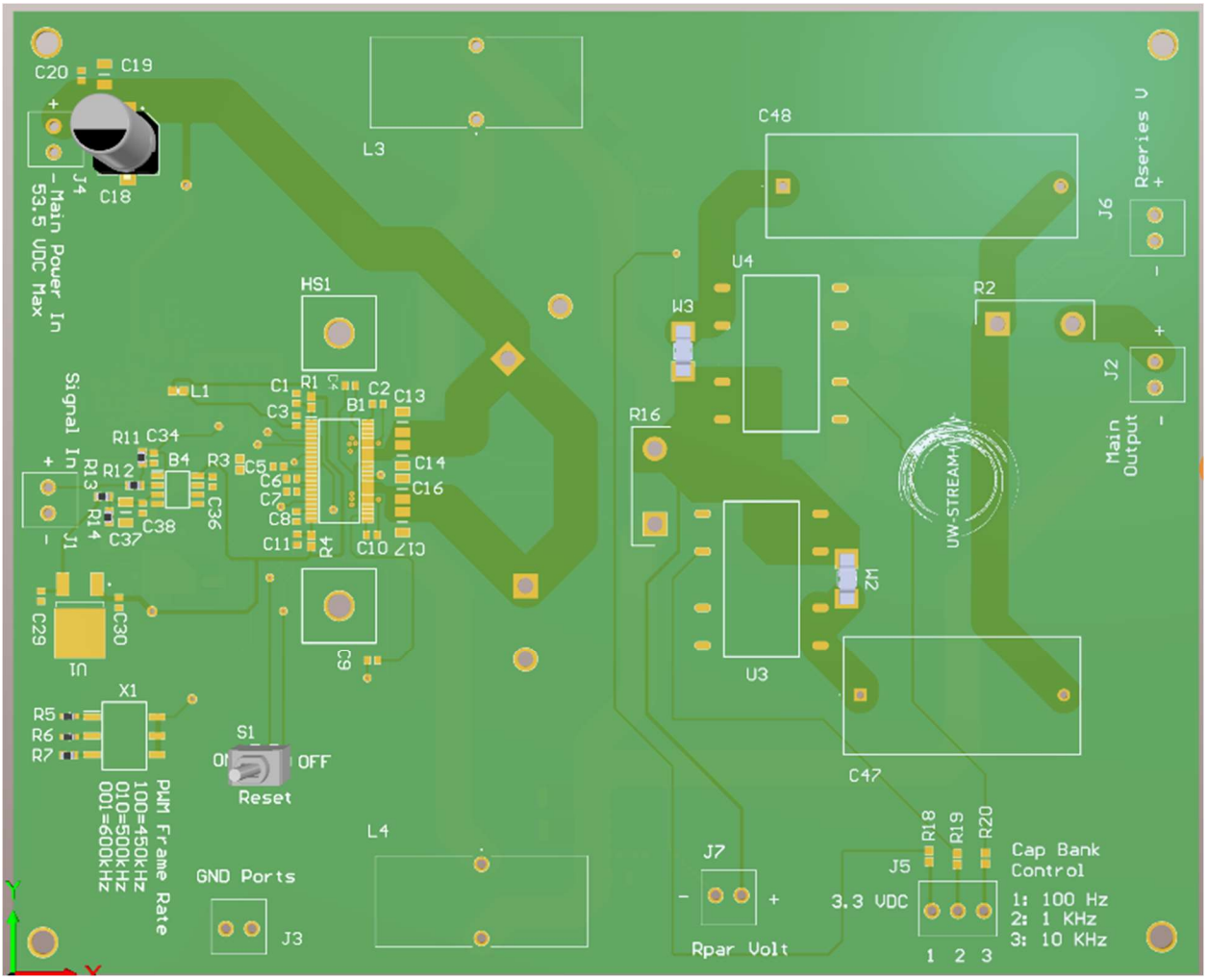

Progress
SEPTEMBER 2024
OCTOBER 2024
NOVEMBER 2024
DECEMBER 2024
6
2
9
16
23
30
7
14
21
28
4
11
18
25
2
9
16
A Front-end for a Magnetic Transmitter/Receiver
87%
Project set up
100%
System Designs
100%
Design Revision
90%
Transmitter Coil Design
100%
Aethan, Ben
FPGA Blocks coded
80%
Jake
H Bridge Design
100%
Aethan, Ben
Low Pass Filter Design
100%
Aethan, Ben
Amplifier PCB Design
100%
Ben
Final Scope Change
Simulated Full Design
PCB Complete
Design Assembly and Testing
39%
PCB & Parts Ordered
100%
System Assembly
10%
Aethan, Ben, Jake
System Land Testing
0%
System Aquatron Testing
0%
Design Report
100%

Appendix B: Transmitter PCB Layout

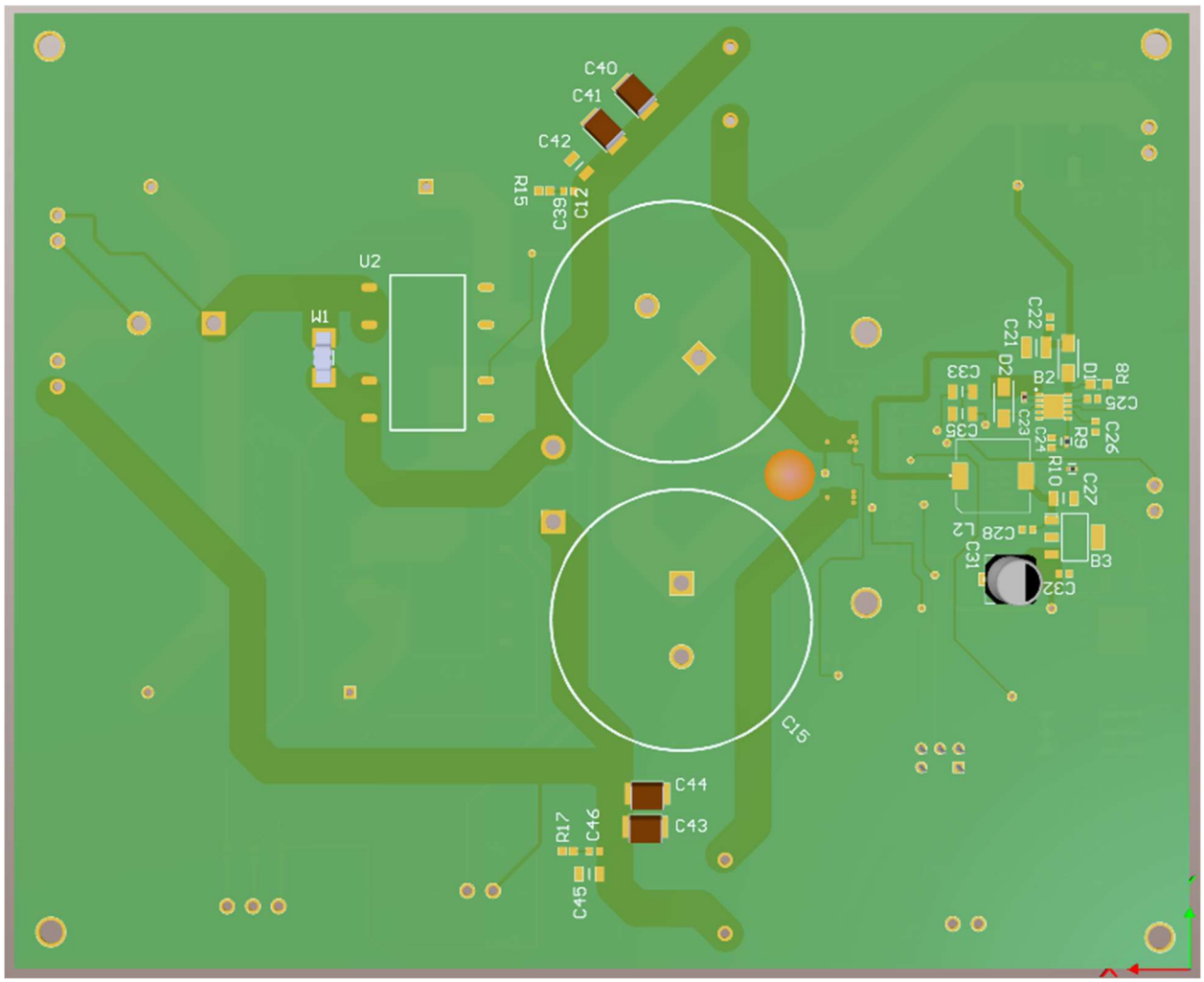


Appendix C: Transmitter PCB

Top Side



Bottom Side


C40
C41
C42
R15
C39
C12
U2
W1
C22
C21
D2
C33
B2
D1
R8
C25
C35
C23
C24
R9
C26
R10
C27
C28
L2
C31
B3
C32
C15
C44
C43
R17
C46
C45

Appendix D: Transmitter PCB BOM

Name	Description	Designator	Quantity	Manufacturer 1	Manufacturer Part Number 1
TPA3255DDV	Audio Amplifiers 325-W Stereo High-Performance, High-Definition, Class-D Amplifier 44-HTSSOP 0 to 70	B1	1	Texas Instruments	TPA3255DDV
LM5010ASD_NOPB	Texas Instruments LM5010ASD/NOPB, Step Down DC-DC Converter, 1A, Adjustable, 2.5 70 V, 10-Pin LLP	B2	1	Texas Instruments	LM5010ASD/NOPB
LM2940IMP-12_NOPB	LDO Regulator Positive 12V 1A SOT223 Texas Instruments LM2940IMP-12/NOPB, LDO Voltage Regulator, 1A, 12 V, Maximum of 26 Vin, 4-Pin SOT-223	B3	1	Texas Instruments	LM2940IMP-12/NOPB
NE5532ADR	NE5532ADR, Dual Operational Amplifier 10MHz, 8-Pin SOIC	B4	1	Texas Instruments	NE5532DR
0.1uF	CAP CER 0.1UF 50V X7R 0603	C1, C3, C11, C25, C29, C32, C36, C38	8	Kemet	C0603C104K5RACTU
0.033uF	0.033 µF ±10% 25V Ceramic Capacitor X7R 0603 (1608 Metric)	C2, C4, C9, C10	4	Murata	GCD188R71E333KA01D
1uF	Murata 1uF Multilayer Ceramic Capacitor MLCC 16V dc +/-10% X7R Dielectric 0603 (1608M) SMD, Max Temp. +125C	C5, C6, C8	3	Murata	GCM188R71C105KA64D
47nF	Cap Ceramic 0.047uF 50V X7R 10% Pad SMD 0603 125C Automotive T/R	C7	1	Murata	GCM188R71H473KA55D
4700uF	Cornell-Dubilier 4700uF 80 V dc Aluminium Capacitor H3, SLPX Series 1000 (Shelf) h, 3000 (Endurance) h 35 x 30mm	C12, C15	2	Cornell	SLPX472M080H3P3
1uF	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1206 1uF 100volts X7R 10%	C13, C14, C16, C17, C19	5	Murata	GRM31CR72A105KA01L
47uF	47ÂµF 63V Aluminum Electrolytic Capacitors Radial, Can - SMD 2000 Hrs @ 105Â°C	C18	1	Panasonic	EEE-FK1J470P
0.01uF	CAP, CERM, 0.01 µF, 100 V, +/- 10%, X7R, 0603	C20, C39, C46	3	Kyocera	KGM15AR72A103KT
2.2uF	Samsung Electro-Mechanics 2.2uF Multilayer Ceramic Capacitor MLCC 100V dc +/-10% X7R Dielectric 1210 (3225M) SMD	C21	1	Samsung	CL32B225KCJSNNE
0.1uF	CAP CER 0.1UF 100V X7R 0603	C22	1	Murata	GRM188R72A104KA35J
47000pF	SMD capacitor X7R (BA) with capacitance 47000pF Tol. 10%. Rated voltage 25Vdc 125C	C23	1	Murata	GRM155R71E473KA88D
5600pF	5600 pF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C24	1	Murata	GCD188R71H562KA01D
4700pF	CAP CER 4700PF 50V X7R 0603	C26	1	Kemet	C0603X472K5RACTU
4.7uF	CAP CER 4.7UF 50V X7R 1206	C27	1	Murata	GRM31CR71H475KA12L
0.47uF	CAP CER 0.47UF 25V X7R 0603	C28	1	Murata	GRM188R71E474KA12D
0.33uF	CAP CER 0.33UF 16V X7R 0603	C30	1	Murata	GCM188R71C334KA37D
47uF	47ÂµF 16V Aluminum Electrolytic Capacitors Radial, Can - SMD 2000 Hrs @ 105Â°C	C31	1	Panasonic	EEE-FK1C470P
10uF	CAP CER 10UF 50V X7R 1206	C33, C35, C37	3	Samsung	CL31B106KBHNNNE
22pF	CAP CER 22PF 50V C0G/NP0 0603	C34	1	Murata	GRM1885C1H220JA01D
0.47uF	C Series 1812 0.47 uF 250 VÂ±10 % Tolerance X7R SMT Multilayer Ceramic Capacitor	C40, C41, C43, C44	4	TDK	C4532X7R2E474K230KA
1000pF	AVX 1nF /-5% 100 V dc C0G Dielectric SMD Ceramic Multilayer Capacitor 1206	C42, C45	2	Kyocera	12061A102JAT2A
14uF	C4AQHM, Film, Metallized Polypropylene, Automotive DC Link, 14 uF, 10%, 500 VDC, 105C, -55C, 85C, 2.1 GOhms, 65 V/us, 25 nH, 23.2 g, 32mm, 30mm, 16mm, Lead Spacing = 27.5mm, 88	C47	1	Kemet	C4AQLBU5140M18K
0.15uF	Metallized Polypropylene Capacitors (MKP/MFP), 0.15uF, 1000VDC, 14mm(W)x25mm(H)x42mm(L)	C48	1	Epcos	B32686A0154K000
3A	Schottky Diodes & Rectifiers 3A, 100V, SMA AEC-Q101 Qualified	D1	1	Vishay	V3SA310SHM3_A/H
1A	DIODES INC. - B1100-13-F - DIODE, REC, SCHOTTKY, 100V, 1A, SMA	D2	1	Diodes Incorporated	B1100-13-F
ATS-TI1OP-519-C1-R3	HEATSINK TI TAS5622 AND TAS5624	HS1	1	Advanced Thermal Solutions	ATS-TI1OP-519-C1-R3
691214110002	3.5MM HORIZONTAL ENTRY MODULAR WITH RISING CAGE CLAMP - WR-TBL, 2 pos	J1, J2, J3, J4, J5, J7	6	Wurth Elektronik	691214110002
691214110003	WR-TBL Terminal block - serie 2141	J5	1	Wurth	691214110003
10uH	TAIYO YUDEN - LBMF1608T100K - INDUCTOR, 10UH, 10%, FULL REEL	L1	1	Taiyo	LBMF1608T100K
100uH 1.5A	Wurth WE-PD Series Shielded Wire-wound SMD Inductor 100 uH +/-20% 1.5A Idc	L2	1	Wurth Elektronik	7447714101
15uH	Fixed Inductors 15uH UnShld 1% 14.2A 31mOhms	L3, L4	2	Coilcraft	PA6331-AE
3R3	RES 3.3 OHM 5% 1/8W 0603	R1, R4, R15, R17	4	KOA	RK73B1JTTD3R3J
2R	Caddock 2 100W Power Film Resistor +/-1% -20 +80ppm/C MP9100-2.00-1%	R2	1	Caddock	MP9100-2.00-1%
22k	22 kOhms Â±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	R3	1	Yageo	RC0603FR-0722KL
30k	RES 30K OHM 1% 1/10W 0603	R5	1	Yageo	RC0603FR-0730KL
20k	RES 20K OHM 1% 1/10W 0603	R6	1	Yageo	RC0603FR-0720KL
10k	10 kOhms Â±1% 0.333W, 1/3W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Pulse Withstanding Thick Film	R7, R11, R12, R13, R14	5	Vishay	CRCW0603 10K0FKEA
183k	RES SMD 182K OHM 1% 1/8W 0805	R8	1	Panasonic	ERJ-6ENF1823V
4.99k	RES Thick Film, 4.99kΩ, 1%, 0.063W, 100ppm/°C, 0402	R9	1	Vishay	CRCW04024K99FKED
1k	RES SMD 1K OHM 1% 1/16W 0402	R10	1	Vishay	CRCW04021K00FKED
8R	Caddock MP900 Series TO-247 Solder Thick Film Resistor 8 1% 100W -20 +80ppm/C	R16	1	Caddock	MP9100-8.00-1%
523R	Thin Film Resistors - SMD 0603 523ohms 25ppm 0.5% AEC-Q200	R18, R19, R20	3	Panasonic	ERA-3AEB5230V
200USP1T1A1M2RE	SWITCH TOGGLE SPDT 0.4VA 20V	S1	1	Eswitch	200USP1T1A1M2RE
L78M08ABDT-TR	Linear Voltage Regulator IC 1 Output 500mA DPAK	U1	1	STM	L78M08ABDT-TR
CPC1907B	Solid State SPST-NO_1 Form A_8-SOP_0.400_ 10.16mm Width_	U2, U3, U4	3	Littelfuse	CPC1907B
5102	2 (1 x 2) Connecteur de dÃ©rivation de position non isolÃ©0,114 Â« Â» (2,90 mm) Argent	W1, W2, W3	3	Keystone	5102
219-3MST	DIP Switches / SIP Switches SPST 3 switch sections	X1	1	CTS	219-3MST