ECED 4460 Project Report

Low Noise Amplifier Design Using Planar TL Structures

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Submitted To:

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Objective

Our objective is to design a low-noise amplifier for a frequency of around 2.4GHz. This design is meant to be completed using a biasing network to bias the amplifying transistor. The second major component of the design is to use input and output matching networks to balance the impedances from the source and load into the amplifier. The outcome of this project will be a PCB board that will amplify a real RF signal.

Design Description

The low-noise amplifier in this project is meant to follow some design specifications and meet the targets summarized in Table 1.

Table 1: Required Amplifier Parameters

Parameter	Design Target
Frequency Range	2.35 to 2.45 GHz
Gain	> 14dB
Input Return Loss	< -8 dB
Output Return Loss	< -10 dB
Noise Figure *NF*	<= 0.8 dB
P_{1dB}	> 10 dBm
Output 3rd Order Intermodulation Product	> 20 dBm

As Table 1 shows, the amplifier needs to have a gain of at least 14 dB. Each of these targets has been taken into consideration in the final design by using the procedure learned in class. For this project the source, load, and characteristic impedance will be 50Ω.

The low-noise amplifier uses a SKY65050-372 n-channel transistor manufactured by SKYWORKS. The general block diagram of the system has been included in Figure 1 below.

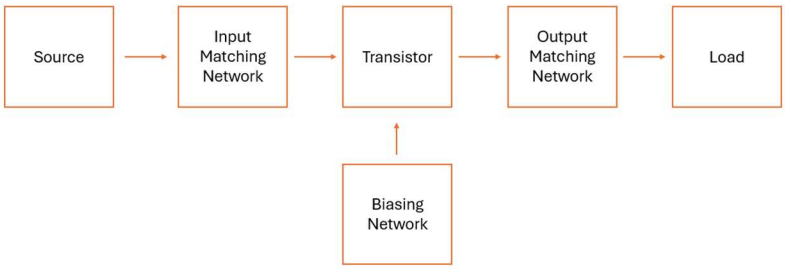


Figure 1: Amplifier Block Diagram

As seen in Figure 1, the transistor is the main component of the system as it is what generates the amplification. The source will generate the RF signal at 2.4GHz; the input matching network (IMN) then needs to convert the source impedance into a value that will result in the parameters being met. Similarly, the output matching network (OMN) will convert the load impedance into a desired value to meet the design target. Finally, the biasing network will be

designed to bias the transistor to its active region and to a desired drain-source voltage and current.

The circuit schematics which show the components of the amplifier more in detail have been included in Figure 2 below.

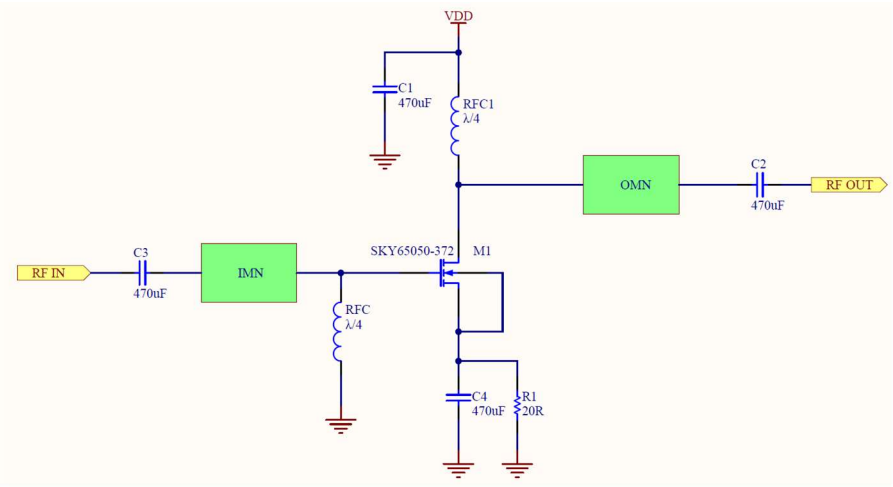


Figure 2: Amplifier Circuit Schematics

In the schematics above, the IMN, OMN, and RFC are replaced by microstrip transmission lines in the actual implementation.

The value of VDD for this system has to be 4.3V, this will ensure that the transistor is biased to the desired conditions. The function of the 20Ω resistor "R1" is to control the drain current into the desired value of 20mA. The function of the RFC is to let the DC current pass for biasing purposes while blocking the 2.4GHz RF signal. Finally, the capacitors have the function of decoupling, acting as AC ground, and blocking DC current.

For the design process, it was decided to aim for a target transducer gain of 18 dB. This was considered to be a good value as it was not in the lower limit, and it would result in an appropriate noise figure for the system.

ADS was used to aid in the design and optimization of the circuit. It was utilized to determine the exact biasing current of the transistor based on the transistor S parameters and biasing components.

Once the initial matching parameters were used, the IMN and OMN were added as microstrip lines to the design. The rest of the initial design that was in component form was redesigned into microstrip lines. The optimization goals were then set and the circuit was optimized.

Once the optimized circuit was created, the layout and symbol was created, following by adding a ground plane, vias, and lengths to add the input and output connector.

The symbol was then created into a Gerber file and sent into the technicians.

Procedures and Methodology

The design procedure started with the calculation of the unilateral figure of the transistor using the MATLAB code in Appendix A. The calculations revealed that a unilateral design was not possible which meant that another method had to be chosen. After consideration of the different available options, it was decided that the Available Power Gain method would be used as it allows one to choose a desired gain value and it does not have a unique solution. This means that this method allows the choice of the most convenient value for the impedances to be matched based on other design parameters.

To have an organized approach, the design flow chart learned in class was used to design the amplifier. To determine whether the transistor is unconditionally stable, the proper calculations were performed using the MATLAB code in Appendix A. The results were that it was not unconditionally stable, so the stability circles were calculated and plotted. Then, the noise considerations were analyzed. The requirements were for a noise figure of less than 0.8 dB, so the MATLAB code in Appendix A was used to plot this noise circle. With the selected values, the calculated Noise Figure was 0.63 dB which is less than the maximum of 0.8 dB. Next, the available power gain method was used to plot the constant VSWR circle for a gain of 18 dB using the MATLAB code in Appendix A.

With all the parameters, the Smith chart in Figure 3 was obtained where the red circle is output stability, the green circle is the available power gain circle for a gain of 18 dB, and the pink circle is the noise circle.

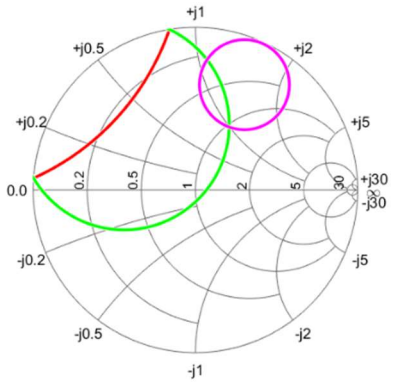


Figure 3: Smith Chart For IMN from MATLAB

This chart was also plotted in ADS using the simulation feature to have more accurate results.

The biasing network was created in ADS with ideal DC and AC blocks to create an output simulation from the S-parameters and biasing network. From this (Appendix C), it was decided

that a good value for the input impedance which satisfies all the parameters was Zs = 0.6+j1.47. This means that the IMN will have to match the source impedance to the normalized value stated before.

From the Smith chart, the value of the source reflection coefficient was measured which through the code in Appendix A allowed us to determine that the value for the load impedance would have to be Zl = 0.9774+j0.9215. This means that the OMN will have to transform the value of the normalized load impedance to the value mentioned before. This point was also plotted in the Smith chart with the output stability circle to ensure the system remained stable, which it was.

The next step was to design the IMN and the OMN. The MATLAB code in Appendix A and the hand calculations in Appendix B were used to obtain the matching networks.

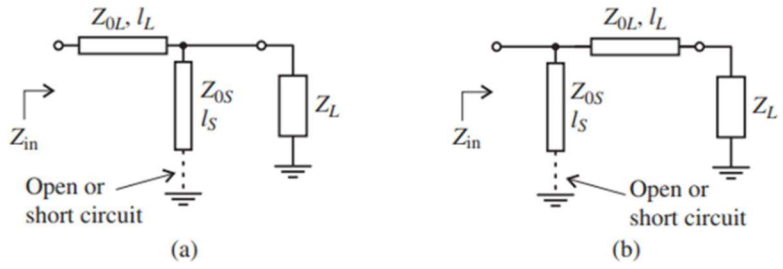


Figure 4: Microstrip Matching Networks Configurations

For the IMN, configuration b) of Figure 4 was used, while for the OMN configuration a) was used. The purpose of this was to have the stubs as far as possible of the RFCs which would be close to the transistor. It was calculated that the length l_L=3.425 cm and the length l_s=0.924cm. Furthermore, it was chosen for l_s to be short-circuited to have a shorter stub and to keep the integrity of the RF signal by allowing it to go to ground. For the OMN, I_L=3.173cm, and l_s=1.674cm. Similarly, the stub was chosen to be short-circuited to have a shorter stub and for signal integrity.

Finally, a non-linear analysis was performed using the MATLAB code in Appendix A to assess the last requirements which include intermodulation distortion, harmonics, and gain compression. Since this amplifier consists only of one stage, the values for P_{1dB} and $IP3_{out}$ are those of the first and only stage. These values are P_{1dB} = 10.5 dBm and $IP3_{out}$ = 23.5 dBm which are higher than the minimum values. Furthermore, it was calculated that the dynamic range d_R = 64.88 dB and the free spurious dynamic range d_f = 51.92 dB. Since the amplifier was designed for a gain of 18 dB, this means that the design would be operating within the linear region and intermodulation distortion would not affect the output.

Implementation and Measurements

The calculated Zs and ZL parameters were then implemented into the line calculation feature in ADS. The network shown in Appendix C is the network created from these values. The optimization of the circuit through the goals in Appendix C changed the IMN lengths to l_L= 2.742 cm and l_s=0.493 cm. The optimization goals also changed the OMN lengths to l_L=2.9235 cm, and l_s=2.659 cm.

In addition, the transition from a theoretical circuit to a real microstrip line circuit resulted in capacitors being added between each stub end and ground except the input quarter wavelength stub. This is to create an AC ground across the capacitors.

The transistor was the main component being added to the board. This requires building the pads from the data sheet on ADS and providing the appropriate gaps for the component to be soldered onto the board. The gap measurements for all parts were measured out based on the gap sizes of the resistors and capacitors. The resistors and capacitors were chosen based on the size in stock and the impedances available. These were then implemented into the circuit with gaps and pads for the components.

Once the amplifier values where calculated and the PCB design was performed using ADS, the PCB was printed. Then, the discrete components like the transistor and capacitors were soldered into the board. A photo of the final physical product has been included in Figure 5 below.

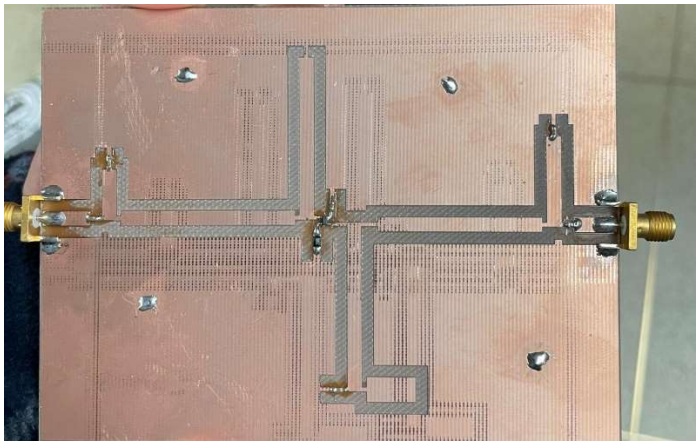


Figure 5: Final Physical Product

On the testing day, the circuit was tested in a lab environment using a special signal generator and oscilloscope to measure the frequency response of the amplifier with respect to S21 (gain), and S11 (input return loss) within a range of frequencies from 0.3MHz to 8.5GHz. Furthermore, the circuit was biased to 4.3 VDC with a DC power supply.

After testing, the data was gathered and the graphs generated have been included in the figures below.

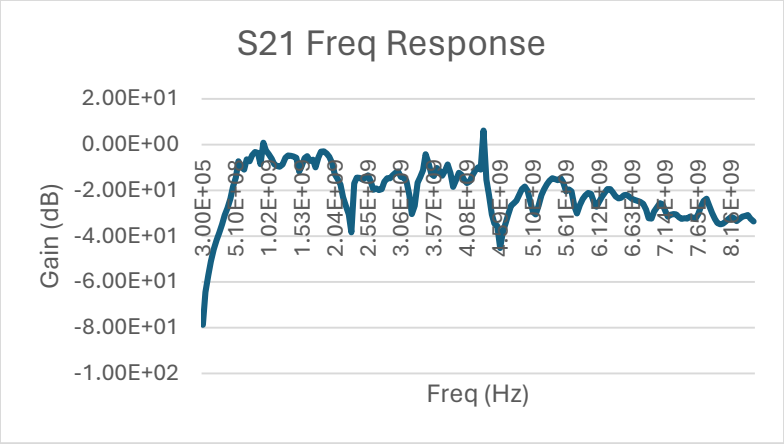


Figure 6: S21 Frequency Response

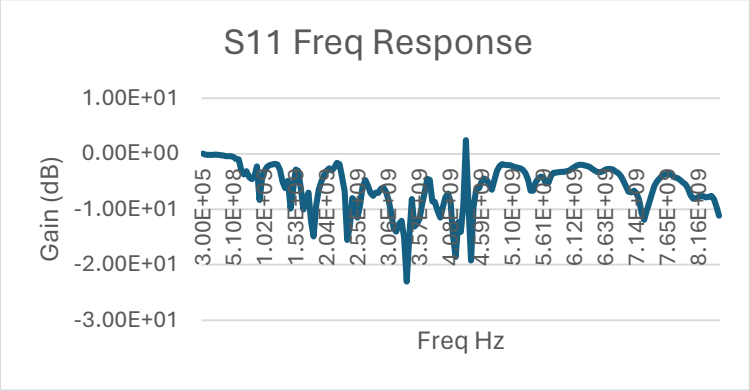


Figure 7: S11 Frequency Response

As seen in figure 6, the graph for the gain (S21) shows that in the design target frequency range of 2.35 to 2.45 GHz the gain is a negative dB value. This means that in the linear scale, the gain was less than 1 and greater than zero which means that the RF signal was attenuated instead of amplified. However, the graph shows that for a frequency of 4.34 GHz, the RF signal experienced a gain of 6.15 dB. These results were unexpected because the amplifier was designed to produce a gain at a frequency of 2.4 GHz, but the actual results showed there was no amplification at this frequency and there was at 4.34 GHz. The possible reasons for this behavior will be discussed in the next section.

As seen in figure 7, the graph for the input return loss (S11) reveals that this parameter has a negative dB value throughout the target design frequency range of 2.35 to 2.45 GHz. The data also shows that at a frequency of 2.47 GHz S11 = -8 dB and at a frequency of 2.51 GHz S11 = -8.52 dB which means that the requirement for the input return loss was achieved at frequencies very close to the target 2.4GHz.

Analysis

As it was discussed in the implementation and measurement section, the final design and testing did not yield the results expected in terms of gain. For the desired operating frequency of 2.4GHz, the RF signal was attenuated instead of amplified. Furthermore, there was an amplification of 6.15 dB at a frequency of 4.34 GHz. There could have been multiple factors that led to the deviation between the theoretical values and real results. Firstly, it is not believed that the deviations were due to a biasing issue. This is because when testing the circuit, the voltage between the gate and the source of the MOSFET was close to 3VDC which was what it was designed for. Furthermore, the biasing voltage was swept across a range of acceptable values without having any success in achieving the desired gain values.

After ruling out the biasing as a possible cause of the inability to obtain the desired gain, it is hypothesized that the reason for this could have been a combination of the matching network design and the PCB design for RF signal integrity. There is a possibility there was a mistake in the design of the matching networks when using the MATLAB code in Appendix A or the hand calculations in Appendix B. If a major mistake was made in the design of the matching networks, this means that the input and output impedances required for the transistor to generate the desired gain were not achieved and another value for the gain was obtained. This could also explain why there was gain observed at 4.34GHz instead of 2.4GHz.

The second possible reason has to do with the design of the PCB. RF design is a complex subject as the PCB needs to have multiple considerations for signal integrity. These factors include shielding along the RF signal traces and multiple vias in the ground plane. Both of these are done to preserve the quality of the RF signal. Due to the learning stage we are at, these other considerations were not taken into account. As a result, the RF signal was not correctly handled in the PCB leading to scattering and additional attenuation within the board.

Another hypothetical reason could be the sections added to the board to accept the SMA connectors did not take into account the wavelength of the input frequency. This shortcoming and misunderstanding of how the input and output interact with the circuit was a highly probable reason for the circuit not performing. In the next iteration of the board we would attach the LNA to be on a wavelength stub to ensure that an integral signal is being input onto the board.

This change would change the length of the connecting stub to 12 mm to 0 mm. By attaching the SMA connector directly to the end of the circuit the wavelength will be inserted without inserting an inaccuracy which un-validated the matching network.

Another improvement in the next iteration of the circuit would be the removal of the extra connecting lines between stubs. The most accurate way to connect each component of the

network is to have them T up directly next to eachother. In the circuit designed we had a space with a thin wire connecting the components, this wire may have brought unforeseen error to our circuit.

The last main component that was missing from the constructed PCB was the fact that we were unable to achieve a simulated gain of more than 8dB. The simulations outcome from the optimizations didn't allow for us to be able to simulate the correct gain. The theoretical gain was calculated to be 18dB but did not match ADS. To fix this error we would allow more components of the circuit to be modified to hopefully allow ADS to achieve a positive gain. Another possible solution to these problems would be to modify the weights or goals themselves more than what has already been changed.

Conclusion

The design of an LNA board is complicated, but also an amazing learning experience. We learned the power of ADS and how it can be applied to help create a gain, but with powerful computing comes complexity. The difference between our theoretical circuit, gains, ADS, and the tested circuit board posed different challenges along the way. We believe we did accurate initial calculations of the circuit, and in the next iteration would put a larger focus and more time on the fine tuning within the ADS software. The key findings of the circuit are shown below.

Table 2: Final Results

	Goal	Achieved
Biasing Voltage	3.0V	3.2V
Biasing Current	20mA	20mA +- 5mA
S11	-8 dB <	-8.52 dB
Gain at 4.3 GHz		6.15 dB

The low noise amplifier design procedure was followed to achieve an amplifier based on theoretical calculations. The final product was achieved by designing a DC biasing network, stability network design, impedance matching network design, layout, ADS simulations and optimizations, nonlinear analysis, Gerber file generation, prototype building, and testing and verification of the final results.

Even though the final product did not achieve the final amplification objectives, the process involved in designing the amplifier was extremely valuable to understanding the process and theory learned in class through its application. This process also was valuable in the development of critical thinking skills and problem-solving through creativity and the use of theoretical concepts.

Finally, both group members contributed equally to the contribution of the project. Tasks were divided equally to make sure understanding of the topics were achieved and collaboration was crutial to achieve the final design.

Appendix A: MATLAB Code

```
%Transistor Parameters
%Freq=2.393675GHz
clc
clear all
disp(['Transistor Parameters'])
s11dBmag=-2.86;
s11dBph=-108.74;
s12dBmag=-25.24;
s12dBph=26.54;
s21dBmag=15.58;
s21dBph=91.14;
s22dBmag=-3.21;
s22dBph=-52.01:;
s11 = 10^(s11dBmag/20)*exp(s11dBph/180 * pi* 1i); % Convert from dB to linear scale
s12 = 10^(s12dBmag/20)*exp(s12dBph/180 * pi * 1i);
s21 = 10^(s21dBmag/20)*exp(s21dBph/180 * pi * 1i);
s22 = 10^(s22dBmag/20)*exp(s22dBph/180 * pi * 1i);
disp(['s11 = ', num2str(abs(s11)), '<', num2str(angle(s11)*180/pi)])
disp(['s12 = ', num2str(abs(s12)), '<', num2str(angle(s12)*180/pi)])
disp(['s21 = ', num2str(abs(s21)), '<', num2str(angle(s21)*180/pi)])
disp(['s22 = ', num2str(abs(s22)), '<', num2str(angle(s22)*180/pi)])
delta = ((s11*s22) - (s12 * s21)); %complex
k = (1 - abs(s11*s11) - abs(s22 * s22) + abs(delta * delta))/(2 * abs(s12*s21));

%Unilateral Design Check
disp(['Unilateral design considerations'])
GTU = 18;
U = (abs(s12*s21*s11*s22))/((1-abs(s11^2))*(1-abs(s22^2)));
MD = 1/(1+U)^2;
LD = 1/(1-U)^2;
MDdB = 10*log10(MD);
LDdB = 10*log10(LD);
Lessval = (MDdB/GTU)*100
Plusval = (LDdB/GTU)*100
%Stability Considerations
%For Output Stability
disp(['Stability Considerations'])
Cout = (conj(s22 - conj(s11)*delta))/ (abs(s22 * s22) - abs(delta * delta));
Coutmag = abs(Cout)
Coutph = angle(Cout)*180/pi
Coutc = [(real(Cout)), (imag(Cout))];
rout = abs(s12 * s21)/ ( abs(abs(s22 * s22) - abs(delta * delta)))
%For Input Stability
```

```
Cin = (conj(s11 - conj(s22)*delta))/ (abs(s11 * s11) - abs(delta * delta));
Cinmag = abs(Cin)
Cinph = angle(Cin)*180/pi
Cinc = [real(Cin), imag(Cin)];
rin = abs(s12 * s21)/ ( abs(abs(s11 * s11) - abs(delta * delta)))

%Available Power Gain Method
disp(['Available Power Gain Method'])
GAdB = 18; %Target gain in dB
GA = 10^(GAdB/10); %Target gain in linear scale
ga = GA/(abs(s21))^2;
dga = (ga*conj(s11-(delta*conj(s22))))/(1+(ga*(abs(s11*s11)-abs(delta*delta))));
dgac = [real(dga), imag(dga)];
numrga = sqrt(1-(2*k*ga*abs(s12*s21))+(ga*ga*(abs(s12*s21))^2));
denrga = abs(1+(ga*(abs(s11*s11)-abs(delta*delta))));
disp(['dga = ', num2str(abs(dga)), '<', num2str(angle(dga)*180/pi)])
rga = numrga/denrga

%Noise Figure Code
Gsmag=0.7 %insert magnitude of gammaS
Gsphase=60.28 %insert phase of gammaS in deg
Gs = Gsmag*exp(1i*deg2rad(Gsphase));
Goptmag = 0.745;
Goptph = 65;
Gopt = 10^(Goptmag/20)*exp(Goptph/180 * pi* 1i)
Fmin = 10^(0.39/10); %dB
Rn = 8;   %this gets divided by 50 to become 0.16
Zo = 50;
F = (Fmin + (4 * Rn / Zo) * (abs((Gs-Gopt)*(Gs-Gopt))) / ((1-abs(Gs * Gs)) *
(abs(1+Gopt))*(abs(1+Gopt))));
NF = 10 * log10(F) %should be less than 0.8
Fk = 10^(0.8/10);
Qk = (abs(1 + Gopt) * abs(1 + Gopt)) * (Fk-Fmin)/(4 * Rn / Zo); % Where in circle
dfk = Gopt/(1 + Qk) %Center of Circle
df = [real(dfk), imag(dfk)];
rfk = sqrt(((1-(abs(Gopt))^2)*Qk)+Qk^2)/(1+Qk)

%Biasing Calculations
syms Rs
VDS=3; %volts
ID = 0.02; %in Amps
Vth = -0.8; %in volts
gm = 0.08; %in S
EQ = (ID*ID*Rs^2)+(2*Vth*ID*Rs)+((Vth^2)-((4*ID^2)/(gm^2)))
R1=solve(EQ)
VDD = VDS+(R1(1)*ID)

%plotting circles on smith chart
h = smithplot
hold on;
viscircles(Cinc, rin, 'Color','r') %input stability red
```

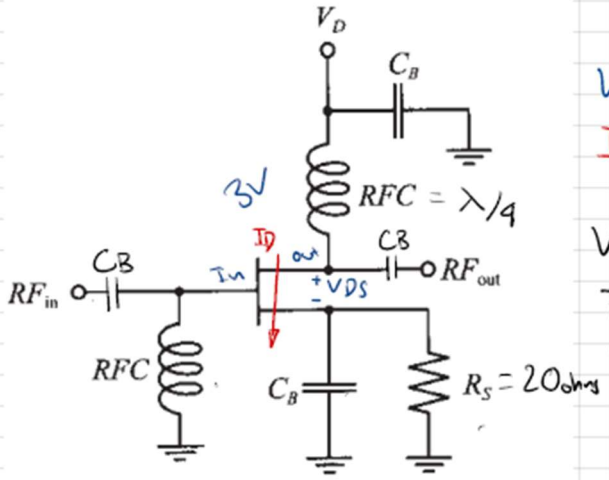
```
%viscircles(Coutc, rout, 'Color', 'b') %output stability
viscircles(dgac, rga, 'Color', 'g') %gain circle
viscircles(df, rfk, 'Color', 'm') %Noise circle

%Output matching network
%Method 1
rsmag=0.7 %insert magnitude of gammaS
rsphase=60.28 %insert phase of gammaS in deg
rs = rsmag*exp(1i*deg2rad(rsphase));
disp(['gammaS = ', num2str(abs(rs)), '<', num2str(angle(rs)*180/pi)])
gammaout = s22 + ((s21*s12*rs)/(1-(s11*rs)));
gammaL = conj(gammaout);
Zl = (1+gammaL)/(1-gammaL)
%Input matching network
freq = 2.4e9;%frequency in Hz
c=299792458; %speed of light m/s
wl=1 %(c/freq)*100
ls1=0.2742*wl
ls2=(0.337+(0.5-0.4372))*wl
ls1rev = (0.437-0.1623)
lst1=(0.5-0.426)*wl
lst2=(0.5-0.074)*wl %both for short end stub for 1
als1=(ls1*360)/0.5
als2=(ls2*360)/0.5
als1rev = (ls1rev*360)/0.5
alst1=(lst1*360)/0.5
alst2=(lst2*360)/0.5
%Output matching network continuation
lL1=0.162+(0.5-0.408)
lL2=0.162-0.0917
lstl1=0.5-0.366
lstl2=0.5-0.162 %both for short end stub
alL1=(lL1*360)/0.5
alL2=(lL2*360)/0.5
alstl1=(lstl1*360)/0.5
alstl2=(lstl2*360)/0.5

%Non-linear Analysis
B = 6e9;%bandwidth (Hz)
G = 18; %gain used
%noise figure is NF allready in dB
kT = -173.8; %This is 10*log10(kT) at 300K
X = 3; %SNR in dB
Pout1dB = 10.5; %dBm
IP3out = 23.5; %dBm
Pnout = kT+(10*log10(B))+G+NF; %dBm
Poutmds = Pnout + X; %dBm
dr = Pout1dB-Poutmds %in dB
df = (2/3)*(IP3out-Poutmds) %in dB
```

Appendix B: Hand Calculations

Biasing network Calculations.



$V_{DS} = 3V$

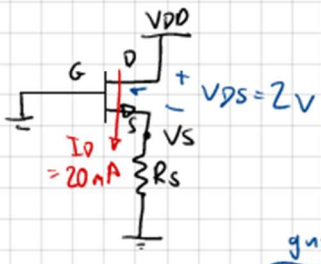
$I_D = 20mA$

$V_{DS} = V_{DD} - V_S =$

$3 = V_{DD} - (R_S I_D)$

$V_{DD} = 3 + R_S I_D$

DC Analysis:



$I_D = \frac{1}{2} K_n (V_{GS} - V_{tn})^2$

$V_{GS} = 0 - V_S \rightarrow V_{GS} = -V_S$

$V_S = I_D R_S$ so $V_{GS} = -I_D R_S$

$R_S = \frac{V_{GS}}{-I_D} = \frac{-0.4}{-0.02}$

$I_D = \frac{1}{2} \underbrace{K_n}_{gm = 80mS} (-I_D R_S - \underbrace{V_{tn}}_{-0.8V})^2$

$I_D = \frac{1}{2} K_n ((I_D R_S)^2 + 2 V_{tn} I_D R_S + V_{tn}^2)$ $\quad K_n = \frac{gm^2}{2I_D}$

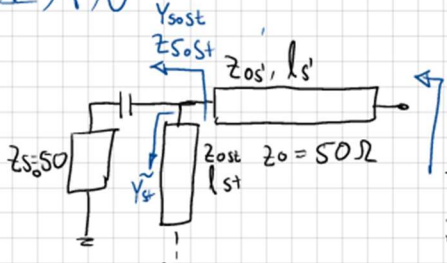
$I_D = \frac{1}{2} \frac{gm^2}{2I_D} ((I_D R_S)^2 + 2 V_{tn} I_D R_S + V_{tn}^2)$

$\frac{4 I_D^2}{gm^2} = I_D^2 R_S^2 + 2 V_{tn} I_D R_S + V_{tn}^2$

$0 = I_D^2 R_S^2 + 2 V_{tn} I_D R_S + \left(V_{tn}^2 - \frac{4 I_D^2}{gm^2} \right)$

$R_{S1} = 65\Omega \quad R_{S2} = 15\Omega$

IMN



$\tilde{z}_{s'} = 0.6 + j\,1.47$

$\tilde{z}_{so} = \frac{50}{50} \rightarrow \tilde{z}_{so} = 1$

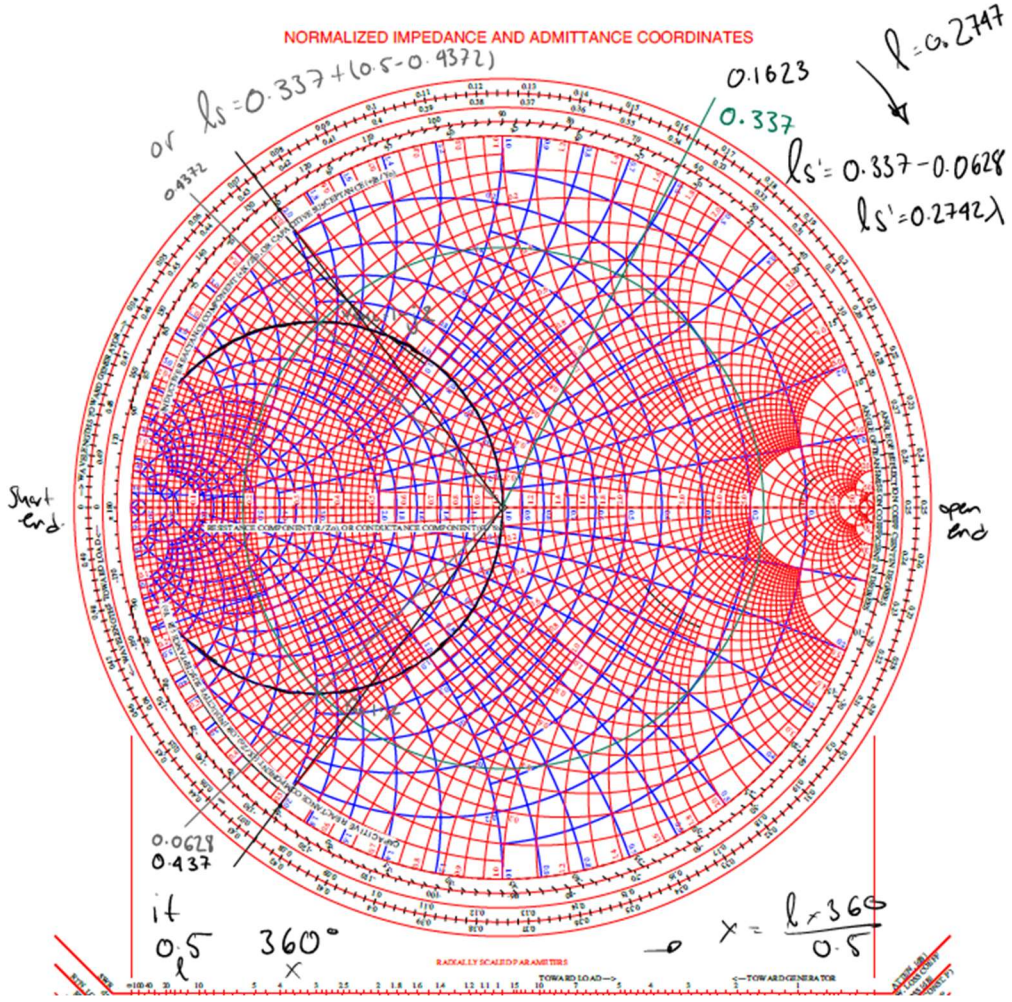
$\tilde{Y}_{so} = 1$

$\tilde{Y}_{sost} = \tilde{Y}_{so} + \tilde{Y}_{st} \rightarrow Y_{st} = Y_{sost} - Y_{so}$

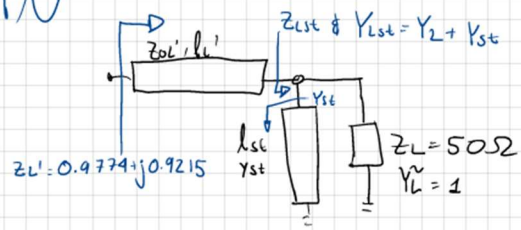
$Y_{sost} = 1 - j2$ $\quad Y_{st} = 1 - j2 - 1$

$Y_{st} = -j2$

So $Y_{st} = -j2$



OMN



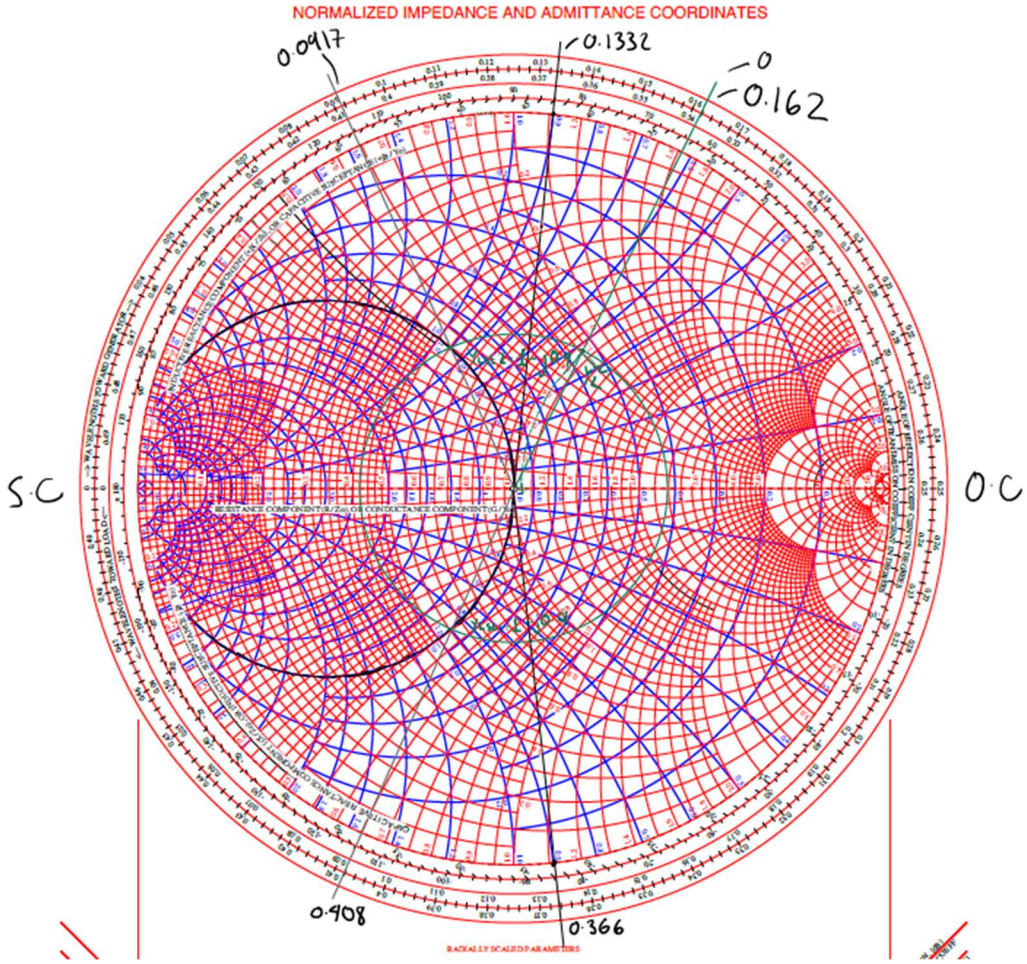
$Y_{lst} = y_{st} + y_L$

$\tilde{y_{st}} = Y_{lst} - y_L$

$= (1 \pm j0.9) - 1$

$y_{st1} = j0.9$

$y_{st2} = -j0.9$



Appendix C

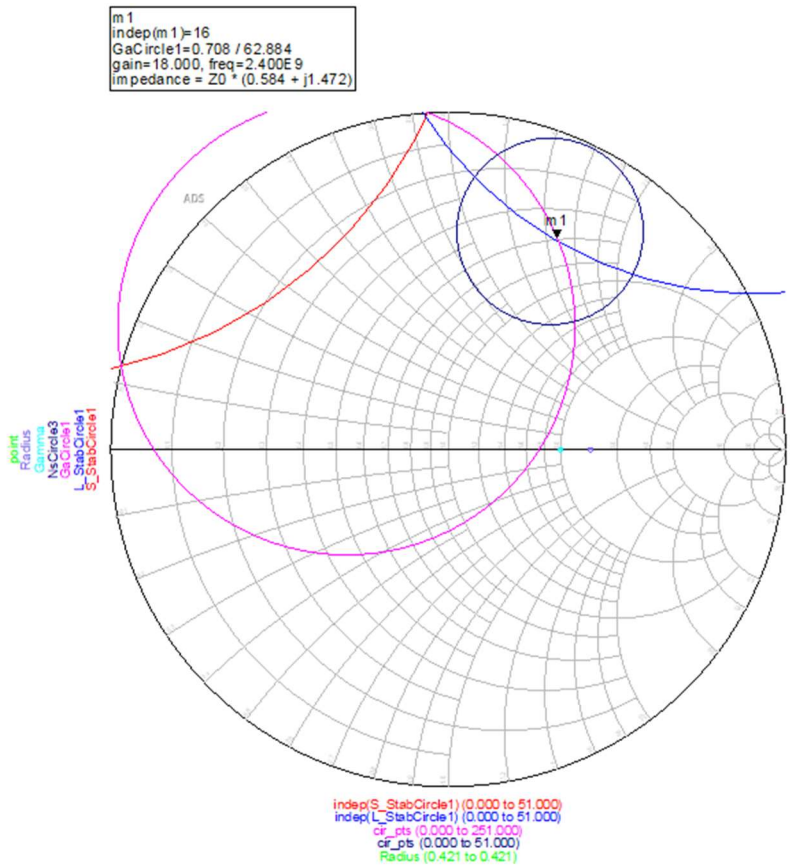
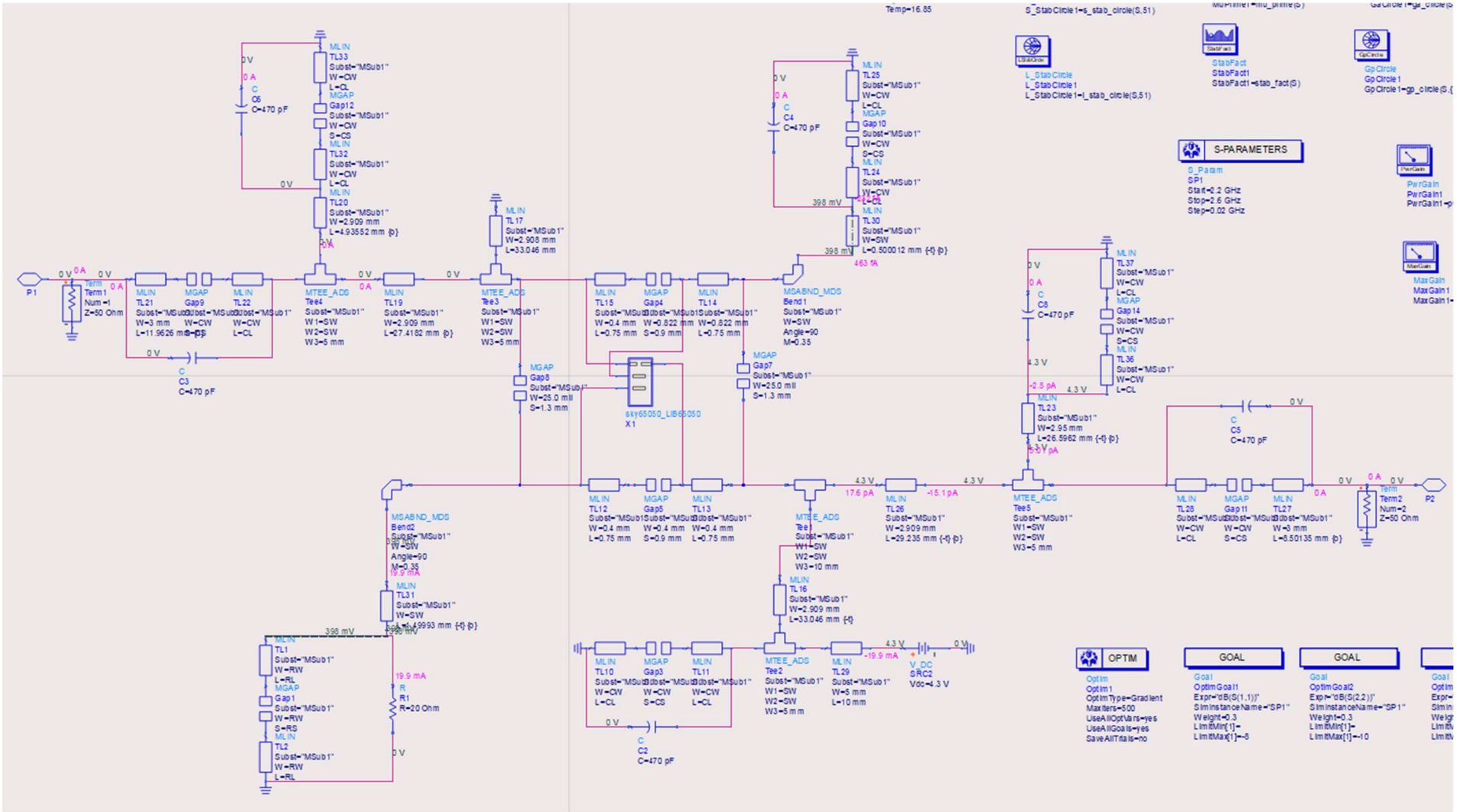
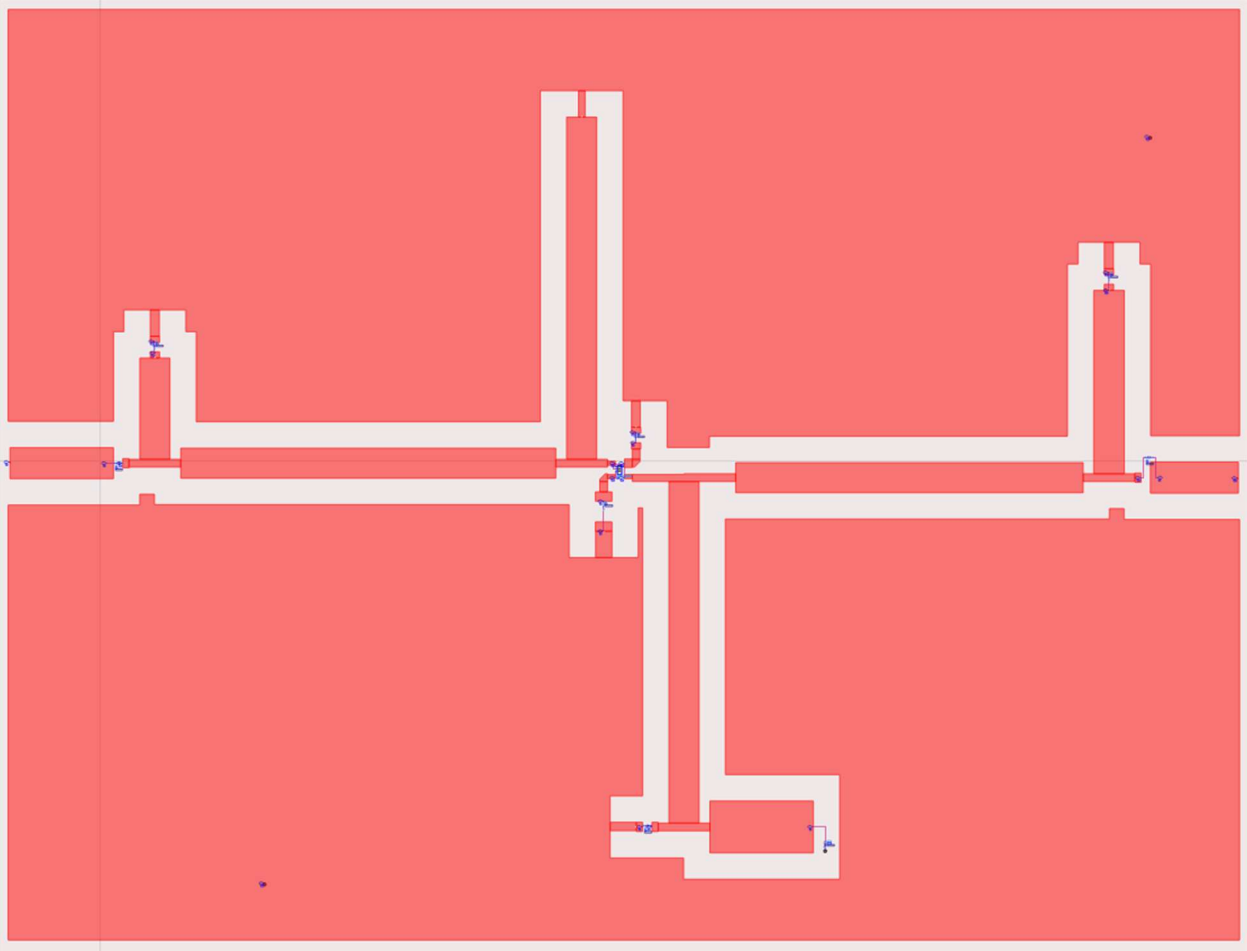


Figure 8: ADS smith chart

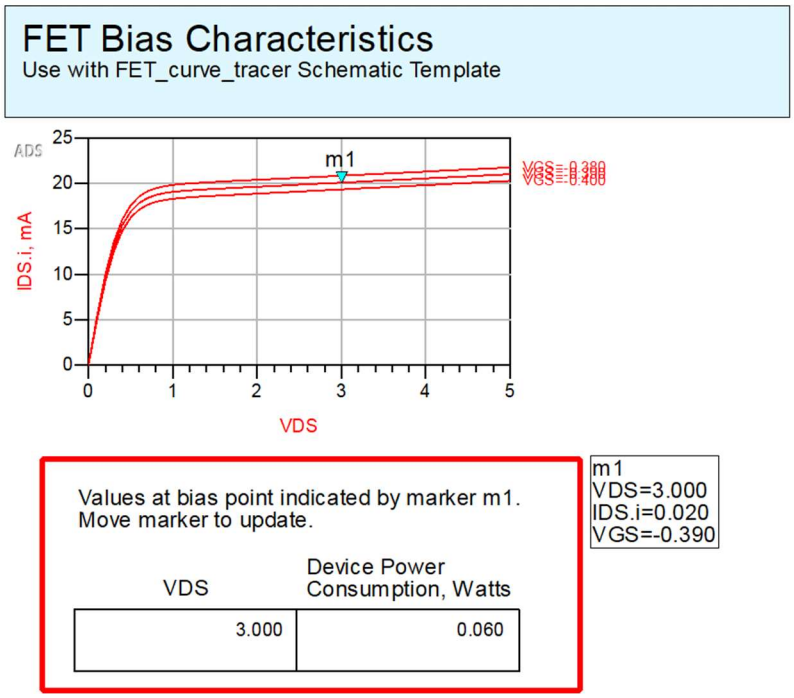

Temp=16.85
S_StabCircle1=s_stab_circle(S,51)
L_StabCircle
L_StabCircle1
L_StabCircle1=l_stab_circle(S,51)
StabFact
StabFact1
StabFact1=stab_fact(S)
GpCircle
GpCircle1
GpCircle1=gp_circle(S,
S-PARAMETERS
S_Param
SP1
Start=2.2 GHz
Stop=2.6 GHz
Step=0.02 GHz
PwrGain
PwrGain1
MaxGain
MaxGain1
P1
Term
Term1
Num=1
Z=50 Ohm
MLIN
TL21
Subst="MSub1"
W=3 mm
L=11.9626 mm {p}
MGAP
Gap9
Subst="MSub1"
W=CW
S=CS
MLIN
TL22
Subst="MSub1"
W=CW
L=CL
C
C3
C=470 pF
MTEE_ADS
Tee4
Subst="MSub1"
W1=SW
W2=SW
W3=5 mm
MLIN
TL20
Subst="MSub1"
W=2.909 mm
L=4.93552 mm {p}
C
C6
C=470 pF
MLIN
TL33
Subst="MSub1"
W=CW
L=CL
MGAP
Gap12
Subst="MSub1"
W=CW
S=CS
MLIN
TL32
Subst="MSub1"
W=CW
L=CL
MLIN
TL19
Subst="MSub1"
W=2.909 mm
L=27.4182 mm {p}
MTEE_ADS
Tee3
Subst="MSub1"
W1=SW
W2=SW
W3=5 mm
MLIN
TL17
Subst="MSub1"
W=2.908 mm
L=33.046 mm
MGAP
Gap8
Subst="MSub1"
W=25.0 mil
S=1.3 mm
MLIN
TL15
Subst="MSub1"
W=0.4 mm
L=0.75 mm
MGAP
Gap4
Subst="MSub1"
W=0.822 mm
S=0.9 mm
MLIN
TL14
Subst="MSub1"
W=0.822 mm
L=0.75 mm
MSABND_MDS
Bend1
Subst="MSub1"
W=SW
Angle=90
M=0.35
MGAP
Gap7
Subst="MSub1"
W=25.0 mil
S=1.3 mm
sky65050_LIB65050
X1
C
C4
C=470 pF
MLIN
TL25
Subst="MSub1"
W=CW
L=CL
MGAP
Gap10
Subst="MSub1"
W=CW
S=CS
MLIN
TL24
Subst="MSub1"
W=CW
L=CL
MLIN
TL30
Subst="MSub1"
W=SW
L=0.500012 mm {-l} {p}
398 mV
463 fA
C
C8
C=470 pF
MLIN
TL37
Subst="MSub1"
W=CW
L=CL
MGAP
Gap14
Subst="MSub1"
W=CW
S=CS
MLIN
TL36
Subst="MSub1"
W=CW
L=CL
MLIN
TL23
Subst="MSub1"
W=2.95 mm
L=26.5962 mm {-l} {p}
-2.5 pA
4.3 V
C
C5
C=470 pF
MLIN
TL12
Subst="MSub1"
W=0.4 mm
L=0.75 mm
MGAP
Gap5
Subst="MSub1"
W=0.4 mm
S=0.9 mm
MLIN
TL13
Subst="MSub1"
W=0.4 mm
L=0.75 mm
MTEE_ADS
Tee1
Subst="MSub1"
W1=SW
W2=SW
W3=10 mm
MLIN
TL16
Subst="MSub1"
W=2.909 mm
L=33.046 mm {-l}
MLIN
TL26
Subst="MSub1"
W=2.909 mm
L=29.235 mm {-l} {p}
MTEE_ADS
Tee5
Subst="MSub1"
W1=SW
W2=SW
W3=5 mm
17.6 pA
-15.1 pA
MLIN
TL28
Subst="MSub1"
W=CW
L=CL
MGAP
Gap11
Subst="MSub1"
W=CW
S=CS
MLIN
TL27
Subst="MSub1"
W=3 mm
L=8.50135 mm {p}
Term
Term2
Num=2
Z=50 Ohm
P2
MSABND_MDS
Bend2
Subst="MSub1"
W=SW
Angle=90
M=0.35
19.9 mA
MLIN
TL31
Subst="MSub1"
W=SW
L=4.49993 mm {-l} {p}
398 mV
MLIN
TL1
Subst="MSub1"
W=RW
L=RL
MGAP
Gap1
Subst="MSub1"
W=RW
S=RS
MLIN
TL2
Subst="MSub1"
W=RW
L=RL
R
R1
R=20 Ohm
19.9 mA
MLIN
TL10
Subst="MSub1"
W=CW
L=CL
MGAP
Gap3
Subst="MSub1"
W=CW
S=CS
MLIN
TL11
Subst="MSub1"
W=CW
L=CL
C
C2
C=470 pF
MTEE_ADS
Tee2
Subst="MSub1"
W1=SW
W2=SW
W3=5 mm
MLIN
TL29
Subst="MSub1"
W=5 mm
L=10 mm
-19.9 mA
V_DC
SRC2
Vdc=4.3 V
OPTIM
Optim
Optim1
OptimType=Gradient
MaxIters=500
UseAllOptVars=yes
UseAllGoals=yes
SaveAllTrials=no
GOAL
Goal
OptimGoal1
Expr="dB(S(1,1))"
SimInstanceName="SP1"
Weight=0.3
LimitMin[1]=
LimitMax[1]=-8
GOAL
Goal
OptimGoal2
Expr="dB(S(2,2))"
SimInstanceName="SP1"
Weight=0.3
LimitMin[1]=
LimitMax[1]=-10

Optimization Goals

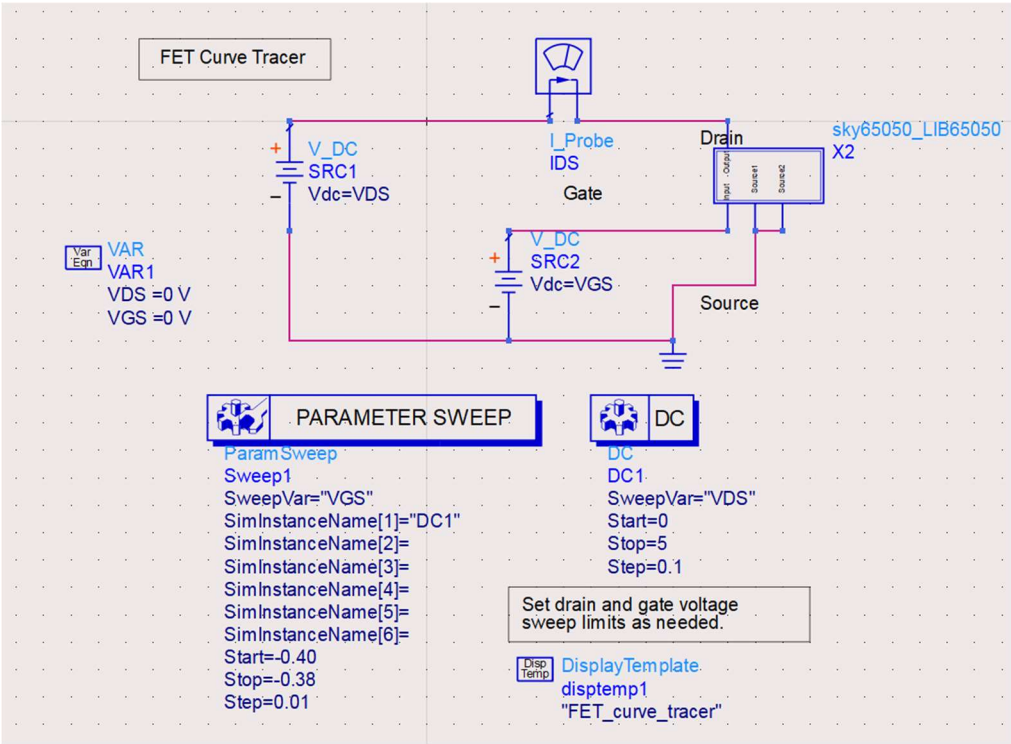
GERBER layout



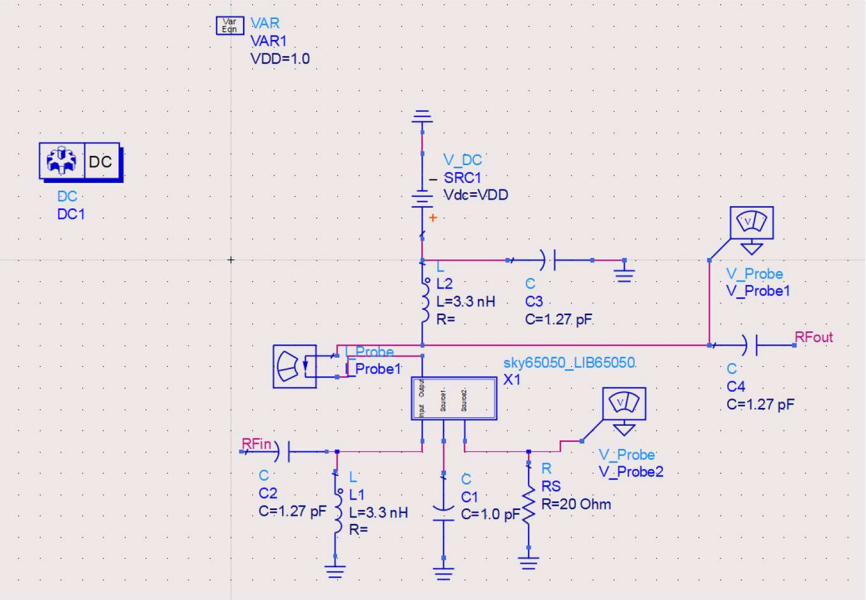
Choosing Id and VDD from FET DC analysis



Circuit for choosing Id and VDD



Biasing network and associated gains.



Gains for above circuit