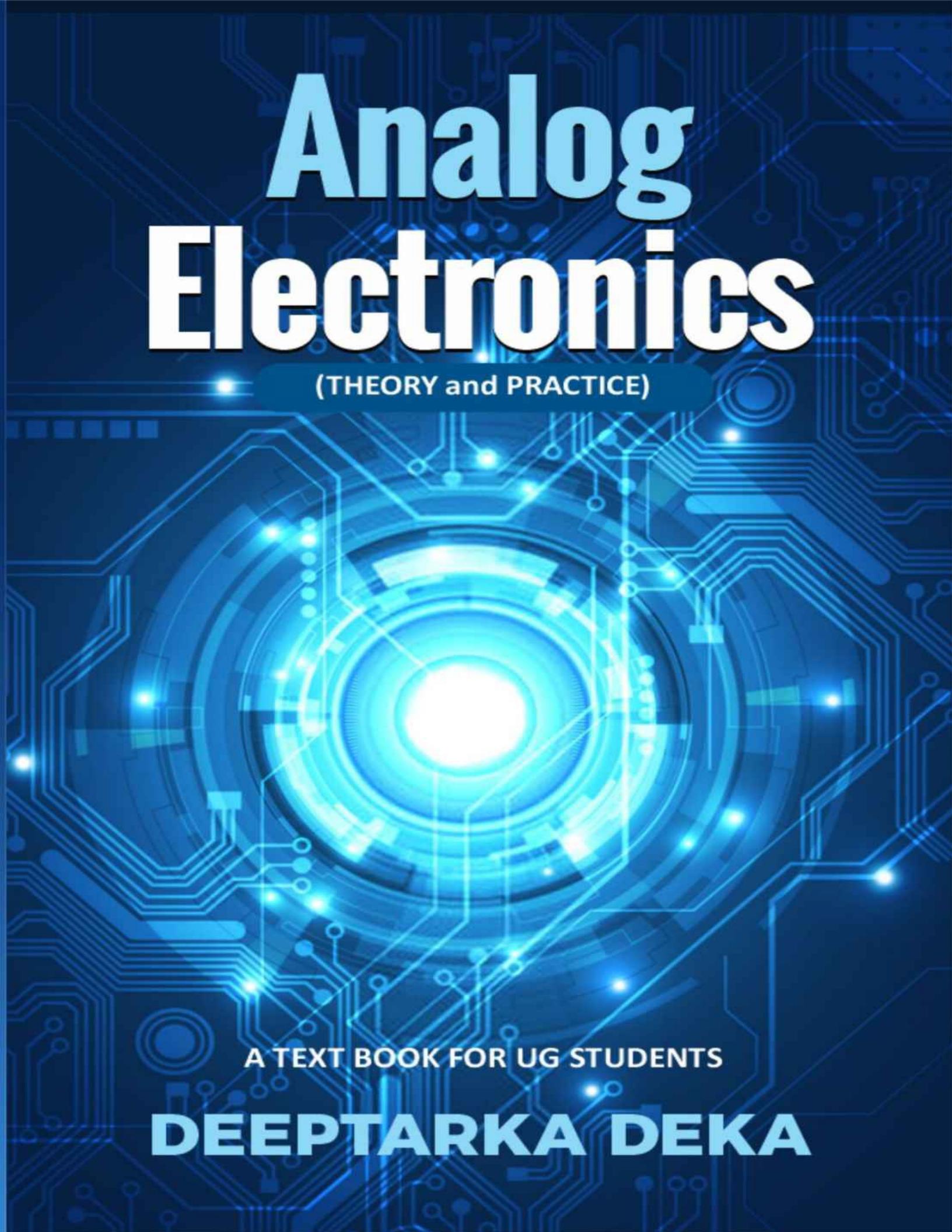


# Analog Electronics

(THEORY and PRACTICE)

The background of the book cover features a complex, glowing blue circuit board pattern. It consists of numerous thin, curved lines representing circuit traces, with small circular nodes at various points. A prominent feature is a large, bright, glowing blue circle in the center, which appears to be a stylized representation of a capacitor or a central node in a network. The overall effect is futuristic and high-tech.

A TEXT BOOK FOR UG STUDENTS

**DEEPTARKA DEKA**

# **ANALOG ELECTRONICS**

Theory and Practice

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*This book is dedicated to My Family and My Students*

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# **Foreword**

This book on Analog Electronics begins with a brief description of Semiconductor Physics, emphasising on the essential principles for the Electronics Industry. This is followed by a number of chapters on the theory and applications common devices, viz, Diodes, Transistors and OPAMPS.

The author's experience in teaching this subject over the course of time, in two Premier Engineering Colleges has been that the UG student gets somewhat intimidated with the heavy dose of Physics and Math in most of the existing material in print as well as on-line. Hence the author made it a practice to e-mail elaborate notes of the lecture classes to his students. This work is essentially an extension of that painstaking effort over the years.

The book is presented in easy to follow steps. Important expressions and equations have been elaborately derived. Each section contains a number of worked out numericals. A number of Practice Problems along with the answers have been included.

The content of the book conforms to the Standard AICTE curriculum followed by India's Technical Universities. Even though this book is primarily meant for the Third and Fourth Semester UG students, this will be of immense help as a refresher course to the Practicing Professional as well as the aspirants of various competitive exams in India as well as abroad.

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**Associate Professor  
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Jalukbari, Guwahati**

**26.03.2021**

## Preface

THIS WORK IS AN OUTCOME FROM THE AUTHOR'S CLASS NOTES , E-MAILED TO HIS STUDENTS OVER THE YEARS. THE FEEDBACK FROM THE STUDENTS WENT A LONG WAY IN IMPROVING THE CONTENT OF THIS BOOK. FOR THIS, THE AUTHOR REMAINS EVER SO GRATEFUL.

## **CHAPTER-WISE CONTENTS**

<b>Sl.No</b>	<b>NAME OF CHAPTERS</b>
1.	<b>SEMICONDUCTOR PHYSICS</b>
	<b>UNIT – 1</b>
	<b>DIODE</b>
2.	<b>THEORY OF P-N JUNCTION</b>
3.	<b>RECTIFIER AND FILTER</b>

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## **CHAPTER – I**

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# **SEMICONDUCTOR PHYSICS**

### *SEMICONDUCTOR PHYSICS*

## **INTRODUCTION**

Electronics is that branch of engineering science which deals with the principles and practice of “Controlling the Flow of Electrons (and Holes)” in a circuit by means of electronic devices. The need for the control of the flow of current in a circuit is with the specific objective of accomplishing a certain function. For example, in an amplifier, the “function” is to be such that the magnitude of the output power be greater than that applied at the input. This requires an Electronic Device. The device required for amplification is a transistor. In addition to amplification, a transistor is also used as an electronic switch. Various combinations transistors, configured as electronic switches form Logic Gates, which are the basic building blocks of the digital computer. Another common device is a Diode, which is most commonly used for converting AC into DC. Moreover, there exist various types of transistors and diodes, used for various diverse purposes along with a large variety of other devices designed to accomplish a plethora of applications and gadgets. Various electronic devices are integrated in a single chip to form an IC. Use of ICs has made it possible of achieving the goal of miniaturization of the size and optimization of the cost of electronic devices. These are the attributes which the modern human race increasingly welcomes in one’s day to day life and work.

Study of the modern electronic devices has to start with the study of Semiconductors. Semiconductors are materials whose electrical conductivity lie somewhere in between that of conductors and insulators. Property of matter is decided by the nature and the structure of the atoms and molecules contained in it.

## 1.1 THE ATOM

The Atom, in general, contains a few numbers of Electrons, an equal number of Protons and some Neutrons. An Electron is a tiny particle with a mass of  $9.1 \times 10^{-31}$  Kg and having a negative electric charge of  $-1.602 \times 10^{-19}$  Coulomb. A Proton is a particle which is 1840 times heavier than the electron and it has a positive charge of exactly the same magnitude as that of the electron, i.e.  $+1.602 \times 10^{-19}$  Coulomb. A neutron has a mass approximately equal to that of the Proton but it is electrically neutral. Protons and Neutrons form the central structure of the atom, called the Nucleus, in which the Protons and the Neutrons are very tightly packed so that they cannot be separated by chemical reactions. The Electrons of the atom circle around the nucleus in orbits of increasing radii. The orbits with the same radii are grouped in shells. Due to the opposite charges of the Nucleus and the Electrons, there exists a Potential Difference and an Electric Field between them. The negatively charged electrons also experience a force of attraction due to the positive charge of the nucleus. If an electron is to be removed from an orbit, an amount of Energy is required to be applied against the potential difference between the electron and the nucleus. This energy is measured in units of ‘Electron Volt’, eV.

**Electron Volt:** -1 eV is defined as the energy required to move a negative charge of  $-1.602 \times 10^{-19}$  C (Charge of an electron), over a potential difference of 1 Volt.

**Energy Level of a shell:** - The electrons in the orbit nearest to the nucleus experience the strongest force of attraction and those away from the nucleus experience lesser force of attraction. In other words, it requires more amount of energy to remove an electron from an inner orbit than that from an outer orbit. An Energy Level is assigned to each

orbit as follows.

- The Shell nearest to the nucleus (Innermost Shell) is assigned an energy level ‘0’.
- The shell next to it is assigned an energy level equal to the difference of energy required to remove an electron from the respective shell. Thus this shell is to be assigned a higher energy level.
- Proceeding this way, each outer shell will be assigned progressively higher energy levels. The outermost shell will be at the Highest Energy Level.

**Energy Gap between shells:** - Energy Gap between two successive shells is defined as the difference between their energy levels. This translates as the difference between the energy required to remove an electron from that shell and that from the next inner shell. Let the Energy required to remove an electron from an outer shell be  $E_1$  AND Energy required to remove an electron from innermost orbit be  $E_0$ .

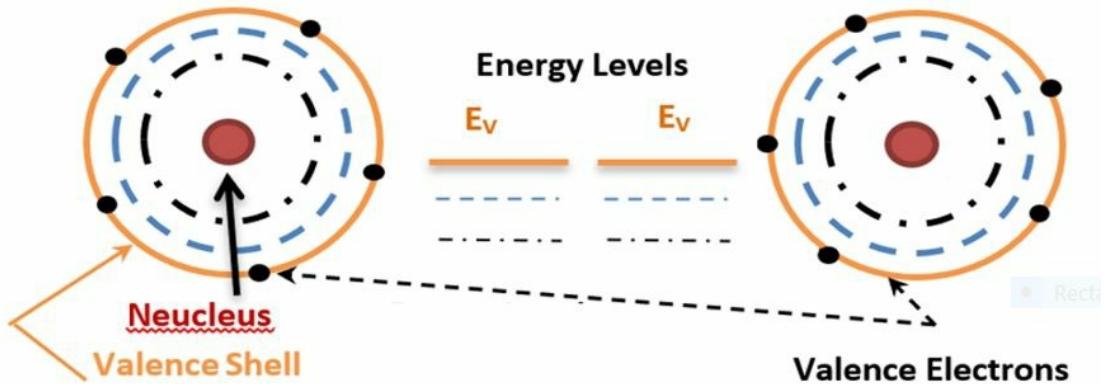
Thus, Energy Gap between the shells is given by

$$E_{\text{GAP}} = (E_1 - E_0)$$

The model of an atom and the associated energy levels of the shells is shown in the Fig- 1. This arrangement of electrons in these shells follows certain laws of quantum mechanics and is governed by laws and postulates, namely, Bohr’s Postulates and Pauli’s Exclusion Principle.

### **Bohr’s Atomic Model, Principal Quantum Number and Shells: -**

- Bohr’s Atomic Model states that electrons in an atom can exist only in some well-defined Orbit or Shells of fixed radii and a certain value of associated Energy Level corresponding to each Shell. The difference in Energy Level of the shells is the Energy Gap  $E_{\text{GAP}}$ . This is often represented as “ $E_g$ ”.
- A given Shell may contain more than one electron in certain Sub-Shells.



**Fig.-1:** - Isolated Atoms at Normal Room Temperature (in a Vapour State) and associated Energy Levels.

- Electron cannot exist in the space in between these shells. Since every shell has an associated Energy Level  $E_n$ , the electrons contained in the shell are said to possess that much amount of energy.
- If an atom is subjected to some external electromagnetic energy ‘E’ of some frequency “v”, then an electron in the outermost shell ‘a’ of Energy Level  $E_a$  will absorb this energy and jump up to the next higher shell ‘b’ of higher Energy Level  $E_b$ , (which will be at a greater radius) and the energy difference between them will be the Energy Gap

$$E_g = E_b - E_a$$

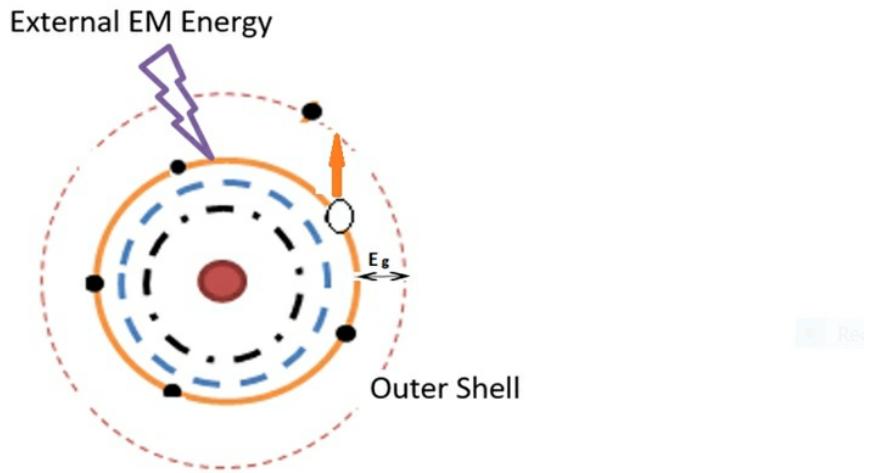
$$E_g = h v$$

Where “h” is Planck’s Constant.

- After absorbing the external energy, the atom is in an ‘Excited’ state.
  - Similarly, if an atom is existing in an excited state, then the excited electrons from the outermost shell will jump down to the next lower energy shell by releasing an amount of energy equal to
- $$E_g = h v$$
- This energy is released in the form of Electro Magnetic

radiation with a of frequency “v. This is shown in Fig.-2.

**Principal Quantum Number** :- A Serial number ‘n’ is each of these Shells or Energy Levels, where ‘n’ is an integer,  $n = 1, 2, 3, 4, \dots$ . The Principal Quantum Number of an electron in an atom is the ‘Serial Number’ of the shell corresponding to the shell where the electron is placed. The innermost Shell has  $n = 1$  and it is named as the ‘K’ shell. The second shell has  $n = 2$  and it is named as the ‘L’ shell. The third shell has  $n = 3$  and named ‘M’ and the fourth shell has  $n = 4$  and named ‘N’.



**Fig.-2:** - Due to externally applied EM energy, Valence Shell Electron jumps up to a higher energy Outer Shell.

**Sub-Shells; Angular Momentum Quantum Number, Magnetic Orientation Quantum Number, Spin Quantum Number:** - For each of the Integer value of the Principal Quantum Number ‘n’ of an electron, there exist three other Quantum Numbers, namely, Angular Momentum Quantum Number ‘l’, whose values are from 0 to  $(n-1)$ , Magnetic Orientation Quantum Number ‘ $m_l$ ’, whose values are from 0 to  $\pm l$ , Spin Quantum Number ‘ $s_p$ ’ whose values are  $\pm \frac{1}{2}$ .

**Pauli’s Exclusion Principle:** - Pauli’s Exclusion Principle states as follows -- “No two electron in an Electronic System can have the same set of values for all the four quantum numbers”. If we consider an atom as an Electronic System, then Pauli’s Exclusion Principle can be interpreted to state that “No two electron in any shell or sub-shell of an

atom can have the same quantum of energy”.

**Atomic Number:** - Atomic Number of an atom is defined as the total number of Protons in the nucleus of the atom. Since the atom must be electrically neutral in Normal Conditions, the number of electrons also equals the Atomic Number. Each element of the Periodic Table has a unique value of Atomic Number.

### **Electronic Configuration of Silicon and Germanium: -**

- The electrons of an atom are distributed in shells and sub-shells in a manner, so that Pauli’s Exclusion Principle is applied. Also, these must be distributed in such a manner that the electrons are assigned the minimum possible value of energy.
- Consider Silicon. Si has the atomic number of 14. These 14 electrons of the Si atom are distributed in the following manner.

#### **For the First shell, $n = 1$ .**

- When  $n = 1$ , the only value of  $l$  will be  $l = 0$  (since  $l$  is from 0 to  $(n-1)$ ).
- For  $l = 0$  the sub-shell is named as the ‘s’ sub-shell.
- When  $l = 0$ , the value of  $m_l$  is also 0.
- For this single value of  $m_l$  there will exist two values of  $s_p$ , namely,  $s_p = -\frac{1}{2}$  and  $s_p = +\frac{1}{2}$ .
- Thus, the first shell will contain two electrons and these will be denoted by  $1 s^2$ .

#### **For the second shell $n = 2$ .**

- When  $n = 2$ , the possible values of  $l$  are  $l = 0$  and  $l = 1$ . Thus, the second shell will contain two sub-shells for these two values of  $l$ . We had got earlier that for  $l = 0$ , the sub-shell is ‘s’. Next, for  $l = 1$  the sub-shell is named as the ‘p’ sub-shell.
- When  $l = 1$ , the possible values of  $m_l$  are -1, 0, and +1. For each of these three values of  $m_l$ , there will be two values of  $s_p$  each, namely  $s_p = -\frac{1}{2}$  and  $s_p = +\frac{1}{2}$ . Thus the ‘p’ sub-shell will contain 6 electrons, which are denoted as,  $2 s^2, 2 p^6$ .
- In total the second shell will have 8 electrons, 2 in ‘s’ sub-shell

and 6 in ‘p’ sub-shell.

- So far we have allocated 10 electrons in the first shell and the second shell. The remaining 4 electrons will be placed in the third shell, which will be the outermost shell of the Si atom. Their only possible distribution will be  $3\text{ s}, 3\text{ p}^2$ .
- When we sum up the above discussion, we get the overall electronic configuration of Si as  $1\text{ s}^2; 2\text{ s}^2, 2\text{ p}^6; 3\text{ s}^2, 3\text{ p}^2$ .
- Thus, the p sub-shell of the third and outermost shell of Si atom will remain partially filled.
- Similarly, for Ge, with the atomic number 32, we can arrange the distribution. This is tabulated for all the other elements of Group-IV below.

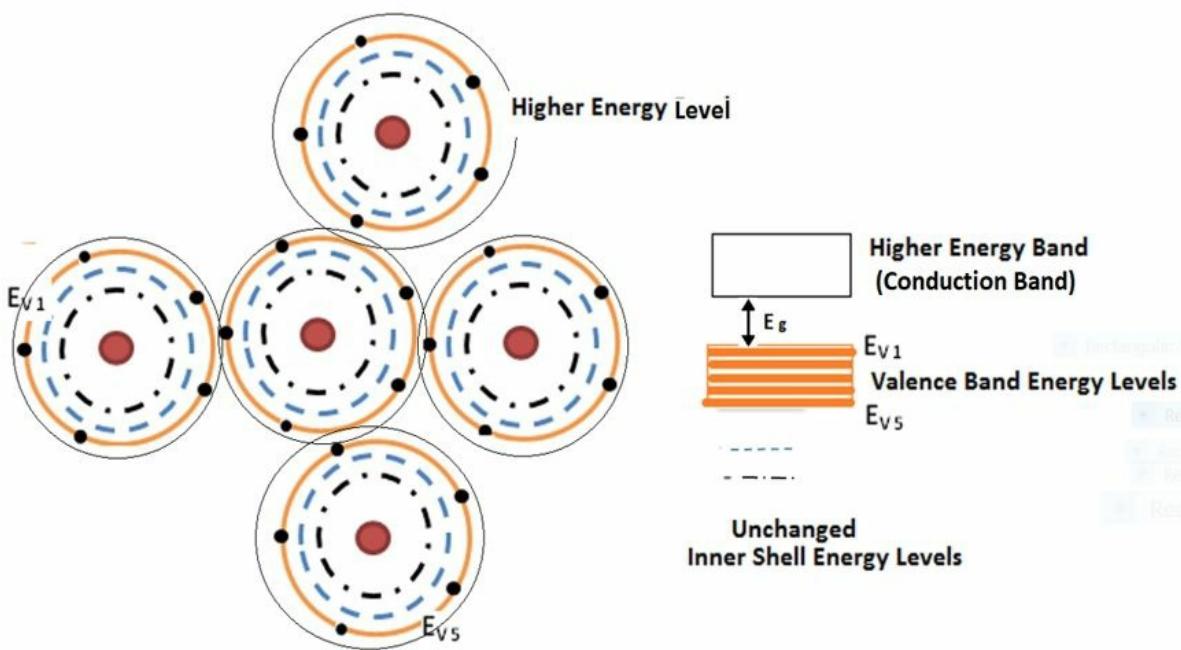
**Table 1** Electronic Configuration of Group-IV (A) Elements

Element	Atomic Number	Electronic Configuration
C	6	$1\text{s}^2; 2\text{s}^2, 2\text{p}^2$
Si	14	$1\text{s}^2; 2\text{s}^2, 2\text{p}^6; 3\text{s}^2, 3\text{p}^2$
Ge	32	$1\text{s}^2; 2\text{s}^2, 2\text{p}^6; 3\text{s}^2, 3\text{p}^6, 3\text{d}^{10}; 4\text{s}^2, 4\text{p}^2$
Sn	50	$1\text{s}^2; 2\text{s}^2, 2\text{p}^6; 3\text{s}^2, 3\text{p}^6, 3\text{d}^{10}; 4\text{s}^2, 4\text{p}^6, 4\text{d}^{10}; 5\text{s}^2, 5\text{p}^2$

## 1.2 Energy Band Theory of Crystals

- Solid matter is formed when the atoms of an element are packed densely, close to each other by means of Chemical Bonding. When the manner of packing is such that a basic structural unit is repeated periodically throughout the solid then the solid is said to be crystalline. This ‘Basic Structural Unit’ is called the **unit cell**. Many solids naturally solidify into crystals.
- When such a solid structure is formed, the Energy Levels of the Valance Shell and the Outer Excited Shell of each atom come under the influence of the nuclei of the neighbouring atoms.
- Due to the Chemical Bonding the electrons in the bonds form a composite Electronic System. Such a system must obey Pauli’s Exclusion Principle.

- This means that the electrons of the Valence Shell of this Electronic Structure are no longer confined to a single Atomic Energy Level. In other words, the energy levels of the cluster of atoms are spread out into a **Band of Energy Levels**. This is now called the **Valence Band**. This spreading out also occurs in the Outer Shell just above the valance shell. The band of energies of the outer shell is called the **Conduction Band**. This is shown in Fig – 3.



**Fig.-3:** – Spreading out of the Valence Shell energy levels into a Band (Valence band) and an outer Higher Energy Band. This higher energy band is called the Conduction Band.

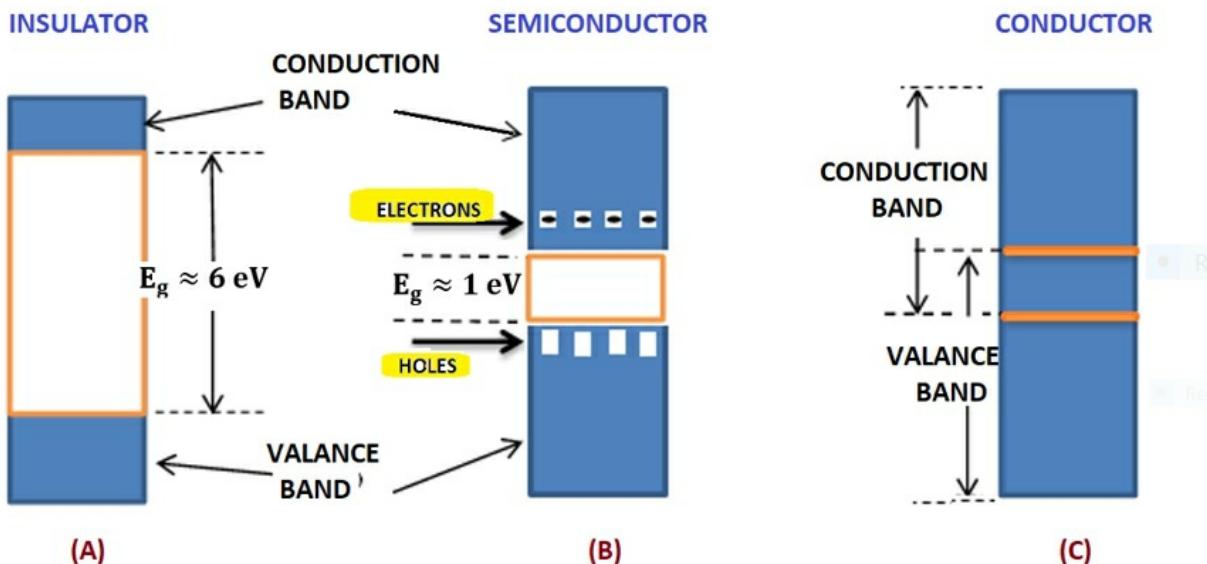
### 1.3 Conductors, Insulators & Semi-Conductors

Electrical Conductivity of matter depend upon the nature of the crystal. The substance is categorized as Conductor, Insulator or Semiconductor depending upon the value of the ‘Energy Gap  $E_g$ ’ between the valence band and conduction band.

- A substance whose Energy Gap is negligible, i.e., a substance

where the valence band and conduction band merge, is a **Conductor**.

- A substance in which the Energy Gap is large, is an **Insulator**.
- If a substance is such that the **Energy Gap is in between 0.6 to 1.8 eV, it is categorized as Semiconductor.**



**Fig.- 4:** - Formation of Energy bands when crystal is formed.

**Conductor:** - In the substance “C” in Fig-(4) the valance band and the conduction band merge. Any amount of ambient thermal or light energy will be absorbed by valance band electrons and these electrons will be easily exited to jump up to the Conduction Band. These energy bands are far away from the nucleus. Consequently, these electrons are loosely bound to the parent atom. Hence application of a potential difference across the substance will be able to set these electrons in motion, thereby giving rise to a current. Hence this substance is a conductor. Metals and carbon, in graphite form, exhibit this behavior.

**Insulator:** - Next, take the substance “A”. In this the valance band and the conduction band are separated by a wide energy gap of  $E_g \approx 6 \text{ eV}$ . Ambient energy in Normal conditions is not enough to excite the valance electrons to overcome this large Energy Gap. Hence the Conduction Band is empty. The valence electrons are tightly bound to the parent atoms. Hence application of external electric potential will not

be able to set these electrons in motion. Hence this substance will be an insulator.

**Semi-Conductor:** - Now consider the substance “B” in Fig-(4). In this the valence band and conduction band are separated by only a small amount of energy gap  $E_g \approx 1.1 \text{ eV}$ . At normal room temperature, the atmospheric heat and light energy of the surrounding will be absorbed by some of the valence electrons. These electrons will now get excited and jump up to the conduction band. Hence these electrons can get moving and give rise to a current when an external electric potential is applied. The electron “Departing” from the Valance Band leave behind a “Hole” in the Valence Band. This is an “Absence of an electron”. The Hole is equivalent to a positive charge of  $+ 1.602 \times 10^{-19} \text{ C}$ . The electron in the Conduction band and the Hole in the Valence Band are in a “Pair”. These are the current carriers in an Intrinsic Semiconductor. Silicon, Germanium and some Alloys like GaAs crystals exhibit this property. In silicon the energy gap  $E_g$  between conduction band and valence band is 1.1 eV at a room temperature of  $300^0 \text{ K}$  while in case of germanium this is about 0.72 eV.

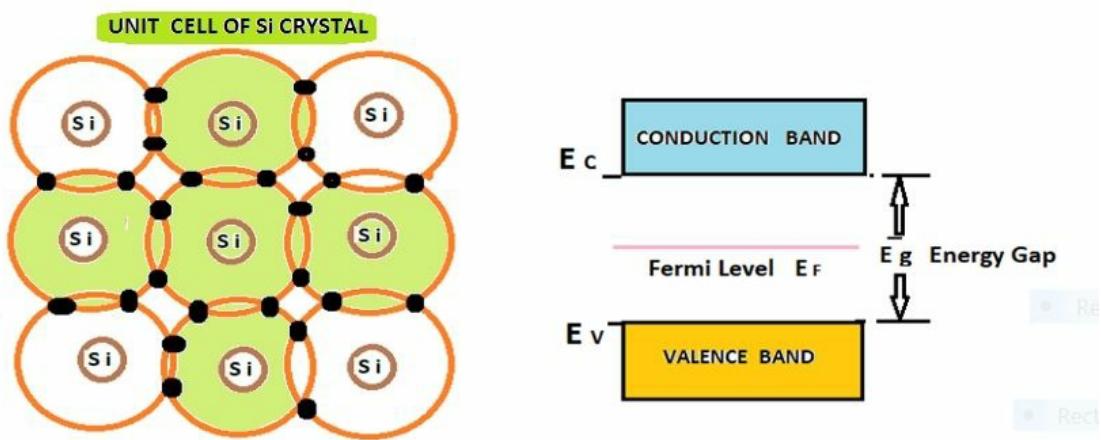
**A pure semiconductor crystal i.e., a semiconductor crystal without any impurity atom is called an “Intrinsic Semiconductor”.**

## 1.4 Energy Band Diagram of Intrinsic Crystal (Intrinsic Effect)

- Silicon and Germanium are tetravalent, i.e., the **outermost shell contains 4 electrons**. A simplified 2-dimensional representation of intrinsic silicon crystal is shown in the Fig- 5 below. The structure of Ge crystal is just similar to this.
- A stable structure of a solid crystal is formed by Covalent Bonding amongst the atoms of Si.
- In the process of formation of bonds, the outermost shell of an atom must attain the Inert Noble Gas configuration of 8 electrons in the valence shell. This can happen when 4 other surrounding Si atoms share one valence electron each, with the atom at the central position, in Covalent Bonding. This is the unit cell of Si crystal. When the unit cell is repeated periodically, each atom of the

crystalline structure will have 8 electrons in the valence shell. The energy band diagram is also shown alongside.

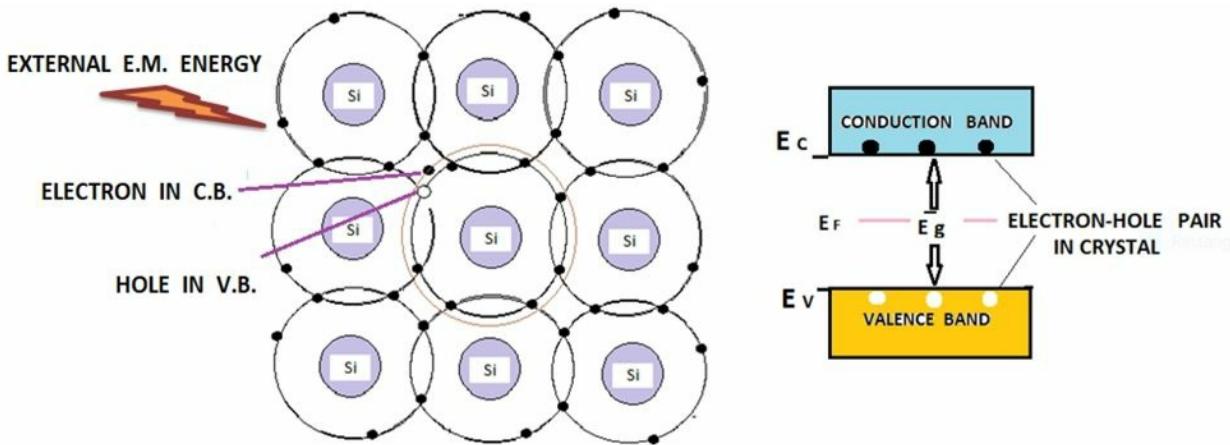
- At very low temperatures near about Absolute Zero, the valence band is completely filled with the valence electrons and the conduction band is completely unoccupied.
- Since the valence electrons are tightly bound to the parent atoms, they are not moved by the application of an external electric potential and the pure silicon crystal is **not** a very good conductor at such low temperatures.



**Fig.-5:** - *Crystal of Intrinsic Silicon and the Energy Band Diagram at near about Absolute Zero temperature. All valence electrons are bound to the valence band and conduction band is unoccupied.*

- Now consider that the crystal of **intrinsic semiconductor** be at normal condition in which there exists sufficient heat and light at the assumed normal room temperature of  $300^0\text{K}$ .
- If a valence electron absorbs an amount of energy equal to  $E_g$  (equal to the energy gap between valence band and conduction band), it is said to be in the excited state. The excited V.B. electron now jumps up to the higher energy level of C B. In the process it leaves behind a "Hole" in the V.B. These Electron-Hole Pairs are the current carriers in the intrinsic semiconductor. This situation is depicted in Figure- 6 below.

- So far we have mentioned that the valence electrons are able to jump up to the conduction band by absorbing heat energy equal to  $E_g$ . In fact this amount of energy may also be absorbed from a source of light, or from certain other forms of electromagnetic energy, namely,  $\gamma$ -Rays (gamma rays), X-rays or microwave radiations.



**Fig- 6.** Energy Band diagram of intrinsic semiconductor at normal room temperature and normal day light with free electrons in Conduction Band and holes in Valence Band.

**Fermi Energy Level in Intrinsic Semiconductor** is defined as the mean value of the energy levels of all charge carriers (Electrons and Holes) in a semiconductor. In case of Intrinsic Semiconductor, there are equal number of electrons in Conduction Band and holes in the Valence Band. Hence, Fermi Level occurs in the middle of the Energy Gap region. This position is at the mid portion between the lower most energy level of the C.B. ( $E_C$ ) and the upper most energy level of the V.B. ( $E_V$ ).

$$E_F = \frac{E_C - E_V}{2}$$

**Intrinsic Concentration and Mass Action Law:** - The concentration of free electrons in CB and concentration of holes in VB of an intrinsic semiconductor are called '**Intrinsic Concentration**'. These are denoted by  $n_i$  and  $h_i$  respectively, and given by the following equations.

$$n_i = 2 \left( \frac{2\pi m q k}{h^2} T \right)^{3/2} e^{(E_c - E_F)/kT} \quad \dots \dots (1)$$

$$n_i = N_C e^{-(E_c - E_F)/kT}$$

$$h_i = N_V e^{-(E_F - E_V)/kT}$$

Where,  $N_C$  and  $N_V$  are constants having dimensions of 'concentration', (i.e. number per cubic metre)  
Since electrons and holes come in pairs in intrinsic semiconductor, we must have  $n_i = h_i$ .

**The Mass Action Law states that product of  $n_i$  and  $h_i$  is a constant, given by**

$$n_i \cdot h_i = n_i^2 \quad \& \quad n_i \cdot h_i = h_i^2$$

Substituting the expression for Fermi Level " $E_F$ " from above and from equations 1 and simplifying we have equation 2

$$n_i^2 = h_i^2 = N_C N_V e^{-(E_c - E_V)/kT}$$

$$n_i^2 = N_C N_V e^{-E_g/kT} \quad \dots \dots (2)$$

(Since  $(E_c - E_V)$  is nothing but the Energy Gap  $E_g$ )

We also have

$$E_g = E_{G0} - \beta T \quad \dots \dots (3)$$

Where  $E_{G0}$  is the energy gap at  $0^0K$ . This quantity is a property of the crystal, whose value is 1.21 eV in Si and 0.785 eV in Ge.

The quantity  $\beta$  is a constant, whose value is  $3.60 \times 10^{-4}$  in Si and  $2.23 \times 10^{-4}$  in Ge.

As seen in Eq.-1, the constants  $N_C$  and  $N_V$  contain the various physical constants, namely, mass of electron  $m$ , effective mass of hole  $m_h$ , charge of electron  $q$ , charge of hole, Boltzmann constant  $k$  and Planck's constant  $h$ . Substituting we get  $E_g$ , and  $n_i^2$  in terms of a constant  $A_0$ .

Value of  $A_o$  for various semiconductor materials is tabulated in Table: 2 below.

$$n_i^2 = A_o T^3 e^{-E_g / kT} \quad \dots(4)$$

### Tab : – 2 Semiconductor Constants

Semiconductor Material	Value of $E_g$ (eV)	Value of $A_o \text{ cm}^{-6} \text{K}^{-3}$
Si	1.1	$2.735 \times 10^{31}$
Ga As	1.5	$4.41 \times 10^{28}$
Ge	0.72	$2.756 \times 10^{31}$

**Example 1:** – Calculate Intrinsic Concentration in (a) silicon (b) GaAs and

(c) Germanium crystals at a room temperature of (i)  $300^0\text{K}$ , (ii)  $310^0\text{K}$  and (iii)  $290^0\text{K}$ .

**SOLUTION:** - Substituting the numerical values of the quantities from the Table 1.2, using the value of Boltzmann Constant  $k = 86 \times 10^{-6} \text{ eV}/\text{K}$  and taking appropriate room temperatures of (i)  $300^0\text{K}$  and (ii)  $310^0\text{K}$  in the Eq. – 4, we get

#### **(a) For Si**

$$(i) \text{ at } 300^0\text{K} \quad n_i^2 = 2.735 \times 10^{31} \times 300^3 \times e^{(-1.1/86 \times 10^{-6} \times 300)}$$

$$n_i^2 = 2.25 \times 10^{20}$$

$$\therefore n_i = 1.5 \times 10^{10} \text{ intrinsic electrons/cm}^3 \text{ (at } 300^0\text{K})$$

$$(ii) \text{ at } 310^0\text{K} \quad n_i^2 = 2.735 \times 10^{31} \times 310^3 \times e^{(-1.1/86 \times 10^{-6} \times 310)}$$

$$n_i^2 = 9.81 \times 10^{20}$$

$$\therefore n_i = 3.1 \times 10^{10} \text{ intrinsic electrons/cm}^3 \text{ (at } 310^0\text{K})$$

$$(iii) \text{ at } 290^0\text{K} \quad n_i^2 = 2.735 \times 10^{31} \times 290^3 \times e^{(-1.1/86 \times 10^{-6} \times 290)}$$

$$n_i^2 = 0.467 \times 10^{20}$$

$$\therefore n_i = 0.68 \times 10^{10} \text{ intrinsic electrons/cm}^3 \text{ (at } 290^0\text{K})$$

**(b) For GaAs**

$$(i) \text{ at } 300^0\text{K} n_i^2 = 4.41 \times 10^{28} \times 300^3 \times e^{(-1.5/86 \times 10^{-6} \times 300)} | \\ n_i^2 = 6.7 \times 10^{10}$$

$$\therefore n_i = 2.6 \times 10^5 \quad \text{intrinsic electrons/cm}^3 \text{ (at } 300^0\text{K})$$

$$(ii) \text{ at } 310^0\text{K} \quad n_i^2 = 4.41 \times 10^{28} \times 310^3 \times e^{(-1.5/86 \times 10^{-6} \times 310)} \\ n_i^2 = 48 \times 10^{10}$$

$$\therefore n_i = 6.9 \times 10^5 \quad \text{intrinsic electrons/cm}^3 \text{ (at } 310^0\text{K})$$

**(c) For Ge**

$$(i) \text{ at } 300^0\text{K} \quad n_i^2 = 2.756 \times 10^{31} \times 300^3 \times e^{(-0.72/86 \times 10^{-6} \times 300)} \\ n_i^2 = 5.65 \times 10^{26}$$

$$\therefore n_i = 2.38 \times 10^{13} \quad \text{intrinsic electrons/cm}^3 \text{ (at } 300^0\text{K})$$

$$(ii) \text{ at } 310^0\text{K} \quad n_i^2 = 2.756 \times 10^{31} \times 310^3 \times e^{(-0.72/86 \times 10^{-6} \times 310)} \\ n_i^2 = 32.5 \times 10^{26}$$

$$\therefore n_i = 5.7 \times 10^{13} \quad \text{intrinsic electrons/cm}^3 \text{ (at } 310^0\text{K})$$

$$(iii) \text{ at } 290^0\text{K} \quad n_i^2 = 2.756 \times 10^{31} \times 290^3 \times e^{(-0.72/86 \times 10^{-6} \times 290)} \\ n_i^2 = 1.95 \times 10^{26}$$

$$\therefore n_i = 1.39 \times 10^{13} \quad \text{intrinsic electrons/cm}^3 \text{ (at } 290^0\text{K})$$

**OBSERVATION: -**

- (i) It is to be noted that the concentration of atoms in a Si crystal is  $5 \times 10^{22}$  atoms/cm<sup>3</sup> while that in Ge is  $4.4 \times 10^{22}$  atoms/cm<sup>3</sup>. From this the intrinsic concentration 'n<sub>i</sub>' (concentration of free electrons), for the Si crystal is found to be  $n_i = 1.5 \times 10^{10}$ , which amounts to about a ratio of 3 :  $10^{13}$  (electrons per atoms). Similar situation occurs for Ge also.
- (ii) As room temperature increases by  $10^0$  the concentration of free electrons (intrinsic concentration) increases approximately two-fold and when temperature decreases by  $10^0$  the intrinsic concentration reduces to half the value.

This is known as **INTRINSIC EFFECT**. This can be summarized as –

1. **Current in an intrinsic semiconductor is proportional to the**

- amount of electromagnetic energy in the surroundings.
2. Current in an intrinsic semiconductor varies by a factor of 2 for every  $10^0$  K change in surrounding temperature. Say, if current in an intrinsic semiconductor at a room temperature of  $300^0$ K is  $10 \mu\text{A}$ , then at  $310^0$ K it will increase to  $20 \mu\text{A}$  and at  $290^0$ K it will decrease to  $5 \mu\text{A}$ .

## 1.5 Current Flow in Intrinsic Semiconductor

The current flow in semiconductors is due to flow both electrons and holes. The conduction band contains “free electrons”. These behave similar to the electrons in a metal conductor. When an electric potential difference is applied, the electrons, being negative charges, begin to drift towards the positive terminal. Holes are in the valence band. These are equivalent to positive charges. Therefore, upon the application of electric potential, they drift towards the negative terminal. Since the negative charges and the positive charges are moving in opposite directions, the Net Current is due to the sum of the Electron Current and the Hole Current. This Net Current is in the direction of flow of positive charges, i.e., in the direction of movement of Holes. In other words, current flows from the positive terminal towards the negative terminal.

**Total current:** - It is observed in Fig.-7 that the direction of current due to movement of electrons and holes are in the same direction. Thus, total current is

$$I = I_h + I_e \quad \underline{\dots(5)}$$

In an Intrinsic Semiconductor, the number of electrons and holes are equal.

$$\therefore I_h = I_e$$

And  $I = 2 I_h \quad \& \quad I = 2 I_e$

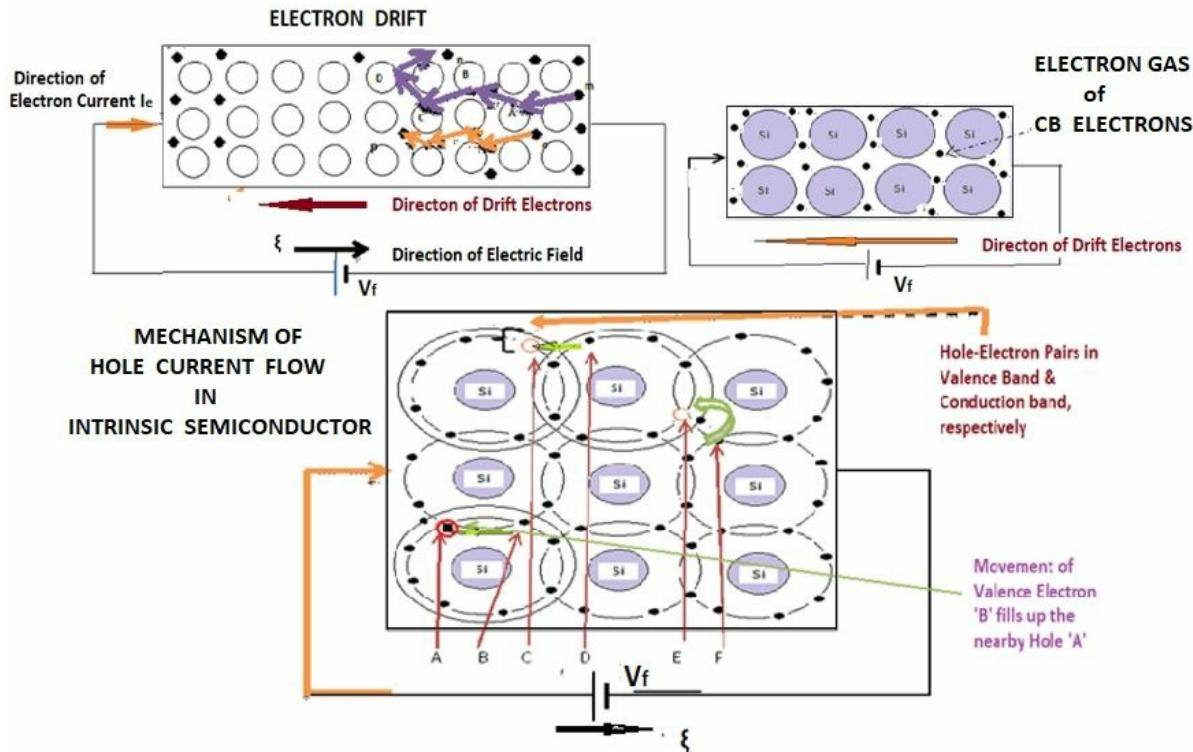
### Drift Current & Diffusion Current

There are two different mechanisms for current flow in a semiconductor. These are

## 1. Drift Current

## 2. Diffusion Current

These mechanisms apply to both electrons in the conduction band and holes of the valence band.



**Fig. -7. Drift Current of Electron in C.B. ( $I_e$ ):** - Electrons of the conduction band are uniformly distributed within the intrinsic semiconductor in the form of an 'Electron Gas'. An external electric potential imparts motion from Negative potential to Positive potential. The resulting current flow is IN OPPOSITE DIRECTION.

**Drift Current of Hole in V.B. ( $I_h$ ):** - Direction of Hole Drift in V.B., due to electron movement (green) and direction of resulting hole current (brown).

### Drift Current: --

- Conduction Band Electrons are “**Free Electrons**”. These are similar to the “**Electron Gas**” of free electrons in a metal conductor. When an electric potential is applied to the

semiconductor, the free electrons drift in a random zig-zag ‘**Drift**’ motion, with a mean direction of drift, towards the positive terminal.

- **Holes are equivalent to positive charges.** They exist in the valence band. They will also be imparted a mean drift motion in the valence band, towards the negative terminal.
- Drift velocity of the electrons ‘ $v_e$ ’ and Drift velocity of holes ‘ $v_h$ ’. Drift velocity is proportional to the applied electric potential. Electric potential gives rise to an **electric field ‘ $\xi$** . The Drift Velocities of electron and hole are proportional to this electric field.
- The Proportionality Constants  $\mu_e$  and  $\mu_h$  are termed as ‘**Mobility of Electron**’ and ‘**Mobility of Hole**’ respectively. These have the unit in  $\text{cm}^2/(\text{volt sec})$ . Using this, the Drift velocities of electron and hole are

$$v_e = \mu_e \xi$$

$$v_h = \mu_h \xi$$

- If the concentration of electrons and holes are  $n_i$  and  $h_i$  respectively, then current density for current due to electrons and holes are given by

$$J_e = n_i q v_e$$

$$J_h = n_i q_h v_h$$

$$J_e = n_i q \mu_e \xi$$

$$J_h = n_i q_h \mu_h \xi$$

$$J_e = \sigma_e \xi$$

$$J_h = \sigma_h \xi$$

Where  $q$  = charge of electron and hole =  $1.602 \times 10^{-19}$  C

$\sigma_e$  = **Conductivity of the semiconductor due to electrons.**

And  $\sigma_h$  = **Conductivity of the semiconductor due to holes.**

Total current density

$$J = J_e + J_h$$

$$J = n_i q \mu_e \xi + n_i q_h \mu_h \xi$$

$$J = (\mu_e + \mu_h) n_i q \xi$$

Where  $\sigma$ , i.e., the conductivity of the semiconductor in units of 'Ohm per centimeter' ( $\Omega \text{ cm}$ ) $^{-1}$  is given by

$$\sigma = (\mu_e + \mu_h) n_i q$$

substituting

$$J = \sigma \xi \quad \dots\dots(6)$$

**It may be noted that Eq. 6 is nothing but another representation of Ohm's Law.**

### Diffusion Current: -

- The term Diffusion Current is applicable only to semiconductors.
- Diffusion current is proportional to the concentration gradient of electrons.

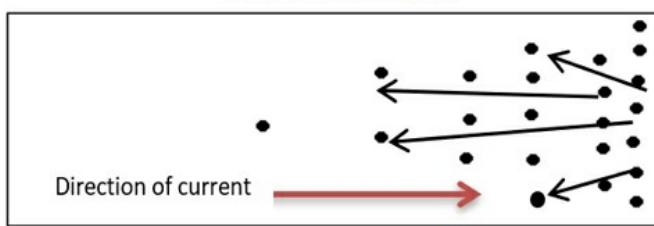
$$J_e \propto -q \frac{dn}{dx}$$

The constant of proportionality is the '**Diffusion Constant**',  $D_e$

Thus, Current Density due to diffusion of Electrons

$$J_e = q D_e \frac{dn}{dx}$$

ELECTRON DIFFUSION



Electrons diffusing from region of high concentration to the region of low concentration resulting in Diffusion Current in the opposite direction.

**Fig.- 8: - Diffusion Current in semiconductors**

$$V_T = \frac{kT}{q} \quad \dots(7)$$

Where  $k$  = Boltzmann Constant =  $1.381 \times 10^{-23} \text{ J}/\text{K} = 8.62 \times 10^{-5} \text{ eV}/\text{K}$ .

$T$  = Room Temperature in  $^{\circ}\text{K}$ .

$q$  = Charge of the electron =  $1.602 \times 10^{-19} \text{ C}$

Substituting these constants and assuming room temperature of  $300^{\circ}\text{K}$

$$V_T = \frac{T}{11600}$$

$$V_T = \frac{300}{11600} = 0.02586 \text{ V or } 26 \text{ mV} \quad \dots(8)$$

**NOTE:** - To be noted that in case of semiconductors, in any given instant of time there will either be the diffusion of electrons only, or diffusion of holes only, but not both together. This is unlike Drift Current, which is caused by drift of electrons as well as holes, together.

## 1.6 Silicon and Germanium

On the basis of the discussion above, the comparison of silicon and germanium may be summarized in a table as follows-

**Table- 3:** Comparison of the physical properties of Ge & Si.

Property	Germanium	Silicon
Atomic Number	32	14
Atomic Weight	72.6	28.1
Density of packing of atoms in crystal ( Atoms/cm <sup>3</sup> )	$4.4 \times 10^{22}$	$5.0 \times 10^{22}$
Energy Gap $E_g$ at $300^{\circ}\text{K}$ ( eV )	0.72	1.1
Energy Gap at $0^{\circ}\text{K}$ $E_{g0}$ ( eV )	0.785	1.21
Intrinsic Concentration at $300^{\circ}\text{K}$ $n_i$ ( cm <sup>-3</sup> )	$2.5 \times 10^{13}$	$1.5 \times 10^{10}$
Intrinsic Resistivity at $300^{\circ}\text{K}$ ( $\Omega\text{-cm}$ )	45	2,30,000
Mobility of Conduction Band Electrons $\mu_e$ ( cm <sup>2</sup> /V-sec )	3,800	1,300
Mobility of Valence Band Holes $\mu_h$ ( cm <sup>2</sup> /V-sec )	1,800	500
Diffusion Constant of Conduction Band Electrons $D_e = \mu_e V_T$ ( cm <sup>2</sup> /sec )	99	34
Diffusion Constant of Valence Band Holes $D_h = \mu_h V_T$ ( cm <sup>2</sup> /sec )	47	13

## 1.7 Extrinsic Semiconductor

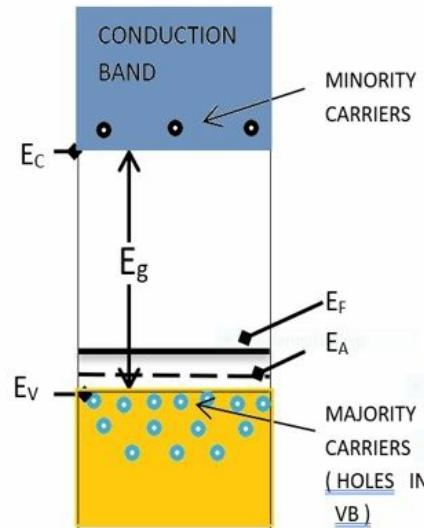
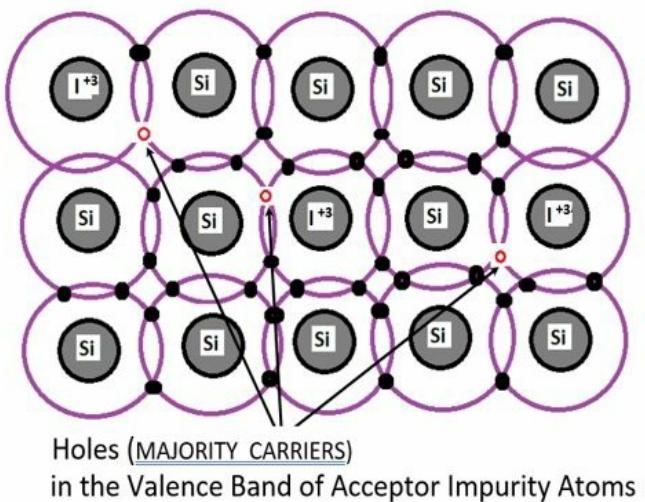
## P-Type Extrinsic Semiconductor

### and Acceptor Impurity

- When a pure crystal of silicon or germanium is doped with a **trivalent** element such as boron (B), gallium (Ga) or indium (In), we have a **P-type extrinsic semiconductor** and the added impurity element is called an **Acceptor Impurity**.
- Since these impurity atoms are ‘Trivalent’ they are shown as “**I<sup>+3</sup>**” in Fig – 9 below.
- In an intrinsic crystal of silicon, the atoms are bound by covalent bonds. Four electrons of the central atom share one electron each from its four neighbours. In this type of bonding the valence shell of each atom will have 8 electrons, so that the bond is chemically stable.
- But, when a **tetravalent** silicon atom bonds with a **trivalent** impurity atom, one of the covalent bonds with the **I<sup>+3</sup>** impurity atom will have **one electron less**. This vacancy of an electron is nothing but a **Hole**.

### Majority Carriers and Minority carriers

- Holes created due to Doping with Acceptor impurity are the **Majority Carriers**. Since holes are equivalent positive charges, this type of extrinsic semiconductor is called “**P-type**”.
- The intrinsic effect also occurs in the extrinsic semiconductor. Due to this some electron-hole pairs are created. Among these, electrons in the Conduction Band are the **Minority carriers**.
- The ‘Fermi Level’ denotes the average energy level of the carriers in the crystal. Since the majority carrier holes are in the valence band, the Fermi Level is nearer to the Valence Band.
- Since the hole has the property of ‘Accepting’ free electrons, the trivalent impurity atom contributing the hole in the P-type semiconductor is called an “**Acceptor Impurity**”.



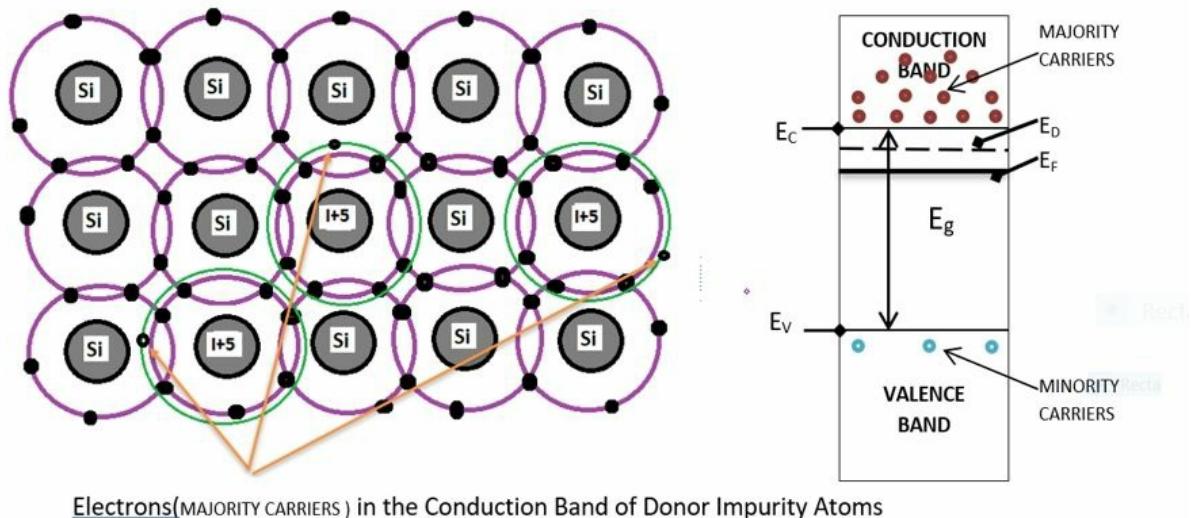
**Fig.-9:** - Formation of **p-type extrinsic semiconductor due to doping by trivalent impurity  $I^{+3}$  (Acceptor Impurity) and Energy Band Diagram.**

## N-type Extrinsic Semiconductor and Donor Impurity

- When a pure crystal of silicon or germanium is doped with a **pentavalent** element such as Phosphorus (P), Antimony (Sb) or Arsenic (As), we have a **N-type extrinsic semiconductor** and the added impurity element is called a **Donor Impurity**.
- Since these impurity atoms are “Pentavalent” they are shown as “ $I^{+5}$ ” in the Fig – 10 below.
- In the covalent bonding between the silicon and the pentavalent impurity atoms, 4 electrons each from the atoms are involved, so that the valence shell of each atom is chemically neutral, with 8 electrons. The **5<sup>th</sup> electron** of the pentavalent impurity atom has to move to a higher shell of the Conduction Band.
- Thus, the covalent Band of the N-type silicon crystal gets filled a large number of free electrons.

### Majority Carriers and Minority carriers

- These free electrons created due to Doping with Pentavalent impurity are the **Majority Carriers**. Since electrons are the majority carriers, this type of extrinsic semiconductor is called “**N-type**”.
- Due to intrinsic effect some electron-hole pairs are created. Among these, holes in the Valence Band are the **Minority carriers**.
- Since the majority carrier are free electrons of the conduction band, the Fermi Level is nearer to the Conduction Band.
- Since the pentavalent impurity has created the majority carriers by ‘Donating’ its electrons, hence it is called a “**Donor Impurity**”.



**Fig.-10:** - Formation of *n*-type extrinsic semiconductor due to doping by pentavalent impurity  $I^{+5}$  (Donor Impurity). And the Energy Band Diagram.

### Carrier concentration in Extrinsic Semiconductor

- Mass Action Law stated that the product of the concentrations of free electrons ' $n_i$ ' and holes ' $h_i$ ' in an intrinsic semiconductor is a constant equal to  $n_i^2$  (Eq-4).
- This relationship is valid for extrinsic semiconductors as well.
- Recall that in an extrinsic semiconductor, introduction of each dope atom results in the creation of one majority carrier. Neglecting the additional majority carriers generated by Intrinsic Effect, we

can assume that --

**Majority carrier concentration equals the concentration of doping.**

$$n_n \approx N_D \quad \text{AND} \quad h_p \approx N_A$$

- Now, Mass Action Law for a N-type semiconductor will take the form

$$n_n \cdot h_n = n_i^2$$

The subscript 'n' indicates that the quantities  $n_n$  and  $h_n$  represent concentration of **majority carrier electrons and minority carrier holes**, in the N-type semiconductor.

Substituting  $n_n = N_D$

$$h_n = n_i^2 / N_D \quad \underline{\dots\dots}(9)$$

- And, Mass Action Law for a P-type semiconductor will take the form

$$h_p \cdot n_p = n_i^2$$

The subscript p indicates that the quantities  $n_p$  and  $h_p$  represent concentration of **majority carrier holes and minority carrier electrons**, in the p-type semiconductor.

Substituting  $h_p = N_A$

$$n_p = n_i^2 / N_A \quad \underline{\dots\dots}(10)$$

**Example 2:** - Calculate the concentrations of electrons and holes in a n-type Si crystal which is doped with a donor concentration of  $10^{17}$  per  $\text{cm}^3$ . Assume thermal equilibrium conditions at  $300^\circ\text{K}$ .

**Solution:** Since this is a n-type crystal, we have

$$n_n \approx N_D = 10^{17} \text{ cm}^{-3}$$

This is the concentration of Majority Carrier electrons.

From Eq. 9 we have the concentration of holes (Minority Carriers) as

$$h_n = n_i^2 / N_D$$

From Table 3 the value of the constant  $n_i$  for Si is  $n_i = 1.5 \times 10^{10}$

Substituting

$$h_n = \frac{(1.5 \times 10^{10})^2}{10^{17}} = 1.5 \times 10^3$$

**Example 3.:** - Calculate the concentrations of holes and electrons in a P-type Ge crystal which is doped with a donor impurity concentration of  $10^{20}$  per  $\text{cm}^3$ . Assume thermal equilibrium conditions at  $300^\circ\text{K}$ .

**Solution::** Since this is a n-type crystal, we have

$$h_p = N_A = 10^{20} \text{ cm}^{-3}$$

This is the concentration of Majority Carrier holes.

From Eq. 10 we have the concentration of electrons (Minority Carriers) as

$$n_p = n_i^2 / N_A$$

From Table 3 the value of the constant  $n_i$  for Ge is  $n_i = 2.5 \times 10^{13}$

Substituting

$$n_p = \frac{(2.5 \times 10^{13})^2}{10^{20}} = 2.5 \times 10^6$$

### OBSERVATIONS:

1. It is observed that the concentration of the “minority Carrier” holes in the N-type semiconductor crystal is negligible compared to the concentration of the “Majority Carriers”. The same is true for the P-type semiconductor crystal.
2. Minority Carrier Concentration in Si is  $10^{-3}$  times less than

**that of Ge. In other words, Si forms a much better Extrinsic Semiconductor compared to Ge. That is the reason why Si is the preferred material in the electronics industry.**

## 1.10 HALL EFFECT

- If any conductor carrying current ‘I’ is placed in a transverse magnetic field ‘B’ then an electric field ‘ $\xi$ ’ is induced in the direction perpendicular to both I and B. This is known as Hall Effect.
- Hall Effect can be observed in both Intrinsic and Extrinsic Semiconductors. In fact, Hall Effect is used to determine whether a semiconductor is N-type or P-type or intrinsic.
- In extrinsic semiconductors, the Hall Effect can be used to determine majority carrier concentration, conductivity and mobility of the carriers.

### Principle

- Consider a piece of semiconductor of thickness ‘d’ and width ‘w’. Let a current ‘I’ flow through it and let it be placed in a transverse magnetic field ‘B’, as shown in the Fig.- 11, below.

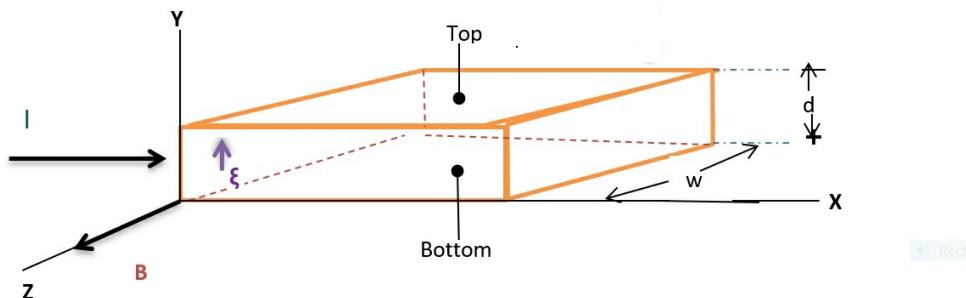


Fig. - 11

- If this semiconductor is of N-type then the current is due to the majority carrier electrons. By Fleming’s Left-Hand Rule, the electric field  $\xi$  is in the direction as shown in the figure. Hence, the

negative charged electrons will concentrate towards the bottom side of the semiconductor piece.

The potential developed due to this electric field over the thickness of the semiconductor is given by  $V_H$ . This is called '**Hall Voltage**'.

$$V_H = \xi \cdot d$$

- This electric field exerts a force equal to  $\xi \cdot q$  on the electron, where  $q$  is the charge of the electron. A moving electron in a magnetic field also experiences a force equal to  $B \cdot q \cdot v$ , where  $v$  is the average drift speed of the electron. At equilibrium these two forces must balance each other, hence we have

$$\xi \cdot q = B \cdot q \cdot v$$

$$\therefore \xi = B \cdot v$$

- Now, current density ' $J$ ' in the semiconductor, defined as current per unit cross sectional area. This is given by

$$J = \rho \cdot v = I / w \cdot d$$

$$\therefore v = J / \rho$$

where,  $I$  is the current,

$\rho$  is the density of charge,

(in this case, density of the negative charge due to the electrons),  
 $w$  and  $d$  are the width and thickness of the semiconductor piece as shown in the figure.

$$\therefore V_H = \xi \cdot d = B \cdot v \cdot d$$

$$V_H = B \cdot J \cdot d / \rho$$

$$\therefore V_H = B \cdot I / \rho \cdot w \quad \dots \dots (11)$$

- By measuring  $V_H$ ,  $B$ ,  $I$  and  $w$  we can calculate the **charge density** ' $\rho$ '. Having calculated  $\rho$ , the **electron density** ' $n$ ' in the N-type semiconductor will be

$$n = \rho / q \quad \dots \dots (12)$$

- Again, **conductivity** ' $\sigma$ ' in a substance in terms of mobility of carriers, ' $\mu$ ' is given by

$$\sigma = \rho \cdot \mu \quad \dots \dots (13)$$

- From this the mobility of electrons in the semiconductor can be calculated.

We have another quantity known as '**Hall Coefficient**' ' $R_H$ ', defined as reciprocal of charge density

$$R_H = 1 / \rho$$

Using Eq. (11) we have

$$R_H = V_H \cdot w / B \cdot I$$

Thus, mobility will be given by

$$\mu = \sigma \cdot R_H \quad \dots \dots (14)$$

- The foregoing is in terms of a N-type extrinsic semiconductor. The very same explanation will hold true for P-type extrinsic semiconductor also. However, when the majority carriers are holes, the Hall Effect will push the holes to the top surface instead of the bottom surface. Therefore the direction of the electric field  $\xi$  and the polarity of  $V_H$  will be opposite.
- If the piece of semiconductor is intrinsic then the intrinsic hole-electron pairs will be very small in number. Since the number of holes and electrons is equal the quantity Hall Voltage  $V_H$  will be zero.
- **Hall Effect is utilized in a number of electronic devices that**

**find widespread application in Instrumentation Engineering and Microwave Engineering.**

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# **UNIT - 1**

## **THE P-N JUNCTION DIODE AND APPLICATIONS OF DIODES**

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### **CHAPTER - II**

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## **THEORY OF P-N JUNCTION**

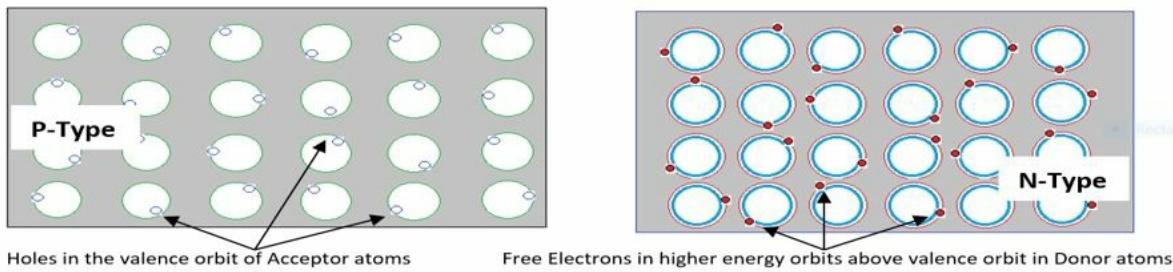
*THEORY OF P-N JUNCTION*

### **INTRODUCTION**

- A **P-N junction** is the physical union of a P-type Semiconductor with a N-type Semiconductor.
- The P-N junctions form the backbone of the Electronics Industry and are found in all Semiconductor Based Electronic Devices.
- The single P-N junction functions as the Diode, which is primarily used to convert AC into DC.
- The **Bi Junction Transistor** is composed of two P-N junctions. It is used for amplifying and switching,
- Heavy Duty Power Control Equipment, that are capable of handling Mega-Watts of Electrical Power, are devices composed of three P-N junctions. This family of electronic devices is called **Thyristors**.
- A **Logic Gate** is a circuit consisting of a number of switching transistors. Logic Gates in various combinations make various types of Digital Processors.
- Some aspects of the theory of operation of the P-N Junction can be explained by the Carrier Injection Model, and some others by means of the Energy Band Model. Together, they fully explain the functioning of the device.

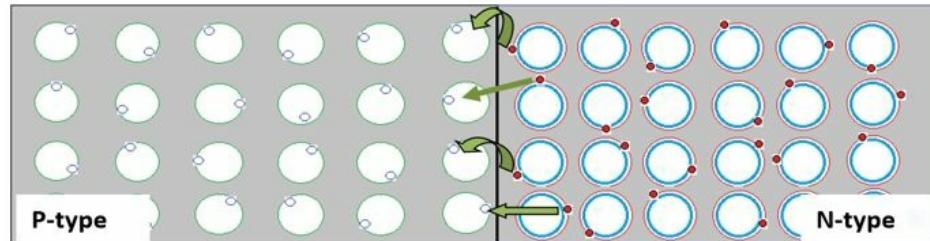
## **2.1 THEORY OF THE P-N JUNCTION: P-N Junction in Equilibrium Condition**

- When two chunks of P-type material and N-type material are not in contact we have the following situation depicted in Fig. – 1. The majority carriers of each material are not affected.



**Fig- 1:** - Holes are present in the valence shells of the Acceptor Atoms, this constitutes the Valence Band (VB) in P-Type material. Free Electrons are present in the higher energy shells of the Donor Atoms of the N-Type material. This constitutes the Conduction Band (CB).

- When the p-type and n-type material are joined in a junction, we have a situation as depicted in Fig.-2.
- Free Electrons of the Conduction Band in the n-type material are at a higher energy level and the Holes in the Valence Band of the p-type material are at a lower energy level. These free electrons are attracted by the hole lying at a lower energy level.



**Fig- 2:** - **Movement of Majority Carriers across the junction.** Free Electrons of the higher energy Conduction Band (CB) shells from N-Type material migrate across the junction and fill up holes in the lower energy Valence Band (VB) shells in the P-Type material.

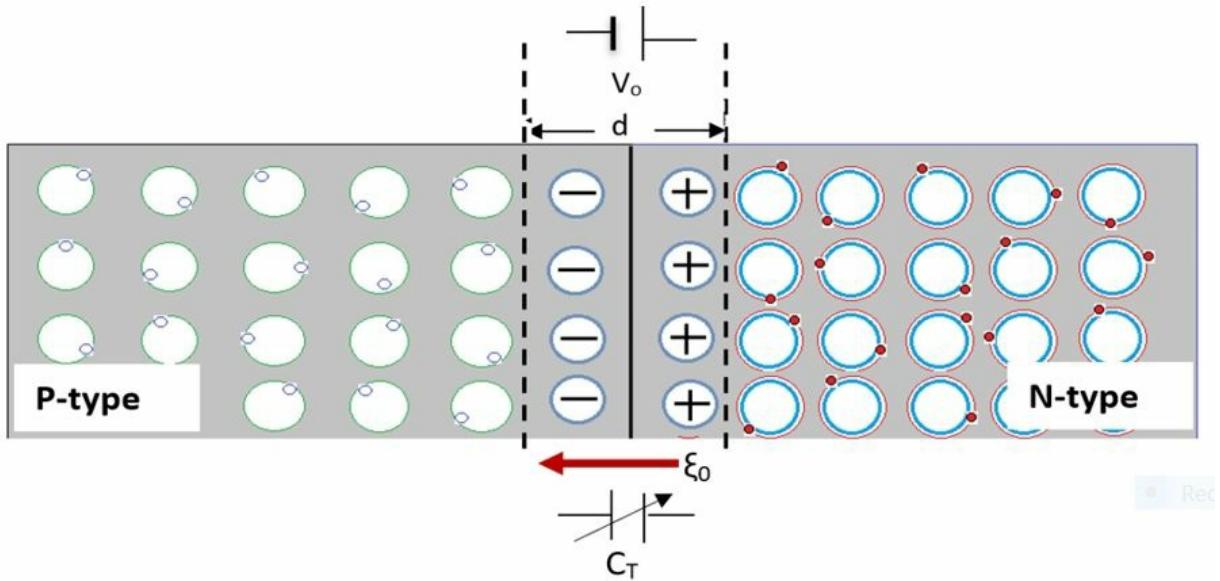
- Recall that the Majority Carriers of an extrinsic semiconductor occur at the respective impurity atoms. When an electron from a donor impurity atom of the N-type material migrates to the other

side, that donor impurity atom becomes a Positive Ion. Similarly, the acceptor impurity atom of the P-type that accepts this migrated electron, becomes a Negative Ion.

- Thus, a layer of Positive ions forms on the boundary of the N-type material, and another layer of Negative ions forms on the boundary of the P-type material.
- The negatively charged boundary layer prevents further movement of free electrons across the junction, from the N-type region to the P-type and the positively charged boundary layer prevents any further migration of holes across the junction. **Thus, there is no current flow at equilibrium.**
- The details of the occurrences at the P-N Junction at equilibrium is depicted in the Fig.- 3.

### **The Depletion Region: -**

- Since this region at the boundary of the P-N Junction has been **depleted** of majority carriers, and hence it is called the **Depletion Region**. The Depletion Region is also variously known as –
  1. **Space Charge Region**
  2. **Barrier Region**
  3. **Transition Region**
- **Thickness of the Depletion Region ‘d’:** - Since the space Charge Region is entirely due to the Doping Atoms, **the width of this region is inversely proportional to the Doping Density or Doping Concentration.** The higher the concentration of doping the narrower the Depletion Region and vice-versa.



**Fig- 3: - P-N Junction at equilibrium.** Movement of the free electrons from the CB orbits of the neutral Donor atoms of N-Type material across the junction to fill up Holes of the VB orbits of the neutral Acceptor atoms of P-Type material has created the layer of positive and negative ions on opposite sides of the junction. This region of static ions is variously called as (a) **Depletion Region**, (b) **Barrier Region**, (c) **Transition Region** or (d) **Space-Charge Region**.

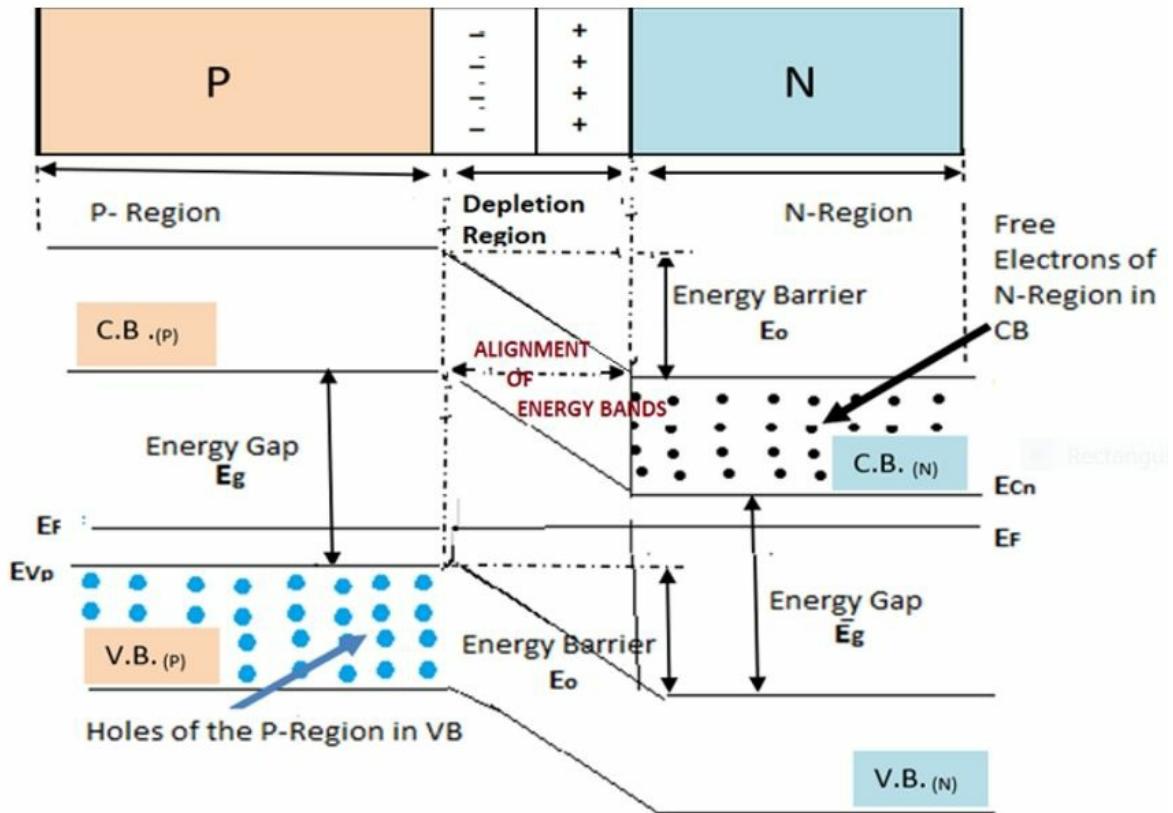
- **Barrier Potential ‘ $V_0$ ’:** - The layer of positive and the negative ions repel any electron or hole trying to diffuse across the P-N Junction. The potential difference between these two charged layers is called **The Barrier Potential ‘ $V_0$ ’**. **The magnitude of  $V_0$  for Si, 0.7 V, and in Ge 0.3 V** (Assuming Room Temperature of  $300^0$  K).
- **Barrier Electric Field ‘ $\xi_0$ ’:** - The Barrier potential  $V_0 = dV$  is between the charged layers. These two layers are separated by a distance  $d = dx$ . Thus, there exists an internal Electric Field  $\xi_0 = dV / dx$ . This Electric Field Vector is oriented from positive potential to negative potential. This internal electric field is called **the Barrier Electric Field ‘ $\xi_0$ ’**.
- The orientation of  $\xi_0$  and polarity of  $V_0$  is such that it prevents any further crossing of majority carriers across the junction at equilibrium. The Barrier Electric Field pushes away majority carriers respectively, of the N and the P regions from the junction.

**Thus, there is no current flow at equilibrium.**

- **Transition Capacitance  $C_T$ :** - The two layers of Space Charge have a layer of Intrinsic Si between them. Intrinsic Resistivity of Si is  $2.3 \times 10^5 \Omega\text{-cm}$ . This can be approximated as an insulator. This results in a Capacitance in the Transition Region, called **Transition capacitance  $C_T$** . Under Reverse Bias condition, the thickness ‘d’ of the depletion region is proportional to the Reverse Bias. Thus,  $C_T$  is inversely proportional to Reverse Bias. Hence it is shown as a variable capacitance in the Fig-3.

## **2.2 Energy Band Diagram of P-N Junction at Equilibrium: -**

- ❖ At equilibrium condition, some free electrons from conduction band of the donor atoms of N-side of the crystal migrate to the P-side. Due to this, the energy bands of the n part lose some energy and both the C.B. and the V.B. of this part **slide down together** by a certain amount of energy levels, while keeping the Energy Gap constant at  $E_g$ .
- ❖ On the other hand, the acceptor atoms of the p-side gain one electron each. Due to this, the energy bands on the p-side of the crystal gain energy and both the V.B. and the C.B. energy levels **slide up** by the same amount of energy levels, keeping  $E_g$  constant. This is depicted in Fig.-4.



**Fig.- 4:** - Energy Band Diagram of P-N junction at equilibrium. Both the C.B. and the V.B. of P-Type are at higher energy levels compared to the corresponding energy bands of N-Type, separated by Energy Barrier  $E_0$ .

- ❖ In this process an “**Energy Barrier**” is created between the p-side and the n-side, in the Depletion Region (Transition Region). Energy Barrier is shown as “ $E_0$ ”. This energy barrier is equal in both the C.B. and

the V.B. The existence of this Energy Barrier prevents the flow of majority carriers across the junction at equilibrium.

- ❖ **Fermi Energy level  $E_F$** , signifies the probability of existence of electrons in a semiconductor crystal. Individually, in the P-Type crystal, the Fermi Level  $E_F$  is very near to  $E_{VP}$ . In the N-Type crystal, the position of  $E_F$  is very near to  $E_{CN}$ . At equilibrium,  $E_F$  of the composite P-N crystal must be at a constant level. Therefore,

the energy bands of the N-type and P-type materials must align so that the lowermost energy levels of both VB and CB of the P-type material gets aligned with the uppermost energy level of the corresponding bands of the N-type material. This is another explanation for the existence of an Energy Barrier or Energy Gradient  $E_o$ .

- ❖ **The numerical value of Barrier Potential  $V_0$  equals the Energy Barrier  $E_o$  for a given semiconductor material.** For example, at  $300^0\text{K}$ , Barrier Potential  $V_0$  for Si equals 0.7 V and Energy Barrier  $E_o$  equals 0.7 eV. In case of Ge Barrier Potential  $V_0$  equals 0.3 V and Energy Barrier  $E_o$  equals 0.3 eV.
- ❖ **There is another interesting relationship. The Energy Barrier is 0.3 eV less than the Energy Gap “ $E_g$ ” of the semiconductor material. This is true for both Si and Ge, as well as for alloy semiconductors, Ga As. (GaAs based alloy semiconductors are used for manufacturing LED and LD).**

## 2.3 P-N Junction at Forward Bias

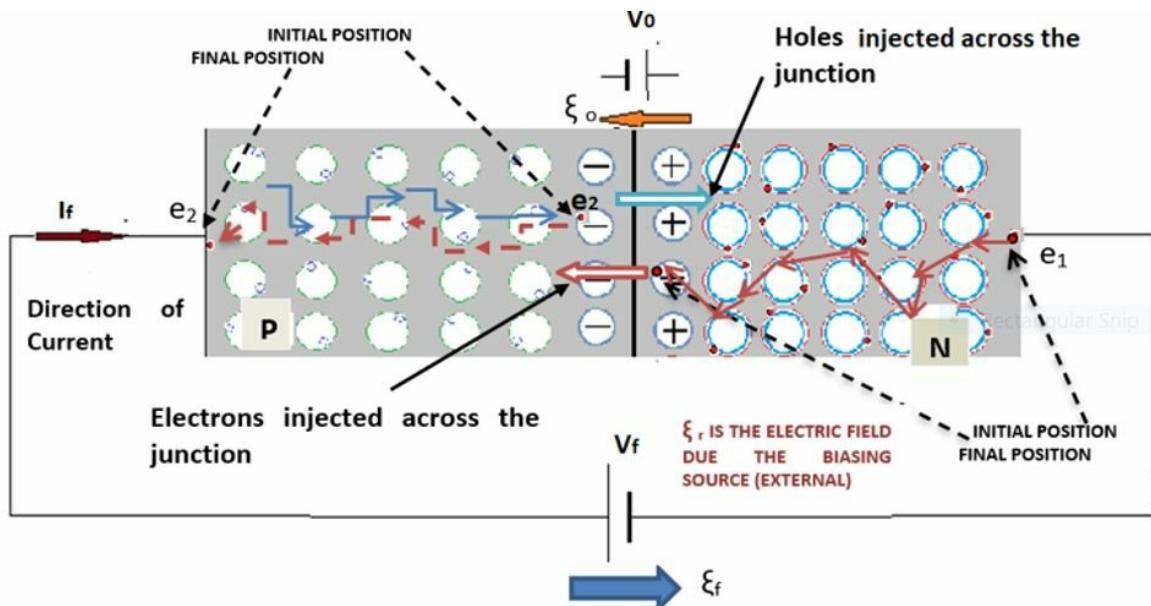
### Current Flow in P-N Junction

#### (By Carrier Injection Theory)

- A **Forward Bias** is defined as the condition when an external DC Potential “ $V_f$ ” is applied, so that the **positive terminal of the bias source is connected to the ‘p-side’ and the negative terminal to the ‘n-side’**. In this condition a current flow is set up in the P-N Junction. This current is primarily due to majority carriers and it flows from the p-side to the n-side. This is called the “**Forward Current**”, denoted by “ $I_f$ ”.
- When a Forward Bias is applied, the applied external potential  $V_f$  and the associated Electric Field  $\xi_f$  are opposing the Barrier Potential  $V_0$  and the Barrier Electric Field  $\xi_0$ , respectively. **Hence net Barrier Potential as well as net Electric Field, both decreases.**
- Some of the Space Charges get neutralized by the applied external potential and, thus **width of the depletion region decreases**.
- **The Net Electric Field  $\xi'$  is oriented from P towards N.** Thus, it

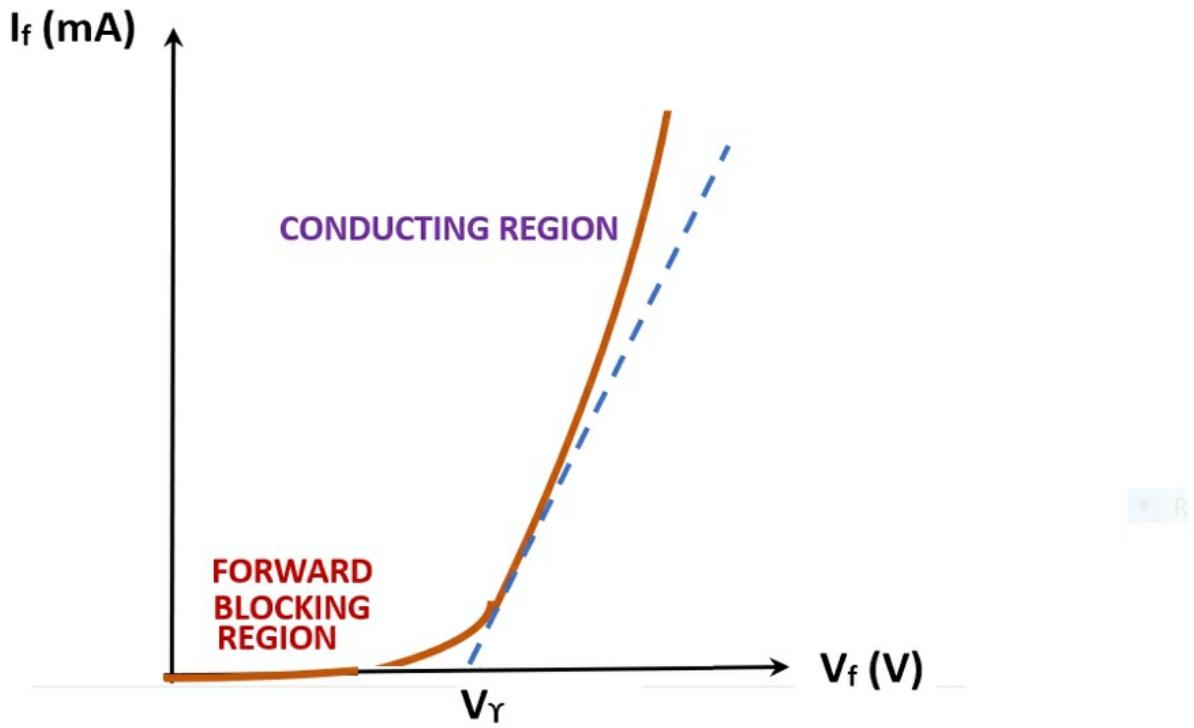
pushes (injects) the holes (i.e., +ve charges) of the P-region into the N-region and electrons (i.e. -ve charges) of the N-region into the P-region. These oppositely charged carriers are moving in opposite directions. Together, they give rise to the current  $I_f$ . Since current flow is defined as the direction of positive charge flow, and opposite to the direction of negative charge flow, the **direction of  $I_f$  is from P to N**. This is elaborated further in Fig.-5.

- Consider the free electron “ $e_1$ ” in the n-type material. This will be repelled by the negative pole of  $V_f$  and set into a random drift motion towards the junction. This is shown by the **solid red arrows**. As soon as it reaches the junction, it will neutralize a positive ion at the depletion region. This will result in the reduction of the width of the depletion region. Since a Space Charge has been neutralized, the **net Barrier Potential** also decreases. Now, this electron will come into the influence of the electric field “ $\xi_f$ ”. This electric field will “inject” these electrons into the p-type material. Injected electrons will now **diffuse** through the P-type material towards the positive terminal and set up the ‘**electron current**’.



**Fig. - 5.: - Injection of Majority Carrier Electrons and Holes across the junction due to Forward Bias. The Polarity for Forward Bias and Direction of Forward Current.**

- Now consider a valence band electron “ $e_2$ ” in a negative ion at the p-type material on the junction. This will be attracted by the positive polarity of  $V_f$ , and will move in a random drift motion, as shown by the **broken red** arrow in the p-type material. As negative ion loses an electron, it is neutralized. This amounts to reduction of the width of the depletion region. This electron will progressively fill up the holes in its path, while leaving behind a hole in its previous atom. **This is equivalent to the movement of a hole in the opposite direction.** The movement of the hole is shown by the **solid blue** arrows. As soon as the hole reaches the junction, it will be “injected” into the n-type material by the electric field “ $\xi_f$ ”. The injected hole will now diffuse through the n-type material and set up the ‘**hole current**’.
- This flow of holes (+ve) and electrons (-ve) add up to give rise to the Forward Current  $I_f$ . This current flows in the direction from P towards N. **Thus,  $I_f$  is due to the process of the majority carrier injection across the junction.**
- **The applied potential  $V_f$  and resulting current  $I_f$  follow an exponential relationship.** At smaller values of  $V_f$  the current  $I_f$  is of the order of  $\mu A$  and the rate of increase of  $I_f$  w.r.t.  $V_f$  is also very small. Since the current across the P-N Junction is negligible during this, the corresponding region of the V-I Characteristic is called the “**Forward Blocking Region**”.



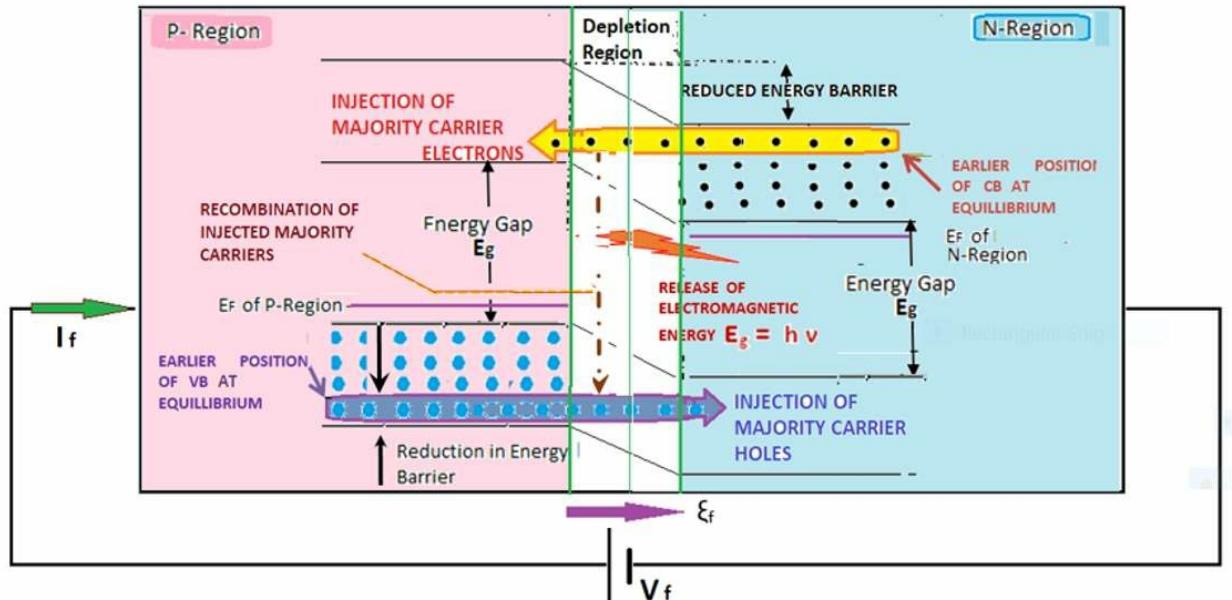
**Fig. - 6.:=** *V-I Characteristic of P-N Junction at Forward Bias.*

- As the Forward Bias **increases beyond a Limiting Value  $V_Y$** , the Barrier Potential completely is overcome (Barrier Potential  $V_0$  equals Threshold Voltage  $V_Y$ ). The Depletion Region disappears and Forward Current begins to rise very sharply. Thus, this region of the V-I characteristic represents current conduction. Accordingly, this region is called the "**Forward Conducting Region**".
- In order to make a PN junction fully conducting, applied **Forward Bias  $V_f \geq V_Y$** . This quantity  $V_Y$ , is called either **(a) Threshold Voltage, or (b) Cut-in-Voltage, or (c) Knee Voltage**.
- **$V_Y$  is nothing but the Barrier Potential  $V_0$  of the Equilibrium Condition**. Thus, in case of Si Threshold Voltage  $V_Y = 0.7$  V; in case of Ge Threshold Voltage  $V_Y = 0.3$  V.

## 2.4 Current Flow in P-N Junction (By Energy Band theory)

## **Forward Bias**

- In Equilibrium Condition, Energy Barrier  $E_0$  and the Barrier Electric field  $\xi_0$  prevented the movement of majority carriers. When an external Forward Bias is applied, the energy levels of the N-type material gain some energy from the bias source and consequently, they slide up a few levels. At the same time, the energy levels of the P-type material lose the same amount of energy and they slide down by the same amount. As a result, the Energy Barrier will be reduced. This is depicted in the Fig.- 7.



**Fig- 7:** - Application of Forward Bias results in the re-alignment of the Energy Bands in such a way that the Energy Bands of the N-Region slide upwards and those of the P-Region slide downwards. This results in the reduction of Energy Barrier. The orientation of the Net Electric Field upon the application of Forward Bias is in the direction from P towards N. This results in the injection of majority carriers as shown by the respective arrows (Blue for Hole injection and Red for Electron Injection), which results in current  $I_f$  in the direction from P towards N.

- Due to the reduction of Energy Barrier, some of the CB Electrons of the N-side, on the uppermost layer of the band (shown yellow shaded) are now aligned above the lowermost energy level of the CB of the P-side. Similarly, some of the VB holes of the P-side, on the lowermost layer of the band (shown blue shaded) are now lying below the uppermost energy level of the VB of the N-side. These electrons and holes are not confronted by the Energy Barrier.
- Since the net Electric Field  $\xi'$  at the junction is oriented from P-towards-N, these electrons and holes are forced into the respective opposite sides. This results in the current  $I_f$ .
- As the Forward Bias is increased, the Energy barrier ' $E_0$ ' is further reduced, resulting in a gradual exponential increase of current. At a certain value of Forward Bias  $V_f = V_Y$  (Where  $V_Y$  equals the

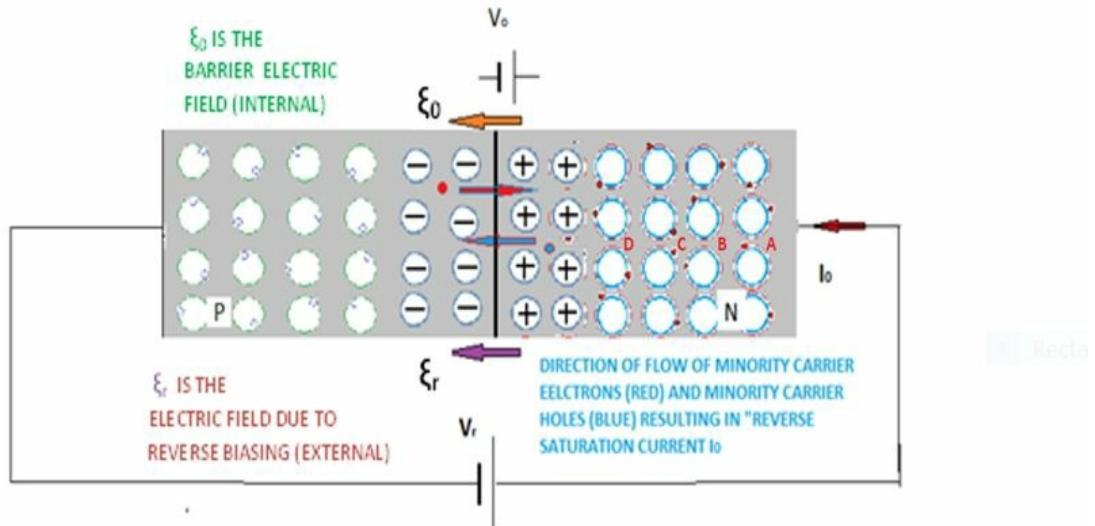
Barrier Potential  $V_0$ ), the Energy Barrier is completely overcome. In this situation, the CB and VB of each side P and N respectively, are aligned with each other. In this situation, the exponential rise in the Forward Current  $I_f$  w.r.t.  $V_f$  becomes very sharp.

- Carriers injected across the junction become the Minority Carriers on the other side. In an Extrinsic Semiconductor Minority Carriers are quickly neutralized by the opposite type of carriers.
- This process of neutralization results in transition of an electron from a higher energy CB level to a lower energy VB level. This will result in the release of a quanta of electromagnetic energy equal to the Band Gap Energy  $E_g = h v$ . Thus, any PN junction operating at forward bias will release electromagnetic energy. In P-N junctions made of Si or Ge this energy is released in the form of Heat. In PN junctions made of alloys of GaAs, energy is released in the form of infra-red or visible light. (GaAs diodes are the LED).
- On the basis of the discussion above, the shape of the V-I Characteristic, shown in Fig.-6, can be explained.

## 2.5 P-N Junction at Reverse Bias

- A **Reverse Bias** on a P-N junction is defined as a DC potential difference  $V_r$  applied across the junction in such a way that the **positive polarity is connected to N and negative polarity to P**. This situation results in the blocking of the flow of Majority Carriers across the junction. However, a negligible current flow due to Minority Carriers.
- The polarity of the external biasing potential  $V_r$  and the electric field  $\xi_r$  associated with the biasing potential are in the **same direction and orientation** as the Barrier Potential  $V_0$  and Barrier Electric Field  $\xi_0$  respectively, as shown in the Fig.- 8. Thus, both the net potential barrier across the junction  $V' = (V_r + V_0)$  and the net barrier electric field  $\xi' = (\xi_r + \xi_0)$  are increased.

- This results in the **increase of the width of the Depletion Region.** The mechanism is as depicted in the Fig.-18.
- The positive terminal of the biasing DC source  $V_r$  sucks out the free electrons from the donor atom ‘A’ of the P-N crystal, lying on the outermost boundary of the N-side. As a result, this atom will become positively charged. Free electrons from the immediate neighbouring donor atom ‘B’ will neutralize this charge, and itself will become positive. This will then pull out the electron from ‘C’ and this way, one-by-one, the donor atoms situated towards the inner portions of the crystal would go on neutralizing the positive charge of its immediate outer neighbor and itself becoming positively charged. Finally, this progression will stop as it reaches the first positive space charge of the depletion region, because this positively charged atom (+ve ion) has no free electron to offer. Thus, the last donor atom to have lost its free electron in neutralizing the immediate neighbor would remain a positive space charge and thus become a part of the depletion region. A similar process of Hole Neutralization takes place on the p-side **resulting in eventual widening of the Depletion Region.**



**Fig.- 8:** - Application of Reverse Bias to P-N junction results in (i) Increase in the width of Depletion Region, (ii) The increase of Barrier Potential (iii) The increase of Net Electric Field at the junction AND (iv) Injection of Minority Carriers across the junction. Direction of injection of Minority carrier electrons is shown with RED arrows and that of Minority carrier holes is shown with BLUE arrows. All of these result in the **Reverse Saturation Current  $I_0$** , in the direction shown above. **This Reverse Saturation Current  $I_0$  is independent of applied Reverse Bias but dependent on ambient temperature and light.**

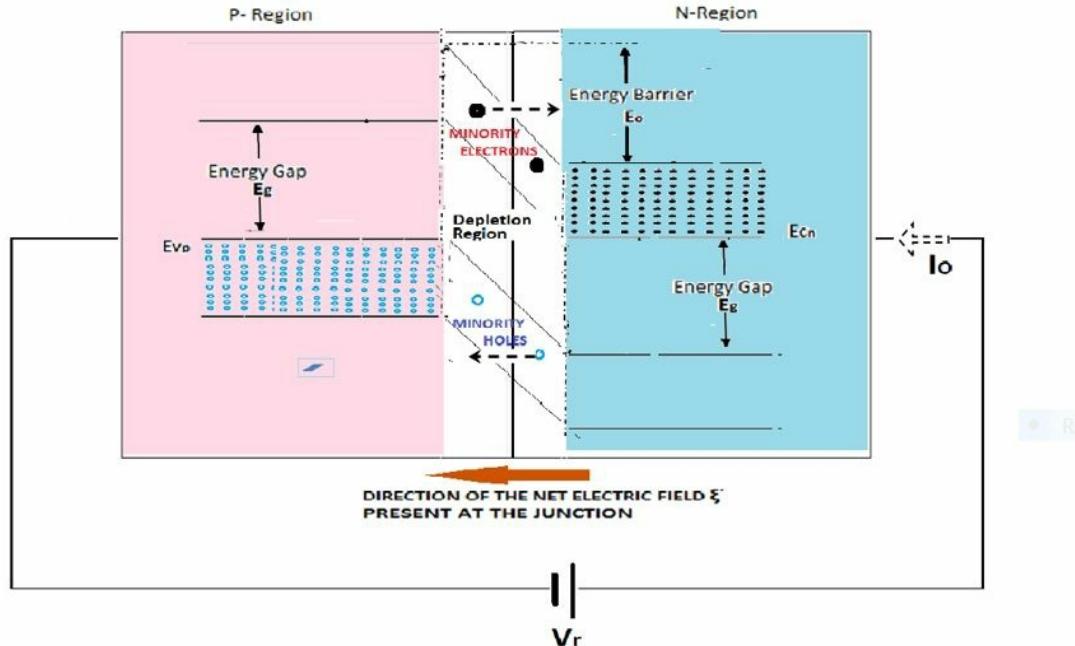
- The width of the depletion region is **directly proportional** to the applied reverse bias and **inversely proportional** to the density of doping (Concentration of impurities) of the p-type and n-type impurities.
- Due to increased Barrier Potential and Barrier Electric Field, the Majority Carriers are prevented from crossing the junction. The process is as explained below.
- The Barrier Potential at **equilibrium itself** was enough to prevent the flow of majority carriers across the junction. At reverse bias condition, the net Barrier Potential is higher than that of the equilibrium value. **Thus, at reverse bias there will be no possibility for current due to majority carriers.**

- **However, a Reverse Saturation Current  $I_0$ .** flows due to Minority Carriers generated within the semiconductor crystal. This flows in the reverse direction, i.e., in the direction from N towards P.
- Minority Carriers are created in the depletion region due to absorption of Thermal Energy from the surroundings (**Intrinsic Effect**). At a constant room temperature, the concentration of Minority Carriers is constant.
- These Intrinsically generated minority carriers will come under the influence of the electric field ‘ $\xi$ ’. The orientation of this field is such that the free electrons of the CB will be pushed into the P-side and the holes in the VB will be pushed into the N-side.
- This flow of minority carriers give rise to a current  $I_0$ , which flows in the direction from N-side to the P-side. The direction of this current is opposite to the majority carrier current due to Forward bias.
- At a constant temperature, the number of intrinsically generated electron-hole pairs is constant. Concentration of Minority Carriers is also independent of the applied reverse bias. Hence the current  $I_0$  is also constant. Hence, it is known as **“Reverse Saturation Current”**.
- If ambient temperature is increased then more minority carriers are created and vice-versa. As an empirical rule, **for every  $10^0\text{C}$  rise in temperature, the concentration of minority carriers increases by a factor of 2 and for every  $10^0\text{C}$  decrease in temperature, decrease by a factor of 2**. This phenomenon is described in Chapter-1.
- Reverse Saturation Current is also specific to a material, as it is dependent on the value of the energy gap  $E_g$  between the Conduction Band and Valence Band of the semiconductor material. If  $E_g$  is more, then more energy will have to be absorbed from the surroundings, and consequently, there is less possibility of creation of intrinsically generated minority carriers and vice-versa. **For example, in Si, in which  $E_g$  equals  $1.1\text{ eV}$ , the magnitude of Reverse Saturation Current  $I_0$  is of the order of nA, whereas in**

**Ge in which  $E_g$  equals 0.7 eV, the magnitude of Reverse Saturation Current  $I_0$  is of the order of  $\mu\text{A}$ .**

### **Energy Band Diagram Of P-N Junction at Reverse Bias**

- When the negative terminal of the DC Biasing Potential Source is connected to the P-side, it **pumps in electrons** into it and neutralize some of the Majority Carrier Holes. Thus, some electrons are introduced into the valence band of the P-Type material. As a result, the **net energy level of the P-side increases**. In other words, CB and the VB of the P-Type material are **lifted upwards** together by a certain number of energy levels. Again, when the positive terminal of the DC Biasing Potential Source is connected to the N-side, it **sucks out** some Majority Carrier electrons. Thus, some **electrons of the CB are neutralized**. As a result, the net energy level of the N-side decreases. In other words, the CB and the VB of the N-Type material are **pushed downwards** together. This is depicted in Fig.-9.



**Fig 9.** Due to the application of Reverse Bias, the energy bands (both CB & VB) of the N-Type material move down and those of the P-Type material move up. Intrinsically generated Minority Carriers produce a “Reverse Saturation Current” ‘ $I_0$ ’. The direction of this current is in the direction from N-towards-P.

- Due to this realignment of the energy bands, the net Energy Barrier  $E_0$  increases. Majority Carriers cannot overcome the Energy Barrier, and hence they cannot cross the junction. Thus, there is no Majority Carrier Current.
- However, due Intrinsic Effect, a few Minority Carriers are generated inside the Depletion region. The Minority Carrier Electrons are **pushed** out by the net Barrier Electric Field  $\xi$  in the direction opposite to its orientation, i.e., into the N-side and the Minority Carrier Holes are pulled along in the direction of the net Barrier Electric Field  $\xi$ , into the P-side.
- This gives rise to the Reverse Saturation Current  $I_0$ , which flows from N-side towards the P-side.

## TUTORIAL - 1

**Example- 1.: -** The Reverse Saturation Current of a diode is measured as 12  $\mu\text{A}$  in an experiential. The room temperature at the time of measurement was  $300^{\circ}\text{K}$ . What will be the magnitude of current at  $320^{\circ}\text{K}$  and  $290^{\circ}\text{K}$ ?

**SOLUTION:** -- Reverse Saturation Current is dependent on Intrinsic Effect.

Given, at  $300^{\circ}\text{K}$ ,  $I_0 = 12 \mu\text{A}$

$\therefore$  At  $290^{\circ}\text{K}$   $I_0$  becomes half, or

$$I_0 = 6 \mu\text{A}$$

And At  $310^{\circ}\text{K}$   $I_0$  becomes double, or  $I_0 = 24 \mu\text{A}$

$\therefore$  At  $320^{\circ}\text{K}$   $I_0$  becomes 4 times of the measure at  $300^{\circ}\text{K}$  of or

$$I_0 = 48 \mu\text{A}$$

**Example – 2.: -** For the measured current of  $12 \mu\text{A}$  in the previous case, how much is the current contributed by the flow of holes?

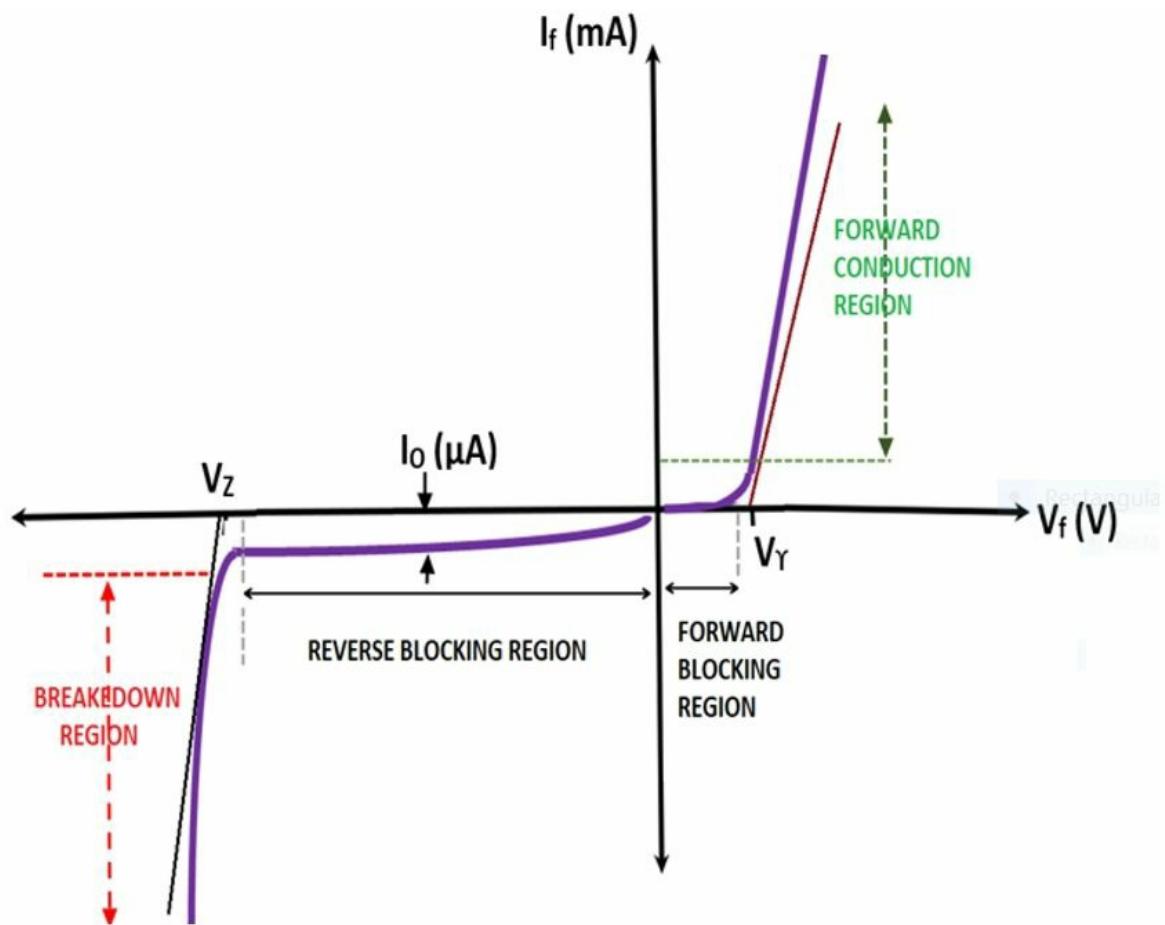
**SOLUTION:** -- Reverse Saturation Current is due to Minority Carriers. There is equal number of electrons and holes as minority carriers. Therefore, half of

the total minority carrier current is due to holes and half due to electrons.

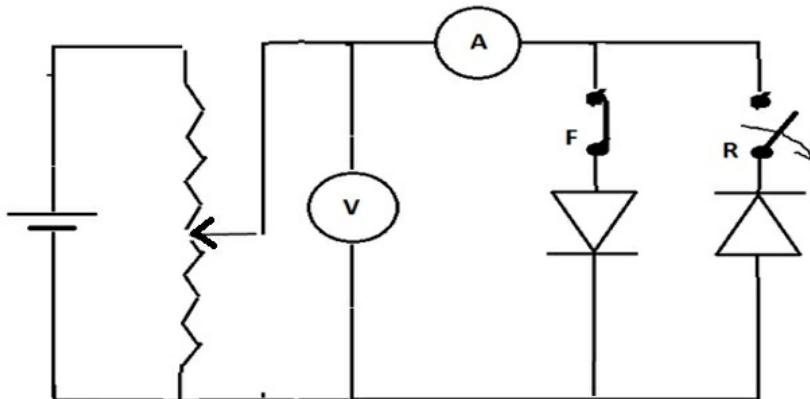
**Therefore, current due to holes is  $6 \mu\text{A}$ .**

### V-I Characteristic of a P-N Junction

Taking into consideration, both the Forward Bias and the Reverse Bias conditions, the variation of current w.r.t the applied bias is shown in the Fig. -10. This can be plotted in the laboratory using a circuit, shown in Fig.-11.



**Fig.-10:** - Complete  $V$ - $I$  Characteristic of a P-N Junction at both Forward Bias and Reverse Bias showing various regions and with typical values of the current and voltage.



Re

**Fig.-11:** - Laboratory circuit for plotting V-I Characteristic of diode. Switch "F" is closed and switch "R" is open for Forward Bias. Whereas, for Reverse Bias the selection of the switches is opposite.

## 2.6 P-N Junction Diode & The Diode Symbol

From our discussion of the P-N Junction we may summarize the few of the salient points as follows –

- ❖ When we apply a Forward Bias, a current will flow due to injection of Majority Carriers across the junction from each side, resulting in a large amount of current flowing in the direction from P-side to N-side as depicted by means of the arrow below



- ❖ When the Forward bias exceeds the quantity  $V_Y$  the current rises very sharply with respect to applied forward bias. The value of Dynamic Resistance is of the order of only a few ohms. This is the Forward Conducting Mode of the diode.
- ❖ Thus, we can say that at Forward bias a current will flow from P towards N and a voltage drop of  $V_Y$  will exist across the device.
- ❖ When we apply a Reverse Bias, current is only due to Minority Carriers and of the order of only few nanoamperes (in case of Si). the dynamic resistance of the P-N junction at Reverse bias is very large, of the order of hundreds of Megaohms. Thus, we can say that at reverse Bias the P-N Junction blocks the flow of current.

This can be depicted as follows --



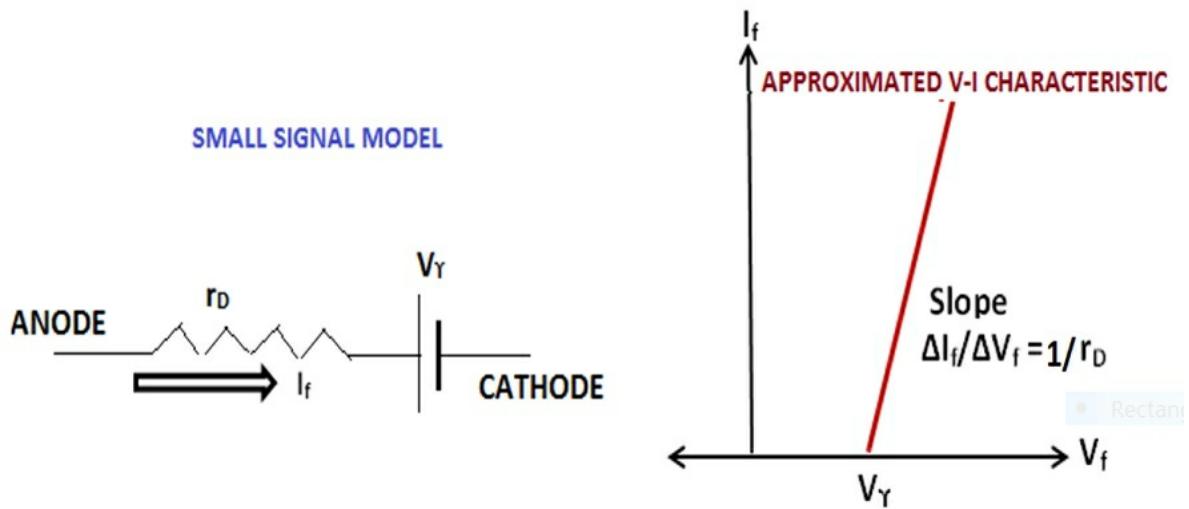
Combining these two depictions Symbol of the device as shown below



**Fig-12:** - The symbol of the DIODE shows that current flow is allowed from P-side (Anode) to N-side (Cathode) while it is blocked in the opposite direction.

## 2.7 Small Signal Model of the Forward Biased Diode (Piece-Wise Linear Model of Diode)

- ❖ It is observed from the graph in Fig.-10, that the Diode begins to conduct only when Forward Bias exceeds the Threshold Voltage  $V_T$ .
- ❖ In the Conduction Region, the slope of the V-I Characteristic is very steep. The reciprocal of the slope of a V-I Characteristic represents the Dynamic Resistance of the device. The reciprocal of the steep graph is very low. This small resistance of the Diode is represented by ' $r_D$ '.
- ❖ With this the Diode can be represented by an Equivalent Circuit and the V-I Characteristic can be approximated as shown in Fig.-13.



**Fig.-13:** - Equivalent Circuit of a Forward Biased Diode. For Ge  $V_Y = 0.3$  V and for Si,  $V_Y = 0.7$  V. The quantity Dynamic Resistance 'r<sub>D</sub>' is of the order magnitude of a few ohms only.

## 2.8 Shockley's Equation

### (P-N Junction Current Equation)

Total current in any semiconductor is always the sum of the current due to electrons and that due to holes.

**Derivation:** ---

Let the current due to the injected holes at the junction, at the point  $x = 0$  be,  $I_{pn}(0)$ . Let the current due to the injected electrons, at the point  $x = 0$  be  $I_{np}(0)$ .

Total Current

$$I = I_{pn}(0) + I_{np}(0) \quad \dots\dots(1)$$

Consider Current due to Holes

- Due to the applied forward bias  $V_f$ , large number of holes will be injected at  $x = 0$ . Increase in Hole Concentration at  $x=0$  is given by an expression known as “**Einstein’s Equation of Carrier Diffusion**” as-

$$p_{n(0)} = p_{no} \cdot e^{(V/V_T)} \quad \dots(2)$$

- a.  $p_{n(0)}$  is the net concentration of holes at the junction at  $x = 0$
- b.  $p_{no}$  is the equilibrium concentration of minority carrier holes in the N-Side
- c.  $V$  = The applied potential difference across the P-N junction
- d.  $V_T$  = The 'Volt Equivalent of Temperature' given by Eq. -7, in Chapter -2 as

$$V_T = \frac{kT}{q}$$

Substituting,

$k$  = Boltzmann Constant =  $1.381 \times 10^{-23} \text{ J/}^\circ\text{K}$ ;

$q$  = Charge of hole =  $+1.602 \times 10^{-19} \text{ C}$

$T$  is the Room Temperature in  ${}^\circ\text{K}$ .

$$V_T = \frac{T}{11600}$$

The increase in the Concentration of Holes due to injection at  $x = 0$  is

$$P_{n(0)} = p_{n(0)} - p_{no} \quad \dots(3)$$

- Injected Holes are Minority Carriers on the N-Side. These Minority Carriers quickly recombine with the Majority Carriers of the opposite side. This is depicted in the Fig.-14 above.

- Concentration of the injected holes  $p_{n(x)}$  in the N-Side begins decrease exponentially.

$$p_{n(x)} = p_{no} - P_{n(o)} \cdot e^{(-x/L_p)} \quad \underline{\dots}(4)$$

$L_p$  is called the “**Diffusion Length**” of injected holes in the N-Side

- Injected holes diffuse into the N-Side. Diffusion Current proportional to “Hole Density Gradient”. Since the concentration of holes is decreasing exponentially, the Hole Density Gradient is a negative quantity. Thus, Diffusion Current due to injected holes in the N-Side  $I_{pn}$ , is

$$I_{pn} \propto q \cdot A \cdot \left( -\frac{dp_{n(x)}}{dx} \right)$$

‘+q’ is the charge of the Hole,

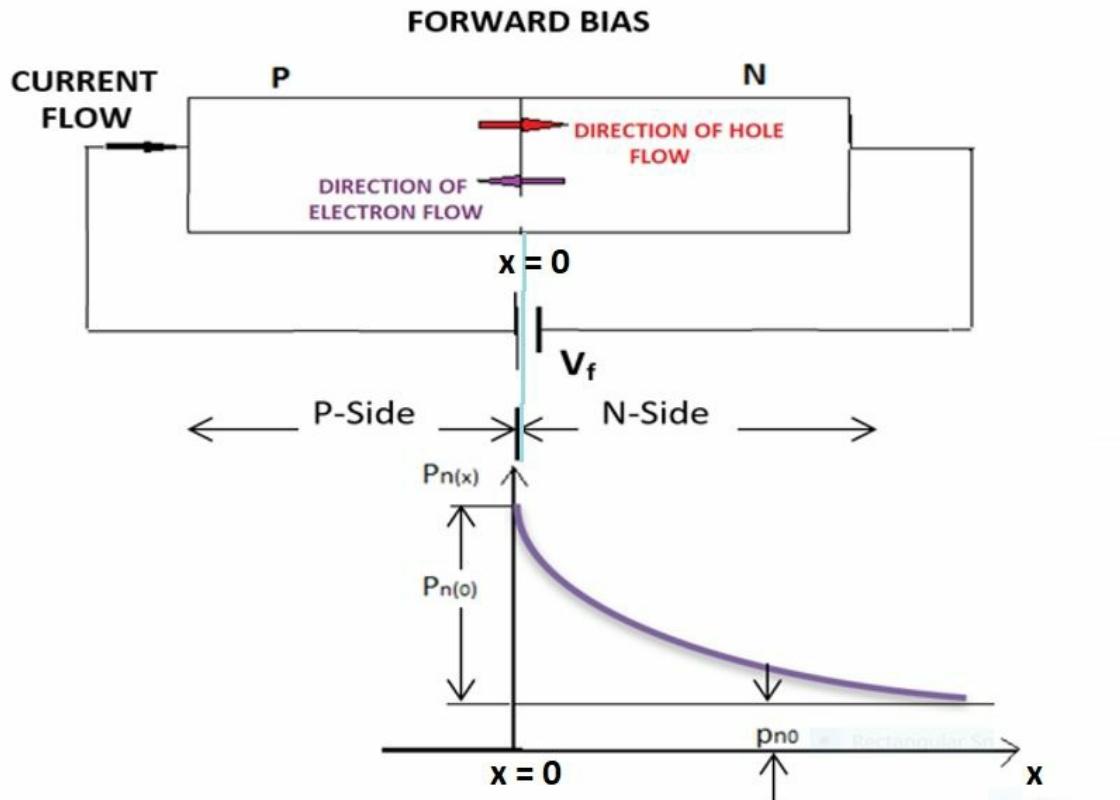
‘A’ is the area of cross section of the junction

and

$p_{n(x)}$  is expressed by equation (4).

The proportionality constant is ‘ $D_p$ ’. This is called the ‘**Diffusion Constant of Holes**’.

$$I_{pn} = -D_p \cdot q \cdot A \cdot \left( \frac{dp_{n(x)}}{dx} \right)$$



**Fig.-14:** - Figure shows increase in "Hole Concentration"  $P_{n(x)}$  at the junction, ( $x = 0$ ), due to the application of Forward Bias. Injected holes become Minority Carriers and recombine with Electrons on the N-side. The concentration of the holes decreases exponentially and attain an equilibrium of ' $p_{no}$ '.

- Taking  $d/dx$  of equation (4) and substituting above we get

$$I_{pn} = \frac{q \cdot A \cdot D_p \cdot P_{n(0)}}{L_p} \cdot e^{-x/L_p} \quad \dots(5)$$

- Substituting for  $P_{n(0)}$  from eq (3) and  $p_{n(0)}$  from eq (2) we get

$$P_{n(0)} = p_{no} \cdot e^{(V/V_T)} - p_{no}$$

$$P_{n(0)} = p_{no} \cdot \left\{ e^{(V/V_T)} - 1 \right\}$$

- Substituting the above in eq (5) and putting  $x = 0$ , we get the current due to holes crossing the junction from P-Side to N-Side (at  $x = 0$ ) as

$$I_{pn(0)} = \frac{q \cdot A \cdot D_p}{L_p} \cdot p_{no} \cdot \left\{ e^{(V/V_T)} - 1 \right\} \quad \dots(6)$$

- Proceeding in a similar way the current due to injection of electrons across the junction,  $I_{np(0)}$ , at  $x = 0$  as

$$I_{np(0)} = \frac{q \cdot A \cdot D_n}{L_n} \cdot n_{po} \cdot \left\{ e^{(V/V_T)} - 1 \right\} \quad \dots(7)$$

$D_n$  is the “Diffusion Constant of Electrons”,

$L_n$  is the “Diffusion Length” of injected electrons in the P-Side  
 $n_{po}$  is the “Equilibrium Concentration” of minority carrier electrons in the P-Side.

- Now substituting for  $I_{pn(0)}$  &  $I_{np(0)}$  in equation (1) we get the current in the P-N Junction due to the applied bias as

$$I = \frac{q \cdot A \cdot D_p}{L_p} \cdot p_{no} \cdot \left\{ e^{\left(\frac{V}{V_T}\right)} - 1 \right\} + \frac{q \cdot A \cdot D_n}{L_n} \cdot n_{po} \cdot \left\{ e^{\left(\frac{V}{V_T}\right)} - 1 \right\}$$

$$I = \left\{ \frac{q \cdot A \cdot D_p}{L_p} \cdot p_{no} + \frac{q \cdot A \cdot D_n}{L_n} \cdot n_{po} \right\} \cdot \left\{ e^{\left(\frac{V}{V_T}\right)} - 1 \right\}$$

- In this 'q', 'A', 'D<sub>p</sub>', 'L<sub>p</sub>', 'D<sub>n</sub>', 'L<sub>n</sub>', 'p<sub>no</sub>' and 'n<sub>po</sub>' are all constants. Using these we define another constant quantity "I<sub>0</sub>", as in Eq.- 9.
- we get the current in a P-N junction as

$$I = I_0 \cdot \left\{ e^{\left(\frac{V}{V_T}\right)} - 1 \right\} \quad \dots(8)$$

Where

$$I_0 = \left\{ \frac{q \cdot A \cdot D_p}{L_p} \cdot p_{no} + \frac{q \cdot A \cdot D_n}{L_n} \cdot n_{po} \right\} \quad \dots(9)$$

Rectangular

**Equation – 8 is known as “Shockley’s Equation”.** This is applicable to both Forward Bias as well as Reverse Bias.

### Justification of the shape of the V-I Characteristic of P-N Junction

In the previous section, we got the V-I Characteristic of a P-N Junction in the Fig-10. This shape of the V-I Characteristic of the P-N Junction can be justified with the help of the Shockley’s equation.

**Forward Blocking Region:** - In this region, the range of forward bias voltage is low and the of current rises very slowly but **exponentially**. The quantity V<sub>T</sub>, called ‘The Volt Equivalent of Temperature’ is given by



$$V_T = \frac{k T}{q}$$

$$V_T = \frac{T}{11600}$$

If we assume a room temperature of 300 <sup>0</sup>K then the value of V<sub>T</sub> works out to

$$V_T = 300/11600$$

$$V_T = 0.02586 \text{ V} \approx 26 \text{ mV}$$

Now, for a **small magnitude** of forward bias say  $V = + 0.08 \text{ V}$ , the exponential term  $e^{V/V_T}$  is calculated as

$$e^{0.08/0.026} = 21.8 \ll 1.$$

Thus, if we neglect '1' in the Shockley's Equation, we get the expression for the current as an exponential.

$$I = I_o \cdot e^{(V/V_T)}$$

**This shows that the curve rises in an exponential manner in the figure.**

**Forward Conducting Region:** - In this region, the forward bias voltage is greater than or equal to the Threshold Voltage, i.e.,

$$V \geq V_T$$

Assume a Ge Diode, where  $V_T = 0.3 \text{ V}$

$$\therefore e^{0.3/0.026} = 102586$$

**This is shown by the almost vertically rising shape of the Exponential curve in the forward bias condition in the figure.**

**Reverse Blocking Region:** - Now, if we consider a reverse bias of  $V_r = - 0.2 \text{ V}$  we get the term

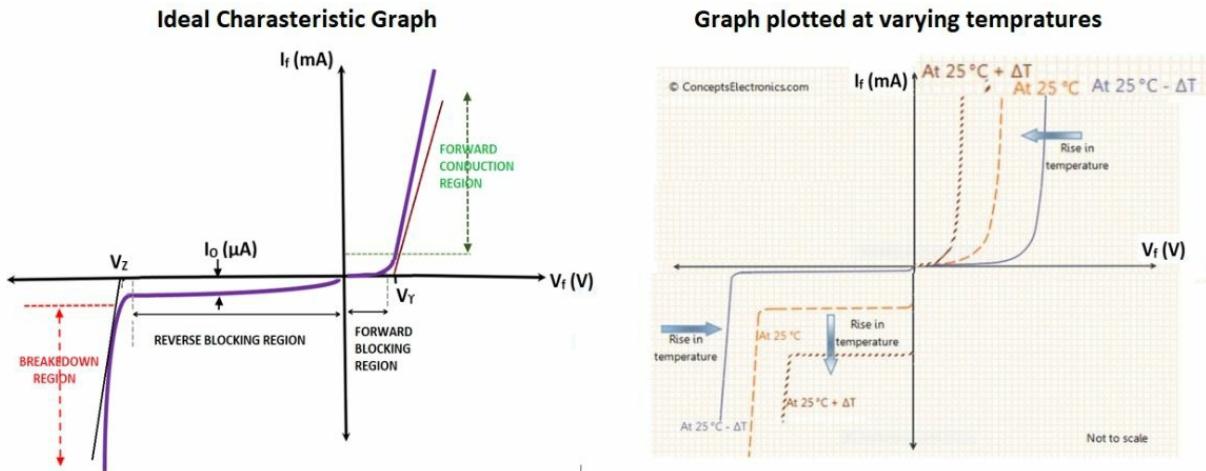
$$e^{-0.2/0.026} = 0.00045.$$

Substituting this value in the Shockley's equation, we get

$$I = I_o \left( e^{-0.2/0.026} - 1 \right)$$

$$I = I_r = I_o (0.00045 - 1) \cong -I_o$$

Thus, we get a **constant value of reverse current**, signified by the negative sign, and plotting in the 2<sup>nd</sup> quadrant, as depicted in the Fig-10. The ideal form of the V-I Characteristic is repeated here for reference. Alongside we show the variation in the diode characteristics w.r.t. temperature.

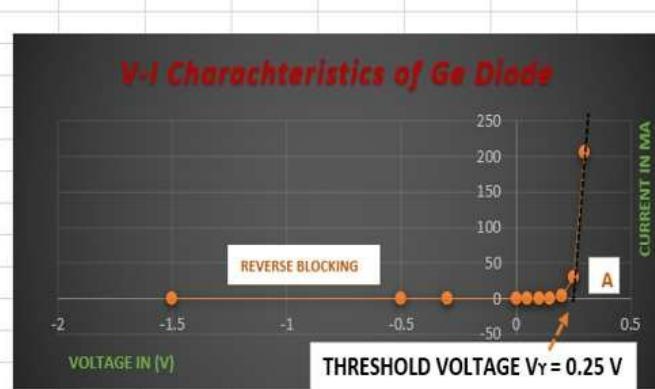


## 2.9 Quantitative Comparison of Ge and Si Diodes from Shockley's Equation

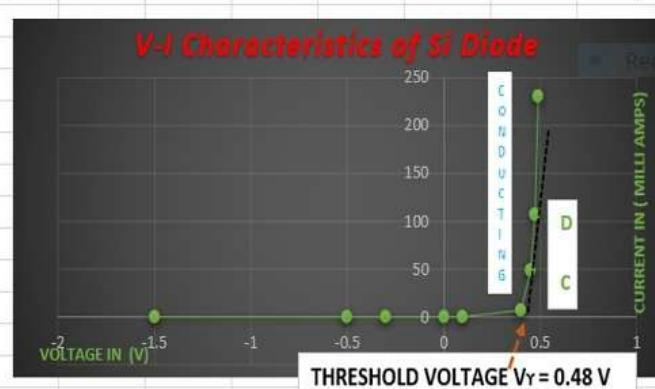
We can make an MS Excel table with a few selected values of forward and reverse bias voltage values and use the Shockley's equation to calculate the corresponding current for these. We can represent these calculated quantities by means of a graph. This has been done in the sample calculation shown in the Fig.-15. Appropriate values for Reverse Saturation current  $I_0$  is taken as **2  $\mu$ A for Ge and 2.5 nA for Si**.

The plot the V-I Characteristics for Si and Ge diodes, shows the expected shape of the V-I Characteristics for both Forward Bias and Reverse Bias conditions. The Threshold voltage  $V_T$  for Ge and Si diodes can also be seen as 0.25 V and 0.5 V respectively.

With $I_0 = 2 \mu\text{A}$ for Ge			
V (Volt)	I (mA)	StaticResistance	DynamicResistance
-1.5	-0.002		
-0.5	-0.002	250000.00	-5.62027E+13
-0.3	-0.001999981	150001.46	-15394998787
0	0		
0.05	0.011683957	4279.37	4279.37224
0.1	0.091625336	1091.40	1250.916626
0.15	0.63858252	234.90	274.2445009
0.2	4.380851736	45.65	53.44350939
A	0.25	29.98537672	8.34
B	0.3	205.1709824	1.46
			9.763899162
			1.712469462



With $I_0 = 1.5 \text{nA}$ for Si			
V (Volt)	I (mA)	StaticResistance	DynamicResistance
-1.5	-1.5E-06		
-0.5	-1.5E-06	333333334.82	1.49877E+17
-0.3	-1.49999E-06	200001949.59	1.36844E+13
0	0		
0.1	6.8719E-05	1455201.58	
0.4	7.203519504	55.53	41.64670642
C	0.45	49.28633329	9.13
D	0.47	106.3651104	4.42
	0.49	229.547135	2.13
			1.18813348
			0.350392931
			0.162361351



**Fig-15.: - Tabulation of Reverse and Forward Bias voltage values and the associated currents, calculated in terms of Shockley's Equation for both Ge (Above) and Si (Below), along with the plot of these values (V-I Characteristic). The shape of the V-I Characteristic deduced earlier is thus verified. Table shows the calculated values of the Static and Dynamic Resistance. Graph shows the different regions of the V-I characteristic and the Threshold Voltage.**

## 2.10 Electrical Parameters of P-N Junction: -

- (i) **Static Resistance:** - Static Resistance “R” of a P-N Junction is defined as the resistance offered by the junction when the voltage and the current in the junction are constant. In other words, Static Resistance is the DC Resistance of the P-N Junction.

Ohm's law with DC current and voltage

$$\mathbf{V} = \mathbf{I} \mathbf{R}$$

$$\therefore \mathbf{R} = \mathbf{V} / \mathbf{I} \quad \dots \dots (10)$$

**(ii) Dynamic Resistance:** - Dynamic Resistance “ $r_D$ ” of a P-N Junction is defined as the resistance offered by the junction when the voltage and the current in the junction are varying, i.e., Dynamic Resistance is the AC Resistance of the P-N Junction.

Ohm's Law with AC current and voltage is expressed as  $v = i R_{AC}$ ,  
Thus

$$r_D = r_{AC} = v / i$$

Where  $v$  &  $i$  are AC quantities.

The AC voltage and current quantities oscillate about the mean values  $V_Q$  and  $I_Q$  with maximum values of  $V_{max}$  and  $I_{max}$  and a minimum value of  $V_{min}$  and  $I_{min}$  respectively.

AC Voltage and Current

$$v = \Delta V = (V_{max} - V_{min}) \text{ and } i = \Delta I = (I_{max} - I_{min})$$

Substituting, the Dynamic Resistance

$$r_D = r_{AC} = v / i = \Delta V / \Delta I$$

$$r_D = r_{AC} = (V_{max} - V_{min}) / (I_{max} - I_{min}).$$

$$r_D = (V_{max} - V_{min}) / (I_{max} - I_{min}) \quad \dots\dots(11.a)$$

**Dynamic Resistance at a certain point of the V-I graph is the ‘RECIPROCAL OF THE SLOPE OF THE TANGENT ON THE GRAPH’ at that point.**

The quantity  $r_D$  can also be expressed as follows –

$$r_D = \frac{dV}{dI} \quad \dots\dots(11.b)$$

**Empirical Formula for Dynamic Resistance:** -

Shockley's equation is approximated as

$$I = I_0 \cdot e^{V/V_T}$$

The slope of the graph of a given equation is the first derivative of the equation w.r.t. the independent variable. Thus the ‘Slope’ of the Shockley's equation is

$$\frac{dI}{dV} = 1/V_T \{ I_0 \cdot e^{V/V_T} \}$$

$$\therefore \frac{dI}{dV} = 1/V_T$$

$\therefore r_D = \text{Reciprocal of the Slope} = V_T / I$

Where  $V_T = \frac{kT}{q}$  Substituting the Physical Constants,

Boltzmann Constant  $1.38 \times 10^{-23} \text{ J K}^{-1}$ ; Electron Charge  $1.6 \times 10^{-19} \text{ C}$

$$V_T = \frac{T}{11600} \text{ V}$$

At  $T = 300^{\circ} \text{ K}$ ,

$$V_T = \frac{300}{11600} \text{ V}$$

$$V_T = 0.026 \text{ V} = 26 \text{ mV.}$$

Substituting this we get the **Empirical Formula** for Dynamic Resistance of a P-N Junction as

$$r_D = \frac{0.026 \text{ (V)}}{I \text{ (A)}} \Omega$$

OR

$$r_D = \frac{26 \text{ (mV)}}{I \text{ (mA)}} \Omega \quad \dots \dots (12)$$

## TUTORIAL – 2

**Example 3:** - Refer to Fig.15 Consider the point ‘A’ for Ge Diode in the table and the corresponding point on the graph. The coordinates of the point ‘A’ are,

$$V = 0.25 \text{ V} \text{ and } I = 29.98 \text{ mA}$$

$$\therefore R = V / I = 0.25 / 0.0299 = 8.36 \Omega$$

**Example 4:** - Refer to Fig.15 Consider the points ‘C’ and ‘D’ in (**Colour ‘Green’**) in the table and graph for Si Diode.  $V_{\min} = 0.45 \text{ V}$  and  $V_{\max} = 0.47 \text{ V}$ . &  $I_{\min} = 49 \text{ mA}$  and  $I_{\max} = 106 \text{ mA}$

$$\therefore v = \Delta V = (V_{\max} - V_{\min}) = (0.47 - 0.45) = 0.02 \text{ V}$$

and

$$i = \Delta I = (I_{\max} - I_{\min}) = (106 - 49) = 57 \text{ mA.}$$

$$\therefore r_D = r_{AC} = v / i = \Delta V / \Delta I$$

$$r_D = (0.47 - 0.45) / (0.106 - 0.049)$$

$$\therefore \underline{r_D = 0.35 \Omega.}$$

**Example 5:** - Using Empirical Formula, taking Mid-Point between points "C" & "D"

Average Current

$$I_D = \frac{(106+49)}{2} = 77.5 \text{ mA}$$

$$r_D = \frac{26 \text{ mV}}{77.5 \text{ mA}} = 0.335 \Omega$$

(Approximately same as Example 4)

**(iii) Threshold Voltage or Cut-in Voltage:** - **Threshold Voltage** is defined as the forward bias voltage at which the diode begins to conduct freely. This is nothing but the Barrier Potential of the P-N Junction in the equilibrium condition. From the graph the Threshold Voltage is found as the point at which the tangent to the graph meets the x-axis. From Fig.-15, it is found that the Threshold Voltage for Ge is 0.25 V and for Si it is near about 0.5 V.

**(iv) Transition Capacitance:** - The capacitance of the Depletion Region (also known as Transition Region) is called the **Transition Capacitance, denoted by  $C_T$ .**

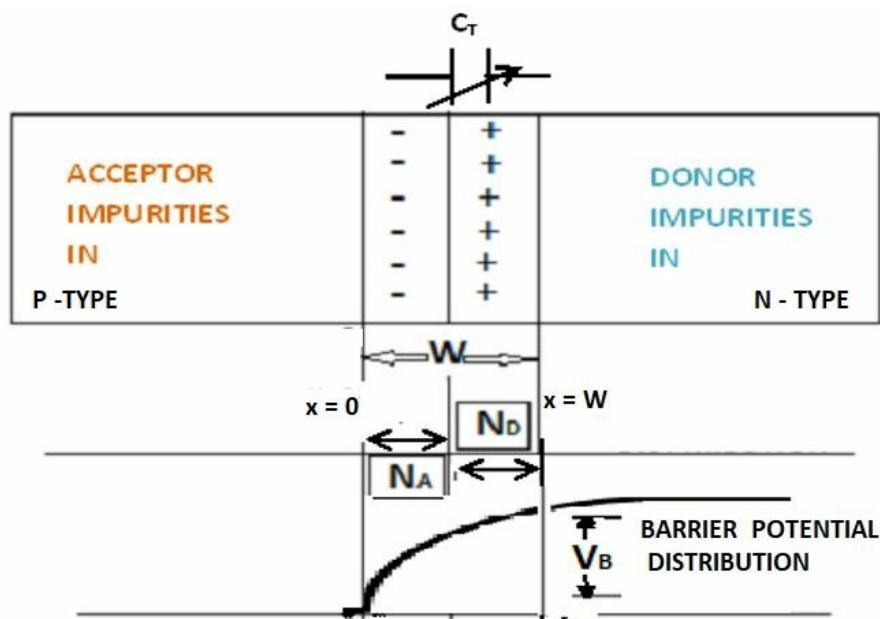
Recall that the width of the depletion Region is dependent upon the applied bias. In other words,  $C_T$  is a variable capacitance.

The Transition Region or the Depletion region contains the static Space Charges of the impurity atoms, which have been 'Depleted' of their active carriers. The density of these charges determines the capacitance present at the junction.

The quantity Capacitance of a capacitor is defined as the "The Charge Stored per Unit Potential Difference".

$$\text{Thus } C_T = \frac{dQ}{dV} \quad (\text{A})$$

- The ‘Charge Density’ of the negative ions in the P-side is proportional to the density of Acceptor impurities, i.e.,  $N_A$  and the ‘Charge Density’ of the positive ions in the N-side is proportional to the density of Donor impurities, i.e.  $N_D$ .



**Fig- 16.: - Charge Density Distribution and Barrier Potential Distribution at a P-N Junction.  $N_A$ =Concentration of Acceptor Impurities:  $N_D$  = Concentration of Donor Impurities:  $W$  = Width of the Depletion Region:  $V_0$  = Magnitude of Barrier Potential.**

- Again, the number of positive ions is exactly equal to the number of negative ions. Therefore, the net charge in the semiconductor crystal is zero. If the width of the Transition Region on the P-side is ‘ $w_p$ ’ and that on the N-side is ‘ $w_n$ ’, then we have

$$-q N_A w_p = +q N_D w_n$$

Where –  $q$  is Electron Charge &  $+q$  is Hole Charge

$$\therefore q N_D w_n + q N_A w_p = 0$$

Assuming  $N_D = N_A$  so that  $w_n = w_p$  & net 'Charge Density' equals  $q N_A$ .

(Where 'W' is the width of the Transition Region)

$$q N_A (w_p + w_n) = q N_A W = 0$$

$$w_p + w_n = W$$

The Net Barrier Potential  $V_B$  appears across the width of the Transition Region. The relationship between Charge Density and Potential Difference is given by "Poisson's Equation" as

$$\frac{d^2V}{dx^2} = \frac{q N_A}{\epsilon}$$

Where ' $\epsilon$ ' is the Electrostatic Permittivity of the semiconductor.

Integrating this twice over the Transition Region, from  $x = 0$  to  $x = W$ , we get

$$\int_0^W \frac{d^2V}{dx^2} = \int_0^W \frac{dV}{dx} = V_B$$


---

$$V_B = \int_0^W \frac{q N_A}{\epsilon} dx$$

Or

$$V_B = \frac{q N_A}{2\epsilon} W^2 \quad (B)$$

**The width of the Transition Region is directly proportional to the net Barrier Potential at the junction and varies in proportion to the square root of  $V_B$ '.**

Area of cross section of the junction is 'A', the total charge in the Transition Region

$$Q = q N_A W A$$

Substituting this in equation (A) (Since 'q', ' $N_A$ ' and 'A' are constant quantities), we get,

$$C_T = q N_A A \frac{dW}{dV}$$

Under a “Reverse Bias” of  $V_B = V$ , and substituting for  $V_B$ , given by equation (B).

$$\begin{aligned} \frac{dV_B}{dW} &= \frac{qN_A W}{\epsilon} \\ \therefore \frac{dW}{dV} &= \epsilon / q N_A \end{aligned}$$

Substituting this in the expression for  $C_T$ , as above, we get

$$C_T = \frac{\epsilon A}{W} \quad \dots\dots(13)$$

**Note.**

- ✓ The expression (13) is exactly the same as that for a Parallel Plate Capacitor with metal plates of area ‘A’, separated by a distance ‘W’ and filled with a dielectric material of electrostatic permittivity ‘ $\epsilon$ ’.
- ✓ From the equation (B) above, it is noted that “Width of the Depletion Region varies as the Square Root of applied reverse bias  $V_B$ ”.
- ✓ **From Fig-16 it is observed that the “Width of the Transition Region is proportional to the Concentration  $N_A$  and  $N_D$  of Acceptor and Donor Impurities respectively”.**

## 2.11 Break Down Condition in P-N Junction

At a certain lower range of reverse bias voltages, the current due to the intrinsically generated minority carriers is the Reverse Saturation Current  $I_0$ . Recall that, value of this Reverse Saturation Current is a few  $\mu\text{A}$  in Ge and a few  $\text{nA}$  in Si. This current remains constant for a quite large range of values of reverse bias. However, at a limiting value of reverse bias  $V_Z$ , the reverse current suddenly increases. This situation is known as the “**Break Down Condition**”. There are two physical mechanisms by means of which the phenomenon of Breakdown occurs in a P-N Junction, viz. (i) **Zener Breakdown Mechanism** (ii) **Avalanche Breakdown Mechanism**. These are explained below.

**Table 1 Difference Between Avalanche Breakdown And Zener Breakdown**

Avalanche Breakdown	Zener Breakdown
a) Electrons are released due to a process of knocking out of valence electrons by free electrons which have been accelerated by the strong electric field present at the depletion region.	a) Electrons are pulled out of valence shells by a strong electric field present at the depletion region.
b) In order to acquire enough KE to knock out valence electrons the striking electron has to interact with the electric field over a certain length of its path. This requires a wider depletion region	b) In order to produce a strong enough electric field at the depletion region, the width of the depletion region must be narrow, since $\xi = dV/dx$
c) In order to have a strong enough electric field to impart enough KE, the applied reverse bias must be large enough.	c) Zener Breakdown can occur at relatively lower reverse biases provided the depletion region is narrow enough.
d) A wide depletion region is produced when the doping concentration is less. Thus, Avalanche Breakdown occurs in relatively lowly doped P-N junctions and at relatively higher reverse biases.	d) A narrow depletion region is created when the doping concentration is high. Thus, Zener Breakdown occurs in relatively highly doped P-N junctions and at relatively lower reverse biases.

ΛΛΛΛΛΛΛΛΛ -PN—P-N--PN- ΛΛΛΛΛΛΛΛΛ

# **CHAPTER – III**

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## **THE RECTIFIER and FILTER**

### *RECTIFIER AND FILTER*

#### **INTRODUCTION**

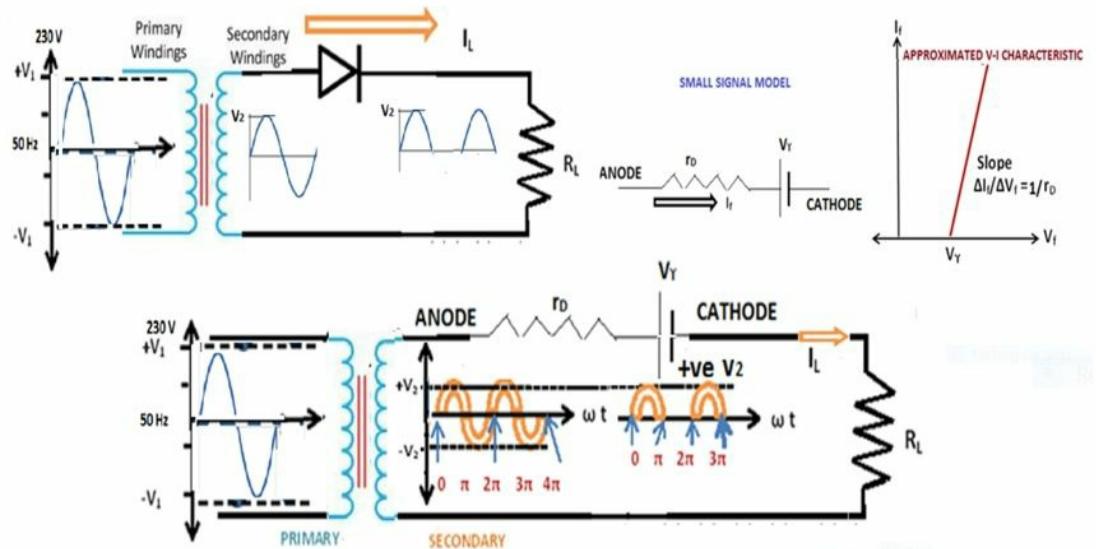
- Electronic Gadgets like TV, Audio/Video Home Theatre, Computer and Mobile Phone etc. have to be powered by a DC source.
- Domestic and Industrial electrical power supply is invariably in the form of AC. Thus, this AC power has to be converted into DC to operate such gadgets.
- Quite often the AC to DC converter, that powers an electronic gadget is incorporated within the gadget itself, say in case of the TV.
- Sometimes the AC / DC Converter comes as a separate unit. Such as the charger for your Mobile Handset.
- All such converters are based upon a Rectifier. A Rectifier is a circuit that converts (“Rectifies”) AC into DC. They are often called “Converter”.
- The AC power supply is at 230 Volt (RMS) and frequency of 50 Hz. Whereas the DC power rating of electronic gadgets is only a few volts (say 5 V to 16 V). Hence the Rectifier circuit is conveniently depicted as being connected to the Secondary side of a Step-Down transformer.
- There are various types of rectifiers, namely, Half Wave Rectifier, Full Wave Centre-Tapped Rectifier and Full Wave Bridge Rectifier.

## SECTION -1

### *THEORY OF RECTIFIERS*

#### **3.1 Half Wave Rectifier**

- ❖ The primary waveform is shown with a peak value of  $V_1$  and the secondary, with a peak value of  $V_2$ , such that  $V_2 < V_1$ .
- ❖ The positive half cycle is from  $\omega t = 0$  to  $\omega t = \pi$ , next positive half cycle is from  $\omega t = 2\pi$  to  $\omega t = 3\pi$ , and so on. During the positive half cycle, the Anode is at a positive potential while the Cathode is at a potential of 0 V. Therefore, the diode is Forward Biased. A Forward Biased Diode can be replaced by the Small Signal Model described in Chapter-2.

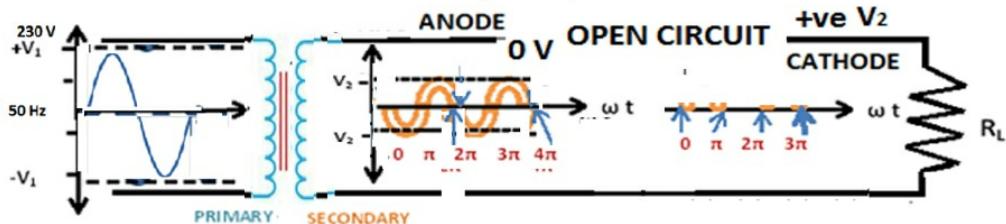


**Fig. – 1:** Circuit of Half Wave Rectifier showing Primary, Secondary and rectified waveforms.

- ❖ Neglect the “**Small DC  $V_f$** ”. If the load  $R_L$  is purely resistive, then

the waveform of the current will be exactly the same as the e.m.f. waveform i.e., the shape of the positive half cycle.

- ❖ The negative half cycles are from  $\omega t = \pi$  to  $\omega t = 2\pi$ ,  $\omega t = 3\pi$  to  $\omega t = 4\pi$ , and so on. During this, the anode is of negative polarity, while the cathode is at zero potential. Hence the diode is Reverse Biased. At reverse bias the diode is “Open Circuit”. Since current is zero the voltage drop across  $R_L$  is also zero. This is depicted in the figure below.



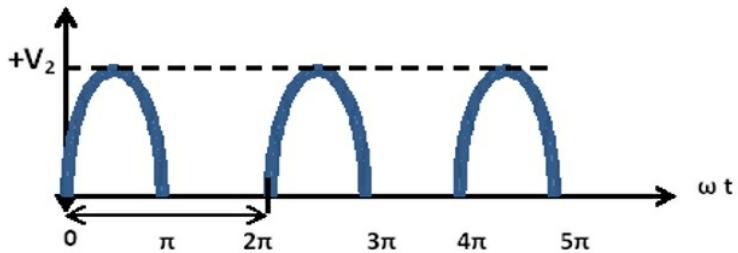
- ❖ In other words, the current through the circuit flows only in the positive half cycle. while during the negative half cycle, the current is zero and the current through the load  $R_L$  flows only in one direction.
- ❖ In other words, the current through the circuit flows only in the positive half cycle. while during the negative half cycle, the current is zero and the current through the load  $R_L$  flows only in one direction. This is equivalent to a DC.
- ❖ In other words, the Bidirectional AC current is “Rectified” as a “Unidirectional” current.

### Average & R.M.S. Value of Rectified Output: -

- ❖ The input to the rectifier is a sine wave  $v_{(t)}$

$$v_{(t)} = V_2 \sin(\omega t)$$

- ❖ This “Rectified” waveform is “Unidirectional” and is of sinusoidal shape from 0 to  $\pi$  in every cycle. The periodicity of the waveform is  $2\pi$ .



**Fig – 2:** - Output Waveform of the H.W. Rectifier consists of only the Positive Half Cycles of the sinusoidal waveform. This has an amplitude of  $V_2$  and angular periodicity of  $2\pi$ .

1. **The Average Value of this waveform is the DC Content of the output waveform.**

This would be the reading of a **PMMC Voltmeter (DC Voltmeter)**

$$V_{AV} = V_{DC} = \frac{1}{2\pi} \int_0^\pi V_2 \sin(\omega t) d(\omega t)$$

$$V_{AV} = \frac{V_2}{2\pi} [(-\cos(\omega t))_0^\pi]$$

$$V_{AV} = \frac{V_2}{2\pi} [(\cos(\omega t))_0^\pi]$$

$$\therefore V_{AV} = \frac{V_2}{2\pi} [\cos(0) - \cos(\pi)]$$

Since  $\cos(0) = 1$  &  $\cos(\pi) = -1$

$$\therefore V_{AV} = V_{DC} = \frac{V_2}{\pi} \quad \dots(1)$$

Where  $V_2$  is the Peak Value of the secondary voltage of the step-down transformer.

2. The RMS Value of this waveform is the **AC Content** of the output waveform.

This would be the reading of a **MI Voltmeter (AC Voltmeter)** connected at the output terminal.

$$V_{rms} = \sqrt{\left[ \left\{ \frac{(V_2)^2}{2\pi} \right\} \int_0^\pi \sin^2(\omega t) d(\omega t) \right]}$$

With  $\sin^2(\omega t) = \frac{1}{2}\{\cos(2\omega t) - 1\}$

$$V_{rms} = \sqrt{\left[ \left\{ \frac{(V_2)^2}{4\pi} \right\} \int_0^\pi \cos(2\omega t) d(\omega t) - \int_0^\pi d(\omega t) \right]}$$

$$V_{rms} = \sqrt{\left[ \left\{ \frac{(V_2)^2}{4\pi} \right\} \left\{ \frac{1}{2} (\sin 2\omega t)_0^\pi \right\} - (\omega t)_0^\pi \right]}$$

In the First Term  $\sin \pi = 0 = \underline{\sin 0}$ .

The second term equates to  $\pi$ .

$$\therefore V_{rms} = \sqrt{\left[ \left\{ \frac{(V_2)^2}{4\pi} \right\} \pi \right]}$$

$$\therefore V_{AC} = V_{rms} = \frac{V_2}{2} \quad \dots(2)$$

Rectangular Ship

### 3. Ripple Factor: -

- The output of the rectifier contains both AC and DC components. The quantity **Ripple Factor** is the measure of the ratio of the AC Component to the DC Component at the output of a rectifier. This is defined by

$$\mathcal{R} = \frac{V_{RMS'}}{V_{DC}}$$

- The quantity  $V_{RMS}$ , given by equation 2 is the RMS value of the complete waveform, whereas, in the definition of Ripple Factor, the quantity  $V_{RMS'}$  is the RMS value of the purely AC component.
- The pure AC component is obtained by removing the DC component from the output waveform  $V_0$ ,

$$V_{AC'} = V_0 - V_{DC}$$

- $\therefore$  The rms value of this would be

$$V_{RMS}' = \sqrt{\frac{1}{2\pi} \left\{ \int_0^{2\pi} (V_o - V_{dc})^2 dt \right\}}$$

$$\therefore V_{RMS}' = \sqrt{\frac{1}{2\pi} \left\{ \int_0^{2\pi} (V_o^2 - 2V_{dc}V_o + V_{dc}^2) dt \right\}}$$

- In this, the first term, is the square of RMS value of the complete output waveform, given by equation 2

$$\left( \frac{1}{2\pi} \int_0^{2\pi} V_o^2 dt \right) = V_{rms}^2$$

The second term is the DC value of the output waveform, given by equation 1.

$$\left( \frac{1}{2\pi} \int_0^{2\pi} (V_o) dt \right) = V_{DC}$$

Therefore, the second term becomes  $2 V_{DC}^2$

$$\therefore V_{RMS}' = \sqrt{V_{rms}^2 - V_{dc}^2}$$

- Substituting this in the expression for Ripple Factor we have

$$\mathcal{R} = \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{dc}}$$

$$\mathcal{R} = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1} \quad \dots(3)$$

- Substituting for  $V_{rms}$  and  $V_{dc}$  from equations (2) and (1) respectively, in equation (3), we get the numerical value of the Ripple Factor of a Half Wave (H.W) rectifier as follows.

$$R_{(HW)} = \sqrt{\frac{\left(\frac{V_2}{2}\right)^2}{\left(\frac{V_2}{\pi}\right)^2} - 1}$$

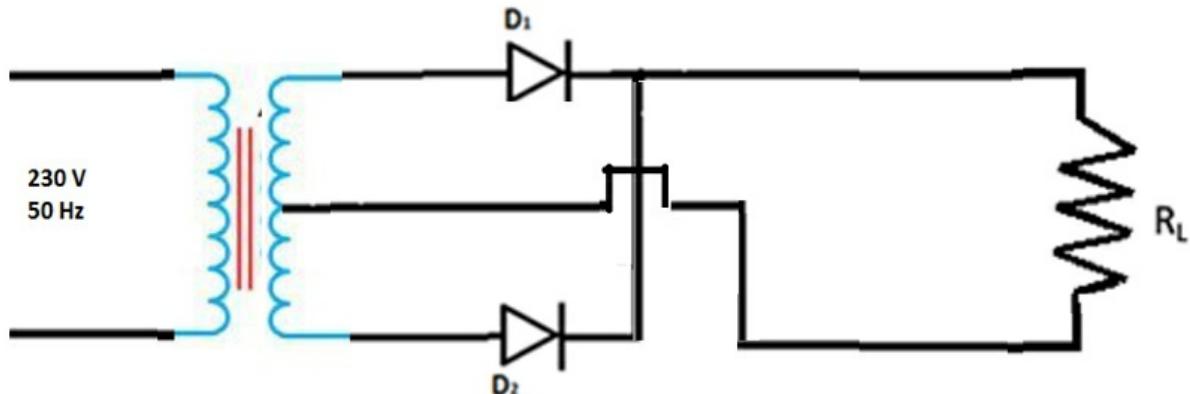
$$R_{(HW)} = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1}$$

$$R_{(HW)} = \sqrt{\left(\frac{3.14}{2}\right)^2 - 1}$$

$$R_{(HW)} = 1.21 \quad \dots\dots (4)$$

### 3.2 Full Wave Center-Tap Rectifier Circuit diagram and working principle

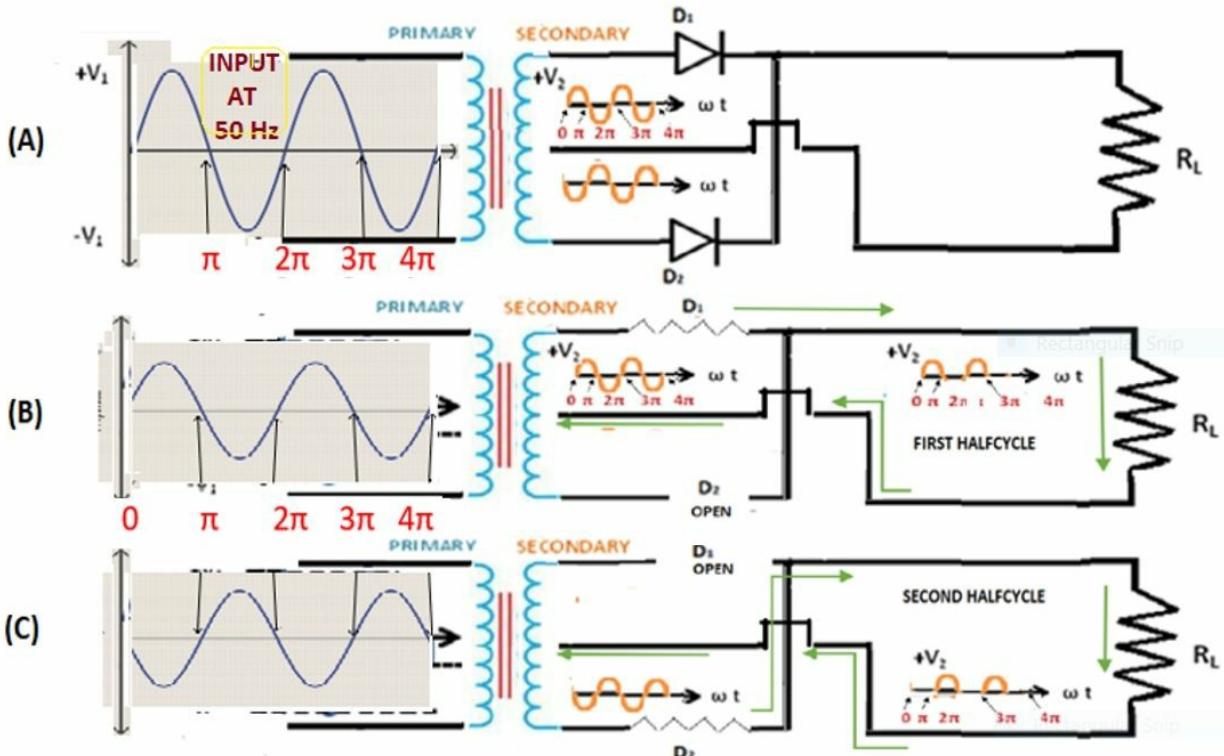
- ✓ The Half Wave Rectifier “Rectify” only half of the sinusoidal signal. Hence it is not very efficient.
- ✓ Full Wave Rectifiers rectify the complete sinusoidal cycle; hence it is more useful.



**Fig. 3**

- ✓ The secondary winding of the step-down transformer has a ‘CENTRE TAP’, i.e., the midpoint of the secondary winding is taken out. This results in the secondary voltage to be equally divided between the two halves of the secondary winding.
- ✓ The transformer is constructed in such a manner that the center tap point always remains at zero potential and that the turn’s ratio of the transformer is such as to produce a secondary voltage

whose peak value is at the desired level of  $V_2$ .

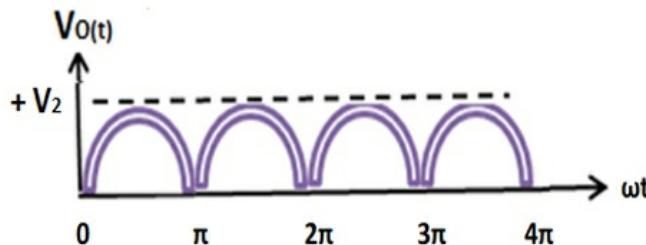


**Fig. 4 :- (A) The complete Circuit Diagram : (B) Equivalent Circuit at +ve half cycle : (C) Equivalent Circuit at -ve half cycle:**

- ✓ The e.m.f. developed in these two halves is of opposite phase.
- ✓ During the First Half Cycle, from  $\omega t = 0$  to  $\omega t = \pi$ , the anode of the diode D<sub>1</sub> is at Positive potential. Therefore, D<sub>1</sub> is forward biased, hence it conducts. On the other hand, the anode of D<sub>2</sub> is at negative potential, hence, it is Open. In this case the current flow is shown by **GREEN ARROW** (Part B of Fig- 4.)
- ✓ During the next Half Cycle, from  $\omega t = \pi$  to  $\omega t = 2\pi$ , the situation is depicted in Part C of Fig-4. D<sub>2</sub> is conducting and D<sub>1</sub> is Open. The direction of current flow is also shown.
- ✓ When we combine these two situations, we have the complete output waveform  $V_{0(t)}$  , as shown in part (D) of Fig-4.
- ✓ Assuming Purely Resistive Load, the voltage  $V_0$  across the load will be of the same waveform as that of the secondary voltage.
- ✓ Since the rectified output voltage waveform is made up of both the half cycles of the full sinusoidal waveform, hence the

**name Full Wave (FW) Rectifier.**

1. **Frequency of the Output Waveform of F.W. Rectifier:** - It is to be noted that the periodicity of the output waveform is  $\pi$  (instead of  $2\pi$ ). The AC power supply frequency of the full sinusoidal cycle of periodicity  $2\pi$  is 50 Hz. Since the periodicity of the output waveform is half, its **frequency is 100 Hz**. (Periodicity and frequency have an inverse proportionality).



**Fig. 4: - (D) Complete waveform at the output.**

2. **The Average Value or  $V_{DC}$  (Reading of a PMMC Voltmeter at the output.)**

$$\begin{aligned}
 V_{AV} &= V_{DC} = \frac{1}{\pi} \int_0^{\pi} V_2 \sin(\omega t) d(\omega t) \\
 V_{AV} &= \frac{V_2}{\pi} [(-\cos(\omega t)) \Big|_0^\pi] = \frac{V_2}{2\pi} [(\cos(0)) - (\cos(\pi))] \\
 \therefore V_{AV} &= \frac{V_2}{\pi} [\cos(0) - \cos(\pi)]
 \end{aligned}$$

Since  $\cos(0) = 1$  &  $\cos(\pi) = -1$

$$\therefore V_{AV} = V_{DC} = \frac{2V_2}{\pi} \quad \dots(5)$$

**Where  $V_2$  is the Peak Value of the sinusoidal voltage at ONE HALF of the secondary of the step-down transformer.**

### 3. The RMS Value or $V_{AC}$ (Reading of a MI Voltmeter.)

$$V_{rms} = \sqrt{\left[ \left\{ \frac{(V_2)^2}{\pi} \right\} \int_0^{\pi} \sin^2(\omega t) d(\omega t) \right]}$$

With  $\sin^2(\omega t) = \frac{1}{2}\{\cos(2\omega t) - 1\}$

$$V_{rms} = \sqrt{\left[ \left\{ \frac{(V_2)^2}{2\pi} \right\} \int_0^{\pi} \cos(2\omega t) d(\omega t) - \int_0^{\pi} d(\omega t) \right]}$$

$$V_{rms} = \sqrt{\left[ \left\{ \frac{(V_2)^2}{2\pi} \right\} \left\{ \frac{1}{2} (\sin 2\omega t)_0^{\pi} \right\} - (\omega t)_0^{\pi} \right]}$$

$$\therefore V_{rms} = \frac{V_2}{\sqrt{2}} \quad \dots\dots(6)$$

4. **Ripple Factor of F.W Rectifier:** - Substituting the expressions for  $V_{rms}$  and  $V_{dc}$  in the equation 3

$$R_{(FW)} = \sqrt{\frac{\left(\frac{V_2}{\sqrt{2}}\right)^2}{\left(\frac{2V_2}{\pi}\right)^2} - 1}$$

$$R_{(FW)} = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$R_{(FW)} = \sqrt{\left(\frac{3.14}{2\sqrt{2}}\right)^2 - 1}$$

$$R_{(FW)} = 0.482 \quad \dots\dots(7)$$

### 5. Rectification Efficiency of F.W. Rectifier

Rectification Efficiency is defined as Output DC Power divided by Input AC Power. In case of a rectifier, the input AC power is the input from the secondary of the transformer and the Output

- DC Power developed across the Load.

$$P_{DC} = \frac{V_{DC}^2}{R_L} = \frac{(2V_2/\pi)^2}{R_L}$$

$$P_{DC} = \frac{(4V_2)^2}{\pi^2 R_L}$$

- AC Power delivered by the secondary also appears across the Load  $R_L$ , the internal resistance of the rectifier section, denoted by  $R_i$ . This includes the resistance of the secondary coil and the dynamic forward resistance of the diodes.

$$P_{AC} = \frac{V_{RMS}^2}{(R_L + R_i)}$$

Since the voltage across the secondary is a pure AC, its RMS value equals  $\frac{V_2}{\sqrt{2}}$

$$P_{AC} = \frac{\left(\frac{V_2}{\sqrt{2}}\right)^2}{(R_L + R_i)}$$

$$P_{AC} = \frac{V_2^2}{2(R_L + R_i)}$$

- From this we get Rectifier Efficiency as

$$\eta_{Rectifier} = \frac{P_{DC}}{P_{AC}} = \frac{\frac{(4V_2)^2}{\pi^2 R_L}}{\frac{V_2^2}{2(R_L + R_i)}}$$

- If we neglect the internal resistance  $R_i$  of the rectifier section, we have

$$\eta_{Rectifier} = \frac{8}{\pi^2}$$

$$\eta_{Rectifier} = 0.811 \text{ Or } 81.1 \% \quad \dots (8)$$

Rectangular Snap

## 6. P.I.V. of F.W. Center – Tap Rectifier

Peak Inverse Voltage (PIV) is the maximum (peak) value of Reverse (Inverse) Bias appearing across the diodes in each cycle of operation.

Recall that a Diode goes into Break-Down condition if the reverse

**bias applied across it crosses a limit denoted by  $V_Z$ .** A Rectifier Diode must never be allowed to go into Break Down. Hence the PIV of the diodes of the rectifier must be well below the  $V_Z$  limit.

In Fig- 4 (A), in the first half cycle,  $D_2$  is reverse biased. The peak of the reverse voltage across  $D_2$ , at the instant  $\pi/2$ , is  $-V_2$  from the lower half of the secondary winding. But at this same instant, since the upper half of the secondary winding is always at a phase difference of  $\pi$ , the upper part of the secondary winding is also applying a reverse voltage of  $-V_2$ . Therefore PIV across  $D_2$  is  $-2 V_2$ . In the next half cycle  $D_1$  would be reverse biased, and similarly PIV appearing across  $D_1$  would also be  $(-2 V_2)$ .

$$\text{Hence, P.I.V. for F.W. Center - Tap Rectifier} = -2 V_2 \quad \dots\dots (9)$$

**7. Output Voltage Considering Voltage Drop across Diodes:** - Recall that, when a diode is forward biased, it becomes fully conducting only when the forward bias across it just overcomes the Barrier Potential. In the V-I Characteristic, this situation is shown by the Threshold Voltage (or Knee Voltage)  $V_Y$ . Thus, it can be assumed that there appears a 'Forward Voltage Drop' equal to  $V_Y$  across a forward biased diode. This is also shown in the 'Small Signal Model' of the diode, given in Lesson-2. The instantaneous output voltage of a rectifier is always reduced by this voltage drop. Hence

**Instantaneous output voltage of FW Center-Tap Rectifier**

$$V_{o(t)} = V_o - V_Y \quad \dots\dots (10)$$

### 3.3 Full Wave Bridge Rectifier

#### Circuit diagram and working principle

The most common Circuit Diagram of a FW Bridge Rectifier is shown in the Fig.-5 below.

- ❖ During the First Half Cycle, i.e., from  $\omega t = 0$  to  $\omega t = \pi$ , (Part B of Fig- 5.), the anode of Diode  $D_1$  is connected to the upper end of the secondary winding. This is at a positive polarity. **The cathode of Diode  $D_3$**  is connected to the lower end of the secondary. This is at a negative polarity. **Hence both  $D_1$ and  $D_3$  are forward biased and conducting.**

- ❖ On the other hand, the anode of  $D_2$  is connected to the lower end and the cathode of  $D_4$  is connected to the upper end of the secondary. **Hence,  $D_2$  and  $D_4$  are both reverse biased.** These two diodes are shown as open circuits.

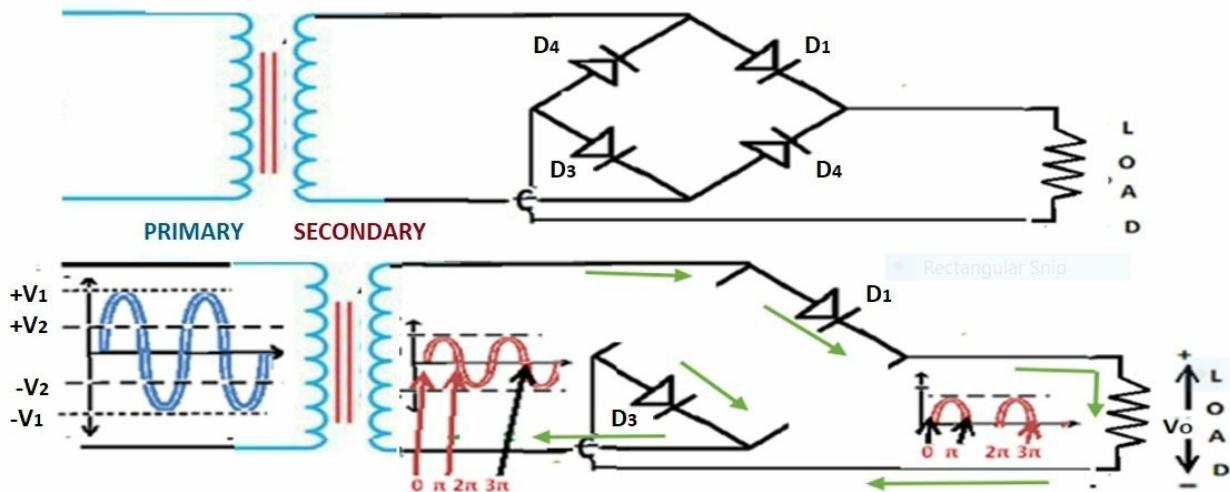
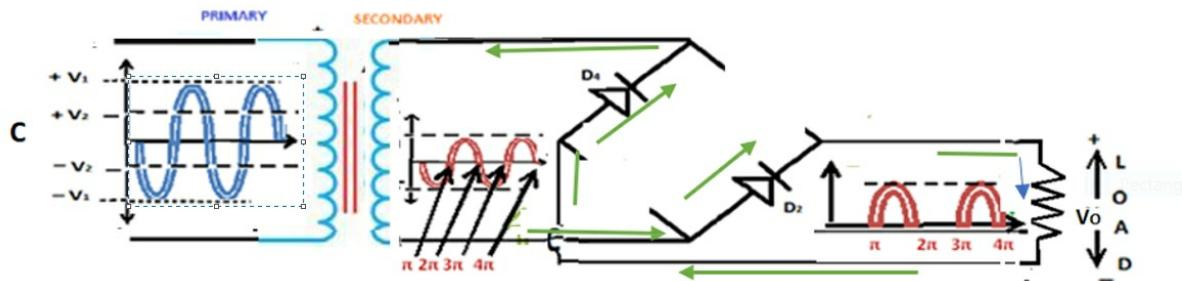
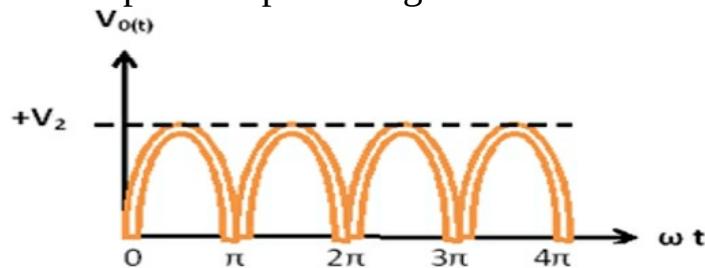


Fig. - 5

- ❖ The equivalent circuit of the rectifier for the First Half Cycle is represented by the part B of the Fig- 5.
- ❖ The forward biased diodes  $D_1$  and  $D_3$  conduct. Therefore, current flows from the upper end of the secondary winding, through the diode  $D_1$ , to the load and then on to the lower end of the secondary winding through  $D_3$ , thus completing the circuit. This path of current flow is shown with **GREEN ARROWS** in the part B of the Fig-5.
- ❖ Since the load is purely resistive the waveform of the voltage across the load is the same as the First Half Cycle of the Secondary. This repeats for every Positive Half Cycle.
- ❖ The next half cycle is from  $\omega t = \pi$  to  $\omega t = 2\pi$ . In this, the lower end of the secondary winding will be at a positive potential and the upper end will be at a negative potential. (Part C of Fig-5.)



- ❖ The anode of Diode  $D_2$  is positive and the cathode of Diode  $D_4$  is negative. **Hence both  $D_2$  and  $D_4$  are forward biased.** On the other hand, the anode of  $D_1$  is negative and the cathode of  $D_3$  is positive. **Hence,  $D_1$  and  $D_3$  are both reverse biased (Hence shown Open Circuited).**
- ❖ Therefore, current flows from the lower end of the secondary winding, through the diode  $D_2$ , to the load and then on to the upper end of the secondary winding through  $D_4$ , thus completing the circuit. This path of current flow is shown with **GREEN ARROWS** in the figure.
- ❖ The complete output voltage waveform is shown in the Fig – 6.



Rec

**Fig. 6**

### Similarity between FW Center-Tap Rectifier & FW Bridge Rectifier

The following are just the same for both FW Center-Tap and Bridge rectifier configurations

**(1) Frequency of the output waveform = 100 Hz**

$$(2) V_{dc} = \frac{2V_2}{\pi}$$

$$(3) V_{rms} = \frac{V_2}{\sqrt{2}}$$

**(4) Ripple Factor = 0.482**

**(5) Rectification Efficiency  $\eta_{rectifier} = 0.811$  or 81.1 %**

### **Dis-similarity between FW Center-Tap Rectifier & FW Bridge Rectifier**

#### **6. PIV of FW Bridge Rectifier: -**

During each Half Cycle, two diodes are at Reverse Bias and they act in Series.

Hence the Peak of the Inverse Voltage of  $-V_2$  appears across both these Diodes.

Hence P.I.V. across each diode for FW Bridge Rectifier

$$\text{P.I.V.} = \frac{-V_2}{2} \quad \dots (11)$$

**In other words, the PIV across each of the diodes of F.W. Bridge Rectifier is 4 times lesser than that for those of the F.W. Center-Tap Rectifier.**

#### **7. Output Voltage Considering Voltage Drop across Diodes**

A diode becomes fully conducting only when the Forward Bias exceeds the quantity  $V_Y$  or, in other words, there occurs a voltage drop of  $V_Y$  across each conducting diode. Since two diodes act in series in each of the half cycles, a voltage drop of  $2 V_Y$  occurs in each half cycle. Therefore, the instantaneous output voltage of a rectifier is reduced by this voltage drop.

Hence Instantaneous Output Voltage of FW Bridge Rectifier

$$V_{o(t)} = V_o - 2V_Y \dots(12)$$

### Diodes used in Rectifiers

- a) **During reverse bias condition the diodes must be fully blocking.** In other words, the Reverse Saturation Current must be negligible. In a Ge Diode Reverse Saturation Current of the order of microamperes ( $\mu A$ ), whereas, in a Diode made of Si, this quantity is of the order of nanoamperes ( $nA$ ). **Therefore, Si diodes are better approximation of open circuit at reverse bias.**
- b) **The diodes must be able to withstand sufficient reverse voltage (PIV) without going into Break-Down Condition.** In case of Ge the Energy Gap between the valence band and the Conduction Band is less compared to that of a Si. Thus, in a Ge diode, there will exist more minority carriers than in case of a Si diode at any given room temperature. Since more minority carriers are available in the diodes made of Ge, they tend to go into **Avalanche Break-Down Condition** at much lesser values of reverse voltage compared to those made of Si. **In other words, the diodes made of Si are able to withstand larger amounts of reverse bias (PIV).**

**IN CONSIDERATION OF THESE PROPERTIES, IT IS CONCLUDED THAT Si DIODES ARE MORE SUITABLE FOR USE IN RECTIFIERS THAN Ge DIO**

**'Suitability' Center-Tap Rectifier and Bridge Rectifier**  
Comparing the properties of F.W. Center-Tap & F.W. Bridge Rectifier

- **FW Center-Tap Rectifier**

$$\text{P.I.V.} = -2V_2.$$

**Bridge Rectifier**

$$\text{P.I.V.} = -V_2/2$$

- Instantaneous output voltage of FW Center-Tap Rectifier

$$V_{o(t)} = V_o - V_Y$$

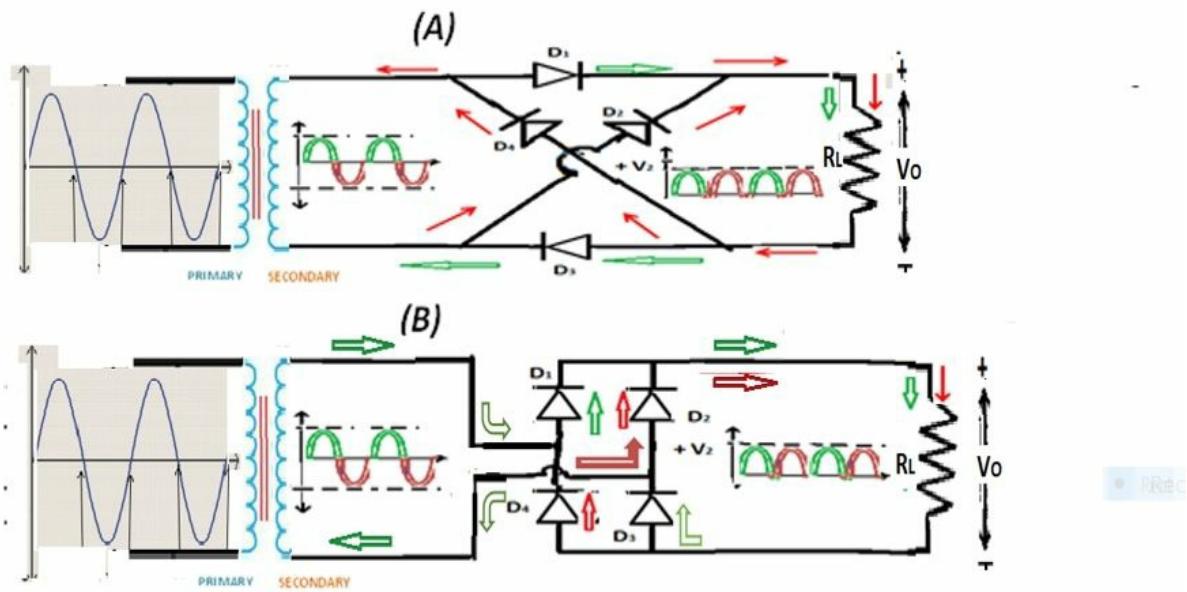
- Instantaneous Output Voltage of FW Bridge Rectifier

$$V_{o(t)} = V_o - 2V_Y$$

- The  $V_{DC}$  output of the rectifier (given by  $V_{DC} = 2 V_2 / \pi$ ), must equal the rated DC voltage of the load. If the rated DC voltage of the load is higher, we would require a transformer whose secondary voltage peak  $V_2$  must be higher.
- Since rectifiers must use diodes made of Si. the value of the quantity  $V_Y = 0.7V$ . Thus, the output voltage would be 0.7 V less than  $V_{DC}$  in a F.W. Center-Tap rectifier. Therefore, **Centre Tap Rectifier is suitable for low voltage applications**. In this case the transformer has to be so chosen that it produces a secondary voltage whose peak value must be 0.7 V higher than rated load voltage.
- On the other hand, for a Bridge Rectifier the output voltage would be 1.4 V lesser than  $V_{DC}$ . Therefore, the transformer has to be so chosen that it produces a secondary voltage whose peak value must be 1.4 V higher.
- The higher the rated DC voltage, the greater is the PIV. Thus, if a Centre Tap Rectifier is used for driving a higher rated load, the PIV would be very high (Since PIV is  $2V_2$  for Centre-Tap).
  - On the other hand, PIV across each diode in Bridge Rectifier is  $\frac{1}{2}V_2$ . Hence it is suitable for higher rated voltage applications.

### Different Representations of FW Bridge Rectifier

The FW Bridge Configuration can also be represented in the following two forms. In these two representations, the positive half cycles and the current flow during these are shown in **GREEN** colour and that in the negative half cycles is shown in **MAROON** colour.



**Fig -7:** - Two different representations of the F.W. Bridge Rectifier. The +ve Half Cycles and the current flow during these are shown in GREEN and -ve Half Cycles are shown in MAROON.

## SECTION-2

### **FILTERS AND VOLTAGE REGULATORS FOR RECTIFIERS**

#### **3.4 Filter Circuits for Rectifiers**

- ❖ The purpose of a rectifier is to replace a DC battery.
- ❖ The output of the rectifier contains both an AC component and a DC component.
- ❖ DC is of ‘Zero Frequency’ while the AC component of the rectifier output is at a frequency of 100 Hz.
- ❖ The AC content at the output of the rectifier is called Ripples.

- ❖ In order to make the output of a rectifier **a pure DC**, the AC component must be removed. This function is carried out by means of electrical filters.
- ❖ The filter circuit must be able to pass the DC and block the 100 Hz AC component.

### 3.5 Shunt Capacitor Filter (Simple Capacitor Filter)

- ❖ The capacitive reactance offered by a capacitor is given by

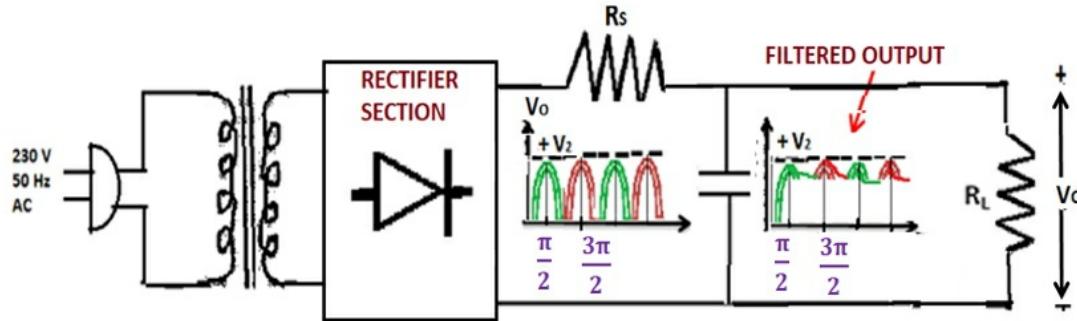
$$X_C = \frac{1}{2\pi f C}$$

- ❖ A sufficiently large capacitance C will offer **a negligible impedance to the 100 Hz Ripple component** of the rectifier.
- ❖ On the other hand, the DC component at frequency 0 Hz will **experience infinite impedance**.
- ❖ When a capacitor connected in parallel to the load at the output of the rectifier it will by-pass the AC Ripple from the load and short circuit this ripple current to the secondary of the transformer.
- ❖ It will also completely block the DC component so that the entire DC current will flow only into the load.
- ❖ The rectifier section is shown symbolically for simplicity. A resistance  $R_S$  is connected in series to limit the load current.

#### Filtered Output Waveform: -

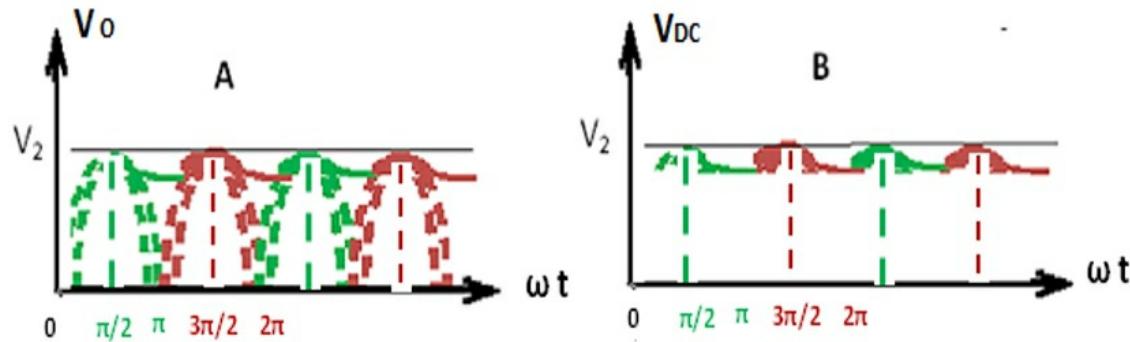
- The output of the FW Rectifier is shown as  $V_O$ . This is applied to the capacitor. At the first half cycle (shown in **GREEN**), the capacitor charges up to the peak of the voltage  $V_2$ , at  $\omega t = \pi/2$ .
- At the instant  $\omega t = \pi/2+$  the potential at the cathode of the diode is  $V_2$ , while the potential at the anode of the diode is lesser than  $V_2$ . Thus, the diode is reverse biased. Therefore, the capacitor has to discharge through the load. This discharge is in an exponential form (shown in **GREEN**) in the figure.
- After sometime of discharging, the potential across the capacitor decreases to a value less than  $V_2$ . By this time the next half cycle appears. This is shown in **MAROON** colour. Now, the potential at the anode is greater than that at the cathode. Therefore, the diode is

forward biased again. This makes the current to flow out from the rectifier and charge up the capacitor again to the peak value  $V_2$  at  $\omega t = 3\pi/2$ .



**Fig- 8.** – The Simple Shunt Capacitor Filter consists of a single capacitor connected in parallel to the load.

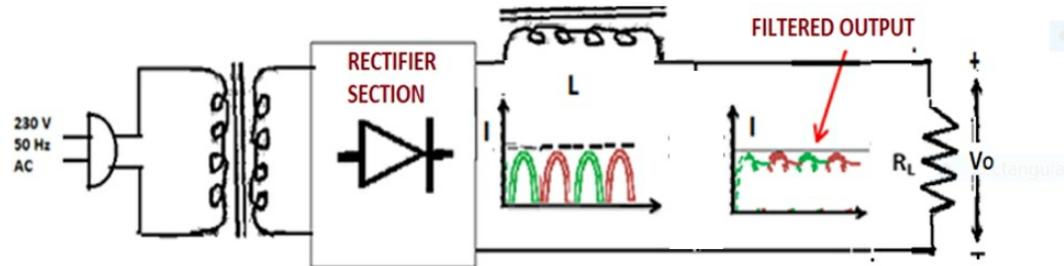
- This process of repeated charging and discharging of the capacitor continues cycle after cycle. The voltage across the capacitor (**Voltage across the Load**) is “Almost Constant”. This is denoted by  $V_{DC}$ .
- During the charging process the load voltage is supplied by the Rectifier and the load current flows out from the diodes. During the discharging process the load voltage is supplied by the capacitor and the load current flows out from the capacitor.



**Fig-9:** - Part (A) shows the output voltage waveform of the FW Rectifier section. Part(B) shows the voltage across the Capacitor.

### 3.6 Series Inductor Filter

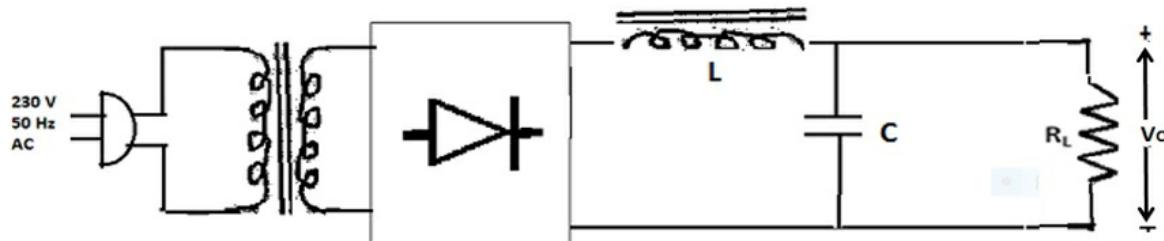
- Inductive reactance offered by an inductor is given by
$$X_L = j \omega L = j 2\pi f L$$
- The inductor will offer very high impedance to the 100 Hz AC Ripple current, while it will offer zero impedance to the DC current.
- If we connect a high inductance coil in series between the rectifier output point and the load, it will block the AC ripple current before it reaches the load while offering a zero-impedance path to the DC current, so that the DC component of the rectifier current will be entirely available at the load.
- The function of ‘Ripple Smoothening’ occurs during a process of repeated energization and de-energization of the inductance by the Ripple Current in much the same manner as that of charging and discharging of a shunt capacitor by the Ripple Voltage as explained in the previous case.
- The load is considered as purely resistive. Hence the waveform of the load voltage is of the same shape as the current in the load.



**Fig- 10:** - The series inductor offers nearly infinite impedance to the 100 Hz AC Ripple current. And zero impedance to the DC component.

### 3.7 L-C Filter or L-Section Filter

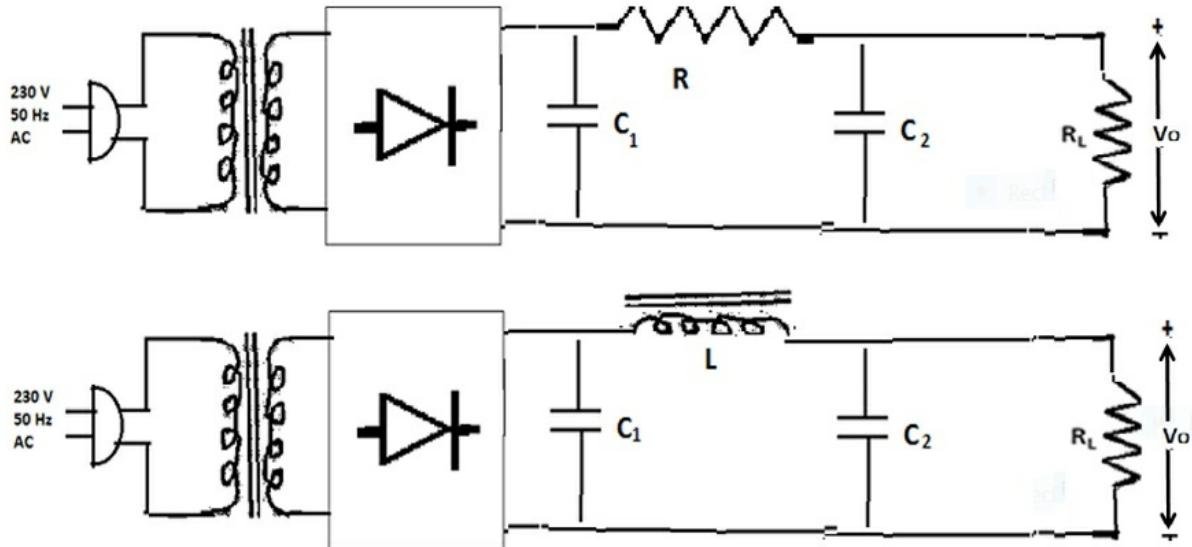
- ✓ The single element filters, namely the Shunt Capacitor Filter, and Series Inductor Filter is unable to completely filter the ripple.
- ✓ In order to remove the ripple further more complex filters are required. These contain combinations of more than one filter element, namely Capacitor or Inductor.
- ✓ The L-C filter (Also called **L-Section Filter**) contains one Series Inductor and one Shunt Capacitor. The remaining AC Ripple from the Inductor is **Shunted Out** by the Capacitor.



**Fig-11:** - The Capacitor in parallel removes the remnants of the 100 Hz ripple which could not be removed by the series Inductor.

### 3.8 R-C and L-C $\pi$ Section Filter

- ✓ The  $\pi$  Section Filter has three filtering elements. These are two Capacitors with either a Resistance or an Inductor being the third element.
- ✓ These three elements are arranged in the form of a ‘ $\pi$ ’.
- ✓ With three filtering elements, the filtering function becomes even better than the L-Section Filter.



**Fig –12:** - Use of three filtering elements namely  $C_1$  and  $C_2$  along with the third element being either the resistance  $R$  or the inductor  $L$  results in better filtering function.

### 3.9 DESIGN OF FILTERS

- The waveform of the output of the rectifier  $V_O$  is shown again in Fig-6. This is a sinusoidal function consisting of only the positive half cycles.
- Figure-13 explains the process in more detail. This is shown with both time ‘ $t$ ’ and angle  $\theta = \omega t$  in the x-axis. In the first part the figure shows the periodicity of a complete sinusoidal cycle of time periodicity ‘ $T$ ’ corresponding to angular periodicity ‘ $360^\circ$ ’.
- In the second part the filtered waveform is shown. This is of **approximately a triangular shape**, having a periodicity of half of the sinusoid.
- The process of **charging of the filter capacitor begins at the angle  $\theta_1$** . At this instant the value of the sinusoidal voltage is  $V_{\min}$ . Charging stops at the peak of a sinusoid, when voltage attains the value  $V_{\max}$ . This occurs during an angle of  $\theta_2$ . This corresponds to the time instant of  $t_2$ . In other words, “**Charging Time =  $t_2$** ”.

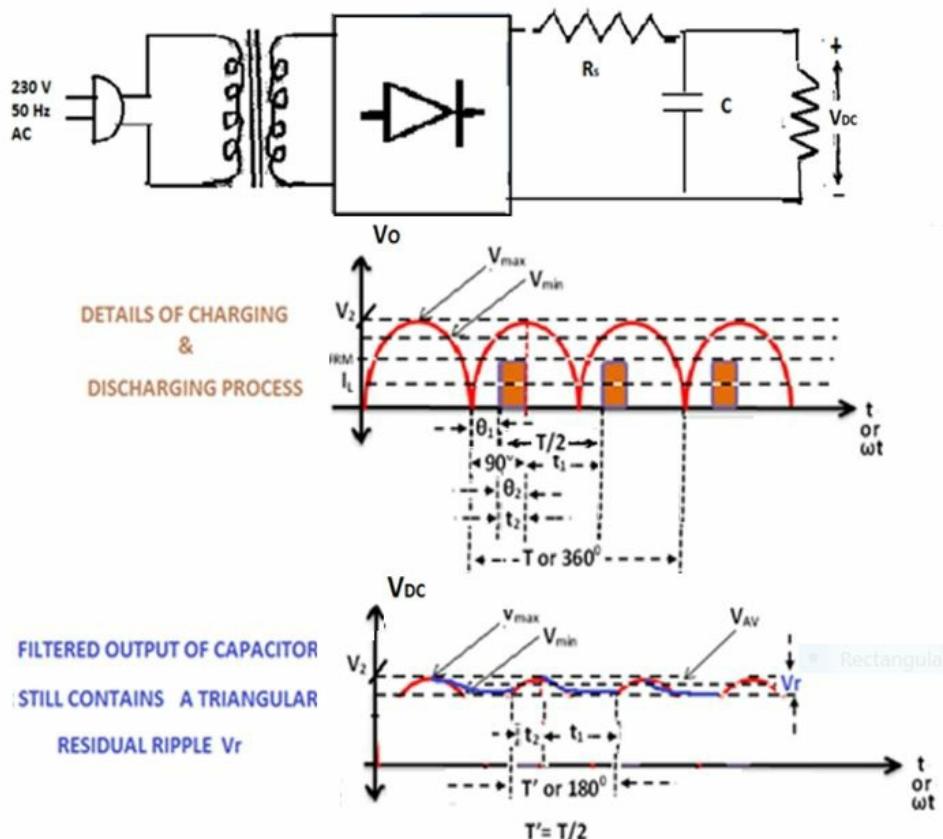
- Considering any one cycle, the instantaneous value of the quantity  $V_{\min}$  will be given by

$$V_{\min} = V_{\max} \sin \theta_1 \dots (1)$$

- From the figure we get  $\theta_2 = 90^\circ - \theta_1$ . Charging occurs once in each half cycle of duration  $T/2$ .

The complete cycle corresponds to  $T$  or  $360^\circ$   
 $\therefore$  Charging Time

$$t_2 = \frac{\theta_2 T}{360^\circ} \dots (2)$$



**Fig- 13:** - The portion of the waveform during charging is shown by **RED** colour and discharging is shown by **BLUE** colour. During charging the capacitor draws a pulsing current shown as  $I_{FRM}$ . The average Load Current is  $I_L$  is assumed to be constant.

- The process of Charging is followed by the process of Discharging. This occurs for a time duration of  $t_1$  during the remaining part of the half cycle.
- Thus, **Discharging Time  $t_1$**  given by

$$t_1 = \left( \frac{T}{2} - t_2 \right) \quad \underline{\dots(3)}$$

- The Average Load Current  $I_L$  is assumed to be constant during charging as well as discharging. Again, it is assumed that, both during charging and discharging, the current in the load is supplied by the Capacitor.
- The voltage across the capacitor is the Filtered Output  $V_{DC}$ . This is the voltage waveform shown in the second part of the figure above.
- This may still contain some **remaining Ripple Voltage  $V_r$** . It may be assumed that the Load is able to tolerate this Ripple. Thus,

$$V_{DC} = V_r$$

- The charge stored in a Capacitor is given by

$$Q = C V$$

Where Charge  $Q = I \cdot t$

This is the charge that is released by the capacitor during the discharging duration  $t_1$  in order to supply the load current  $I_L$ .

$$Q = I_L \cdot t_1$$

During this time the potential across the capacitor is  $V_{DC} = V_r$

$$\therefore C \cdot V_r = I_L \cdot t_1$$

$$\therefore C = \frac{I_L \cdot t_1}{V_r} \quad \dots(4)$$

- Also, **Charge Stored = Charge Discharged**

During Charging Time  $t_2$  the amplitude of the current pulse is  $I_{FRM}$

$$\text{Charge Stored} = I_{FRM} \cdot t_2$$

And **Charge Discharged =  $\{I_L \cdot (t_1 + t_2)\}$**

$$\therefore I_{FRM} = \frac{I_L(t_1 + t_2)}{t_2} \quad \dots(5)$$

- Average Forward Current in the Rectifier section = Load Current  $I_L$

But each diode in the rectifier conducts for only one Half Cycle. This is true for both FW Centre-Tap Rectifier as well as for FW Bridge Rectifier.

Average Forward Current in each Diode

$$I_{F(ave)} = I_L/2 \quad \dots(6)$$

- Each Diode has a **Maximum Current Limit of ' $I_{FSM}$ '**. This is given in the Data Sheet. The series Resistor  $R_s$  in the circuit must be able to limit the maximum current to this value  $I_{FSM}$ . Thus

$$R_s = V_{max} / I_{FSM} \quad \dots(7)$$

### TUTORIAL-3 (A)

#### **DESIGN PROBLEM**

**EXAMPLE -1 (Shunt Capacitor Filter):** - Design a FW Bridge Rectifier for a 20 V, 500  $\Omega$  DC Load which can tolerate a Peak-to Peak Ripple Voltage of 10 % of the rated DC voltage. Design the circuit with a 'Shunt Capacitor Filter'. Calculate  $R_s$ , given  $I_{FSM} = 5$  A. Specify the ratings of the Transformer.

**SOLUTION:** -

#### Calculation of Capacitor Specifications

Given,

$$V_L = V_{av} = 20 \text{ V}$$

Peak-to Peak Ripple

$$V_r = 10 \% \text{ of } V_{av} = 0.1 \times 20 = 2 \text{ V}$$

As shown in the Fig-13,  $V_{av}$  is the mid value between

$V_{max}$  and  $V_{min}$

$$V_{max} = 20 + V_r/2 = 20 + 0.5 \times 2 = 21 \text{ V}$$

$$V_{min} = 20 - V_r/2 = 20 - 0.5 \times 2 = 19 \text{ V}$$

Time Period

$$T = 1/50 = 0.02 \text{ sec.}$$

From equation 1 we get charging and discharging angle as

$$\theta_1 = \sin^{-1} \left( V_{min}/V_{max} \right)$$

$$\theta_1 = \sin^{-1} (19/21) = 65^\circ$$

$$\theta_2 = 90 - \theta_1 = 90 - 65 = 25^\circ$$

From equation 2 we get Charging time

$$t_2 = \theta_2 T / 360^\circ$$

$$t_2 = (25 \times 0.02) / 360 = 0.0014 \text{ sec}$$

From equation 3, Discharging Time is

$$t_1 = \left( \frac{T}{2} - t_2 \right) = \left( \frac{0.02}{2} - 0.0014 \right) = 0.0086 \text{ sec}$$

Load Current

$$I_L = V_{AV} / R_L = 20 \text{ V} / 500 \Omega = 0.04 \text{ A}$$

Now, from equation 4

$$C = I_L t_1 / V_r$$

$$C = (0.04 \times 0.0086) / 2$$

$$C = 0.000172 \text{ F} = 172 \mu\text{F}$$

- Choose a standard value for Capacitor of  $C = 200 \mu\text{F}$ .

### **Calculation for Surge Limiting Resistance**

From the Data Sheets  $I_{FSM}$  for the diode is 5 A.

From equation 5, value of "Surge Limiting Resistance" is

$$R_S = V_{max}/I_{FSM} = 21 \text{ V} / 5 \text{ A} = 4.2$$

- Choose a standard value for Resistance of  $R_S = 5 \Omega$ .

### **Transformer Specifications**

From the waveform in Fig-6

- $V_{max} = V_2$  of the secondary side of transformer.
- The transformer secondary voltage must be equal to  $(V_{max} + \text{drop across the diode})$ .
- In a Bridge Rectifier there are 2 Si diodes in series in each half cycle. For each of the Si diodes Forward Voltage Drop  $V_Y = 0.7 \text{ V}$ .

**Therefore secondary r.m.s. voltage of the transformer must be**

$$\begin{aligned} V_{Srms} &= (1/\sqrt{2}) \cdot (V_{max} + 2V_Y) \\ &= (1/\sqrt{2}) \cdot (21 + 2 \times 0.7) \\ V_{Srms} &= 15.13 \text{ V} \end{aligned}$$

As a thumb rule for calculating current at the secondary we use

$$I_{Srms} = 1.6 (I_{LAV})$$

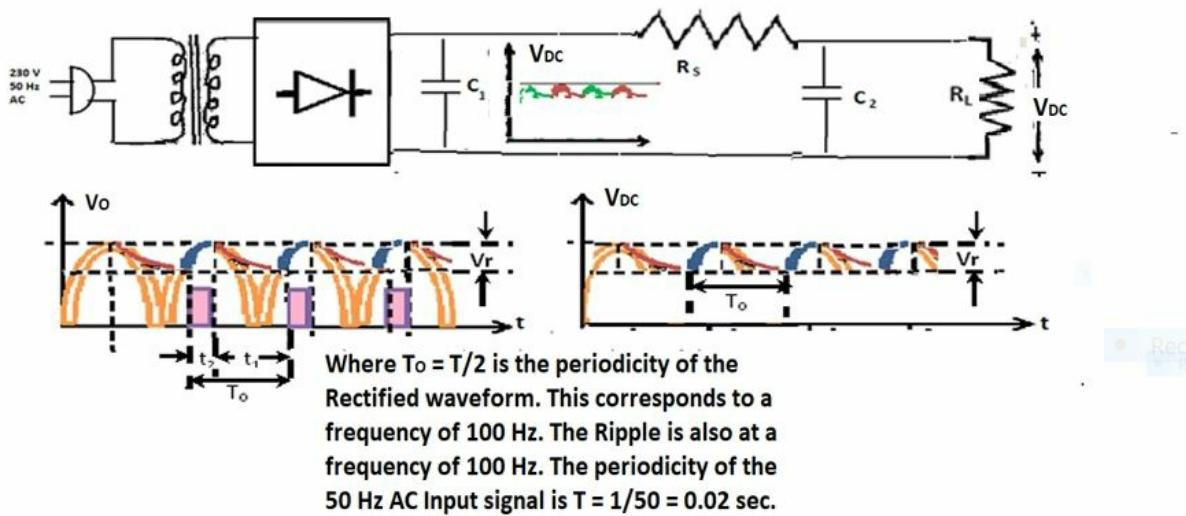
$$= 1.6 \times 0.04 = 0.064 \text{ A}$$

$$\text{Or } I_{Srms} = 64 \text{ mA}$$

- Chose Step Down Transformer with the following specifications –

**Primary 230 V Secondary 16 V, 100 mA ::(Turns Ratio 230 : 16)**

### 3.10 R-C $\pi$ Section Filter Design



**Fig –14: - R-C  $\pi$  Section Filter with the waveforms.**

- After the first capacitor  $C_1$  filters the rectifier output a Ripple  $V_r$  remains.
- This ripple  $V_r$  is periodic with a periodicity of  $T_0 = T/2$  and is of approximately triangular in shape.
- Any Periodic waveform can be expanded in a Fourier series as

$$V_{r(t)} = \frac{1}{T_0} \int_{-T_0/2}^{+T_0/2} V_{r(t)} \sin(2\pi n f_0 t) dt$$

$$V_{r(t)} = V_0 + \sum_{n=0}^{\infty} V_n \cos(2\pi n f_0 t + \Phi_n)$$

Where 'n' is the set of Integers,  $n = 1, 2, 3, \dots$

- This expression contains of a **DC quantity  $V_0$**  and a sequence of sinusoids at amplitudes given by  $V_n$ , at harmonic frequencies  $n f_0$  where  $n$  takes integer values  $n = 1, 2, 3, \dots$

- The term  $V_n$  is evaluated in terms of the Fourier Integrals  $A_n$  and  $B_n$ , as follows-

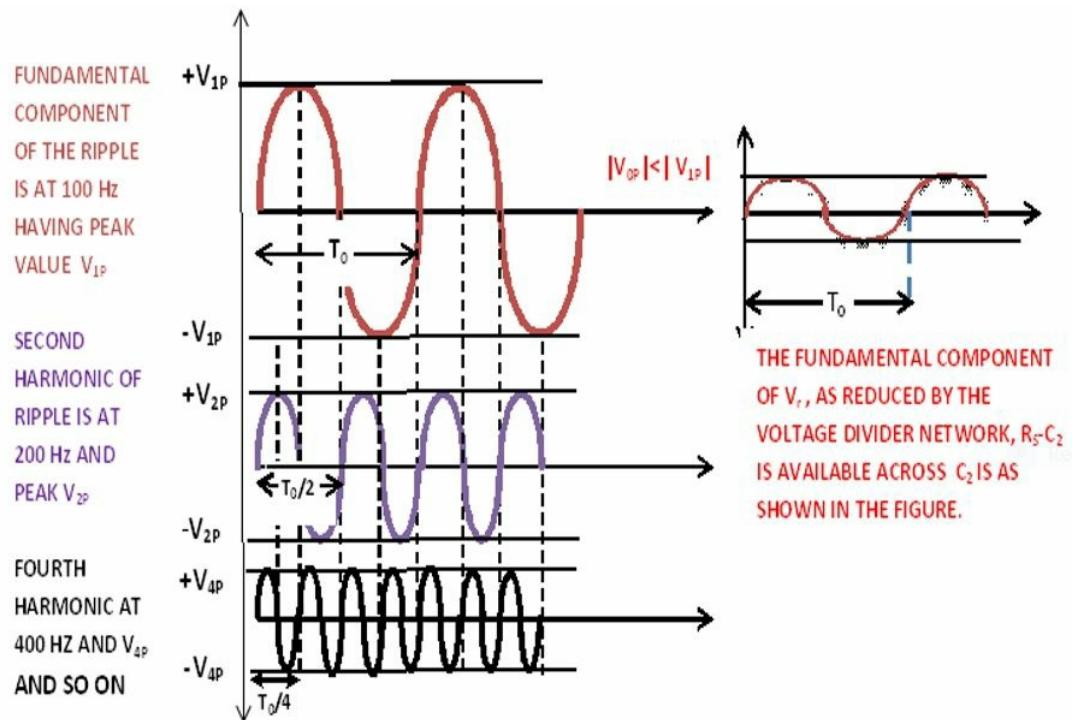
$$V_n = \sqrt{(A_n^2 + B_n^2)}$$

$$A_n = \frac{2}{T_0} \int_{-T_0/2}^{+T_0/2} V_r(t) \sin(2\pi n f_0 t) dt$$

&

$$B_n = \frac{2}{T_0} \int_{-T_0/2}^{+T_0/2} V_r(t) \cos(2\pi n f_0 t) dt$$

In view of the above, the Fourier series Expansion of the ripple voltage  $V_r$  is as follows



**Fig.15:** - The Fundamental and some of the Harmonic components at the output of the first capacitor  $C_1$  of the R-C  $\pi$ -Section Filter.

The Fundamental Component occurs at the same frequency as the given waveform, i.e.,  $f_0 = 1/T_0$ . This waveform is of a triangular shape,

as observed from **Fig.-14**. A Triangular waveform has a Peak value given by

$$V_{1P} = V_r / \pi \quad \dots (8)$$

- The other Harmonics are at progressively decreasing amplitudes and increasing frequencies. These are shown in the Fig.-15.
- This Triangular Ripple  $V_r$  is the input to the  $R_S C_2$  Voltage Divider network. This attenuates the triangular wave  $V_r$  to a lesser amplitude voltage across the second capacitor  $C_2$ , whose Fundamental component is shown in the figure.
- By voltage Divider Rule, Voltage across  $C_2$  is given by

$$V_{C2} = V_0 = \frac{V_r X_{C2}}{\sqrt{(R_S^2 + X_{C2}^2)}} \quad \dots (9)$$

From the equation above we get

$$X_{C2} = \frac{R_S}{\sqrt{\left(\left(V_r/V_0\right)^2 - 1\right)}}$$

Since Ripple is assumed to be reduced, we have the condition,  $V_0 < V_r$

$$\therefore \left(V_r/V_0\right)^2 \gg 1$$

Using this approximation, we get,

$$X_{C2} = \frac{R_S}{V_i/V_0} \quad \dots (10)$$

**Thus, if  $R_S$  is known, the value of the Capacitor  $C_2$  required to reduce the ripple to the desired level of  $V_0$  is calculated from equation (10). Conversely, if  $C_2$  is known, the required value of  $R_S$  can be calculated.**

### TUTORIAL-3 (B)

**EXAMPLE-2:** -The Ripple Voltage remaining across  $C_1$  is  $V_r = 2$  V. Let  $R_S = 22 \Omega$ ,  $C_1 = C_2 = 150\mu F$ , Load Voltage = 20V and Load Current = 40 mA. Calculate  $V_{o(DC)}$  and Ripple at the output for a  $RC\pi$  Filter.

**SOLUTION:** -

$$V_{o(DC)} = V_{L(AV)} - I_L R_S$$

∴  $\underline{V_{o(DC)}} = 20 - (0.04 \times 22)$   
 $= 19.12 \text{ V}$

Assuming the Ripple across  $C_1$  to be a Triangular waveform,

Peak of the Fundamental of the Ripple is given by equation (8).  
Substituting  $V_r = 2V$ , we have

$$V_{1P} = \frac{V_r}{\pi} = \frac{2}{\pi} = 0.636 \text{ V} = 636 \text{ mV}$$

Given  $C_2 = 150 \mu F$ ,

$$X_{C2} = \frac{1}{2 \pi f_0 C_2} = \frac{1}{2\pi \times 100 \times 150 \times 10^{-6}} = 10.61 \Omega$$

(Since Ripple Frequency is 100 Hz)

From equation (9) Peak of the Ripple at the output

$$V_{C2} = V_0 = \frac{V_i X_{C2}}{\sqrt{(R_S^2 + X_{C2}^2)}} = \frac{0.636 \times 10.61}{\sqrt{(22^2 + 10.61^2)}} = 0.277 \text{ V (peak)}$$

∴ Peak-to-Peak Ripple =  $2 V_{C2} = 2 \times 0.277 = 0.554 \text{ V or } 554 \text{ mV}$

### DESIGN PROBLEM

**EXAMPLE-3 :-** To design a Bridge rectifier with  $RC\pi$  filter to supply a Load rated at 25 V , 55 mA. Let the Ripple Tolerance of the Load be 0.5 % of average load voltage. Calculate  $R_S$  assuming Si Diodes having  $I_{FSM} = 4A$ . Calculate the required value of  $C_1$  &  $C_2$  if Ripple output of  $C_1$  is to be reduced by 10 % by the  $R_S C_2$  combination. Give specifications of the step-down transformer to be used.

**SOLUTION:-**

#### Filter Specifications

Given:  $V_{L(AV)} = 25 \text{ V}$  :  $I_L = 55 \text{ mA}$  : Ripple Tolerance is 0.5

% of  $V_{L(AV)}$

Therefore, Maximum of Tolerable Ripple voltage is

$$V_{0(r)} = 0.005 \times 25 = 0.125 \text{ V} = 125 \text{ mV.}$$

The  $R_S C_2$  combination is to reduce the Ripple to this value.

Since reduction by this section is specified as 10 % of the input to this section,

Therefore, Input Ripple to  $R_S C_2$  section =  $V_{i(r)} = 0.125 / 0.1 = 1.25 \text{ V}$

This is the value of the Peak-to-Peak Ripple output of the first Capacitor  $C_1$  of the circuit.

Therefore,  $V_{0(MAX)}$  at output of  $C_1$  is

$$\begin{aligned} V_{0(MAX)} &= V_{L(AV)} + V_r / 2 \\ &= 25 + 1.25/2 = 25.625 \text{ V} \end{aligned}$$

&

$$\begin{aligned} V_{0(MIN)} &= V_{L(AV)} - V_r / 2 \\ &= 25 - 1.25/2 = 24.375 \text{ V} \end{aligned}$$

$$\begin{aligned} \therefore \theta_1 &= \sin^{-1} (V_{0(MIN)} / V_{0(MAX)}) \\ &= \sin^{-1} (24.375/25.625) = 72^\circ \\ \theta_2 &= 90 - \theta_1 = 90 - 72 = 18^\circ \end{aligned}$$

$$\therefore \text{Charging Time } t_2 = \theta_2 \times T / 360 = |18 \times 0.02 / 360| = 0.001 \text{ s}$$

$$\therefore \text{Discharging Time } t_1 = (T/2) - t_2 = 0.01 - 0.001 = 0.009 \text{ s}$$

$$\therefore C_1 = (I_L t_1) / V_r = 0.055 \times 0.009 / 1.25 = 0.000396 \text{ F} = 396 \mu\text{F}$$

$$R_S = V_{0(MAX)} / I_{FSM} = 25.625 / 4 = 6.4 \Omega$$

Rectangular Snip

$$\begin{aligned} X_{C2} &= R_S / \sqrt{(V_i / V_0)^2 - 1} \\ &= 6.4 / \sqrt{(1.25 / 0.125)^2 - 1} \\ &= 0.64 \Omega \end{aligned}$$

$$\begin{aligned} C_2 &= 1 / 2\pi f_0 X_C \\ &= 1 / 2\pi \times 100 \times 0.64 \\ &= 0.002475586 \text{ F} = 2475.586 \mu\text{F} \end{aligned}$$

### Transformer Specifications

Since there are 2 Diodes in each half Cycle, the Peak of the

Secondary Voltage must be

$$\begin{aligned}V_{SP} &= V_{0(MAX)} + 2 V_F \\&= 25.625 + 2 \times 0.7 = 27.025 \text{ V}\end{aligned}$$

$$\therefore V_{S \text{ rms}} = 1/\sqrt{2} V_{SP} = 19.01$$

As a Rule of the thumb

$$I_{S \text{ rms}} = 1.6 I_{L(AV)} = 1.6 \times 0.055 = 0.088 \text{ A} = 88 \text{ mA}$$

Therefore, we require a 230 V: 20 V, 100 mA Step-down transformer.

### 3.11 ZENER DIODE VOLTAGE REGULATOR

The purpose of a Rectifier is to replace a DC battery which supplies a constant DC. In practice there occur two factors that tend to cause the DC voltage to fluctuate.

a). Variable Load Current due to load resistance variations.

b). Power Supply Variations in the primary AC supply line.

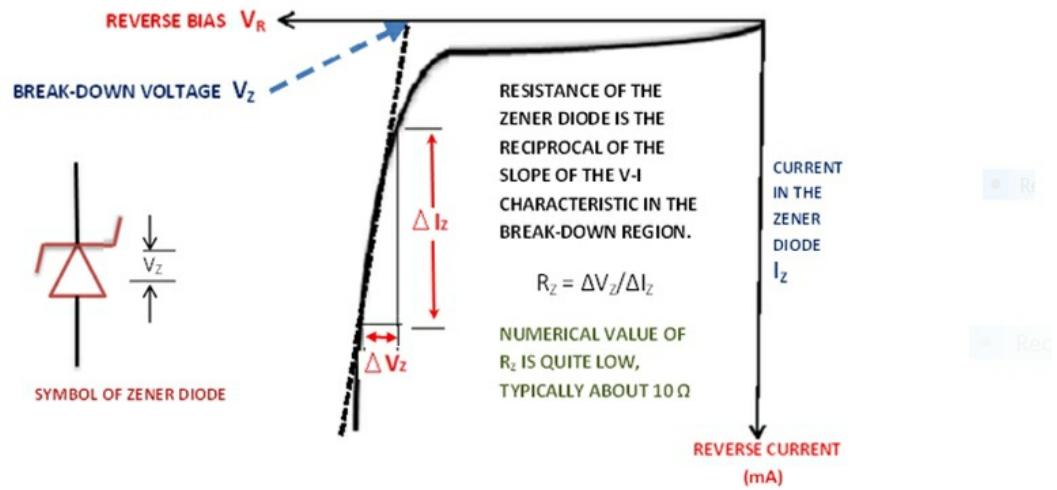
**Voltage Regulation** is defined in the form of a percentage of voltage fluctuation at the load, as –

$$V.R. = \left\{ \frac{(V_{Lmax} - V_{Lmin})}{V_{Lmax}} \right\} \times 100 \quad \underline{\underline{(11)}}$$

In order to overcome Load Voltage Fluctuations a **Voltage Regulator** is to be included with Rectifiers.

**Zener Diode:** - Zener Diode is a “Special Purpose Diode” made of Silicon that is designed to operate at Break-Down Region of the diode characteristic.

- ❖ Recall that when the Reverse Bias on a diode is made extremely high it goes into the Break-Down Region of its characteristic. The Break-Down Region for a Zener Diode is shown in greater details in the Fig-16.

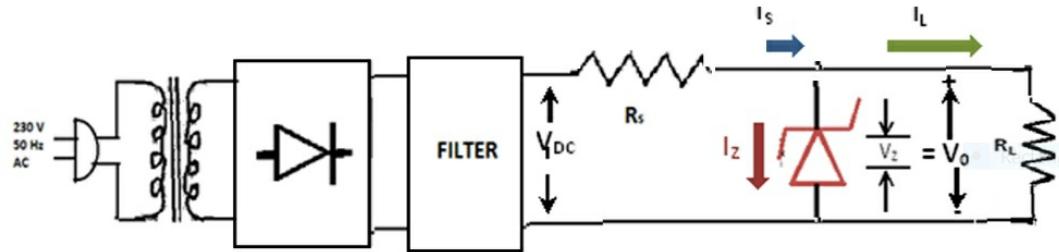


**Fig-16:** - *Circuit Symbol and Break-Down Region of the V-I Characteristic of a Zener Diode. Formula for calculation of  $R_Z$  and its typical value is shown.*

- ❖ A Zener Diode is designed in such a way that it has a very sharp slope in the Break-Down Region. Thus, there is a very large  $\Delta I_Z$  corresponding to a very small  $\Delta V_Z$ .
- ❖ This very small change  $\Delta V_Z$  can be considered to be negligible. In other words, the **voltage across the Zener Diode remains essentially constant at  $V_Z$ , while the current through it may vary widely over a large range  $\Delta I_Z$ .**

### Working Principle of Zener Voltage Regulator

- The circuit of a Rectifier with a “Zener Diode Voltage Regulator” is shown in the Fig- 17.
- Filter section of a rectifier often has a series resistance  $R_s$ . This resistance is shown outside the Filter Block in this figure.



**Fig- 17: -**

- The magnitude and polarity of  $V_{DC}$  is such that it is reverse biases the Zener Diode at the limiting point of Breakdown.

$$|V_{DC}| \geq V_Z$$

- Since the Zener Diode will operate in the Break-Down Region, voltage across the Zener Diode will remain essentially constant at  $V_Z$ , irrespective of the current flowing through it. Since  $V_Z$  remains constant, the voltage across the load is also constant.

$$V_o = V_Z$$

- Recall the “Factors Effecting Voltage Regulation”
  - Variable Load Current due to load resistance variations.**
  - Power Supply Variations in the primary AC supply line.**

#### **(a) Variable Load Current due to load resistance variations.**

- The DC Load Current  $I_L$  will vary with Load Resistance.
- This variable load current flows through (1) the secondary coil of the transformer, (2) The Series Resistance of the filter section and (3) The internal resistance of the diodes. Due to this, there occurs a variable voltage drop, resulting in a variable voltage appearing across the load.
- In the Fig. 17 the current  $I_S$  that is flowing out of the rectifier, is divided into two parts,  $I_L$  and  $I_Z$ . If the load resistance is varying,

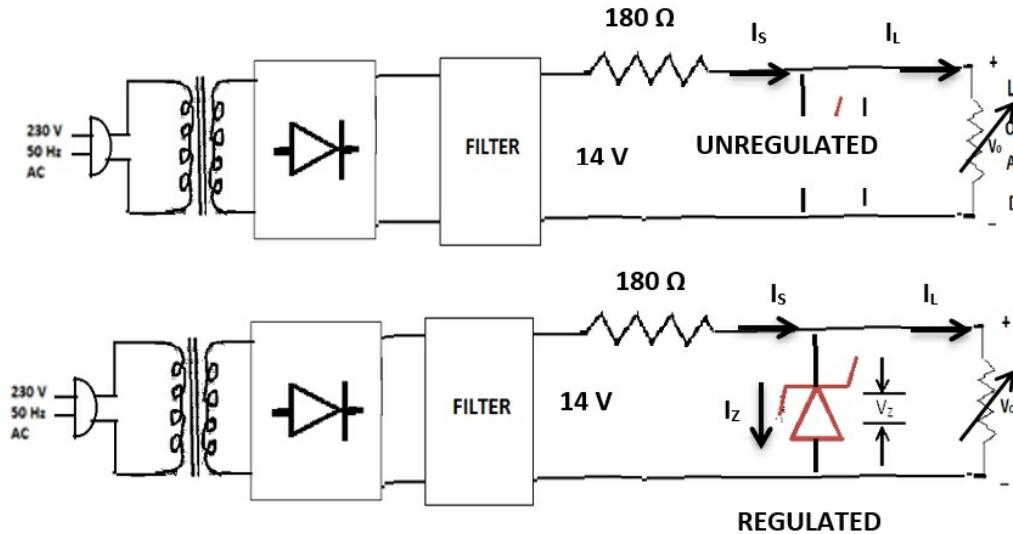
the net current  $I_S$  would vary. This change in current will be absorbed by the Zener Diode in the form of a larger current swing  $\Delta I_Z$ . However, since the Zener Diode is in Break-Down condition, we have that  $V_Z$  is essentially constant.

- Thus,  $V_0 = V_Z$  remains constant.
- Dynamic Resistance is defined as the reciprocal of the slope of the V-I Characteristic. Since the slope of the V-I Characteristic is very high, the dynamic resistance of the Zener Diode is very small.

$$R_Z = \frac{\Delta V_Z}{\Delta I_Z} \quad \dots(12)$$

### **TUTORIAL-4 (A)**

**Example-4 :-** Calculate  $V_{Lmax}$  and  $V_{Lmin}$  and Voltage Regulation (V.R.) under two conditions, (i) when Zener Diode is absent and (ii) when Zener Diode is used, in the given circuit where the load resistance varies from  $2000 \Omega$  to  $\infty$  (infinity). The rated DC load voltage is 12 V and the resistance of the Zener Diode is  $R_Z = 7 \Omega$ . Assume constant AC power supply



### **SOLUTION :-**

#### **(i) UREGULATED (ZENER DIODE ABSENT)**

In this case  $I_L = I_S$ . This produces a voltage drop across  $R_S$ .

When the Load Resistance is minimum ( $2000 \Omega$ ), the Load Current is Maximum.

$$I_{L\max} = \frac{V_L}{R_L} = \frac{12 \text{ V}}{2000 \Omega} = 0.0060 \text{ A} = 6 \text{ mA}$$

Voltage Drop across  $R_S = I_S \cdot R_S = I_L R_S$

$$\therefore I_S R_S = 0.006 \times 180 = 1.08 \text{ V}$$

$$\therefore V_{L\min} = V_{0\min} = 14 - 1.08 = 12.92 \text{ V}$$

When the Load Resistance is infinity (maximum), Load Current is zero.

Therefore

$$I_S = I_L = 0 \quad \& \quad V_{0\max} = 14 \text{ V}$$

Using Eq. (11) we get

$$\% VR = \frac{(14 - 12.92)}{14} \times 100 = 7.28 \%$$

Thus, the output voltage has a **7.28 % variation, which is not desirable.**

## (ii) REGULATED WITH ZENER DIODE VOLTAGE REGULATOR

When a Zener Diode is used.

$$I_S = I_L + I_z$$

$$\begin{aligned} \text{Where } I_S &= (V_{DC} - V_Z)/R_S \\ &= (14 - 12)/180 \\ &= 0.011 \text{ A} = 11 \text{ mA}. \end{aligned}$$

When the Load Resistance is  $2000 \Omega$  (minimum) and at the rated Load voltage of 12 V, we get

$$I_{L\max} = \frac{V_L}{R_L} = \frac{12 \text{ V}}{2000 \Omega} = 0.006 \text{ A} = 6 \text{ mA}$$

$\therefore$  Minimum Change in Current

$$\begin{aligned} \Delta I_{Z\min} &= I_S - I_{L\max} \\ &= 11 - 6 = 5 \text{ mA} = 0.005 \text{ A} \end{aligned}$$

Net Voltage Drop across Zener Diode

$$\begin{aligned} V_{Z\min} &= V_Z + \Delta V_Z = V_Z + \Delta I_{Z\min} R_Z \\ &= 12 + 0.005 \times 7 = 12.035 \text{ V} \end{aligned}$$

$$V_{L\min} = V_{Z\min} = 12.035 \text{ V}$$

When the Load Resistance is infinity (maximum), Load Current is zero.

$$\therefore I_S = I_Z = \Delta I_{Z\max} = 11 \text{ mA} = 0.011 \text{ A}$$

Drop across Zener Diode

$$V_{Z\max} = V_Z + \Delta I_{Z\max} R_Z$$

$$V_{Z\max} = 12 + 0.011 \times 7 = 12.077 \text{ V}$$

Since  $V_{Z\max} = V_{L\max}$ , we may substitute this I Eq.-11 to get

$$\% \text{ VR} = \frac{(12.077 - 12.035)}{14} \times 100 = 0.35 \%$$

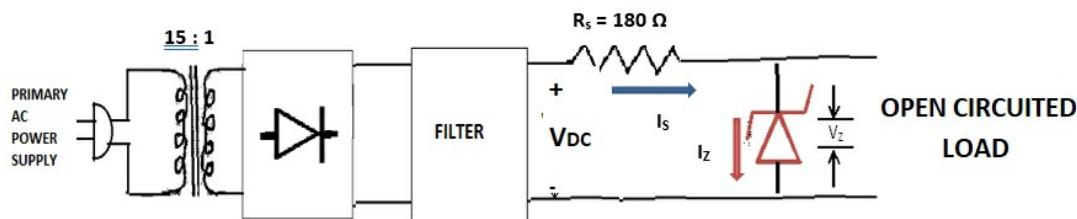
Thus, the output voltage has only 0.35 % variation.

**(b). Power Supply Variations in the primary AC supply line.**

- ✓ AC power supply is not always constant at 230 V RMS. In that case the voltage at the secondary of the step-down transformer will also fluctuate. The quantity Peak Voltage at the Secondary,  $V_2$  is variable. This results in the load voltage being variable and results in a high amount of V.R.
- ✓ When a Zener Diode is used, the variation in  $V_2$  will result in a variation  $\Delta V_Z$  in the Zener Diode. The resulting variation in the current  $\Delta I_Z$  will be absorbed by the Zener Diode. This will result in a lowering of the voltage fluctuation across the load.

### TUTORIAL-4 (B)

**EXAMPLE- 5 :-** The turns-ratio of the step-down transformer in the figure is 15 : 1. The Primary AC power supply varies from 240 V to 180 V. the circuit uses a Zener Diode with  $V_Z = 10 \text{ V}$  and  $R_Z = 10 \Omega$ . Assume open circuited load and calculate V.R. What is the value of V.R. if the Zener Diode was absent?



**SOLUTION :-**

### IN THE ABSENCE OF ZENER DIODE

Maximum RMS Primary voltage = 240 V. & Turns ratio = 15 : 1  
 Maximum RMS Secondary voltage is  
 $V_{SRMS} = 240/15 = 16 \text{ V}$

$\therefore$  Peak-to-Peak Secondary Voltage  
 $V_m = \sqrt{2} V_{SRMS} = \sqrt{2} \times 16 = 22.63 \text{ V}$

$$\therefore V_{DC} = \frac{2 V_m}{\pi} = \frac{2 \times 22.63}{\pi} = 14.4 \text{ V}$$

Where  $V_{DC} = V_{0max} = 14.4 \text{ V}$

Minimum RMS Primary voltage = 180 V.

Minimum RMS Secondary voltage is

$$V_{SRMS} = 180/15 = 12 \text{ V}$$

$\therefore$  Peak-to-Peak Secondary Voltage  
 $V_m = \sqrt{2} V_{SRMS} = \sqrt{2} \times 12 = 16.97 \text{ V}$

$$\therefore V_{DC} = \frac{2 V_m}{\pi} = \frac{2 \times 16.97}{\pi} = 10.8 \text{ V}$$

This is  $V_{0min} = 10.8 \text{ V}$

Substitute this in Eq.-11

$$\% VR = \frac{(14.4 - 10.8)}{14.4} \times 100 = 25 \%$$

### WHEN REGULATED WITH ZENER DIODE

In the Open Circuited Load condition,

$$I_s = I_z$$

By Kirchhoff's Voltage Law,

$$V_{DC} = I_s R_s + V_z + I_z R_z$$

$$\therefore V_{DC} = \frac{(V_{DC} - V_z)}{(R_s + R_z)} = I_z$$

We had

$$V_{DCmax} = V_{Omax} = 14.4 \text{ V}$$

$$V_{DCmin} = V_{Omin} = 10.8 \text{ V} \quad \& \quad V_Z = 10 \text{ V}$$

$$I_{S((max))} = I_{Z(max)} = \frac{(V_{DC(max)} - V_Z)}{(R_S + R_Z)}$$

$$I_{Z(max)} = \frac{(14.4 - 10)}{(180 + 10)} = 0.02316 \text{ A} = 23.16 \text{ mA}$$

$\therefore$  Max output voltage across the load at Open Circuit

$$V_{Lmax} = V_Z + I_{Zmax} R_Z = 10 + 0.02316 \times 10 = 10.2316 \text{ V}$$

AND

$$I_{S((min))} = I_{Z(min)} = \frac{(V_{DC(min)} - V_Z)}{(R_S + R_Z)}$$

$$I_{Z(min)} = \frac{(10.8 - 10)}{(180 + 10)} = 0.0042 \text{ A} = 4.2 \text{ mA}$$

$\therefore$  Minimum output voltage across the load at Open Circuit

$$V_{Lmin} = V_Z + I_{Zmin} R_Z = 10 + 0.0042 \times 10$$

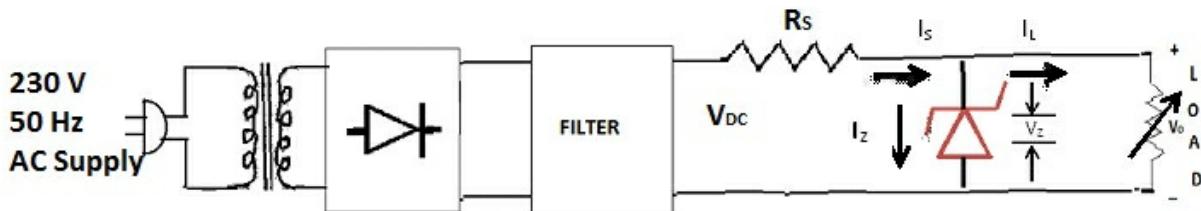
$$= 10.042 \text{ V}$$

$$\therefore \text{V. R.} = \frac{(10.2316 - 10.042)}{10.2316} \times 100 = 1.85 \%$$

Thus, the output voltage has 1.85 % variation, which is quite acceptable.

## DESIGN PROBLEM

**EXAMPLE-6:** - The Rectifier-Filter section provides an output varying from 15 V to 20 V. The load current varies from 20 mA to 100 mA. Calculate the minimum value of  $R_S$  required for acceptable voltage regulation. The rated load voltage is 10 V.



## SOLUTION :-

Worst case scenario is when the supply voltage is minimum and the load current is maximum. The value of the resistance  $R_S$  is to be calculated for this case.

$$R_{Smax} = \frac{(V_{DCmin} - V_Z)}{I_{Lmax}}$$

Since

$V_O = 10$  V, we must use a Zener Diode with  $V_Z = 10$  V.

Given that  $V_{Omin} = 15$  V.

$$R_{Smax} = \frac{(15 - 10)}{0.1} = 50 \Omega$$

- While designing the Filter Section, we had calculated the MINIMUM value of  $R_S$  required to keep the current through the diode below the maximum permissible current IFSM. In this section we have calculated the MAXIMUM value of  $R_S$  required to keep the V.R. within a permissible limit.
- Since we have to use a single resistor, we have to choose the higher value resistor between these two.

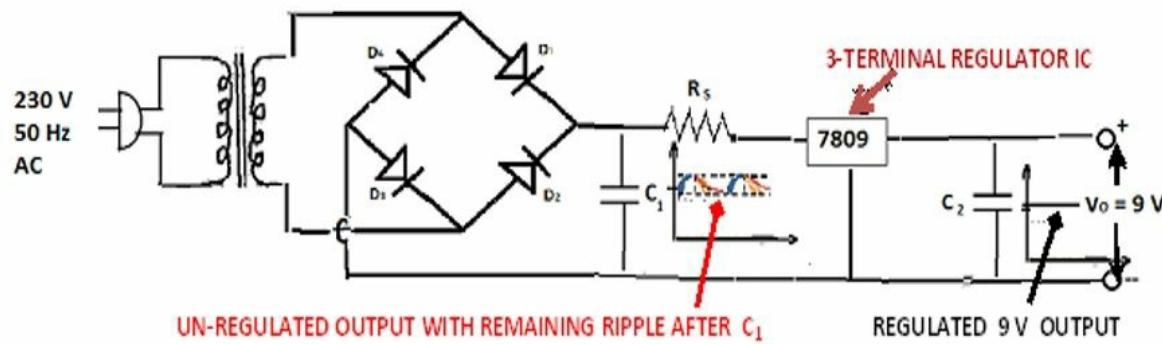
## 3.12 BATTERY ELIMINATOR

(A COMPLETE DC POWER SUPPLY UNIT)

The Design Requirements

1. A Rectifier Section that provides a  $V_{DC}$  output slightly greater than the rated DC voltage of the load to be connected.
2. A suitable Filter Section to keep the ripple within permissible limits.
3. A Voltage Regulator Section. The Zener Diode Voltage Regulator is a rather simple solution. **In practice more sophisticated 3-terminal Regulator ICs are used. A popular series of such ICs is the 78-XX series.** In these the XX refer to the numerical value of the rated DC output required for the load. For example, for a load rated at 5 V DC then a regulator IC with **IC number 7805** is to be used; if the load is rated at 12 V DC then a regulator IC with **IC number 7812** is to be used and so on.

4. A complete Battery Eliminator Unit for supplying a DC output voltage of 9 V is shown in the Fig-18. This is shown with a Bridge Rectifier Section. **Recall that for lower DC voltage rated loads a Centre-Tap Rectifier is more suitable.** The circuit is shown with the **R-C  $\pi$  Filter**. It is to be noted that any other configuration of the filters can also be used.
5. The values of the Resistance  $R_S$  and Capacitances used in the circuit are based on calculations done on lines similar to the numerical examples given above.



**Fig-18:** - A complete DC Power Supply Unit for supplying 9 V regulated DC to a load connected at the output terminal. This uses an IC Voltage Regulator “**7809**”. For loads rated above 6 V it is advisable to use a Bridge Rectifier. If a lower voltage rated load is to be driven then a Centre-Tap Rectifier can also be used.

# **CHAPTER – IV**

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## **THE SPECIAL APPLICATIONS OF DIODES**

**and**

### **SPECIAL PURPOSE DIODES**

#### ***SPECIAL APPLICATIONS OF DIODES***

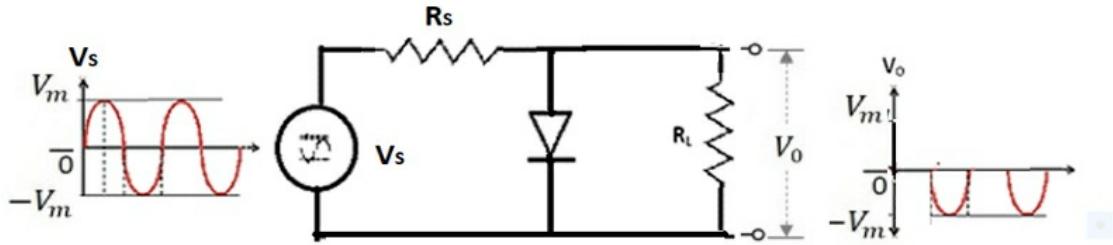
The primary application of the Diode is in the rectifiers. However, in addition to this, the Diode finds a number of other applications. Also, that, there are a number of Special Purpose Diodes, used in a variety of specialized applications.

#### **SECTION- 1**

##### **4.1 Diode Circuits used for Special Applications**

**(1) VOLTAGE CLIPPER:** - A Voltage Clipper is a circuit that “Clips off” or “Removes” a portion of an AC input voltage signal. There are broadly two types of Clippers, namely, **Positive Clipper** and **Negative Clipper**.

**Positive Clipper:** - A Positive Clipper is used to Clip-Off a portion or the whole of the positive half cycle of an AC. The circuit diagram is shown in Fig- 1 below.



**Fig – 1: - Positive Clipper**

**PRINCIPLE: -**

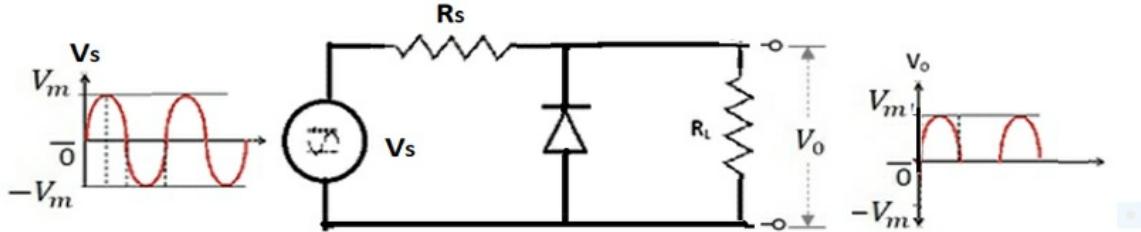
- During the positive half cycle, the diode is Forward Biased. Hence it is equivalent to a short circuit. Since the voltage across the short circuit is zero, the output voltage  $V_O$  is also zero.
- During the negative half cycle, the diode is Reverse Biased. Hence current flows out from the AC source through the load resistance ‘ $R_L$ ’ and the current limiting series resistance ‘ $R_S$ ’ , so that the voltage across the load has the same shape as the negative half cycle.
- The output is a voltage waveform where the positive half cycle being **clipped off**. Hence the name “Positive Clipper”.
- The two resistances  $R_S$  and  $R_L$  form a Voltage Divider so that output voltage during Negative half-Cycle is

$$V_0 = \frac{R_L}{(R_L + R_S)} V_S \quad \dots(1)$$

If  $R_S$  is negligible compared to  $R_L$  then we have

$V_O = V_S$  (**During Negative Half Cycle Only**).

**Negative Clipper:** - The circuit of a **Negative Clipper** is shown in Fig-2.



**Fig – 2: - Negative Clipper**

#### PRINCIPLE: -

- During the positive half Cycle, the diode is Reverse Biased. Hence it offers an infinite resistance. The current flows through the resistance  $R_S$  into the load. Therefore, the voltage developed across the load is of the same shape as that of the input waveform.
- During the negative half cycle, the diode is Forward Biased and hence it acts as a short circuit, so that it by-passes the current from the load. Therefore, no current flows into the load and the voltage developed across it is zero.
- The expression for output voltage is the same as that for the Positive Clipper but it is applicable only during the negative half cycle.
- **A Half Wave Rectifier removes the negative half cycle from the AC input. Hence a HW rectifier is also a Negative Clipper.**

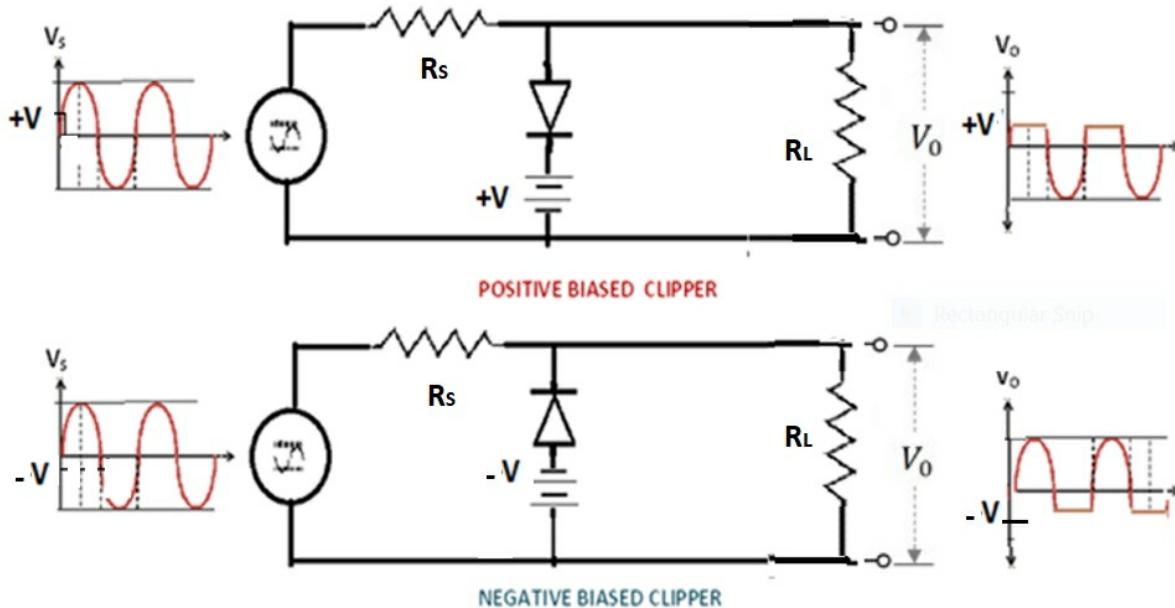
**Biased Clipper:** - A Biased Clipper will clip off the input voltage at any desired value of voltage  $+V$  or  $-V$ . Accordingly, we have (a) Positive Biased Clipper (b) Negative Biased Clipper. The circuit diagrams are shown in the Fig-3 below.

#### **Positive Biased Clipper**

#### PRINCIPLE: -

- At  $t = 0$  of the positive half cycle,  $V_s = 0$ . The diode is reverse biased by the DC battery. As resistance of the diode is infinite, the current flows only into the load and the voltage developed across it has the same shape as the input waveform.

- At some later time instant  $t = t_1$ , as soon as  $V_s = +V$ , the diode goes into forward bias. Now it offers zero resistance. Therefore, the current is bypassed from the load. Since no current flows into it, the voltage developed across the load remains **constant at  $+V$** . This remains constant for the remaining portion of the positive half cycle till when the input voltage remains greater than  $+V$ .



**Fig – 3: - Biased Clipper**

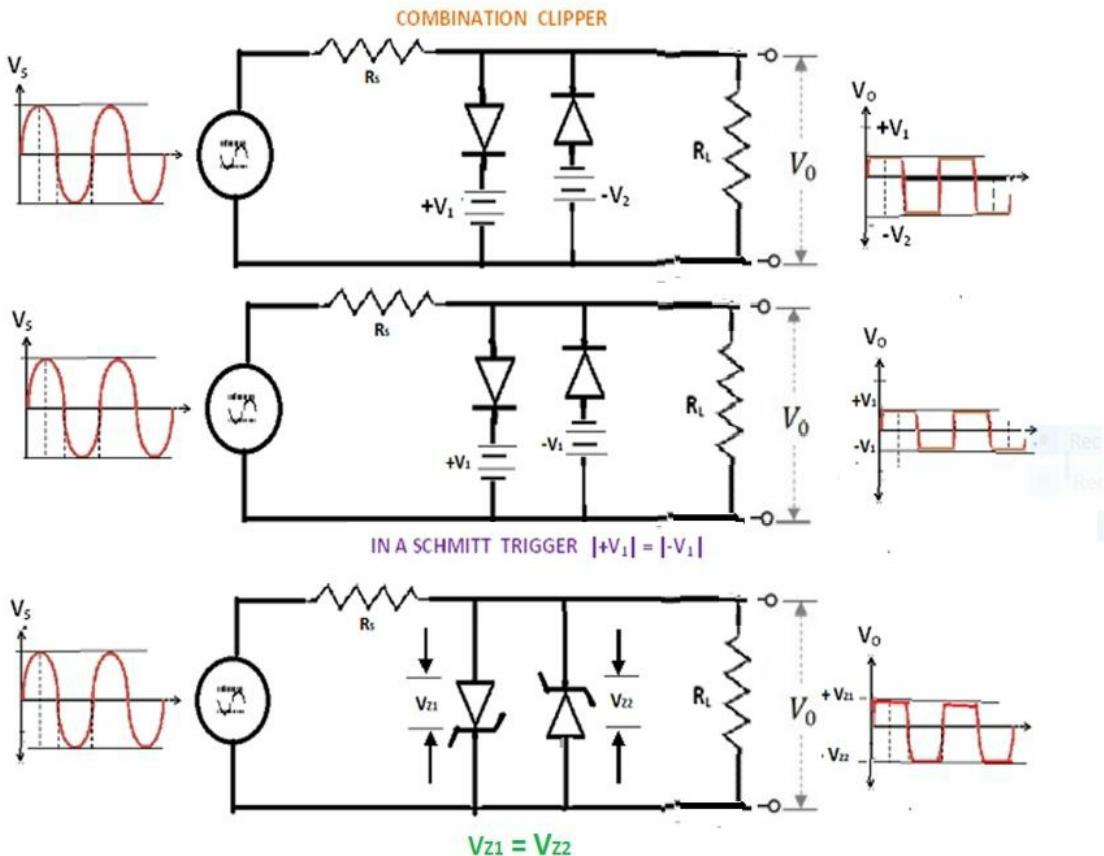
- Again, later in the positive half cycle itself, as soon as the input voltage becomes less than  $+V$  the diode goes into reverse bias and the voltage developed across the load again becomes of the same shape as that of the input waveform. This continues into the negative half cycle also. Hence the shape of the output waveform is as shown in the figure. In other words, the output waveform is clipped at the voltage level of  $+V$ .
- In the case of the Negative Biased Clipper, the opposite occurs and the output waveform is clipped at the voltage level of  $-V$ .

**Combination Clipper:** - When we combine the Positive Biased Clipper and the Negative Biased Clipper, we have a Combination Clipper. This clips off the input AC signal at two different voltage

levels, which are  $+V_1$  and  $-V_2$ . this shown in the Fig-4.

**Schmitt Trigger:** - A Schmitt Trigger is a circuit that converts an AC signal into a square wave signal of the same frequency. This has wide ranging applications in the electronics industry. A Schmitt Trigger can be configured in various forms. The configuration shown in Fig- 4 is one that is implemented using diodes. If the two bias voltages  $+V_1$  and  $-V_1$  are of the same magnitude then the output voltage will be clipped at these two voltage levels, so that the magnitude of the positive peak and that of the negative peak would be of the same magnitude, thus resulting in a square wave output.

**Combination Clipper Using Zener Diode:** - A Combination Clipper can be configured using Zener Diodes which will have clipping levels at  $+ V_{Z1}$  and  $- V_{Z2}$ . This does not require the DC batteries for providing the bias as in the Combination Clipper of the figure above. Zener Diodes can be manufactured which have different values of the Break-down voltage  $V_Z$ . This is achieved by using different concentrations of doping at the time of manufacture. If the doping concentration is high the Break-Down voltage is low and vice-versa. Thus, Zener Diodes with different specifications are available in the market. Therefore, any specific set of clipping levels  $+ V_{Z1}$  and  $- V_{Z2}$  is possible

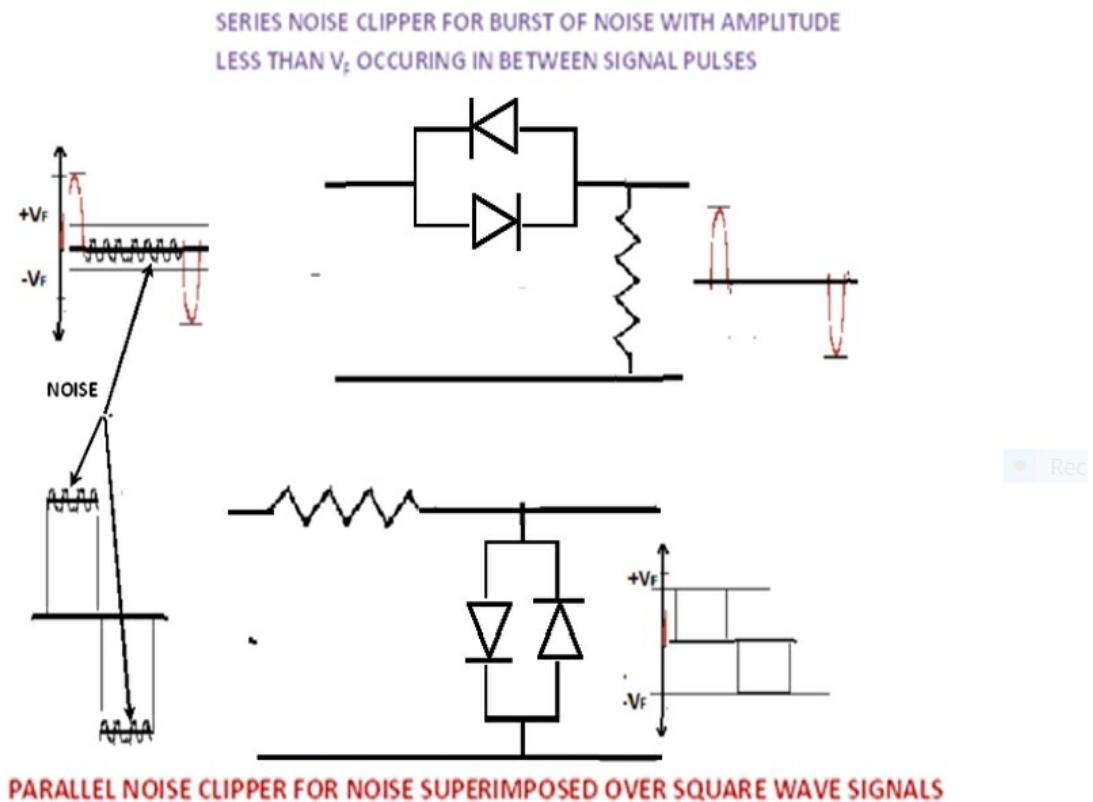


**Fig –4:** - Combination Clipper and Schmitt Trigger

**Noise Clipper:** - In electronic systems, signals are often corrupted by noise. Noise is defined as unwanted electromagnetic interference that causes a superimposed disturbance on a signal. Usually, noises are of unpredictable amplitude and frequency (Random Quantities). Two types of clippers can be configured to eliminate two common types of disturbances as explained below.

- **Series Noise Clipper** is used for clipping Noise Bursts occurring in between signal pulses. If the noise amplitude is less than or equal to the “Forward voltage Drop  $V_F$ ” of the diode, then the noise burst will be unable to forward bias the diode. Hence, they will not appear at the output.
- **Parallel Noise Clipper** can be used for clipping noise that gets

superimposed over square wave signals only. Assume the noise amplitude to be less than the signal amplitude. The circuit acts as a Schmitt Trigger, where the battery for the DC Bias is not connected. The required DC Bias to take the diodes into conduction is provided by the signal itself. At Forward Conducting Region of the diode the voltage drop across the diode is  $V_F$ . Thus, the clipping level is  $V_F$  in each cycle.

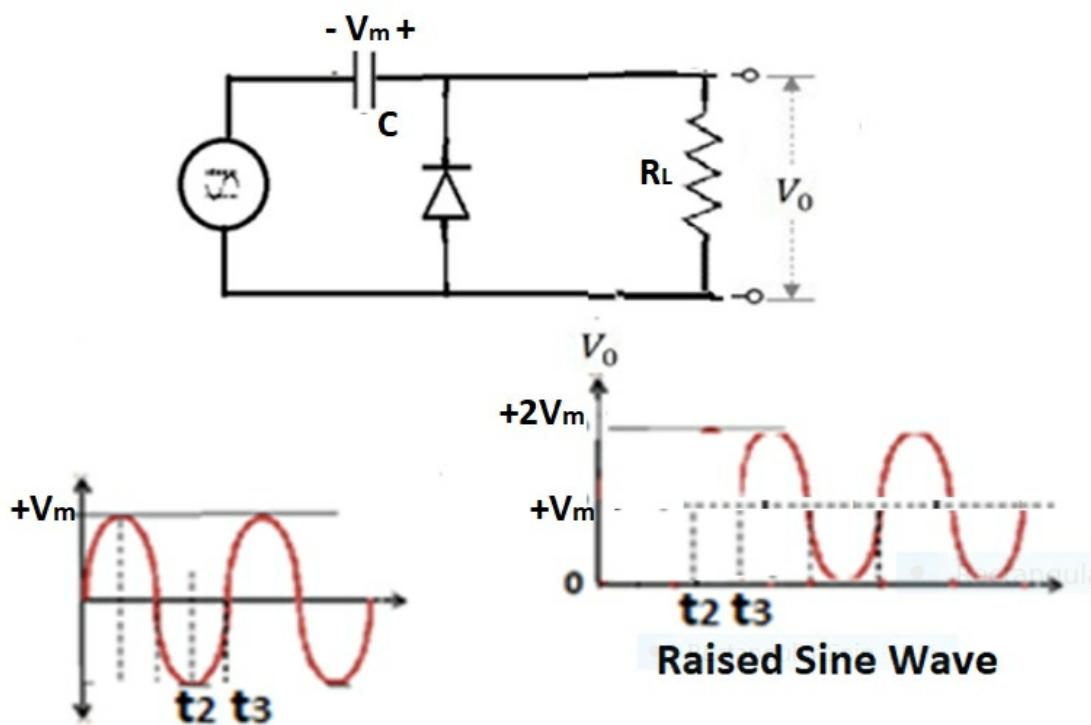


**Fig- 5:** - Series Noise Clipper and Parallel Noise Clipper.

**(2) VOLTAGE CLAMPER:** - The function of a Clamper is to add a DC Bias to an AC signal. In other words, the input AC signal is “Clamped” or “Raised” on to a fixed voltage level. The circuit diagram for a Clamper is shown in Fig- 6. and it's working principle is as described below.

PRINCIPLE: -

- During the first positive half cycle the diode is reverse biased. The capacitor just begins to store charge. Therefore, there is no current flow in the circuit. Assume that the load resistance is very high. Therefore, the charging current will be negligible and so the stored charge also will be negligible.



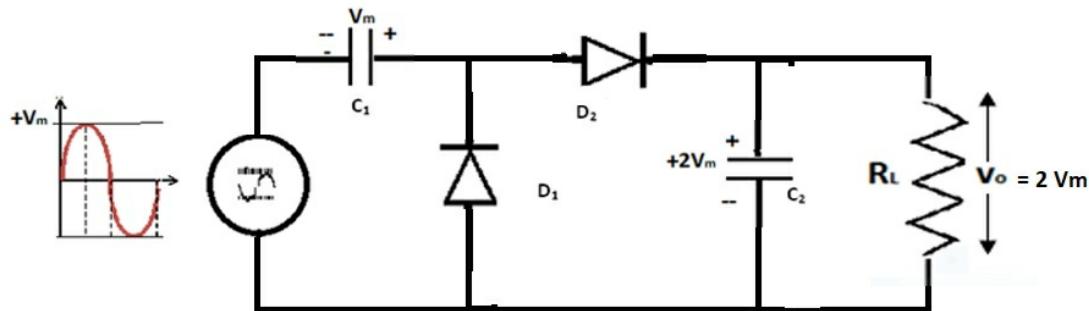
**Fig –6: - Voltage Clamper**

- At the first negative half cycle the diode gets forward biased. Therefore, it conducts. But since the load resistance is very high, the current flows into the capacitor instead of R<sub>L</sub>, and charges it up to the peak value V<sub>m</sub> of the input AC signal. This is at  $t = t_2$ . The polarity of the potential is as shown in the figure.
- After the negative peak value is reached, the input AC voltage is less than +V<sub>m</sub>. On the other hand, the potential to which the capacitor had been charged up to, is +V<sub>m</sub>. This will now apply a reverse bias on the diode. Since the load resistance is assumed to be high, the time constant  $C R_L \gg T$  (where T is the time period of

the input AC), then charge stored in the capacitor will be retained up to the next cycle.

- At the next cycle, at  $t = t_3$ , the capacitor will charge up again up to  $+V_m$ . The AC input is in series with the stored DC potential  $+V_m$ . Thus, they get added, so that the output voltage appearing across the load  $R_L$  is the sum of the input AC and the stored DC. This is shown in the output waveform in the figure. **In other words, the AC signal gets “Clamped” or “Raised” up to the DC level  $+V_m$ .**
- This repeats in every subsequent cycle.
- A **Biased Clammer** can be configured by connecting a DC bias along with the diode. In this case the clamping will occur at a level with the DC bias added to  $V_m$ .

**(3) VOLTAGE MULTIPLIERS:** - A Voltage Multiplier is a circuit that “Steps-Up” the DC voltage. (*AC voltage is stepped up or down using transformer. But a transformer cannot work with DC*). However, in the Voltage Multipliers, the stepping up can be only in multiples of the peak value  $V_m$ . Accordingly, we have Voltage Doubler, Voltage Tripler, Voltage Quadrapler etc. These are explained with the help of the circuit diagrams shown in Fig-7 below.



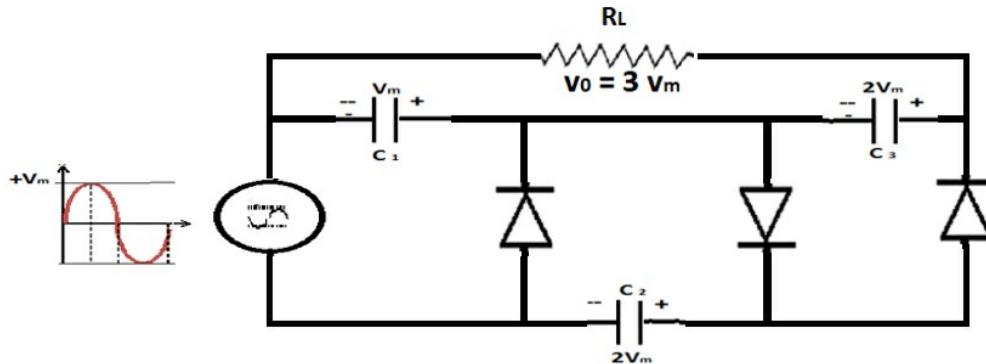
**Fig – 7:** - Voltage Doubler. Output is a constant DC of  $2 V_m$

#### PRINCIPLE: -

- ✓ In the circuit above, the  $D_1 - C_1$  combination works as a Voltage Clammer so that the anode of the diode  $D_2$  gets a clamped AC with the peak value  $2 V_m$ . (Refer to Fig-6 & Fig -7). During the second positive half cycle, the diode  $D_2$  gets forward biased.
- ✓ If we assume that the load resistance is very high, the current flows

only into the capacitor  $C_2$  and charges it up to the voltage level of  $2V_m$ , with a polarity as shown in the figure.

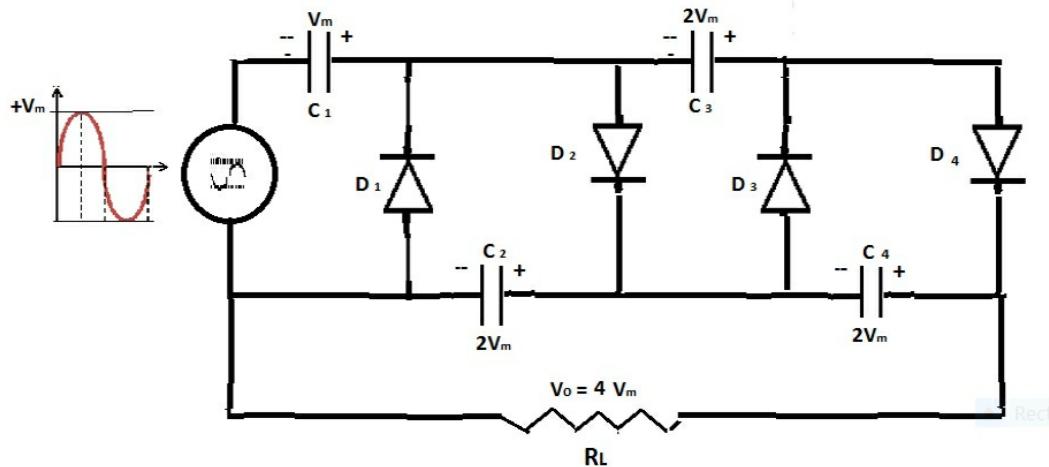
- ✓ During the negative half cycle, the diode gets reverse biased and hence it does not conduct. Since the load resistance is very high, the capacitor retains its charge and the potential across its plates remain at the  $2V_m$  level.
- ✓ In the subsequent positive half cycle, the diode  $D_2$  gets forward biased again and charge up the capacitor  $C_2$  up to  $2V_m$  again. Thus, we can assume that the voltage across  $C_2$  remains constant at  $2V_m$ . Since the load resistance is connected in parallel to  $C_2$ , the output voltage also remains constant at this voltage  $2V_m$ , which is “Double” of the peak of the input voltage.



**Fig –8:** - Voltage Tripler. Output is a constant DC of  $3 V_m$

- ✓ **Voltage Tripler**, The Clamped AC of peak value  $2V_m$  is applied to  $D_2$ . During the positive half cycle, the conducting  $D_2$  charges up  $C_2$  up to  $2V_m$  in the polarity as shown in the figure.
- ✓ During the negative half cycle,  $D_2$  is reverse biased.  $D_1$  is also reverse biased by the constant potential of  $V_m$  stored in  $C_1$ . But  $D_3$  is forward biased by the charged capacitor  $C_2$ . This charge is now stored in  $C_3$ . Thus, at the end of the negative half cycle,  $C_3$  gets charged up to a potential of  $2V_m$  in the polarity as shown in the figure.
- ✓ Since the potential of  $C_1$  and  $C_3$  are in series, the voltage across the load is  $3V_m$ . Hence, we have a Voltage Tripler.
- ✓ By adding another Diode-Capacitor combination of  $D_4 - C_4$  we

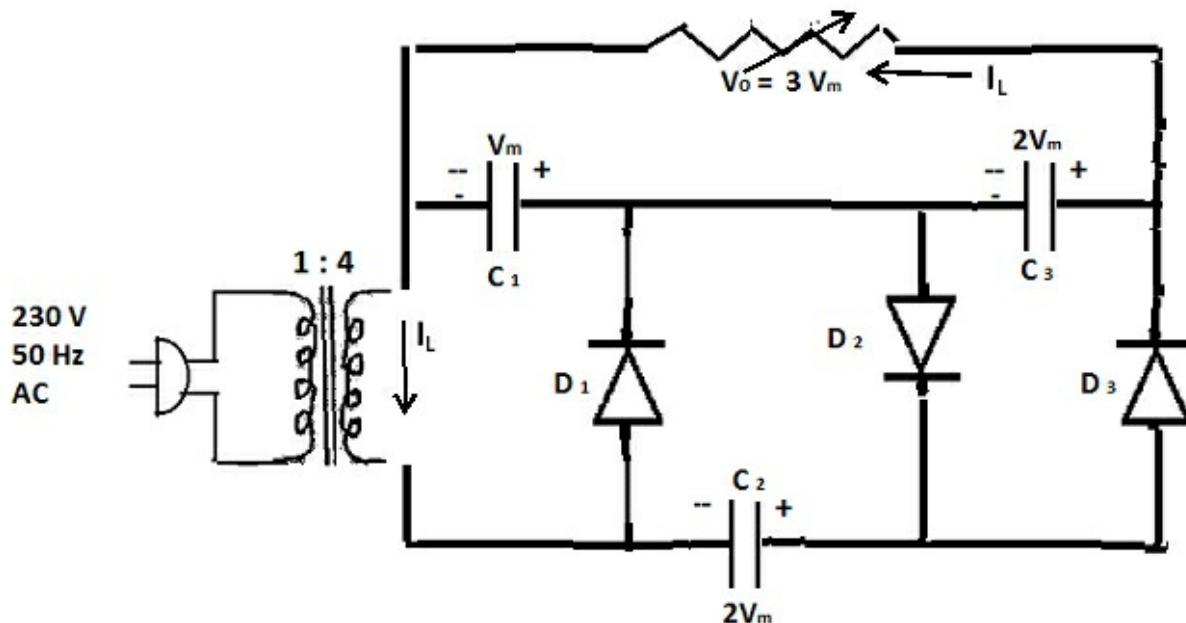
have a **Voltage Quadrupler** and so on.



**Fig -9:** - Voltage Quadrupler. Output is a constant DC of  $4 V_m$

#### TUTORIAL-4

**EXAMPLE- 1** Calculate output voltage at the load of a voltage tripler when the load resistance varies from  $500 \text{ k}\Omega$  to infinity (open circuit) and calculate V.R. assuming that secondary coil of transformer has an internal resistance of  $725\Omega$ .



**SOLUTION:** - Load current flows from the load to the secondary of the transformer. Since the current is DC the capacitors act as open circuit for this current. Thus the current cannot flow through  $D_1$ . Since the direction of this current is opposite in case of  $D_2$ , it does not flow through  $D_2$  either. The circuit is completed through  $D_3$  by the

discharging of  $C_2$ .

Primary AC RMS voltage is 230 V. The transformer is a Step-Up transformer of turns ratio 1 : 4. Therefore peak of the secondary voltage is

$$\begin{aligned}V_m &= 4 \times \sqrt{2} \times 230 = 1301 \text{ V} \\V_O &= 3 V_m \\&= 3 \times 1301 = 3903 \text{ V}\end{aligned}$$

At maximum load resistance  $R_L = \infty$ , load current is 0 and voltage across load is maximum

$$\therefore V_{O\max} = 3903 \text{ V}$$

At minimum load resistance  $R_{L\min} = 500 \text{ K}\Omega$  load current is maximum

$$I_{L\max} = V_O / R_{tot}$$

Where,

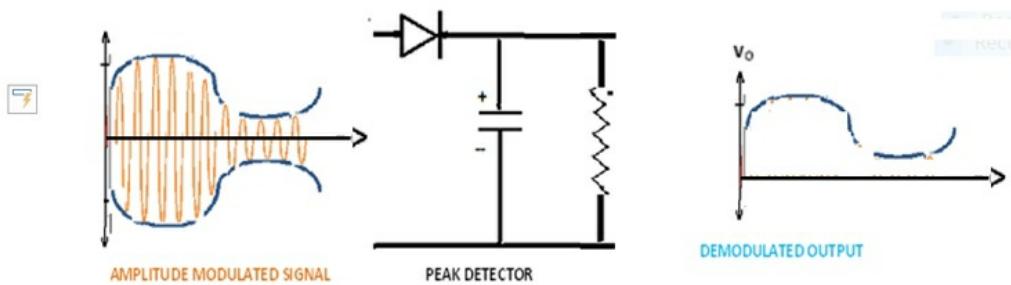
$$\begin{aligned}R_{tot} &= R_{L\min} + R_{secondary} \\&= 500 \times 10^3 + 725 = 500725 \Omega\end{aligned}$$

$$\begin{aligned}\therefore I_{L\max} &= 3903 / 500725 \\&= 0.0078 \text{ A} = 7.8 \text{ mA}\end{aligned}$$

$$\begin{aligned}\therefore V_{O\min} &= \underline{R_{L\min} \cdot I_{L\max}} \\&= 500000 \times 0.0078 = 3900 \text{ V} \\ \therefore \text{V. R.} &= (3903 - 3900) / 3903 \times 100 = 0.077 \%\end{aligned}$$

#### (4) AM Detector (Peak Detector) :-

Amplitude Modulation (AM) is a technique used for communicating electrical signals by modulating the message signal over a very high frequency carrier signal. When the message signal is superimposed over the carrier amplitude, we call it Amplitude Modulation. At the receiving end, the message signal is to be “Detected” by separating it from the carrier signal. This function is carried out by a circuit known as “Peak Detector”.



**Fig-10: - Peak Detector for Demodulation of AM**

- The AM signal is a high frequency signal (**ORANGE**) whose instantaneous amplitude equals the amplitude of the message signal (**BLUE**).
- At the positive half cycle the diode is forward biased and it charges up the capacitor up to the peak value of the half cycle. We assume again that the load resistance is very high. As a result, the capacitor is able to discharge very little during the rest of the cycle.
- At the next positive half cycle, it will get charged up again to the peak value of this half cycle. This will repeat in each positive half cycle so that the peak value of each positive half cycle will appear at the output.
- Thus, the voltage across the capacitor is nothing but the instantaneous peak value of each positive half cycle. Since this instantaneous amplitude represents the message signal, we have the message signal detected at the output.

## SECTION- 2

### 4.2 SPECIAL PURPOSE DIODES

In the previous sections the circuits that were discussed used normal PN Junction diodes made of silicon. In all these applications the unidirectional conducting property (Rectifying property) of the P-N Junction was used. In the following sections the other properties of the P-N Junction diodes and their applications will be discussed. While, some of these diodes are not even made of Si, some are not even P-N junctions. While some of them have very wide depletion regions, in some the depletion region is only a few Angstrom-Units

wide. All of these are used for certain specific applications.

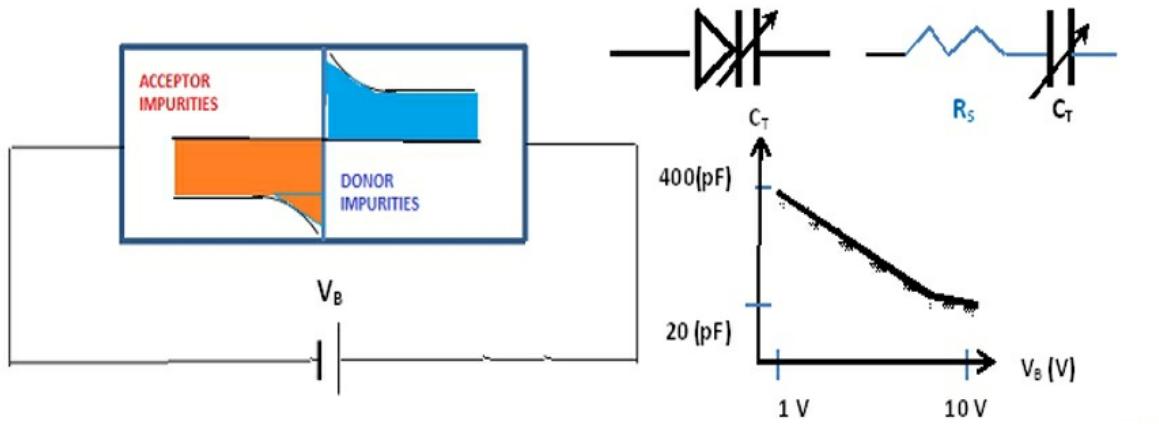
### (1) VARACTOR DIODE (VARICAP)

#### CONSTRUCTION AND PRINCIPLE OF OPERATION

- A Varactor Diode or Varicap is a PN Junction designed as to act as a “Voltage Variable Capacitance”.

In the Chapter-II we studied about the various electrical properties of the P-N Junction. One such property was “Transition Capacitance” denoted by  $C_T$ . the expression for  $C_T$  is given by,

$$C_T = \frac{\epsilon A}{W} \quad \dots(2)$$



**Fig – 11:** - A Varactor Diode is constructed as a P-N Junction with a “Hyper Abrupt Concentration Gradient” of Acceptor and Donor impurities. When a reverse bias is applied this diode behaves as a “Voltage Variable Capacitance” having a high sensitivity. **Varactor Diode is also called Varicap.**

- The width of the junction ‘W’ is proportional to the square root of the net Reverse Bias  $V_B$ . Thus, a reverse biased P-N junction behaves as a Capacitance  $C_T$  and this capacitance is inversely proportional w.r.t. the applied reverse bias.
- In order to make the device more sensitive, the doping density of Acceptor and Donor Impurities across the junction is made to vary exponentially as shown in the Fig-11. A P-N Junction with

such a variation of impurities is called a “**Hyper Abrupt**” junction.

- The inversely proportional relationship between  $C_T$  and  $V_B$  is given by the following –

$$C_T = V_B^{-1/2} \quad \underline{\dots}(3)$$

- The graph of variation of  $C_T$  vs  $V_B$ , the circuit symbol and the equivalent circuit of Varactor Diode is also shown in the figure above.
- Varactor Diodes are primarily used in Communication Engineering applications that require tuning by remote control. A parallel circuit of L and C, called an L-C Tank circuit, has a resonant frequency given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

- If either the Inductance L or Capacitance C is varied the resonant frequency becomes variable. By varying the resonant frequency, the circuit can be tuned to that frequency at which it is resonating.
- It is convenient to use a Varicap in a tuning circuit since the capacitance can be set at the desired value by applying an appropriate amount of a reverse bias across it.

## TUTORIAL-5

**EXAMPLE- 2:** - The reverse bias of a Varactor Diode is varied from 6 V to 3 V. If the capacitance of the device is 250 pF at 3 V then calculate its capacitance at 6 V.

**SOLUTION:** - From Eq. 3 we have

$$C_T \propto V_B^{-\frac{1}{2}}$$

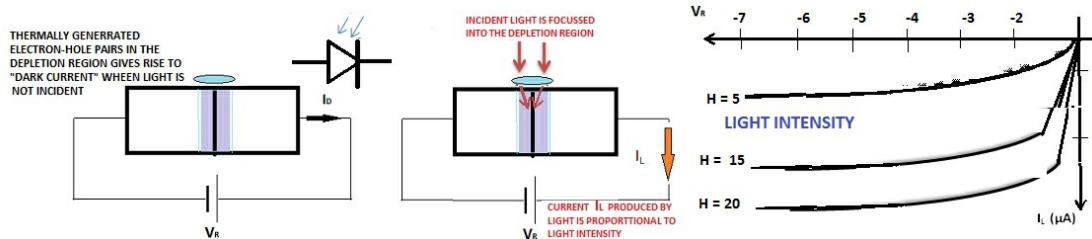
By proportionality, when the reverse bias is varied from  $V_1 = 3$  V to  $V_2 = 6$  V we have,

$$\begin{aligned}\frac{C_2}{C_1} &= \left(\frac{V_1}{V_2}\right)^2 \\ \therefore C_2 &= C_1 \times (3/6)^2 \\ &= 250 \times .5^2 = 62.5 \text{ pF}\end{aligned}$$

**ANSWER:** -  $C_2 = 62.5 \text{ pF}$

## (2) PHOTO DIODE AND PHOTO DETECTOR CONSTRUCTION AND PRINCIPLE OF OPERATION

- A Photo Diode is a Si diode that is operated at reverse bias. It is constructed by incorporating a Micro-Lens over the junction region, as shown in the Fig-12.
- When no light is incident on the device only a very negligible reverse current flows, which is due to the electron-hole pairs generated in the Depletion Region by the surrounding thermal energy only. This is in the range of a few nA. Hence it is called the **“Dark Current”** and denoted by  $I_D$ .
- The properties of the Depletion Region are similar to Intrinsic Semiconductor. When light is focused on the Depletion Region by the micro-lens, the energy of the light beam energizes some valence electrons of silicon to jump up to the conduction band, thereby creating additional electron-hole pairs. This results in an increase in the reverse current. The current is proportional to the intensity of light
- Thus, this device can act as a detector of light, or PHOTO DETECTOR. The circuit symbol of the device is also shown in the figure below.



**Fig- 12: -**

**APPLICATIONS:** - Photo -Detector has various applications as enumerated below

1. As a Reverse Biased Diode, it can function as a Photo Detector that produces a Reverse Current which is proportional to the Light Intensity.
2. Photo detectors are used as receivers in Fiber Optic Cable Systems. In this digital signal in the form of bits is transmitted as light pulses which are converted into current pulses at the receiving end by Photo Detectors.
3. An array of Unbiased Diodes functions as a Solar Cell that generates a DC current when sunlight is incident on it.

### (3) LIGHT EMITTING DIODE – LED

#### CONSTRUCTION AND PRINCIPLE OF OPERATION

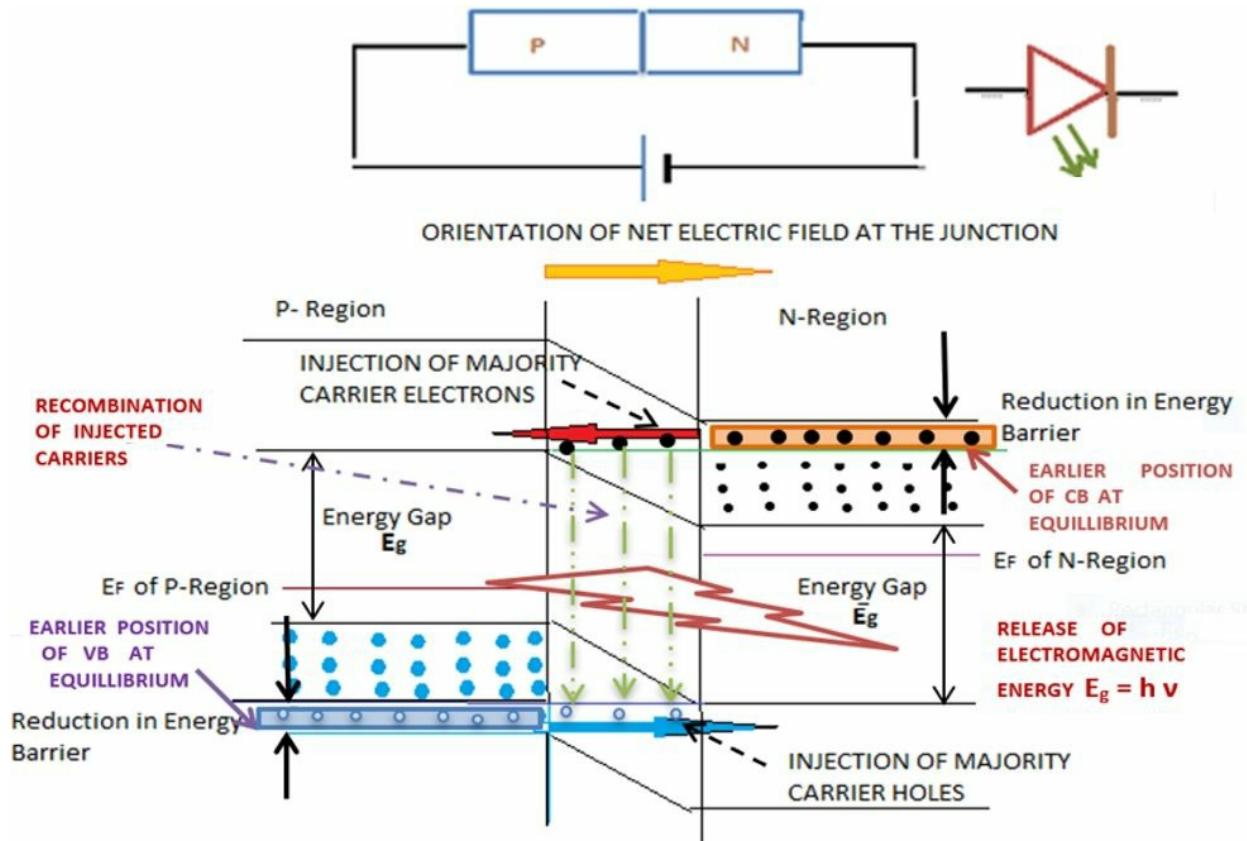
A Light Emitting Diode (LED) is a PN Junction made from alloy semiconductors such as Ga-As, Ga-In-As, Ga-In-As-P (pronounced as “gallium-arsenide”, “gallium-indium-arsenide”, “gallium-indium- arsenide-phosphide” respectively). Such alloys are almost transparent to light unlike Si or Ge and compared to Si and Ge, they have a larger Energy Gap ( $E_g$ ) between the valence band and the conduction band

Such a diode will emit visible or Infra-Red radiation, when it is forward biased.

- The action of a forward biased P-N Junction was explained in terms of the Energy-Band Theory in the Chapter-II. This is shown

again in Fig-13.

- Recall that, when a P-N junction is forward biased, majority carrier electrons of the conduction band of the N-side are injected into corresponding band on the P-side and majority carrier holes of the valence band of the P-side are injected into corresponding band on the N-side. The principle of the LED is summarized in the table below and explained as follows.



**Fig -13:** - Action of Emission of EM radiation from a forward biased P-N Junction. For a PN Junction made of Ga-As alloy, the radiation is of the wavelength of Visible Light or IR. Circuit Symbol is also shown. Arrows of light point OUTWARDS.

- These injected majority carriers from either side recombine with the respective majority carriers of the opposite side. In this process an electron has to come down from the conduction band to the valence band.
- These two energy bands are separated by the Energy Gap  $E_g$ . This difference of energy between the conduction band and the valence band has to be **released by the electron in the form of Electro-Magnetic radiation**.
- By Bohr's Postulate, any two energy levels of an atom are separated by an amount of energy equal to the product of Planck's Constant ' $h$ ' and frequency of radiation ' $v$ '. Thus, the released Electro-Magnetic radiation is at a frequency  $v$ .

$$E_g = h \cdot v$$

- The quantity Energy Gap  $E_g$  between VB and CB is a characteristic of the semiconductor material. In case of silicon Energy Gap  $E_g$  equals 1.1 eV. While in case of the InGaAsP (Indium-Gallium-Arsenide-Phosphide) group of alloys the quantity  $E_g$  ranges from 1.5 eV to 2 eV.
- If we make a comparing calculation for the frequency of the radiated electro-magnetic energy in forward bias condition for Si and the Ga-As group of alloys, we have a table the result as shown below—

**Table: - 1** Table of comparison Si Diode and LED

### CALCULATION FOR SILICON

We had Energy Gap between CB & VB is

$$E_g = h \nu$$

Numerical Value of Planck's Constant

$$h = 6.626 \times 10^{-34} \text{ J-sec}$$

Converting the energy unit from J to eV

$$h = 4.2 \times 10^{-15} \text{ eV-sec}$$

For Si

$$E_g = 1.1 \text{ eV}$$

Therefore amount of radiated energy

$$E_g = h \nu = 1.1 \text{ eV}$$

Therefore frequency of radiated energy

$$\nu = 1.1/h = 1.1/4.2 \times 10^{-15} = 2.6 \times 10^{14} \text{ Hz}$$

Relationship between frequency and wavelength of radiation is

$$\lambda = c/\nu$$

where  $c$  is the speed of E-M radiation

$$c = 3 \times 10^8 \text{ m/sec}$$

Therefore

$$\lambda = 3 \times 10^8 / 2.6 \times 10^{14} = 1.154 \times 10^{-6} \text{ m}$$

or

$$\lambda = 11540 \text{ } \overset{\circ}{\text{A}} \text{ [Angstrom]} = 1154 \text{ nm}$$

Radiations of such wavelengths

correspond to that of Heat Energy.

Therefore silicon diode releases heat, when it is operating in forward bias.

### CALCULATION FOR Ga-As

For Ga-As Energy Gap between CB & VB is

$$E_g = 1.8 \text{ eV}$$

Therefore amount of radiated energy

$$E_g = h \nu = 1.8 \text{ eV}$$

Therefore frequency of radiated energy

$$\nu = 1.8/h = 1.8/4.2 \times 10^{-15} = 4.2 \times 10^{14} \text{ Hz}$$

Relationship between frequency and wavelength of radiation is

$$\lambda = c/\nu$$

where  $c$  is the speed of E-M radiation

$$c = 3 \times 10^8 \text{ m/sec}$$

Therefore

$$\lambda = 3 \times 10^8 / 4.2 \times 10^{14} = 0.714 \times 10^{-6} \text{ m}$$

or

$$\lambda = 7140 \text{ } \overset{\circ}{\text{A}} \text{ (Angstrom)} = 714 \text{ nm}$$

Radiations of such wavelengths correspond to that of visible light.

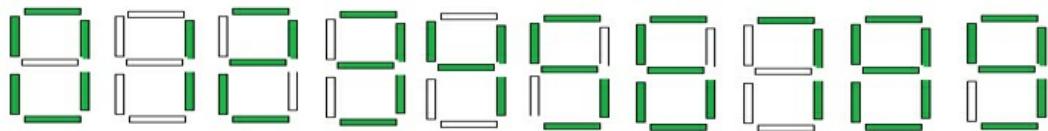
Therefore diodes made of Ga-As group of alloys releases light when it is operating in forward bias.

Hence the name LED. The colour of the light radiation depends upon the element alloyed with Ga-As such as In or In+P. In general RED, GREEN and YELLOW colours are common.

**APPLICATIONS OF LED:** - The common applications of LED are as enumerated below—

1. As a source of light in Optical Fiber Cable systems. The bit '1' is introduced into the fiber as a switching ON of the LED and the bit '0' is introduced when the LED is switched OFF. In Optical Fiber systems however, Infra-Red LED is used rather than LED emitting visible light.
2. As individual segments in Seven-Segment-Displays. Various information such as display of time in digital clocks, display of a

reading in various measuring and scientific devices etc. are in the form of Seven-Segment-Displays. In these seven individual segments are arranged as shown in the figure below. In many cases, each of these segments is an LED. By lighting up some or all of these LED segments, any of the Alpha-Numeric characters may be displayed.



3. As source of Infra-Red Pulse in a Remote-Control unit of gadgets such as TV or Air Conditioner etc.
4. As indicators to indicate presence of an event in various electronic gadgets, such as indication of switching on of electrical power in a TV or a Fridge etc.

#### (4) LASER DIODE – LD

- The term LASER is the acronym for “*Light Amplification by Stimulated Emission of Radiation*”. The characteristics of such emission are (a) Emitted Electro-Magnetic radiation is highly concentrated in a narrow beam. (b) The radiation is of very high intensity. (c) The radiation is strictly monochromatic, i.e., at a single wavelength.
- For ‘Lasing’ to occur a condition known as “**Population Inversion**” is to be created.
- Population Inversion is defined as the condition in which there occur a significantly more population of electrons at a certain higher energy level compared to a certain lower energy level.
- This is achieved by stimulating a large number of valence band electrons of the ‘Lasing Medium’ to jump up to an energy level far higher than the conventional conduction band and make them occupy this energy level for a certain specified long enough duration of time. While eventually, these stimulated electrons drop down to the lower energy states, there have to be an intermediate energy level which will hold a fewer number of these electrons for

an equal duration of time as the upper energy level did. Thus, there will occur a situation when the higher energy level has more electrons than the lower one. **This situation will create Population Inversion.**

- The phenomenon of electron transition take place, as usual, from the population inverted higher level to the lower level. The EM energy released in this process is a beam of LASER.
- In case of a LD made of Ga-As as the Lasing Medium, stimulation is provided by applying a very high value of forward bias. The LASER rays emitted due to this process are made to undergo multiple internal reflections with an arrangement where the Ga-As crystal is placed between two parallel mirrors. The multiple crisscrossing of light through the “Lasing Medium” leads to sustained stimulation of the material to sustain a LASER beam as long as the external bias source is kept switched on.
- This process is supported by a few substances, other than the alloys of the Ga-As family.

**APPLICATIONS OF LD:-** The common applications of LD are as enumerated below—

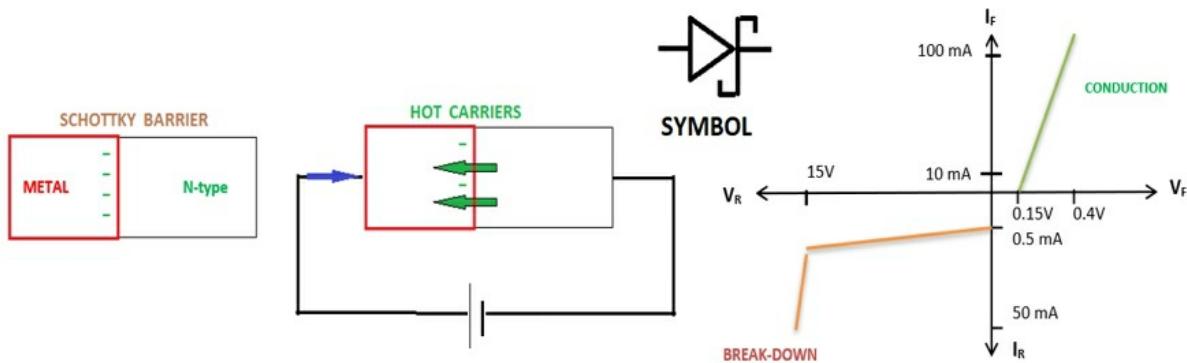
1. As a source of light in high efficiency fiber optic cable systems.
2. As a READ/WRITE transducer for CD and DVD ROMs used in computers and CD/DVD players.

## (5) SCHOTTKY DIODE OR HOT-CARRIER DIODE

### CONSTRUCTION AND PRINCIPLE OF OPERATION

A Schottky Diode is not a P-N Junction. **Rather, it is a junction between A Highly Doped N-type Crystal with A “Low Electron Pressure” Metal.** Generally, two metals are used, namely (a) Molybdenum (Mo) and (b) Tungsten (W). These metals have a lower concentration of free electrons compared to a highly conductive metal (such as Al, Cu or Ag). Consequently, such a metal has a very low conductivity. On the other hand, the N-type crystal is doped very heavily with donor impurities so that it has an abundance of free electrons and consequently, a very high conductivity. In fact, the N-Type crystal is so heavily doped, that it

behaves almost like a good conductor. A substance with a high conductivity is a substance with a “High Electron Pressure”. A junction between a Highly Doped N-type silicon crystal and A Low Electron Pressure metal is shown in the Fig-14 below.



**Fig- 14:** - Construction, Working Principle, Circuit Symbol and V-I Characteristic of Schottky Diode.

- ❖ Since the N-Type semiconductor crystal has a High Electron Pressure compared to the Metal part, some of the free electrons from the semiconductor part will cross over to the metal part. Thus, a layer of elections will be formed at the junction. This layer will repel the other electrons trying to cross the junction. This is called a Schottky Barrier.
- ❖ When a bias is applied such that N-Type part is connected to the negative terminal and the metal part to the positive terminal, some of the electrons from the Schottky Barrier will get attracted by the positive terminal and the barrier potential will be reduced.
- ❖ Now some free electrons of the N-type semiconductor will rush into the metal part thereby resulting in a Forward Current. These free electrons are called the “Hot Carriers”.
- ❖ As the forward bias is increased, more hot carriers will cross and increase the current.
- ❖ At reverse bias the Schottky Barrier will become wider, hence it will resist flow of reverse current.
- ❖ At a high enough value of reverse bias Avalanche Break-down process will occur and the diode will go into Break-Down condition

### DIFFERENCE BETWEEN P-N JUNCTION DIODE AND SCHOTTKY DIODE

<u>P-N JUNCTION DIODE</u>	<u>SCHOTTKY DIODE</u>
<ol style="list-style-type: none"> <li>1. In P-N Junction diode current flow is due to both Holes and Electrons.</li> <li>2. The minimum forward voltage <math>V_F</math>, at which conduction begins, i.e. 'Cut-In Voltage' for Si is 0.7 V and for Ge it is 0.3V.</li> <li>3. There occur two types of capacitances in a P-N Junction diode due to the existence of the 'Depletion Region'. A quantity called 'Diffusion Capacitance' during forward bias and 'Transition Capacitance' during reverse bias. Due to these the device cannot immediately switch from On State to Off State or vice versa since a capacitance cannot charge up or discharge instantaneously. The time delay involved in this process is called 'Reverse Recovery Time'.</li> <li>4. Reverse saturation Current in P-N Junction diode is negligible, being in the range of nA for Si and <math>\mu</math>A for Ge.</li> <li>5. Break-Down Voltage for P-N Junction diode is adjustable w.r.t. the concentration of doping. It can be made very high or very low by manufacturing the device with a predetermined level of doping.</li> </ol>	<ol style="list-style-type: none"> <li>1. In Schottky Diode current flow is due to electrons only.</li> <li>2. Value of Cut-In-Voltage <math>V_F</math> for Schottky Diode is only 0.15 V.</li> <li>3. Since there is no Depletion Region the Schottky Diode does not have either 'Diffusion Capacitance' or 'Transition Capacitance'. Therefore the quantity 'Reverse Recovery Time' does not exist and the Schottky Diode can immediately change state from On State to Off State and vice-versa.</li> <li>4. Current during reverse bias is not strictly constant. It increases slightly w.r.t. reverse bias. Also the reverse current is much larger, being in the range of mA.</li> <li>5. Break-Down Voltage of Schottky Diode is fixed at 15 V and it is not adjustable unlike P-N junction diode.</li> </ol>

**APPLICATIONS OF SCHOTTKY DIODE:** - The common applications of Schottky Diode are as enumerated below—

1. As a Rectifier for very high frequency signals.
2. As a Peak Detector for Microwave Receives.
3. As a low voltage clamping diode.
4. As a low voltage clamp for lowering switching voltage in Schottky Clamped TTL ICs.

### (6) TUNNEL DIODE or ESAKI DIODE

Tunnel Diode is also known as ESAKI DIODE, after the name of its inventor. It is a P-N junction with a VERY HIGH LEVEL OF DOPING. Tunnel Diodes can work at very high frequencies of the GHz band, they

are resistant to High Radiation Environment and they have a very long service life exceeding 50 years. These attributes make them highly suitable for Space Applications.

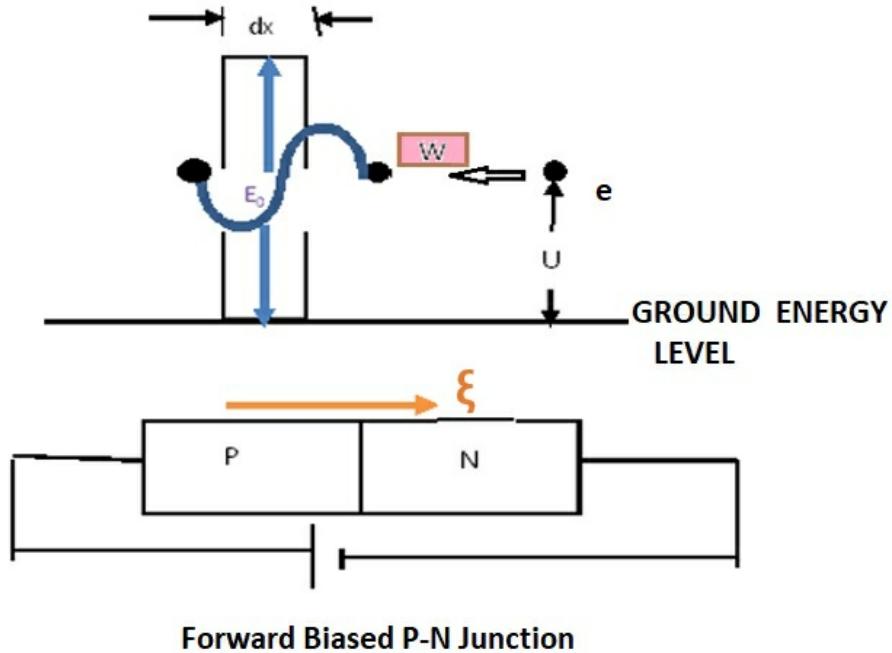
### CONSTRUCTION AND PRINCIPLE OF OPERATION

- In a general-purpose Diode, the concentration of impurities is about  $1:10^6$  to about  $1: 10^8$ . Whereas in the T- Diode it is of the order of  $1:10^3$ .
- This results in a very narrow depletion region in the T-Diode, which is of the order of around  $50 \text{ \AA}$  to  $100 \text{ \AA}$ . This is around 1/50th of the wavelength of light and this even less than the electron wavelength.

### TUNNELING PHENOMENON: -

- In a normal P-N Junction current conduction takes place when majority carriers cross the junction by overcoming the Barrier Energy due to the application of a forward bias.
- Tunnelling phenomenon is shown in Fig.15.
- When a small magnitude of Forward Bias be applied to the P-N junction an electron ‘e’ will travel in the direction shown. The total energy of the electron is  $(U + W)$ , where  $U$  is the potential energy due to its location in a shell in the atom and  $W$  is the kinetic energy of motion due to the external bias. Since the magnitude of the bias has been assumed to be small, the value of  $W$  is also small.
- Very high concentration of doping in Tunnel Diode results in a very narrow depletion region  $dx$ . This in turn results in a very strong Barrier Electric Field  $E_0 = dv / dx$ . Consequently, a high value of Barrier Energy  $E_0$  occurs in the depletion region of the Tunnel Diode. This Energy Barrier is greater than the total energy of the electron.

$$E_0 > (U + W)$$



**Fig.-15:** - An electron shown both as a particle and a wave in a biased Tunnel Diode.

- Due to the heavy doping, the Depletion Region in T-Diode is around  $50 \text{ \AA}$  to  $100 \text{ \AA}$ . This is less than the wavelength of the electron. Thus, there is a high probability that the electron wave may extend across the junction.
- Thus, even a low energy electron will be able to cross the junction **if the following conditions are satisfied.**

### **CONDITIONS FOR TUNNELLING**

1. **The thickness of the depletion layer should be less than or equal to a limiting value  $d_0$ , where  $d_0$  is given by**

$$d_0 = \frac{h}{4\pi} \left[ \frac{1}{2m\{E_0 - (U + W)\}} \right]^{1/2} \quad \dots\dots(4)$$

**Where,**

- a)  **$h$  = Planck's Constant**
- b)  **$m$  = Mass of Electron**

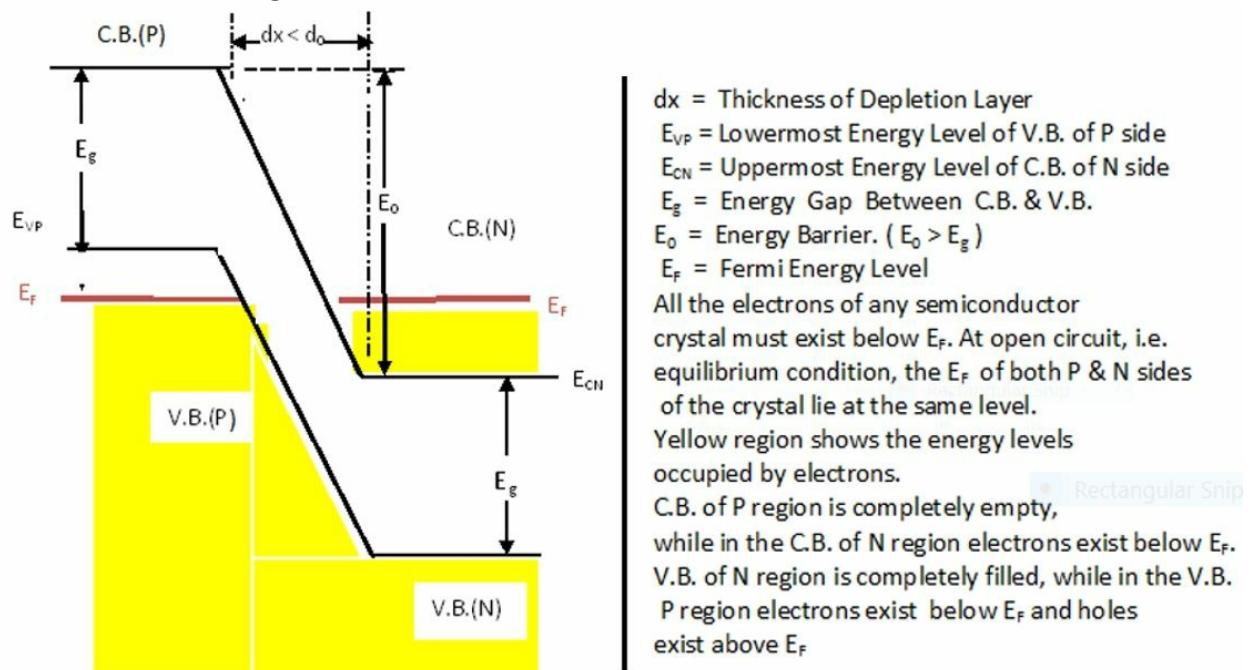
- c)  $E_0$  = Barrier Energy
- d)  $(U+W)$  = Total Energy of the electron (PE+KE).

2. There must exist an ‘Un-occupied’ energy level within either the valence band or the conduction band on that side of the junction into which the electron is expected to tunnel in, and this must be at the same energy level as that at which the electron existed before tunneling.

If these two conditions are known as **Esaki Conditions**. If these conditions are satisfied tunneling can take place in small magnitudes of **both forward bias as well as reverse bias**.

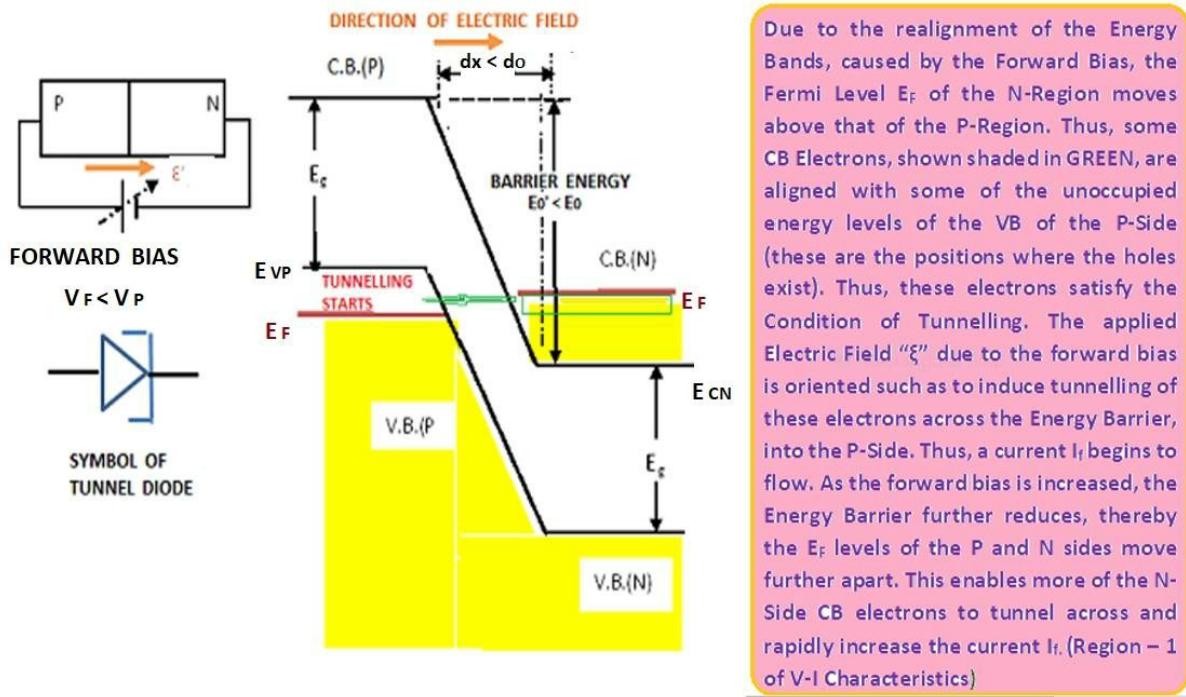
### ENERGY BAND DIARAM OF TUNNEL DIODE AT OPEN CIRCUIT

➤ It was explained that the Tunnel Diode has a very high level of doping resulting in a high value of Barrier Energy  $E_0$ . This Energy Barrier is greater than the Band Gap Energy of the semiconductor.  $E_0 > E_g$ . This is shown in the Fig. 16 below.



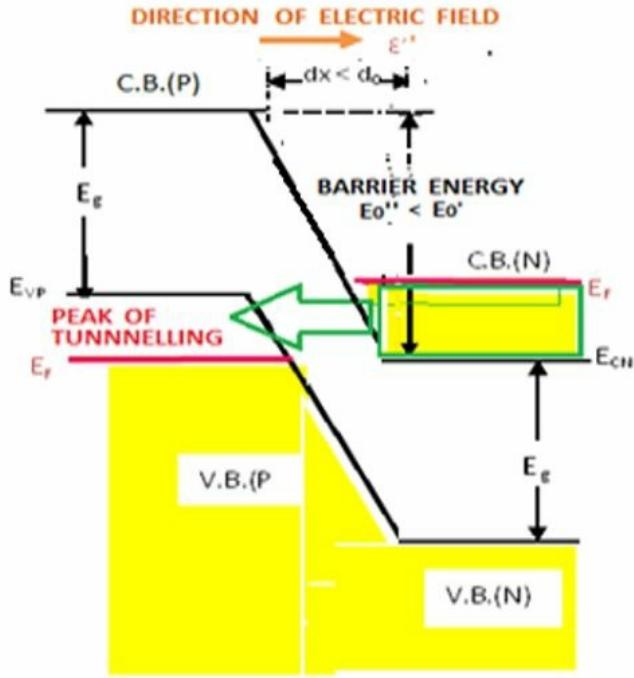
**Fig.- 16:** - Energy Band Diagram of Tunnel Diode at Open Circuit condition or Equilibrium Condition.

1. **Forward bias  $V_f < V_p$**  :- Consider a small amount of forward bias  $V_f < V_p$ . This results in the energy bands of the P region sliding downwards, while those of the N region slide upwards, thereby reducing the energy barrier to  $E_0'$ . The situation with realigned Energy Bands is shown below in Fig-17. **This situation results in Tunneling.** Due to tunnelling a current flow occurs. The rate of increase of the current w.r.t. forward bias is very sharp.



**Fig.-17:** - Tunelling starts as soon as a forward bias is applied. As the forward bias increases, the forward current increases rapidly due to a rapid increase in the number of C.B. electrons available for tunnelling.

ii **Forward bias  $V_f = V_p$**  :- When forward bias increases to  $V_f = V_p$  Energy Barrier further reduces to  $E_0''$  and tunneling current becomes maximum. This situation is known as the “**Peak Tunnelling**”. This is shown in Fig-18.

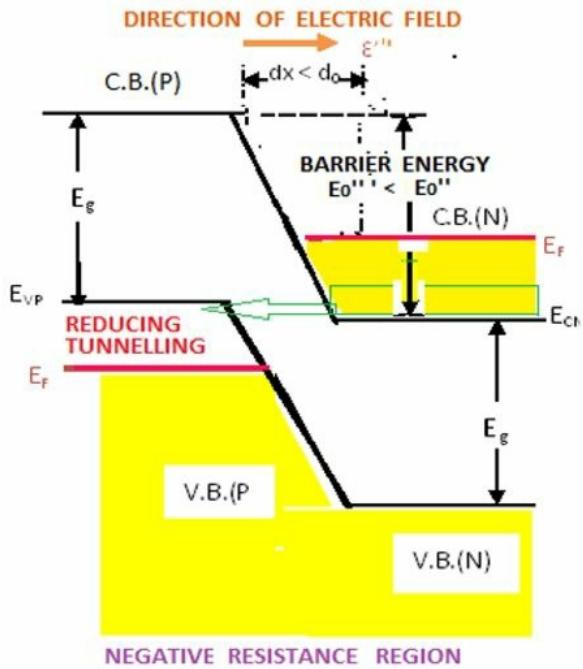


Due to the re-alignment of energy bands caused by increased forward bias, the Fermi Level  $E_F$  of the N-Region shifts further up and that of P-Region shifts further down. At a particular value of forward bias  $V_f = V_p$  the situation is such that EF level of N-Region is aligned with the upper limit of the EVP of the VB of the P-Region and the EF level of P-Region is aligned with the upper limit of the ECN of the CB of the N-Region. In this case all of the CB electrons of the N-Region are aligned with the empty energy levels of the VB of the P-side (those energy levels that correspond to the holes). Thus all these electrons satisfy the Condition-2 of tunnelling. Therefore the current due to tunnelling reaches the Peak Value  $I_P$ .

**Fig.-18:** - Peak of Tunneling occurs when  $V_f = V_p$ . In this situation, all the C.B electrons of the N-Side are available for tunneling, giving rise to the peak value of current.

### iii Forward bias $V_p < V_f < V_V$ (Negative Resistance Region) :-

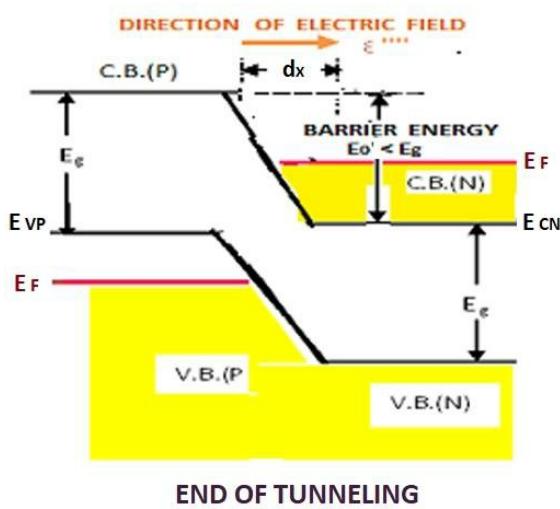
When a forward bias is between  $V_p$  and a higher value  $V_V$  ( $V_p < V_f < V_V$ ), the Energy Barrier further reduces and tunneling current begins to decrease w.r.t. increasing forward bias. Thus, the Tunnel Diode works with a Negative Resistance. This is indicated by the Region-2 of the V-I Characteristics. Fig.-19. explains this situation graphically.



Due to the realignment of energy bands caused by increased forward bias, the energy levels of N region shifts further up and those of the P region shifts further down. At the values of forward bias  $V_p < V_f < V_v$  the situation is such that the  $E_F$  Level of N region is aligned at a level higher than  $E_{VP}$ . Thus the C.B. electrons lying above this level no longer satisfy the Condition 2, i.e., these electrons are now aligned with energy levels corresponding to the 'Energy Gap'  $E_g$ , which must not be occupied by electrons. Only the remaining C.B. electrons that lie between  $E_{VP}$  and  $E_{CN}$  continue to satisfy the Condition 2. Thus, current due to Tunneling reduces. As we go on increasing forward bias, the N side energy bands move further upwards and those of the P side further downwards, thereby reducing the number of electrons available for tunneling. Thus, in this range of forward bias, the current reduces with increasing values of forward bias. Thus, this region is called "Negative Resistance Region". This is shown by Region 2 in the V-I characteristics.

**Fig.- 19:** - When the forward bias is in the range  $V_p < V_f < V_v$  the T-Diode exhibits Negative Resistance.

iv **Forward bias  $V_f = V_v$  (Valley Region):-** When a forward bias  $V_f$  is increased further, the net Barrier Potential further decreases. Consider that forward bias  $V_f = V_v$ . This results in the energy bands of the P& N regions realigning such that Energy Barrier reduces to less than  $E_0'''$  of the earlier case, as shown below in Fig-20. In this situation, the tunneling stops and thereafter the T-Diode behaves like a normal P-N junction.



Due to the realignment of the Energy Bands caused by the Forward Bias, the energy bands of the N-Region shift further up and those of the P-Region shift further down. At the value of forward bias  $V_F = V_v$ , the situation is such that the  $E_{CN}$  level is above  $E_{VP}$ . Thus, the entire CB is aligned with the Energy Gap. Thus, the CB electrons of N-Side no longer satisfy Condition-2. At this point Tunneling stops and the current reaches a low value  $I_v$ . As we go on increasing the forward bias further, the energy bands of N-Side slide further up and those of the P-Side slide down. This reduces the Energy Barrier to such an extent, that the CB electrons of the N-Side are able to overcome this under the influence of the Forward Electric Field. In other words, the Tunnel Diode begins to behave like an ordinary diode in FORWARD Conduction condition. This is represented by region-3 in the V-I Characteristics.

**Fig.20:** - When forward bias is greater than the value  $V_v$ , tunneling stops and the T-Diode begins to behave like a normal P-N junction.

**TUNNEL DIODE AT REVERSE BIAS :-** When a reverse bias is applied, the energy bands of the N-Region move downwards and those of the P-Region moves upwards. In this process, the Energy Barrier increases to a value greater than the equilibrium value. As a result of this re-alignment of the energy bands, the Fermi Level of the P-Side is now above that of the N-Side. The applied bias is of such a polarity that the electric field is directed from the N-Side towards the P-Side. This orientation of the electric field will now influence VB electrons lying between the Fermi Levels of the two sides to tunnel across the junction. Thus, a high value of reverse current will flow as soon as a reverse bias is applied. If the reverse bias is increased, the reverse current will also increase rapidly. This is equivalent to the situation of Break-Down. Therefore, the **Tunnel Diode is never operated in reverse bias condition.**

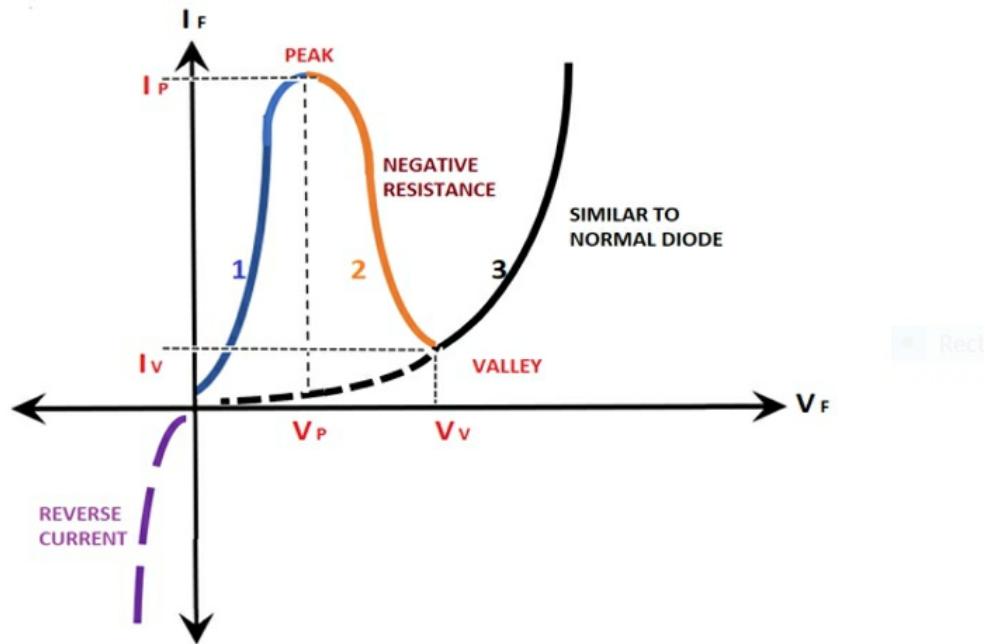
#### V-I CHARACTERISTIC OF TUNNEL DIODE

From the foregoing discussion the V-I Characteristic of the T-Diode will be as shown in Fig.-21, shown below.

From the discussion above, and from the V-I Characteristic, the following observations are made.

- a) As soon as a Forward bias is applied Tunneling Phenomenon starts and the forward current increases rapidly up to the PEAK point. This occurs due to tunneling of electrons from the Conduction band (CB) of N-Side into the Valance band (VB) of the P-Side.

- b) Current due to tunneling attains a peak value  $I_P$  at a forward bias  $V_f = V_P$ .
- c) When the forward bias is increased beyond  $V_P$  the tunneling phenomenon still continues, but the current begins to decrease due to the decrease in the number of electrons available for tunneling.
- d) The forward current attains a minimum value  $I_V$ , corresponding to a forward bias of  $V_V$ . This is the VALLEY point. At this point the tunneling phenomenon stops.
- e) When the forward bias is increased beyond  $V_V$  the diode behaves like a normal P-N junction. In this condition, the CB electrons can overcome the energy barrier and cross the junction like in a normal P-N junction diode.

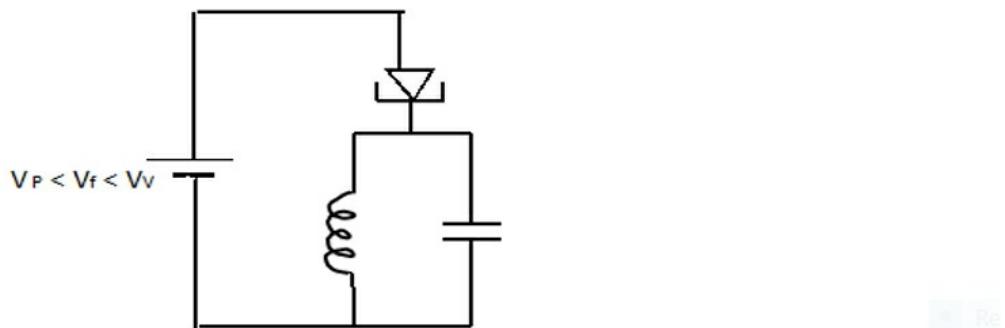


**Fig.21:** - V-I Characteristic of Tunnel Diode.

### APPLICATIONS

The Tunnel Diode is a special purpose diode, whose specialty is the existence of the Negative Resistance Region in the V-I Characteristics. The negative resistance occurs in the forward bias range of  $V_P < V_f < V_V$ . Thus, the operating range of the T-Diode is this range of voltages. The following are the two most common applications of the T-Diode.

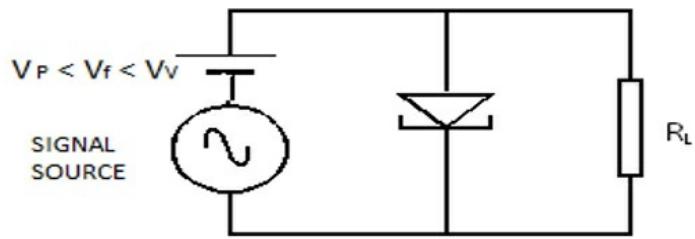
- (a) Sinusoidal Oscillator: -- The circuit diagram of the T-Diode Oscillator is as shown in the Fig. 22.



**Fig.-22:** - Application of Tunnel Diode in a Sinusoidal Oscillator Circuit.

- When a voltage pulse is applied to a L-C tank circuit, it produces sinusoidal oscillations at the resonant frequency  $f_0 = 1 / 2\pi \sqrt{LC}$
- However, the internal resistance of the coil will cause a power dissipation, due to which the amplitude of the oscillation will go on decreasing.
- When a T-Diode, biased in the Negative Resistance Region is connected in series the net resistance of the circuit can be made equal to zero. In this case there will be no power dissipation and the sinusoidal oscillations will be sustained.

- (b) Parallel Amplifier :- Parallel Amplifier is another common application of the T-Diode. It is a convention to represent a signal as an AC in electronic circuits. An amplifier is, in general capable of amplifying any signal. The circuit for the Parallel Amplifier is as shown in the Fig.-23. The working principle is discussed below.



**Fig.-23: - Tunnel Diode used as a Parallel Amplifier.**

- The T-Diode is biased to operate in the Negative Resistance Region. When the negative resistance of the T-Diode is connected in Parallel to the Load Resistance, the net resistance decreases. Thus, current in this parallel combination is greater than the source current. Hence, we get “Current Amplification”. However, since load and source are parallel, the load voltage is equal to source voltage. Therefore, voltage amplification does not occur.

##### SA-SD-SA-SD #####

# **UNIT - 2**

## **THE TRANSISTOR AMPLIFIERS AND OTHER APPLICATIONS**

# CHAPTER – V

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# THEORY OF BI-JUNCTION TRANSISTOR

## *THEORY OF BI-JUNCTION TRANSISTORS*

### INTRODUCTION

The BI-JUNCTION TRANSISTOR (BJT), also known as BIPOLEAR JUNCTION TRANSISTOR (BJT), is a very versatile and important electronic device. It has two primary functions, namely,

(i) **Amplification**

And

(ii) **Switching.**

**Many varied applications are implemented with this device, either in discrete form or as integrated component in IC's.**

### Section-1 *Transistor Action*

#### 5.1 Transistor Action and Schematic Diagram

##### CONSTRUCTION

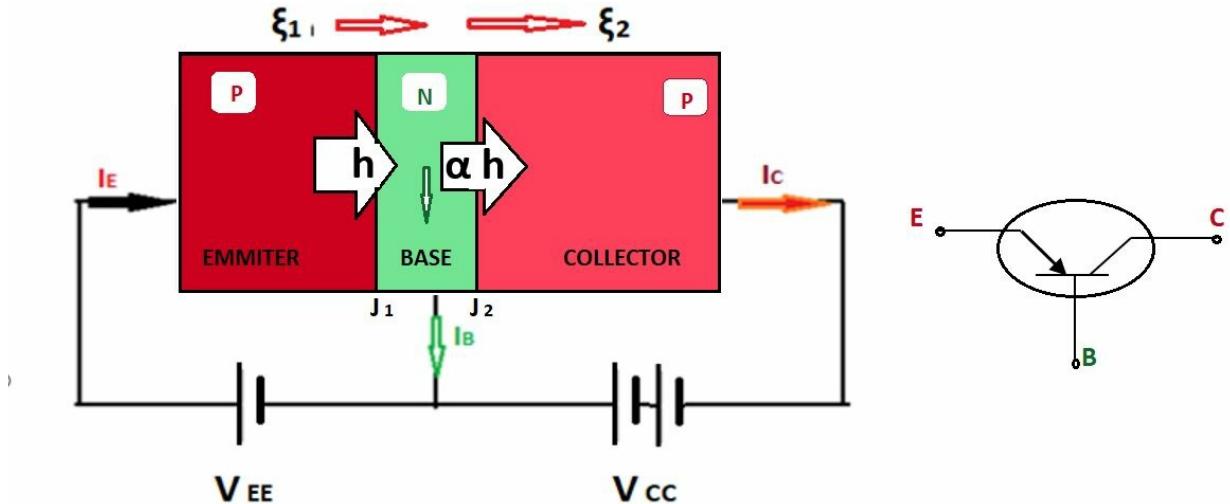
- The BJT consists of two P-N junctions constructed back-to-back on a single crystal of semiconductor.
- It can have two forms, namely,
  - (a) PNP or (b) NPN.
  - Both these forms have the same applications. In fact, the PNP and the NPN transistors are said to be **Duals** of each other.
  - In the PNP transistor the majority carrier current is due to Holes and in the NPN transistor, the majority carrier current is due to

Electrons.

- But in both of them, the minority carriers also constitute a current, which plays a very significant role in the stability of operation of the device.
- Since these devices are composed of two P-N Junctions, they are called “Bi-Junction Transistors” and since current flow is due to both majority carriers as well as minority carriers, i.e., carriers of both the polarities, hence they are also known as “Bipolar Transistors”.
- Some authors prefer to call them “Bipolar Junction Transistors (BJT)”.

### **PNP Transistor: -**

- ❖ A BIPOLAR JUNCTION TRANSISTOR (BJT), consists of **three** distinct layers of extrinsic semiconductors and **two** distinct P-N Junctions.
- ❖ The schematic diagram of the PNP transistor is shown in the Fig- 1 below.
- ❖ The first region is a heavily doped, P-Type region of large volume. This is called the “**Emitter**”. The middle region is very narrow (thin) and very lightly doped N-Type region. This region is called the “**Base**” of the transistor. The third region is also a P-Type region, of much larger volume than the Emitter and it is moderately doped, with a doping level lesser than the emitter region. This region is called the “**Collector**”.



**Fig.-1:** - Schematic Diagram and Circuit Symbol of PNP Transistor. The biasing potentials and the flow of majority carrier (holes) and the resulting current is for **Active Bias**.

### Working Principle (PNP)

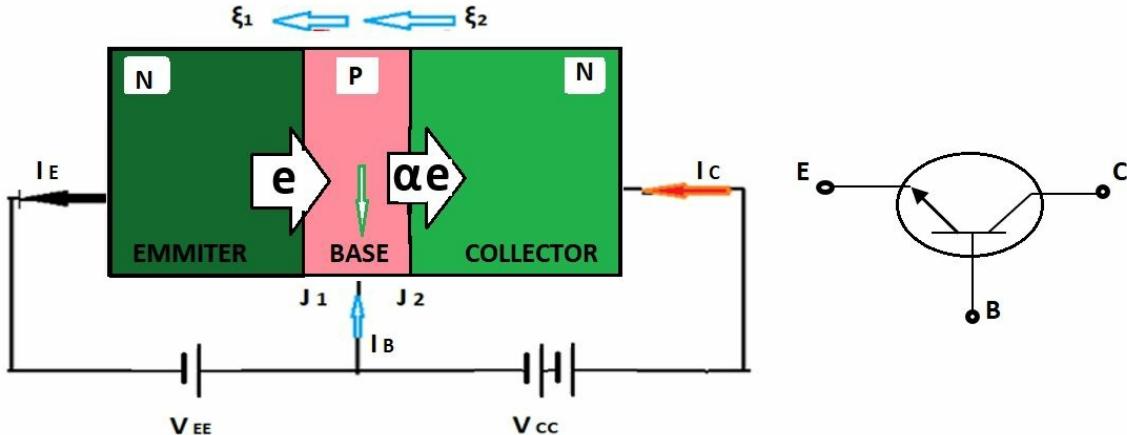
- ❖ The positive terminal of  $V_{EE}$  is connected to the P side and the negative terminal is connected to the N side. Therefore, the Emitter-Base junction, **(E-B junction),  $J_1$  is Forward Biased.**
- ❖ The negative terminal of  $V_{CC}$  is connected to the P side of the second P-N junction  $J_2$  and the positive terminal of  $V_{CC}$  is connected to the N side. Hence the Collector-Base junction, **(C-B junction) ,  $J_2$  is Reverse Biased.**
- ❖ The associated electric fields  $\xi_1$  and  $\xi_2$ , respectively are set up by  $V_{EE}$  and  $V_{CC}$  at the junctions  $J_1$  and  $J_2$ . The directions of these two electric fields is as shown in the figure above.
- ❖ Due to the application of the Forward Bias at the junction  $J_1$ , a large number of majority carrier “**h**” (Holes) will be **injected** by the Emitter in to the Base Region.
- ❖ This flow of holes from the Emitter gives rise to the **Emitter Current  $I_E$** .
- ❖ The Base region is N-Type. Hence some of the injected holes will be neutralized by the free electrons present in the N-Type Base. This flow of carriers due to the **recombination** process will give

rise to the **Base Current  $I_B$** .

- ❖ However, since the Base region is very narrow and since it is very lightly doped, it has a very few numbers of free electrons. Hence very few of the injected holes get neutralized in the base and constitute the **Base Current  $I_B$** . This current is very small in magnitude.
- ❖ A large fraction ‘ $\alpha$ ’ of the injected holes remain in the Base region. These are subjected to the electric field  $\xi_2$  of the junction  $J_2$ . This electric field is oriented from the N-type Base towards the P-type Collector. These remaining holes numbering “ $\alpha h$ ” are accelerated along the direction of the electric field. Thus, these holes are said to be **transported into** the Collector region.
- ❖ These “transported” holes constitute the **Collector Current  $I_C$** .
- ❖ It is observed that the Emitter current flows into the emitter terminal. Hence this terminal is indicated with an incoming arrow in the symbol of the PNP Transistor.

#### NPN Transistor: -

- ❖ In NPN Transistor the **Emitter region is a heavily doped with N-Type impurity**, the **Base region is very lightly doped P-type impurity** and the **Collector region** is doped with **N-Type impurity** with a concentration less than the emitter.
- ❖ The negative terminal of  $V_{EE}$  is connected to the N side and the positive terminal is connected to the P side. Therefore, the **Emitter-Base Junction  $J_1$  (E-B junction), is Forward Biased**.
- ❖ The negative terminal of  $V_{CC}$  is connected to the P side of the **Collector-Base junction  $J_2$ , (C-B junction) is Reverse Biased**.
- ❖ The Forward Bias at the junction  $J_1$ , **injects** a large number of majority carrier electrons “ $e$ ” in to the Base Region.
- ❖ This flow of electrons from the Emitter gives rise to the **Emitter Current  $I_E$** . Since electrons are flowing, the current direction is opposite to electron flow, as shown in the figure.



**Fig- .2:** - Schematic Diagram of NPN Transistor and Circuit Symbol. The potentials and the direction of flow of majority carrier (electrons) and the resulting currents is shown.

- ❖ Since the **Base region is P-Type**, some of the injected electrons will be neutralized by the holes present in the P-Type Base. This flow of carriers due to the **recombination** process will give rise to the **Base Current  $I_B$** .
- ❖ However, since the Base region is very narrow and since it is very lightly doped, it has a very few numbers of holes. Hence the **Base Current  $I_B$  is very small in magnitude**.
- ❖ A large fraction ‘ $\alpha e$ ’ of the injected electrons remaining in the Base region are **transported** by the electric field  $\xi_2$  into the Collector region, thereby constituting the **Collector Current  $I_C$** .
- ❖ Since the Emitter current flows out of the emitter terminal it is indicated with an outward arrow in the electrical symbol of the NPN Transistor.

## TRANSfer – reSISTOR

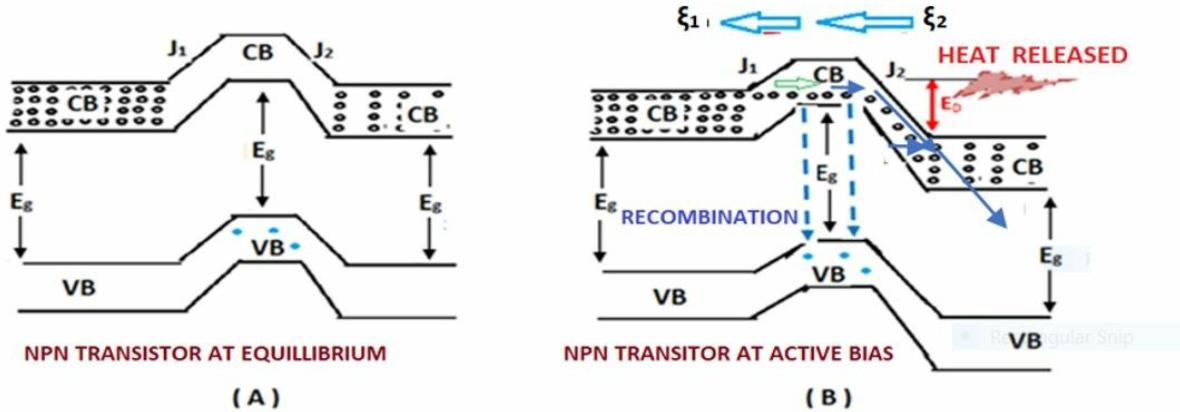
- It is observed in both the cases of the NPN and PNP Transistors the Emitter-Base Junction  $J_1$  is Forward Biased while the Collector-Base Junction  $J_2$  is Reverse Biased.
- A forward biased P-N junction has a **very low resistance**, while a reverse biased P-N junction has a **very high resistance**.

- In the transistor, a current is transported or ‘**transferred**’ from the very low resistance E-B circuit to the very high resistance C-B circuit.
- Thus, we can visualise that the transistor is a **RESISTOR** that **TRANSFERS** a current from one terminal to another. Hence the name **TRANsfer-re**SISTOR**** or **TRANSISTOR**.

**This process of majority carrier transportation from the E-B junction to the C-B junction is known as THE TRANSISTOR ACTION.**

### **Transistor Action in Terms of Energy Band Theory**

- Recall that in the equilibrium condition, the energy bands of a P-N Junction are aligned in such a manner that the **lower-most energy level  $E_{CP}$**  of the CB of the P-side is aligned with the **upper-most energy level  $E_{CN}$**  of the CB of the N-side and that the **lower-most energy level  $E_{VP}$**  of the VB of the P-side is aligned with the **upper-most energy level  $E_{VN}$**  of the VB of the N-side.
- This results in the situation that, **both the CB and VB P-side are aligned slightly above the corresponding energy bands of the N-side**. This gives rise to an “Energy Barrier”  $E_0$  between the P-side and the N-side.
- Recall again that when a **forward bias is applied the energy barrier is reduced while, when a reverse bias is applied the energy barrier increases**.
- The **energy band diagram of an N-P-N transistor** at equilibrium (no bias is applied) is shown in the Fig.- 3(A).
- Application of forward bias to the E-B junction  $J_1$  results in the reduction of the energy barrier between the Emitter and the Base regions. The reverse bias in C-B junction  $J_2$  results in the increase of the energy barrier between the Collector and the Base regions. This situation is shown in of Fig. – 3(B).



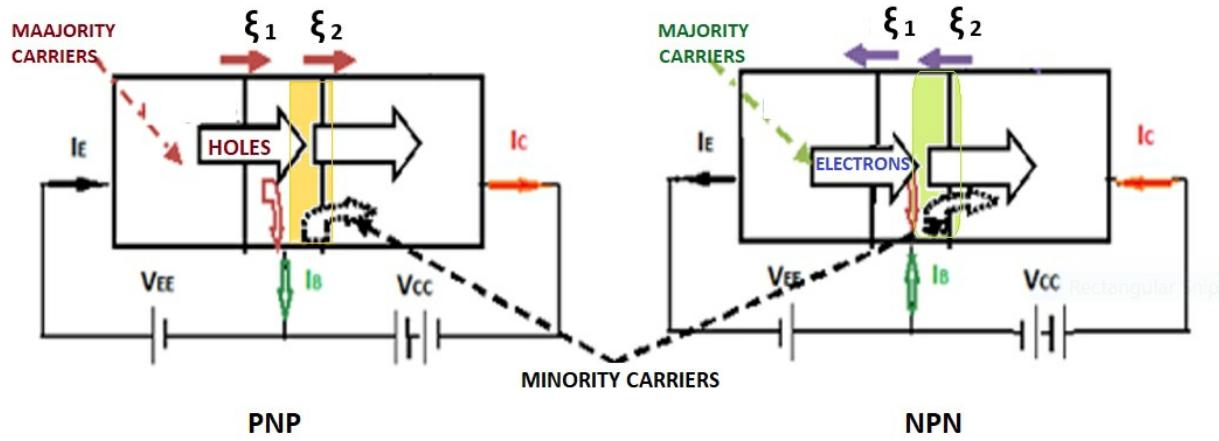
**Fig- 3: - Energy Band Diagram of N-P-N Transistor (A) When it is at Equilibrium (Unbiased); (B) When it is biased with Forward bias on  $J_1$  and Reverse Bias on  $J_2$ .**

- At equilibrium condition the Energy Barrier of  $E_0$  between the N-side and P-side of a P-N Junction prevents the flow of majority carriers.
- When Forward Bias is applied at the Emitter-Base Junction  $J_1$  the energy barrier gets reduced. Now some of the free electrons in the CB of the emitter region are aligned with the vacant energy levels of the CB of the base region. The orientation of the electric field  $\xi_1$  at  $J_1$  is from Base towards Emitter. Therefore, this electric field will inject these free electrons from the emitter into the base region.
- Since base region is very thin and very lightly doped only a few of the injected electrons will be able to recombine with a few holes. This is shown by BLUE ARROW in the figure.
- The large fraction ‘ $\alpha$ ’ of the remaining electrons are influenced by the electric field  $\xi_2$  of the Collector-Base junction  $J_2$ . This electric field is oriented from the Collector region to the Base region. Thus, this electric field will transport (“push”) these electrons in to the collector. The process of transportation is shown with a thick BLUE ARROW pointing downwards into the collector.
- In this transportation process the electrons have to move down

from the CB of the P-type Base to the CB of the N-type Collector. These two energy levels are separated by an energy difference  $E_D$ , as shown in the figure. The transported electrons release this difference of energy is released in the **form of heat**. This is shown by ORANGE ARROW in the figure above.

## 5.2 Transistor Current Equation and Primary Transistor Parameters (DUALITY of PNP and NPN Transistors)

The action of the PNP and NPN transistors are shown in a little more detail, in Fig-4.



**Fig-4:** - Similarities between PNP & NPN Transistors and their 'Duality'.

- In the PNP Transistor the Emitter Current  $I_E$  enters the transistor while the Base Current  $I_B$  and Collector Current  $I_C$  come out of it. Application of Kirchhoff's Current Law (KCL) gives the expression (A)

$$I_E = I_C + I_B \text{ (A)}$$

- In the NPN Transistor, the Collector Current  $I_C$  and Base Current  $I_B$  enter the transistor the Emitter Current  $I_E$  come out of it. Application of KCL gives the expression (B)

$$I_C + I_B = I_E \text{ (B)}$$

- Since these two expressions are the same, we get the **First Transistor Current Equation**.

$$I_E = I_C + I_B \quad \dots(1)$$

- Referring back we have that the Emitter Current  $I_E$  is due the flow of Majority Carriers due to the forward bias on junction  $J_1$  (holes in case of PNP and electrons in case of NPN). The collector current  $I_C$  is due the **large fraction** “ $\alpha$ ” those majority carriers that get **transported** from the Base Region in to the Collector Region due to the electric field  $\xi_2$  of the reverse biased C-B junction. Thus we have an expression for  $I_C$  and the quantity “ $\alpha$ ” (**known as “Transport Factor”**).

$$I_C = \alpha I_E \quad \dots(2(a))$$

$$\therefore \alpha = \frac{I_C}{I_E} \quad \dots(2(b))$$

“ $\beta$ ”

We can define a quantity “ $\beta$ ” as the ratio of the Collector Current  $I_C$  with respect the Base Current  $I_B$ . This quantity “ $\beta$ ” is **known as the “Current Amplification Factor”**.

$$\beta = \frac{I_C}{I_B} \quad \dots(3)$$

- These two quantities “ $\alpha$ ” and “ $\beta$ ” are called the **Primary Transistor Parameters**.

### Relationship between $\alpha$ and $\beta$

$$\frac{I_E}{I_C} = 1 + \frac{I_B}{I_C}$$

$$\therefore \frac{1}{\alpha} = 1 + \frac{1}{\beta} = \left\{ \frac{(1 + \beta)}{\beta} \right\}$$

$$\therefore \alpha = \frac{\beta}{(1 + \beta)} \quad \dots(4)$$

Again

$$\frac{1}{\beta} = \left( \frac{1}{\alpha} - 1 \right) = \left\{ \frac{(1 - \alpha)}{\alpha} \right\}$$

$$\therefore \beta = \frac{\alpha}{(1 - \alpha)} \quad \dots(5)$$

Dividing **both sides of Eq.- 1 by  $I_C$**  we have

### Minority Carrier Current ( $I_{CO}$ )

- So far, in both the PNP and NPN transistor we have only considered the Majority Carrier.
- In the transistor the Base-Collector junction  $J_2$  is reverse biased. In a reverse biased P-N junction there occurs a Depletion Region. In this Minority Carriers are generated due to thermal energy of the surroundings . These constitute the Minority current component  $I_{CO}$ . This is true for both PNP and NPN transistors (Fig-4).
- This current adds up with the Collector current due to Majority carriers. Thus, the net collector current of either PNP or NPN transistor is as follows-

$$I_C = \alpha I_E + I_{CO} \quad \dots(6)$$

### **Second Transistor Current Equation**

If we substitute Eq-1 in Eq-6 we get

$$I_C = \alpha (I_C + I_B) + I_{CO}$$

$$\therefore (1 - \alpha) I_C = \alpha I_B + I_{CO}$$

$$\therefore I_C = \left\{ \frac{\alpha}{(1-\alpha)} \right\} \cdot I_B + \left\{ \frac{I_{CO}}{(1-\alpha)} \right\}$$

|From Eq- 5

$$\frac{\alpha}{(1-\alpha)} = \beta \quad \text{and} \quad \left\{ \frac{1}{(1-\alpha)} \right\} = (1 + \beta)$$

$$\therefore I_C = \beta I_B + (1 + \beta) I_{CO} \quad \dots(7)$$

This expression is a very important expression for transistor operation and is known as “**The Second Transistor Current Equation**”.

### **Duality between P-N-P and N-P-N Transistors**

In both the PNP and the NPN transistors the E-B Junction  $J_1$  is forward biased and the C-B Junction  $J_2$  is reverse biased. This form of biasing in a transistor is known as ‘Active Bias’.

1. As a result of Active Biasing Majority Carriers from the

Emitters are injected into the Base and the large fraction ‘ $\alpha$ ’ of the majority carriers that still remain in the Base after recombination are transported into the Collector. This action occurs both in the PNP and NPN Transistors.

2. The equations for the currents and the transistor parameters from Eq-1 to Eq-7 are the same for both PNP and NPN transistors.
3. Even though the overall action equations governing the action of both PNP and NPN transistors are the same, however, the following differences are present (1) Polarity of each of the biasing sources  $V_{EE}$  and  $V_{CC}$  are opposite between PNP and NPN and (2) The directions of each of the currents  $I_E$ ,  $I_C$ ,  $I_B$  and  $I_{CO}$  are exactly opposite in PNP and NPN transistors.

**The discussion above suggests that either the PNP or the NPN transistor may be used for the same applications provided the biasing polarity is reversed.**

**Thus, the PNP and NPN transistors are known as DUALS of each other.**

### **Typical Values of Transistor Currents and Transistor Parameters**

Numerical values of the various currents and the parameters of the transistor vary from device to device depending upon the conditions of manufacturing. However, for the purpose of studying the device further the list of numerical values of these quantities of a typical transistor may be considered as follows.

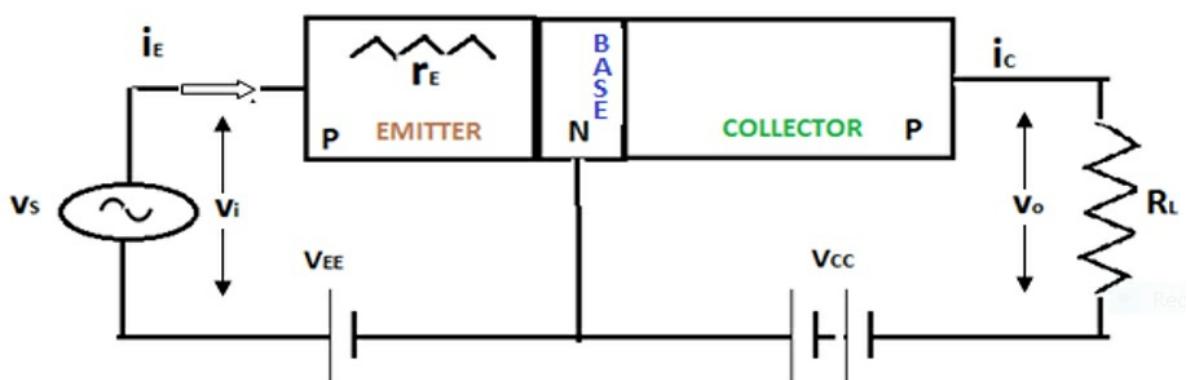
1. Emitter Current  $I_{E\ MAX} = 100$  mA.
2. Collector Current  $I_{C\ MAX} = 98$  mA.
3. Base Current  $I_{B\ TYPICAL} = 98$   $\mu$ A.
4.  $I_{CO}$  (at  $300^0K$ )  $= 10$   $\mu$ A.
5. Transport Factor  $\alpha = 0.98$
6. Current Gain Factor  $\beta = 1000$

## Section-2

### ***Transistor Amplifier Configurations & Transistor Characteristics***

#### **5.2 Concept of Amplification**

- The function of an Amplifier is to increase the current and voltage levels of a signal produced by a “Source” and apply the amplified signal across a “Load”.
- It is a convention to show the signal source as an AC source. The load is shown as a pure resistance  $R_L$ . A Transistor is used for the purpose of amplification. The schematic is shown in the Fig-5, below.



**Fig- 5.: - Transistor Amplifier Action**

- In a transistor the Emitter-Base junction is forward biased. Therefore, it has a very low resistance  $r_E$ .

In the transistor the collector current and emitter current are related by

$$i_C = \alpha i_E$$

where the numerical value of “Transport Factor”  $\alpha = \geq 0.98$

$$\therefore i_C \approx i_E$$

Input voltage and Output voltage are respectively,

$$v_i = i_E \cdot r_E$$

$$v_o = i_C \cdot R_L$$

$$\text{However, since } i_C \approx i_E$$

And since

$$R_L > r_E$$

$$\therefore$$

$$v_o > v_i \dots (8)$$

**The Eq-8 demonstrates amplification**

## 5.4 THE THREE TRANSISTOR CONFIGURATIONS FOR AMPLIFIERS

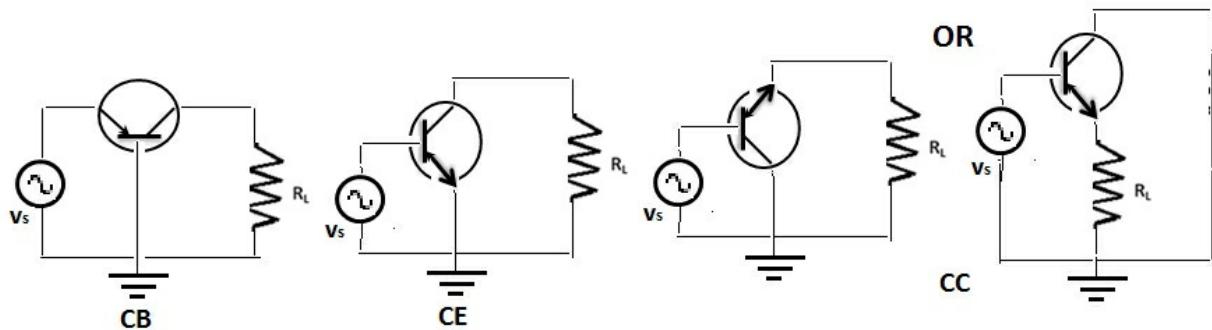
- Transistor (BJT) has three terminals, the **signal source** is connected to one terminal, the **load resistance** is connected to the second terminal and the third terminal is to be connected common “Ground” terminal so that it is common to both the “Source Circuit” and the “Load Circuit”.
- Accordingly, we can have three possible Configurations in which the Transistor Amplifier can work. Namely --

1. **Common Base Configuration (CB)**
2. **Common Emitter Configuration (CE)**
3. **Common Collector Configuration (CC)**

- Amplifiers connected in each of these configurations have certain distinct characteristics.
- **The conceptual circuit diagrams of these three configurations are as follows-**

(The circuits are shown with PNP or NPN transistors, at a random mix. Since the PNP and NPN are “Duals” of each other, any one of

them can be used as per requirement)



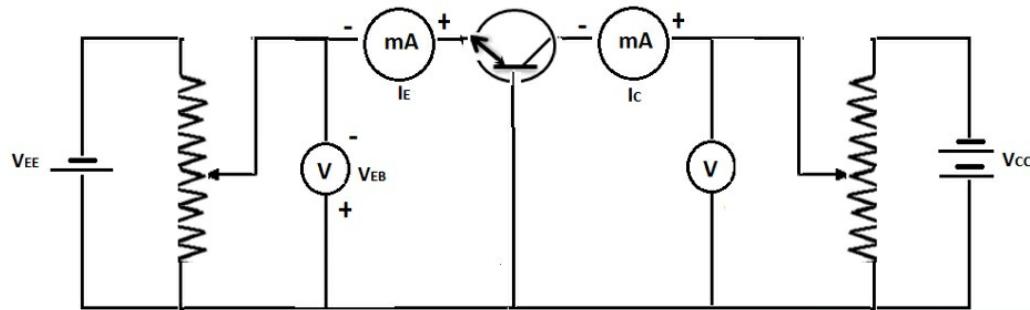
**Fig. 6**

## Transistor Characteristics

- ❖ The behaviour and property of any electrical or electronic device is determined by the graph of the relationship of current in the device under the application of potential difference across its terminals, (V-I Characteristics).
- ❖ The task of designing any application using such a device is based on these V-I Characteristics.
- ❖ Referring to the Conceptual Transistor Amplifier in the Fig-5, note that this involves two sets of currents and voltages, namely the input current and the input voltage and the output current and the output voltage.
- ❖ Thus, we define two sets of V-I characteristics of the transistor, namely, the **Input Characteristics and the Output Characteristics**.
- ❖ Since there are three configurations for amplifiers, accordingly we would have three sets of I/P & O/P characteristics for the same device. However, it is a common practice to plot only the **Common Base** and **Common Emitter** characteristics.
- ❖ These characteristics are obtained by an experiment in the lab and are plotted on the basis of the result of that experiment.

### Common Base Characteristics

The circuit shown in the Fig-7 is set up in the lab.



**Fig-7**

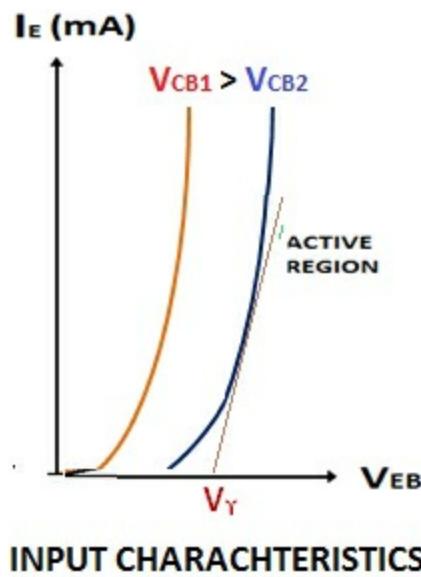
### The Experiment

**Input Characteristics** :- The electrical quantities associated with the input terminal in the Common Base configuration are (i) **Input Voltage  $V_{EB}$  and** (ii) **Input Current  $I_E$** .

#### PROCEDURE:

1. **The rheostat on the collector side is kept at a fixed position so that the Output Voltage  $V_{CB}$  remains at a constant value say,  $V_{CB\ 1}$ .**
2. The rheostat on the emitter side is slowly varied step-by-step from the lowermost point and the values of Input Voltage  $V_{EB}$  and Input Current  $I_E$  are noted at each step. A graph is plotted between  $V_{EB}$  and  $I_E$  by taking  $V_{EB}$  along x-axis and  $I_E$  along y-axis.
3. The experiment is repeated by using a higher value of output voltage  $V_{CB\ 2} > V_{CB\ 1}$  and the corresponding graph is plotted. This may be repeated for any number of higher values of  $V_{CB}$ .

**SHAPE:** -- Since the input terminal of the transistor is forward biased, it is expected that the shape of the Input Characteristics is similar to the shape of the V-I Characteristic of a forward biased P-N Junction.



**Fig-8**

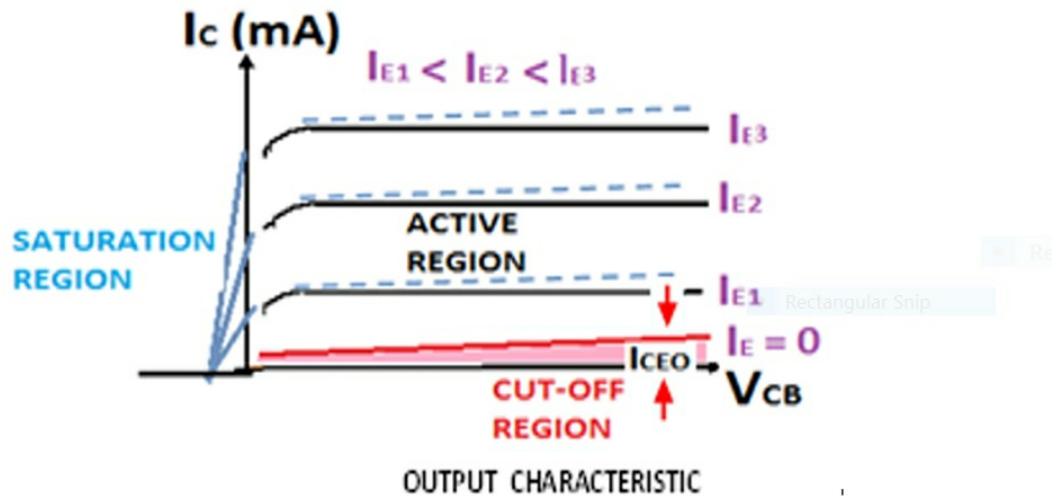
**Output Characteristics :-** The electrical quantities associated with the output terminal in the Common Base configuration are (i) **Output Voltage  $V_{CB}$**  and (ii) **Output Current  $I_C$** .

**PROCEDURE:**

1. The rheostat on the emitter side is kept at a **fixed** position so that the Input Current  $I_E$  remains at a constant value say,  $I_{E1}$ .
2. The rheostat on the collector side is slowly varied step-by-step from the lowermost point and the values of Output Voltage  $V_{CB}$  and Output Current  $I_C$  are noted at each step. A graph is plotted between  $V_{CB}$  and  $I_C$  by taking  $V_{CB}$  along x-axis and  $I_C$  along y-axis.
3. The experiment is repeated by using a higher value of input current  $I_E$   $2 > I_E 1$  and the corresponding graph is plotted. This may be repeated for any number of higher values of  $I_E$ .

**SHAPE:** -- It was observed in Section– 1 that the collector current  $I_C$  is independent of the collector voltage and dependent only on the value of  $I_E$ , (Eq.- 2).

$$I_C = \alpha I_E$$



**Fig-9**

Hence, the shape of the Output Characteristic are a set of horizontal lines, independent of voltage, and these lines occur at a height proportional to the value of  $I_E$  at which it is evaluated. This is verified by means of the present experiment.

### The Three Regions of the Transistor Characteristics

When we examine the output characteristic graph we observe three distinct regions, which are (i) Active Region, (ii) Saturation Region and (iii) Cut-Off Region

**Active Region** is defined as that region of the characteristics in which the equation for the collector current given by Eq. 2 is valid, namely, the region in which the collector current is constant w.r.t. the collector voltage. **This is the region in which the transistor acts as an amplifier.** In this region the Emitter-Base junction  $J_1$  is Forward Biased and the Collector-Base junction  $J_2$  is Reverse Biased. In terms of the Input Characteristics (Fig.-8), the Active Region is that in which the input voltage  $V_{EB}$  is greater than the Threshold voltage  $V_T$  and therefore input current  $I_E$  is sharply, and, almost linearly increasing w.r.t. the emitter voltage  $V_{EB}$ .

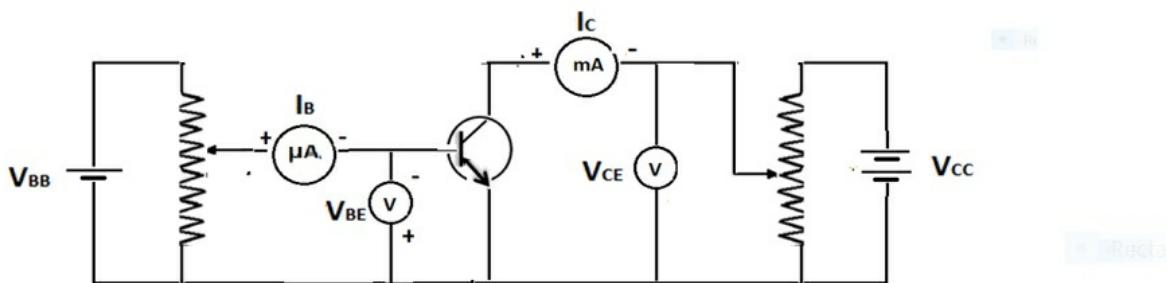
**Saturation Region** is defined as the region in which the collector

current rises sharply w.r.t. the collector voltage. In this region the transistor is not acting as an amplifier. In this region both the Emitter – Base junction and the Collector-Base junction are Forward Biased. In fact, the **transistor acts as a Closed Switch in this region**.

**Cut-Off Region** is defined as the region in which the collector current is plotted by keeping the input terminal Open Circuited. This is done by adjusting the input current to zero ( $I_E = 0$ ). Hence, the collector current is entirely due to the reverse saturation current of the junction  $J_2$ . In the graph this current is denoted as  $I_{CEO}$  (Collector current when ‘Emitter is Open’). In this region also, the transistor is not acting as an amplifier. In this region both the Emitter – Base junction and the Collector-Base junction are Reverse Biased. In fact, the **transistor acts as an Open Switch in this region**.

### Common Emitter Characteristics

The circuit shown in the Fig-10 is set up in the lab.



**Fig-10**

**Input Characteristics** :- The electrical quantities associated with the input terminal in the Common Emitter configuration are (i) **Input Voltage  $V_{BE}$**  and (ii) **Input Current  $I_B$**  (in  $\mu\text{A}$ ).

### PROCEDURE:

1. The rheostat on the collector side is kept at a **fixed** position so that the Output Voltage  $V_{CE}$  remains at a constant value say,  $V_{CE 1}$ .
2. The rheostat on the base side is slowly varied step-by-step from the lowermost point and the values of Input Voltage  $V_{BE}$  and Input Current  $I_B$  are noted at each step. A graph is plotted between  $V_{BE}$  and  $I_B$  by taking  $V_{BE}$  along x-axis and  $I_B$  along y-axis.

3. The experiment is repeated by using a higher value of output voltage  $V_{CE} 2 > V_{CE} 1$  and the corresponding graph is plotted. This may be repeated for any number of higher values of  $V_{CE}$ .

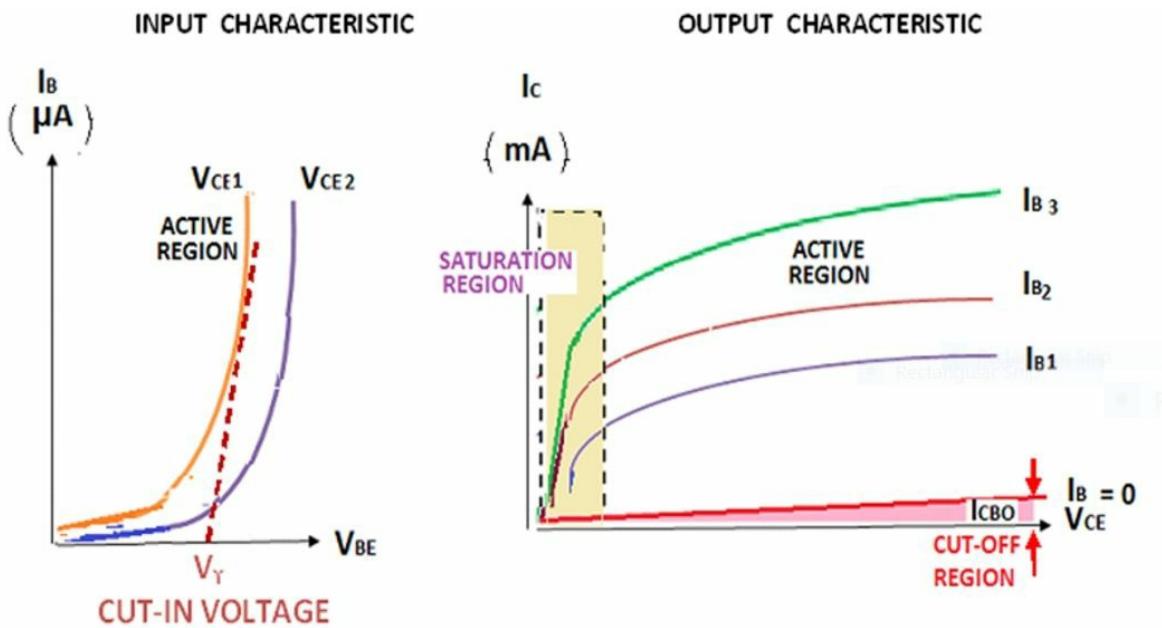
**SHAPE:** -- Since the input terminal of the transistor is forward biased, it is expected that the shape of the Input Characteristics is similar to the shape of the V-I Characteristic of a forward biased P-N Junction. This is verified by means of the present experiment.

**Output Characteristics :-** The electrical quantities associated with the output terminal in the Common Base configuration are (i) **Output Voltage  $V_{CE}$  and** (ii) **Output Current  $I_C$**  ( in mA).

#### PROCEDURE:

1. The rheostat on the base side is kept at a fixed position so that the Input Current  $I_B$  remains at a constant value say,  $I_{B1}$ .
2. The rheostat on the collector side is slowly varied step-by-step from the lowermost point and the values of Output Voltage  $V_{CE}$  and Output Current  $I_C$  are noted at each step. A graph is plotted between  $V_{CE}$  and  $I_C$  by taking  $V_{CE}$  along x-axis and  $I_C$  along y-axis.
3. The experiment is repeated by using a higher value of input current  $I_B 2 > I_B 1$  and so on Thereafter the corresponding graph is plotted. This may be repeated for any number of higher values of  $I_B$ .

**SHAPE :**-- It is observed from equation Eq- 7 that the collector current  $I_C$  is independent of the collector voltage and dependent only on the value of  $I_B$  Hence the shape of the Output Characteristic is expected to be a set of horizontal line at a height proportional to the value of  $I_E$  at which it is evaluated. However, in case of the Common Emitter configuration the output current begins to rise sharply for very small values of  $V_{CE}$ , signifying the Saturation Region before becoming constant at higher values of  $V_{CE}$ . At this point the transistor comes into the Active Region. This is verified by means of the present experiment.



**Fig- 11**

## 5.5 Early Effect or Base-Width Modulation

In the previous sections we discussed the shape of the Input and Output Characteristic curves of a transistor for both CB and CE configurations. We note the following discrepancies in the discussion.

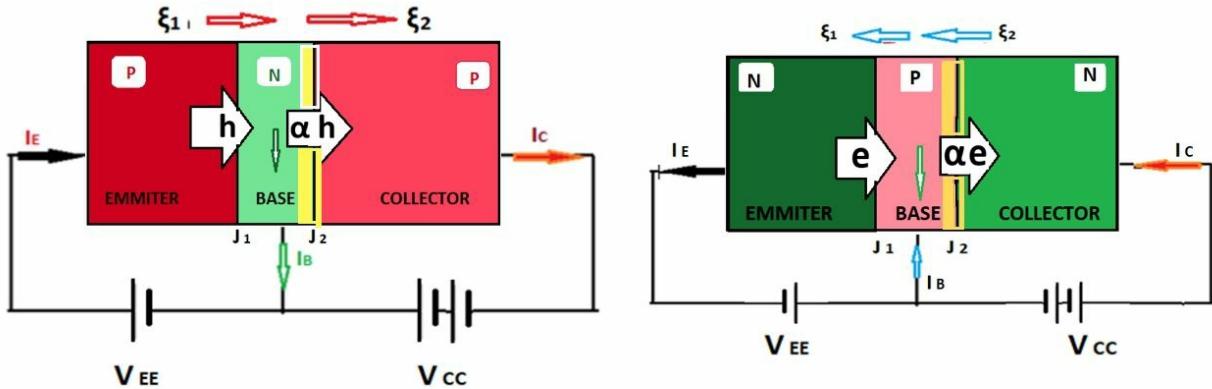
- The Input Characteristic curve should have been of the same shape and trace irrespective of the voltage applied to the collector terminal, since the Input Characteristic curve is supposed to show the relationship between current and voltage of the forward biased Input junction  $J_1$ . Instead of this we get different traces for the input current when the output voltage varies.
- The Output Characteristic graph should have been exactly parallel to the x-axis irrespective of the voltage applied to the output terminal, i.e., the collector since the expression for collector current  $I_C$  given by Eq. 2 and Eq. 7 are independent of collector voltage. Instead of this we get a slight upward slope in the trace of the output characteristic graphs, which means that the collector current is not really independent of collector voltage.

**These discrepancies are explained by Early Effect.**

**Early Effect on Input Characteristics**

## (CB Configuration)

- Due to the applied forward bias at the Emitter-Base junction  $J_1$  a large number of majority carrier holes are injected into the Base. Injection of majority carriers across a P-N junction is proportional to the Density Gradient of the majority carriers.
- The Collector-Base junction  $J_2$  is reverse biased. The width of the Depletion Region is Directly proportional to the Reverse bias, but Inversely proportional to the Doping Concentration.
- The Base region is very lightly doped compared to the Collector region. Therefore, Depletion Layer is very wide in this region. Thus, the effective width of the base will reduce. The width of the Depletion Region will be Modulated by the Reverse Bias voltage. As the width of the depletion region is controlled by the reverse bias, the **effective width** of the Base Region will also vary in the reverse order. **This phenomenon is called “Base Width Modulation”.**
- When this happens, the number of majority carriers in the base will reduce, so that the majority carrier gradient across the Emitter-Base junction will increase. This will result in the injection of a greater number of holes across the junction, resulting in the increase of the Emitter Current  $I_E$ .
- Thus ‘**A certain amount of Emitter Current  $I_E$  will flow at lesser value of forward bias  $V_{EB}$  when the reverse bias  $V_{CB}$ , of the C-B junction is increased, compared to the amount of  $V_{EB}$  required to cause that same amount of  $I_E$  when  $V_{CB}$  is lesser.**’
- This reasoning explains the situation that, the Input Characteristic Curves shift to the left when the Reverse bias  $V_{CB}$  is higher and vice-versa.



**Fig- 12:- (Early Effect)** Crystal Model of PNP and NPN transistors showing majority carrier injection from Emitter, recombination at Base and transportation into Collector. Depletion Region of the reverse biased Collector-Base junction  $J_2$  is also shown.

### Early Effect on Output Characteristics (CB Configuration)

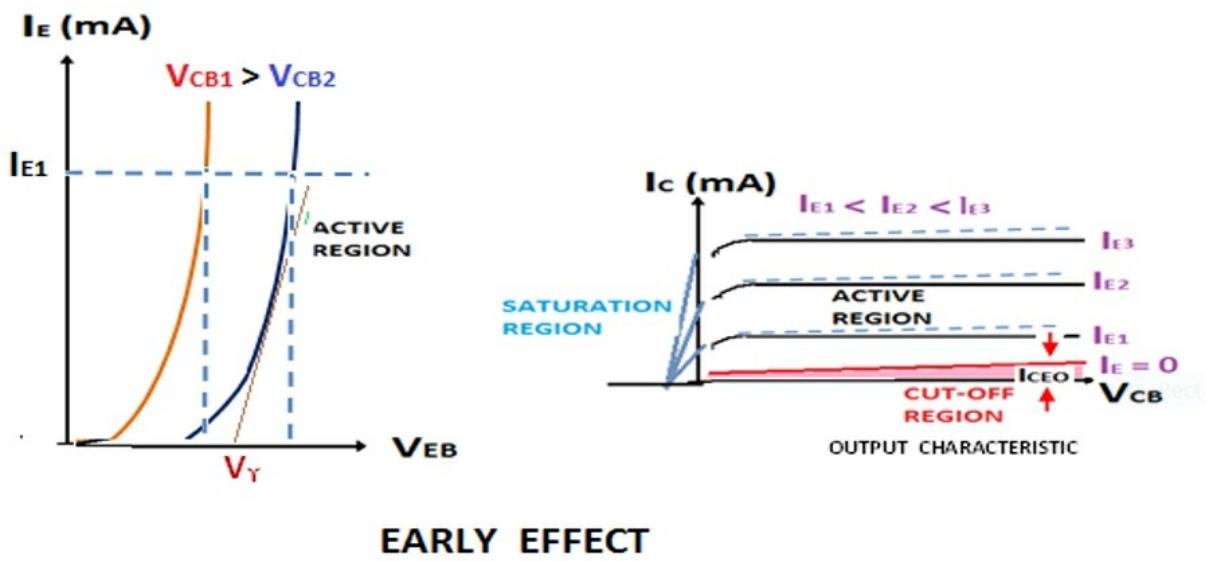
- Due to Base Width Modulation, the effective Base Width decreases with increasing reverse bias. This results in increase in Concentration Gradient between the majority carriers of the Emitter and the Base regions. This results in an increased flow of holes from Emitter to Base.
- Since the effective base width is reduced, fewer number of majority carrier electrons remain in the base. Thus, a smaller number of the holes is neutralized in the Base region, resulting in more holes remaining within the base region, to be transported into the collector region by Transistor Action. This results in an increase in Collector Current  $I_C$  with increasing values of the Collector Bias  $V_{CB}$ . This explains the slight upward slope of the Output Characteristic curves.

### Early Effect on Input Characteristics (CE Configuration)

- Due to Base Width Modulation, the effective Base Width decreases with increasing Reverse Bias on the collector. This results in less recombination of Majority Carrier electrons in the Base Region. **This results in a decrease of the Base Current  $I_B$**

**with increasing collector voltage.**

- Thus, a larger amount of Forward Bias  $V_{EB}$  will have to be applied to get a certain amount of Base Current  $I_B$  when the Reverse Bias  $V_{CE}$  is higher compared to the case when the Reverse Bias was lesser.
- This reasoning explains the situation that, the Input Characteristic Curves shift to the right when the Reverse bias  $V_{CE}$  is higher and vice-versa.

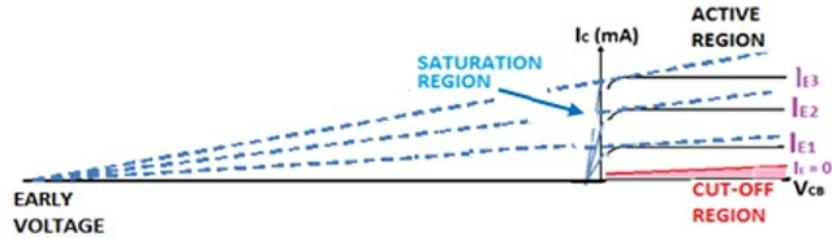


**Fig- 13**

### Early Effect on Output Characteristics (CE Configuration)

Due to Early Effect, the output characteristic graph tends to have a slight upward slope. Consider the Output Characteristic of CB configuration. The Output Characteristics have a slight upward slope due to Early Effect, which is shown with dotted lines in the Fig- 13. If we extrapolate these lines, they tend to meet at a single point in the second quadrant. The voltage corresponding to this point is called the **Early Voltage**. This is shown in the figure below--

**This discussion applies to both PNP and NPN transistors.**



**Fig-15:-** Early Voltage of a transistor is defined as the point of convergence of the output characteristic traces, when they are projected into the second quadrant.

### Section - 3 Biasing Circuits: Load Line: Bias Stability

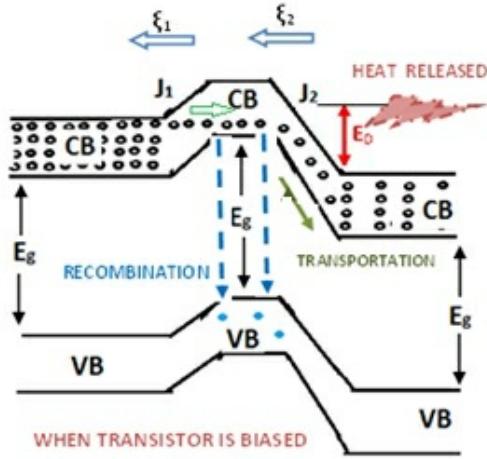
## 5.6 Transistor Biasing Circuits

### Purpose of Biasing Circuit

- To provide Forward Bias to Emitter-Base junction ( $J_1$ ) and Reverse Bias to Collector-Base junction ( $J_2$ ) using a single DC source.
- To provide a stable operating point “Q” at a suitable position in the Active Region of the Output Characteristics of a transistor.
- To ensure operating stability of the transistor w.r.t. temperature variations by providing a suitable value of “Stability Factor”.

### Thermal instability of operation, Thermal Runaway and Stability Factor

- ❖ In explaining Transistor Action in terms of Energy Band Theory it was explained that the process results in the release of Heat Energy from the reverse biased Collector-Base junction. Diagram is repeated



- The expression for collector current of a transistor given by Eq.-7, in section-1

$$I_C = \beta I_B + (1 + \beta) I_{CO}$$

The quantity  $I_{CO}$  is the Temperature Dependent, minority carrier current of the depletion region of the C-B Junction. The generation of minority carriers is governed by the Intrinsic Rule, such that for every increase in temperature by  $10^\circ C$ , the minority carrier current increases by a factor of 2.

- Due to the heat released in the C-B Junction (Shown in figure), the temperature rises, thereby increasing the value of  $I_{CO}$ . Due to a certain amount of increase in  $I_{CO}$ , the net collector current  $I_C$  increases by a factor  $1 + \beta$ . Since the  $\beta$  of a transistor is a large real value, the increase in collector current will be significant.
- A large amount of collector current flowing down the Energy Hill results in the increase of junction temperature. This will in turn result in a larger value of  $I_{CO}$ , and thus the **collector current will go on increasing cumulatively**.
- This exponential increase in  $I_C$  accompanied by the increase of junction temperature will ultimately lead to the permanent damage of the transistor. This situation is known as **Thermal Runaway**.

**A very important function of the biasing circuit of a transistor is to provide Thermal Stability of operation and prevent Thermal Runaway.**

**Stability Factor 'S'**

Stability Factor of a transistor biasing circuit is defined as the “Rate of change of  $I_C$  with respect to change in  $I_{CO}$ .”

$$S = \frac{dI_C}{dI_{CO}}$$

Taking the first derivative of equation-7, given above, for  $I_C$  w.r.t.  $I_{CO}$ ,

$$1 = \beta \frac{dI_B}{dI_C} + (1 + \beta) \frac{dI_{CO}}{dI_C}$$

$$\beta \frac{dI_B}{dI_C} + (1 + \beta) \frac{1}{S} = 1$$

$$\therefore S = \frac{(1+\beta)}{\left(1-\beta \frac{dI_B}{dI_C}\right)} \quad \underline{\dots\dots\dots}(9)$$

**This expression is the General Equation of “Stability Factor” of a Transistor Biasing Circuit.**

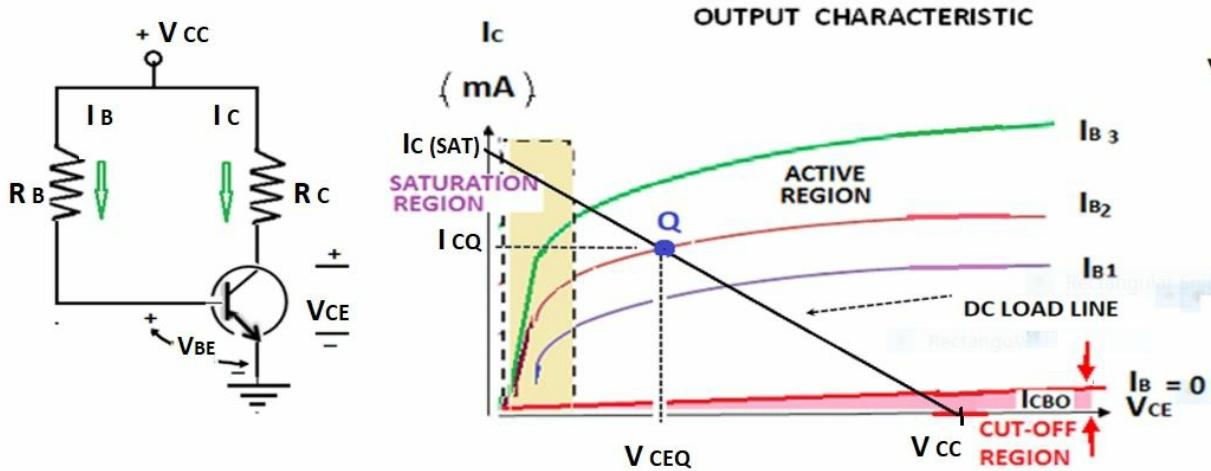
**The goal of a biasing circuit is to provide a value of Stability Factor ‘S’, as nearly equal to unity as possible.**

### VARIOUS COMMON BIASING CIRCUITS

#### 1. Base Bias Circuit or Fixed Bias Circuit

This is one of the simplest biasing circuits.

- The Biasing DC Battery of  $+V_{CC}$  is connected at the Collector of the NPN transistor. Since the Emitter is at a ground potential, it is relatively negative w.r.t. Therefore, the Emitter-Base junction is forward biased and the Collector-Base junction is reverse biased.



**Fig. 16:** - Fixed Bias Circuit or The Base Bias Circuit and it's Load Line.

- Since the Emitter-Base junction is forward biased, a potential  $V_{BE}$  appears, with the polarity as shown in the figure. For proper bias, the magnitude of  $V_{BE}$  must be greater than or equal to the Cut-in-Voltage  $V_Y$  of the transistor. (**In case of Si  $V_{BE} = 0.7$  v and in case of Ge ,  $V_{BE} = 0.3$  V** ).
- This condition is set up by calculating the correct value for the resistance  $R_B$ .
- Again, the transistor must be operating somewhere in the Active Region of it's characteristic, say at the point 'Q' as shown in the figure. In order to ensure this, the value of  $R_C$  is to be calculated correctly.

### Design

1. A Load-Line is drawn superimposed over the Output Characteristic of the transistor. The Q Point is selected at a location within the Active Region. The co-ordinates of the Q Point are  $V_{CEQ}$  and  $I_{CQ}$  respectively. Accordingly, we can calculate  $R_C$  as

$$R_C = \frac{(V_{CC} - V_{CEQ})}{I_{CQ}} \quad \dots(10)$$

2. The value of  $R_B$  is calculated as follows, with,

$$R_B = \frac{(V_{CC} - V_{BE})}{I_{BQ}} \quad \text{where,} \quad I_{BQ} = \frac{I_{CQ}}{\beta} \quad \& \quad V_{BE} = V_Y$$

$$\therefore I_B = \frac{(V_{CC} - V_Y)}{R_B} \quad \dots(11)$$

**Since  $V_Y$  is a constant for a P-N junction, and since biasing potential  $V_{CC}$  is a DC (constant), the Base Current  $I_B$  is ‘Fixed’ by the resistor  $R_B$ . Hence the name ‘Fixed Bias Circuit’.**

### Load Line Equation

- The Load Line is defined as the locus of the plot between Collector Current  $I_C$  (Load Current) and the Collector voltage  $V_{CE}$  (Voltage across the Load), that are set-up by the biasing circuit.
- In the graph above,  $V_{CE}$  is the independent variable and  $I_C$  is the dependent variable. The Kirchhoff’s Voltage Law (KVL) equation of the Collector-Emitter circuit is given by

$$V_{CC} = I_C R_C + V_{CE}$$

Rearranging we have

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} \quad \dots(12)$$

**This expression is the Load Line Equation, since it describes the variation of the Load Current  $I_C$  (Dependent Variable) as a function of the Load Voltage  $V_{CE}$  (Independent Variable).**

- This is the equation of a straight line; the vertical intercept is  $\frac{V_{CC}}{R_C}$  and the slope is  $(-\frac{1}{R_C})$ . (Load Line has a **negative slope**).

### Operating Point or Quiescent Point ‘Q’

- When the transistor is “Active biased”, and when Signal Source is not connected, a DC current  $I_{CQ}$  flows in the Collector terminal

and a DC voltage,  $V_{CEQ}$  appears between the Collector and the Emitter terminals.

- The point ‘Q’ on the Load Line, whose x-coordinate is  $V_{CEQ}$  and y-coordinate is  $I_{CQ}$  is known as the ‘**Operating Point**’ or ‘**Quiescent Point**’ of the circuit. The meaning of the word **Quiescence is Silence**.
- The transistor amplifier is just ‘Sitting’ silently, at the Q Point and is at the ready to get into the action of amplifying as soon as an input signal is applied.

### **Procedure to Sketch Load Line –**

The procedure to sketch the Load line is as follows.

1. The Load Line Equation, Eq. (12) is an equation of a Straight Line. To “plot” a Straight Line, we just **need to find two points** on the locus of the line defining it, and join them and extrapolate, as necessary.
2. In order to obtain the vertical intercept, put  $V_{CE} = 0$  in the expression for Load Line (Eq. 12). Under this condition the transistor is operating in the Saturation Region. Therefore, we obtain a current defined as  $I_{C(SAT)}$ .

$$I_C = I_{C(SAT)} = \frac{V_{CC}}{R_C}$$

- iii. In order to obtain the horizontal intercept, put  $I_C = 0$  in the Load Line. Under this condition the transistor is operating in the Cut-Off Region

$$\begin{aligned} \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} &= 0 \\ \frac{V_{CC}}{R_C} - \frac{V_{CE(CUT-OFF)}}{R_C} &= 0 \\ \therefore V_{CE(CUT-OFF)} &= V_{CC} \end{aligned}$$

3. Now, when we join these two points  $I_{C(Sat)}$  and  $V_{CE(CUT-OFF)}$ ,

we obtain the Load Line.

### Stability Factor

Stability Factor is given by the Eq. 9 above as-

$$S = \frac{(1 + \beta)}{\left(1 - \frac{dI_B}{dI_C}\right)}$$

The quantity  $\frac{dI_B}{dI_C}$  for the biasing circuit is to be obtained and

substituted in the expression for S.

We had

$$I_B = \frac{(V_{CC} - V_Y)}{R_B} \quad \& \quad I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$$

From these two expressions we find that  $I_B$  and  $I_C$  are independent of each other

$$\therefore \frac{dI_B}{dI_C} = 0$$

Substituting this in Eq. 9 we get

$$S = (1 + \beta) \quad \dots(13)$$

### TUTORIAL-1 (A)

**Example - 1:** - In the Fixed Bias circuit in the figure, the circuit uses a Si NPN transistor, which has a value of  $\beta = 90$ . Sketch the DC Load Line and locate the Q-Point. Calculate Stability Factor and comment.

Load Line equation is given by Eq. 12 as

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$$

This is the equation of a straight line. Hence it can be sketched by locating the Vertical Intercept and the Horizontal Intercept, and thereafter joining these two points.

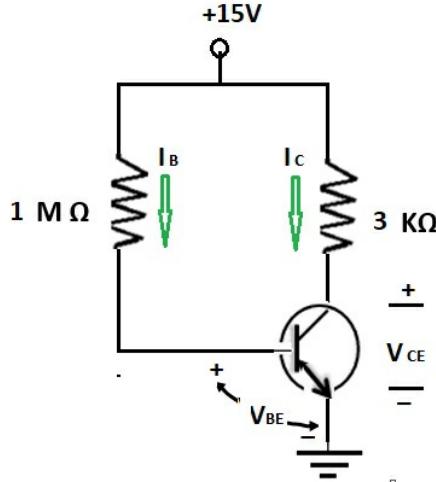
Putting  $V_{CE} = 0$  we get the Vertical Intercept as

$$I_C = I_{C(Sat)} = \frac{V_{CC}}{R_C} = \frac{15V}{3K\Omega}$$

$$\begin{aligned} I_{C(Sat)} &= 15 / 3000 \\ &= 5 \times 10^{-3} A = 5 mA \end{aligned}$$

Putting  $I_C = 0$  we get the Horizontal Intercept as

$$V_{CE(CUT-OFF)} = V_{CC} = 15 \text{ V}$$



#### Location of Q-Point :-

From Eq. 11 we have (Since we have a Si transistor, assume  $V_{BEQ} = V_Y = 0.6 \text{ V}$ ).

$$R_B = \frac{(V_{CC} - V_Y)}{I_{BQ}}$$

$$\therefore I_{BQ} = \frac{(V_{CC} - V_{BEQ})}{R_B} = \frac{15 - 0.6}{1 \times 10^6} = 14.4 \times 10^{-6} \text{ A} = 14.4 \mu\text{A}$$

$$\therefore I_{CQ} = \beta I_{BQ} = 90 \times 14.4 \times 10^{-6}$$

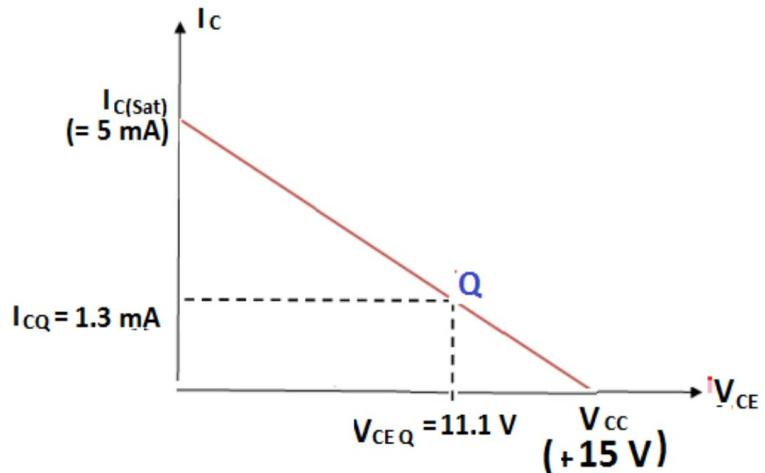
$$= 1.296 \times 10^{-3} \text{ A} \cong 1.3 \text{ mA}$$

From the Load Line equation, Eq. 12 we have

$$V_{CEQ} = V_{CC} - I_{CQ} R_C$$

$$\text{Substituting, } V_{CEQ} = 15 - 1.3 \times 10^{-3} \times 3 \times 10^3 = 11.1 \text{ V}$$

The Load Line is sketched and the Q-Point is placed upon it using the co-ordinates, ( $V_{CEQ}$ :  $I_{CQ}$ )



Stability Factor 'S' :-- From Eq. 13 Stability Factor of this circuit is  
 $S = (1 + \beta) = 91$

**COMMENT:**-- The value of S is quite high. The quantity S denotes the rate of change of  $I_C$  w.r.t.  $I_{CO}$ . Hence a certain change in the value of  $I_{CO}$  will result in a change of 91 times in  $I_C$ . Thus stability of operation is rather poor.

## 2. Collector Feed-Back Bias Circuit

**Stability Factor :-** The KVL equation of the Collector-Base loop  
 $V_{CC} = (I_C + I_B) R_C + I_B R_B + V_{BE}$

In this we can neglect  $V_{BE}$  w.r.t.  $V_{CC}$  and simplify as

$$V_{CC} = I_C R_C + I_B (R_C + R_B)$$

$$\therefore I_B = \frac{(V_{CC} - I_C R_C)}{(R_C + R_B)}$$

Partially differentiating this expression w.r.t.  $I_C$  and substituting g in Eq-9 we have

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{(R_C + R_B)}$$

And

$$S = \frac{(1+\beta)}{\left(1+\beta \frac{R_C}{(R_C+R_B)}\right)}$$

In this expression, the ratio  $\frac{R_C}{R_B + R_C} < 1$

$$\therefore S < (1 + \beta)$$

**COMMENT:** - The Stability Factor for the Collector Feed-Back Bias circuit is lesser than that of the Fixed Bias circuit. In other words, this circuit provides better thermal stability of operation compared to the Fixed Bias circuit.

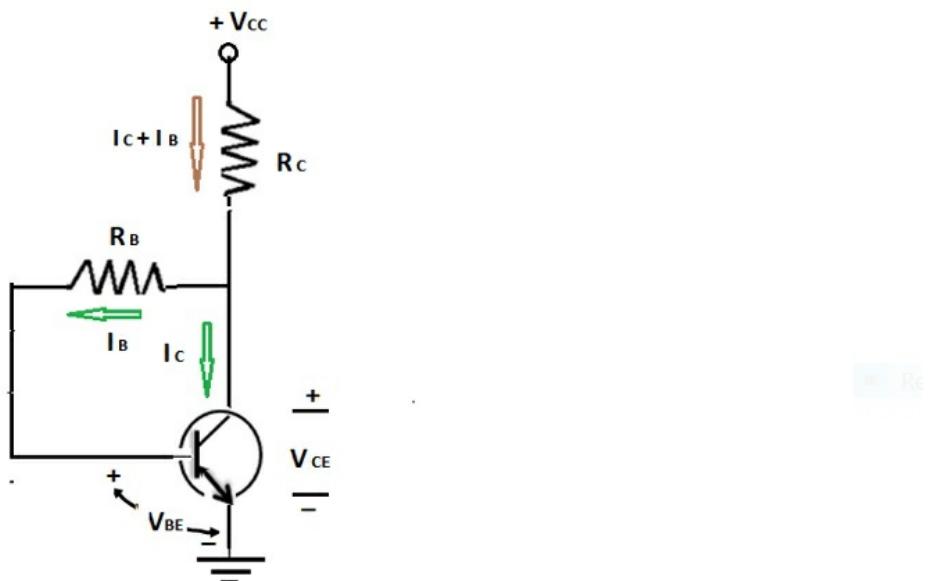


Fig. 17-

**Load Line Equation :-** The KVL equation of the Collector –Emitter circuit is given by

$$V_{CC} = (I_C + I_B) R_C + V_{CE}$$

Since  $I_B \ll I_C$ , we can neglect this term and rearrange the equation as

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} \quad \dots (15)$$

**This is the same expression as the Load Line equation of the Fixed bias circuit, described in the previous section. The same procedure as explained above can be adopted to plot the Load Line as in the previous section.**

### Design Procedure

The design procedure to ensure that the Q-point should lie in the middle of the Load Line is as follows. --

The maximum collector current is  $I_{C(sat)}$ ,

$$\begin{aligned} I_{C(SAT)} &= \frac{V_{CC}}{R_C} \\ \therefore I_{CQ} &= \frac{1}{2} I_{C(SAT)} = \frac{V_{CC}}{2 R_C} \end{aligned} \quad (A)$$

The KVL equation of the Base Loop is  $I_B R_B + V_{BE} = V_{CE}$

Here

$$\begin{aligned} I_B &= \frac{I_C}{\beta} \\ \therefore V_{CE} &= \frac{I_C}{\beta} R_B + V_{BE} \end{aligned} \quad (B)$$

Again, from Load Line equation we have

$$V_{CE} = V_{CC} - I_C R_C \quad \dots (C)$$

Equating B & C and neglecting  $V_{BE}$  we have

$$\begin{aligned}\frac{I_C}{\beta} R_B &= V_{CC} - I_C R_C \\ \therefore V_{CC} &= \left\{ \frac{R_B}{\beta} + R_C \right\} I_C \\ \therefore I_C &= I_{CQ} = \frac{V_{CC}}{\left\{ \frac{R_B}{\beta} + R_C \right\}}\end{aligned}\quad \underline{\dots}(D)$$

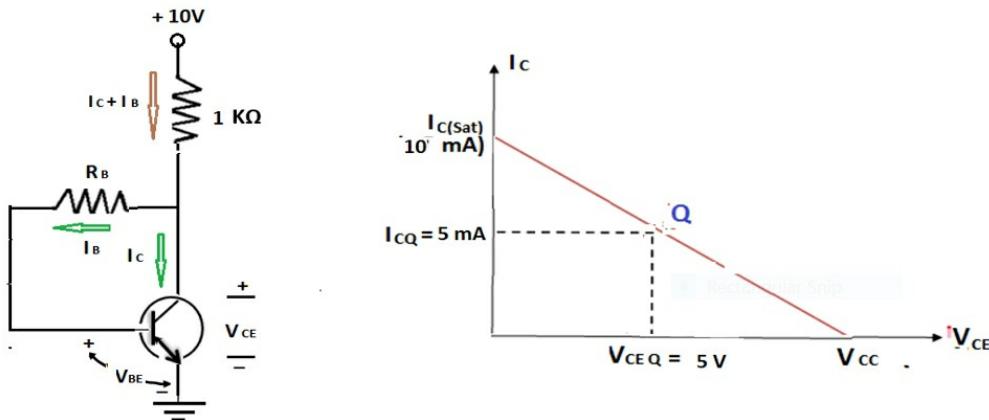
Now equating A & D and simplifying we have

$$\begin{aligned}\frac{R_B}{\beta} + R_C &= 2 R_C \\ \therefore R_C &= \frac{R_B}{\beta}\end{aligned}\quad \underline{\dots}(16)$$

Thus, the condition for placing the Q-Point in the middle of the Load Line is that the circuit must use a value of  $R_C$  given by the Eq. 16.

### TUTORIAL-1 (B)

**Example - 2:** - The circuit uses the same transistor as that given in Example – 1. The collector resistance is  $R_C = 1 K$ . Sketch the Load Line and calculate  $R_B$  so that the Q-Point is in the middle of the Load Line. Calculate S and compare with that of the Fixed Bias circuit.



### SOLUTION :-

From the Load Line equation, Eq. 15, and from the given circuit diagram, we have

$$I_{C(Sat)} = \frac{V_{CC}}{R_C} = \frac{10 V}{1 K} = 10 \text{ mA AND } V_{CC} = 10 \text{ V}$$

Joining these two points, we get the Load Line.

The Q Point is required to be in the middle of the Load Line. Hence, we have

$$\mid I_{CQ} = 5 \text{ mA AND } V_{CEQ} = 5 \text{ V}$$

The condition for placing the Q Point in the middle of the Load Line is given by Eq. 16 as

$$R_C = \frac{R_B}{\beta} \quad \therefore R_B = \beta R_C$$

Given that  $\beta$  of the transistor is 90 (Refer to Ex- 5.1)

$$\therefore R_B = 90 \text{ K}$$

The expression for Stability Factor of the Collector Feed-Back Bias circuit is given by Eq. 14 as

$$S = \frac{(1 + \beta)}{1 + \beta \left( \frac{R_C}{R_B + R_C} \right)}$$

Substituting the given and calculated values in this we have

$$S = \frac{(1 + 90)}{1 + 90 \times \frac{1000}{90000 + 1000}} = 45.75 \approx 46$$

**Lesser value of “S” in Collector Feedback Bias Circuit as compared to Fixed Bias Circuit, for the same transistor.**

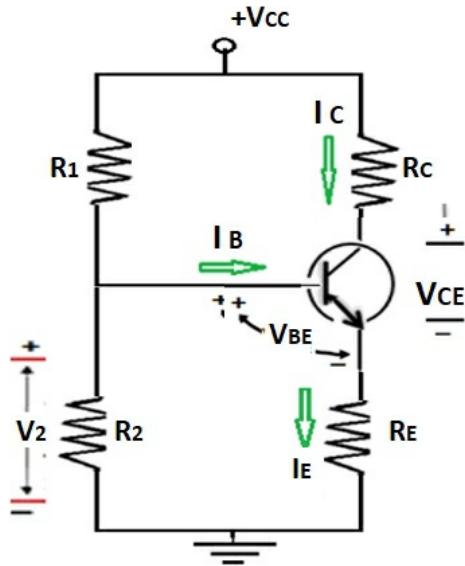
### 3. Voltage Divider Bias Circuit or Self Bias Circuit OR Universal Biasing Circuit

The Voltage Divider Bias circuit is a better circuit in providing better thermal stability. This circuit also provides some other advantages, as follows. Hence this circuit is universally used for amplifier applications in any of the transistors and in any of the configurations.

- Stability Factor can be chosen at any desired value.
- Performance is independent of the load resistance  $R_C$ . Hence all

types of load as well as all types of coupling circuits can use this biasing circuit.

- Impedance matching of both source and load is possible.
- Transistor replacement is possible without changing the other circuit components.



**Fig.- 18**

### WORKING PRINCIPLE :-

- ✓ For Active Bias on a transistor **(i) The Base-Emitter junction must be forward biased and (ii) The Collector-Base junction must be reverse biased.**
- ✓ In part-A of the Fig.- 19, the two resistances  $R_1$  and  $R_2$  in the Base circuit constitute a Voltage Divider network. Voltage  $V_2$ , developed across  $R_2$ , is given by the Voltage Divider Rule, as

$$V_2 = \frac{V_{CC} \cdot R_2}{(R_1 + R_2)} \quad \underline{\dots(17)}$$

This voltage must be greater than the Cut-In voltage  $V_Y$  of the base emitter junction, i.e.,

$$V_{BE} \geq V_Y. \quad (V_Y \text{ for Si} = 0.7 \text{ V}).$$

**When this condition is satisfied, the Base-Emitter junction is forward biased.**

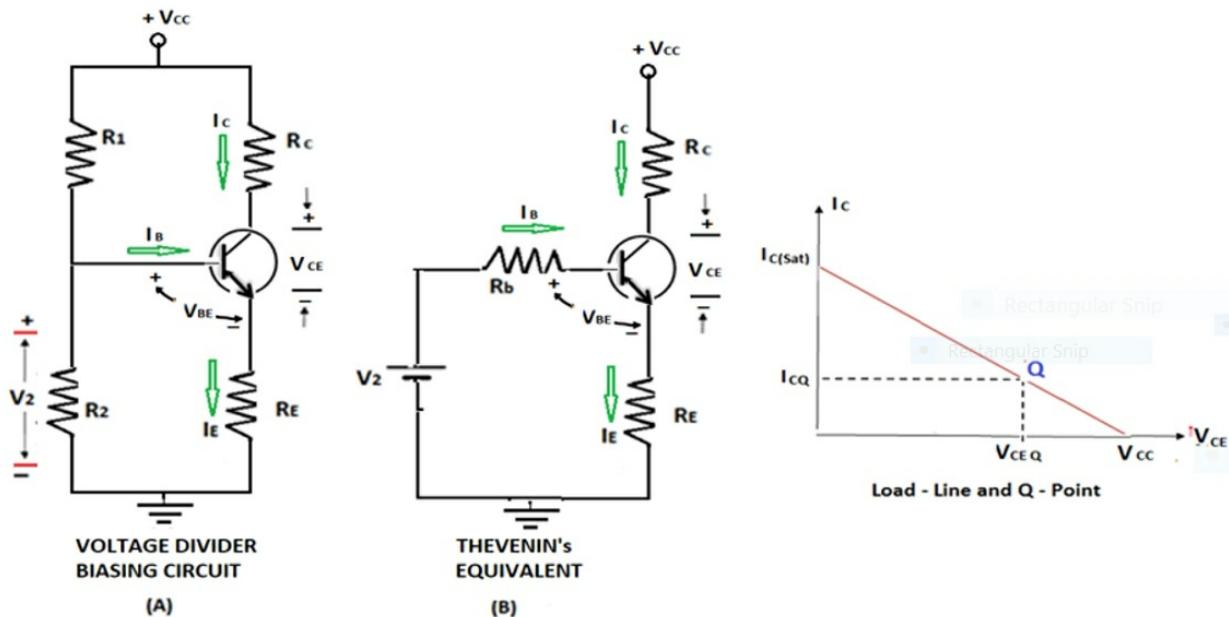
In the Collector-Emitter loop  $I_C \approx I_E$ . Hence it can be assumed that the same current flows through the two series resistances  $R_C$  and  $R_E$ . The voltage dropped in these two resistances must be such that the voltage  $V_{CE}$ , remaining across the Collector and Emitter terminals is greater than the voltage  $V_{CE(SAT)}$  of the transistor. **When this condition is met the Collector-Base junction is reverse biased.**

#### ANALYSIS :-

- ❖ Thevenizing the Base-Emitter loop of the circuit (A), we get the circuit (B).
- ❖ In this the Thevenin's Equivalent Voltage is  $V_{Th} = V_2$  and the Thevenin's Equivalent resistance is  $R_{Th} = R_b$

Where,  $R_b$  is the parallel combination of  $R_1$  and  $R_2$ ,

$$R_b = R_1 \parallel R_2 = \frac{R_1 R_2}{(R_1 + R_2)} \quad \dots(18)$$



#### 5.7 Stability Factor :-

The Kirchhoff's Voltage Law equation of the Base Emitter loop in the part (B) of the figure is

$$V_2 = I_B R_b + V_{BE} + I_E R_E$$

Where

$$I_E = I_C + I_B.$$

Substituting and neglecting  $V_{BE}$  (since  $V_{BE} \ll V_2$ ) and simplifying,

$$V_2 = I_B (R_b + R_E) + I_C R_E$$

Or

$$I_B = \frac{V_2}{(R_b + R_E)} - \frac{I_C \cdot R_E}{(R_b + R_E)}$$

Now, taking partial derivative of this expression w.r.t.  $I_{CO}$  we get

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_b + R_E}$$

Substituting this in the general expression for Stability Factor 'S' we have

$$S = \frac{(1 + \beta)}{\left\{ 1 + \beta \left( \frac{R_E}{R_b + R_E} \right) \right\}}$$

$$\underline{S} = \frac{(1 + \beta)(R_b + R_E)}{R_b + R_E + \beta R_E}$$

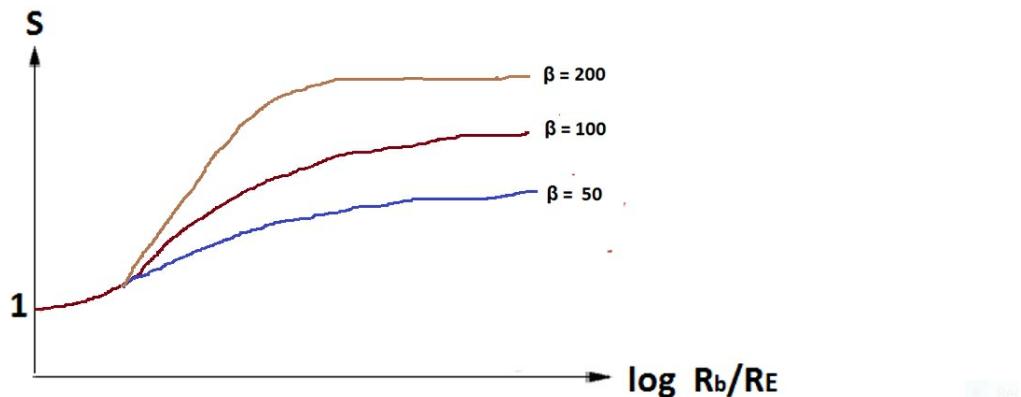
Dividing throughout by  $R_E$  and simplifying and rearranging we get the final expression for Stability Factor as

$$S = \frac{(1+\beta)[1 + (\frac{R_b}{R_E})]}{1 + \beta + (\frac{R_b}{R_E})} \quad \dots(19)$$

When the ratio  $R_b/R_E$  tends to zero, the Stability Factor S tends to Unity.

Since S represents the rate of change of  $I_C$  w.r.t.  $I_{CO}$ , the situation when  $S \rightarrow 1$  represents the situation where there is no change in the value of  $I_C$  w.r.t.  $I_{CO}$ . In other words, **this is the most stable operation of the transistor.**

If we plot a graph of variation of S as a function of the ratio  $R_b/R_E$  we get the following as shown in Fig.20.



**Fig. 19.**

From the figure above the following observations can be made –

1. The value of Stability Factor ‘S’ tends to be Unity when the value of the ratio  $R_b/R_E$  tends to be zero.
2. When the ratio  $R_b/R_E$  tends to be zero, the Stability Factor ‘S’ tends to be independent of the value of  $\beta$ .

### LOAD LINE EQUATION :-

From the Part(B) of Fig.-19 we have the KVL equation of the Collector-Emitter Loop

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

Assuming  $I_C \approx I_E$  and rearranging we get the equation of  $I_C$  as a function of  $V_{CE}$ .

$$I_C = \frac{V_{CC}}{(R_C + R_E)} - \frac{V_{CE}}{(R_C + R_E)} \quad \dots(20)$$

### This is the Load Line Equation.

The following points are to be noted from this expression.

1. This is a first order equation of the variable  $V_{CE}$ . Hence this is the equation of a straight line.
2. The first term is a constant. Hence it represents the ‘Vertical Intercept’ of the straight line.
3. The straight line has a negative slope of  $-\frac{1}{(R_C + R_E)}$ .
4. Since the plot of the Eq. 20 has a slope proportional to the DC Load Resistance of the circuit, hence the straight line is called the DC Load Line.

### Plotting of dc load line: -

- a) For locating the Vertical intercept, substitute  $V_{CE} = 0$  in the Load line equation

$$I_{C(SAT)} = \frac{V_{CC}}{(R_C + R_E)} \quad \dots(21)$$

For Horizontal intercept substitute  $I_C = 0$  in the Load line equation

$$V_{CE(CUT-OFF)} = V_{CC}$$

These two points are joined with a straight line. This is the plot of the DC Load Line.

### Location of Q-point: -

- ✓ The Operating Point or Q-Point is located within the Active Region, on the DC Load Line.
- ✓ From the circuit in part (B) of Fig.-19 we get

$$V_2 = I_B R_b + V_{BE} + I_E R_E$$

Where  $I_E = I_B + I_C$   
and  $I_C = \beta I_B$

$$\therefore V_2 = V_{BE} + \{R_b + (1 + \beta)R_E\} I_B$$

$$\therefore I_B = I_{BQ} = \frac{(V_2 - V_{BE})}{\{R_b + (1 + \beta)R_E\}} \quad \underline{\dots(22)}$$

From this we get

$$I_{CQ} = \beta I_B$$

Substituting in the Load Line equation and rearranging we get

$$V_{CEQ} = V_{CC} - I_C (R_C + R_E)$$

**The point Q described by the co-ordinates ( $I_{CQ}$  :  $V_{CEQ}$ ) is the Operating Point or Bias Point of the circuit.**

### UNIVERSALITY OF THE VOLTAGE DIVIDER BIASING CIRCUIT

The Voltage Divider Biasing circuit is universally applicable for a variety of applications. This is applicable to BJTs as well as FETs. The following are the salient features of the circuit that make it universally applicable.

- Stability Factor can be chosen at any desired value.
- Performance is independent of the load resistance  $R_C$ . Hence all types of load as well as all types of coupling circuits can use this biasing circuit.
- Impedance matching of both source and load is possible.
- Transistor replacement is possible without changing the other circuit components.

### TUTORIAL -2 (A)

**Example 3:** - The transistor used in the circuit below is made of Si and has a  $\beta = 200$ . Plot the DC Load Line and locate the Q-Point. Also calculate Stability Factor.

**SOLUTION:** - Substituting the appropriate values of  $R_2$ ,  $R_1$  and  $V_{CC}$  the Eq. 17, 18 and 21, we get

$$V_2 = \frac{22 \times 15}{68+22} = 3.67 \text{ V} \quad R_b = \frac{68 \times 22}{68+22} = 16.62 \text{ K} \quad I_{C(\text{sat})} = \frac{15}{(5.6+12.2)} = 0.843 \text{ mA}$$

Joining  $I_{C(\text{sat})}$  and  $V_{CC}$  we get the DC Load Line.

Substituting appropriate values in the Eq. 22, and using  $V_{BE} = 0.7 \text{ V}$  for Si and  $\beta=200$ , we get

$$I_{BQ} = \frac{3.67 - 0.7}{16.62 + (200+1) \cdot 12.2} = 0.00124 \text{ mA}$$

$$\therefore I_{CQ} = \beta I_{BQ} = 200 \times 0.00124 = 0.248 \text{ mA}$$

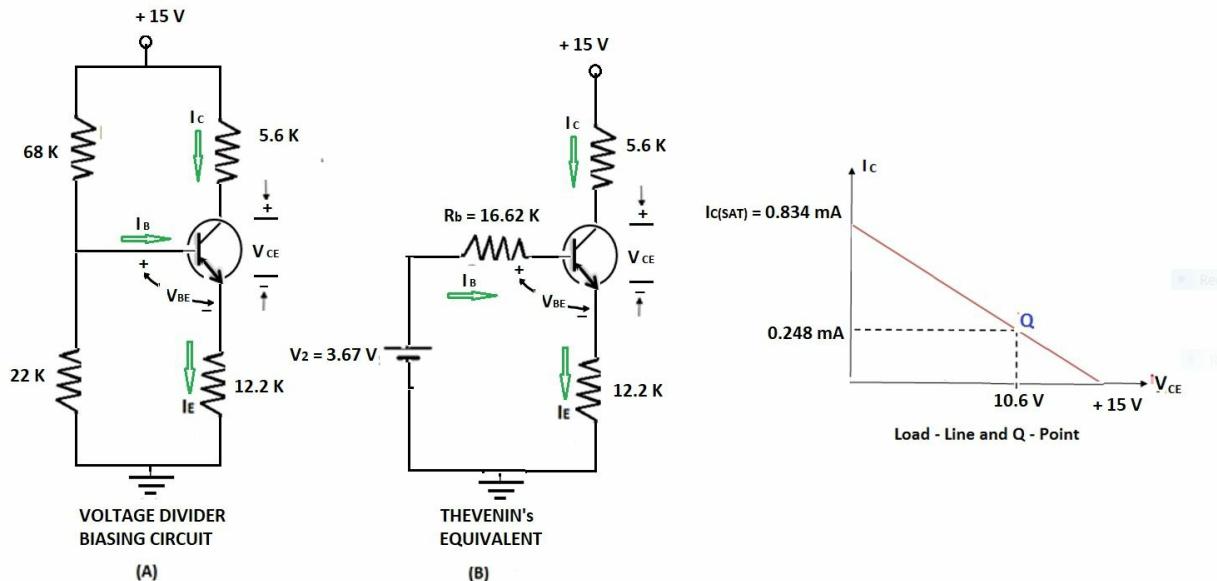
Rearranging the Load Line equation (Eq. 21) and substituting we get

$$V_{CEQ} = V_{CC} - I_{CQ} (R_E + R_C) \\ = 15 - 0.248 \times (12.2 + 5.6) = 10.6 \text{ V}$$

The Co-ordinates of the Q-Point are  $V_{CEQ}$  and  $I_{CQ}$ . Using the numerical values we can plot the Q-Point.

Substituting the appropriate numerical values in the Eq. 4.20 we get the value of the Stability Factor as

$$S = \frac{(1+200)(1+16.6/12.2)}{1+200+16.6/12.2} = 2.33$$



If we compare the value of S for the Voltage Divider Bias Circuit with that of the others, we observe that the Voltage Divider Bias Circuit provides much better stability.

## **TUTORIAL -2 (B)**

**Example 4 (Design Problem) :-** Design a Voltage Divider Biasing Circuit for a Si PNP transistor with  $\beta = 50$ , so that it can drive a load of  $R_C = 5.6 \text{ K}$  at the collector, with a Stability Factor of  $S \leq 3$ . The transistor is to be biased at  $I_{CQ} = 1.5 \text{ mA}$ ;  $V_{CEQ} = 11.5 \text{ V}$ , using a DC biasing source  $V_{CC} = 22 \text{ V}$ .

**SOLUTION:** - From the Load Line equation of Eq. 19 , which can be reproduced as follows, and by substituting the numerical values from the given data we get -

$$I_{CQ} = \frac{(V_{CC} - V_{CEQ})}{(R_C + R_E)}$$

  $\therefore (R_C + R_E) = \frac{(V_{CC} - V_{CEQ})}{I_{CQ}}$

$$= \frac{(22 - 11.5)}{1.5} = 7 \text{ K}$$

$$\therefore R_E = 7 - 5.6 = 1.4 \text{ K}$$

Assuming the Worst Case Scenario of  $S = 3$ , and rearranging the Stability Factor equation of Eq.-20, and substituting the appropriate numerical values we get –

$$S = \frac{(1 + \beta)[1 + (R_b/R_E)]}{1 + \beta + (R_b/R_E)}$$

$$\therefore \frac{R_B}{R_E} = \frac{(S-1).(1+\beta)}{(1+\beta-S)}$$

$$= \frac{(3-1)(1+50)}{1+50-3} = 2.1$$

Since  $R_E = 1.4 \text{ K}$

  $\therefore R_b = 2.1 \times 1.4 = 2.96 \text{ K}$ .

We had the KVL equation of the Emitter –Base loop as  
 $V_2 = I_{BQ} R_b + V_{BE} + (I_{CQ} + I_{BQ}) R_E$   
where  $I_{BQ} = I_{CQ} / \beta = 1.5 / 50 = 0.03 \text{ mA}$ . and  $V_{BE} = 0.7 \text{ V}$  for a Si transistor.

Substituting we get  
 $V_2 = 0.03 \times 2.96 + 0.7 + (1.5 + 0.03) \times 1.4 = 2.93 \text{ V.}$

We had the expressions for  $V_2$  and  $R_b$  given by Eq. 4.17 and Eq. 18 as

$$V_2 = \frac{R_2 V_{CC}}{(R_1 + R_2)} \quad \& \quad R_b = \frac{R_1 R_2}{(R_1 + R_2)}$$

Rearranging and substituting

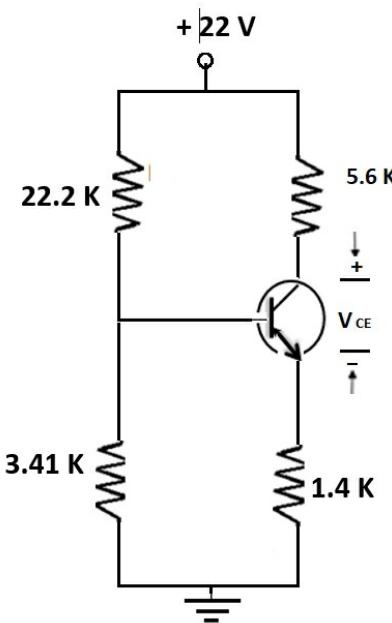
$$V_2 = \frac{R_b}{R_1} V_{CC} \quad \& \quad R_2 = \frac{R_1 V_2}{(V_{CC} - V_2)}$$

$$\therefore R_1 = \frac{R_b}{V_2} V_{CC} \\ = \frac{2.96}{2.93} \times 22 = 22.2 \text{ K}$$

&

$$R_2 = \frac{22.2 \times 2.93}{22 - 2.93} = 3.41 \text{ K}$$

Since we have calculated the unknown values of the resistances  $R_1$ ,  $R_2$  and  $R_E$ , the design is completed.



## 5.8 Prevention of Thermal Runaway

### by Heat Sink

We discussed the phenomenon of Thermal Runaway in an earlier section. It was mentioned that this has to be avoided in a transistor amplifier. One of the desired functions of a Biasing Circuit is to provide as low a value of Stability Factor so that the ‘Rate of change of  $I_C$  w.r.t.  $I_{CO}$ ’ remains at as low a value as possible. The Voltage Divider Biasing circuit has been found to be most suitable in this regard. However, in case of Power Amplifiers, which work at high values of Collector Current  $I_C$ , the transistor has a high probability of going into the Thermal Runaway mode. This undesirable phenomenon has to be prevented by a mechanical means.

For this purpose, the transistor of a power amplifier is mounted on a structure made of a metal. Sometimes the transistor may also be encapsulated with a metal casing. Metals are good thermal conductors as well as thermal radiators. Thus, the internal heat generated in the transistor is easily transferred to the metal strip. Often this heat is dissipated by radiation. In certain cases, a small electric fan is often provided in electronic gadgets for the purpose of dissipation of heat. Such a metal mountings or encasings are called ‘Heat Sink’ (Fig. - 21).



**Fig. –20 :-** Heat Sink is a metal structure. Transistors are often mounted on Heat Sink in order to dissipate the internally generated heat in order to prevent Thermal Runaway.

!!!!!! BJT – BJT ~ BJT !!!!!!!

# **CHAPTER – VI**

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## **SMALL SIGNAL AMPLIFIERS**

### *SMALL SIGNAL BJT AMPLIFIERS*

#### **INTRODUCTION**

Amplifiers are required to amplify a wide variety of signals in practice.

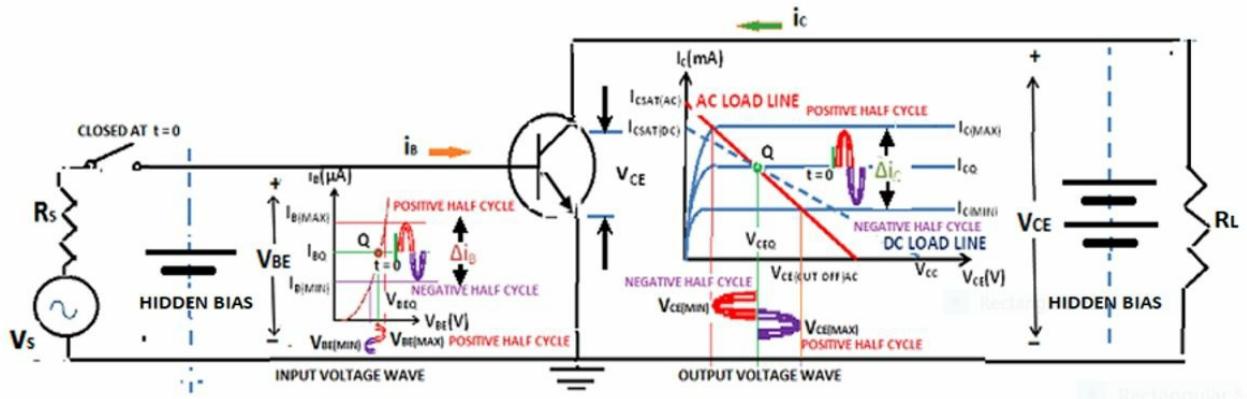
In an auditorium, the music performed on the stage is to be amplified so as to be audible to a large audience seated in a large hall. Signals received by a variety of communication equipment from far away sources are very weak and need to be amplified before processing. Electronic control devices such as Computer and Microprocessors produce output signals with electrical power levels of a few milli Watts. These have to be used for controlling and monitoring heavy industrial plants. For this purpose, the output signal of the computer needs to be sufficiently amplified so as to be compatible with the high-power levels at which the industrial plants work.

In practice, the signals applied to the amplifiers are AC signals. Thus, in the circuit diagrams used in the text books use a AC signal source at the input end. The amplified power is shown to be delivered to a purely resistive load.

#### **6.1BJT Amplifier**

A BJT will work as an amplifier only when it biased in the Active Region of its characteristic. The Biasing Circuit places the

**Operating Point, “Q”** on the Load Line such that an amount current “ $I_C$ ” flows through the collector, and the voltage between the collector terminal and ground is “ $V_{CEQ}$ ”. Once the transistor is properly biased, it can amplify an input signal. The concept of this process is depicted in the diagram in the Fig.-1. This shows the currents and the voltages at the Input and Output terminals, in relation to the Input and Output characteristics of a transistor. The transistor is shown in the CE configuration. It will be shown later that **the CE configuration is the most suitable configuration for a transistor amplifier.**



**Fig. - 1**

- ❖ The “Input Characteristics” of the transistor is reproduced at the “Input Point” in the Fig. (1). This shows the variation of the Input Current (Base Current  $i_B$ ) w.r.t. the Input Voltage ( $v_{BE}$ ).
- ❖ Similarly, the “Output Characteristics” of the transistor, showing variation of the Output Current (Collector Current  $i_C$ ) w.r.t. the Output Voltage ( $v_{CE}$ ) is shown in the “Output Loop”.
- ❖ When the Signal Source is Open Circuited, the currents and the voltages in the circuit are only due to the DC Bias. At the input characteristics, the Q-Point is at  $V_{BEQ}$  and  $I_{BQ}$ . And the Q-Point at the output characteristics is at  $V_{CEQ}$  and  $I_{CQ}$ .
- ❖ When the AC signal is applied (at “ $t = 0$ ”), it is superimposed over the DC Biasing voltage  $V_{BEQ}$ . In the positive half cycle, the net Input Voltage “ $v_{BE}$ ” increases sinusoidally and reaches the peak value  $V_{BE(MAX)}$ , and in the negative half cycle, it decreases and

reaches  $V_{BE(MIN)}$ . Similarly, the sinusoidal oscillation of net Input Current “ $i_B$ ” is also sinusoidal between  $I_{B(MAX)}$  and  $I_{B(MIN)}$ .

- ❖ The output current and voltage variation is determined by two graphs, (a) The Output Characteristics and (b) The Load Line. The Majority Carrier Collector Current is independent of the Collector Voltage, and is given by

$$I_C = \beta I_B$$

Thus, as the Input Current oscillates between  $I_{B(MAX)}$  and  $I_{B(MIN)}$  the Output Current will also oscillate between  $I_{C(MAX)}$  and  $I_{C(MIN)}$ . This oscillation must be along the Load Line. Since the Load Line has a Negative Slope, the Output Voltage “ $V_{CE}$ ” will **decrease** when “ $i_C$ ” is increasing (in the positive half cycle) and “ $V_{CE}$ ” will **increase** when “ $i_C$ ” is in the negative half cycle).

- ❖ A Very Important Observation is to be made from the figure above.

**“When the input voltage “ $v_{BE}$ ” is in the Positive Half Cycle, the output voltage “ $v_{CE}$ ” is in the Negative Half Cycle, and vice – versa”. This means that the Output Voltage is  $180^0$  ( $\pi$  radian) OUT OF PHASE w.r.t. the Input Voltage. In other words, the CE configuration of amplifier introduces a PHASE REVERSAL between Input & Output voltages.**

- ❖ In order to calculate these currents and voltages in the amplifier, the amplifier circuit has to be analyzed. For the purpose of analysis, the Semiconductor Crystal of the PNP or NPN form has to be replaced by a “Model”, and this “Model” must consist of Electrical Circuit Elements, namely, Passive elements and Active Elements.

### The Small Signal Models of BJT

- ❖ Two of the most commonly used Small Signal Models of the BJT are

- The “**r-Parameter Model**” (resistance- Parameter Model).
- The “**h-Parameter Model**” (hybrid- Parameter Model).

These models have to be such that they conform to either or both of the

concept of the semiconductor crystal structure in PNP (or NPN) form of the transistor or the conceptual model of the amplifier circuit.

- ❖ The “**r-Parameter Model**” is obtained by simplifying the Eber’s Moll Model. This itself is obtained by modeling the Physical Attributes of either a PNP or an NPN crystal and relating it to the response of the crystal in an Electrical Circuit.
- ❖ The “**h-Parameter Model**” is obtained by an abstract process of relating the input and output voltages and currents with Thevenin’s equivalent circuit at the input point and Norton’s equivalent circuit at the output point of an amplifier circuit.
- ❖ By using either of these Small Signal Models it becomes possible to calculate the amplified output signal of an amplifier as well as study various other aspects of the behaviour of the amplifier.

## 6.2 Eber’s’-Moll Model of BJT

- ❖ The **Eber’s-Moll Model** has a one-to-one correspondence with the crystal model and it also provides a justification for the shape of the Input and Output Characteristic Curves of the transistor.
- ❖ Taking the “NORMAL (Active)” operation of a PNP Transistor, the Emitter-Base junction  $J_1$  is forward biased and the Collector-Base junction  $J_2$  is reverse biased. As a result of the “Transistor Action”, a current  $I_C$  flows in the collector terminal, which is proportional only to the Input Current  $I_E$  and independent of the voltage applied at the collector terminal.

$$I_C = \alpha_N I_E$$

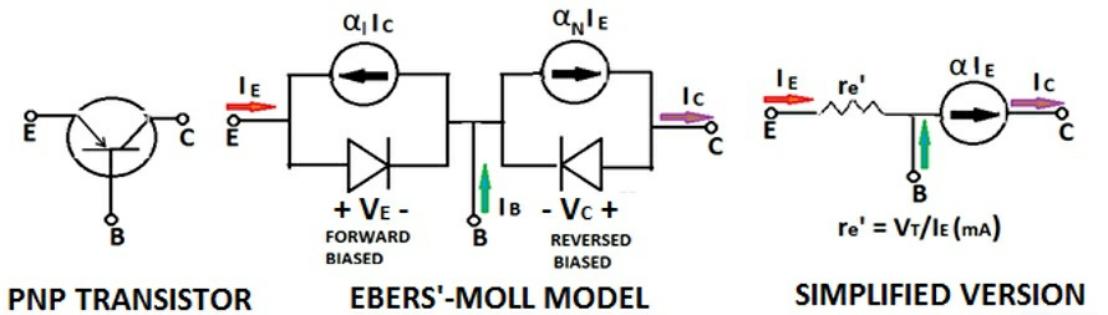
- ❖ Thus, the Collector terminal is represented by a Current Source  $\alpha_N I_E$ , where the subscript “N” denotes “Normal” operation of the transistor. The Forward Biased E-B junction is represented by a Diode, across which a Forward Bias ‘ $V_E$ ’ is appearing, so that terminal ‘E’ is positive and terminal ‘B’ is negative.
- ❖ When the transistor can be “Inversely” connected, by applying a Forward Bias at the Collector-Base junction  $J_2$  and a Reverse Bias at the Emitter-Base junction  $J_1$ . In that case also Transistor Action

will take place, but in the reverse direction.

Thus, Emitter Current will be given by

$$I_E = \alpha_I I_C$$

- ❖ Therefore Emitter terminal can also be represented by a Current Source  $\alpha_I I_C$ , where the **subscript “I”** denotes “Inverse” operation of the transistor.
- ❖ Similarly, in the “Inverse Operation”, the forward biased C-B junction can be represented by a Diode, across which a Forward Bias ‘ $V_E$ ’ is appearing so that terminal ‘C’ is positive and terminal ‘B’ is negative.
- ❖ The resulting circuit is the Ebers’-Moll Model. This is shown in Fig –2.
- ❖ The same can be obtained for the NPN transistor also, since they are duals of each other. However, the polarity of the respective potentials  $V_E$  and  $V_C$ , the directions of the respective currents  $I_E$ ,  $I_C$  and  $I_B$  and **orientation** of the respective Diodes will be opposite.



**Fig- 2**

### Ebers’ Moll Equations

- ❖ For Normal (Active) operation the Collector Current  $I_C$  is given by

$$I_C = \alpha_N I_E + I_{CO}$$

Where  $I_{CO}$  is the Minority Carrier current in the reverse biased C-B junction ( $J_2$ ), and  $\alpha_N$  is the primary transistor parameter ‘ $\alpha$ ’ for Normal Operation.

- ❖ The current in a P-N Junction is given by Shockley’s equation and this is valid for both Forward Bias as well as Reverse Bias.

$$I = I_0 \left( e^{(V/v_T)} - 1 \right)$$

- ❖ Expressing the Minority Carrier current in the junction  $J_2$  by Shockley's equation and representing the applied reverse bias as  $V_C$ , and substituting in the expression for collector current

$$I_C = \alpha_N I_E + I_{CO} \left\{ e^{(V_C/v_T)} - 1 \right\} \quad (A)$$

- ❖ By analogy, if we operate the transistor in the Inverse Mode, with Forward Bias applied to  $J_2$  and Reverse Bias to  $J_1$  we have

$$I_E = \alpha_I I_E + I_{EO} \left\{ e^{(V_E/v_T)} - 1 \right\} \quad (B)$$

Here,  $\alpha_I$  is the primary transistor parameter ' $\alpha$ ' for Inverse Operation.

- ❖ Substituting Eq.-B for  $I_E$  in the Eq. (A)

$$\begin{aligned} I_C &= \alpha_N \left[ \alpha_I I_E + I_{EO} \left\{ e^{(V_E/v_T)} - 1 \right\} + I_{CO} \left\{ e^{(V_C/v_T)} - 1 \right\} \right] \\ I_C &= \alpha_N \alpha_I I_E + \alpha_N I_{EO} \left\{ e^{(V_E/v_T)} - 1 \right\} + I_{CO} \left\{ e^{(V_C/v_T)} - 1 \right\} \end{aligned}$$

Simplifying and rearranging we have

$$I_C = \frac{\alpha_N I_{EO}}{(1-\alpha_N \alpha_I)} \left\{ e^{(V_E/v_T)} - 1 \right\} + \frac{I_{CO}}{(1-\alpha_N \alpha_I)} \left\{ e^{(V_C/v_T)} - 1 \right\} \quad ... (1a)$$

- ❖ Now considering the operation of the transistor in Inverse Mode we obtain the expression for the current  $I_E$  in a similar manner as

$$I_E = \frac{\alpha_I I_{CO}}{(1-\alpha_N \alpha_I)} \left\{ e^{(V_C/v_T)} - 1 \right\} + \frac{I_{EO}}{(1-\alpha_N \alpha_I)} \left\{ e^{(V_E/v_T)} - 1 \right\} \quad ... (1b)$$

**These equations Eq. 1(a) and 1(b) are known as "Ebers' Moll Equations". They describe the complete operation of the BJT and provide a basis for the theoretical evaluation of the Input and Output Characteristics of the BJT.**

### Theoretical Evaluation of the Input and output Characteristics of BJT

- Consider the Common Base Configuration. The circuit, the Ebers

'Moll model and the Input and Output Characteristics are shown.

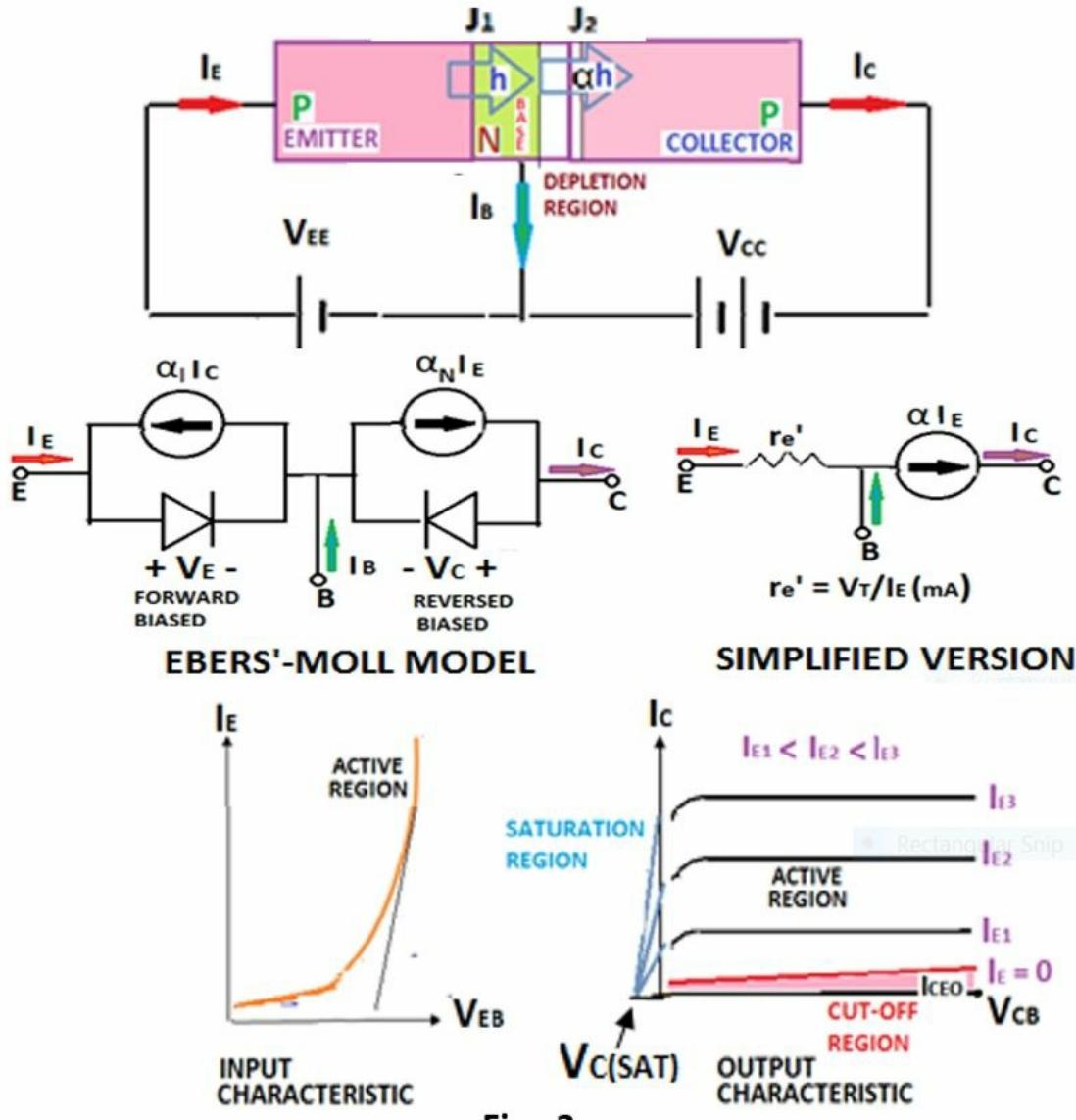


Fig -3.

### ACTIVE REGION

- In the Normal Mode  $\alpha_N = \alpha \approx 1$  and  $\alpha_I \ll 1$ .
- ∴  $\alpha_N \alpha_I \ll 1$

Using the simplified Ebers Moll Model and referring to the First Ebers Moll equation, Eq. 1(a),

1. The quantity  $V_E$  is a forward bias greater than the Cut-in-Voltage  $V_T$
  2. Therefore, the term  $e^{(V_E/V_T)}$  is predominant over 1.
  3. The quantity  $\frac{\alpha_N}{(1-\alpha_N\alpha_I)}$  has a large numerical value.
  4. The second term contains the Reverse Bias  $V_C$ . Thus, the term  $e^{(V_C/V_T)}$  is negligible.
- Therefore, these two terms of this equation together represent a large constant positive current which is determined by the numerical value of  $V_E$ , irrespective of the value of  $V_C$ . Thus, the graph of this current  $I_C$  w.r.t.  $V_C$  is a line parallel to the x-axis. The height of this line above the x-axis is determined by the value of the quantity  $V_E$ . Since  $I_E$  is proportional to  $V_E$  the graph is drawn by indicating the reference parameter as  $I_E$ . this is the Active Region.

### SATURATION REGION

- A Transistor is in the Saturation region when both the junctions  $J_1$  &  $J_2$  are forward biased. In that case both  $V_E$  and  $V_C$  of the Ebers-Moll equation 1 (a) are positive constants.
- But the second term represents a current flowing in the Collector-Base junction in a direction opposite to that represented by the first term. Hence this current is subtracted from the first.
- Hence for increasing values of  $V_C$ , the net current  $I_C$  goes on reducing rapidly and finally become 0 at a value of  $V_C = V_{C(SAT)}$ .

### CUT-OFF REGION

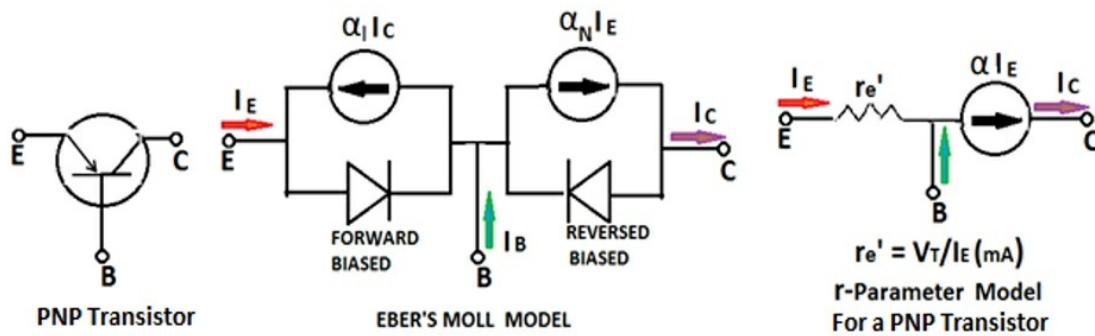
- A Transistor is in the Cut-Off region when both the junctions  $J_1$  &  $J_2$  are reverse biased. both  $V_E$  and  $V_C$  are negative, i.e., when both the junctions are reverse biased, then, in terms of Eq.1, the value of the collector current  $I_C$  becomes a very low, constant quantity of positive sign. Thus, the trace of the output characteristic is a graph of a straight line  $I_{CEO}$ , whose value is very close to the x-axis and essentially parallel to it.

## Section-1

### BJT Amplifier analysis by r-Parameter Model

#### 6.3r-Parameter Model

- The Eber's Moll Model closely corresponds to the physical attributes of the Transistor crystal. **The r-parameter Model is a simplified version of the Eber's Moll Model.**



**Fig. 4.**

**The Simplified Version** of the Ebers-Moll Model is obtained as follows.

- The figure alongside also shows a Simplified Version of the Ebers-Moll Model. This is obtained as follows. The transistor is generally operated in 'Normal' mode. Thus, the components used to represent the 'Inverse' mode can be neglected. Also, the Forward Biased Diode of the E-B junction can be replaced by the 'Forward Resistance' of the junction. This is denoted by the resistance  $r_e'$ .
- The C-B junction is Reverse biased. A reverse biased P-N junction has nearly infinite resistance. Hence the Diode representing the C-B junction can be Open Circuited.
- The simplified Eber's Moll Model is the 'r-Parameter Model' of a transistor.**

- The complete amplifier circuit includes the Biasing arrangement, along with the Source and the Load. The r-parameter model is very convenient even though some of the results obtained are not strictly accurate.

### **The r-Parameter**

The Forward Dynamic Resistance,  $r_D$ , of a P-N junction was given by the following expression

$$r_D = \frac{V_T}{I_f}$$

In the context of the E-B junction this resistance is  $r_e'$ , which is given by

$$r_e' = \frac{V_T}{I_E}$$

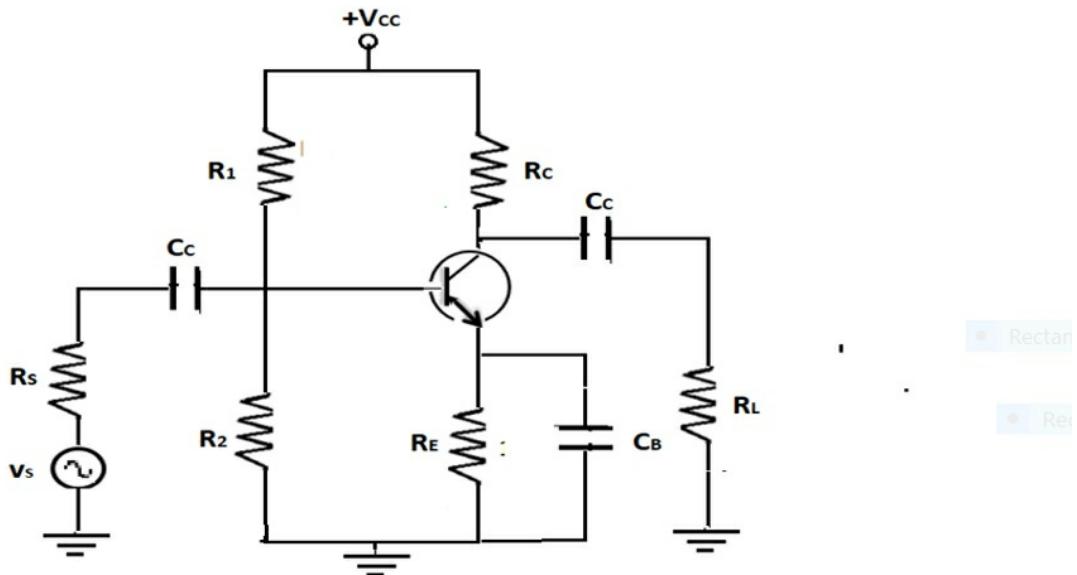
Where,  $I_E$  is the current in the emitter terminal and  $V_T$  is the “Volt equivalent of temperature”. At  $300^0$  K this quantity evaluates to 0.025 V or 25 mV

$$\therefore r_e' = \frac{25 \text{ (mV)}}{I_E \text{ (mA)}} \quad (\text{in units of } \Omega) \quad \dots\dots(1)$$

### **Consider a R-C Coupled Common Emitter Amplifier**

- In ‘R-C Coupled Amplifier’ the signal from the source is **coupled** to the input point of the amplifier by a ‘**Coupling Capacitor**’  $C_C$ . The amplified output signal is **coupled** to the external load by another **Coupling Capacitor**. A “**By Pass**

**Capacitor** “ $C_B$ ” is required to by-pass the AC signal from the resistance  $R_E$ .

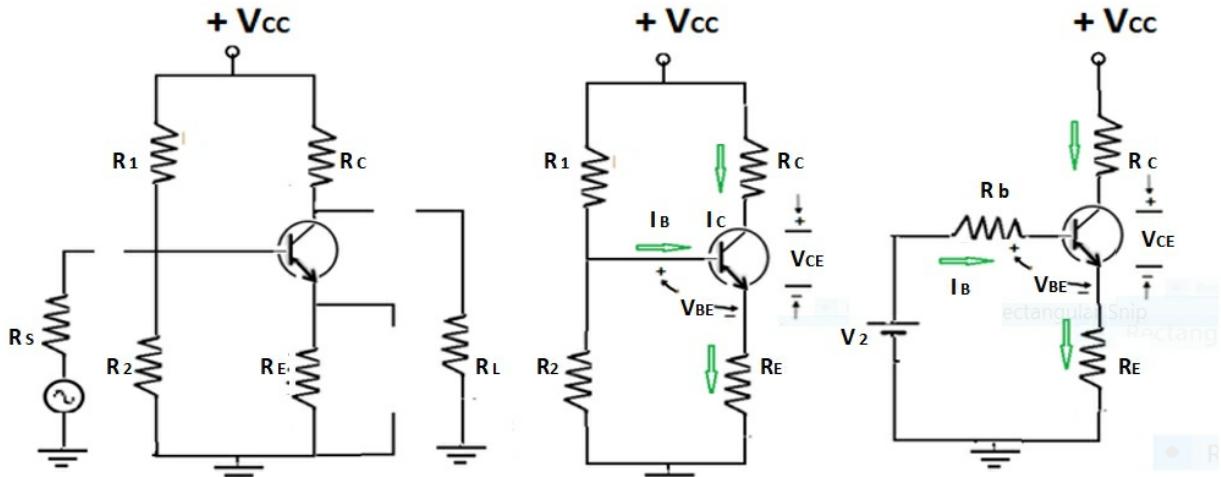


### STEPS OF ANALYSIS:

- ✓ The Amplifier is a circuit containing two voltage sources, the DC Biasing voltage, “ $V_{CC}$ ” and the AC Signal voltage, “ $v_s$ ” and. Hence it is analyzed using ‘**Superposition Principle**’.
- ✓ Thus we have the two steps as ( i ) DC Analysis and ( ii ) AC Analysis.

### DC Analysis

- ✓ The AC signal source is short circuited, the circuit works only with the DC biasing signal  $V_{CC}$ .
- ✓ For DC signal, frequency  $f = 0$ . Capacitive reactance is  $X_C = 1 / 2 \pi f C$ . At  $f = 0$ , the capacitive reactance is infinity.
- ✓ Hence **all capacitors are to be open circuited**. By doing this we obtain the DC equivalent circuit of the amplifier, which is shown in the **Fig –5** below. This circuit is analyzed to obtain the DC Emitter current  $I_E$  and from this we calculate the ‘Forward Resistance’ ‘ $r_e$ ’ of the E-B junction by using Eq. 1.



DC EQUIVQLENT CIRCUIT      THEVENIN's EQUIVALENT

**Fig –5**

- ✓ The DC equivalent circuit of Fig. – 5 is the **Voltage Divider Biasing Circuit** that we discussed and analyzed in the previous chapter. The steps of analysis are repeated underneath for convenience.

1. The voltage across the biasing resistance  $R_2$  is given by the Voltage Divider Rule and parallel combination of  $R_1$  and  $R_2$  is given as

$$V_2 = \frac{R_2 V_{CC}}{(R_1 + R_2)} \quad R_b = R_1 || R_2 = \frac{R_1 R_2}{(R_1 + R_2)}$$

2. Thevenizing the Base-Emitter loop with  $V_2$  as the Thevenin's Equivalent voltage and the parallel combination of  $R_1$  and  $R_2$  as the Thevenin's Equivalent resistance, we get -

The KVL equation of the Base –Emitter Loop is

$$V_2 = I_B R_b + V_{BE} + I_E R_E$$

Where  $I_E = I_C + I_B$       AND       $I_C = \beta I_B$ . Substituting and simplifying

$$V_2 - V_{BE} = I_B \{R_b + (1 + \beta)R_E\}$$

$$\therefore I_B = I_{BQ} = \frac{V_2 - V_{BE}}{\{R_b + (1+\beta)R_E\}} \quad \dots (2)$$

From this we get

$$I_{CQ} = \beta I_B = I_E \quad \dots (3)$$

3. After calculating  $I_E$  the r-Parameter ' $r_e'$  of the transistor is calculated, using Eq. –1

$$r_e' = \frac{25 \text{ (mV)}}{I_E \text{ (mA)}} \quad (\text{in units of } \Omega) \quad \dots (4)$$

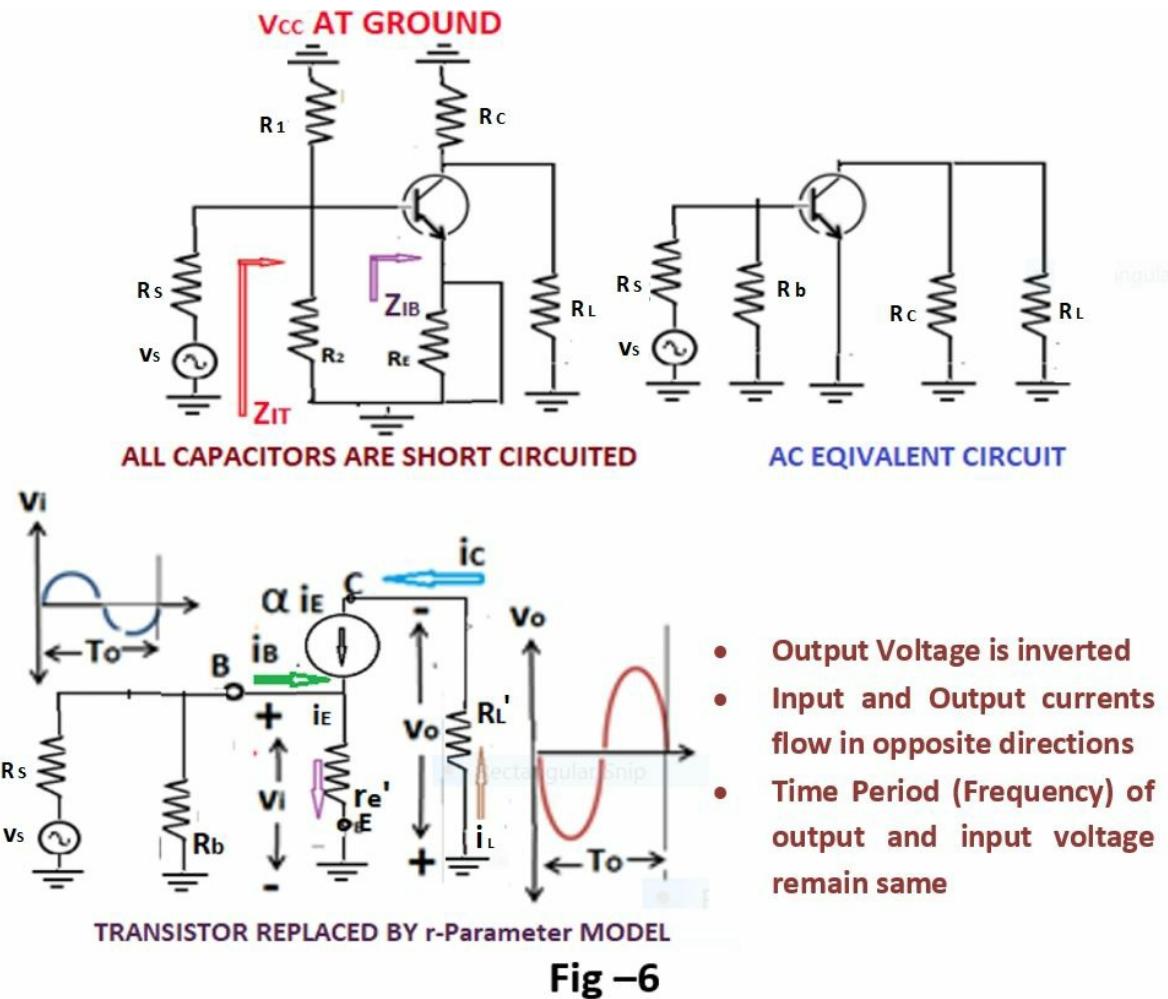
### AC Analysis

- ✓ We assume the DC biasing source to be short circuited, so that the circuit works only with the AC signal source signal  $v_s$ .
- ✓ Assuming that the AC signal is of a high frequency 'f', the capacitors have a capacitive reactance  $X_C = 1 / 2 \pi f C$ , tending to zero.
- ✓ Hence all capacitors are to be short circuited. When the coupling capacitors are short circuited, the signal source ' $v_s$ ' and the load ' $R_L$ ' are directly connected to the rest of the circuit.
- ✓ When the By-Pass capacitor  $C_B$  is short circuited, the equivalent resistance of the parallel combination of  $R_E$  and  $C_B$  becomes zero. Hence the Emitter terminal is directly connected to ground.
- ✓ The Short Circuited  $V_{CC}$  point is at zero potential, which is the 'ground potential'. Thus, we obtain the AC equivalent circuit of the amplifier, shown in **Fig –6** below.

The AC Equivalent Circuit can be simplified as follows –

1. **The two resistances  $R_1$  and  $R_2$  are in parallel. Hence, they are replaced by their parallel combination ' $R_b$ '. This had been evaluated during DC Analysis.**
2. **The biasing resistance  $R_C$  and the load resistance  $R_L$  appear in parallel at the collector terminal. Hence these are replaced by their parallel combination ' $R_L'$ '.**
3. **Thereafter the transistor circuit symbol is replaced by the r-**

## Parameter Model.



- Output Voltage is inverted
- Input and Output currents flow in opposite directions
- Time Period (Frequency) of output and input voltage remain same

### (1) Voltage Gain: $A_V$

Voltage gain of an amplifier is defined as

$$A_V = \frac{V_o}{V_i}$$

Where ' $v_0$ ' is the **amplified voltage** developed across the Load Resistance  $R_L$ .

In the equivalent circuit  $R_L'$  is the parallel combination of  $R_C$  and  $R_L$ . Hence the voltage shown to be appearing across  $R_L'$  is the same as that actually appears across the external load resistance  $R_L$ .

$$v_0 = i_C R_L' = -i_0 R_L'$$

(the current through  $R_L$  is in opposite direction to  $i_C$ , hence the - ve sign)

And

' $v_i$ ' is the Input Voltage at the input of the transistor. Thus ' $v_i$ ' is the voltage developed across the resistance  $r_e'$ , due to the current ' $i_E$ '.

$$\therefore v_i = i_E r_e' = i_C r_e' \quad (\text{since } i_E \approx i_C)$$

Substituting we have

$$A_v = \frac{v_o}{v_i} = \frac{-i_C R_L}{i_C r_e'}$$

OR

$$A_v = \frac{-R_L}{r_e'} \quad \dots (5)$$

## (2) Input Impedance at the Base: $Z_{I(B)}$

The current ' $i_E$ ' flows between the input point Base and the grounded point Emitter. Thus, the Input Impedance at the Base,

$$Z_{I(B)} = \frac{v_i}{i_B} = \frac{i_E r_e'}{i_B}$$

In a transistor,

$$i_E = i_C \quad \text{and} \quad i_C / i_B = \beta$$

$$\therefore Z_{I(B)} = \beta r_e' \quad \dots (6)$$

### (3) Total Input Impedance OR Net Input Impedance across the source: $Z_{I(T)}$

Total Input Impedance of the amplifier is the impedance appearing between the point at which the source is connected and the grounded point, that is the parallel combination of ' $Z_{I(B)}$ ' and ' $R_b$ '. Thus

$$Z_{I(T)} = Z_{I(B)} \parallel R_b = \frac{Z_{I(B)} R_b}{(Z_{I(B)} + R_b)} \quad \dots(7)$$

### (4) Current Gain: $A_I$

In order to derive an expression for Current Gain the AC Equivalent circuit of the amplifier is to be looked at in more details. This is reproduced in Fig – 7 below.

Current Gain of the amplifier can be defined as

$$A_I = \frac{i_L}{i_s} = \frac{-i_C}{i_s}$$

In the circuit in Fig – 7 the current supplied by the source is divided into two paths, one through the resistance  $R_b$ , which is current 'i' and the other is the current flowing into the Base of the transistor, ' $i_B$ '

Thus

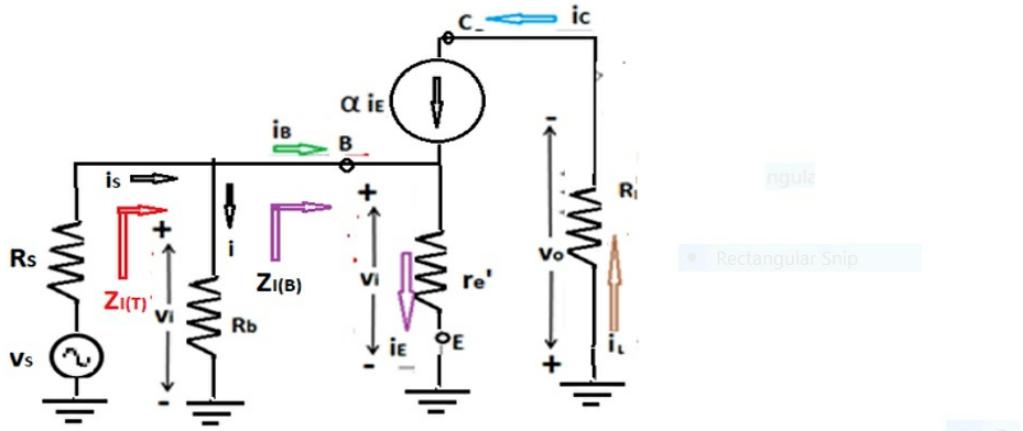
$$i_s = i + i_B \quad \text{where} \quad i_s = \frac{v_i}{Z_{I(T)}} \\ & \text{&} \\ i_L = \frac{v_o}{R'_L} \quad ; \quad i = \frac{v_i}{R_b} \quad \& \quad i_B = \frac{v_i}{Z_{I(B)}}$$

Substituting in the expression for  $A_I$ ,

$$A_I = \frac{i_L}{i_s} = \frac{\left(v_o/R'_L\right)}{\left(v_i/Z_{I(T)}\right)}$$

Where,  $v_o / v_i = A_v$

$$\therefore A_I = A_v \cdot \frac{Z_{I(T)}}{R'_L} \quad \dots 8(a)$$



**Fig – 7.**

Using the Eq. 5. for  $A_V$  and substituting

$$A_I = \frac{-R'_E}{r'_e} \cdot \frac{Z_{I(T)}}{R'_E}$$

$$\therefore A_I = \frac{-Z_{I(T)}}{r'_e} \quad \dots 8(b)$$

### SIGNIFICANCE OF THE NEGATIVE SIGN OF $A_V$ & $A_I$ : -

The directions of the currents ' $i_E$ ' and ' $i_L$ ' in Fig –6 are such as,  $i_E$  is flowing from top to bottom,  $i_L$  is flowing from bottom to top. While  $i_E$  flowing through  $r_e'$  produces  $v_i$ ,  $i_L$  flowing through  $R_L'$  produces  $v_o$ . In other words, the polarities of  $v_o$  and  $v_i$  are opposite to each other.

**When the input signal is in the positive half cycle, the output signal is in the negative half cycle and vice-versa. This demonstrates a phase angle inversion of  $180^\circ$  of  $v_o$  w.r.t.  $v_i$ . This inversion of the output signal is represented by the negative sign of  $A_V$ .**

### EFFECT OF SOURCE RESISTANCE ' $R_s$ '.

A portion of the signal power is absorbed by the internal resistance, ' $R_s$ ' of the source.

Drop in the input signal power compared to the signal generated by the source is given by the '**voltage divider rule**' and the '**current divider rule**' respectively.

By voltage divider rule

$$v_i = \frac{Z_{I(T)}}{R_s + Z_{I(T)}} \cdot v_s \quad \& \quad i_i = \frac{R_s}{R_s + Z_{I(T)}} \cdot i_s$$

$$\therefore \frac{v_i}{v_s} = \frac{Z_{I(T)}}{R_s + Z_{I(T)}} \quad \& \quad \frac{i_i}{i_s} = \frac{R_s}{R_s + Z_{I(T)}}$$

**Real Voltage Gain** and **Real Current Gain** is evaluated by taking into consideration the drop in  $R_s$ .

$$A_{VS} = \frac{v_o}{v_s} = \frac{v_o}{v_i} \cdot \frac{v_i}{v_s}$$

where  $\frac{v_o}{v_i} = A_v$  defined by Eq. 5 as

$$A_v = \frac{-R_L}{r_e}$$

Substituting for  $\frac{v_i}{v_s}$

---


$$A_{VS} = \frac{Z_{I(T)}}{R_s + Z_{I(T)}} \cdot A_v$$

$$A_{VS} = \frac{-Z_{I(T)} R_{L'}}{(R_s + Z_{I(T)}) r_{e'}} \quad \dots (9)$$

And

$$A_{IS} = \frac{i_o}{i_s} = \frac{i_o}{i_i} \cdot \frac{i_i}{i_s}$$

where  $\frac{i_o}{i_i} = A_I$  defined by Eq. 8 (b)

Substituting for  $\frac{i_i}{i_s}$

$$A_{IS} = \frac{R_s}{R_s + Z_{I(T)}} \cdot A_I$$

$$A_{IS} = \frac{-Z_{I(T)} R_s}{(R_s + Z_{I(T)}) r_{e'}} \quad \dots (10)$$

## EFFECT OF EMITTER BY-PASS CAPACITANCE $C_B$ .

The R-C Coupled Amplifier contains a capacitor  $C_B$ . The purpose of this capacitor is to **By-pass the AC signal** from the biasing resistance  $R_E$ . Assume a situation that this capacitor is not connected. This will not affect the DC analysis. But the AC equivalent circuit will now contain the resistance  $R_E$ .

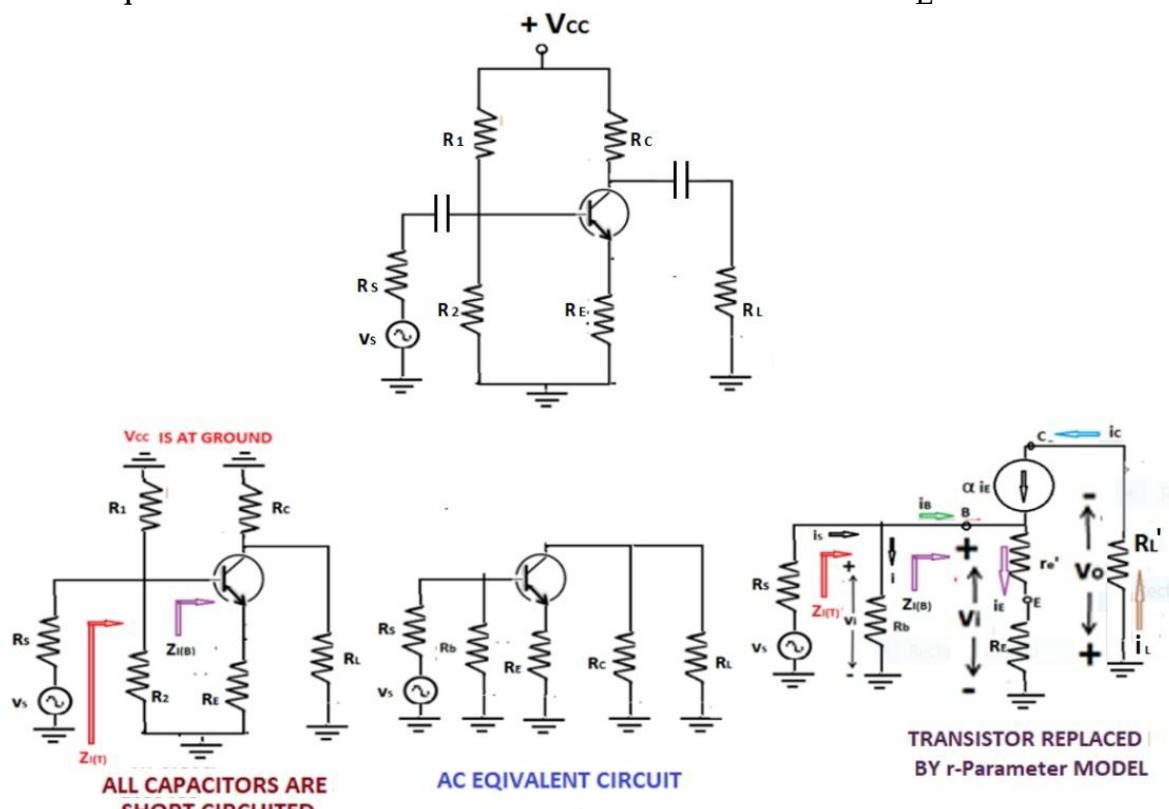


Fig- 8.

Because of the inclusion of  $R_E$  in the AC equivalent circuit, the input voltage ' $v_i$ ' and ' $Z_{I(B)}$ ' will be as shown below. Accordingly, the equations (5) to (9) will also be modified.

$$v_i = i_E(r_e' + R_E)$$

&

$$Z_{I(B)} = \beta(r_e' + R_E)$$

$$\therefore A_V = \frac{-R_L'}{(r_e' + R_E)} \quad \dots(11)$$

$$Z_{I(B)} = \beta (r_e' + R_E) \quad \dots(12)$$

$$A_I = \frac{-Z_{I(T)}}{(r_e' + R_E)} \quad \dots(13)$$

Comparing Eq.-11 and Eq.-13 with Eq.-5 and Eq.-8 respectively, we see that the denominator in the later equations is larger than the respective former ones. Thus, the Voltage Gain and Current Gain is reduced when the By-Pass Capacitor is removed. Comparing Eq-12 with Eq.-6 , we observe that the Input impedance is increased when the By-Pass capacitor is absent.

### EFFECT OF TEMPERATURE VARIATION ON AMPLIFIER PERFORMANCE

The expressions of  $A_V$ ,  $A_I$  and  $Z_{I(B)}$ , dependent on the value of the resistance  $r_e'$  of the **r-parameter Model**. This resistance is given by the Eq.-1, is reproduced below for reference.

$$r_e' = \frac{V_T(Volt)}{I_E(A)}$$

The quantity  $V_T$  is known as '**Volt Equivalent of Temperature**', given by

$$V_T = \frac{kT}{q}$$

Where 'k' is Boltzmann Constant, 'T' is room temperature in  $^0K$  and 'q' is charge of electron.

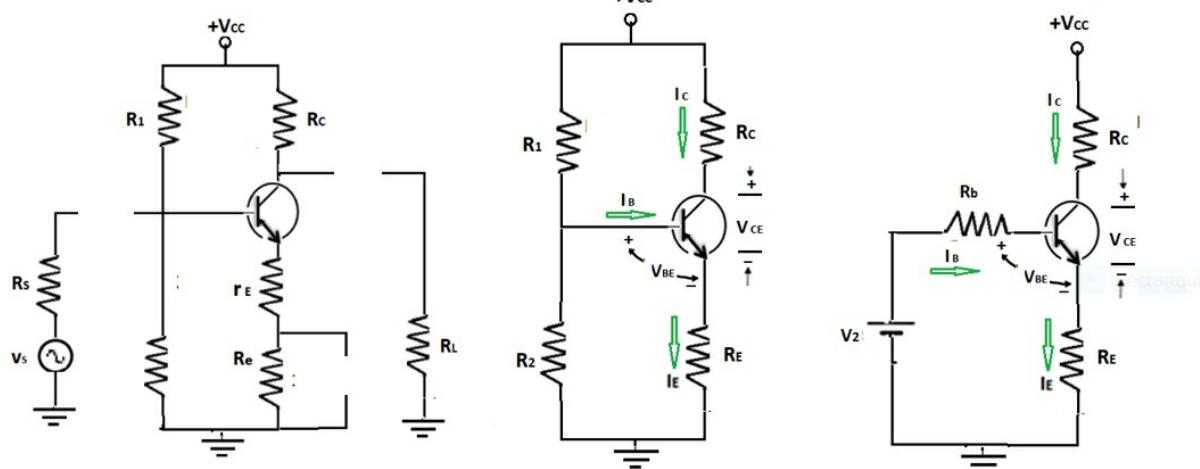
Thus  $r_e'$ , is dependent on temperature. This temperature dependence of performance of amplifier is overcome by the use of an extra resistance ' $r_E$ ' in the Emitter.

**This resistance is called the 'Emitter Swamping Resistance'.**

### **EFFECT OF 'EMITTER SWAMPING RESISTANCE'**

The Amplifier circuit with the 'Emitter Swamping Resistance', connected to the Emitter terminal as shown in the Fig- 9 below.

### **DC Analysis**



AMPLIFIER CIRCUIT WITH CAPACITORS OPEN CIRCUITED

DC EQUIVALENT CIRCUIT &amp; IT'S THEVENIN'S EQUIVALENT

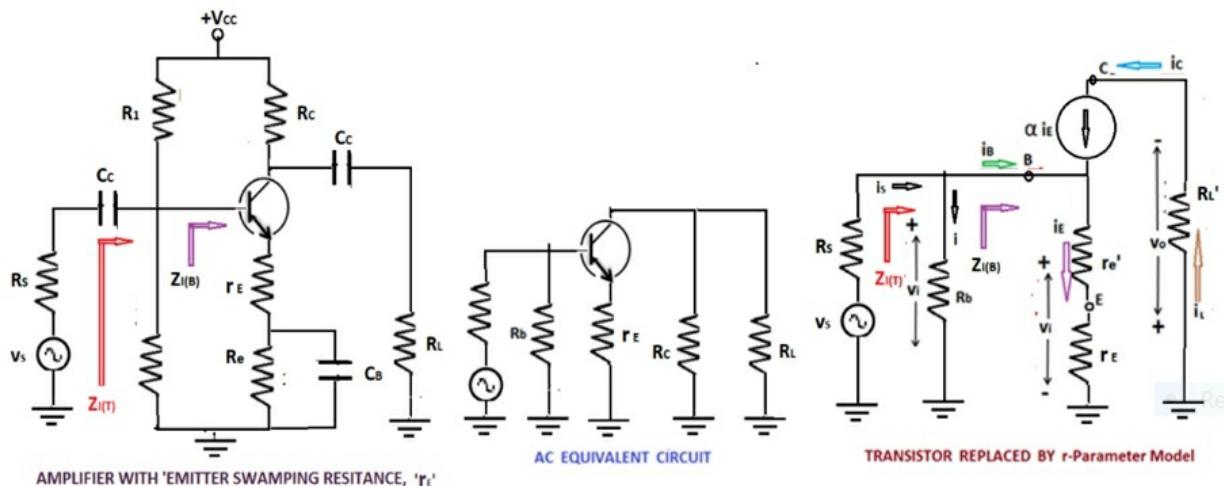
The DC equivalent circuit of the amplifier, shown in the figure will contain a series combination of the resistances ' $r_E$ ' and ' $R_e$ '. The net DC resistance at the emitter terminal is the sum of these two resistances.

$$R_E = R_e + r_E$$

Thus, there will be no change in the DC Analysis.

### AC Analysis

The By-Pass capacitor  $C_B$  will be short circuited across the resistance  $R_e$ . Only the Emitter Swamping Resistance  $r_E$  will remain in the AC Equivalent circuit. After replacing the transistor with the **r-parameter Model**, which contains the resistance  $r_E$ , we have



AMPLIFIER WITH 'EMITTER SWAMPING RESISTANCE, 'r\_E'

AC EQUIVALENT CIRCUIT

TRANSISTOR REPLACED BY r-Parameter Model

Fig.-9

$$v_i = i_E (r_e' + r_E)$$

$$\therefore A_v = \frac{-R_{L'}}{(r_{e'} + r_E)}$$

$$Z_{I(B)} = \beta (r_e' + r_E)$$

$$A_I = \frac{-Z_{I(T)}}{(r_{e'} + r_E)}$$

Where  $Z_{I(T)} = Z_{I(B)} \parallel R_b$

$$Z_{I(T)} = \frac{Z_{I(T)} \cdot R_b}{Z_{I(T)} + R_b}$$

Now in this circuit, if we take a high enough resistance  $r_E$  such that

$$r_E \gg r_e'$$

We will have the expressions of  $A_v$ ,  $Z_{I(B)}$  and  $A_I$  approximated as

$$A_v \approx \frac{-R_{L'}}{r_E} \quad \dots(14)$$

$$Z_{I(B)} \approx \beta r_E \quad \dots(15)$$

$$A_I \approx \frac{-Z_{I(T)}}{r_E} \quad \dots(16)$$

In these expressions the resistance ' $r_E$ ' is not temperature dependent.

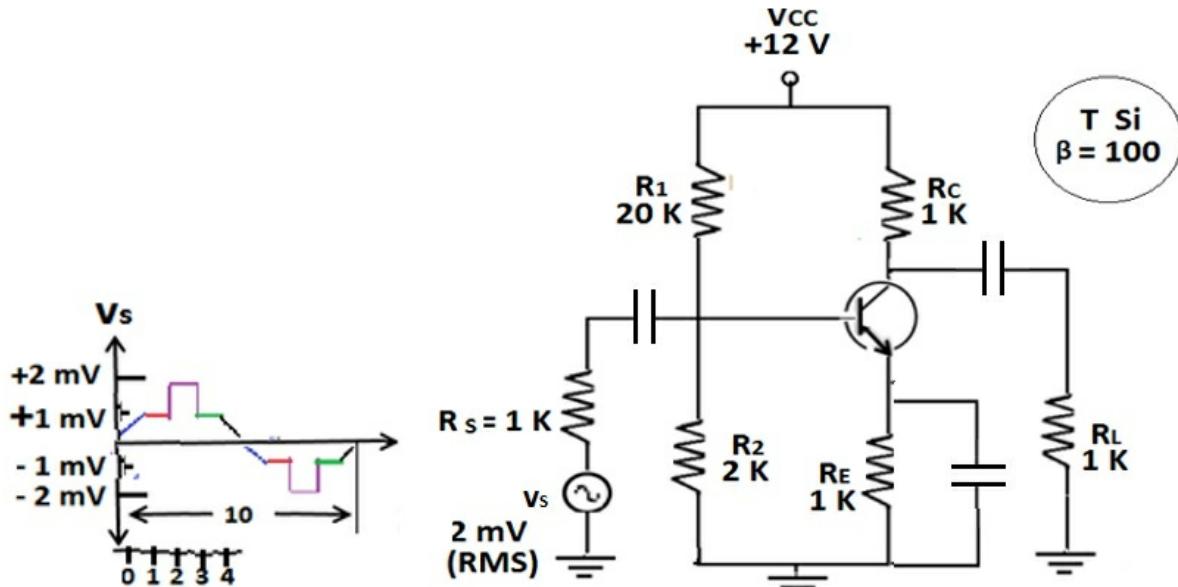
Thus, the effect of the use of the Emitter Swamping Resistance ' $r_E$ ' is to make the performance of the amplifier independent of temperature variations.

In other words, the performance of the amplifier is stabilized due to the use of the Emitter Swamping Resistance.

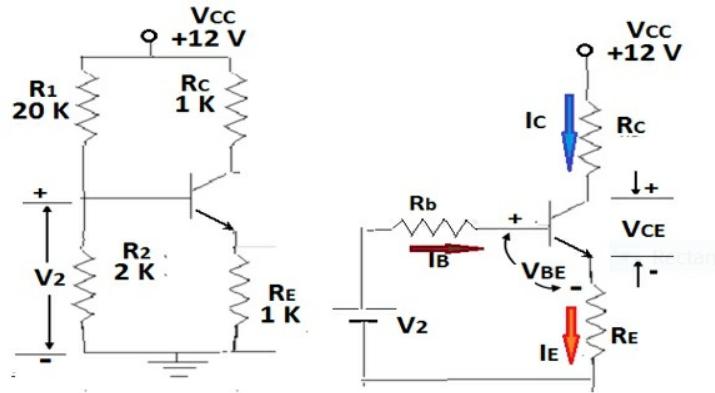
**IMPORTANT NOTE :- THE STEPS OF ANALYSIS OF AMPLIFIERS DISCUSSED ABOVE APPLY TO BOTH P-N-P AND N-P-N TRANSISTORS, AND USE THE SAME FORMULAE FOR BOTH DC & AC ANALYSIS**

## Tutorial-1(A)

**Example – 1:** - To analyze the amplifier shown in figure and sketch the output voltage waveform. The Data about the transistor is as shown in the label in the diagram.



**DC Analysis**



**DC EQUIVALENT CIRCUIT & IT'S THEVENIN'S EQUIVALENT**

**DC Analysis is required to be carried out to calculate ' $r_e$ ' and ' $R_b$ '.**

The steps for DC Analysis are as follows

- The signal source ' $v_s$ ' is open circuited
- All the capacitors are short circuited.
- This results in the DC Equivalent Circuit.
- The Thevenin's Equivalent of the Base-Emitter loop of the DC Equivalent Circuit is obtained for the purpose of DC analysis.

Thevenizing the Base-Emitter loop, with

$$V_2 = \frac{R_2 V_{CC}}{(R_1 + R_2)} = \frac{2 \times 12}{2+20} = 1.09 \text{ V}$$

$$R_b = \frac{R_1 R_2}{(R_1 + R_2)} = \frac{2 \times 20}{2+20} = 1.82 \text{ k}\Omega$$

$$I_B = I_{BQ} = \frac{V_2 - V_{BE}}{\{R_b + (1+\beta)R_E\}}$$

Given that we have Si Transistor having  $\beta = 100$ , since Si,  $V_{BE} = 0.7 \text{ V}$   
; substituting --

$$I_{BQ} = \frac{1.09 - 0.7}{\{1.82 + (1+100) \cdot 1\}} = 0.0038 \text{ mA}$$

In this calculation we have divided  $(1.09 - 0.7)$  Volt with a resistance having a value expressed in  $\text{k}\Omega$ . Hence, we obtain the value of  $I_{BQ}$  in units of mA. The reason for this is, that, the **r-parameter  $r_e'$** , expressed by Eq. – 1 requires the value of  $I_E$  in the units of mA.

We have

$$I_E \approx I_{CQ} = \beta I_{BQ} = 100 \times 0.0038 = 0.38 \text{ mA}$$

$$\therefore r_e' = \frac{25}{I_E (\text{mA})} = \frac{25}{0.38} = 65.8 \Omega$$

### Location Of Q-Point

We have the DC Load-Line equation as –

$$I_C = \frac{V_{CC}}{(R_C + R_E)} - \frac{V_{CE}}{(R_C + R_E)}$$

Substituting for  $I_{CQ} = 0.38 \text{ mA}$

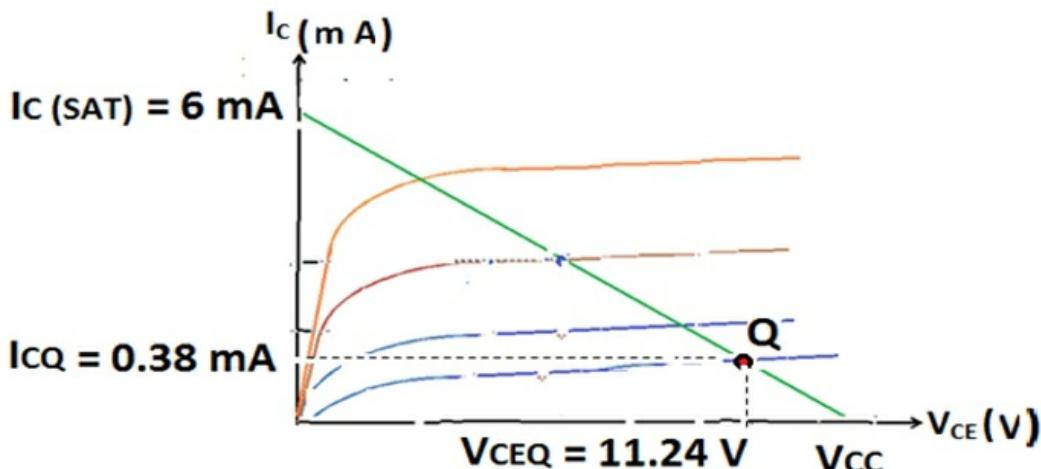
$$V_{CEQ} = V_{CC} - I_{CQ} (R_C + R_E) = 12 - 0.38 \times (1 + 1)$$

$$V_{CEQ} = 11.24 \text{ V}$$

From the Load Line Equation we also get ‘Vertical-Intercept’  $I_{C(SAT)}$  and ‘horizontal Intercept’ as  $V_{CC}$

$$I_{C(SAT)} = \frac{V_{CC}}{(R_C + R_E)} = \frac{12 \text{ V}}{(1K + 1K)}$$

$$I_{C(SAT)} = 6 \text{ mA}$$



THE Q-POINT LOCATION ON THE DC LOAD – LINE IS SHOWN ABOVE

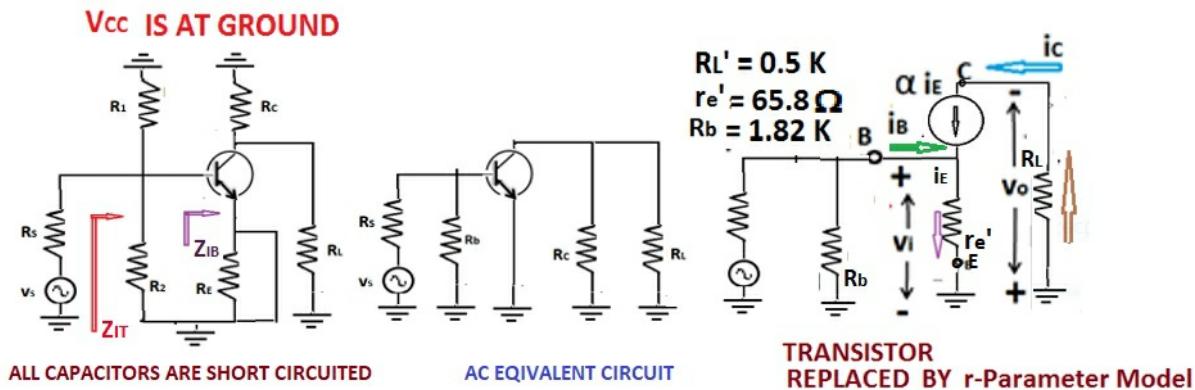
### AC ANALYSIS

AC Analysis is done to calculate  $A_V$ ,  $A_I$  and  $Z_I$ . The steps for AC Analysis are as follows-

- The DC Bias  $V_{CC}$  is short circuited and the ends of the resistances to which  $V_{CC}$  was connected is assumed to be at ‘Ground’.
- All capacitors are open circuited. The parallel combination of

the short circuited capacitor  $C_B$  (zero impedance) across  $R_E$  results in a net impedance equal to zero. Thus the Emitter terminal is connected to Ground.

- The resistances  $R_1$  and  $R_2$  are now in parallel at the Base point. Hence it is represented by their parallel combination ' $R_b$ '. The resistances  $R_C$  and  $R_L$  are in parallel at the Collector point. Hence it is represented by their parallel combination ' $R_{L'}$ '.
- The transistor is replaced by the **r-parameter Model** for the purpose of AC Analysis.



Using the circuit shown above and using Eq. 5 to Eq. –10, we have

$$A_V = \frac{-R_L}{r_e} = \frac{-500 \Omega}{65.8 \Omega}$$

$$A_V = -7.6$$

$$Z_{I(B)} = \beta r_e' = 100 \times 65.8 = 6580 \Omega$$

$$Z_{I(B)} = 6.58 \text{ K}$$

$$Z_{I(T)} = \frac{Z_{I(B)} R_b}{(Z_{I(B)} + R_b)} = \frac{6.58 \times 1.82}{6.58 + 1.82} = 1.43 \text{ K}$$

$$Z_{I(T)} = 1430 \Omega$$

$$A_I = \frac{-Z_{I(T)}}{r_e'} = \frac{-1430}{65.8} = -21.73$$

$$A_{Vs} = \frac{-Z_{I(T)} R_{L'}}{(R_s + Z_{I(T)}) r_e'} = \frac{(-1430 \times 500)}{(1000 + 1430) \times 65.8}$$

$$A_{VS} = -4.47$$

$$A_{IS} = \frac{-Z_{I(T)} R_S}{(R_S + Z_{I(T)}) r_e'} = \frac{(-1430 \times 1000)}{(1000 + 1430) \times 65.8}$$

$$A_{IS} = -8.93$$

**Net Power Gain G =  $A_{VS} \cdot A_{IS} = (-4.47) \times (-8.93) = 39.9$**

**Output Voltage  $v_o = A_{VS} \cdot v_s = -4.47 \times 2 = -8.9 \text{ mV (rms)}$**

(Given  $v_s = 2 \text{ mV (rms)}$ )

**Output Power is delivered across the external load resistance  $R_L$**

$$P_o = \frac{v_o^2}{R_L} = \frac{0.0089^2}{1000} = 7.9 \times 10^{-8} \text{ W}$$

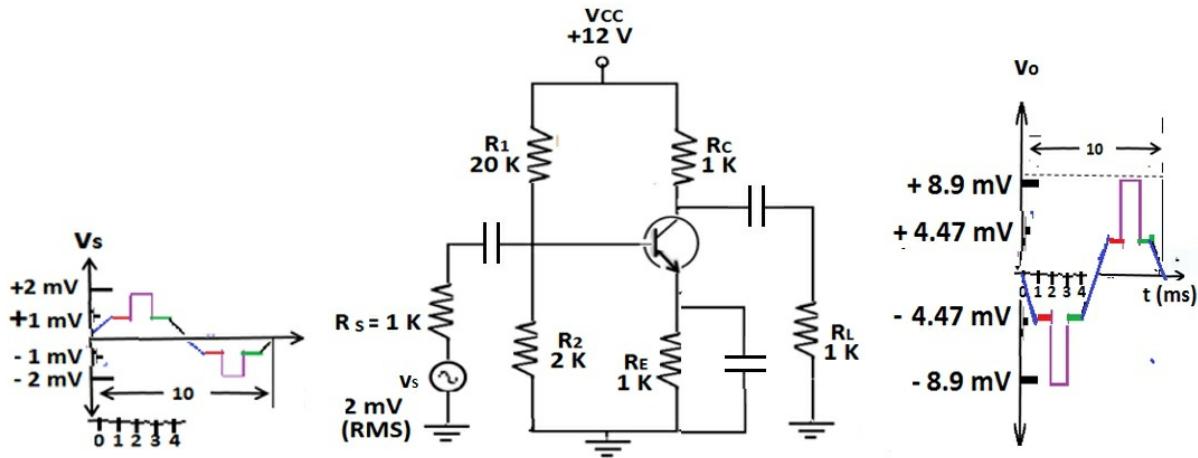
$$P_o = 0.079 \mu \text{W}$$

## OUTPUT VOLTAGE WAVEFORM

The output voltage is given by

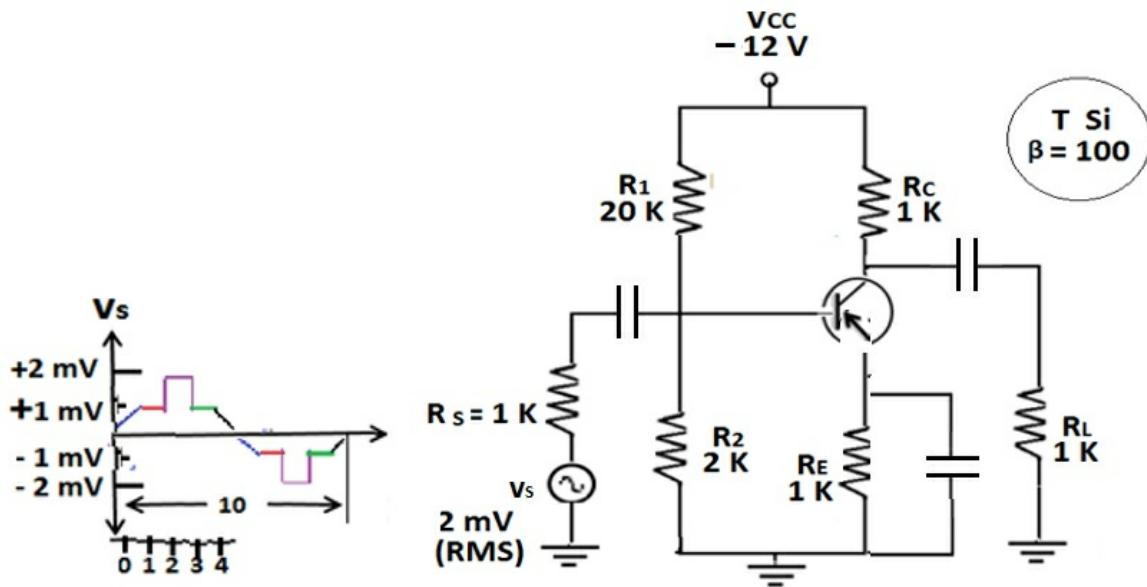
$$v_o = A_{VS} \cdot v_s$$

- Here  $A_{VS}$  is a negative quantity. The instantaneous output voltage is obtained by multiplying each of the instantaneous input voltage values with  $A_{VS}$ .
- During the time interval  $t = 0$  to  $t = 1$  (on the time scale shown in the figure) the Input is '**rising**', shown by the '**Blue**' trace. Since  $A_{VS}$  is negative, the corresponding output during this time interval is '**rising**' in the negative direction, shown by '**Blue**'.
- This correspondence of the output waveform with respect to the input waveform is shown with different colours at the different time intervals on the time scale.
- Due to the negative sign of  $A_{VS}$  the output voltage appears with a phase shift of  $-180^\circ$ . This phase shift makes the output voltage inverted, as shown in the figure below.



**OUTPUT SIGNAL IS AMPLIFIED WITH A VOLTAGE GAIN OF “-  $A_{VS}$ ”, WHICH RESULTS IN A  $-180^\circ$  PHASE DIFFERENCE BETWEEN INPUT AND OUTPUT VOLTAGES. IN OTHER WORDS, THE OUTPUT VOLTAGE WAVEFORM IS INVERTED.**

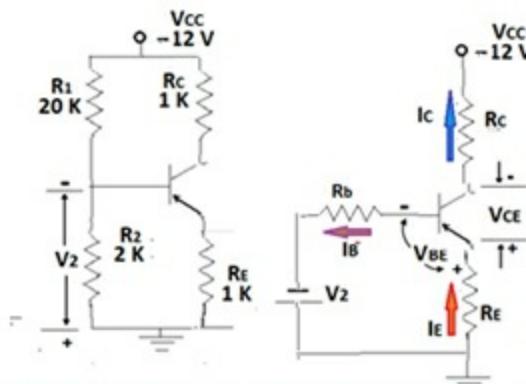
**Example – 2(P-N-P Transistor):-** We use a PNP transistor , with the same characteristic and primary parameters as the NPN Transistor of Example-1. (We need to demonstrate that PNP & NPN Transistors are Duals of each other. Which means, that for the same source and the same load, both of these transistors produce the same result).



## SOLUTION :: DC ANALYSIS

The steps for DC Analysis are same as before,

- The signal source ‘ $v_s$ ’ is open circuited
- All the capacitors are short circuited.
- This results in the DC Equivalent Circuit.
- The Thevenin’s Equivalent of the Base-Emitter loop of the DC Equivalent Circuit is obtained for the purpose of DC analysis.



DC EQUIVALENT CIRCUIT & IT'S THEVENIN'S EQUIVALENT

Using Thevenin’s equivalent voltage and Thevenin’s equivalent resistance--

$$V_2 = \frac{R_2 V_{CC}}{(R_1 + R_2)} = \frac{2 \times 12}{2+20} = 1.09 \text{ V}$$

$$R_b = \frac{R_1 R_2}{(R_1 + R_2)} = \frac{2 \times 20}{2+20} = 1.82 \text{ k}\Omega$$

$$I_B = I_{BQ} = \frac{V_2 - V_{BE}}{\{R_b + (1+\beta)R_E\}}$$

Given that we have Si Transistor having  $\beta = 100$ , since Si ,  $V_{BE} = 0.7 \text{ V}$  ; substituting --

$$I_{BQ} = \frac{1.09 - 0.7}{\{1.82 + (1+100) \cdot 1\}} = 0.0038 \text{ mA}$$

$$I_E \approx I_{CQ} = \beta I_{BQ} = 100 \times 0.0038 = 0.38 \text{ mA}$$

$$\therefore r_e' = \frac{25}{I_E (\text{mA})} = \frac{25}{0.38} = 65.8 \Omega$$

### Location Of Q-Point

DC Load-Line equation –

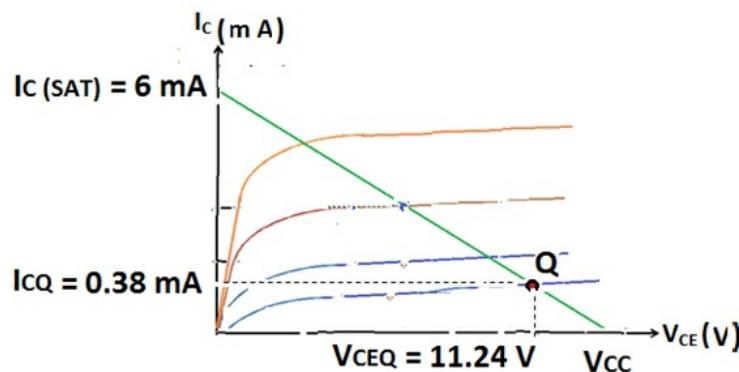
$$I_C = \frac{V_{CC}}{(R_C + R_E)} - \frac{V_{CE}}{(R_C + R_E)}$$

$$V_{CEQ} = V_{CC} - I_{CQ} (R_C + R_E)$$

$$= 12 - 0.38 \times (1 + 1) = 11.24 \text{ V}$$

DC Load Line is drawn by taking ‘Horizontal Intercept’ as  $V_{CC}$  and ‘Vertical-Intercept’ as  $I_{C(SAT)}$ , where,

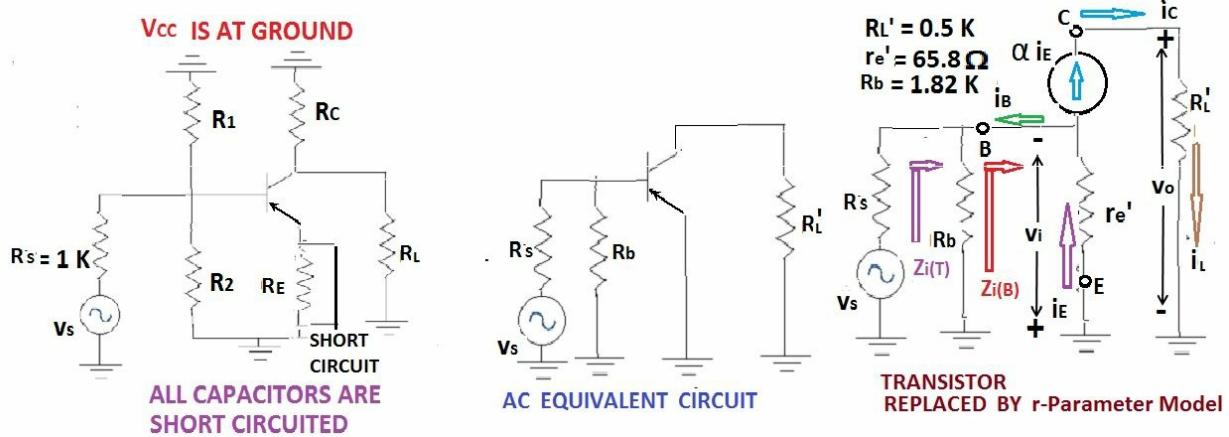
$$I_{C(SAT)} = \frac{V_{CC}}{(R_C + R_E)} = \frac{12 \text{ V}}{(1 \text{ K} + 1 \text{ K})} = 6 \text{ mA}$$



## AC ANALYSIS

AC Analysis is done to calculate  $A_V$ ,  $A_I$  and  $Z_I$ . The steps for AC Analysis are as follows-

- The DC Bias  $V_{CC}$  is short circuited and the ends of the resistances to which  $V_{CC}$  was connected is assumed to be at ‘Ground’.
- All capacitors are open circuited. The parallel combination of the short circuited capacitor  $C_B$  ( zero impedance ) across  $R_E$  results in a net impedance equal to zero. Thus the Emitter terminal is connected to Ground.
- The resistances  $R_1$  and  $R_2$  are now in parallel at the Base point. Hence it is represented by their parallel combination ‘ $R_b$ ’. The resistances  $R_C$  and  $R_L$  are in parallel at the Collector point. Hence it is represented by their parallel combination ‘ $R_L$ ’.
- The transistor is replaced by the **r-parameter Model** for the purpose of AC Analysis.



Using the circuit shown above and using the equations 5 to 10

$$A_V = \frac{-R_L}{r_e'} = \frac{-500 \Omega}{65.8 \Omega} = -7.6$$

$$Z_{I(B)} = \beta r_e' = 100 \times 65.8 = 6580 \Omega = 6.58 \text{ K}$$

$$Z_{I(T)} = \frac{Z_{I(B)} R_b}{(Z_{I(B)} + R_b)} = \frac{6.58 \times 1.82}{6.58 + 1.82} = 1.43 \text{ K} = 1430 \Omega$$

$$A_I = \frac{-Z_{I(T)}}{r_e'} = \frac{-1430}{65.8} = -21.73$$

$$A_{VS} = \frac{-Z_{I(T)} R_L'}{(R_s + Z_{I(T)}) r_e'} = \frac{(-1430 \times 500)}{(1000 + 1430) \times 65.8} = -4.47$$

$$A_{IS} = \frac{-Z_{I(T)} R_s}{(R_s + Z_{I(T)}) r_e'} = \frac{(-1430 \times 1000)}{(1000 + 1430) \times 65.8} = -8.93$$

Net Power Gain

$$G = A_{VS} \cdot A_{IS} = (-4.47) \times (-8.93) = 39.9$$

Output Voltage

$$v_O = A_{VS} \cdot v_S = -4.47 \times 2 = -8.9 \text{ mV (rms)}$$

( Given  $v_S = 2 \text{ mV (rms)}$  )

Output Power is delivered across the external load resistance  $R_L$

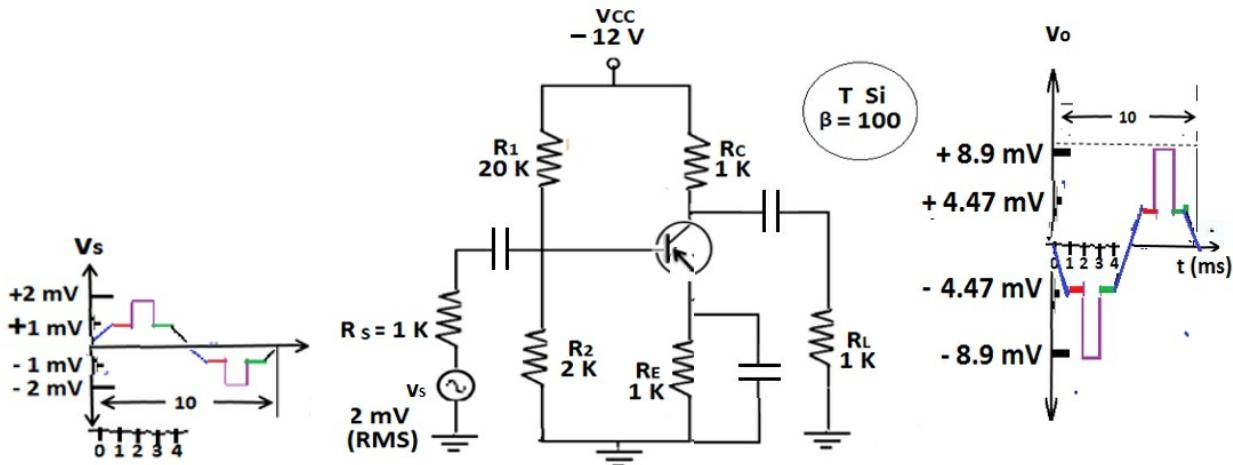
$$\begin{aligned} P_O &= \frac{v_O^2}{R_L} = \frac{0.0089^2}{1000} \\ &= 7.9 \times 10^{-8} \text{ W} = 0.079 \mu \text{W} \end{aligned}$$

## OUTPUT VOLTAGE WAVEFORM

The output voltage is given by  $v_O = A_{VS} \cdot v_S$

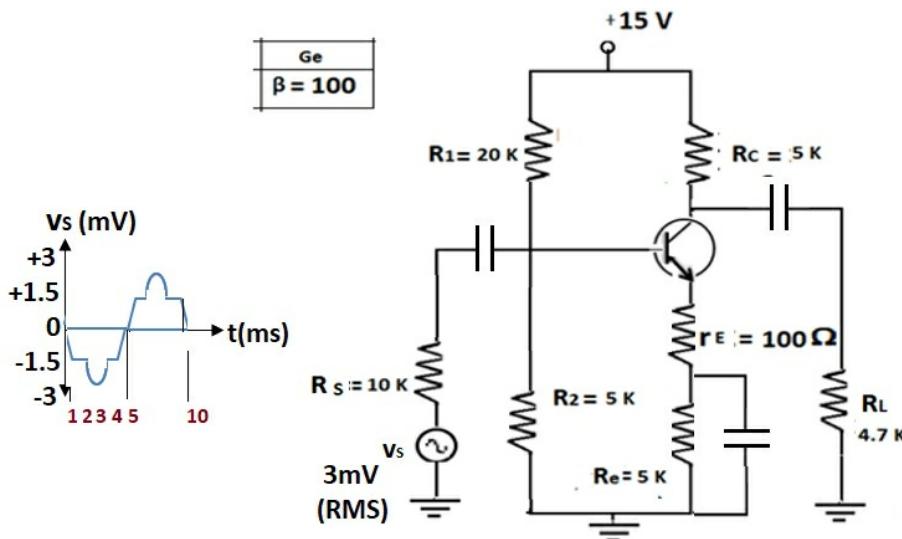
Here  $A_{VS}$  is a negative quantity. The instantaneous output voltage is

obtained by multiplying each of the instantaneous input voltage values with  $A_{VS}$ . This is shown in the figure for the given input signal waveform. During the time interval  $t = 0$  to  $t = 1$  (on the time scale shown in the figure) the Input is ‘**rising**’, shown by the ‘**Blue**’ trace. Since  $A_{VS}$  is negative, the corresponding output during this time interval is ‘**rising**’ in the negative direction, shown by ‘**Blue**’. This correspondence of the output waveform with respect to the input waveform is shown with different colours at the different time intervals on the time scale. Due to the negative sign of  $A_{VS}$  the output voltage appears with a phase shift of  $-180^\circ$ . This phase shift makes the output voltage inverted, as shown in the figure below.

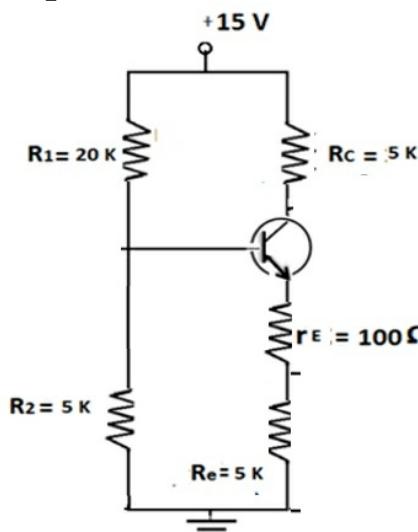


**Output signal is amplified with a voltage gain of “-  $A_{VS}$ ”, which results in a  $-180^\circ$  phase difference between input and output voltages. In other words, the output voltage waveform is inverted.**

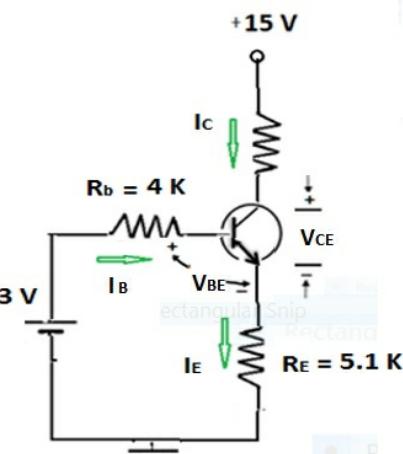
**EXAMPLE 3** – Evaluate the Output Voltage, Output Power, Voltage Gain, Current Gain, and Power gain for the amplifier with ‘Emitter Swamping Resistance’. The transistor is made of Ge. (Demonstrates that the same set of formulae are applicable, as in the case of Si transistors)



### DC Analysis: -- DC Equivalent Circuit



DC Equivalent Circuit



Thevenin's Equivalent

$R_E$  consists of **the series** the  $100\ \Omega$  and  $5\ K$ , thus

$$R_E = 5.1\ K.$$

Thevenizing the Base Emitter circuit of this we get the circuit alongside.

Here

$$V_2 = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{5 \times 15}{5+15} = 3 \text{ V} \quad \& \quad R_b = \frac{R_1 R_2}{R_1 + R_2} = \frac{5 \times 20}{5+20} = 4\text{K} = 4000 \Omega$$

From the KVL equation of the base-emitter loop we get the equation for  $I_B$  as

$$I_B = \frac{(V_2 - V_{BE})}{(R_b + (1+\beta)R_E)}$$

This is a Ge transistor, hence  $V_{BE} = 0.3 \text{ V}$  and  $\beta = 100$  (Given)

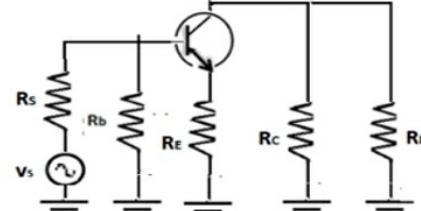
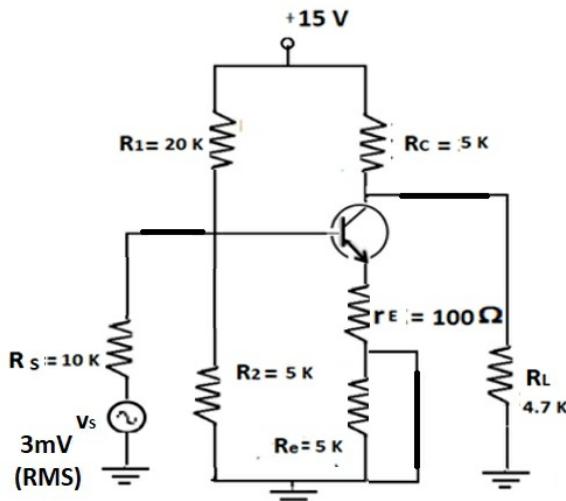
$$I_B = \frac{(3-0.3)}{(4+(1+100)\times 5.1)} = 0.005 \text{ mA}$$

$$I_C \approx I_E = \beta I_B = 100 \times 0.005 = 0.5 \text{ mA}$$

$$\therefore r_e' = \frac{25}{I_E \text{ mA}} = \frac{25}{0.5} = 50 \Omega$$

## AC Analysis

### AC Equivalent Circuit



AC EQUIVALENT CIRCUIT

**ALL CAPACITORS ARE  
SHORT CIRCUTED**

The transistor is replaced by the r-parameter model.

Referring to the AC Equivalent Circuit in the figure below, and using the formulae –

$$1. A_v = \frac{-R'_L}{(r'_e + r_E)}$$

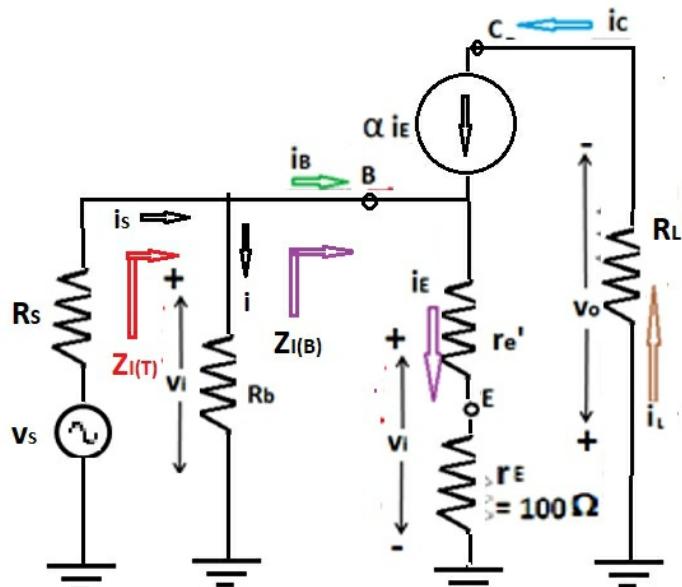
$$\text{Where } R'_L = R_C \parallel R_L = 5 \text{ K} \parallel 4.7 \text{ K} = \frac{5 \times 4.7}{(5+4.7)}$$

$$R'_L = 2.4 \text{ K}$$

Using the value of  $r'_e = 50 \Omega$  calculated in the DC Analysis and taking

$$r_E = 100 \Omega$$

$$A_v = \frac{-2400}{(50+100)} = -16$$



$$2. Z_{I(B)} = \beta (r'_e + r_E) = 100 \times (50 + 100)$$

$$Z_{I(B)} = 15000 \Omega = 15 \text{ K}$$

$$3. Z_{I(T)} = R_b \quad | \quad Z_{I(B)} = 4 \quad | \quad 15 = \frac{4 \times 15}{(4+15)}$$

$$Z_{I(T)} = 3.16 \text{ K} = 3160 \Omega$$

$$4. A_I = \frac{-Z_{I(T)}}{(r_e' + r_E)} = \frac{-3160}{(50+100)}$$

$$A_I = -21$$

### NET VOLTAGE GAIN AND NET CURRENT GAIN:

$$A_{VS} = \frac{Z_{I(T)}}{(R_S + Z_{I(T)})} \times A_V$$

$$A_{IS} = \frac{R_S}{(R_S + Z_{I(T)})} \times A_I \quad |$$

$Z_{I(T)}$  is the “Net Input Impedance.

Substituting we have—

$$A_{VS} = \frac{3.16}{(10+3.16)} \times (-16) = -3.84$$

$$A_{IS} = \frac{10}{(10+3.16)} \times (-21) = -15.95$$

$$\begin{aligned} \therefore V_{O(rms)} &= |A_{VS}| \cdot V_S \\ &= |-3.84| \times 3 = 11.52 \text{ mV (rms)} \end{aligned}$$

Output Power is developed across the external load resistance  $R_L$

$$\therefore P_O = \frac{V_{O(rms)}^2}{R_L}$$

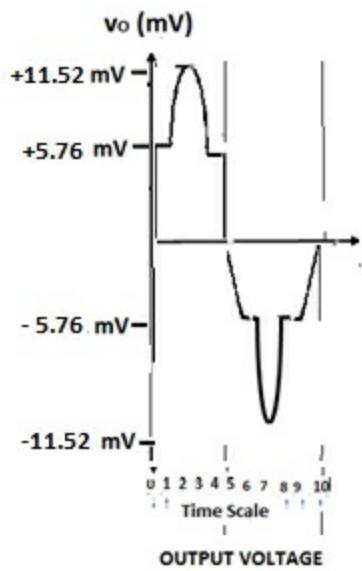
Where  $V_{O(rms)} = 11.52 \text{ mV} = 0.01152 \text{ V}$  and  $R_L = 4.7 \text{ K} = 4700 \Omega$

OR

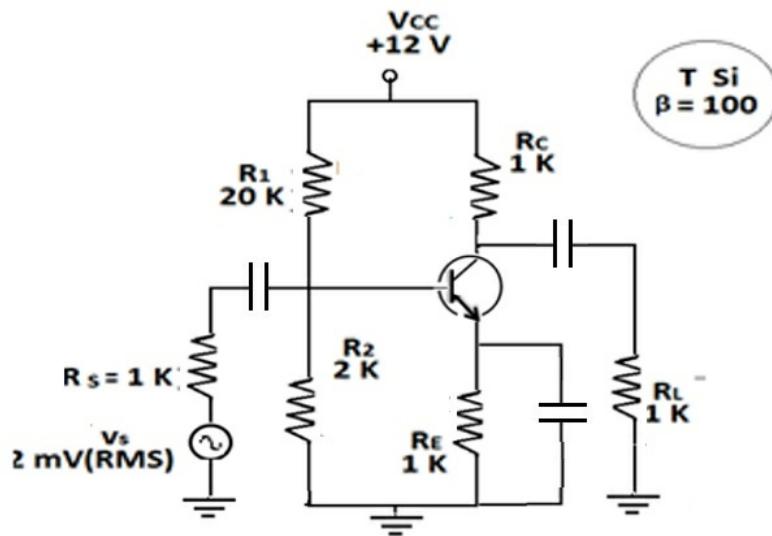
$$P_O = \frac{0.01152^2}{4700} = 2.8 \times 10^{-8} \text{ W}$$

### Output Voltage Waveform

- When instantaneous Input Voltage is 1.5 mV the instantaneous Output Voltage is  $-3.84 \times 1.5 = -5.76 \text{ mV}$
- When instantaneous Input Voltage is 3 mV the instantaneous Output Voltage is  $-3.84 \times 3 = -11.52 \text{ mV}$
- When instantaneous Input Voltage is  $-1.5 \text{ mV}$  the instantaneous Output Voltage is  $+5.76 \text{ mV}$  and when instantaneous Input Voltage is  $-3 \text{ mV}$  the instantaneous Output Voltage is  $+11.52 \text{ mV}$



**Example 4: - (Effect of temperature):** -- Repeat Example – 1 when the room temperature is (a)  $5^{\circ}\text{C}$  and (b)  $40^{\circ}\text{C}$ .



**SOLUTION ::**

a) Room temperature 5°C

At 5°C we get  $T = 273 + 5 = 278\text{K}$

$$\therefore V_T = \frac{278}{11600} = 0.024\text{V} = 24\text{mV}$$

DC Analysis of the given amplifier circuit resulted in the value of  $I_E$  as (as solved in the previous example )

$$I_E = 0.38\text{mA}$$

$$\therefore r_e' = \frac{24(\text{mV})}{0.38(\text{mA})} = 63\Omega$$

Using the results of the AC Analysis of the previous example and substituting in the expressions for  $A_V$ ,  $Z_{I(B)}$ ,  $Z_{I(T)}$  and  $A_I$  we have

$$A_V = \frac{-R_L}{r_e'} = \frac{-500\Omega}{63\Omega} = -7.9$$

$$Z_{I(B)} = \beta r_e' = 100 \times 63 = 6300\Omega = 6.3\text{K}$$

$$Z_{I(T)} = \frac{Z_{I(B)} R_b}{(Z_{I(B)} + R_b)} = \frac{6.3 \times 1.82}{6.3 + 1.82} = 1.41\text{K} = 1410\Omega$$

$$A_I = \frac{-Z_{I(T)}}{r_e'} = \frac{-1410}{63} = -22.4$$

(b) Room temperature 40°C

Repeating the calculations for 40°C we have

At 40°C we get  $T = 273 + 40 = 313\text{K}$

$$\therefore V_T = \frac{313}{11600} = 0.027\text{V} = 27\text{mV}$$

DC Analysis of the given amplifier circuit resulted in the value of  $I_E$  as (as solved in the previous example )

$$I_E = 0.38\text{mA}$$

$$\therefore r_e' = \frac{27(\text{mV})}{0.38(\text{mA})} = 71\Omega$$

Using the results of the AC Analysis of the previous example and substituting in the expressions for  $A_V$ ,  $Z_{I(B)}$ ,  $Z_{I(T)}$  and  $A_I$  we have

$$A_V = \frac{-R_L}{r_e} = \frac{-500 \Omega}{71 \Omega} = -7$$

$$Z_{I(B)} = 6 r_e' = 100 \times 71 = 7100 \Omega = 7.1 K$$

$$Z_{I(T)} = \frac{Z_{I(B)} R_b}{(Z_{I(B)} + R_b)} = \frac{7.1 \times 1.82}{7.1 + 1.82} = 1.45 K = 1450 \Omega$$

$$A_I = \frac{-Z_{I(T)}}{r_e'} = \frac{-1450}{71} = -20.4$$

**CONCLUSION:** -- Comparing the results of the calculations in the Part (a) and Part (b) we observe that the performance of the amplifier is dependent on the room temperature.

This is made clearer with the help of the table below.

**Table -1**

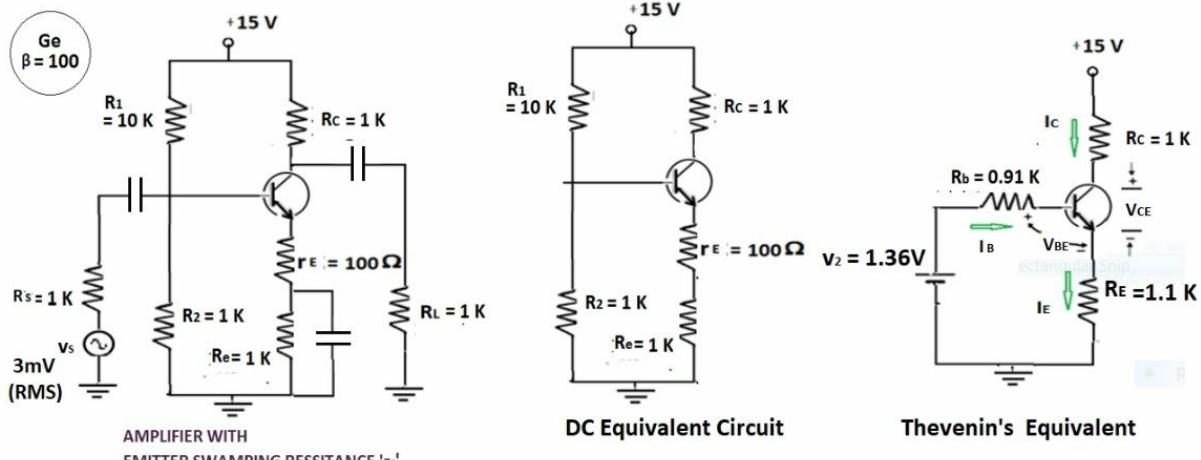
	$A_V$	$Z_{I(B)}$	$Z_{I(T)}$	$A_I$
5°C	-7.9	6.3 K	1.4 K	-22.9
40°C	-7	7.1 K	1.45 K	-20.4

**REMEDY:** -- The effect of temperature variation is overcome with the use of the '**Emitter Swamping Resistance**',  $r_E$  such that

$$r_E \gg r_e'$$

which is a physical resistance of a value much larger than the Forward Bias Resistance of the Emitter-Base junction. The **Performance Stabilizing** effect of  $r_E$  is understood by means of the following example.

**Example – 5:** -- (**use of emitter swamping resistance**) Using the amplifier circuit shown in the figure, show that performance of the amplifier remains nearly constant at room temperatures of (a) 300°K (b) 5°C and (c) 45°C due to the use of the Emitter Swamping Resistance  $r_E = 100 \Omega$



### SOLUTION :: DC ANALYSIS

The net resistance at the Emitter terminal is

$$R_E = R_e + r_E$$

From the values of  $R_E$  and  $r_E$  given in the circuit we have

$$R_E = 1 \text{ K} + 100 \Omega = 1.1 \text{ K}$$

Thevenizing the Base-Emitter loop, and using Eq.- 1 to Eq- 4, we have -

$$V_2 = \frac{R_2 V_{CC}}{(R_1 + R_2)} = \frac{1 \times 15}{1+15} = 1.36 \text{ V}$$

$$R_b = \frac{R_1 R_2}{(R_1 + R_2)} = \frac{1 \times 10}{1+10} = 0.91 \text{ K}$$

$$I_B = I_{BQ} = \frac{V_2 - V_{BE}}{\{R_b + (1+\beta)R_E\}}$$

Given that we have Ge Transistor having  $\beta = 100$ , since, for Ge,  $V_{BE} = 0.3 \text{ V}$ , substituting

$$I_{BQ} = \frac{1.36 - 0.3}{\{0.91 + (1+100) \cdot 1.1\}} = 0.0094 \text{ mA}$$

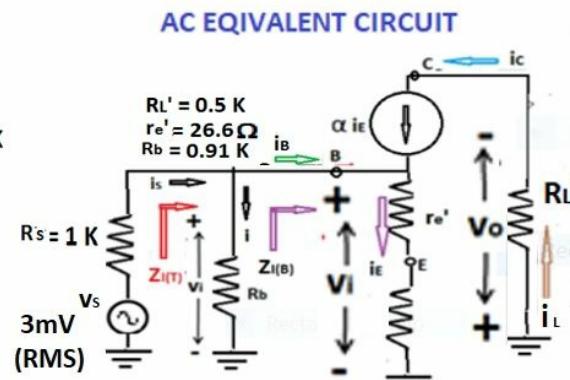
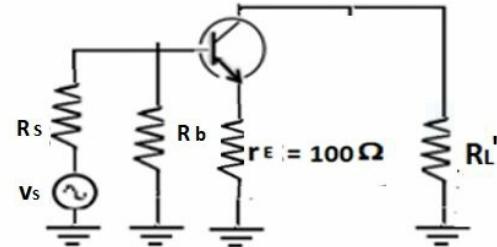
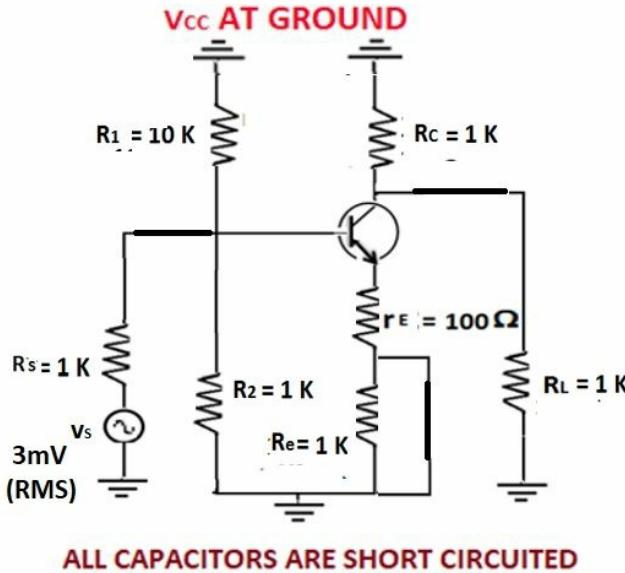
$$I_E \approx I_{CQ} = \beta I_{BQ} = 100 \times 0.0094 = 0.94 \text{ mA}$$

At a room temperature of  $300^{\circ}\text{K}$  the **r-parameter** of the transistor,  $r_e'$  is given by

$$r_e' = \frac{25}{I_E (\text{mA})} = \frac{25}{0.94} = 26.6 \Omega$$

## AC ANALYSIS

Using the steps of AC Analysis and Eq. 5 to Eq. 10 for the AC Equivalent Circuit we obtain  $A_V$ ,  $A_I$  and  $Z_I$ . as follows-



$$A_V = \frac{-R_{L'}}{(r_{e'} + r_E)} = \frac{-500}{(26.6 + 100)} = -3.9$$

$$(\text{Using Approx. formula } A_V = \frac{-R_{L'}}{r_E} = \frac{-500}{100} = -5)$$

$$\begin{aligned} Z_{I(B)} &= \beta(r_e' + r_E) \\ &= 100 \times (26.6 + 100) \\ &= 12660 \Omega = 12.66 \text{ K} \end{aligned}$$

(Using Approx. formula )

$$Z_{I(B)} = \beta \cdot r_E = 100 \times 100 = 10000 = 10 \text{ K}$$

$$Z_{I(T)} = \frac{12.66 \times 0.91}{12.66+0.91} = 0.85 \text{ K} = 850 \Omega$$

(Using Approx. value)

$$Z_{I(T)} = \frac{10 \times 0.91}{10+0.91} = 0.834 \text{ K}$$

$$A_I = \frac{-Z_{I(T)}}{(r_e' + r_E)} = \frac{-850}{(26.6+100)} = -6.71$$

$$(Using \text{ Approx. formula } A_I = \frac{-Z_{I(T)}}{r_E} = \frac{-834}{100} = -8.34)$$

### Check For Effect of Temperature Variation

#### (b) Room temperature 5°C

At 5°C we get T = 273 + 5 = 278°K

$$\therefore V_T = \frac{278}{11600} = 0.024 \text{ V} = 24 \text{ mV}$$

DC Analysis of the given amplifier circuit resulted in the value of I<sub>E</sub> as

$$I_E = 0.94 \text{ mA}$$

$$\therefore r_e' = \frac{24 \text{ (mV)}}{0.94 \text{ (mA)}} = 25.5 \Omega$$

Using the results of the AC Analysis of the previous example and substituting in the expressions for A<sub>V</sub>, Z<sub>I(B)</sub>, Z<sub>I(T)</sub> and A<sub>I</sub> we have

$$A_V = \frac{-R_L'}{(r_{e'} + r_E)} = \frac{-500}{(25.5+100)} = -3.98$$

$$\begin{aligned} Z_{I(B)} &= \beta (r_e' + r_E) = 100 \times (25.5 + 100) \\ &= 12550 \Omega = 12.55 \text{ K} \end{aligned}$$

$$Z_{I(T)} = \frac{12.55 \times 0.91}{12.55+0.91} = 0.85 \text{ K} = 848 \Omega$$

$$A_I = \frac{-Z_{I(T)}}{(r_e' + r_E)} = \frac{-848}{(25.5+100)} = -6.76$$

(c) Room temperature 40°C

Repeating the calculations for 40°C we have

At 40°C we get  $T = 273 + 40 = 313^\circ\text{K}$

$$\therefore V_T = \frac{313}{11600} = 0.027 \text{ V} = 27 \text{ mV}$$

DC Analysis of the given amplifier circuit resulted in the value of  $I_E$  as

$$I_E = 0.94 \text{ mA}$$

$$\therefore r_e' = \frac{27 \text{ (mV)}}{0.94 \text{ (mA)}} = 28.7 \Omega$$

Using the results of the AC Analysis of the previous example and substituting in the expressions for  $A_V$ ,  $Z_{I(B)}$ ,  $Z_{I(T)}$  and  $A_I$  we have

$$A_V = \frac{-R_L'}{(r_e' + r_E)} = \frac{-500}{(28.7+100)} = -3.88 \quad |$$

$$\begin{aligned} Z_{I(B)} &= \beta (r_e' + r_E) = 100 \times (28.7 + 100) \\ &= 12660 \Omega = 12.87 \text{ K} \end{aligned}$$

$$Z_{I(T)} = \frac{12.87 \times 0.91}{12.87+0.91} = 0.8499 \text{ K} = 849.9 \Omega$$

$$| \quad A_I = \frac{-Z_{I(T)}}{(r_e' + r_E)} = \frac{-849.9}{(28.7+100)} = -6.6$$

For the purpose of comparison, we can tabulate these results as follows.

**Table -2**

	$A_I$	$Z_{I(B)}$	$Z_{I(T)}$	$A_V$
27°C	-3.9	12.6 K	850 Ω	-6.71
5°C	-3.98	12.55 K	848 Ω	-6.76
40°C	-3.88	12.87 K	849.9 Ω	-6.6

**CONCLUSION:** -- Comparing the performance of the amplifier at the three different temperatures of (a) 17° C, (b) 5° C and (c) 40° C, we observe that the performance remains nearly constant. Whereas, in case of the Example- 4 when the **Emitter Swamping Resistance** was not present, the performance showed wide variation with respect to temperature variations.

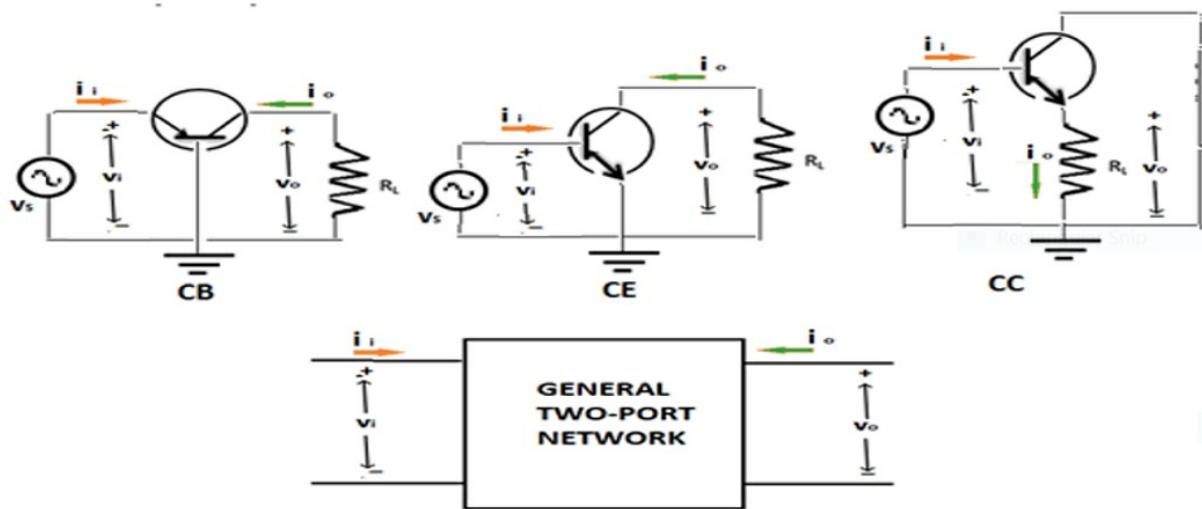
## Section - 2

### BJT Amplifier analysis by h-Parameter Model

#### 6.4 The h-Parameter Model of Transistor

- The h-parameter model is very commonly used Small Signal Model. It can be used to analyze the entire range of performance characteristics of the BJT amplifiers.
- There are four “hybrid Parameter” quantities associated with each of the amplifier configurations of a BJT.
- These can be either obtained from the Input and Output characteristics of the device, or they can be measured using certain circuits which can be set up in a lab, or, by using a set of conversion formulae.
- In general, the device manufacturer provides the set of h-parameter values of usually the Common Emitter configuration in Data Sheets. Any user may then use these values and convert them to the required configuration.

- In each of the transistor configurations, namely, CB CE & CC, can be considered as “Two-Port Networks”. A Two-Port Network can be described by a set of four variables, namely Input voltage  $v_i$ , Input Current  $i_i$ , Output Voltage  $v_o$  and Output Current  $i_o$ . This is shown in Fig.-10.



**Fig.-10**

- Assume that the Two-Port Network does not contain any reactive elements.
- We let the Input Current  $i_i$  and Output Voltage  $v_o$  as Independent Variables and Input Voltage  $v_i$  and Output Current  $i_o$  as Dependent Variables.
- Then the Two-Port Network can be described by a set of equations as follows.

$$v_i = h_{11} i_i + h_{12} v_o \quad \dots(1(a))$$

$$i_o = h_{21} i_i + h_{22} v_o \quad \dots(1(b))$$

The coefficients of these equations are as follows

- a)  $\mathbf{h}_{11} = \mathbf{h}_i = \left[ \frac{v_i}{i_i} \right]_{v_o=0}$   
     i.e., "input impedance" when output port is short circuited.
- b)  $\mathbf{h}_{12} = \mathbf{h}_r = \left[ \frac{v_i}{v_o} \right]_{i_i=0}$   
     i.e., "reverse voltage ratio" when input port is open circuited.
- c)  $\mathbf{h}_{21} = \mathbf{h}_f = \left[ \frac{i_o}{i_i} \right]_{v_o=0}$   
     i.e., "forward current ratio" when output terminal is short circuited.
- d)  $\mathbf{h}_{22} = \mathbf{h}_o = \left[ \frac{i_o}{v_o} \right]_{i_i=0}$   
     i.e., "output admittance" when input port is open circuited.

These quantities  $\mathbf{h}_i$ ,  $\mathbf{h}_r$ ,  $\mathbf{h}_f$  and  $\mathbf{h}_o$  are called the **hybrid Parameters** or **h-parameters of the Two-Port Network**.

Using these the equation 1(a) and 1(b) can be rewritten as follows--

$$v_i = h_i i_i + h_r v_o \quad \dots(1(c))$$

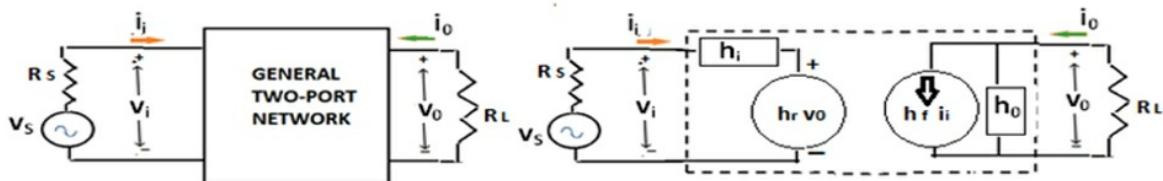
$$i_o = h_f i_i + h_o v_o \quad \dots(1(d))$$

- In the Eq. 1(c), the first term represents a voltage dropped across an impedance ' $h_i$ ' due to a current ' $i_i$ ' flowing through it. The second term represents a voltage proportional to the output voltage  $v_o$ , since the quantity ' $h_r$ ' is dimensionless (i.e. since it represents a ratio). Thus, this term represents a 'Voltage Source'.
- The sum of these two terms gives the voltage across the input terminals. Thus, this expression gives the expression for 'Kirchhoff's Voltage Law' applied to the Input Port. In other words, the Eq. 1 (c) represents the expression corresponding to the **Thevenin's Equivalent of the Input Port**.
- In the Eq. 1(d), the second term represents a current flow through an admittance ' $h_o$ ' due to a voltage ' $v_o$ ' appearing across it. The first term represents a current proportional to the input current ' $i_i$ ', since the quantity ' $h_f$ ' is dimensionless (i.e. since it represents a ratio). Thus, this term represents a 'Current Source'.
- The sum of these two terms gives the **current flowing into the output port**. Thus, this expression gives the expression for 'Kirchhoff's Current Law' applied to the output Port. In other words, the Eq. 1 (d) represents the expression corresponding to

the Norton's Equivalent of the Output Port.

- Thus, the General Two-Port Network may be redrawn as in the Fig- 11.

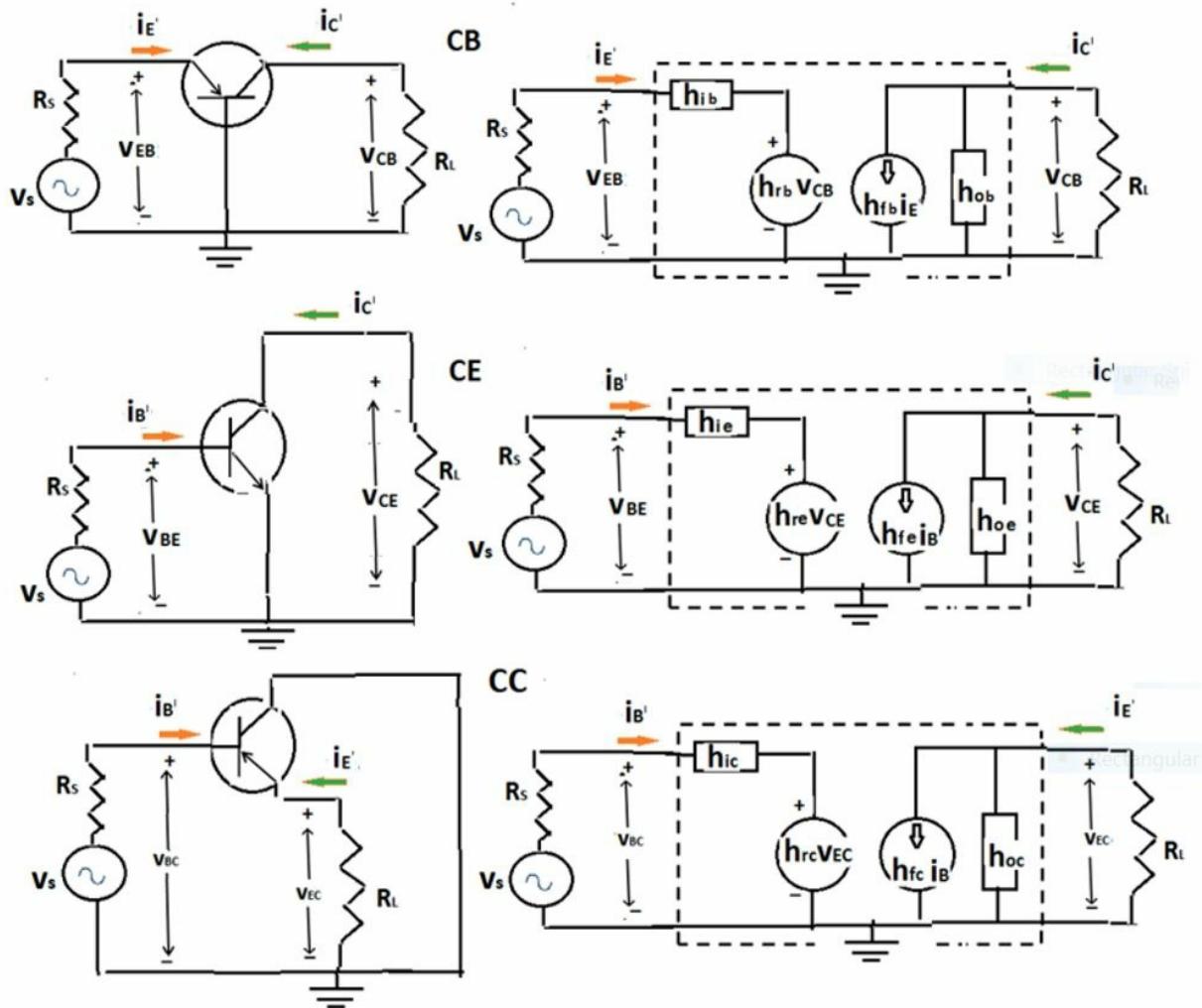
**This is the h-parameter equivalent circuit model of a General Two-Port Network.**



**Fig.-11: General Two-Port Network and General h-parameter model.**

Since the three transistor amplifier configurations are also Two-Port Networks, hence these too can be represented by the h-Parameter Model as shown in the Fig- 10 and Fig.-11. It is **to be noted that, when the amplifier is in a certain specified configuration, the h-parameters appear with a second subscript denoting the configuration.**

1. Thus, **in case of CB configuration**, the second subscript is 'b' e.g.  $h_{ib}$ ,  $h_{rb}$ ,  $h_{fb}$  and  $h_{ob}$ .
2. In case of **CE configuration**, the second subscript is 'e' e.g.,  $h_{ie}$ ,  $h_{re}$ ,  $h_{fe}$  and  $h_{oe}$ .
3. **In case of CC configuration, the second subscript is 'c'** e.g.  $h_{ic}$ ,  $h_{rc}$ ,  $h_{fc}$  and  $h_{oc..}$ .



**Fig.- 12 : The Three Transistor Configurations and their respective h-parameter models.**

### Determination of h – parameters

- Determination of h-parameters from transistor characteristics.
- Determination of h-parameters using specialized circuits.
- Determination of h-parameters using conversion formulae.

#### 1. Determination of h-parameters from transistor characteristics.

- The Input and output characteristics of a transistor describe the manner in which the voltages and currents behave at the input and output terminals respectively. The transistor amplifier in each of the three configurations is described by means of an h-parameter

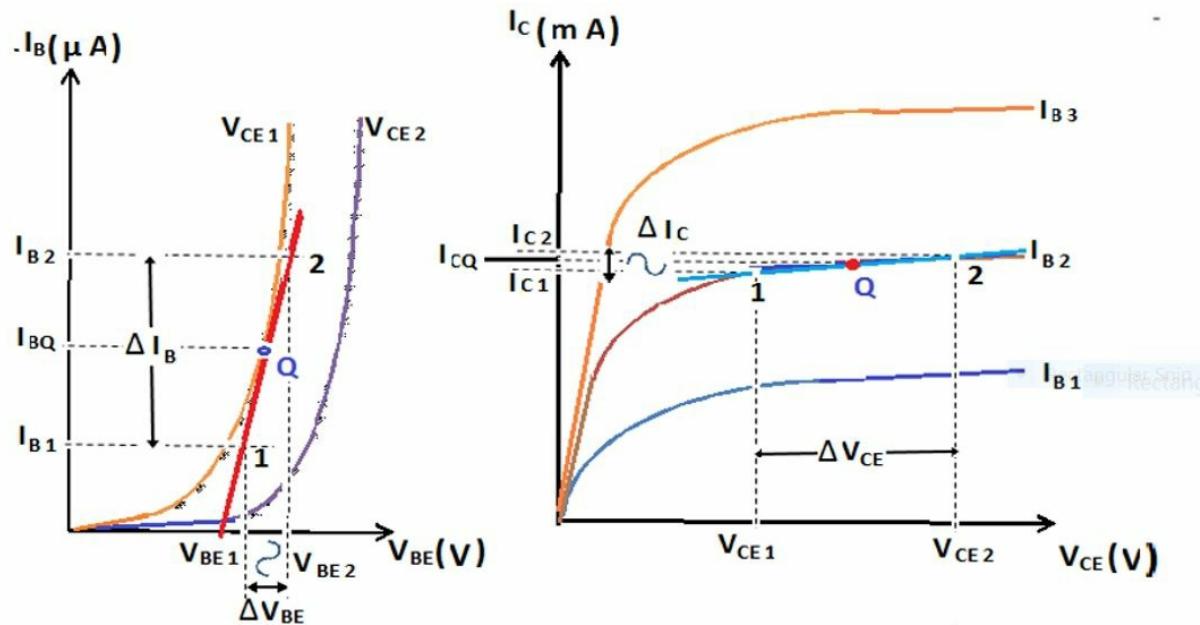
model. Thus, the h-parameter values can be evaluated from the Input and Output characteristics of the transistor.

- Consider the Common Emitter configuration. The set of h-parameters of the **CE configuration** are denoted by  $h_{ie}$ ,  $h_{re}$ ,  $h_{fe}$  and  $h_{oe}$ . The h-parameter model of the CE configuration is given in Fig – 3.. The set of equations that describe the h-parameter model are given by the set of equations Eq. – 1. For CE Configuration, these equations are modified as—

$$v_{BE} = h_{ie} i_B + h_{re} v_{CE} \dots (2. (a))$$

$$i_C = h_{fe} i_B + h_{oe} v_{CE} \dots (2. (b))$$

- These the currents and voltages in the Eq. - 2 are AC quantities. AC quantities are oscillations, between two constant levels (DC levels), about a mean value. That mean value is nothing but the Q – Point.



**Fig – 13.**

### Evaluation of $h_{ie}$ and $h_{oe}$

In terms of Eq. – 2 the definitions of the h-parameters  $h_{ie}$  and  $h_{oe}$  are –

$$h_{ie} = \left[ \frac{v_{BE}}{i_B} \right]_{v_{CE}=0} \quad \dots (3. (a))$$

i.e. “input impedance”

$$h_{oe} = \left[ \frac{i_C}{v_{CE}} \right]_{i_B=0} \quad \dots (3. (b))$$

i.e., “output admittance”

- In order to evaluate  $h_{ie}$  a tangent is drawn on the Input characteristic for the Collector Bias of  $V_{CE1}$ , at a point Q. Two points ‘1’ and ‘2’ are marked on the tangent, which are equidistant from Q. The x-coordinates and y-coordinates of these two points are  $V_{BE1}$  and  $V_{BE2}$ , and  $I_{B1}$  and  $I_{B2}$  respectively. The oscillation  $\Delta V_{BE}$  between  $V_{BE1}$  and  $V_{BE2}$  represents the AC input voltage  $v_{BE}$  oscillation  $\Delta I_B$  between  $I_{B1}$  and  $I_{B2}$  represents the AC input current  $i_B$ . Using this

$$h_{ie} = \left[ \frac{v_{BE}}{i_B} \right] = \frac{\Delta V_{BE}}{\Delta I_B}$$

$$h_{ie} = \left\{ \frac{(V_{BE2} - V_{BE1})}{(I_{B2} - I_{B1})} \right\} \quad \dots (4.(a))$$

- In order to evaluate  $h_{oe}$  a tangent is drawn on the Output characteristic, at a point Q. Two points ‘1’ and ‘2’ are marked on the tangent, which are equidistant from Q. The x-coordinates and y-coordinates of these two points are  $V_{CE1}$  and  $V_{CE2}$ , and  $I_{C1}$  and  $I_{C2}$  respectively. The oscillation  $\Delta V_{CE}$  between  $V_{CE1}$  and  $V_{CE2}$  represents the AC output voltage  $v_{CE}$  and oscillation of output current  $\Delta I_C$  between  $I_{C1}$  and  $I_{C2}$  represents the AC output current  $i_C$ .

$$h_{oe} = \left[ i_c / v_{CE} \right] = \Delta I_c / \Delta V_{CE}$$

$$h_{oe} = \left\{ \frac{(I_{C2} - I_{C1})}{(V_{CE2} - V_{CE1})} \right\} \quad \dots (4. (b))$$

### Evaluation of $h_{re}$ and $h_{fe}$

From the set of Eq. – 2 the h-parameters  $h_{re}$  and  $h_{fe}$  can be defined as follows—

$$h_{re} = \left[ v_{BE} / v_{CE} \right]_{i_B = 0} \quad i_B = 0 \quad \dots (5.(a))$$

i.e. “reverse voltage ratio”

$$h_{fe} = \left[ i_c / i_B \right]_{v_{CE} = 0} \quad v_{CE} = 0 \quad \dots (5.(b))$$

i.e., “forward current ratio”

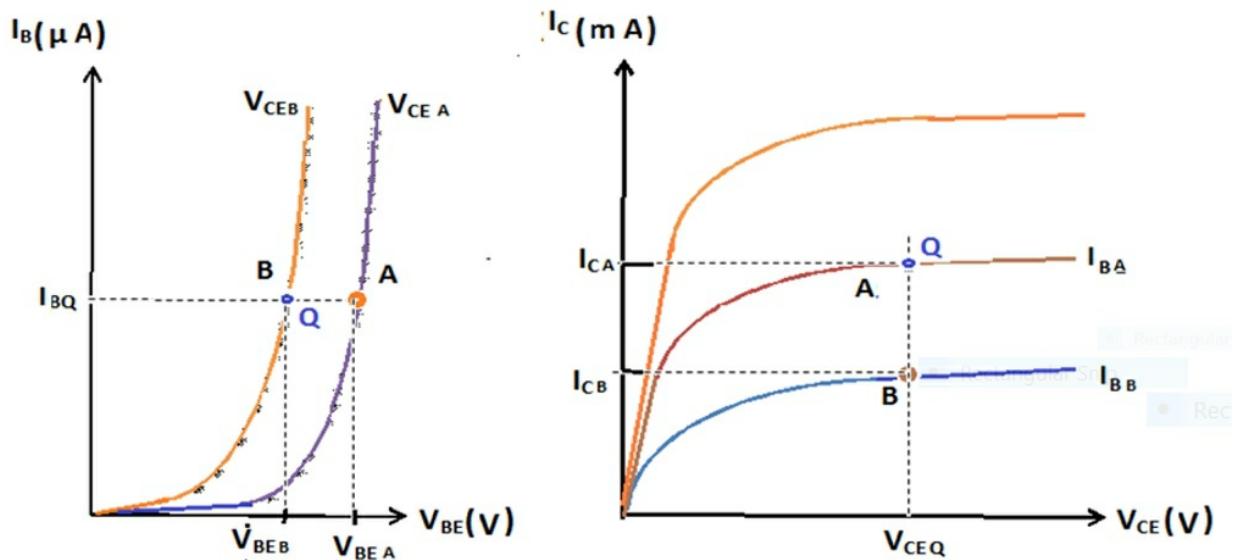
- The parameter  $h_{re}$  is defined at the AC input current  $i_B = 0$ . That means that  $h_{re}$  is the ratio of the incremental quantities  $\Delta V_{BE}$  and  $\Delta V_{CE}$  which is evaluated with the input AC current  $i_B$  is switched off (In which case the transistor is working at the DC Bias Current  $I_{BQ}$ ).
- **In order to evaluate  $h_{re}$  the Input Characteristic is used.** A line, passing through the Q-Point is drawn (At  $I_{BQ}$ ). This line intersects the two Input Characteristic graphs at the points ‘B’ and ‘A’ respectively, whose x-coordinates  $V_{BEB}$  and  $V_{BEA}$ . These two graphs had been plotted with two different values of voltages  $V_{CEB}$  and  $V_{CEA}$  respectively. The AC voltages  $v_{BE}$  and  $v_{CE}$  of the Eq. 5(a) are taken as  $\Delta V_{BE}$  and  $\Delta V_{CE}$  respectively

$$\Delta V_{BE} = V_{BEA} - V_{BEB} \quad \text{AND} \quad \Delta V_{CE} = V_{CEA} - V_{CEB}$$

$$\therefore h_{re} = \left[ \frac{V_{BE}}{V_{CE}} \right] = \frac{\Delta V_{BE}}{\Delta V_{CE}}$$

$$h_{re} = \left\{ \frac{(V_{BEA} - V_{BEB})}{(V_{CEA} - V_{CEB})} \right\} \quad \dots (6.(a))$$

- Similarly, the ratio  $h_{fe}$  is defined as the ratio of the incremental quantities  $\Delta I_C$  and  $\Delta I_B$  which is evaluated with the output AC voltage  $v_{CE}$  is switched off. (In which case the transistor is working at the DC Bias Voltage  $V_{CEQ}$ ).



**Fig – 14**

- In order to evaluate  $h_{fe}$  the Output Characteristic is used. A line, passing through the Q-Point is drawn, ( at  $V_{CEQ}$  ). This line intersects the two of the Output Characteristic graphs at the points 'B' and 'A' respectively. These two graphs had been plotted with two different values of input currents  $I_{BA}$  and  $I_{BB}$  respectively. The corresponding y-coordinates  $I_{CA}$  and  $I_{CB}$  of the points 'A' and 'B' are located. Now, the AC currents  $i_C$  and  $i_B$  of the Eq. 5(b) are taken as  $\Delta I_C$  and  $\Delta I_B$  respectively, where,

$$\Delta I_C = I_{CA} - I_{CB} \quad \text{AND} \quad \Delta I_B = I_{BA} - I_{CB}$$

$$\therefore h_{fe} = \left[ \frac{i_C}{i_B} \right] = \frac{\Delta I_C}{\Delta I_B}$$

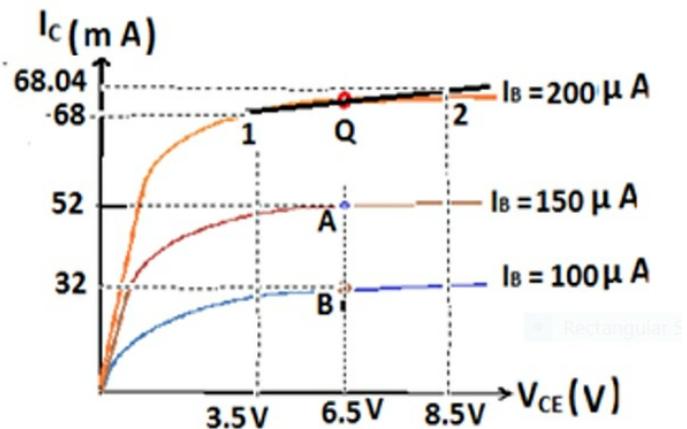
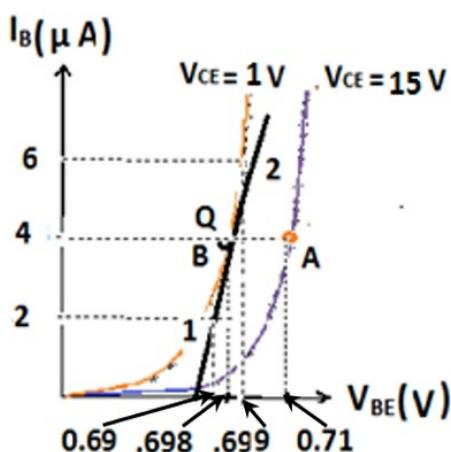
$$h_{fe} = \left\{ \frac{(I_{CA} - I_{CB})}{(I_{BA} - I_{BB})} \right\} \quad \dots (6.(b))$$

*Recall that, since both the Input and Output characteristic graphs consist of parallel traces in the Active Region of the characteristic, it is not necessary to strictly take the Q-Point as the reference point for evaluating the h-parameters. Any point in the Active Region can be taken for this purpose.*

## **TUTORIAL**

**Example 6:** Calculate the four h-parameters of a transistor whose Input and Output Characteristics are shown in the figure below.

**Solution:**



### Evaluation of $h_{ie}$

$h_{ie}$  is evaluated using the Input Characteristic curves.

From Eq. – 4 (a) we have

$$h_{ie} = \frac{(V_{BE\ 2} - V_{BE\ 1})}{(I_{B\ 2} - I_{B\ 1})}$$

From the Input Characteristics, marking the points '1' and '2' on the tangent. The x- and y-coordinates of these two points.

$I_{B\ 2} = 6 \mu A$  and  $I_{B\ 1} = 2 \mu A$ . ;  $V_{BE\ 2} = 0.699 V$  and  $V_{BE\ 1} = 0.69 V$

$$h_{ie} = \frac{(0.699 - 0.69)V}{(6 - 2) \mu A} = \frac{0.009}{4 \times 10^{-6}} \\ = 2250 \Omega = 2.25 K \Omega$$

### Evaluation of $h_{oe}$

$h_{oe}$  is evaluated using the Output Characteristic curves.

From Eq. – 4 (b) we have

$$h_{oe} = \frac{(I_{C\ 2} - I_{C\ 1})}{(V_{CE\ 2} - V_{CE\ 1})}$$

We mark the points '1' and '2' on the tangent drawn on the Output Characteristics. The x- and y-coordinate of these two points.

$I_{C\ 2} = 68.04 m A$  and  $I_{C\ 1} = 68 m A$ . ;  $V_{CE\ 2} = 3.5 V$  and  $V_{CE\ 1} = 8.5 V$

$$h_{oe} = \frac{(68.04 - 68) \text{mA}}{(8.5 - 3.5) \text{V}} = \frac{0.04 \times 10^{-3}}{5} = 8 \times 10^{-6} \text{ mho}$$

### Evaluation of $h_{re}$

$h_{re}$  is evaluated using the Input Characteristic curves. From Eq. – 6 (a) we have

$$h_{re} = \frac{(V_{BEA} - V_{BEB})}{(V_{CEA} - V_{CEB})}$$

Marking the points ‘A’ and ‘B’ on the line passing through the Q-Point, the x-coordinates of these two points

$$V_{CEA} = 15 \text{ V} \text{ and } V_{CEB} = 1 \text{ V} ; V_{BEA} = 0.71 \text{ V} \text{ and } V_{BEB} = 0.698 \text{ V}$$

$$\begin{aligned} h_{re} &= \frac{(0.71 - 0.698) \text{V}}{(15 - 1) \text{V}} \\ &= \frac{0.012}{14} = 8.5 \times 10^{-4} \end{aligned}$$

### Evaluation of $h_{fe}$

$h_{fe}$  is evaluated using the Input Characteristic curves. From Eq. – 6 (b) we have

$$h_{fe} = \frac{(I_{CA} - I_{CB})}{(I_{BA} - I_{BB})}$$

Marking the points ‘A’ and ‘B’ on the line passing through the Q-Point, the y-coordinates of these two points.

$$\begin{aligned} I_{CA} &= 52 \text{ mA} \text{ and } I_{CB} = 32 \text{ mA} ; I_{BA} = 150 \mu\text{A} \text{ and } I_{BB} = 100 \mu\text{A} \\ h_{fe} &= \frac{(52 - 32) \text{mA}}{(150 - 100) \mu\text{A}} = \frac{20 \times 10^{-3}}{50 \times 10^{-6}} = 400 \end{aligned}$$

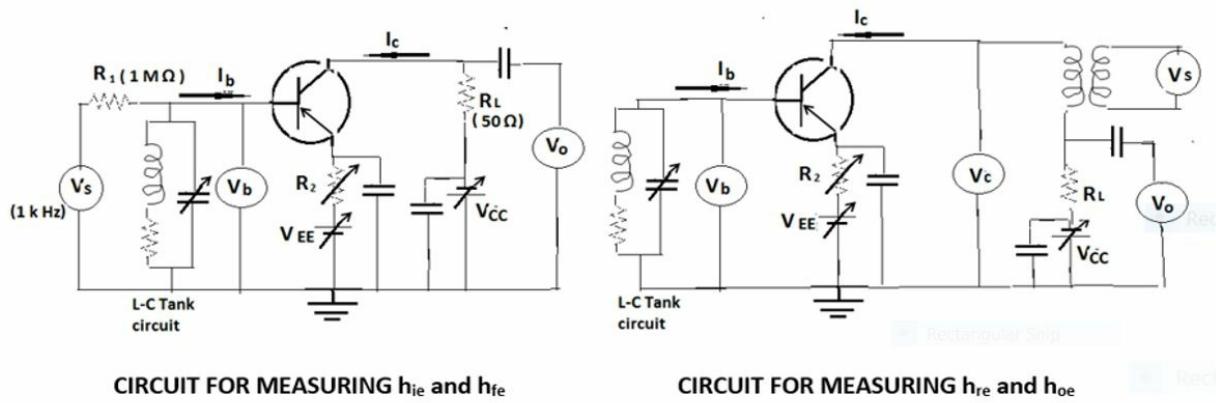
The method described above is also used for the evaluation of h-parameters in other two configurations CB and CC. The Input and Output Characteristic curves in the respective configuration are plotted and the method described above is applied to evaluate the h-parameters in that configuration. If we use the same transistor we get the set of typical values of the h-parameters of all the three configurations. This is tabulated below.

**Table 1:** Table of typical h-parameter values of a transistor in various configurations.

Parameter	CE	CB	CC
$h_i$	$h_{ie} = 2.25 \text{ k}\Omega$	$h_{ib} = 5.6 \Omega$	$h_{ic} = 2.25 \text{ k}\Omega$
$h_r$	$h_{re} = 8.5 \times 10^{-4}$	$h_{rb} = 8 \times 10^{-4}$	$h_{rc} = 1$
$h_f$	$h_{fe} = 400$	$h_{fb} = -0.997$	$h_{fc} = -401$
$h_o$	$h_{oe} = 8 \times 10^{-6} \text{ mhos}$	$h_{ob} = 1.99 \times 10^{-8} \text{ mhos}$	$h_{oc} = 8 \times 10^{-6} \text{ mhos}$

## 2. Determination of h-parameters using specialized circuits.

Certain specialized circuits can be set up in the lab to directly measure the h-parameter values on the basis of their definitions as functions of the various input and output currents and voltages. The required input or output currents or voltages are directly measured. Two of the most commonly used circuits are shown below and the method of evaluation is described.



**Fig – 15:** - Circuits for measuring h-parameters directly.

Recall that the h-parameters are defined under the condition when the AC signal is present and when the transistor is biased in the Active Region. In the two circuits above, the required bias is set-up by means of the DC batteries  $V_{EE}$  and  $V_{CC}$  and by adjusting the resistance  $R_2$ . The AC signal is provided by means of a 1 kHz AC signal source. Two of the h-parameters,  $h_{ie}$  and  $h_{fe}$  are defined

when the output terminal is short circuited. Instead of using a Dead Short Circuit, the short circuit condition is approximated in the first circuit by the use of the very low valued load resistance  $R_L = 50 \Omega$ . Thus, the first circuit is used for the measurement of  $h_{ie}$  and  $h_{fe}$ .

By definition

$$h_{ie} = \left[ \frac{v_b}{i_b} \right]_{v_c=0}$$

i.e., "input impedance" when collector terminal is short circuited.

In the circuit above,

$$I_b = V_s / R_1$$

$$\therefore h_{ie} = \frac{V_b R_1}{V_s}$$

Thus, by measuring  $V_s$  and  $V_b$  the parameter  $h_{ie}$  can be calculated.

By definition

$$h_{fe} = \left[ \frac{i_c}{i_b} \right]_{v_c=0}$$

i.e., "forward current ratio" when collector terminal is short circuited.

where  $I_c = V_o / R_L$  and  $I_b = V_s / R_1$

$$\therefore h_{fe} = \frac{V_o R_1}{V_s R_L}$$

Rectangular Strip

Thus, by measuring  $V_s$  and  $V_o$  the parameter  $h_{fe}$  can be calculated.

The other two h-parameters  $h_{re}$  and  $h_{oe}$  are defined when the input signal current is zero. This condition is set-up in the second circuit by not connecting the signal source at the base terminal. However, to make the signal current available at the collector, the source is coupled to the collector by means of the transformer. Thus, the second circuit can be used for the measurement of  $h_{re}$  and  $h_{oe}$ .

By definition

$$h_{re} = \left[ \frac{v_b}{v_c} \right]_{i_b=0}$$

i.e., "reverse voltage ratio" when input signal current is zero.

Thus, by measuring  $V_b$  and  $V_c$  the parameter  $h_{re}$  can be calculated.

By definition

$$h_{oe} = \left[ \frac{i_c}{v_c} \right]_{i_b=0}$$

i.e., "output admittance" when input signal current is zero

where  $I_c = V_o / R_L$

$$\therefore h_{oe} = \frac{V_o}{V_C R_L}$$

Thus, by measuring  $V_o$  and  $V_C$  the parameter  $h_{oe}$  can be calculated.

### Determination of h-parameters using conversion formulae

We can obtain the conversion formulae for conversion of h-parameter values of one configuration into the other. The complete list of conversion formulae are tabulated in Table – 2. These formulae can be derived as shown with the help of the Example 7 shown below. For this purpose, the h-parameter equivalent model in a certain configuration is **reconfigured** into the configuration, whose conversion formula is required, and the resulting circuit is solved. Figure below shows the h-parameter model of the CB configuration **reconfigured** in CE. When this circuit is solved, we obtain the set of conversion formulae of h-parameters in CE configuration, in terms of the h-parameters of the CB configuration.

**Example 7:** - To Derive the set of conversion formulae for conversion of the h-parameter values in terms of CB configuration into CE configuration.

The figure below shows the CB h-parameter equivalent circuit connected in CE configuration. This figure is used for conversion formulae for  $h_{re}$  and  $h_{oe}$ .

- By definition

$$h_{re} = \left[ \frac{V_{BE}}{V_{CE}} \right]_{iB=0}$$

In the figure (ii),  $V_{BE} = V_{BC} + V_{CE}$

$$\therefore h_{re} = \left[ 1 + \frac{V_{BC}}{V_{CE}} \right]_{iB=0} \quad \text{..... (A)}$$

By Kirchhoff's Current Law at the Node (1)

$$h_{fb} i_E = i_C + i$$

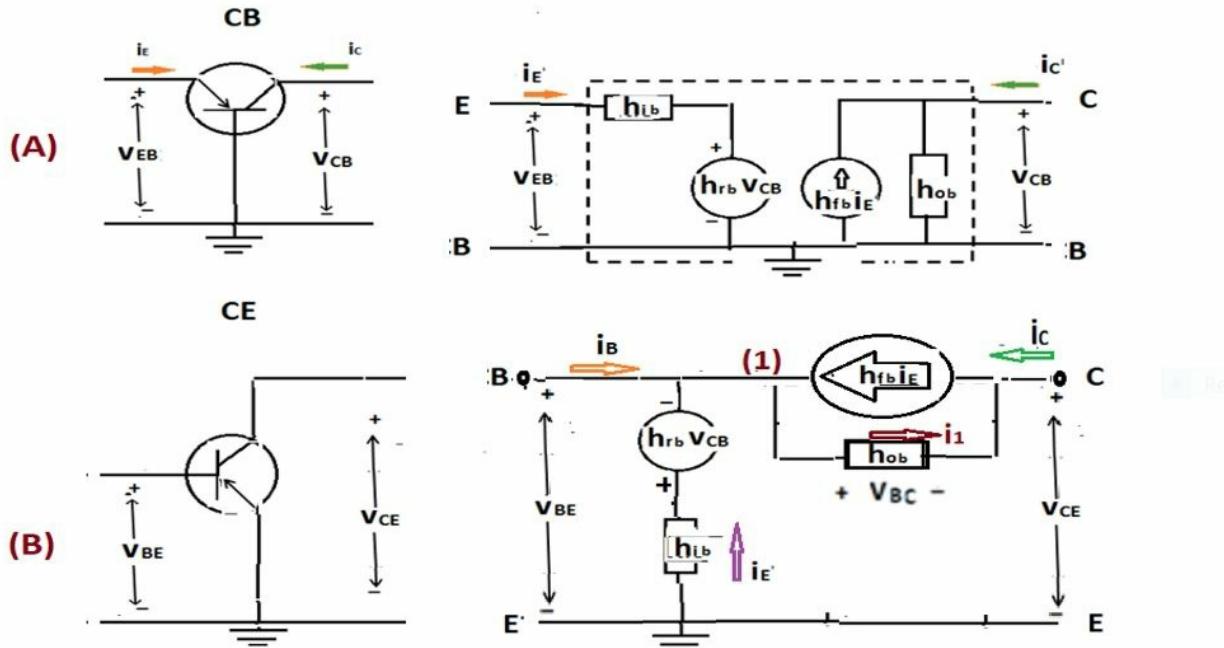
Where 'i' is the current through the admittance 'h<sub>ob</sub>' in the circuit (B) with  $i_B = 0$  we have  $i_C = -i_E$

$$\therefore i = h_{fb} i_E + i_C = (1 + h_{fb}) i_E$$

The voltage across the admittance is  $V_{BC}$

$$\therefore i = h_{ob} V_{BC}$$

$$\therefore h_{ob} V_{BC} = (1 + h_{fb}) i_E \quad \dots(\text{B})$$



**Fig – (a): - Circuit (A) CB configuration and h-parameter model: Circuit (B) CB h-parameter model of transistor RECONFIGURED in CE.**

Applying Kirchhoff's Voltage Law to the output loop we have

$$h_{ib} i_E + h_{rb} V_{CB} + V_{BC} + V_{CE} = 0 \quad \dots(C)$$

From Eq. (B) we have

$$i_E = \frac{h_{ob} V_{BC}}{1 + h_{fb}} \quad \dots(D)$$

Substituting in Eq. (C) we have

$$\frac{h_{ib} h_{ob} V_{BC}}{1 + h_{fb}} - h_{rb} V_{CB} + V_{BC} + V_{CE} = 0$$

Since,  $V_{CB} = -V_{BC}$  we have

$$\left\{ \left( \frac{h_{ib} h_{ob}}{1 + h_{fb}} \right) + (1 - h_{rb}) \right\} V_{BC} + V_{CE} = 0$$

Dividing by  $V_{CE}$  we have

$$\left\{ \frac{h_{ib} h_{ob}}{1 + h_{fb}} + (1 - h_{rb}) \right\} V_{BC} / V_{CE} + 1 = 0$$

$$\therefore \frac{V_{BC}}{V_{CE}} = \frac{-(1 + h_{fb})}{h_{ib} h_{ob} + (1 - h_{rb})(1 + h_{fb})} \quad \dots(E)$$

Substituting in Eq. (A)

$$h_{re} = \left[ 1 + \frac{V_{BC}}{V_{CE}} \right] = \left[ 1 - \frac{(1 + h_{fb})}{h_{ib} h_{ob} + (1 - h_{rb})(1 + h_{fb})} \right]$$

$$\therefore h_{re} = \left[ \frac{h_{ib} h_{ob} + (1 - h_{rb})(1 + h_{fb}) - (1 + h_{fb})}{h_{ib} h_{ob} + (1 - h_{rb})(1 + h_{fb})} \right]$$

$$\text{Or } h_{re} = \left[ \frac{h_{ib} h_{ob} - h_{rb} (1 + h_{fb})}{h_{ib} h_{ob} + (1 - h_{rb})(1 + h_{fb})} \right]$$

Now, referring to the Typical Values of the h-parameters from Table – 5.1. we observe that,

1.  $h_{rb} \ll 1$
2.  $h_{ib} h_{ob} \ll (1 + h_{fb})$

Using these approximations, we get

$$h_{re} = \left\{ \frac{h_{ib} h_{ob}}{1 + h_{fb}} \right\} - h_{rb} \quad \dots(1)$$

- By definition

$$h_{oe} = \left[ \frac{i_c}{V_{CE}} \right]_{i_B=0}$$

From the KCL equation of the Node (1)

$$h_{fb} i_E = i_C + i$$

$$\text{where, } i = h_{ob} V_{BC}$$

$$\therefore i_C = h_{fb} i_E - h_{ob} V_{BC}$$

Substituting for  $i_E$  from Eq. (C) above,

$$i_C = h_{fb} \left( \frac{h_{ob} V_{BC}}{1 + h_{fb}} \right) - h_{ob} V_{BC}$$

$$= h_{ob} V_{BC} \left\{ \frac{h_{fb}}{1 + h_{fb}} - 1 \right\}$$

$$\text{Or } i_C = \frac{-h_{ob} V_{BC}}{1 + h_{fb}} \quad \dots(F)$$

Again, from Eq. (E)

$$V_{CE} = \left[ \frac{-V_{BC} \{ h_{ib} h_{ob} + (1 - h_{rb})(1 + h_{fb}) \}}{(1 + h_{fb})} \right] \quad \dots(G)$$

Substituting Eq. (F) and Eq. (G) in the expression for  $h_{oe}$  we get

$$h_{oe} = \left[ \frac{i_C}{V_{CE}} \right] = \frac{\left\{ -\frac{(h_{ob} V_{BC})}{(1+h_{fb})} \right\}}{-V_{CE} \left[ \left\{ \frac{(h_{ib} h_{ob} + (1-h_{rb})(1+h_{fb}))}{(1+h_{fb})} \right\} \right]}$$

Simplifying

$$h_{oe} = \left\{ \frac{h_{ob}}{h_{ib} h_{ob} + (1-h_{rb})(1+h_{fb})} \right\}$$

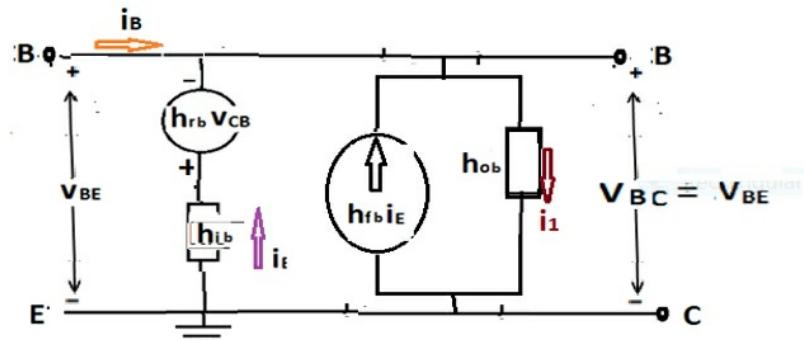
Using the approximations,

i.  $(1 - h_{rb}) \cong 1$

ii.  $h_{ib} h_{ob} \ll 1$

$$h_{oe} = \frac{h_{ob}}{(1+h_{fb})} \quad \dots(2)$$

The remaining two h-parameters  $h_{ie}$  and  $h_{fe}$  are defined with the output terminal short circuited. For this purpose, we need to redraw the **Common Emitter configured CB h-parameter equivalent circuit** with the collector terminal shorted to the grounded emitter terminal. Thus, the circuit is to be modified as shown in the figure below. By using the definitions of the h-parameters and solving the circuit, we obtain the conversion formulae for  $h_{ie}$  and  $h_{fe}$ .



**Fig – (b):** -- The CB h-parameter equivalent circuit is modified by short circuiting the output terminal 'C' being connected to the grounded common terminal 'E'. Thus,  $V_{CE} = 0$

- By definition

$$h_{ie} = \left[ \frac{V_{BE}}{i_B} \right]_{v_{CE}=0}$$

In this circuit,  $V_{BE} = V_{BC} = -V_{CB}$

The KVL equation of the Base – Emitter loop is

$$h_{rb} V_{CB} + h_{ib} i_E = -V_{BE}$$

Using  $V_{CB} = -V_{BE}$  we have

$$h_{ib} i_E + V_{BE} - h_{rb} V_{BE} = h_{ib} i_E + (1 - h_{rb}) V_{BE} = 0$$

$$\therefore i_E = \left\{ \frac{-(1 - h_{rb}) V_{BE}}{h_{ib}} \right\} \quad \dots(H)$$

Now, applying KCL at the Base Node ‘B’ we have

$$i_B + i_E + h_{fb} i_E - i = 0$$

Where ‘ $i_1$ ’ is the current through the admittance  $h_{oe}$

Thus,

$$i = h_{ob} V_{BC}$$

Substituting and simplifying we have

$$i_B + (1 + h_{fb}) i_E = h_{ob} V_{BC}$$

$$\therefore i_B = h_{ob} V_{BC} - (1 + h_{fb}) i_E$$

Substituting for  $i_E$  from Eq. (H) and simplifying

$$i_B = h_{ob} V_{BC} + (1 + h_{fb}) \left\{ \frac{-(1 - h_{rb})V_{BE}}{h_{ib}} \right\} \quad \underline{\dots(1)}$$

Dividing by  $V_{BE}$  and substituting  $V_{BC} = V_{BE}$  we have

$$\frac{i_B}{V_{BE}} = \frac{1}{h_{ie}} = h_{ob} + \left\{ \frac{(1 + h_{fb})(1 - h_{rb})}{h_{ib}} \right\}$$

$$\frac{1}{h_{ie}} = \left[ \frac{(h_{ib} h_{ob}) + (1 + h_{fb})(1 - h_{rb})}{h_{ib}} \right]$$

Or

$$\therefore h_{ie} = \left[ \frac{h_{ib}}{(h_{ib} h_{ob}) + (1 + h_{fb})(1 - h_{rb})} \right]$$

Using the approximations, |

i.  $h_{ib} h_{ob} \ll 1$

ii.  $(1 + h_{fb}) \gg (1 - h_{rb})$

$$h_{ie} = \frac{h_{ib}}{(1 + h_{fb})} \quad \underline{\dots(3)}$$

Rectangular Snip

- By definition

$$h_{fe} = \left[ \frac{i_C}{i_B} \right]_{V_{CE}=0}$$

Where,  $i_C = h_{fb} i_E - i = h_{fb} i_E - h_{ob} V_{BE}$         (with  $V_{BC} = V_{BE}$ )

Substituting for  $i_E$  from Eq. (H) we have

$$i_C = \frac{-h_{fb}(1 - h_{rb})V_{BE}}{h_{ib}} - h_{ob} V_{BE}$$

$$i_C = \frac{-\{h_{fb}(1-h_{rb}) + h_{ib}h_{ob}\}}{h_{ib}} V_{BC}$$

Substituting this equation and substituting for  $i_B$  the Eq. (I) in the definition for  $h_{fe}$  we have

$$h_{fe} = \frac{\left[ \frac{-\{h_{fb}(1-h_{rb}) + h_{ib}h_{ob}\}}{h_{ib}} \right] V_{BC}}{\left[ \frac{\{h_{ib}h_{ob} + (1+h_{fb})(1-h_{rb})\}}{h_{ib}} \right] V_{BE}}$$

Putting  $V_{BE} = V_{BC}$  and simplifying

$$h_{fe} = \left\{ \frac{-\{h_{fb}(1-h_{re}) + h_{ib}h_{ob}\}}{\{h_{ib}h_{ob} + (1+h_{fb})(1-h_{rb})\}} \right\}$$

Using the approximations

- i.  $h_{ib}h_{ob} \ll 1$
- ii.  $(1 + h_{fb}) \gg (1 - h_{rb})$

$$h_{fe} = \frac{-h_{fb}}{(1 + h_{fb})} \quad \dots(4)$$

Rectangular Snip

## Table of Conversion Formulae of h-parameter values

The reader is required to understand that these data pertain to a certain class of transistor. Every class of transistor available in the market will have a typical set of h-parameter values, which need to be evaluated by any of these three methods.

**Table– 2:** - Conversion formulae for h-parameters from one configuration to the other.

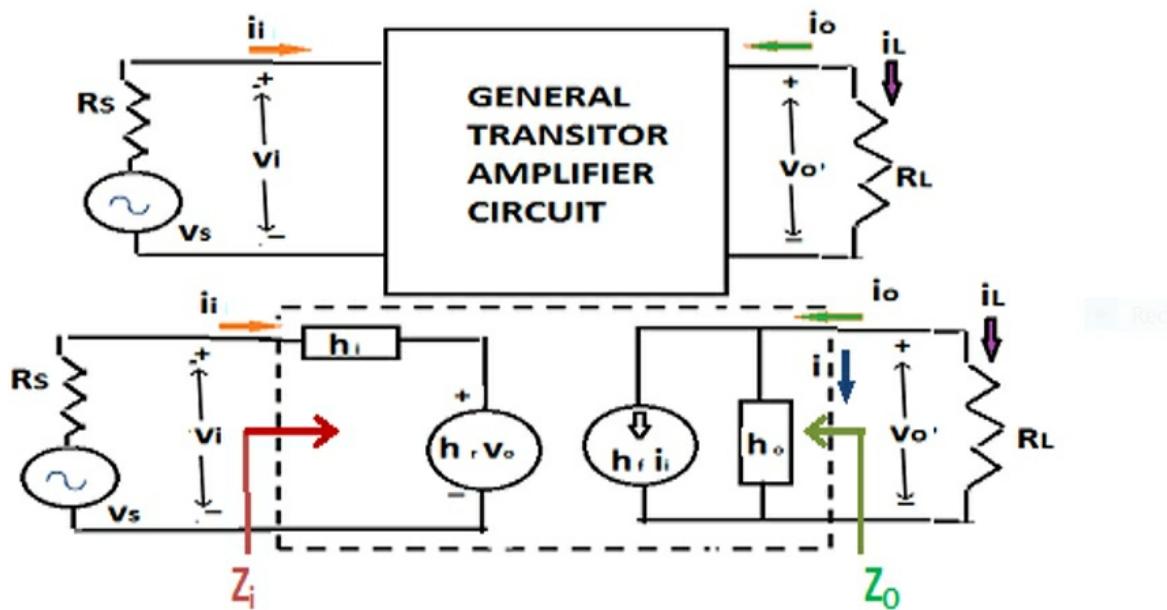
PARAMETER	CE	CB	CC
$h_{ie}$	$2.25 \text{ K}\Omega$	$h_{ib}/(1 + h_{fb})$	$h_{ic}$
$h_{re}$	$8.5 \times 10^{-4}$	$\{h_{ib} h_{ob}/(1 + h_{fb})\} - h_{rb}$	$1 - h_{rc}$
$h_{fe}$	400	$-h_{fb}/(1 + h_{fb})$	$-(1 + h_{fc})$
$h_{oe}$	$8 \times 10^{-6} \text{ mho}$	$h_{ob}/(1 + h_{fb})$	$h_{oc}$
$h_{ib}$	$h_{ie}/(1 + h_{fe})$	$5.6 \Omega$	$\frac{-h_{ic}}{h_{fc}}$
$h_{rb}$	$\{h_{ie} h_{oe}/(1 + h_{fe})\} - h_{re}$	$8 \times 10^{-4}$	$h_{rc} - \{(h_{ic} h_{oc})/h_{fc}\} - 1$
$h_{fb}$	$h_{fe}/(1 + h_{fe})$	- 0.997	$-(1 + h_{fc})$
$h_{ob}$	$h_{oe}/(1 + h_{fe})$	$1.99 \times 10^{-8} \text{ mho}$	$\frac{-h_{oc}}{h_{fc}}$
$h_{ic}$	$h_{ie}$	$h_{ib}/(1 + h_{fb})$	$2.25 \text{ K}\Omega$
$h_{rc}$	$1 - h_{re}$	1	1
$h_{fc}$	$-(1 + h_{fe})$	$-1/(1 + h_{fb})$	- 401
$h_{oc}$	$h_{oe}$	$h_{ob}/(1 + h_{fb})$	$8 \times 10^{-6} \text{ mho}$

## 6.5 Analysis of Transistor Amplifier using h – parameter model

A simplified representation of an amplifier system will be as shown in

the Fig –14, below. Recall that this is of the form of a general Two-Port Network. Hence the amplifier can be replaced by an h-parameter model. Also recall that an amplifier in any of the configurations of the transistor is also a Two-Port Network. Hence the h-parameter model fits all the three configurations

The analysis of the performance of an amplifier is performed by considering the general h-parameter equivalent circuit shown in Fig – 11 earlier. When an amplifier of a certain configuration is to be analyzed, the general h-parameters are replaced with those of the required configuration. The specific h-parameter models of each of the three configurations had been shown in Fig – 12. The Fig – 16, shown below is nothing but the Fig.-11 redrawn for convenience.



**Fig – 16**

### ( i ) Current Gain $A_I$

Current Gain of an amplifier is defined as the ratio of Output Current to Input Current.

$$A_I = \frac{i_L}{i_i} = \frac{-i_o}{i_i}$$

The negative sign in the expression is due to the fact that,  $i_L$  and  $i_o$  are flowing in opposite directions.

$$i_O = h_f i_i + i$$

'i' is the current flowing through the admittance  $h_o$ .

Thus

$$i = h_o V_O$$

Substituting for  $i$  AND Taking

$$v_O = i_L R_L = -i_o R_L$$

$$i_O = h_f i_i + h_o V_O = h_f i_i - h_o i_o R_L$$

$$\therefore h_f i_i = (1 + h_o R_L) i_o$$

$$\therefore A_I = \frac{-i_o}{i_i}$$

$$\therefore A_I = \frac{-h_f}{(1 + h_o R_L)} \quad \dots(1)$$

### (ii) Input Impedance $Z_i$

Input Impedance is defined as

$$Z_i = \frac{V_i}{I_i}$$

Applying KVL at the input terminal we have

$$V_i = h_i i_i + h_r V_o = h_i i_i - h_r i_o R_L \quad (\text{with } V_o = -i_o R_L)$$

Dividing by  $i_i$  we get

$$Z_i = \frac{V_i}{I_i} = h_i - h_r I_o / I_i R_L$$

$$Z_i = h_i + h_r A_I R_L \text{ (with } A_I = -I_o / I_i)$$

$$\therefore Z_i = h_i + h_r A_I R_L \quad \underline{\dots}(2(a))$$

Substituting for  $A_I$  from Eq.1. and simplifying, we have

$$Z_i = h_i - \left\{ h_r \frac{-h_f}{(1+h_o R_L)} \right\} R_L$$

$$Z_i = \left[ \frac{\{h_i + (h_i h_o - h_f h_r) R_L\}}{(1+h_o R_L)} \right]$$

**Putting  $\Delta h = (h_i h_o - h_f h_r)$**

$$Z_i = \left\{ \frac{h_i + \Delta h R_L}{(1+h_o R_L)} \right\} \quad \underline{\dots}(2(b))$$

### (iii) Voltage Gain $A_V$

Voltage Gain of an amplifier is defined as the ratio of Output Voltage to Input voltage.

$$A_V = \frac{V_o}{V_i}$$

We had  $V_o = -I_o R_L$

and

$$A_I = \frac{-I_o}{I_i} \text{ so that, } -I_o = A_I I_i$$

$$\text{Thus } V_o = A_I I_i R_L$$

Substituting for  $V_o$  in the expression for  $A_V$

$$A_V = \frac{A_I I_i R_L}{V_i}$$

$$\text{Where } I_i / V_i = 1 / Z_i$$

$$\therefore A_V = \frac{A_I R_L}{Z_i} \quad \underline{\dots}(3(a))$$

**The quantity  $A_I$  , in Eq. 1 has a Negative Sign. Therefore, the quantity  $A_V$  also will have a Negative Sign.**

Substituting for  $A_I$  and for  $Z_i$  from Eq 1 & 2(b)

$$A_V = \frac{\left[ \frac{-h_f}{(1 + h_o R_L)} R_L \right]}{\left[ \frac{h_i + \Delta h R_L}{(1 + h_o R_L)} \right]}$$

Simplifying,

$$A_V = \left\{ \frac{-h_f R_L}{h_i + \Delta h R_L} \right\} \quad \underline{\underline{(3(b))}}$$

#### (iv) Output Impedance $Z_o$

Output impedance is defined with the source signal at ground  
Thus

$$Z_o = \left[ \frac{v_o}{i_o} \right]_{v_s=0}$$

Where,

$$i_o = h_f i_i + h_o v_o \quad (\text{From a derivation step for } A_I).$$

Dividing by  $v_o$  we have  $Y_o$ , which the output admittance, i.e. reciprocal of  $Z_o$  as

$$Y_o = \frac{i_o}{v_o} = h_o + h_f \left[ \frac{i_i}{v_o} \right]_{v_s=0} \quad \underline{\underline{(A)}}$$

Now, if we take  $v_s = 0$  and write down the KVL equation at the input terminal we get

$$R_s i_i + h_i i_i + h_r v_o = (R_s + h_i) i_i + h_r v_o = 0$$

Dividing throughout by  $v_o$

$$(R_s + h_i) \frac{i_i}{v_o} + h_r = 0$$

$$\therefore \left[ \frac{\mathbf{i}_i}{\mathbf{v}_o} \right]_{v_s=0} = \frac{-\mathbf{h}_r}{(\mathbf{R}_s + \mathbf{h}_i)}$$

Substituting for  $\frac{\mathbf{i}_i}{\mathbf{v}_o}$  in the equation (A) we have

$$Y_o = h_o - \frac{h_f h_r}{(R_s + h_i)}$$

$$Y_o = \frac{(h_o R_s + h_o h_i - h_f h_r)}{(R_s + h_i)}$$

$$Y_o = \left\{ \frac{(h_o R_s + \Delta h)}{(R_s + h_i)} \right\}$$

$$\therefore Z_o = \left\{ \frac{(R_s + h_i)}{(h_o R_s + \Delta h)} \right\} \quad \underline{\dots(4)}$$

### (v) Power Gain G

Power Gain is defined as the ratio of output power  $P_o$  to input power  $P_i$ .

Where  $P_o = v_o i_o$  and  $P_i = v_i i_i$

Thus

$$G = \frac{P_o}{P_i} = \frac{v_o i_o}{v_i i_i}$$

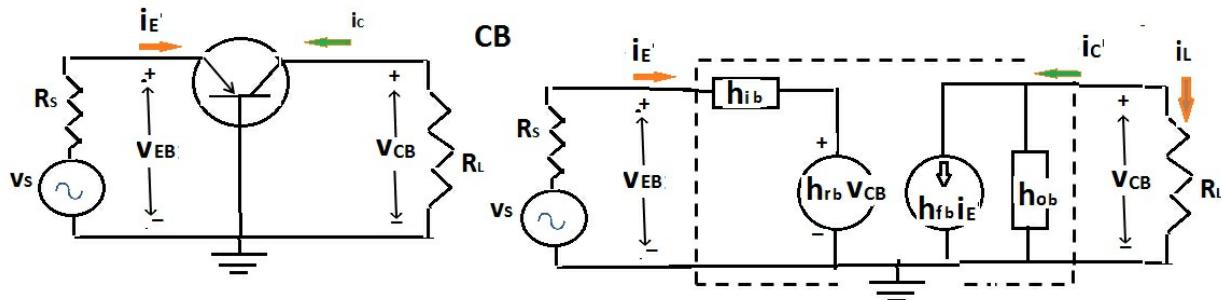
Or  $G = A_V A_I \dots(5)$

### TUTORIAL-2

**Example 8:** - Calculate Current gain, Voltage Gain, Input Impedance, Output Impedance and Power Gain of the CB amplifier shown in the circuit. The h-parameters of the transistor in CB configuration are given as  $h_{ib} = 21 \Omega$ ,  $h_{rb} = 2.9 \times 10^{-4}$ ,

$h_{fb} = -0.98$  and  $h_{ob} = 4.9 \times 10^{-7}$  mho. Assume that the amplifier is connected to an AC source having internal resistance,  $R_s = 1 K \Omega$  and the load resistance is also

$$R_L = 1 K \Omega.$$



**SOLUTION:** -- The performance of the amplifier will be analyzed using the formulae derived in the previous section. The values of the h-parameters given above will be substituted in these formulae.

### (i) Current Gain $A_I$

From Eq. 1 we have

$$A_I = \frac{-h_{fb}}{(1 + h_{ob} R_L)}$$

Given,  $h_{fb} = -0.98$  and  $h_{ob} = 4.9 \times 10^{-7}$  mho and  $R_L = 1 \text{ K } \Omega$ .

$$A_I = \frac{-(-0.98)}{(1 + 4.9 \times 10^{-7} \times 1 \times 10^3)} \cong 0.98$$

### (ii) Input Impedance $Z_i$

From Eq. 2(a) and 2(b) we have

$$Z_i = h_{ib} + h_{rb} A_I R_L$$

$$Z_i = \frac{h_{ib} + \Delta h_b R_L}{(1 + h_{ob} R_L)}$$

Given

$$h_{ib} = 21 \Omega, h_{rb} = 2.9 \times 10^{-4}, h_{fb} = -0.98$$

$$h_{ob} = 4.9 \times 10^{-7} \text{ mho}; R_L = 1 \text{ K } \Omega.$$

Substituting,

$$\begin{aligned} \Delta h_b &= (h_{ib} h_{ob} - h_{rb} h_{fb}) \\ &= (21 \times 4.9 \times 10^{-7} - 2.9 \times 10^{-4} \times (-0.98)) \\ &= 0.0003 \end{aligned}$$

Using Eq. 2 (a),

$$Z_i = 21 + 2.9 \times 10^{-4} \times 0.98 \times 1 \times 10^3 = 21.28 \Omega$$

Using Eq. 2 (b)

$$Z_i = \frac{21 + 0.0003 \times 1 \times 10^3}{1 + 4.9 \times 10^{-6} \times 1 \times 10^3} = 21.28 \Omega$$

### (iii) Voltage Gain $A_v$

From Eq. 3(a) and 3(b) we have

$$A_v = \frac{A_I R_L}{Z_i} = \frac{-h_{fb} R_L}{h_{ib} + \Delta h_b R_L}$$

Using Eq. 3(a) and the values of  $A_I$  and  $Z_i$  calculated above

$$A_v = \frac{0.98 \times 1 \times 10^3}{21.28} = 46$$

Using Eq. 3(b) and the given h-parameter values

$$A_v = \frac{-(-0.98) \times 1 \times 10^3}{21 + 0.0003 \times 1 \times 10^3} = 46$$

### (iv) Output Impedance

From Eq. 4 we have

$$Z_o = \frac{(R_S + h_{ib})}{(h_{ob} R_S + \Delta h_b)}$$

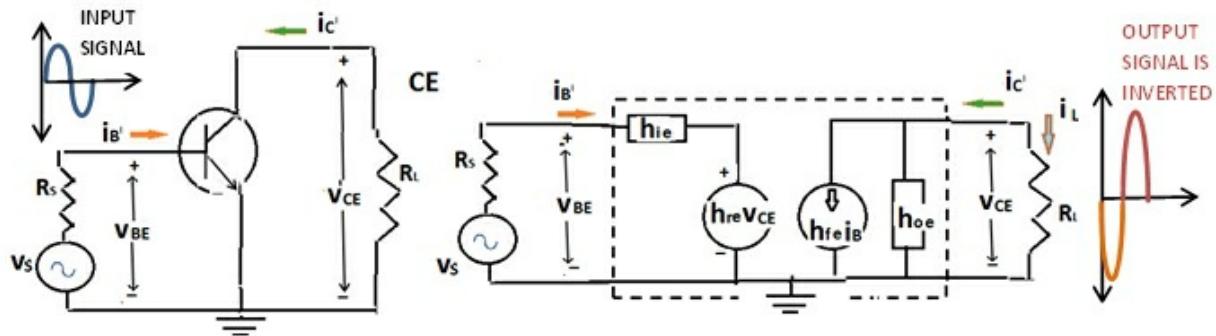
Substituting the previously calculated quantities and using

$$h_{ob} = 4.9 \times 10^{-7} \text{mho} \quad \text{and} \quad R_S = 1 \text{K}\Omega.$$

$$\begin{aligned} Z_o &= \frac{1 \times 10^3 + 21}{4.9 \times 10^{-7} \times 1 \times 10^3 + 0.0003} \\ &= |1.29 \times 10^6 \Omega| = 1.29 \text{M}\Omega \end{aligned}$$

**Example 9 :** - Calculate Current gain, Voltage Gain, Input Impedance, Output Impedance and Power Gain of the CE amplifier shown in the circuit. The h-parameters of the transistor in CE configuration are given as  $h_{ie} = 1100 \Omega$ ,  $h_{re} = 2.5 \times 10^{-4}$ ,  $h_{fe} = 50$  and  $h_{oe} = 25 \times 10^{-6} \text{mho}$ . Assume that the amplifier is connected to an AC source having  $R_S = 1 \text{K}\Omega$  and the load resistance is also  $1 \text{K}\Omega$ .

## SOLUTION :-



### (i) Current Gain $A_I$

From Eq. 1 we have

$$A_I = \frac{-h_{fe}}{(1 + h_{oe} R_L)}$$

Given

$$h_{fe} = 50 \text{ and } h_{oe} = 25 \times 10^{-6} \text{ mho and } R_L = 1 \text{ K } \Omega.$$

Substituting,

$$A_I = \frac{-50}{(1 + 25 \times 10^{-6} \times 1 \times 10^3)} \cong -48.8$$

### (ii) Input Impedance $Z_i$

From Eq. 2(a) and 2(b) we have

$$Z_i = h_{ie} + h_{re} A_I R_L = \frac{h_{ie} + \Delta h_e R_L}{(1 + h_{oe} R_L)}$$

Given

$$h_{ie} = 1100 \text{ } \Omega, h_{re} = 2.5 \times 10^{-4}, h_{fe} = 50 \text{ and} \\ h_{oe} = 25 \times 10^{-6} \text{ mho; and } R_L = 1 \text{ K } \Omega.$$

Substituting,

$$\begin{aligned} \Delta h_e &= (h_{ie} h_{oe} - h_{re} h_{fe}) \\ &= (1100 \times 25 \times 10^{-6} - 2.5 \times 10^{-4} \times 50) \end{aligned}$$

Or

$$\Delta h_e = 0.015$$

Using Eq. 2(a)

$$\begin{aligned} Z_i &= 1100 + 2.5 \times 10^{-4} \times (-48.8) \times 1 \times 10^3 \\ &= 1087.8 \text{ } \Omega = 1.088 \text{ K } \Omega \end{aligned}$$

Using Eq. 2(b)

$$Z_i = \frac{1100 + 0.015 \times 1 \times 10^3}{1 + 25 \times 10^{-6} \times 1 \times 10^3}$$

$$= 1087.8 \Omega = 1.088 K \Omega$$

### (iii) Voltage Gain $A_v$

From Eq. 3(a) and 3(b) we have

$$A_v = \frac{A_I R_L}{Z_i} = \frac{-h_{fe} R_L}{h_{ie} + \Delta h_e R_L}$$

Using Eq. 3(a) and the values of  $A_I$  and  $Z_i$  calculated above

$$A_v = \frac{-48.8 \times 1 \times 10^3}{1088} = -44.85$$

Using Eq. 3(b) and the given h-parameter values

$$A_v = \frac{-(50) \times 1 \times 10^3}{1100 + 0.015 \times 1 \times 10^3} = -44.85$$

**THE SIGNIFICANCE OF THE NEGATIVE SIGNS IN  $A_I$  AND  $A_v$  IS THAT THE OUTPUT SIGNAL IS APPEARS WITH A PHASE SHIFT OF  $180^\circ$  (or  $\pi$  radian) w.r.t. THE INPUT SIGNAL. THIS IS SHOWN IN THE FIGURE WITH THE HELP OF THE INPUT AND OUTPUT WAVEFORMS.**

### (iv) Output Impedance

From Eq. 4 we have

$$Z_o = \frac{(R_s + h_{ie})}{(h_{oe} R_s + \Delta h_e)}$$

Substituting the previously calculated quantities and using

$$h_{oe} = 25 \times 10^{-6} \text{ mho and } R_s = 1 K \Omega.$$



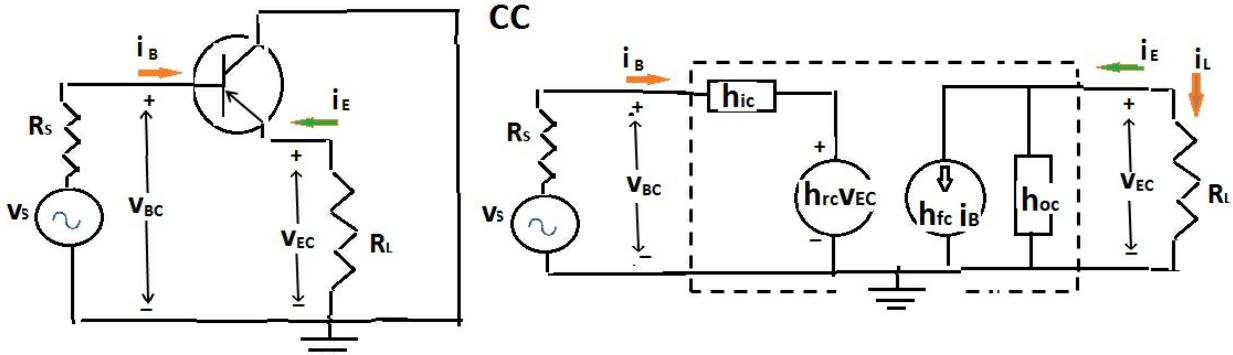
$$Z_o = \frac{1 \times 10^3 + 1100}{25 \times 10^{-6} \times 1 \times 10^3 + 0.015}$$

$$= 52500 \Omega = 52.5 K\Omega$$

**Example 10:** - Calculate Current gain, Voltage Gain, Input Impedance, Output Impedance and Power Gain of the CC amplifier shown in the circuit. The h-parameters of the transistor in CC

configuration are given as  $h_{ic} = 1100 \Omega$ ,  $h_{rc} = 1$ ,  $h_{fc} = -51$  and  $h_{oc} = 25 \times 10^{-6}$  mho. Assume that the amplifier is connected to an AC source having  $R_s = 1 K\Omega$  and the load resistance is also  $1 K\Omega$ .

### SOLUTION :-



#### (i) Current Gain $A_I$

From Eq. 1 we have

$$A_I = \frac{-h_{fc}}{(1 + h_{oc} R_L)}$$

Given  $h_{fc} = -51$  and  $h_{oc} = 25 \times 10^{-6}$  mho. and  $R_L = 1 K\Omega$ .

Substituting,

$$A_I = \frac{-(-51)}{(1 + 25 \times 10^{-6} \times 1 \times 10^3)} \cong 49.76$$

#### (ii) Input Impedance $Z_i$

From Eq. 2(a) and 2(b) we have

$$Z_i = h_{ic} + h_{rc} A_I R_L = \frac{h_{ic} + \Delta h_c R_L}{(1 + h_{oc} R_L)}$$

Given

$h_{ic} = 1100 \Omega$ ,  $h_{rc} = 1$ ,  $h_{fc} = -51$  and  
 $h_{oc} = 25 \times 10^{-6}$  mho; and  $R_L = 1 K\Omega$ .

Substituting,

$$\begin{aligned} \Delta h_c &= (h_{ic} h_{oc} - h_{rc} h_{fc}) \\ &= (1100 \times 25 \times 10^{-6} - 1 \times (-51)) \end{aligned}$$

Or  $\Delta h_c = 51.02$

Using Eq. 2(a)

$$Z_i = 1100 + 1 \times 49.76 \times 1 \times 10^3$$

$$= 50860 \Omega = 50.86 \text{ K } \Omega$$

Using Eq. 2(b)

$$\boxed{Z_i = \frac{1100 + 51.02 \times 1 \times 10^3}{1 + 25 \times 10^{-6} \times 1 \times 10^3}}$$

$$= 50860 \Omega = 50.86 \text{ K } \Omega$$

### (iii) Voltage Gain $A_v$

From Eq. 3(a) and 3 (b) we have

$$A_v = \frac{A_I R_L}{Z_i} = \frac{-h_{fc} R_L}{h_{ic} + \Delta h_c R_L}$$

Using Eq. 3(a) and the values of  $A_I$  and  $Z_i$  calculated above

$$A_v = \frac{49.76 \times 1 \times 10^3}{50860} = 0.978$$

Using Eq. 3(b) and the given h-parameter values

$$A_v = \frac{-(-51) \times 1 \times 10^3}{1100 + 51.02 \times 1 \times 10^3} = 0.978$$

### (iv) Output Impedance

From Eq. 4 we have

$$Z_o = \frac{(R_s + h_{ic})}{(h_{oc} R_s + \Delta h_c)}$$

Substituting the previously calculated quantities and using  $h_{oe} = 25 \times 10^{-6}$  mho and  $R_s = 1 \text{ K } \Omega$ .

$$Z_o = \frac{1 \times 10^3 + 1100}{25 \times 10^{-6} \times 1 \times 10^3 + 51.02} = 41.14 \Omega$$

## 6.6 Comparison of Transistor Amplifier configurations

In the three numerical examples, the same transistor was connected in the three configurations, were driven by the same source and delivered power to the same load. Hence this forms a basis for the

**comparison of the performance of an amplifier in these three configurations.** The results obtained in the three previous examples are tabulated below.

**Table 3::** Table of Comparison of Transistor Amplifier Configurations

PERFORMANCE	CONFIGURATION		
	CB	CE	CC
<b>Current Gain</b>	0.98	- <b>48.8</b>	49.76
<b>Voltage Gain</b>	46	- <b>44.85</b>	0.978
<b>Input Impedance</b>	21.28 $\Omega$	<b>1.085 K<math>\Omega</math></b>	50.86 K $\Omega$
<b>Output Impedance</b>	1.29 M $\Omega$	<b>52.5 K<math>\Omega</math></b>	41.14 $\Omega$

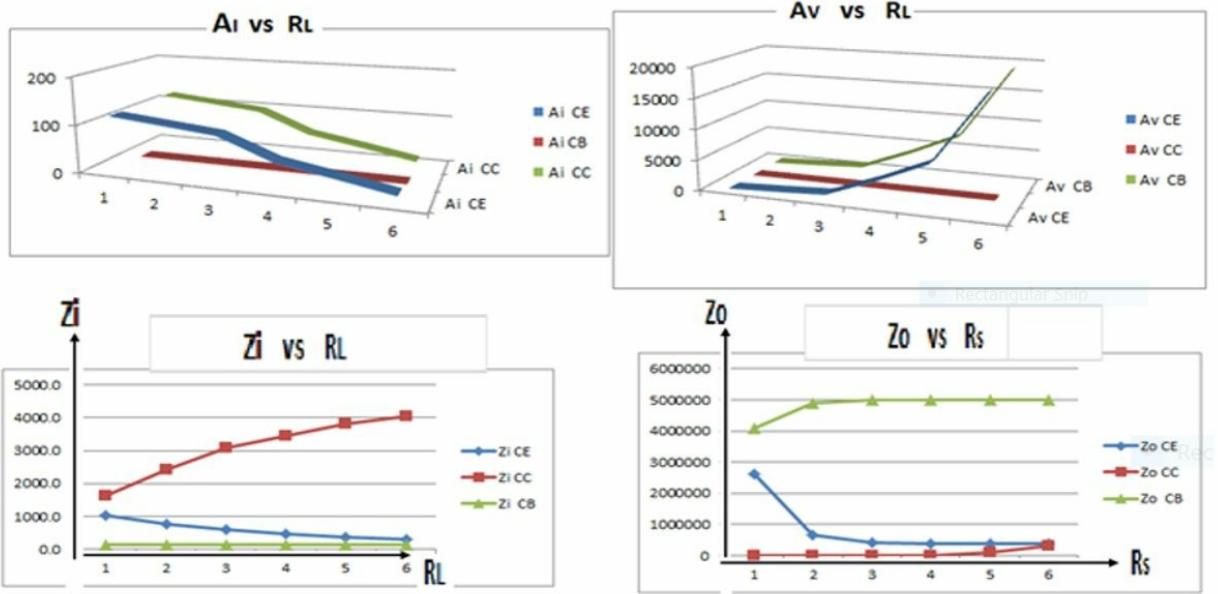
### OBSERVATION :-

1. The **CE configuration** provides **BOTH Voltage Gain and Current Gain**. Whereas the CB configuration provides **only a voltage gain** its **current gain is nearly equal to unity**. This means that output current is equal to the input current (nearly). Again, the **CC configuration** provides **only a current gain**, but its **voltage gain is nearly equal to unity**. The **output voltage is equal to the input voltage**.
2. **The Current Gain and the Voltage Gain of the CE configuration appears with a negative sign.** This means that whereas the output signal is **amplified**, it also gets **INVERTED** w.r.t. the input signal. In other words, the **output signal appears with a phase shift of  $180^0$  w.r.t. the input signal**.
3. **The Input Impedance of the CC configuration is the highest** while the input impedance CB configuration is lowest. The **Input Impedance of the CE configuration is moderate**.
4. **The Output Impedance of the CB configuration is highest** while that of the **CC configuration is lowest**. The **Output Impedance of the CE configuration is moderate**.

### Graphical Comparison

The set of formulae for  $A_I$ ,  $A_V$ ,  $Z_I$  and  $Z_O$ , are such that **while  $A_I$ ,  $A_V$ , and  $Z_I$  are functions of the Load Resistance  $R_L$ , the Output**

**Impedance  $Z_0$  is a function of the internal resistance  $R_s$  of the source.** When these quantities are plotted as functions of the respective resistances, we obtain the following comparison on the basis of the plots. This is shown in Fig –17. below.



**Fig-17: -- Graphical comparison of performance of a Transistor Amplifier in the three configurations.**

In this, we chose some evenly placed values of the Load Resistance,  $R_L$  and Source Resistance,  $R_s$ , in the range from  $10 \Omega$  to  $1 M\Omega$  and calculated the quantities  $A_I$ ,  $A_V$ ,  $Z_I$  and  $Z_0$  for a particular transistor, with the typical values of the h-parameters for each of the configurations, with the help of the formulae, in an Excel Table. The results were represented with the help of the following graphics.

**OBSERVATION:** - The following observations are made from the graphs in the Fig – 17. These observations further confirm the earlier observations and bring out a few more aspects of the performance of the amplifier.

1. **Current Gains of both CE and CC amplifier are high and nearly equal. They also vary in the same manner w.r.t. variations of  $R_L$ . The CB amplifier does not provide current gain.**
2. **Voltage Gains of both CE and CB amplifier are high and**

nearly equal. They also vary in the same manner w.r.t. variations of  $R_L$ . The CC amplifier does not provide voltage gain.

3. Input Impedance of the CE amplifier is not only MODERATE but also,  $Z_I$  is constant over a large range of values of  $R_L$ . This property makes the CE amplifier compatible with a variety of ranges of Load Devices. When the Input Impedance is either too high (as in case of CC) or too low (as in case of CB), the compatibility of the amplifier w.r.t. to the load device becomes tricky.
4. Output Impedance of the CE amplifier is not only MODERATE but also,  $Z_O$  is constant over a large range of values of  $R_S$ . This property makes the CE amplifier compatible with a variety of signal sources. For the same reasons as described in point no. 3, the **CB and CC amplifier are not compatible** with a wide variety of signal sources.

## CONCLUSION

**FROM THE DISCUSSION IT CAN BE CONCLUDED THAT THE CE CONFIGURATION IS MOST SUITABLE FOR A WIDE RANGE OF APPLICATIONS.**

### 6.7 Simplified h-parameter model

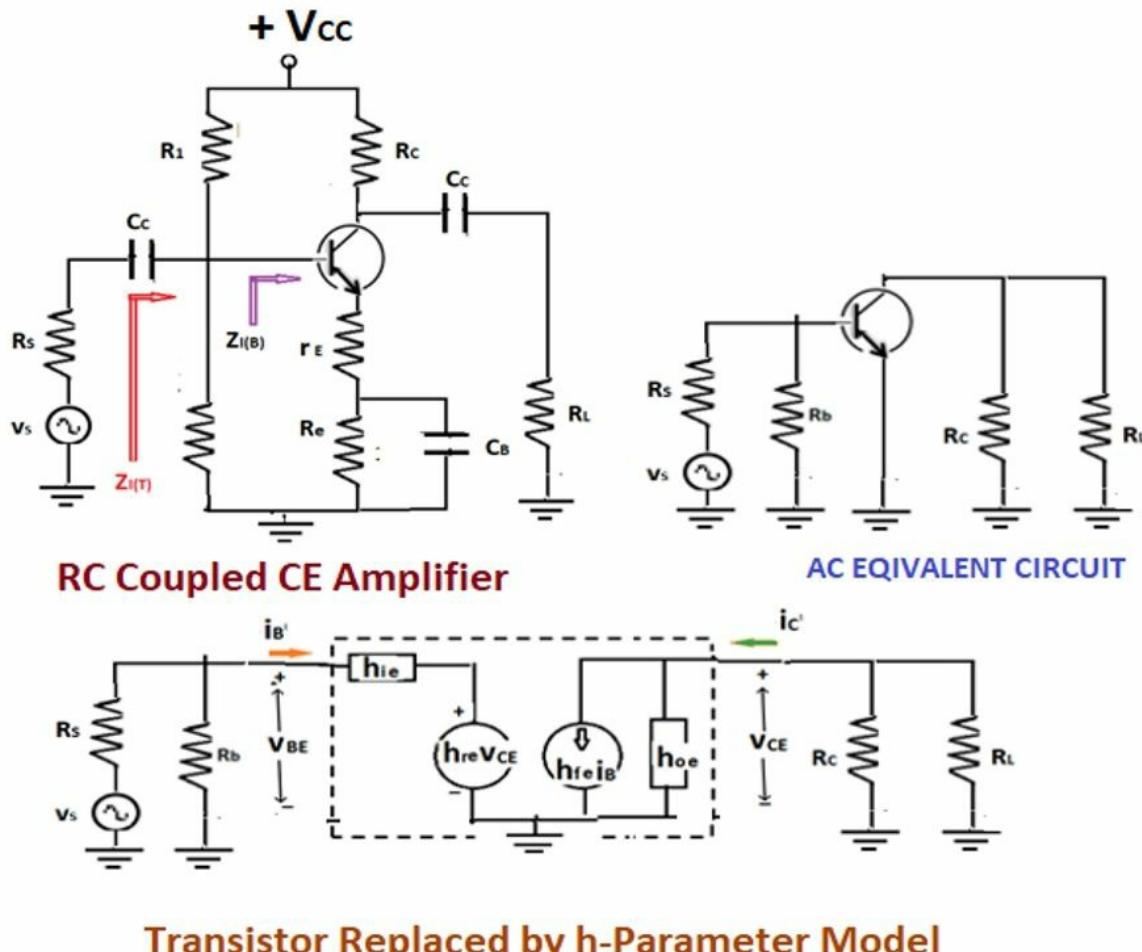
The h-parameter model is rather complex. It further complicates the analysis of the amplifier when the complete circuit along with the biasing resistances is considered. Consider the amplifier in the circuit to be analyzed. The AC Equivalent circuit and the h-parameter equivalent circuit are shown in the figure, in order to realize the complexity of our task at hand.

A simplified version of the h-Parameter model is developed using some approximations. The typical CE h-Parameter values, tabulated above, are reproduced below for convenience.

Parameter			
CE   $h_{ie} = 2.25 \text{ k}\Omega$	$h_{re} = 8.5 \times 10^{-4}$	$h_{fe} = 400$	$h_{oe} = 8 \times 10^{-6} \text{ mho}$

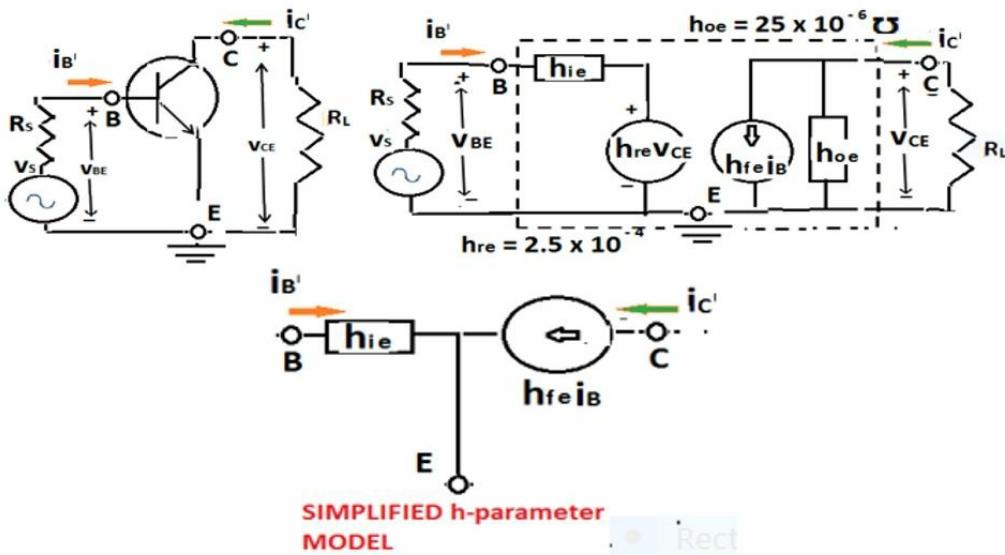
The approximations to be used to simplify the h-parameter Model are as follows—

- The numerical value of the parameter  $h_{re}$  is of the order of  $10^{-4}$ . The voltage “ $v_{CE}$ ” is of the order of a few millivolts. Thus, the voltage source “ $h_{re} v_{CE}$ ” in the input loop can be neglected.
- The numerical value of the parameter  $h_{oe}$  is of the order of  $10^{-6}$ . This parameter represents an “Admittance”. Since this admittance is of the order of a micro-mho, **this can be approximated as an Open-Circuit**.



- The h-Parameter Model of the CE configuration can be

simplified as shown in the Fig- 19 below.



**Fig – 19:** -- The *h*-parameter Model of the Common Emitter Amplifier can be simplified.

### Analysis using Simplified h-parameter Model

- ✓ The AC Equivalent Circuit of the amplifier is taken, in which the transistor is replaced by the Simplified h-parameter Model (in this case DC Analysis is not required).
- ✓ The resulting circuit is analyzed to obtain the performance characteristics of the amplifier.
- ✓ The Fig – 2 shows a CE amplifier, along with its AC Equivalent Circuit and the resulting circuit where the transistor is replaced by the simplified h-parameter Model.

#### (1) Input impedance at Base $Z_{I(B)}$

Input Impedance at the Base is defined as

$$Z_{I(B)} = \frac{V_i}{i_B}$$

Where,

$$V_i = i_B h_{ie} + i_E r_E$$

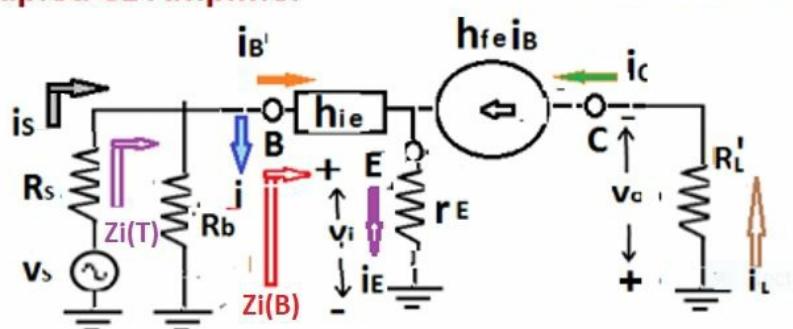
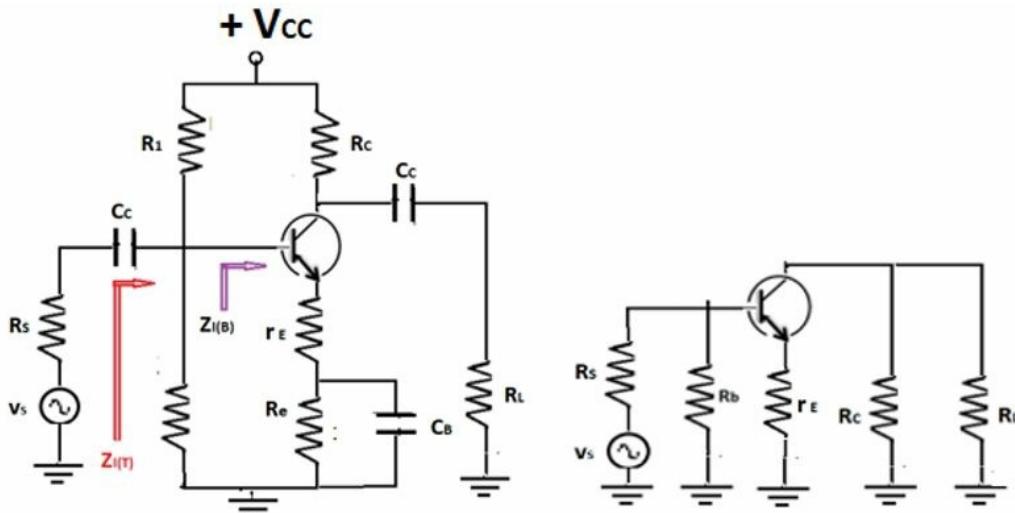
Where

$$i_E = i_B + i_C = (1 + h_{fe}) i_B$$

$$\therefore v_i = \{h_{ie} + (1 + h_{fe} r_E\} i_B$$

Substituting and simplifying, we have

$$Z_I(B) = h_{ie} + (1 + h_{fe}) r_E \dots (1)$$



**Fig. – 20**

## (2) Current Gain $A_I$

By definition, Current Gain of an amplifier is the ratio of the Load Current and the current supplied by the source.

$$A_I = \frac{i_L}{i_S} = \frac{-i_C}{i_S}$$

We can express this also as

$$A_I = \frac{-i_C}{i_S} = \frac{-i_C}{i_B} \cdot \frac{i_B}{i_S}$$

In the circuit above, the current ' $i_S$ ', supplied by the source gets divided into two parts, i.e. ' $i$ ' and ' $i_B$ ', where ' $i$ ' is the current through the resistance  $R_b$  and  $i_B$  is the base current that flows into the impedance at the Base, namely  $Z_{I(B)}$ . Applying Current Divider Rule we get –

$$i_B = \frac{i_S \cdot R_b}{R_b + Z_{I(B)}}$$

$$\therefore \frac{i_B}{i_S} = \frac{R_b}{R_b + Z_{I(B)}}$$

In this circuit, we also have

$$Z_{I(T)} = R_b \parallel Z_{I(B)} = \frac{R_b \cdot Z_{I(B)}}{R_b + Z_{I(B)}}$$

$$\therefore \frac{R_b}{R_b + Z_{I(B)}} = \frac{Z_{I(T)}}{Z_{I(B)}}$$

$$\therefore \frac{i_B}{i_S} = \frac{Z_{I(T)}}{Z_{I(B)}}$$

It is observed that  $i_C$  is the current supplied by the current source of the simplified h-parameter model.

Thus

$$i_C = h_{fe} i_B$$

$$\therefore \frac{i_C}{i_B} = h_{fe}$$

Substituting all these in the expression for  $A_I$  and simplifying, we get

$$A_I = -h_{fe} \cdot \frac{Z_{I(T)}}{Z_{I(B)}} \dots (2(a))$$

In the expression for  $Z_{I(B)}$  in Eq. 1 the quantity

$$h_{ie} \ll (1 + h_{fe}) r_E$$

and

$$(1 + h_{fe}) \approx h_{fe}.$$

Using these approximations, we have

$$Z_{I(B)} \approx h_{fe} r_E$$

Thus

$$A_I \approx -\frac{Z_{I(T)}}{r_E} \dots (2(b))$$

### (3) Voltage Gain $A_V$

By definition Voltage Gain is given by

$$A_V = \frac{V_O}{V_I}$$

Where  $V_O = i_L R_L' = -i_C R_L' = -h_{fe} i_B R_L'$

Substituting and simplifying we have,

$$A_V = \frac{-h_{fe} \cdot R_L'}{\{h_{ie} + (1 + h_{fe}) \cdot r_E\}}$$

$$\therefore A_V = \frac{-h_{fe} \cdot R_L'}{Z_{I(B)}} \dots (3(a))$$

Using the approximation for  $Z_{I(B)} \approx h_{fe} r_E$  we have

$$A_V \approx -\frac{R_L'}{r_E} \dots (3(b))$$

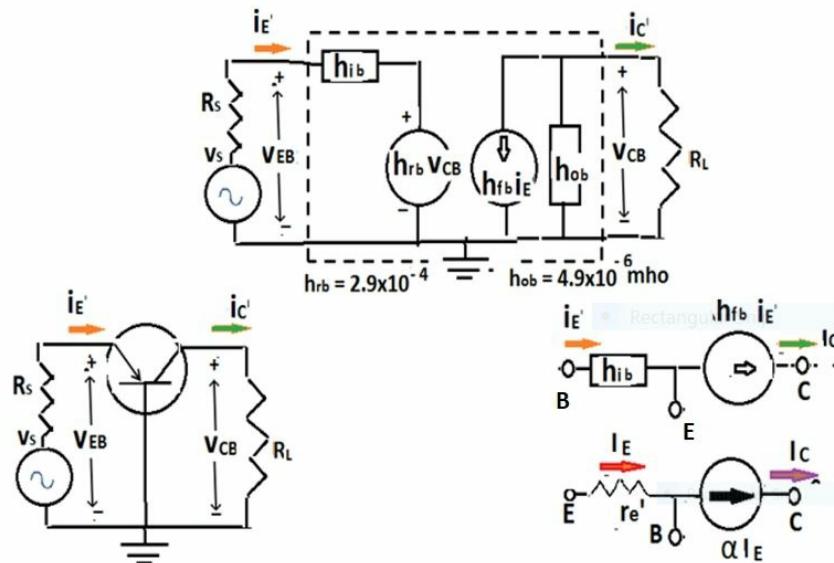
**NOTE :** EQUATIONS FOR  $A_V$  AND  $A_I$  ARE THE SAME AS THOSE, DERIVED FOR r-parameter MODEL (Section- 2)

HENCE, WE CONCLUDE THAT THE ANALYSIS USING THE r-parameter MODEL AND THE SIMPLIFIED h-parameter MODEL RESULT IN THE SAME.

**Similarity between Simplified h-parameter Model & r-parameter Model**

The Simplified h-parameter Model had been developed by applying certain approximations to the h-parameter Model of the CE configuration. If we use similar approximations to the h-parameter Model of the CB configuration as –

- The numerical value of the parameter  $h_{rb}$  is of the order of  $10^{-4}$ . This parameter defines a voltage source “ $h_{re} v_{CB}$ ” in the input loop. The voltage “ $v_{CB}$ ” is of the order of a few millivolts in practice. Hence this voltage source in the input loop can be approximated as a Short-Circuit.
- The numerical value of the parameter  $h_{ob}$  is of the order of  $10^{-6}$ . This parameter represents an “Admittance”. Since this admittance is of the order of a micro-mho, this can be approximated as an Open-Circuit.



**Fig – 21:** - Similarity between Simplified h-parameter Model of the CB configuration and the r-parameter Model. This is true because by definition,  $h_{ib} = r_e'$  &  $h_{fb} = \alpha$ .

Applying these approximations, the h-Parameter Model of the CB configuration can be simplified as shown above.

- In this, ‘ $h_{ib}$ ’ is the “Forward Resistance” of the forward biased

Emitter-Base junction, looking into the Emitter terminal. It is defined as the ‘Reciprocal of the Slope of the Input Characteristic’ of the transistor. **The definition of the ‘r-parameter’  $r_e$  is also the same. Thus,  $h_{ib}$  is nothing but  $r_e$ .**

Again, ‘ $h_{fb}$ ’ is defined as

$$h_{fb} = \frac{\Delta i_C}{\Delta i_E}$$

The definition of the “Transport factor”  $\alpha$  of the transistor is also the same. Hence  $h_{fb}$  is nothing but  $\alpha$ .

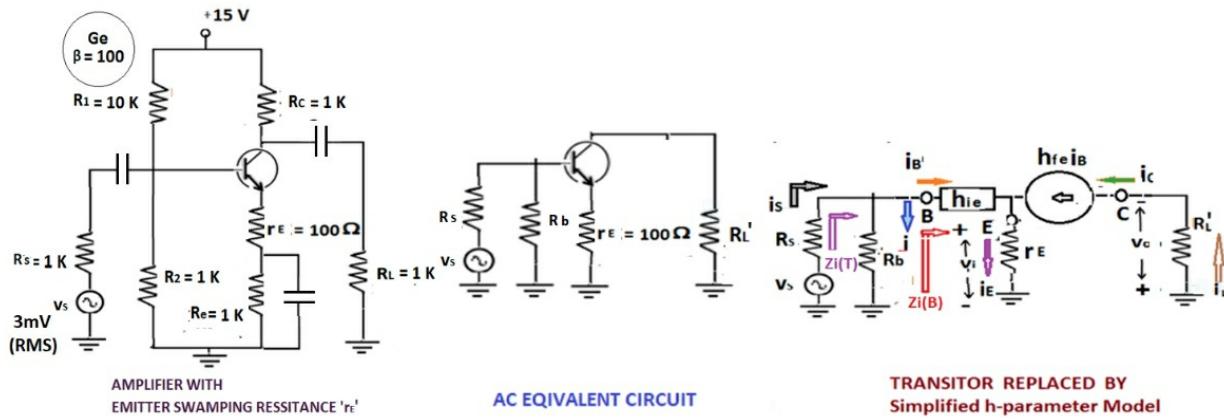
Thus, we see that the **r-parameter Model is nothing but the Simplified h-parameter Model of the CB configuration.**

**Hence, we realize that the analysis using the r-parameter model and the simplified h-parameter result in the same.**

### TUTORIAL-3

**Example 11:** – Use the simplified h-parameter Model to analyze the performance of the amplifier given in the circuit. The relevant h-parameters of the transistor are  $h_{ie} = 1.1 \text{ K}$  and  $h_{fe} = 100$ .

### SOLUTION



Using the equations 1 to 3 derived above, and using the h-parameter values given, we have, from Eq. 1

$$Z_I(B) = h_{ie} + (1 + h_{fe}) r_E$$

$$\text{Given } h_{ie} = 1.1 \text{ K} = 1100 \Omega, h_{fe} = 100$$

and from the circuit  $r_E = 100 \Omega$

$$\therefore Z_{I(B)} = 1100 + 101 \times 100 = 11200 \Omega = 11.2 K$$

In the given circuit

$$R_1 = 10 K \text{ & } R_2 = 1 K.$$

Thus, their parallel combination is

$$R_b = \frac{R_1 R_2}{R_1 + R_2} = \frac{10 \times 1}{10 + 1} = 0.909 K = 909 \Omega$$

Total Input Impedance of the amplifier is  $Z_{I(T)}$ , which is the **parallel combination of  $Z_{I(B)}$  and  $R_b$** .



Hence

$$Z_{I(T)} = \frac{R_b \cdot Z_{I(B)}}{R_b + Z_{I(B)}} = \frac{0.909 \times 11.2}{0.909 + 11.2} = 0.841 K$$

OR

$$Z_{I(T)} = 841 \Omega$$

From Eq. 2 and substituting for  $h_{fe}$ ,  $Z_{I(B)}$  and  $Z_{I(T)}$  we have—

$$A_I = - h_{fe} \cdot \frac{Z_{I(T)}}{Z_{I(B)}} = - 100 \cdot \frac{0.841}{11.2}$$

$$A_I = - 7.5$$

From Eq.3

$$A_V = \frac{- h_{fe} \cdot R_L'}{Z_{I(B)}}$$

Where  $R_L'$  is the parallel combination of  $R_C$  and  $\underline{R_L}$ . Hence,

$$R_L' = \frac{1 \times 1}{1+1} = 0.5 K$$

Substituting

$$A_V = \frac{- 100 \times 0.5}{11.2} = - 4.46$$

**CONCLUSION:** -- THE RESULTS OF ANALYSIS BY SIMPLIFIED h-parameter MODEL ARE COMPATIBLE WITH THOSE OBTAINED BY r-parameter ANALYSIS

## Section- 3

### Special Amplifier Connections

## 6.8 Common Collector Amplifier

### (Emitter Follower)

- ❖ In the previous Section we had seen that a transistor amplifier in CC configuration provides only Current Gain, but it's Voltage gain is unity. **Thus, it is not preferred for general purpose amplification.**
- ❖ However, it has very high Input Impedance and very low Output Impedance.
- ❖ These special qualities make it suitable when the signal source has a very high internal resistance  $R_s$  or when the external load resistance  $R_L$  is very low – or both.
- ❖ In the **former case** the CC amplifier is used as **the first stage of a cascaded amplifier**, and in the **latter case** it is used as **the last stage of the cascaded amplifier**. (A Cascaded Amplifier is a Multi Stage Amplifier, which is used to provide a high gain. The mid stages of the Cascaded Amplifier need to be CE in order to provide high gain).

### Analysis of CC Amplifier (Emitter Follower)

The circuit in the **Fig-21** shows a CC amplifier. The transistor in the AC Equivalent Circuit is replaced by the simplified h-parameter model. Note that the most suitable biasing circuit for an amplifier is the Voltage Divider Biasing circuit. The CC amplifier also needs to use this biasing circuit. In the circuit shown in figure, the **collector resistance  $R_C$**  is bypassed by the By-Pass Capacitor  $C_B$ . Hence in the AC equivalent circuit, this resistance will be short circuited, as shown in the figure. The various steps of analysis are as follows.

#### 1. Current Gain $A_I$

By definition

$$A_I = \frac{i_o}{i_i}$$

In this circuit  $i_o = i_E = i_C + i_B$  and  $i_i = i_B$ , with  $i_C = h_{fe} i_B$

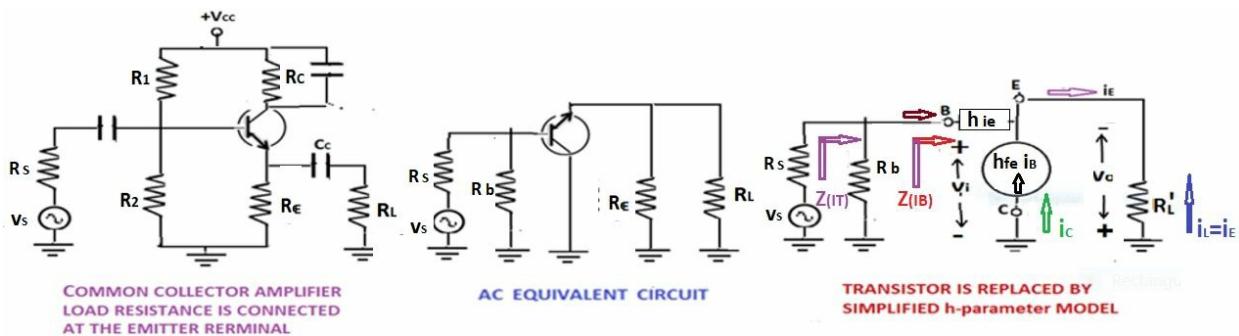
∴

$$i_E = (1 + h_{fe}) i_B$$

Substituting we have

$$A_I = (1 + h_{fe}) \dots (1)$$

In this expression, if we use the **typical value of h-parameter  $h_{fe} = 100$** , we observe that Current Gain is high.



**Fig –22:** - Circuit Diagram of the CC Amplifier or Emitter Follower. The AC Equivalent Circuit and the circuit obtained by replacing the transistor by the Simplified h-parameter Model, which is used for analyzing the amplifier are also shown.

## 2. Input Impedance at the Base $Z_{I(B)}$

By definition

$$Z_{I(B)} = \frac{v_i}{i_i}$$

The **Input Voltage  $v_i$**  is the voltage between the Base and the common terminal, Collector. However, the Collector is at ground and the bottom end of the load  $R_L'$  is also at ground. Since in between we have a Current Source " $h_{fe} i_B$ " contributing to the current flow  $i_E$ , thus Input Voltage  $v_i$  is the sum of the voltage dropped across  $h_{ie}$  due to the current  $i_B$  and the voltage dropped across  $R_L'$  due  $i_E$ .

∴

$$v_i = i_B h_{ie} + i_E R_L' = \{h_{ie} + (1 + h_{fe})R_L'\} i_B$$

Substituting we have

$$Z_{I(B)} = h_{ie} + (1 + h_{fe}) R_L' \dots (2)$$

In this expression, if we use the **typical value of h-parameter  $h_{fe} = 100$**

and  $h_{ie} = 1.1$  K and assume,  $R_L' = 1$  K, we can calculate that Input Impedance at the Base is

$$Z_{I(B)} = 1100 + 101 \times 1000 = 102100 \Omega$$

$$Z_{I(B)} = 102.1 \text{ K}$$

**Input Impedance of the Emitter Follower is a very high.**

### 3. Voltage Gain $A_V$

By definition

$$A_V = \frac{v_o}{v_i}$$

In this the output Voltage  $v_o$  is the voltage developed across  $R_L'$  due to the output current  $i_E$ .

$$\therefore v_o = i_E R_L' = 1 + h_{fe}) R_L' \cdot i_B$$

Substituting for  $v_i$ , we have

$$A_V = \left\{ \frac{(1 + h_{fe}) R_L'}{h_{ie} + (1 + h_{fe}) R_L'} \right\} \quad \dots(3)$$

In this expression the **numerator is less than the denominator**. Thus, **Voltage Gain is less than Unity**. If we substitute the typical values of the h-parameters and  $R_L'$  as above, we get

$$A_V = \frac{(1+100) \times 1000}{1100 + (1+100) \times 1000} = 0.99$$

Output Voltage **equals** Input Voltage.

1. The **sign of the Voltage Gain is positive**. Which means **polarity** of the output voltage is the **same as** that of the Input Voltage.
2. In the CC amplifier, the output is taken at the Emitter. Thus we can say that the “Voltage at the Emitter **follows** that at the input terminal”. Hence the name “**Emitter Follower**”.

### 4. Output Impedance $Z_O$

By definition

$$Z_o = \frac{v_o}{i_o}$$

In this

$$i_o = i_E = (1 + h_{fe}) i_B$$

In this circuit, we normally have  $R_b \gg h_{ie}$ . Thus, **assuming**  $R_b$  to be **open circuit** we have

$$i_B = \frac{v_s}{R_s + h_{ie}}$$

$$\therefore i_o = (1 + h_{fe}) \cdot \frac{v_s}{R_s + h_{ie}}$$

Since we had  $A_V \approx 1$       $\therefore v_o \approx v_s$ . Substituting for  $i_o$  from above we have

$$Z_o = \frac{R_s + h_{ie}}{(1 + h_{fe})} \quad \underline{\underline{(4)}}$$

If we substitute the **typical values of the h-parameters** as above and assume  $R_s = 1 \text{ K}$  we get

$$Z_o = \frac{(1000+1100)}{(1+100)} = 21 \Omega$$

**Thus, we observe that output impedance is very low.**

## SUMMARY OF THE PROPERTIES OF Emitter FOLLOWER

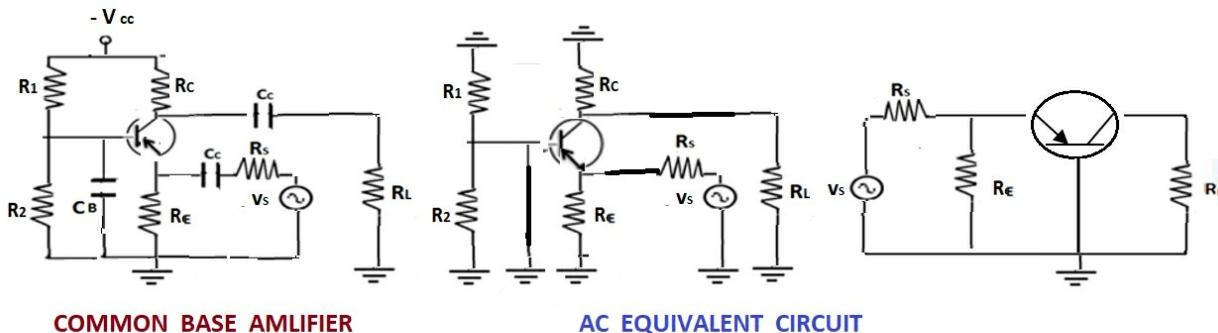
1. Current Gain of the Emitter Follower is high and essentially, its magnitude equals that if the CE amplifier. However, the sign of the Current Gain parameter is positive, unlike the CE Amplifier.
2. Input Impedance of the Emitter Follower is very high.
3. Voltage Gain of the Emitter Follower is ‘Unity’ and its sign is positive. Thus Output voltage equals the Input Voltage in both magnitude and phase.
4. Output Impedance is very low.

## APPLICATIONS OF THE Emitter FOLLOWER

1. Emitter Follower is used as a First Stage of a cascaded amplifier system when the source resistance is very high.
2. Emitter Follower is used as a Last Stage of a cascaded amplifier system when the external load resistance is very low.

## 6.9 Common Base Amplifier

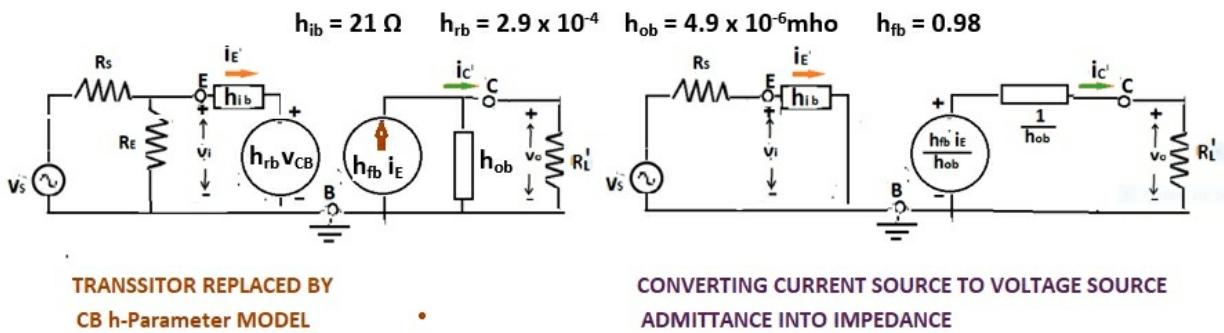
- The CC Amplifier or the Emitter Follower is used as the First Stage when the Source Resistance is high and/or as the Last Stage when the external load resistance is low, in a cascaded amplifier system.
- In the opposite situation, **when the source resistance is low and/or the external load resistance is high, the Common Base amplifier is used as the first stage and/or the last stage of a cascaded amplifier system**, as the case may be.
- The Voltage Divider Biasing Circuit is the “Universal Biasing Circuit”. Hence this is used in a CB amplifier also, as shown in the Fig –22 below.



**Fig –23:** - Common Base Amplifier Circuit, and its AC Equivalent circuit

- The transistor in the circuit shown in Fig –22, is biased by a Voltage-Divider Biasing Circuit, consisting of R<sub>1</sub>, R<sub>2</sub>, R<sub>C</sub> and R<sub>E</sub>, as in all the previous cases in this chapter.
- The signal from the source is coupled into the Emitter terminal and the amplified signal from the Collector is coupled to the external load R<sub>L</sub> by means of Coupling Capacitors C<sub>C</sub>.

- A By-Pass Capacitor  $C_B$  is used to by-pass the AC signal from the biasing resistors of the Base.
- The AC Equivalent circuit is obtained by short circuiting the DC Biasing source  $V_{CC}$  to ground and short circuiting all the capacitors. (However, in the second figure above, we have shown the capacitor  $C_B$  to make it clear that, this capacitor is in parallel to the biasing resistors of the Base, namely  $R_1$  &  $R_2$ . Since, in reality, this capacitor will be short circuited, the resistors  $R_1$  &  $R_2$  will not appear in the AC Equivalent circuit, as shown in the third figure.)
- The AC Equivalent circuit is redrawn to show that the transistor is in CB configuration, in the third part of the Fig – 22. In order to analyze the amplifier, the transistor is replaced by the h-parameter equivalent circuit of the CB configuration. Thus, we obtain the following figure.



- ✓ Since  $h_{rb}$  is negligible, the voltage source “ $h_{rb} v_{CB}$ ” may be neglected.
- ✓ Recall that the value of  $R_E$  need to be large in a voltage divider biasing circuit, in order for the stability factor to be good. Since we are going to use this amplifier to amplify a source with a low value of  $R_S$  and since  $h_{ib}$  of the transistor is also of a low value, we **may neglect  $R_E$**  in the equivalent circuit.
- ✓ Next, we convert the “Current Source & Admittance” parallel combination into the equivalent “Voltage Source + Impedance” series combination. The resulting circuit is now analyzed to obtain the performance parameters of the Common Base Amplifier as follows.

### (i) Voltage Gain $A_V$

Voltage Gain is the ratio of output Voltage to Input Voltage;

$$A_V = \frac{v_o}{v_i}$$

Where

$$v_o = i_c R_L' = h_{fb} i_E \cdot R_L' \quad \& \quad v_i = i_E \cdot h_{ib}$$

$$\therefore A_V = \frac{h_{fb} R_L'}{h_{ib}} \approx \frac{R_L'}{h_{ib}} \quad \dots (1)$$

(Since  $h_{fb} \approx 1$ )

In this, since  $R_L' \gg h_{ib}$  we have a large Voltage Gain in the Common Base amplifier.

### (ii) Current Gain $A_I$

Current Gain is the ratio of Output Current to Input Current

$$A_I = \frac{i_o}{i_i}$$

Rectangular Snip

Where

$$i_o = h_{fb} i_E \quad \& \quad i_i = i_E$$

$$\therefore A_I = h_{fb} \quad \dots (2)$$

In this, since  $h_{fb} \approx 1$ , Output Current is equal to the Input Current. Hence there is no Current Gain in the Common Base amplifier.

### (ii) Input Impedance $Z_I$

By definition

$$Z_{I(B)} = \frac{v_i}{i_i}$$

Substituting for  $v_i$  and  $i_i$  from above we have

$$Z_I = h_{ib} \quad \dots (3)$$

Since the typical numerical value of  $h_{ib}$  is in the range of a few ohms only, the **Input Impedance of the Common Base Amplifier is**

**quite low**, compares to the CE and CC amplifiers.

(iii) **Output Impedance  $Z_o$**

$$Z_o = \frac{v_o}{i_o}$$

In this

$$i_o = i_c = h_{fb} i_E$$

Output Voltage  $v_o$  is also the **voltage dropped across the series impedance  $1/h_{oe}$**  due to the Output Current  $i_c$ . Thus

$$v_o = i_c \cdot \frac{1}{h_{ob}} = \frac{h_{fb} i_E}{h_{ob}}$$

Substituting for  $i_o$  from above we have

$$Z_o = \frac{1}{h_{ob}} \quad \underline{\dots(4)}$$

If we substitute the **typical values of the h-parameter**

$$h_{ob} = 4.9 \times 10^{-7} \text{ mho},$$

$$Z_o = \frac{1}{4.9} \times 10^7 \Omega = 2 \times 10^6 \Omega = 2 \text{ M}\Omega$$

Thus, we observe that the **Output impedance of the Common base amplifier is very high**.

### SUMMARY OF THE PROPERTIES OF COMMON BASE AMPLIFIER

1. Voltage Gain,  $A_V$  of the CB amplifier is as high as that of the CE amplifier. However, the sign of the Voltage Gain parameter is positive, unlike the CE Amplifier.
2. Input Impedance of the Common Base amplifier is very low.
3. Current Gain of the Common Base amplifier is ‘Unity’. Thus, Output Current equals the Input Current.
4. Output Impedance of the Common Base amplifier is very high.

### APPLICATIONS OF THE COMMON BASE AMPLIFIER

1. Common Base amplifier is used as a First Stage of a cascaded

amplifier system when the source resistance is very low.

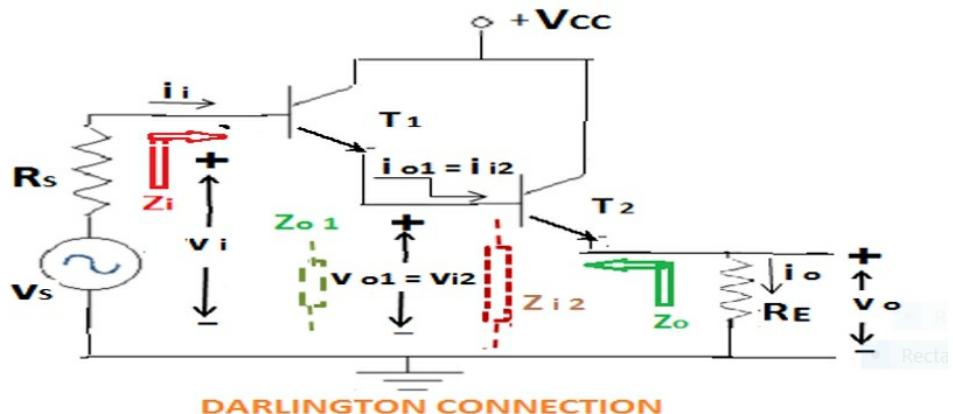
2. Common Base amplifier is used as a Last Stage of a cascaded amplifier system when the external load resistance is very high.

3. Common Base amplifier is used to amplify extremely high frequency signals.

## 6.10 DARLINGTON CONNECTION

### and DARLINGTON PAIR

- A Darlington Amplifier is a “Series Connection” (cascade) of two CC amplifiers.
- Recall that, while the Input Impedance of the CC amplifier is very high, the Output Impedance is low; while the Current Gain is high, the Voltage Gain is nearly unity.



**Fig –24:** -- Darlington Amplifier is the cascade of two CC stages. The Input Impedance of the second stage acts as the load impedance of the first stage.

- These properties are improved in the Darlington Amplifier, i.e., the **Input Impedance** is made **enormously higher** and **Output Impedance** is made **very much lower**. **Current Gain** becomes **much higher**; however, the **Voltage Gain remains nearly unity**. The Darlington Amplifier is shown in Fig. 23 above.

1. The load resistance of the second stage is the resistance  $R_E$  and the load resistance of the first stage is the Input Impedance of the second stage, which is shown by dashed line as  $Z_{i2}$ .
2. The first stage provides output current  $i_{o1}$  and voltage  $v_{o1}$ . The output current of the first stage is the input current of the second stage and the output voltage of the first stage is the input voltage of the second stage.
3. The second stage is the source of signal for the first stage. Hence, the output impedance,  $Z_{o1}$  of the first stage acts as the source resistance of the second stage.

With these, can use the formulae, derived for the analysis of the CC amplifier to analyze the Darlington amplifier as follows

**1. Current Gain  $A_I$ :** Current Gain of the two stages are

$$A_{I1} = \frac{i_{o1}}{i_i} \quad \& \quad A_{I2} = \frac{i_o}{i_{i2}}$$

The net Current Gain of the Darlington amplifier is

$$A_I = \frac{i_o}{i_i}$$

Expressing this as

$$A_I = \frac{i_o}{i_{i2}} \cdot \frac{i_{i2}}{i_i}$$

Since the output current of the first stage is the input current of the second stage.

$$\text{Hence } i_{i2} = i_{o1}$$

Substituting

$$A_I = \frac{i_o}{i_{i2}} \cdot \frac{i_{o1}}{i_i} = A_{I2} \cdot A_{I1}$$

Using Equation for Current Gain of CC amplifier, and assuming identical transistors, so that

$$h_{fe1} = h_{fe2}$$

$$A_{I1} = (1 + h_{fe1}) \quad \& \quad A_{I2} = (1 + h_{fe2})$$

Hence Current Gain of the Darlington Amplifier is

$$A_I = A_{I1} \cdot A_{I2} = (1 + h_{fe})^2 \quad \dots(5)$$

## **NUMERICAL VALUE CALCULATION**

Using typical values of the h-parameters of a transistor, as  $h_{fe} = 100$  we can calculate the quantity Current Gain as

$$A_I = (1 + 100)^2 = 10201$$

**2. Input Impedance:** The Net Input Impedance of the Darlington amplifier is the Input Impedance of the First Stage.

$$Z_i = Z_{i(B)1}$$

The Input Impedance of the first stage, which is a CC amplifier, is given by

$$Z_{i(B)1} = h_{ie1} + (1 + h_{fe1}) R_{L1}'$$

From the observations given earlier,  $R_{L1}'$ , i.e., the load connected to the emitter terminal of the first stage is the Input Impedance of the second stage. Hence

$$R_{L1}' = Z_{i(B)2} = h_{ie2} + (1 + h_{fe2}) R_E$$

Since the transistors are assumed to be identical, we have

$$h_{ie1} = h_{ie2} = h_{ie} \quad \& \quad h_{fe1} = h_{fe2} = h_{fe}$$

Substituting we have

$$Z_i = h_{ie} + (1 + h_{fe}) [h_{ie} + (1 + h_{fe}) R_E]$$

Simplifying

$$Z_i = h_{ie} (2 + h_{fe}) + (1 + h_{fe})^2 R_E \dots(6)$$

## **NUMERICAL VALUE CALCULATION**

Using typical values of the h-parameters of a transistor, as  $h_{fe} = 100$  and  $h_{ie} = 1.1 \text{ K}$ , and taking  $R_E = 1 \text{ K}$  we can calculate the quantity as

$$Z_i = 1100. (2 + 100) + (1 + 100)^2. 1000 = 1.031 \times 10^7 \Omega = 10.31 \text{ M } \Omega$$

**3. Voltage Gain:** The general expression for voltage gain

$$A_v = \frac{A_I \cdot R_L'}{Z_i}$$

Using the expressions for  $A_I$  and  $Z_i$  from Eq. (10 & (2) respectively and taking  $R_L' = R_E$  and substituting, we have

$$A_v = \left[ \frac{(1 + h_{fe})^2 \cdot R_E}{\{h_{ie}(2 + h_{fe}) + (1 + h_{fe})^2 \cdot R_E\}} \right] \quad |.....(7)$$

### NUMERICAL VALUE CALCULATION

Using typical values of the h-parameters of a transistor, as  $h_{fe} = 100$  and  $h_{ie} = 1.1$  K, and taking  $R_E = 1$  K we can calculate the quantity Voltage Gain as

$$A_v = \frac{(1+100)^2 \cdot 1000}{1100 \cdot (2+100) + (1+100)^2 \cdot 1000} = 0.989$$

**4. Output Impedance:** The Net Output Impedance of the Darlington amplifier is the Output Impedance of the Second Stage.

$$Z_o = Z_{o2}$$

Now, Output Impedance of a CC stage is given by

$$Z_{o2} = \frac{R_S + h_{ie}}{(1 + h_{fe})}$$

Where  $R_S$  is the internal resistance of the source. in case of the second stage  $R_S$  is nothing but the Output Impedance of the first stage

Thus;

$$Z_o = \frac{R_{S1} + h_{ie}}{(1 + h_{fe})} \quad \& \quad R_{S1} = \frac{R_S + h_{ie}}{(1 + h_{fe})}$$

Substituting for  $R_{S1}$  in the expression for  $Z_o$  we have

$$Z_o = \left[ \frac{\left\{ \left( \frac{R_s + h_{ie}}{1 + h_{fe}} \right) + h_{le} \right\}}{1 + h_{fe}} \right]$$

Simplifying and rearranging we have

$$Z_o = \frac{(R_s + h_{ie}) + h_{ie} \cdot (1 + h_{fe})}{(1 + h_{fe})^2} \quad \dots\dots(4)$$

### NUMERICAL VALUE CALCULATION

Using typical values of the h-parameters of a transistor, as  $h_{fe} = 100$  and  $h_{ie} = 1.1 \text{ K}$ , and taking  $R_E = 1 \text{ K}$  and  $R_S = 1 \text{ K}$  we can calculate the quantity Output Impedance as

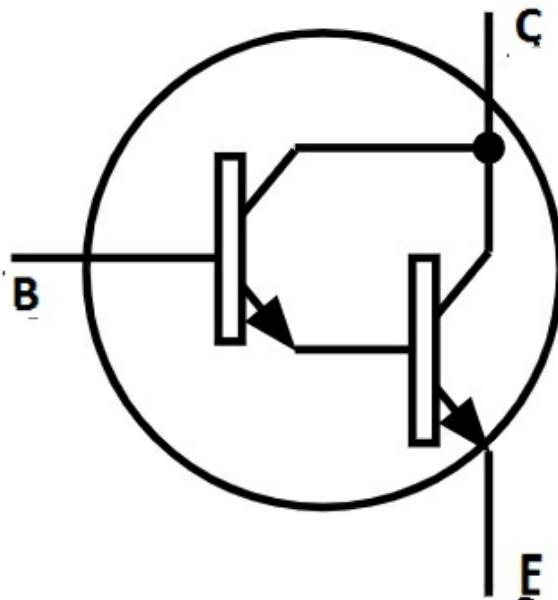
$$Z_o = \frac{(1000 + 1100) + 1100 \cdot (1 + 100)}{(1 + 100)^2} = 11.09 \Omega$$

### SUMMARY OF THE PROPERTIES OF DARLINGTON AMPLIFIER

1. Current Gain of the Darlington Amplifier is extremely high.
2. Input Impedance of the Darlington Amplifier is extremely high.
3. Voltage Gain of the Darlington Amplifier is essentially 'Unity'.
4. Output Impedance is very low.

### DARLINGTON PAIR

While analyzing the Darlington Amplifier that we assumed identical transistors. It may be difficult to **find transistors with exactly identical h-parameter values**. Therefore, manufacturers provide a pair of exactly identical transistors integrated as a Darlington Connection, and packaged in a single packet. Such a package is called a Darlington Pair.



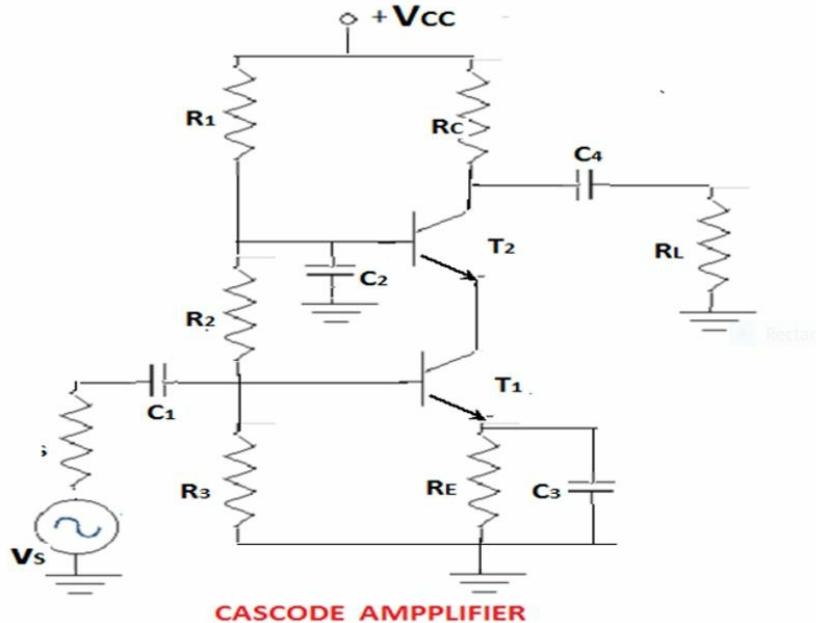
## **APPLICATIONS OF DARLINGTON AMPLIFIER / DARLINGTON PAIR**

1. The Darlington Amplifier / Darlington Pair is used in much of the same situations as the Emitter Follower, as enumerated above, but when extremely high Current Gain and input Impedances are required.
2. A Darlington Pair may be used as a “Single Transistor”,(since the two transistors are internally connected in parallel ), and used in any of the amplifier circuits we have studied so far.
3. Darlington Pair is used as a Current Source to drive high current loads.

### **6.11 CASCODE CONNECTION**

- **A common application of a CB amplifier is in the amplification of extremely high frequency signals,**
- Its major disadvantage is the extremely low input impedance. Since the input impedance is low, it tends to load the signal source, resulting in a high value of current flowing out of the source and thereby resulting in losses.

- This is overcome by a Cascode Amplifier. Cascode Connection is **the combination of a CE input stage and a CB output stage** as shown in the Fig –24.



**Fig – 25:** - Cascode Amplifier is the combination of a CE stage followed by a CB stage. This provides the applications of a CB amplifier, while at the same time overcoming the Loading Effect of a single CB stage.

- The input to the First Transistor (First Stage) is on the Base Terminal, the Emitter is at ground due to  $C_3$  and the output is taken out from the Collector to be fed to the next stage. Hence the **first stage is in the CE configuration**.
- In the next stage, i.e. the second transistor, the input is applied in the Emitter, the Base is bypassed to ground by  $C_2$  and the output is taken out at the Collector. Hence the **second stage is in CB configuration**.
- Since the first stage is a CE stage, the Input Impedance of the order of a few Kilo Ohms, while the second stage being CB enables high frequency applications. Thus this circuit **eliminates the primary disadvantage of a single stage CB amplifier vis – a – vis , the loading effect on a signal source**, at the same time retaining the property required for it's **primary application, viz,**

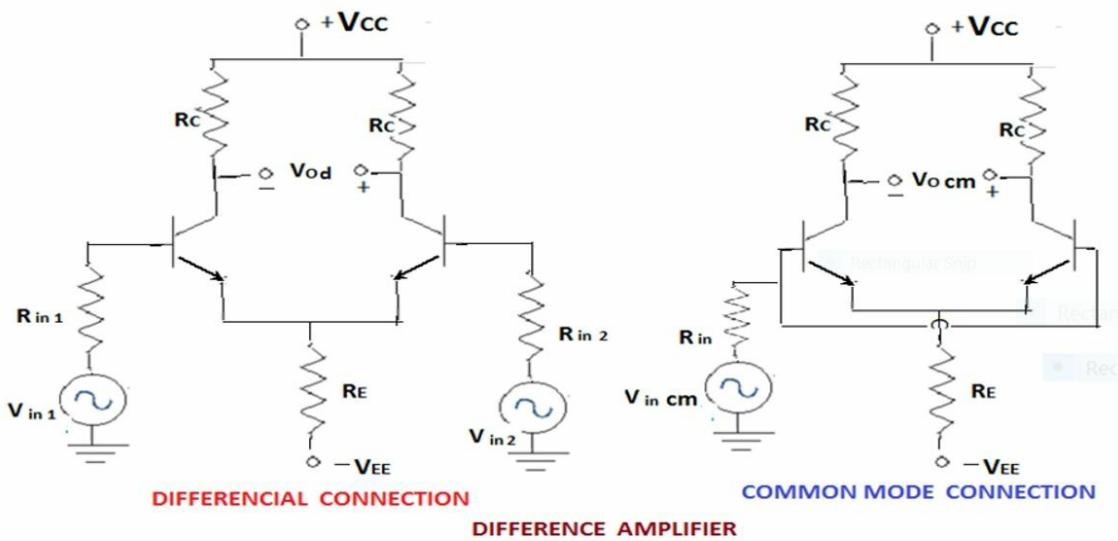
amplification of extremely high frequency signals.

### Voltage Gain

Assuming identical transistors and without going into complete analysis, it can be easily visualized that the Voltage Gain of the Cascode Amplifier should be

$$A_V = \frac{-h_{fe} \cdot R'_L}{h_{ie}}$$

## 6.12 DIFFERENCE AMPLIFIER



**Fig – 26 :** - Difference Amplifier is the connection of two identical transistors in CE configuration. Output voltage is proportional to the instantaneous arithmetic difference between the two input signals.

- Two identical transistors with two equal resistances \$R\_C\$, connected in the configuration of the circuit shown in Fig – 24, is known as a **Difference Amplifier**.
- This amplifier can be used to obtain a signal which is

**proportional to the difference between the two input signals  $v_1$  and  $v_2$ .**

- This configuration is used as the building block of a genre of IC's, namely **Operational Amplifiers (OPAMPS)**.

The Difference Amplifier can be connected either in **2 configurations, namely**

1.     **“Differential” configuration**
2.     **“Common Mode” configuration.**

### **Output Voltage & Input Impedance**

The instantaneous output voltage and Input impedance are given by the following,

$$v_o = \frac{R_C}{r_{e'}} (v_{in\ 1} - v_{in\ 2}) \quad \dots(5)$$

$$Z_i = 2 \beta R_E \quad \dots(6)$$

### **Differential Voltage Gain and CMRR**

The output voltage in Differential configuration is given by Eq.5. From this we obtain the quantity “**Differential Voltage Gain**” as

$$A_d = \frac{v_{od}}{(v_{in\ 1} - v_{in\ 2})} = \frac{R_C}{r_{e'}} \quad \dots(7)$$

In the Common Mode configuration, the Input and Output quantities are

$$v_{in\ 1} = v_{in\ 2} = v_{in\ cm} \quad \& \quad v_o = v_{ocm}$$

Hence, we can define a quantity “**Common Mode Voltage Gain**” as

$$A_{CM} = \frac{v_{ocm}}{v_{in\ cm}}$$

### **CMRR**

- In the ideal situation, if the two input terminals of the difference amplifier are driven by the same source, (in the Common Mode configuration),

$$v_{in\ CM} = v_{in\ 1} - v_{in\ 2} = 0.$$

- Hence, the output should have been zero, in terms of Eq.1 .
- However, if the two transistors and/or the resistances  $R_C$  are not exactly identical, there may appear some non-zero output voltage  $v_{ocm}$  .

- The quantity CMRR (Common Mode Rejection Ratio) defines a figure of merit of the Difference Amplifier. This quantity is defined as follows

$$\text{CMRR} = \frac{A_d}{A_{CM}} \quad \underline{\dots(8)}$$

Ideally  $A_d > 1$  and  $A_{CM} \rightarrow 0$

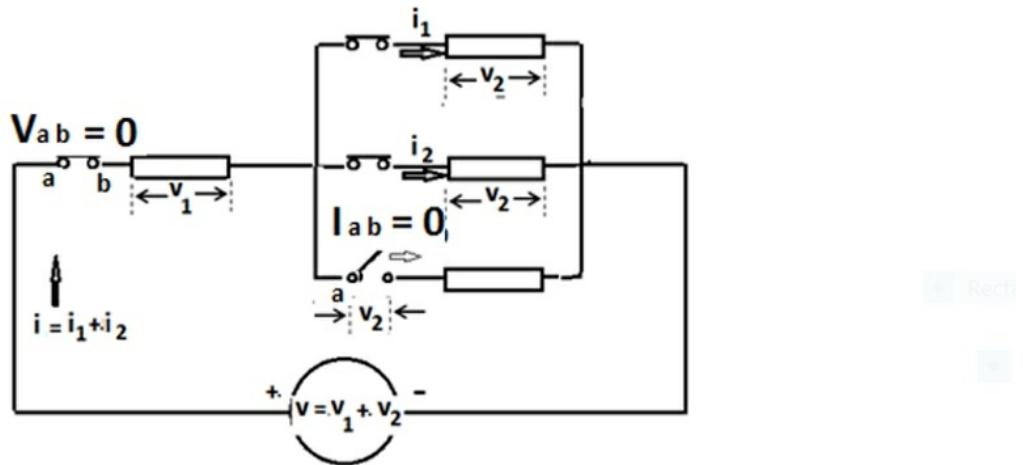
Hence CMRR should tend to infinity.

- However, in practice the quantity CMRR is of the order of  $10^7$ .  
**The higher the value of CMRR, the nearer the Difference Amplifier tends to ideal behavior.**

## Section-4

### 6.13 The Transistor Switch (BJT)

- Both the classes of the transistor, BJT, or FET can be configured as a switch with much greater efficiency and speed compared to a conventional mechanical switch.
- The underlying concept relevant to a switch is explained below. Consider a simple circuit as shown in the Fig. 25 below. In this circuit a few elements are connected in series and parallel combinations to a voltage source. The currents in various branches and the voltage drop across various elements are shown.



**Fig. 27:** – A simple circuit showing the underlying principles of a switch.

- When an ideal switch is **closed**, the voltage drop across the terminals must be zero and when it is **open**, the current through the switch must be zero.
- In other words, a closed switch is a short circuit between the terminals (a) and (b), conversely, an open switch is an Open Circuit between the terminals. These situations are shown in the figure.
- If these conditions are violated then Kirchhoff's Laws will be violated. In other words,

if

$$V_{ab} \neq 0$$

then

$$v \neq v_1 + v_2 \quad (\text{violation of KVL})$$

and if

$$I_{ab} \neq 0$$

then

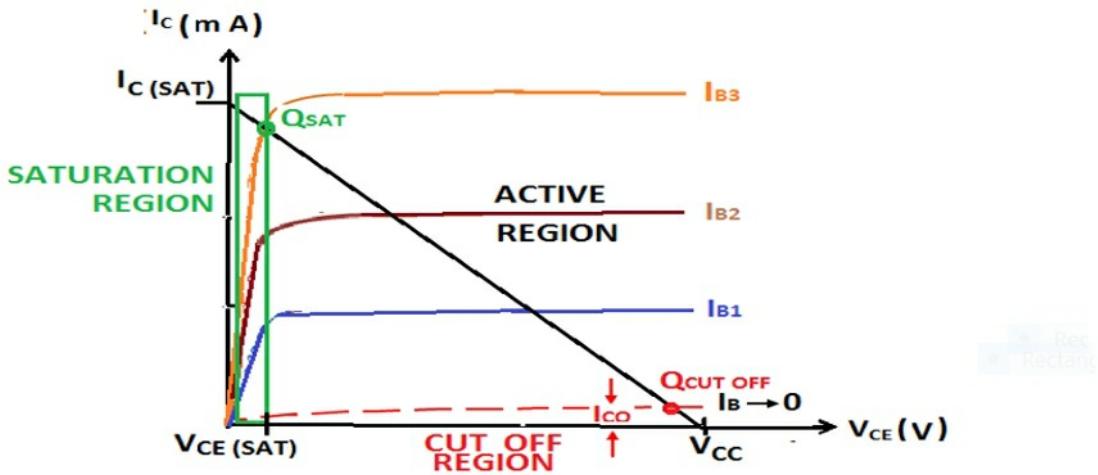
$$i \neq i_1 + i_2 \quad (\text{violation of KCL})$$

## A BJT SWITCH

- Behaviour of any electronic device is determined by the V-I Characteristic. The Output Characteristics of a BJT is reproduced below for reference.
- The Output Characteristics of the transistor have three distinct regions, namely, The Active Region, The Saturation Region and The Cut-Off region.
- We studied in the previous sections that the transistor is to be biased in the Active Region when it is to work as an amplifier. On the other hand, the same device can act as a Closed Switch when it is operating in the Saturation region and as an Open Switch when it operates in the Cut- Off Region.

**Saturation Region → Closed Switch: -**

- When a transistor is operating in the Saturation Region, the voltage across the Collector and Emitter Terminals is  $V_{CE} = V_{CE(SAT)}$ . The numerical value of  $V_{CE(SAT)}$  is very close to zero. On the other hand, the current  $I_C$ , flowing from Collector to Emitter is a high value equal to  $I_{C(SAT)}$ .
- Thus, there exists a Short Circuit between the C and E terminals of the transistor, in other words, **the Saturation region of a BJT is the equivalent of a Closed Switch.**

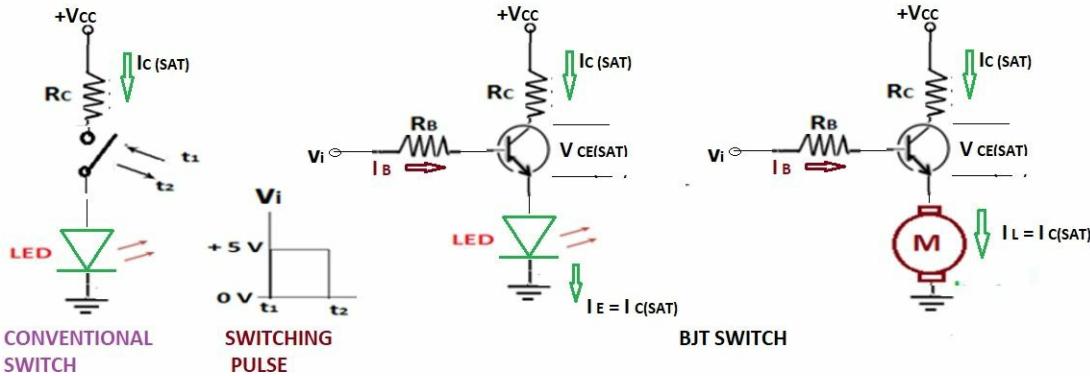


**Fig – 28 : – A BJT is equivalent to a **closed switch** when it is operating in The **Saturation Region** and as an **open switch** when it is operating in The **Cut – Off Region**.**

### Cut-Off Region → Open Switch: -

- When a transistor is operating in the Cut-Off Region, the voltage across the Collector and Emitter Terminals is  $V_{CE} = V_{CC}$ . On the other hand, the current  $I_C$ , flowing from Collector to Emitter is of a very low value equal to  $I_{CO}$ , which is of the order of a fraction of a microampere, hence it can be neglected.
- Thus, there exists an Open Circuit between the C and E terminals of the transistor, in other words, **the Cut-Off Region of a BJT is the equivalent of an Open Switch.**

This is illustrated by means of the following figure.



**Fig – 29:** – A BJT Switch is shown driving a DC load in the form of an LED or a DC Motor. When the BJT is driven into saturation by the voltage pulse at  $t=t_1$ , the LED glows, or the motor turns on. On the other hand, when the BJT goes into Cut Off at  $t= t_2$  the LED stops glowing or the motor stops running.

- When a positive voltage is applied at the Base at  $t = t_1$  it drives the Base Current  $I_B$  to a high enough value  $I_{B3}$  so that the BJT is driven into Saturation. Hence it acts as a Closed Switch between the terminals C and E allowing a current  $I_{C(SAT)}$  to pass through and making the LED glow.
- On the other hand, when input voltage pulse drops to 0 at  $t = t_2$  , the BJT is driven into Cut Off and it acts as an Open Switch, thus turning off the LED.
- The equivalent mechanical switch is also shown alongside. Instead of an LED any other DC load, for example a DC motor can also be driven by this arrangement.

The most suitable application of the transistor as a switch is in the form of various logic gates integrated in the form of ICs. The physical volume occupied by a junction transistor or an FET is very small. Hence millions of such devices can be integrated on a single silicon wafer, which forms the basis for modern electronic devices.

#### TUTORIAL-4

**Example 12: Design Problem:** Design a BJT switch to drive a DC motor rated at 12 V, 500 mA. Use a Si transistor with  $\beta = 100$ .

**Solution:** Referring to the design requirement we must have

$$V_{CC} = V_L = 12 \text{ V}$$

$$I_L = I_{C(SAT)} = 500 \text{ mA}$$

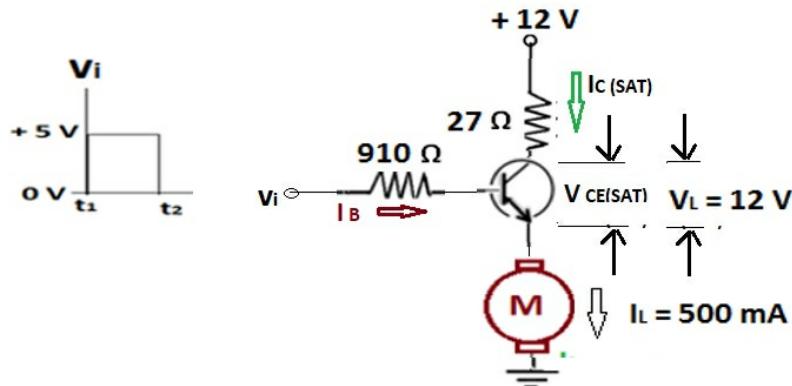
$$\therefore R_C = \frac{V_L}{I_L} = \frac{V_{CC}}{I_{C(SAT)}} = \frac{12 \text{ V}}{500 \text{ mA}} = 0.024 \text{ K} = 24 \Omega$$

$$I_B = \frac{I_{C(SAT)}}{\beta} = \frac{500}{100} = 5 \text{ mA}$$

$$\therefore R_B = \frac{V_i - V_{BE}}{I_B} = \frac{(5 - 0.7)V}{5 \text{ mA}} = 0.86 \text{ K} = 860 \Omega$$

In practice the nearest higher standard value of resistance available in the market is to be used in the circuit implementation. In this case we use

$$R_B = 910 \Omega \quad \text{AND} \quad R_C = 27 \Omega$$



----- BJT-BJT-BJT-BJT -----

# CHAPTER – VII

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## CASCADED AMPLIFIER

### *CASCADED AMPLIFIER*

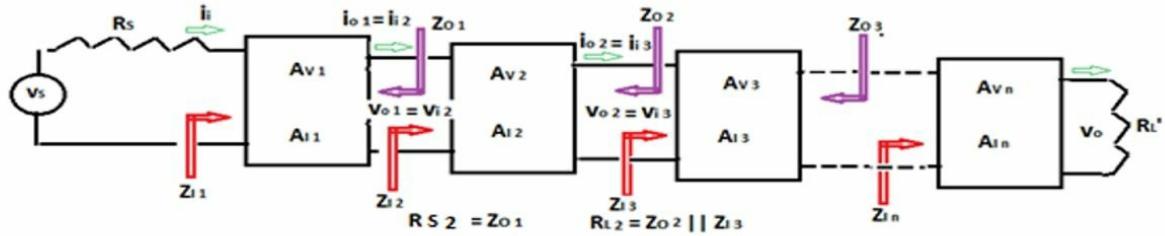
#### Section-1

#### ***COUPLING SCHEMES IN CASCADED AMPLIFIERS***

##### **7.1 Concept of Cascading**

- Amplifiers are required for the purpose of amplifying the signals generated by converting physical processes into electrical signals by the Primary Transducers, such as a microphone. The Primary signal produced by the transducer is of very low power levels.
- These signals have to be significantly amplified before being made useful for the purposes they are meant to be used for, say, driving a bank of Loud Speakers in an auditorium, or for driving an Electrical Motor, etc.
- A single stage Small Signal amplifier can produce a voltage output of only a few milli volt with the output current being in micro ampere range, at best. Thus, it is apparent that a single stage of amplification will not suffice. (The reader is referred back to the solved numerical examples of the previous chapter).
- In practice, a series of small signal amplifiers are used one after the other in such a manner that the preceding stage acts as the ‘Source’ and the succeeding stage acts as the ‘Load’. This is called a “**Cascaded Amplifier**”.
- Since this stage also performs the First Stage amplification, it is

also called “**Pre-Amplifier**”. The Fig.- 1 shows the schematic of a Cascaded Amplifier.



**Fig. – 1:** - Net Gain in a Cascaded Amplifier is the product of the Gains of the individual stages. The Net Load Resistance of each stage is the parallel combination of the input impedance of the present stage and the output impedance of the next stage. The Source Resistance of each stage is the output impedance of the previous stage.

**Analysis:** The First stage amplifies the signal supplied by the source to produce the output

$$v_{o1} = A_{V1} v_s \quad \& \quad i_{o1} = A_{I1} i_s$$

Where

$$A_{V1} = \text{Voltage Gain of the First Stage} = \frac{v_{o1}}{v_s}$$

And

$$A_{I1} = \text{Current Gain of the First Stage} = \frac{i_{o1}}{i_s}$$

The First Stage acts as the source of signal for the second stage.

Hence

$$v_{i2} = v_{o1} \quad \& \quad i_{i2} = i_{o1}$$

This is amplified by the Second Stage as

$$v_{o2} = A_{V2} v_{i2} = A_{V2} v_{o1} \quad \& \quad i_{o2} = A_{I2} i_{i2} = A_{I2} i_{o1}$$

Where

$$A_{V2} = \text{Voltage Gain of the Second Stage} = \frac{v_{o2}}{v_{i2}} = \frac{v_{o2}}{v_{o1}}$$

And

$$A_{I2} = \text{Current Gain of the Second Stage} = \frac{i_{o2}}{i_{i2}} = \frac{i_{o2}}{i_{o1}}$$

This continues stage by stage as

$$v_{03} = A_{V3} v_{i3} = A_{V3} v_{02} \quad \& \quad i_{03} = A_{I3} i_{i3} = A_{I3} i_{02}$$

Where

$$A_{V3} = \text{Voltage Gain of the Second Stage} = \frac{v_{03}}{v_{i3}} = \frac{v_{03}}{v_{o2}}$$

And

$$A_{I3} = \text{Current Gain of the Second Stage} = \frac{i_{03}}{i_{i3}} = \frac{i_{03}}{i_{02}}$$

And so, on up to the  $n^{\text{th}}$  stage, on to the load as

$$v_0 = v_{o(n)} = A_{Vn} v_{0(n-1)} \quad \& \quad i_0 = i_{o(n)} = A_{In} i_{0(n-1)}$$

Where

$$A_{Vn} = \text{Voltage Gain of the } n^{\text{th}} \text{ Stage} = \frac{v_{0n}}{v_{0(n-1)}}$$

And

$$A_{In} = \text{Current Gain of the } n^{\text{th}} \text{ Stage} = \frac{i_{0n}}{i_{0(n-1)}}$$

The overall Voltage Gain, the overall Current Gain and the overall Power Gain of the Cascaded Amplifier is

$$A_V = \frac{v_o}{v_s} \quad \underline{=} \quad A_I = \frac{i_o}{i_s} \quad : \quad G = \frac{P_o}{P_i}$$

These can be expressed as

$$A_V = \frac{v_o}{v_s} = \frac{v_{01}}{v_s} \cdot \frac{v_{02}}{v_{01}} \cdot \frac{v_{03}}{v_{02}} \dots \frac{v_{0(n-1)}}{v_{0(n-2)}} \cdot \frac{v_{0n}}{v_{0(n-1)}}$$

OR

$$A_V = A_{V1} \cdot A_{V2} \cdot A_{V3} \cdot \dots \cdot A_{Vn} \dots (1)$$

And

$$A_I = \frac{i_o}{i_s} = \frac{i_{o1}}{i_s} \cdot \frac{i_{o2}}{i_{o1}} \cdot \frac{i_{o3}}{i_{o2}} \cdots \frac{i_{o(n-1)}}{i_{o(n-2)}} \cdot \frac{i_{on}}{i_{o(n-1)}}$$

OR

$$A_I = A_{I1} \cdot A_{I2} \cdot A_{I3} \cdots A_{In} \quad \underline{\dots(2)}$$

Since power is the product of voltage and current and the Power gain of an amplifier is the product of  $A_V$  and  $A_I$ , we have

$$G = \frac{P_o}{P_i} = \frac{V_o \cdot i_o}{V_s \cdot i_s}$$

$$G = \left( \frac{V_{o1}}{V_s} \cdot \frac{V_{o2}}{V_{o1}} \cdot \frac{V_{o3}}{V_{o2}} \cdots \frac{V_{on}}{V_{o(n-1)}} \right) \cdot \left( \frac{i_{o1}}{i_s} \cdot \frac{i_{o2}}{i_{o1}} \cdot \frac{i_{o3}}{i_{o2}} \cdots \frac{i_{on}}{i_{o(n-1)}} \right)$$

$$\therefore G = (A_V \cdot A_{V2} \cdot A_{V3} \cdots A_{Vn}) \cdot (A_{I1} \cdot A_{I2} \cdot A_{I3} \cdots A_{In})$$

$$\therefore G = A_V \cdot A_I$$

OR

$$G = G_1 \cdot G_2 \cdot G_3 \cdots G_n \quad \underline{\dots(3)}$$

 Rectangular Snip

### Gain in dB.

Gain of an amplifier is expressed as a ratio, i.e. without any unit being assigned to it.

Power Gain can also be defined in the Logarithmic Scale with a **dB (deci Bell)** unit. This dB unit is defined as –

$$G_{(dB)} = 10 \log G = 10 \log \left( \frac{P_o}{P_i} \right) \quad \underline{\dots(4)}$$

We had also expressed Power Gain as

$$G = A_V \cdot A_I$$

It is a common design practice to design each stage of a cascaded amplifier with equal numerical values for Current gain and Voltage Gain

Thus

$$|A_V| = |A_I|$$

&

$$G = A_V^2 = A_I^2$$

Thus, in terms of Eq. – 4 we have

$$G_{(dB)} = 20 \log (A_V) \quad \dots(5 \text{ (a)})$$

$$G_{(dB)} = 20 \log (A_I) \quad \dots(5 \text{ (b)})$$

Overall Gain of a cascaded amplifier as the product of the gains of each stage (Eq. 1 to Eq 3). Thus, in the logarithmic dB scale the Overall gain will be

$$G_{(dB)} = G_{1(dB)} + G_{2(dB)} + \dots + G_{n(dB)} \quad \dots(6)$$

## TUTORIAL-1

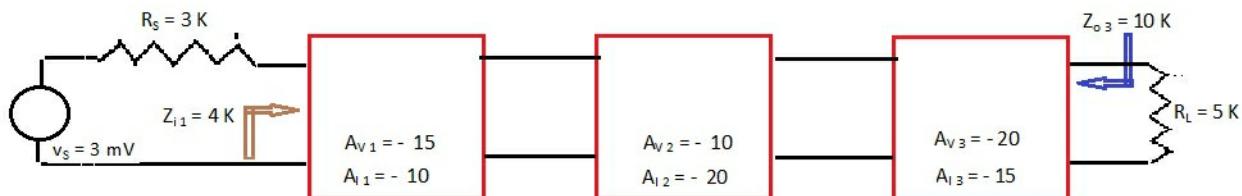
**Example 1:** – A 3-stage Cascaded Amplifier is composed of stages with the following parameters.

$$A_{V1} = -15; A_{V2} = -10; A_{V3} = -20; A_{I1} = -10;$$

$$A_{I2} = -20; A_{I3} = -15 :: R_S = 3 K ;$$

$$Z_{i1} = 4 K ; Z_{o3} = 10 K ; R_L = 5 K ; v_S = 3 mV$$

Calculate output voltage, output current, output power and Overall Gain in dB.



**SOLUTION:** –Overall Voltage Gain is

$$A_V = A_{V1} \cdot A_{V2} \cdot A_{V3}$$

$$A_V = (-15) \cdot (-10) \cdot (-20) = -3000$$

**Overall Current Gain is**

$$A_I = A_{I1} \cdot A_{I2} \cdot A_{I3}$$

$$A_I = (-10) \cdot (-20) \cdot (-15) = -3000$$

$\therefore$  Overall power Gain is

$$G = A_V \cdot A_I = (-3000) \cdot (-3000) = 9000000$$

**AND**

**Gain in dB**

$$G_{dB} = 10 \log (9000000) = 69.54 \text{ dB}$$

Since we have a Source resistance input to the first stage is less than  $v_S$ . If we consider the source resistance, the net Voltage Gain is

given by

$$A_{Vs} = \frac{Z_I}{(Z_I + R_S)} \cdot A_V$$

Substituting

$$A_{Vs} = \frac{4}{(4+3)} \times 3000 = 1714.3$$

$$\therefore v_o = A_{Vs} \cdot v_s = 1714.3 \times 3 = 5142.8 \text{ mV} = 5.143 \text{ V}$$

$\therefore$  Output Current

$$i_o = \frac{v_o}{R_L} = \frac{5.143}{5 \times 10^3} = 0.00108 \text{ A} = 1.08 \text{ mA.}$$

Recalculating stage by stage we have

$$\text{Stage - 1 } G_1 = A_{V1} \cdot A_{I1} = (-15) \cdot (-10) = 150$$

$$G_1 \text{ dB} = 10 \log (150) = 21.76 \text{ dB}$$

$$\text{Stage - 2 } G_2 = A_{V2} \cdot A_{I2} = (-10) \cdot (-20) = 200$$

$$G_2 \text{ dB} = 10 \log (200) = 23.01 \text{ dB}$$

$$\text{Stage - 3 } G_3 = A_{V3} \cdot A_{I3} = (-20) \cdot (-15) = 300$$

$$G_3 \text{ dB} = 10 \log (300) = 24.77 \text{ dB}$$

$$\text{Overall Power Gain } G = G_1 \cdot G_2 \cdot G_3$$

$$= 150 \times 200 \times 300 = 9000000$$

AND

$$\begin{aligned} G_{\text{dB}} &= G_1 \text{ dB} + G_2 \text{ dB} + G_3 \text{ dB} \\ &= 21.76 + 23.01 + 24.77 = 69.54 \end{aligned}$$

Another Recalculation

We can also calculate Overall Power Gain in dB as

$$G_{\text{dB}} = 20 \log (|A_V|) = 20 \log (3000) = 69.54 \text{ dB}$$

Also

$$G_{\text{dB}} = 20 \log (|A_I|) = 20 \log (3000) = 69.54 \text{ dB}$$

## 7.2 COUPLING BETWEEN STAGES IN CASCADED

## **AMPLIFIERS.**

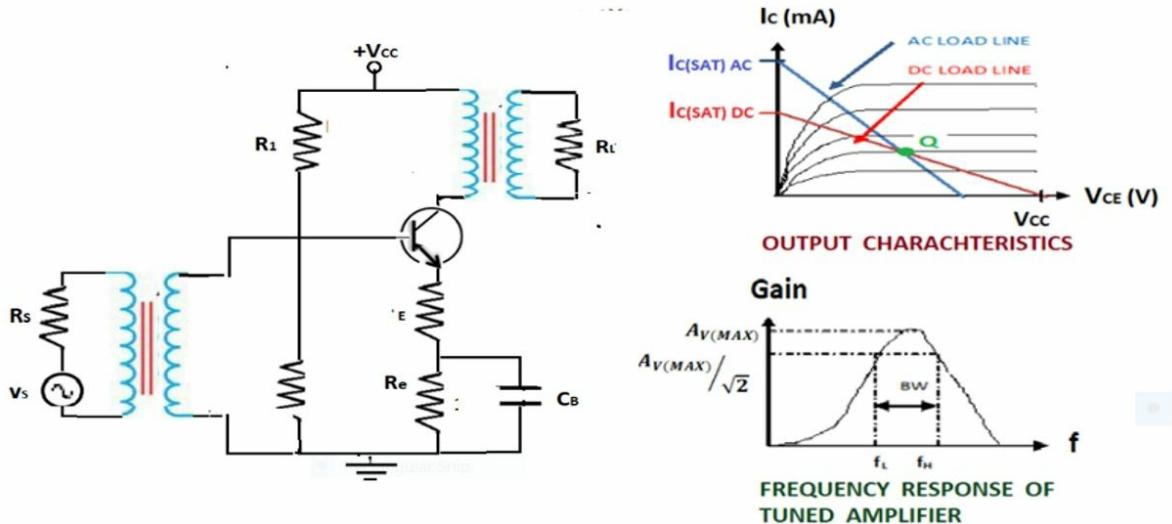
- Various stages of a cascaded amplifier need to be coupled to each other in such a way that the amplified signal from the preceding stage is fed as input into the succeeding stage without any attenuation. In doing this it is to be **ensured that “Maximum Power Transfer Theorem”** is satisfied.
- Recalling the statement of the Maximum Power Transfer Theorem – **maximum power from a source of an electrical circuit is transferred to the load if the output impedance of the source part equals the input impedance of the load part.**
- In a Cascaded Amplifier, the preceding stage acts as the source for the succeeding stage. Thus, the output impedance of the preceding stage has to be equal to the input impedance of the succeeding stage.
- Further, the internal resistance  $R_S$  of the signal source also has to be matched with the input impedance of the First Stage to ensure that maximum amount of signal power is transferred to the amplifier cascade.
- The output impedance of the Last Stage has to be matched to the external load resistance  $R_L$ , so that maximum amount of the amplified signal power is transferred to the load.
- In this process of coupling signal from one stage to the other the Coupling Arrangement also has to ensure that the DC Bias of each stage stays independent of each other.

**Taking into consideration the above, in practice, various stages of a cascaded amplifier can be coupled to each other as well as the signal source and the external load in 3 different ways- as tabulated below -**

1. **Transformer Coupling.**
2. **Direct Coupling.**
3. **R-C Coupling.**

### **Transformer Coupling.**

The signal from the source to the input point of the amplifier is connected via a transformer. The input signal from the source is connected to the primary side and the secondary side is connected to the input point of the amplifier. Similarly, the output point of the amplifier is connected to the primary of the transformer and the load is connected to the secondary. This is shown in the figure below.



**Fig. – 2 : – Single Stage Transformer Coupled Amplifier. The input and the output signals are coupled by means of a transformer with an appropriate turn's ratio for Impedance matching.**

## ADVANTAGES

- As per Maximum Power Transfer Theorem,  $R_s$  must match with  $Z_{i(T)}$  and  $Z_o$  must match with  $R_L$ . Similarly, in case of cascaded amplifier, the  $Z_o$  of each stage must match with  $Z_{i(T)}$  of the subsequent stage. In a transformer, the secondary resistance reflected onto the primary is given by  $n^2 \cdot R$ , where  $1 : n$  is the turn's ratio. Thus by using a transformer of the appropriate turns ratio, the impedance connected at the primary side can be exactly matched with the reflected impedance of the secondary side.
- Since  $R_C$  for the DC equivalent circuit is very low (since it is

the internal resistance of the primary coil), the value of  $I_{C(sat)}$  given by

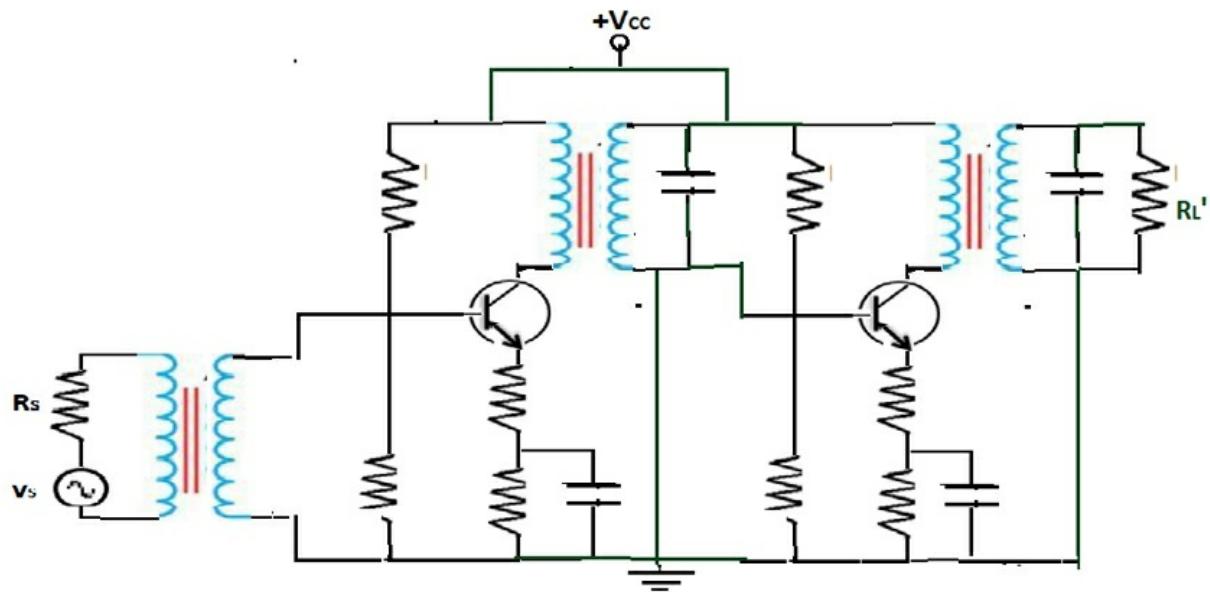
$$I_{C(sat)} = \{ V_{cc} / ( R_c + R_E ) \},$$

will be high. Thus, a larger range of the active region of the transistor will be available to the amplifier. This is shown with the red and blue coloured DC and AC Load Lines, respectively, in the figure above. Using a larger region of the output characteristic results in more power handling capacity for the amplifier. This results in greater efficiency.

3. By connecting a capacitor of an appropriate value across the primary and secondary coils, the coupling between various stages can be tuned to the resonant frequency of the L-C combination. Such tuned amplifiers are used for high efficiency – high fidelity amplification.

## DISADVANTAGES

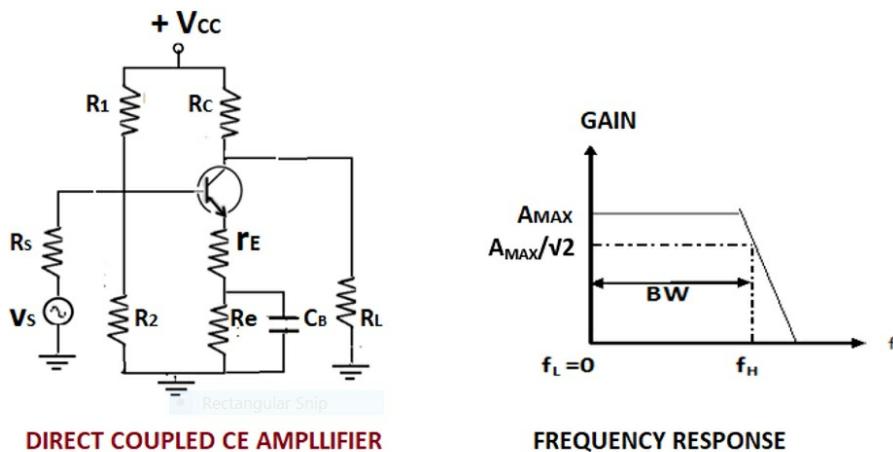
1. The primary disadvantage of transformer coupling is that the amplifier becomes bulkier because of the presence of the transformers.
2. Not suitable for integration in ICs.
3. Band width is low.



**Fig. – 3: – Transformer Coupled Cascaded Tuned Amplifier.**

### Direct Coupling.

The signal from the source is connected directly to the input point of the amplifier. Similarly, the output point of the amplifier is also directly connected to the load. This is shown in the figure below.



**Fig. – 4 : – Single Stage Direct Coupled Amplifier.**

### ADVANTAGES

1. This can amplify very low frequency signals, including DC (DC signal has a frequency equal to zero).

**REASON:-** When there is no coupling capacitor at the input terminal then signal at any frequency, particularly at low frequency, can go into the input terminal without attenuation. Similarly, the amplified signal at such low frequencies will be able to go into the  $R_L$  from the output terminal without any attenuation. However, at high frequencies gain drops due to the presence of “Stray Capacitance”.

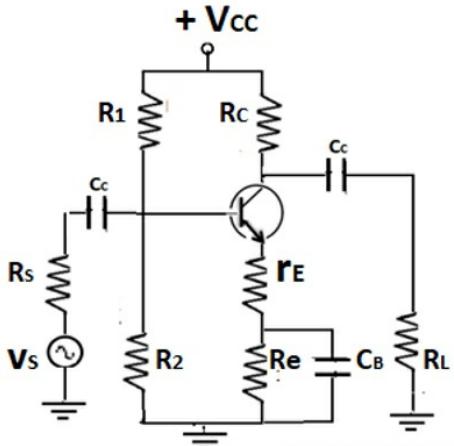
2. The circuit is Light-Weight (not bulky), therefore very much suitable for integration in the form of ICs.

### **DISADVANTAGES**

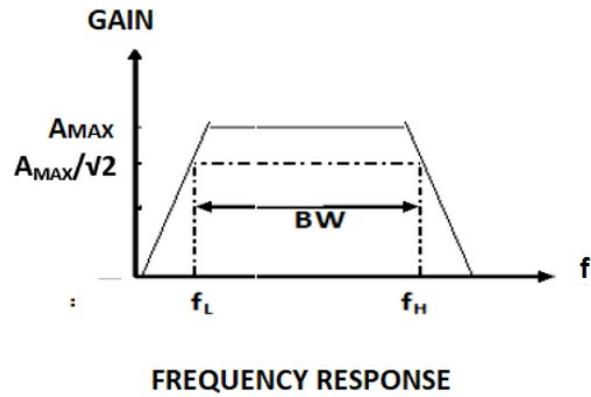
1. There is no DC Isolation of signal source and the external load resistance from the DC bias of the amplifier. Also, in cascaded stages, the biasing conditions of one stage may effect the biasing conditions of the previous as well as the following stage.

### **R-C Coupling.**

In RC Coupled Amplifiers, the coupling between the stages, as well as the coupling of the amplifier to the source and the external load resistance is by means of “Coupling Capacitors”  $C_c$ .



RC COUPLED CE AMPLIFIER



**Fig. – 5 : – Single Stage R-C Coupled Amplifier.**

#### ROLE OF $C_C$ & $C_B$ :-

- The primary role of Coupling Capacitor  $C_c$  is to couple the signal from the source to the input point of the amplifier as well as that between the intermediate stages and from the output point of the amplifier to the external load resistance.
- The primary role of  $C_B$  is to bypass the AC signal from the resistance  $R_e$ , connected in the emitter terminal, so that the resistance at the emitter in the AC equivalent circuit is  $r_E$ , where  $r_E \ll R_e$ . In this way the voltage gain of the amplifier is kept at a desired high enough value (recall that  $A_v = -R_L' / (r_e' + r_E)$ , where  $r_e'$  is the resistance of the junction  $J_1$  when it is in forward bias). This resistance  $R_e$  comes into effect only in the DC equivalent circuit (i.e. the biasing circuit). In the biasing circuit the net resistance of the emitter circuit is  $R_E = (r_E + R_e)$ . A high resistance is required in order to provide a good stability w.r.t. temperature variations (recall that in the equation for Stability Factor the ratio  $R_b/R_E$  should tend towards infinity in order that the value of S tends to the desired value of unity).
- Both  $C_C$  and  $C_B$  play a significant role in the shape of the “Frequency Response Curve” of the RC Coupled Amplifier at low

frequencies. Within the working range of frequencies from  $f_L$  to  $f_H$  (i.e. within the Band Width BW), the capacitive reactance provided by  $C_c$  and  $C_B$  tends to zero since frequency 'f' is high enough ( $X_C = 1/2\pi f C$ ). But at frequencies lower than  $f_L$  the capacitive reactance due to  $C_c$  is high. Thus the signal experiences high impedance due to  $C_c$ , thus less amount of signal gets coupled to the input terminal of the amplifier. Since signal level at input is low, the output signal at the output terminal of the amplifier is also low, resulting in reduction of Gain. At  $f = 0$ ,  $X_C = \infty$ . Thus signal is completely blocked and gain drops to zero.

- Capacitive reactance of  $C_B$  at the working range of frequencies tends to zero as explained earlier. Since  $C_B$  is in parallel with  $R_e$ , the parallel combination of  $R_e$  and  $X_C$  equals zero. Thus the resistance connected to the emitter terminal in the AC equivalent circuit is only  $r_E$ . Thus  $A_v$  is of the desired value provided by expression  $A_v = -R_L' / (r_e' + r_E)$ . If the frequency of the signal is less than  $f_L$  then  $X_C$  will be high. Thus net impedance at the emitter terminal in the AC equivalent circuit will be greater than  $(r_e' + r_E)$ . Therefore,  $A_v$  will get reduced.

## FREQUENCY RESPONSE OF RC COUPLED AMPLIFIER

1. **Mid Frequency Response** :- The working range of frequencies is termed as the 'Mid-Frequency Range' or the 'Band Width'.

In the Mid Frequency Range, the h-parameter values of the transistor are assumed to be constant. In the h-parameter model the expressions of  $A_I$  and  $A_v$  are as follows—

$$A_I = \frac{-h_{fe}}{1 + h_{oe} \cdot R_L'} \quad :: \quad A_v = \frac{A_I \cdot R_L'}{Z_I}$$

Where,

$$Z_I = h_{ie} + h_{re} \cdot A_I \cdot R_L'$$

All of these expressions are functions of the h-parameter values and the

resistance  $R_L'$ . All these quantities are independent of signal frequency. Hence  $A_{max}$  is shown as constant in the ‘Mid Frequency Range’ in the Fig. 5.

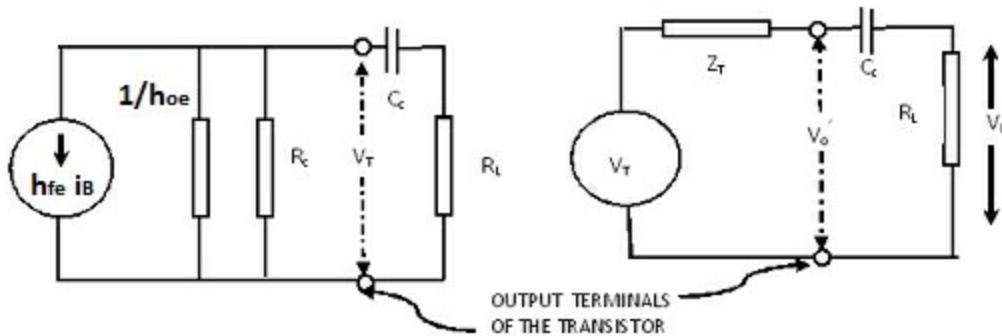
## 2. Response in Low Frequency Range (Low Frequency Response) :-

Figure shows the coupling capacitor  $C_C$  between the output stage of the h-parameter model of a transistor with the admittance  $h_{oe}$  being shown as the resultant impedance  $1/h_{oe}$ , from the earlier stage with the **next stage** being shown as the **load  $R_L$** .

In the first figure, there exists a Thevenin’s voltage  $V_T$  at the output terminals of the transistor. The Thevenin’s equivalent impedance  $Z_T$  is the parallel combination of  $1/h_{oe}$  and  $R_C$ .

**In the Thevenin’s equivalent, we have shown the output voltage of the amplifier as  $V_0'$ .**

The coupling capacitor couples this to the external load resistance  $R_L$  and the output voltage across the load is  $V_L$ .



**Fig. 6. :- Low Frequency Equivalent Circuit for RC Coupled Amplifier.**

From this, the “Voltage Transmission Factor” of the coupling capacitor will be

$$A' = V_L / V_0'$$

In the figure, we have

$$V_L = \frac{R_L \cdot V_o'}{R_L - j X_C}$$

$$\text{Where } X_C = 1/(2\pi f C_C)$$

With this we get the Voltage Transmission Ratio as

$$A' = \frac{V_L}{V_o'} = \frac{R_L}{R_L - j \{1/(2\pi f C_C)\}}$$

Dividing both Numerator and Denominator by  $R_L$  we get

$$A' = \frac{1}{1 - j \{1/(2\pi f R_L C_C)\}}$$

$R_L C_C$  is the “Time Constant” of a RC circuit, which has dimensions of ‘T’ (in units of ‘second’). Reciprocal of time or  $s^{-1}$  represents “Frequency” in the units of Hz. Thus the term ( $1/2\pi f R_L C_C$ ) has the dimensions of frequency in the units of Hz.

Let this term be denoted by a frequency term  $f_L = 1/2\pi f R_L C_C$

Thus we get the quantity “Voltage Transmission Ratio” as

$$A' = \frac{1}{1 - j \{f_L/f\}} \quad \underline{\dots(7)}$$

Evaluating the Magnitude

$$|A'| = \sqrt{\frac{1}{1 - \{f_L/f\}^2}} \quad \underline{\dots(8)}$$

Evaluating this at various frequencies we get –

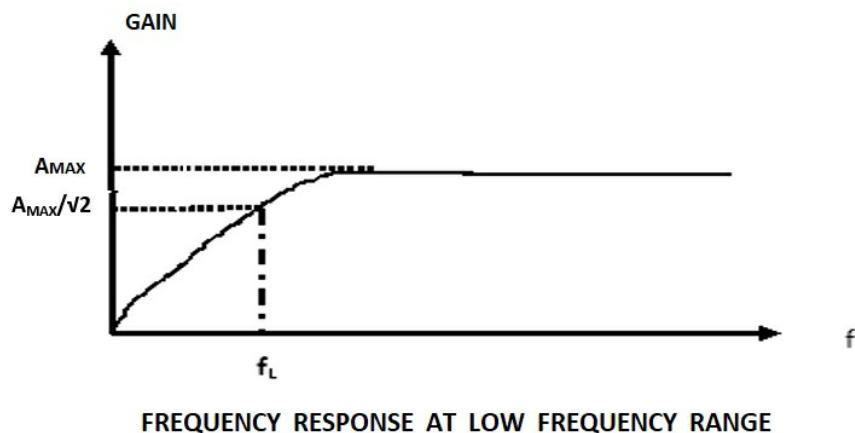
- At some **high frequency**  $f \gg f_L$  the term  $(f_L/f)^2$  will lend to zero. Hence  $|A'| \approx 1$ . This means that all the signal available at the output terminal of the amplifier will be transmitted to the load. Hence gain will be the maximum value as determined by the h-parameter model. In other words, we have a gain equal to  $A_{max}$ . This term  $A_{max}$  is constant since it is determined by the h-parameter values, as described above .
- At a frequency  $f = f_L$  the denominator of the equation will become equal to  $\sqrt{2}$ . Thus  $A' = A_{MAX}/\sqrt{2}$ .

In other words, only  $1/\sqrt{2}$  times the output signal will be transmitted to the load. Thus gain will drop to  $1/\sqrt{2}$  times the

maximum gain.

- At very low frequencies when  $f_L \ll f$  the denominator of the expression for  $A'$  tends to  $\alpha$ . Thus we get  $A' \approx 0$ . Thus at low frequencies, the gain drops down and becomes zero when signal frequency is zero. A zero frequency signal means a DC signal.

This discussion is illustrated in the plot of Gain vs frequency curve for the ‘Low Frequency Range’ as shown below.



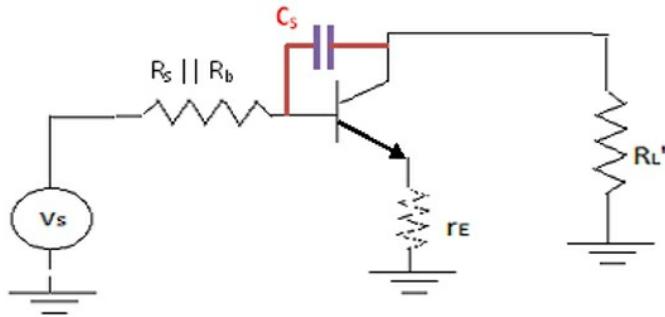
### 3. Response in the High Frequency Range (High Frequency Response) :-

- At high frequencies also the gain gradually drops off. This is proved as follows. In a transistor, the Collector-Base junction  $J_2$  is reverse biased. In a reverse biased PN junction the width of the depletion region is large. The “Space Charges” of the Depletion Region gives rise to a capacitance, called ‘Transition Capacitance’ and is denoted by  $C_T$ . In addition to this there exists an ‘Inter-Electrode Capacitance’ in between the metal terminals of a transistor.

These two capacitances occur in parallel, hence they add up to form the net ‘Stray Capacitance’  $C_S$ . The amount of stray capacitance  $C_S$  is so less that at low frequencies the reactance is very high ( $X_C = 1/2\pi f C$ ). Thus, the amplifier performance is not affected by low frequency signals.

- However, at high frequencies greater than a certain value  $f_H$ , the

capacitive reactance due to the stray capacitance is very low. The effect of this capacitance is to offer very low impedance to high frequency signals. Thus high frequency signals at the input (base terminal) are directly shunted to the output (collector terminal), without passing drops off as signal frequency increases.



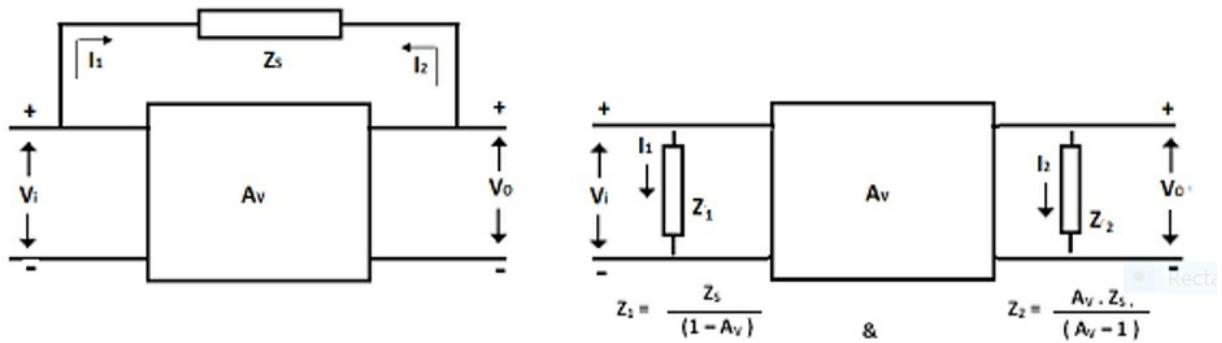
HIGH FREQUENCY AC EQUIVALENT CIRCUIT OF AN AMPLIFIER WITH STRAY CAPACITANCE  $C_s$ . THE EFFECT OF THIS CAPACITANCE IS THAT A PORTION OF THE INPUT SIGNAL IS BYPASSED FROM THE INPUT TERMINAL (BASE) DIRECTLY TO THE OUTPUT TERMINAL (COLLECTOR) WITHOUT GETTING AMPLIFIED BY THE TRANSISTOR. THUS GAIN IS REDUCED. THIS EFFECT TAKES PLACE ONLY AT HIGH FREQUENCIES

Rectang

**Fig. 7.: - High Frequency Equivalent Circuit for RC Coupled Amplifier.**

### MILLER'S THEOREM (Only Statement is given, Proof is not given)

- Any amplifier having a Voltage Gain equal to  $A_V$ , and an impedance  $Z_S$ , connected in shunt between the input and output terminals in such a way that a part of the input signal is shunted to the output, is equivalent to a circuit in which the 'Shunt Impedance' is replaced by two impedances  $Z_1$  and  $Z_2$  at the input and output terminals respectively so that  $Z_1$  and  $Z_2$  draw the same currents  $I_1$  and  $I_2$  respectively from the input and output terminals respectively, as were drawn by  $Z_S$  when it is shunting a part of the input signal to the output.



Amplifier having a Shunt Impedance  $Z_s$  is replaced with the same amplifier with two impedances  $Z_1$  and  $Z_2$  at the Input and output terminals respectively so that these two impedances draw the same currents  $I_1$  and  $I_2$  respectively, from the input and output terminals as was drawn by the shunt impedance  $Z_s$

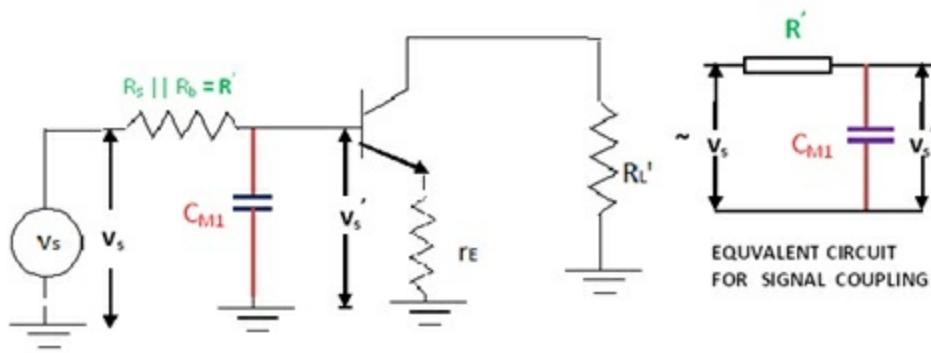
**Fig. 8.: - Representation of Miller's Theorem.**

- The impedances  $Z_1$  and  $Z_2$  are given by the following expressions --

$$Z_1 = \frac{Z_s}{(1 - A_v)} \quad :: \quad z_2 = \frac{A_v \cdot Z_s}{(A_v - 1)} \quad ... (9)$$

- If we apply Miller's theorem to the High Frequency Ac Equivalent Circuit of the Amplifier we get the following situation as shown in the figure below, where  $C_{M1}$  is the Miller Equivalent Impedance  $Z_1$ .

The signal ' $v_s$ ' from the source is attenuated by the  $R' - C_{M1}$  combination so that the actual input signal to the transistor is ' $v_s'$ . the simplification is shown as an equivalence alongside the figure-



- In the equivalent circuit, the signal voltage  $v_s'$  transmitted by the  $R' - C_{M1}$  combination is given by,

$$v_s' = \frac{-j X_{CM1} \cdot v_s}{R' - j X_{CM1}}$$

Dividing both numerator and denominator by ' $j X_{CM1}$ ' we get,

$$v_s' = \frac{-v_s}{(R'/jX_{CM1} - 1)} = \frac{v_s}{1 - R'/jX_{CM1}} = \frac{v_s}{1 + j R'/X_{CM1}}$$

Substituting for  $X_{CM1} = 1 / 2 \pi f C_{M1}$

$$v_s' = \frac{v_s}{1 + j 2 \pi f C_{M1} R'}$$

From this, we have the "Voltage Transmission Ratio"

$$\frac{v_s'}{v_s} = \frac{1}{1 + j 2 \pi f C_{M1} R'}$$

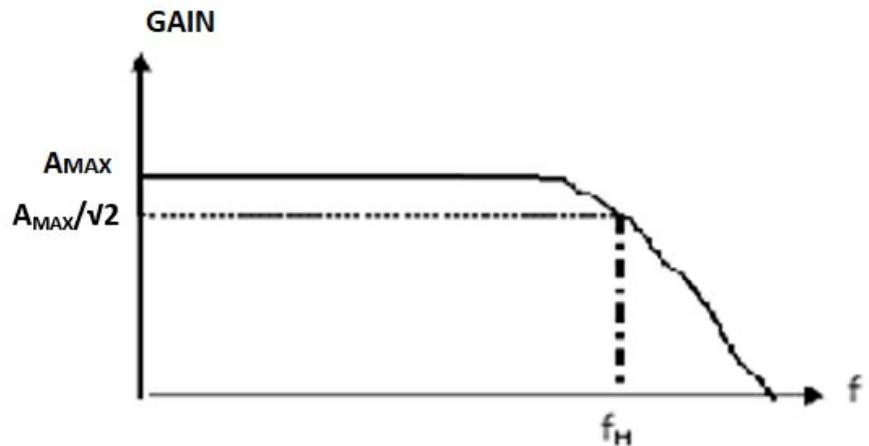
In this, the quantity  $2 \pi C_{M1} R'$  has the dimension of time. Therefore its reciprocal will have the dimension of frequency  $f_H$ . Expressing voltage transmission ratio as  $A'$  and its magnitude  $|A'|$  as follows

$$A' = \frac{v_s'}{v_s} = \frac{1}{1 + j (f/f_H)} \quad \dots(10)$$

$$|A'| = \sqrt{\left\{ 1 + \left( f/f_H \right)^2 \right\}} \quad \dots(11)$$

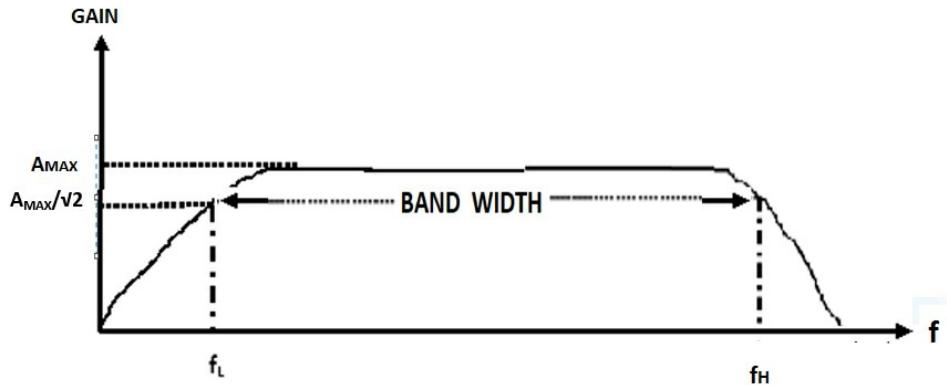
Evaluating this at various frequencies: –

- ❖ At  $f \ll f_H$  the term  $f/f_H$  tends to zero. Therefore  $|A'| \approx 1$ . In other words, the entire signal power is transferred from the source to the amplifier. Hence gain will be the maximum value as determined by the h-parameter model. In other words, we have a gain equal to  $A_{max}$ . This term  $A_{max}$  is constant since it is determined by the h-parameter values, as described above .
- ❖ At  $f = f_H$  we get  $|A'| = A_{MAX} / \sqrt{2}$ . Hence only  $1/\sqrt{2}$  times the signal power will get transferred to the amplifier to the load.
- ❖ At some high frequency  $f >> f_H$  the term  $f/f_H$  will tend to infinity. Hence the Voltage Transmission Ratio will tend to zero. This means that no signal will get transmitted to the amplifier and the gain will drop to zero. This is shown in the figure below.



#### FREQUENCY RESPONSE AT HIGH FREQUENCY RANGE

Combining the High frequency and the Low frequency response we get the complete “Frequency Response of the RC Coupled Amplifier” as—



**Fig. 9. :- Frequency Response of RC Coupled Amplifier.**

### POINTS OF HALF POWER FREQUENCY or 3dB DOWN POINTS

- At the frequencies  $f_L$  and  $f_H$  the Voltage Gain  $A_V$  as well as Current Gain  $A_I$  is reduced to an amount which is  $1/\sqrt{2}$  times the maximum gain .
- If we calculate the Power Gain at these frequencies, where Power Gain is  $G = (A_V \cdot A_I)$ , we get that **G is reduced to  $\frac{1}{2} G_{max}$** . Thus, these two points ' $f_L$ ' and ' $f_H$ ' on the x-axis of the Frequency Response curve are known as "**Half Power Points**".
- Power Gain is expressed in dB scale as  $G_{dB} = 10 \log G$ . The value of  **$10 \log (1/2) = -3dB$** . The value of Power Gain in dB scale is reduced by an amount of 3dB at the frequencies ' $f_L$ ' and ' $f_H$ '. Hence these two points ' $f_L$ ' and ' $f_H$ ' are also known as "**3dB Down Points**".

### GAIN – BANDWITDH PRODUCT

- It is possible to either increase or decrease the Gain of an amplifier. Recall that the formula for  $A_V$  for such an amplifier is as follows,

$$A_V = \frac{R'_L}{(r'_e + r_E)}$$

Hence, if we decrease the “Emitter Swamping Resistance”  $r_E$  the Voltage Gain will be increased, and vice-versa.

- Choosing an appropriate value of Emitter Swamping Resistance the Voltage gain can be adjusted at a desired value.
- The Band Width of an amplifier is increased when Negative Feedback is applied. It can be decreased with Positive Feedback. In other words, both Gain and Band Width are adjustable.
- **However, the product (Gain x Band Width) always remains constant.** An increase in Gain is always automatically associated with the decrease of Band Width by such an amount so that “Gain-Bandwidth Product” remains constant. The reverse is also true, that, for a decrease of gain, bandwidth increases.
- Essentially Gain-Bandwidth Product is a measure of the electrical energy being processed by the amplifier. **Since energy can neither be created nor destroyed, the Gain-Bandwidth Product must remain constant.**

### 7.3 CALCULATION OF CAPACITOR VALUES

- There are three capacitors in each stage of a RC Coupled amplifier. Two Coupling Capacitors  $C_C$  at the input and output terminals, and a By Pass Capacitor  $C_B$ , across the biasing resistance ‘ $R_e$ ’.
- This resistance  $R_e$ , is usually a large resistance, and it is in series with the smallest resistance of the circuit, namely,  $r'_e$ . Therefore, the capacitive reactance of the By Pass Capacitor must be very small so as to completely by pass the AC signal from the resistance  $R_e$ .
- Since capacitive reactance is inversely proportional to Capacitance,  $C$ , this capacitor  $C_B$  must be the largest of the three capacitors in the circuit. The value of this must be calculated for the lowest frequency of the AC signal, which is the lower Cut-Off

frequency  $f_L$ . If we consider this, the voltage gain of the amplifier, calculated from the simplified h-parameter analysis method will be modified as follows.

$$A_V = \frac{-h_{fe}R'_L}{h_{ie} + (1 + h_{fe})R_e || X_{CB}}$$

- Since  $R_e \gg X_{CB}$  the parallel combination of  $R_e$  and  $X_{CB}$  approximately equals  $X_{CB}$ . Rewriting this as

$$A_V = \frac{-h_{fe}R'_L}{\sqrt{[h_{ie}^2 + (1 + h_{fe})X_{CB}]^2}}$$

If we put

$$h_{ie} = (1 + h_{fe})X_{CB}$$

we have

$$A_V = \frac{-h_{fe}R'_L}{h_{ie}\sqrt{1+1}}$$

Where, the term  $\frac{-h_{fe}R'_L}{h_{ie}}$  is the Mid – frequency Gain of the amplifier .

$$\therefore A_V = \frac{\text{(Mid-Frequency Gain)}}{\sqrt{2}}$$

$$\therefore X_{CB} = \frac{h_{ie}}{1+h_{fe}} : \text{at the frequency } f_L$$

From the h-parameter Conversion Table we have

$$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$$

Also

$$h_{ib} = r'_e$$

This quantity  $r'_e$  is nothing but the internal resistance of the forward biased Emitter–Base junction.

$$\therefore X_{CB} = r'_e \text{ at the frequency } f_L$$

$$\therefore C_B = \frac{1}{2\pi f_L r'_e} \quad \underline{\dots(12(a))}$$

- The Coupling Capacitors at the Input and the Output terminals must not attenuate the Input Signal and the Output Signal respectively.

$$\therefore X_{CC} \ll Z_{IB} + R_S \text{ at the frequency } f_L \text{ (At Input)}$$

And

$$X_{CC} \ll Z_o + R_L \text{ at the frequency } f_L \text{ (At Output)}$$

$$\therefore C_C = \frac{1}{2\pi f_L (Z_{IB} + R_S) / 10} \quad \underline{\dots(12(b))} \text{ (At the Input)}$$

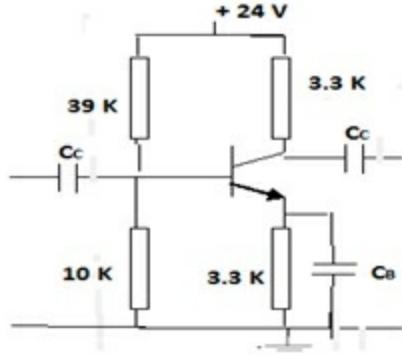
And

$$C_C = \frac{1}{2\pi f_L (Z_o + R_L) / 10} \quad \underline{\dots(12(c))} \text{ (At the Output)}$$

## TUTORIAL-2

**Example 2 :- (Design Problem)** The transistor in the circuit has  $h_{fe} = 50$  and  $h_{ie} = 1 K$ . The amplifier is to be operated within a band width from 100 Hz to 20 kHz. Calculate

1.  $C_C$  &  $C_B$
2.  $A_V$  when  $C_B$  is correctly calculated.
3.  $A_V$  when  $C_B$  is wrongly calculated using  $X_{CB} = R_E/10$



### SOLUTION ::

$$(i) \quad h_{ib} = \frac{h_{ie}}{1+h_{fe}} = \frac{1000}{1+50} = 19.6 \Omega$$

$$r_e' = h_{ib} = 19.6 \Omega$$

$$\therefore C_B = \frac{1}{2\pi \times 100 \times 19.6} = 81 \times 10^{-6} F$$

To use Standard Value capacitor  $\approx 80 \mu F$

In this circuit, the AC Emitter resistance is  $r_e'$

$$\therefore Z_{IB} = h_{ie} + (1 + h_{fe})r_e' = 1000 + (1 + 50) \times 19.6$$

$$Z_{IB} = 1999.6 \Omega$$

Assuming  $R_s = 0$  and  $Z_o = R_L$ , using Eq. 12(b) and 12(c), we have

$$C_{C(\text{input})} = \frac{1}{2\pi \times 100 \times (\frac{1999.6}{10})} = 7.9 \times 10^{-6} F$$

$$C_{C(\text{input})} \approx 8 \mu F$$

$$C_{C(\text{output})} = \frac{1}{2\pi \times 100 \times (\frac{3300}{10})} = 4.823 \times 10^{-7} F$$

Rectangular Snip

$$C_{C(\text{output})} \approx 0.5 \mu F$$

(ii) At the Lower Cut-Off frequency  $f_L$  the capacitive reactance  $X_{CB}$  equals  $r_e'$ .

Substituting in the formula for  $A_V$  given by the following, taking  $R_L' = R_C$

$$A_V = \frac{-h_{fe}R'_L}{\sqrt{[h_{ie}^2 + (1+h_{fe})X_{CB}]^2}}$$

$$A_V = \frac{-50 \times 3300}{\sqrt{1000^2 + [(1+50) \times 19.6]^2}}$$

$$A_V = -116.7$$

(iii) When  $X_{CB}$  is wrongly calculated as  $R_E/10$  we have the wrong value of voltage gain as

$$A_{V(\text{wrong})} = \frac{-h_{fe}R'_L}{\sqrt{[h_{ie}^2 + (1+h_{fe})X_{CB}]^2}}$$

$$A_{V(\text{wrong})} = \frac{-50 \times 3300}{\sqrt{1000^2 + [(1+50) \times 3300/10]^2}}$$

$$A_{V(\text{wrong})} = 9.8$$

## Section-2

### CASCADED R-C COUPLED AMPLIFIER (PRE-AMPLIFIER)

#### 7.4 Analysis of Cascaded Amplifier

The reader will recall that a single stage of amplifier can provide limited amplification. Most of the signal sources in practice can produce only very low power signals. These have to be highly amplified for use in general purpose applications. Thus, amplifiers are connected in Cascade. From the foregoing discussion of the R-C Coupled amplifier, it was observed that these amplifiers can provide uniform gain over a large range of frequencies. This property makes this class of amplifiers particularly suitable to amplify signals from a variety of sources. R-C Coupled Cascaded amplifiers are commonly used for this purpose. Since this constitutes the initial stage of amplification, this is commonly called **Pre-Amplifier** Stage. Since these work over a large Band Width, these are also called **Broad Band Amplifiers**.

#### Solution of Cascaded Amplifier Problems

For the solution of any BJT amplifier circuit, either r-parameter analysis or h-parameter analysis can be used. It is more convenient to use the Simplified h-parameter model. The following points are to be noted while solving Cascaded Amplifier problems

### **For solution with r-parameter analysis**

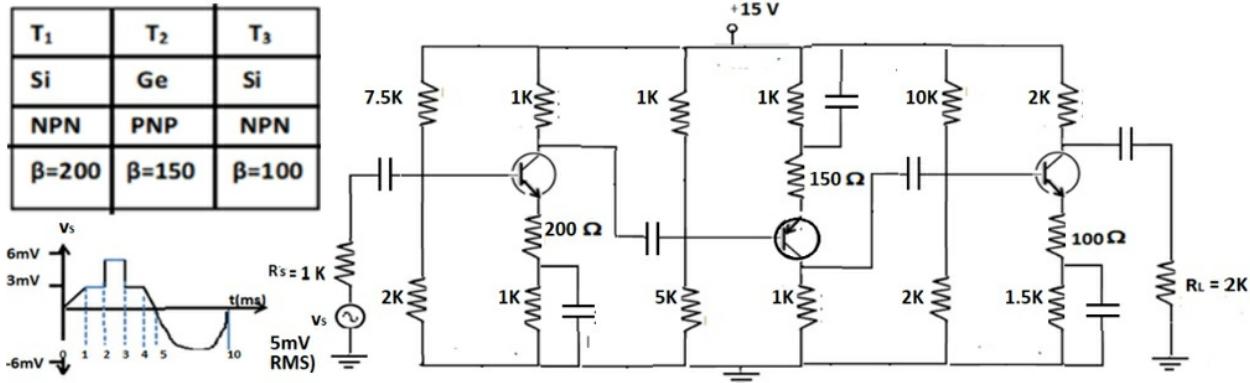
1. First the DC Equivalent Circuit is solved to obtain  $R_b$  and  $r_e'$  of each stage. Since the DC Equivalent circuit is obtained by open Circuiting the capacitors, each stage become independent of each other and they can be solved individually
2. These two quantities are substituted in the r-parameter model of each corresponding stage in the AC Equivalent circuit.
3. The solution of the AC equivalent circuit has to be performed from the LAST stage and proceed backwards to the FIRST stage. This is because, the load resistance  $R_L''$  of an inner stage is the parallel combination of the  $R_C$  of that stage and the  $Z_{i(T)}$  of the previous stage.

### **For solution with h-parameter analysis**

Since h-parameter analysis is performed by substituting the h-parameter model on the AC equivalent circuit, only the 3<sup>rd</sup> point in the previous list is relevant.

The foregoing is emphasized with the help of the following numerical examples.

**Example (r-parameter analysis):-** Calculate the output power delivered to the load and sketch the output signal waveform. The relevant parameters for the transistors are tabulated.

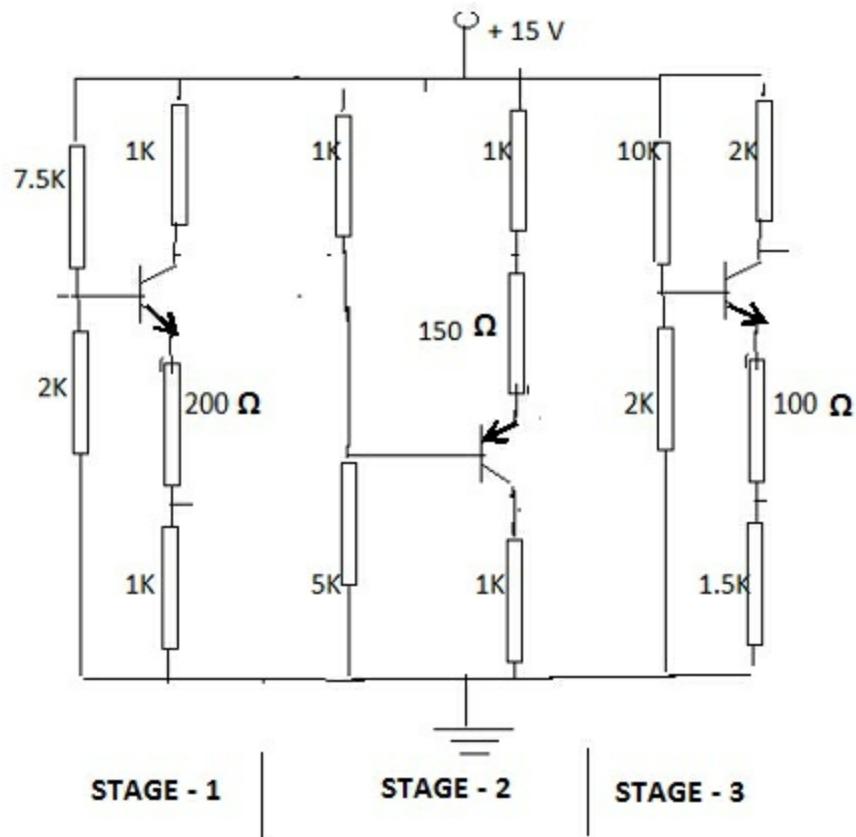


**Fig. 10.: - Cascaded Amplifiers with a mix of PNP and NPN transistors.  
(PNP in "Upside-Down" configuration).**

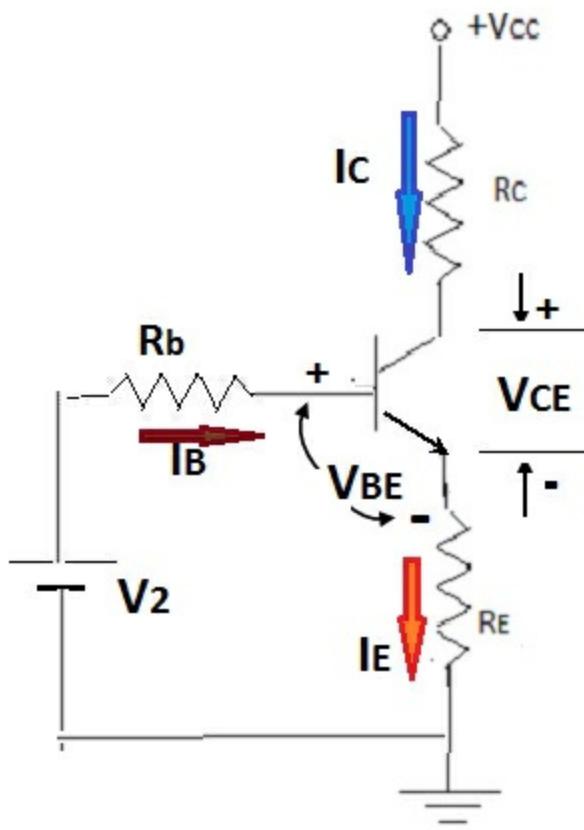
**NOTE :-** This amplifier circuit shows the Upside-Down convention. The second transistor is PNP while the first and the third are NPN. Since Collector of the NPN transistor and the Emitter of the PNP transistor must be positive, while Emitter of NPN and Collector of PNP need to be negative, these two types of transistors must be connected Upside-Down with respect to each other.

## SOLUTION DC Analysis

- For DC Analysis all capacitors are to be open circuited.
- The AC signal source is to be short circuited.
- Thus, we get the DC Equivalent Circuit of the amplifier as follows. In this, each stage is disconnected from its predecessors and its followers. In other words, each stage is independent. Hence, we can solve the DC Equivalent circuit of them **individually**.



**First Stage:** In this  $R_1 = 7.5\text{ K}$ ,  $R_2 = 2\text{ K}$ ,  $R_C = 1\text{ K}$  and  $R_E$  consists of the series combination of  $200\ \Omega$  and  $1\text{ K}$ ; thus  $R_E = 1.2\text{ K}$ . Thevenizing the Base Emitter circuit of this we get the following-



$$V_2 = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{2 \times 15}{7.5+2} = 3.16 \text{ V} \quad \& \quad R_{b1} = \frac{R_2 R_2}{R_1 + R_2} = \frac{7.5 \times 2}{7.5+2} = 1.58 \text{ K}$$

From the KVL equation of the base-emitter loop we get the equation for  $I_B$  as

$$I_B = \frac{(V_2 - V_{BE})}{(R_b + (1+\beta)R_E)}$$

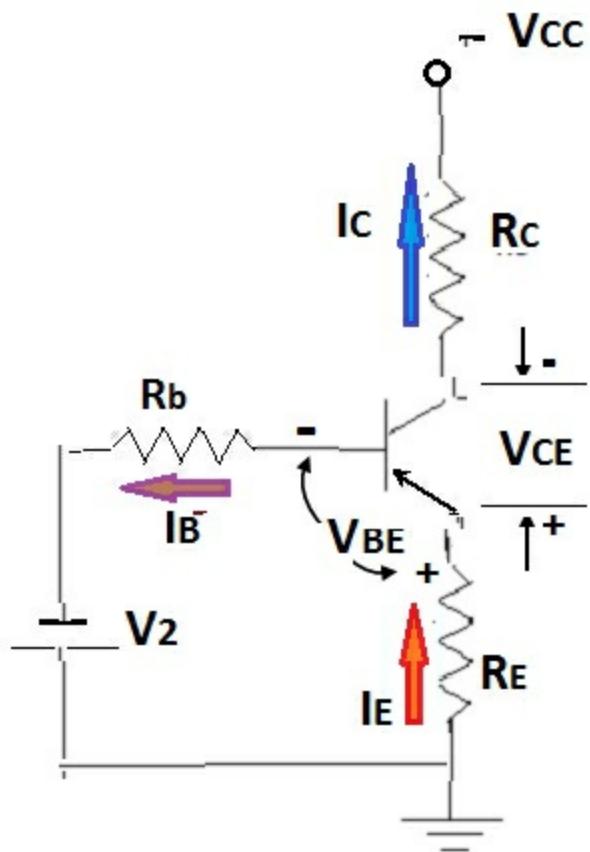
This is a Si transistor, hence  $V_{BE} = 0.7 \text{ V}$  and  $\beta = 200$

$$I_B = \frac{(3.16 - 0.7)}{(1.58 + (1+200) \times 1.2)} = 0.01013 \text{ mA}$$

$$I_C \approx I_E = \beta I_B = 200 \times 0.01013 = 2.026 \text{ mA}$$

$$\therefore r_{e1}' = \frac{25}{I_E \text{ mA}} = \frac{25}{2.026} = 12.34 \Omega$$

**Second Stage :** Note that, the transistor in the second stage is PNP, hence it is connected Up-Side-Down. Therefore,  $R_1$  is 5 K and  $R_2$  is 1 K,  $R_C$  is also 1 K.  $R_E$  consists of the series the 150  $\Omega$  and 1.5 K, thus  $R_E = 1.65$  K. Thevenizing the Base Emitter circuit of this we get the following-



$$V_2 = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{1 \times 15}{5+1} = \underline{\underline{3 \text{ V}}} \quad \& \quad R_{b2} = \frac{R_2 R_2}{R_1 + R_2} = \frac{5 \times 1}{5+1} = \underline{\underline{0.833 \text{ K}}} = \underline{\underline{833 \Omega}}$$

From the KVL equation of the base-emitter loop we get the equation for  $I_B$  as

$$I_B = \frac{(V_2 - V_{BE})}{(R_b + (1 + \beta)R_E)}$$

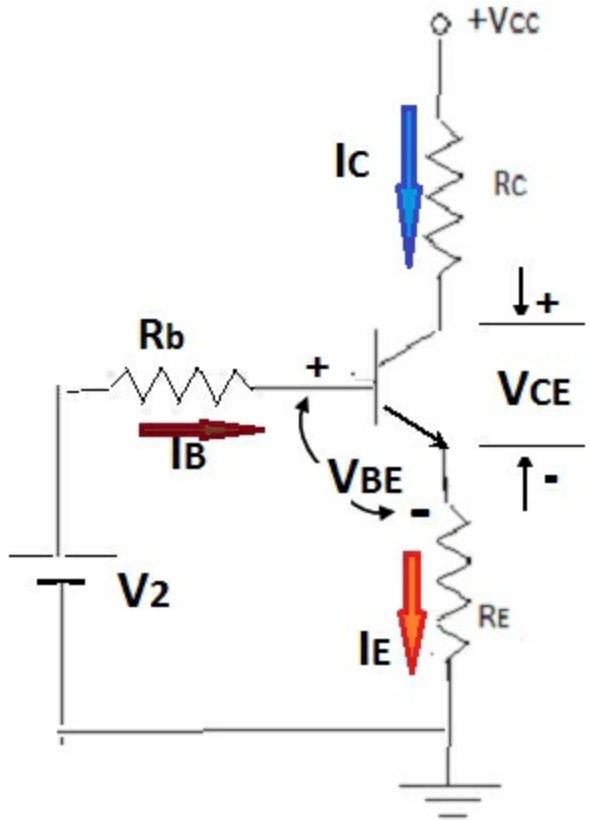
This is a Ge transistor, hence  $V_{BE} = 0.3 \text{ V}$  and  $\beta = 150$

$$I_B = \frac{(3 - 0.3)}{(0.833 + (1 + 150) \times 1.65)} = \underline{\underline{0.01547 \text{ mA}}}$$

$$I_C \approx I_E = \underline{\underline{\beta I_B}} = 150 \times 0.01547 = 2.32 \text{ mA}$$

$$\therefore r_{e2}' = \frac{25}{I_E \text{ mA}} = \frac{25}{2.32} = \underline{\underline{10.78 \Omega}}$$

**Third Stage:** In this  $R_1 = 10 \text{ K}$ ,  $R_2 = 2 \text{ K}$ ,  $R_C = 2 \text{ K}$  and  $R_E$  consists of the series combination of  $100 \Omega$  and  $1.5 \text{ K}$ ; thus  $R_E = 1.6 \text{ K}$ . Thevenizing the Base Emitter circuit of this we get the following-



$$V_2 = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{2 \times 15}{10+2} = 2.5 \text{ V} \quad \& \quad R_{b3} = \frac{R_2 R_2}{R_1 + R_2} = \frac{10 \times 2}{10+2} = 1.67 \text{ K}$$

From the KVL equation of the base-emitter loop we get the equation for  $I_B$  as

$$I_B = \frac{(V_2 - V_{BE})}{(R_b + (1 + \beta)R_E)}$$

This is a Ge transistor, hence  $V_{BE} = 0.3 \text{ V}$  and  $\beta = 100$

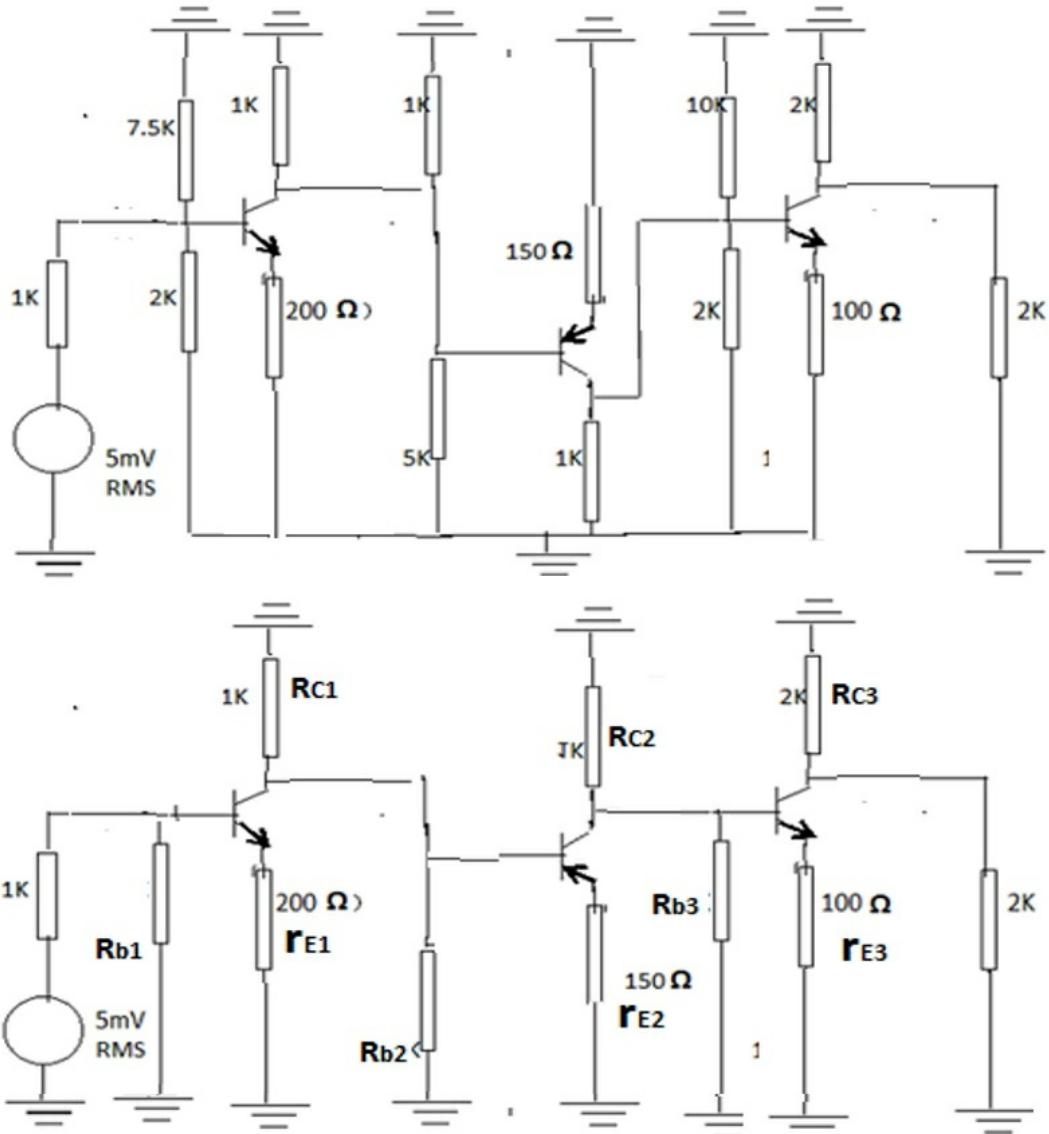
$$I_B = \frac{(2.5 - 0.3)}{(1.67 + (1 + 100) \times 1.65)} = 0.01307 \text{ mA}$$

$$I_C \approx I_E = \underline{\beta} I_B = 100 \times 0.01307 = 1.3 \text{ mA}$$

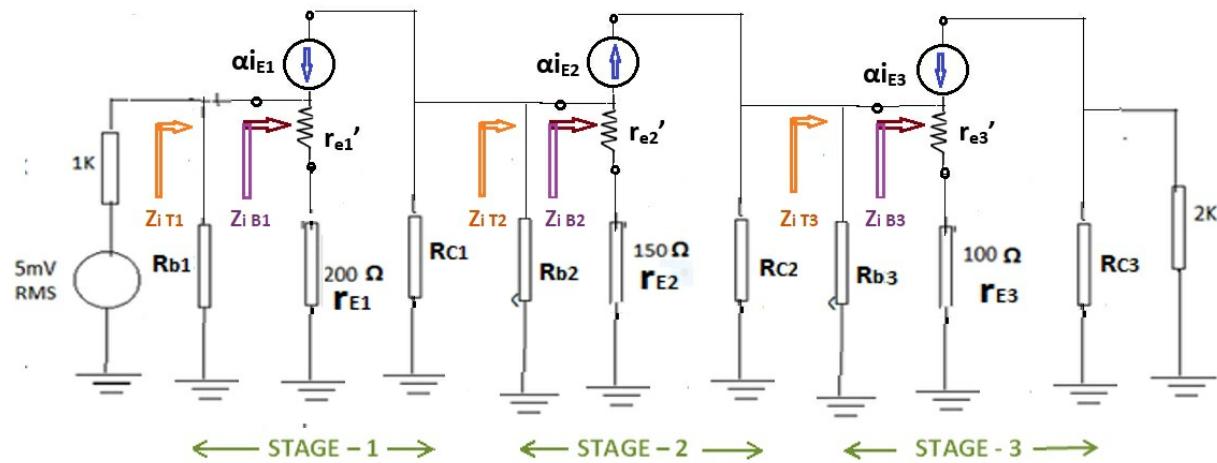
$$\therefore r_{e3}' = \frac{25}{I_E \text{ mA}} = \frac{25}{1.3} = 19.23 \Omega$$

## AC Analysis

- For AC Analysis all capacitors are to be short circuited. When the capacitor across a resistance is short circuited, the net impedance becomes zero.
- The DC signal  $V_{CC}$  is to be short circuited, so that all connections to  $V_{CC}$  now go to ground.
- Using these we get the AC Equivalent Circuit as follows. In this, the transistor  $T_2$  need no longer be shown in up-Side-Down connection since no DC Bias is involved.



- In the next step we show the connections of the  $R_C$  resistors of each inner stage as being parallel to the  $R_b$  resistors of the next stage and in the last stage,  $R_C$ , as being parallel to the external load  $R_L$ . Thereafter, we replace the transistors with the r-parameter model.



- In this the numerical value of  $r_{e1}'$ ,  $r_{e2}'$  and  $r_{e3}'$ , as well as those of  $R_{b1}$ ,  $R_{b2}$  and  $R_{b3}$  had been calculated in the DC Analysis step done earlier.

### **RULES FOR SOLVING AC EQUIVALENT CIRCUIT OF MULTISTAGE AMPLIFIER**

- For AC Analysis we can use the formulae we derived in Chapter-6 directly.
- In the formula for  $A_V$  and  $A_I$  we have to use  $R_L'$  and  $Z_{I(T)}$  respectively. The apparent load resistance  $R_L'$  is the parallel combination of  $R_C$  and the external load resistance  $R_L$ .
- For the inner stages, the external load resistance is  $Z_{I(T)}$  of the successor stage.** Hence for the inner stages  $R_L'$  is not known independently.
- However, for the last stage,  $R_L'$  is evident. **Hence the rule for solving AC Equivalent circuit of Multistage Amplifier is to start at the last stage and proceed backwards.**

#### **1. Last Stage (Third Stage)**

$$1. \quad A_{v3} = \frac{-R'_{L3}}{(r'_{e3} + r_{E3})}$$

Where,

$$R'_{L3} = R_{C3} \parallel R_L = 2 \text{ K} \parallel 2 \text{ K} = \frac{2 \times 2}{(2+2)} = 1 \text{ K}$$

Using the value of  $r'_{e3} = 19.23 \Omega$  calculated in the DC Analysis and taking the value of  $r_{E3} = 100 \Omega$  from the circuit diagram we have

$$A_{v3} = \frac{-1000}{(19.23+100)} = -8.4$$

$$2. \quad Z_{I(B)3} = \beta_3 (r'_{e3} + r_{E3}) = 100 \times (19.23 + 100)$$

$$Z_{I(B)3} = 11923 \Omega = 11.92 \text{ K}$$

$$3. \quad Z_{I(T)3} = R_{b3} \parallel Z_{I(B)3} \\ = 1.67 \parallel 11.92 = \frac{1.67 \times 11.92}{(1.67+11.92)}$$

$$Z_{I(T)3} = 1.465 \text{ K} = 1465 \Omega$$

$$4. \quad A_{I3} = \frac{-Z_{I(T)3}}{(r'_{e3} + r_{E3})} = \frac{-1465}{(19.23+100)} \\ A_{I3} = -12.3$$

## 2. Second Stage

The apparent load resistance  $R'_{L2}$  for the Second Stage is the parallel combination of the Collector Resistance of this stage  $R_{c2}$  and the Input impedance of the previous stage  $Z_{I(T)3}$ .

Thus

$$R_{L2}' = R_{C2} \parallel Z_{I(T)3} = \frac{R_{C2} Z_{I(T)3}}{(R_{C2} + Z_{I(T)3})}$$

$$R_{L2}' = \frac{1 \times 1.465}{(1+1.465)} = 0.594 \text{ K} = 594 \Omega$$

1.  $A_{V2} = \frac{-R'_{L2}}{(r'_{e2} + r_{E2})}$

Using the value of  $r'_{e2} = 10.78 \Omega$  calculated in the DC Analysis and taking the value of  $r_{E2} = 150 \Omega$  from the circuit diagram we have

$$A_{V2} = \frac{-594}{(10.78+150)} = -3.7$$

2.  $Z_{I(B)2} = \beta_2 (r'_{e2} + r_{E2}) = 150 \times (10.78 + 150)$

$$Z_{I(B)2} = 24117 \Omega = 24.12 \text{ K}$$

3.  $Z_{I(T)2} = R_{b2} \parallel Z_{I(B)2} = 833 \parallel 24.12 = \frac{0.833 \times 24.12}{(0.833+24.12)}$

$$Z_{I(T)2} = 0.805 \text{ K} = 805 \Omega$$

4.  $A_{I2} = \frac{-Z_{I(T)2}}{(r'_{e2} + r_{E2})} = \frac{-805}{(10.78+150)}$

$$A_{I2} = -5$$

### (iii) First Stage

The apparent load resistance  $R_{L1}'$  for the First Stage is the parallel combination of the Collector Resistance of this stage  $R_{c1}$  and the Input impedance of the next stage  $Z_{I(T)2}$ .

Thus

$$R_{L1}' = R_{C1} \parallel Z_{I(T)2} = \frac{R_{C1} Z_{I(T)2}}{(R_{C1} + Z_{I(T)2})}$$

$$R_{L1}' = \frac{1 \times 0.805}{(1+0.805)} = 0.446 \text{ K} = 446 \Omega$$

$$1. \quad A_{V1} = \frac{-R'_{L1}}{(r'_{e1} + r_{E1})}$$

Using the value of  $r'_{e1} = 12.34 \Omega$  calculated in the DC Analysis and taking the value of  $r_{E1} = 200 \Omega$  from the circuit diagram we have

$$A_{V1} = \frac{-446}{(12.34+200)} = -2.1$$

$$2. \quad Z_{I(B)1} = \beta_1 (r'_{e1} + r_{E1}) = 200 \times (12.34 + 200)$$

$$Z_{I(B)2} = 42465 \Omega = 42.47 \text{ K}$$

$$3. \quad Z_{I(T)1} = R_{b1} \parallel Z_{I(B)1} = 1.58 \parallel 42.47 = \frac{1.58 \times 42.47}{(1.58+42.47)}$$

$$Z_{I(T)1} = 1.52 \text{ K} = 1520 \Omega$$

$$4. \quad A_{I1} = \frac{-Z_{I(T)1}}{(r'_{e1} + r_{E1})} = \frac{-1520}{(12.34+200)}$$

$$A_{I1} = -7.2$$

### ACTUAL VOLTAGE GAIN AND CURRENT GAIN TAKING SOURCE RESISTANCE INTO CONSIDERATION:

$$A_{Vs} = \frac{Z_{I(T)}}{(R_S + Z_{I(T)})} \times A_V$$

&

$$A_{Is} = \frac{R_S}{(R_S + Z_{I(T)})} \times A_I$$

$Z_{I(T)}$  is the “Net Input Impedance”. In case of the Multistage Amplifier, Input Impedance of the First Stage is the Net Input Impedance of the amplifier .

∴

$$Z_{I(T)} = Z_{I(T)1}$$

$A_V$  is the “Net Voltage Gain” and  $A_I$  is the “Net Current Gain” of the amplifier,

With

$$A_V = A_{V1} \cdot A_{V2} \cdot A_{V3} \quad \& \quad A_I = A_{I1} \cdot A_{I2} \cdot A_{I3}$$

$$\therefore A_{VS} = \frac{Z_{I(T)1}}{(R_S + Z_{I(T)})} \times A_{V1} \cdot A_{V2} \cdot A_{V3}$$

&

$$A_{IS} = \frac{R_S}{(R_S + Z_{I(T)1})} \times A_{I1} \cdot A_{I2} \cdot A_{I3}$$

Substituting we have—

$$A_{VS} = \frac{1.52}{(1+1.52)} \times (-2.1) \cdot (-3.7) \cdot (-8.4) = -39.37$$

$$A_{IS} = \frac{1}{(1+1.52)} \times (-7.2) \cdot (-5) \cdot (-12.3) = -175.7$$

Output Voltage is  $A_{VS}$  times greater than Input Voltage  $V_S$  produced by the source.

Given that  $V_S = 5 \text{ mV (rms)}$

$$\therefore V_O = A_{VS} \cdot V_S = -39.37 \times 5 = 196.85 \text{ mV (rms)}$$

Output Power is developed across the external load resistance  $R_L$

$$\therefore P_O = \frac{V_{O(rms)}^2}{R_L} \quad \text{Where } V_{O(rms)} = 196.85 \text{ mV} = 0.197 \text{ V}$$

and

$$R_L = 2 \text{ K} = 2000 \Omega$$

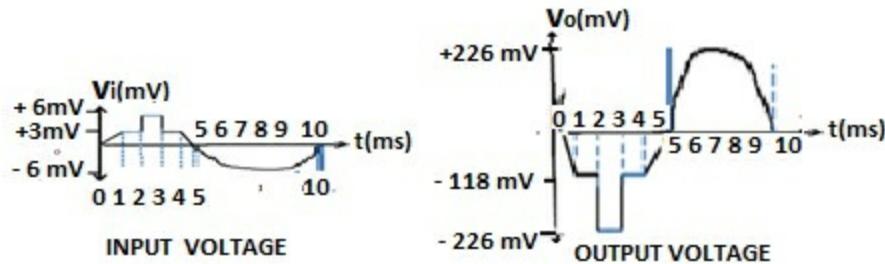
OR

$$P_O = \frac{0.197^2}{2000} = 1.9 \times 10^{-5} \text{ W}$$

### Output Voltage Waveform

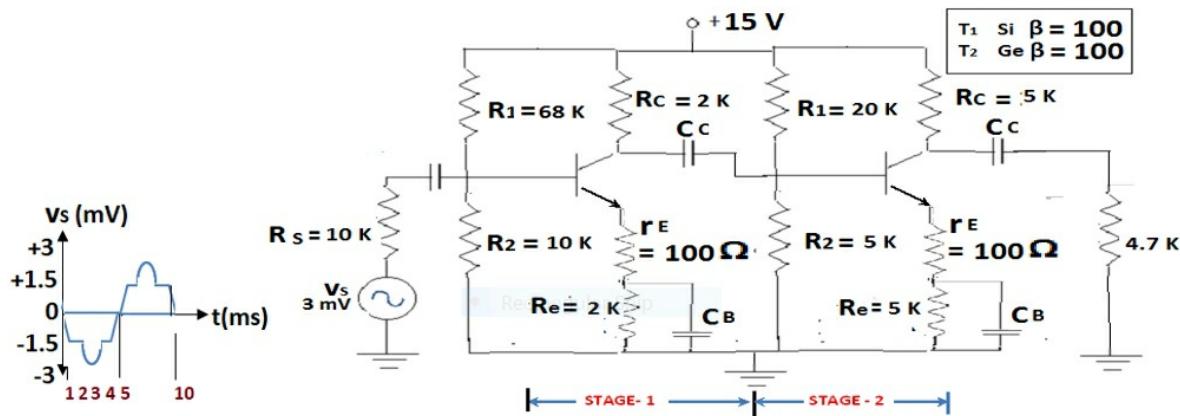
- The instantaneous Output Voltage is the product of  $A_{VS}$  with the instantaneous Input Voltage at every instant of time. However, since  $A_{VS}$  is negative, the Output Voltage is inverted w.r.t. the Input Voltage Waveform. Thus we get .
- When instantaneous Input Voltage is 3 mV the instantaneous Output Voltage is  $(-39.37).3 \text{ mV} = -118.11 \text{ mV}$ .
- When instantaneous Input Voltage is 6 mV the instantaneous Output Voltage is  $(-39.37).6 \text{ mV} = -236.22 \text{ mV}$ .
- When instantaneous Input Voltage is -6 mV the instantaneous Output Voltage is  $(-39.37).(-6) \text{ mV} = +236.22 \text{ mV}$ .

The Output Voltage Waveform is as shown in the figure below



## TUTORIAL-1

**EXAMPLE 4 : – Evaluate the Output Voltage, Output Power and Output Voltage Waveform.**



## SOLUTION

### DC Analysis :-

Short circuiting the AC signal source, using only the DC Bias  $V_{CC}$ , and Open Circuiting all capacitors we get the DC Equivalent circuits of the two stages independently as follows—

#### 1. DC Equivalent Circuit of First Stage

In this  $R_1 = 68\text{ K}$ ,  $R_2 = 10\text{ K}$ ,  $R_C = 2\text{ K}$  and  $R_E$  consists of the series

combination of  $100\ \Omega$  and  $2\ K$ ; thus  $R_E = 2.1\ K$ . Thevenizing the Base Emitter circuit of this we get the circuit alongside.

Here

$$V_2 = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{10 \times 15}{68+10} = 1.92\ V$$

$$R_{b1} = \frac{R_1 R_2}{R_1 + R_2} = \frac{68 \times 10}{68+10} = 8.7\ K = 8700\ \Omega$$

From the KVL equation of the base-emitter loop we get the equation for  $I_B$  as

$$I_B = \frac{(V_2 - V_{BE})}{(R_b + (1 + \beta)R_E)}$$

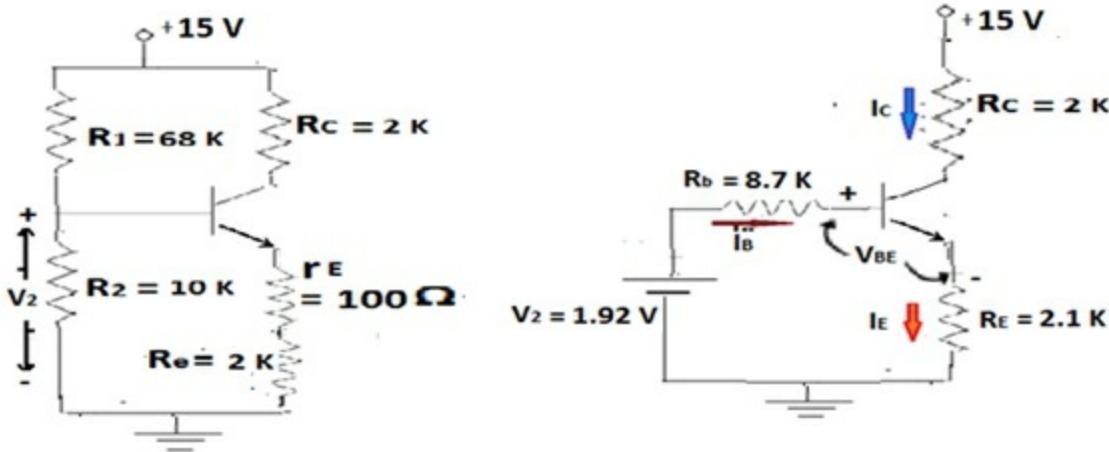
This is a Si transistor, hence  $V_{BE} = 0.7\ V$  and  $\beta = 100$

$$I_B = \frac{(1.92 - 0.7)}{(8.7 + (1 + 100) \times 2.1)} = 0.0055\ mA$$

$$I_C \approx I_E = \underline{\beta} I_B = 100 \times 0.0055 = 0.55\ mA$$

$$\therefore r_{e1}' = \frac{25}{I_E\ mA} = \frac{25}{0.55} = 45.45\ \Omega$$

Rectangular Snip



## 2. DC Equivalent Circuit of Second Stage

Here  $R_1$  is  $20\ K$  and  $R_2$  is  $5\ K$ ,  $R_C$  is also  $5\ K$ .  $R_E$  consists of the series the  $100\ \Omega$  and  $5\ K$ , thus  $R_E = 5.1\ K$ . Thevenizing the Base Emitter circuit of this we get the circuit alongside.

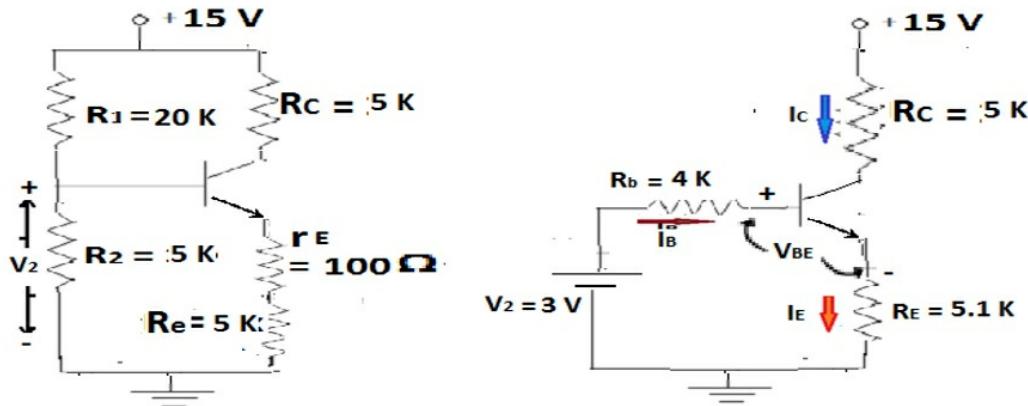
Here

$$V_2 = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{5 \times 15}{5+15} = \underline{\underline{3 \text{ V}}}$$

$$R_{b2} = \frac{R_2 R_1}{R_1 + R_2} = \frac{5 \times 20}{5+20} = \underline{\underline{4K = 4000 \Omega}}$$

From the KVL equation of the base-emitter loop we get the equation for  $I_B$  as

$$I_B = \frac{(V_2 - V_{BE})}{(R_b + (1 + \beta)R_E)}$$



This is a Ge transistor, hence  $V_{BE} = 0.3 \text{ V}$  and  $\beta = 100$

$$I_B = \frac{(3-0.3)}{(4+(1+100)\times 5.1)} = \underline{\underline{0.005 \text{ mA}}}$$

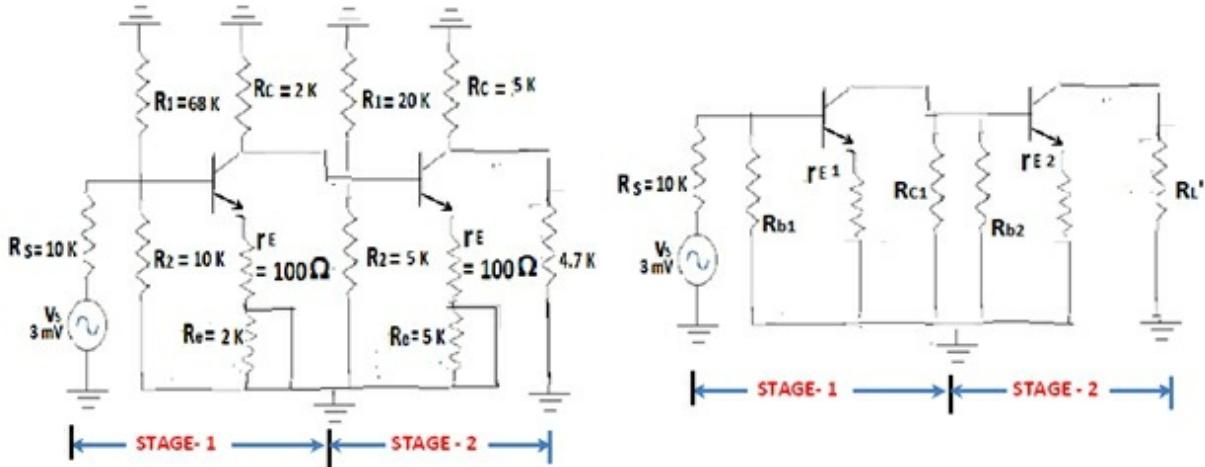
$$I_C \approx I_E = |\beta| I_B = 100 \times 0.005 = \underline{\underline{0.5 \text{ mA}}}$$

$$\therefore r_{e2}' = \frac{25}{I_E \text{ mA}} = \frac{25}{0.5} = \underline{\underline{50 \Omega}}$$

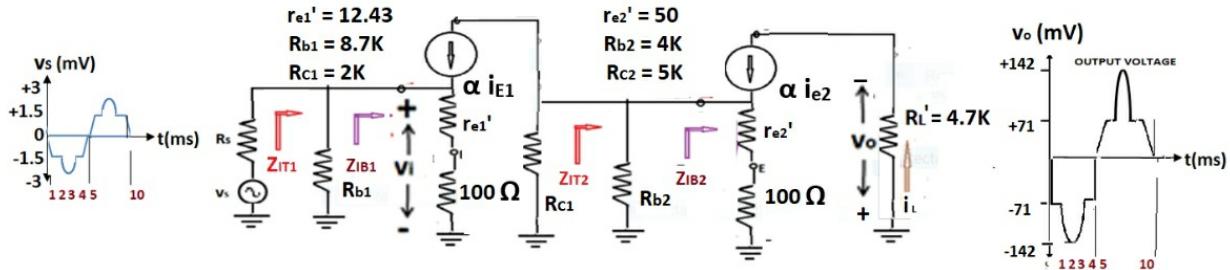
## AC Analysis

Grounding the DC Bias and using only the AC Signal Source and Short Circuiting all capacitors we get the AC Equivalent Circuit. When  $R_e$  is in parallel with a Short Circuit it will be removed in the AC Equivalent circuit. The parallel combinations of the resistances  $R_1$  &  $R_2$  is replaced by  $R_b$  at the Base and the parallel combination of  $R_C$  &  $R_L$  by  $R_L'$  at the Collector.

### (i) AC Equivalent Circuit



The transistors are replaced by the r-parameter model. And the AC Analysis is started from the Last Stage and proceed backwards.



(i) Last Stage (Second Stage)

$$1. \quad A_{V2} = \frac{-R'_{L2}}{(r'_{e2} + r_{E2})}$$

Where

$$R'_{L2} = R_{C2} \parallel R_L = 5 \text{ K} \parallel 4.7 \text{ K}$$

$$R'_{L2} = \frac{5 \times 4.7}{(5+4.7)} = 2.4 \text{ K}$$

Using the value of  $r'_{e2} = 50 \Omega$  calculated in the DC Analysis and taking the value of  $r_{E2} = 100 \Omega$  from the circuit diagram we have

$$A_{V2} = \frac{-2400}{(50+100)} = -16$$

$$2. \quad Z_{I(B)2} = \beta_2 (r'_{e2} + r_{E2}) = 100 \times (50 + 100) \\ Z_{I(B)2} = 15000 \Omega = 15 \text{ K}$$

$$3. \quad Z_{I(T)2} = R_{b2} \parallel Z_{I(B)2} = 4 \parallel 15 = \frac{4 \times 15}{(4+15)}$$

$$Z_{I(T)2} = 3.16 \text{ K} = 3160 \Omega$$

$$4. \quad A_{I2} = \frac{-Z_{I(T)2}}{(r'_{e2} + r_{E2})} = \frac{-3160}{(50+100)} \\ A_{I2} = -21$$

### (ii) First Stage

$$R'_{L1} = R_{C1} \parallel Z_{I(T)2} = \frac{R_{C1} Z_{I(T)2}}{(R_{C1} + Z_{I(T)2})}$$

$$R'_{L1} = \frac{2 \times 3.16}{(2+3.16)} = 1.22 \text{ K} = 1220 \Omega$$

Rectangular Snip

$$1. \quad A_{V1} = \frac{-R'_{L1}}{(r'_{e1} + r_{E1})}$$

Using the value of  $r_{e1}' = 12.34 \Omega$  calculated in the DC Analysis and taking the value of  $r_{E1} = 100 \Omega$  from the circuit diagram we have

$$A_{V1} = \frac{-1220}{(45.45+100)} = -8.4$$

$$2. \quad Z_{I(B)1} = \beta_1 (r_{e1}' + r_{E1}) = 100 \times (45.45 + 100)$$

$$Z_{I(B)2} = 14545 \Omega = 14.545 \text{ K}$$

$$3. \quad Z_{I(T)1} = R_{b1} || Z_{I(B)1} = 8.7 || 14.545 = \frac{8.7 \times 14.545}{(8.7+14.545)}$$

$$Z_{I(T)1} = 5.444 \text{ K} = 5444 \Omega$$

$$4. \quad A_{I1} = \frac{-Z_{I(T)1}}{(r'_{e1} + r_{E1})} = \frac{-5444}{(45.45+100)}$$

$$A_{I1} = -37.43$$

### NET VOLTAGE GAIN AND NET CURRENT GAIN:

$$A_{Vs} = \frac{Z_{I(T)}}{(R_S + Z_{I(T)})} \times A_{V1} \cdot A_{V2}$$

&

$$A_{Is} = \frac{R_S}{(R_S + Z_{I(T)})} \times A_{I1} \cdot A_{I2}$$

$Z_{I(T)}$  is the “Net Input Impedance”. In case of the Multistage Amplifier, Input Impedance of the First Stage is the Net Input Impedance of the amplifier.

$$\therefore Z_{I(T)} = Z_{I(T)1}$$

Substituting we have—

$$A_{Vs} = \frac{5.444}{(10+5.444)} \times (-8.4) \cdot (-16) = +47.38$$

$$A_{Is} = \frac{10}{(10+5.444)} \times (-37.43) \cdot (-21) = +509$$

Output Voltage is  $A_{Vs}$  times greater than Input Voltage  $V_S$  of the source.

Given that  $V_S = 3 \text{ mV (rms)}$

$$\therefore V_O = A_{VS} \cdot V_S = 47.38 \times 3 = 142.14 \text{ mV (rms)}$$

Output Power is developed across the external load resistance  $R_L$

$$\therefore P_O = \frac{V_O^2}{R_L} \quad \text{Where, } V_O(\text{rms})$$

$$= 142.14 \text{ mV} = 0.142 \text{ V}$$

and

$$R_L = 4.7 \text{ K} = 4700 \Omega$$

OR

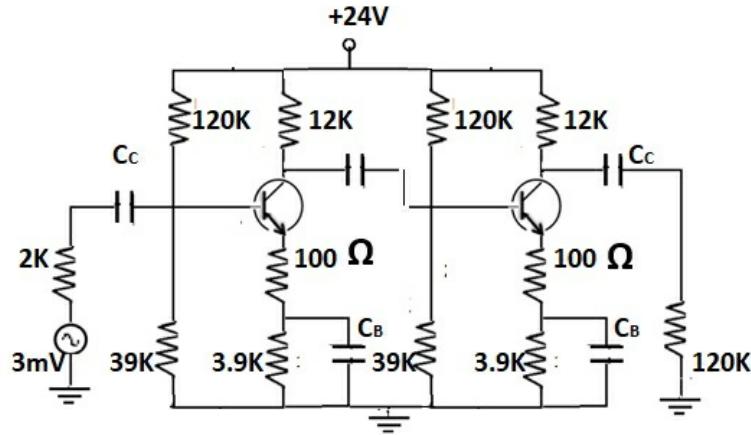
$$P_O = \frac{0.142^2}{4700} = 4.3 \times 10^{-6} \text{ W}$$

### Output Voltage Waveform

- When instantaneous Input Voltage is 1.5 mV the instantaneous Output Voltage is  $47.38 \times 1.5 = 71 \text{ mV}$
- When instantaneous Input Voltage is 3 mV the instantaneous Output Voltage is  $47.38 \times 3 = 142 \text{ mV}$
- When instantaneous Input Voltage is  $-1.5 \text{ mV}$  the instantaneous Output Voltage is  $-71 \text{ mV}$  and when instantaneous Input Voltage is  $-3 \text{ mV}$  the instantaneous Output Voltage is  $-142 \text{ mV}$

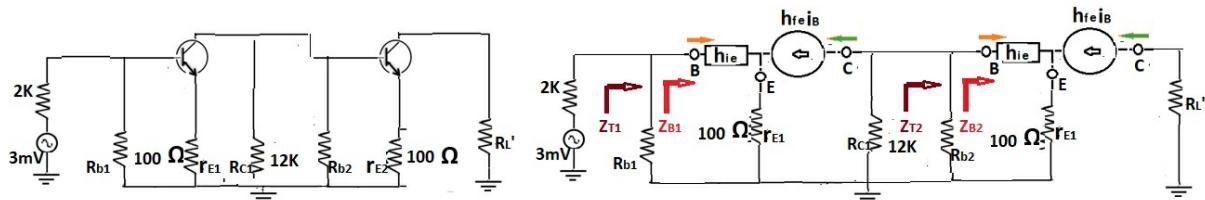
In this case the Net Voltage Gain is a positive quantity. Hence the output voltage waveform is **Not Inverted**. The Output Voltage Waveform is as shown in the figure above.

**Example 5 :-** Calculate the rms output voltage of the cascaded amplifier using Simplified h-parameter model. The two transistors are identical, with  $h_{fe} = 50$  and  $h_{ie} = 1 \text{ K}$ .



### SOLUTION ::

The AC Equivalent circuit, and the simplified h-parameter circuit of the amplifier is shown in the figure below. The transistors are replaced by the Simplified h-Parameter model in the AC Equivalent circuit.



### Analysis

Starting the analysis from the Last Stage, using the formulae we derived in Chapter-6, we have

### 2 nd Stage Calculations

$$A_{V2} = \frac{-h_{fe}R'_L}{[h_{ie} + (1 + h_{fe})r_{E2}]}$$

From the given circuit

$$R_L = 120 \parallel 12 = 10.9 \text{ K} \quad \& \quad r_{E2} = 100 \Omega$$

Substituting

$$A_{V2} = \frac{-50 \times 10900}{[1000 + (1+50) \times 100]} = -89.34$$

$$1. \quad Z_{IB2} = h_{ie2} + (1 + h_{fe2})r_{E2} = 1000 + (\underline{1} + 50) \cdot 100 \\ Z_{IB2} = 1000 + (\underline{1} + 50) \cdot 100 = 6100 \Omega = 6.1 \text{ K}$$

And

$$2. \quad Z_{IT2} = Z_{IB2} \parallel R_{b2} \quad \text{where } R_{b2} = 120 \text{ K} \parallel 39 \text{ K} = 29.4 \text{ K}$$

$$\therefore Z_{IT2} = \frac{6.1 \times 29.4}{6.1 + 29.4} = 5.05 \text{ K}$$

### 1 st Stage Calculations

1. Load for the First Stage is

$$R_{L1}' = R_{C1} \parallel Z_{IT2} = \frac{12 \times 5.05}{12+5.05} = 3.55 \text{ K}$$

Substituting the appropriate quantities in Eq.5.29 and Eq 5.27

$$A_{V1} = \frac{-50 \times 3550}{[1000 + (1+50) \times 100]} = -29.1$$

2.  $| Z_{IB1} = h_{ie1} + (1 + h_{fe1})r_{E1}$   
 $Z_{IB1} = 1000 + (1 + 50) \cdot 100 = 6100 \Omega = 6.1 \text{ K}$

And

3.  $Z_{IT1} = Z_{IB1} \parallel R_{b1} \text{ where } R_{b1} = 120 \text{ K} \parallel 39 \text{ K} = 29.4 \text{ K}$

$$\therefore Z_{IT2} = \frac{6.1 \times 29.4}{6.1+29.4} = 5.05 \text{ K}$$

• Rectangular Snip

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XXXXXXXX-CA-CA-CA-CA- XXXXXXXX

# CHAPTER – VIII

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## THE FIELD EFFECT TRANSISTORS

### *FIELD EFFECT TRANSISTORS*

#### INTRODUCTION

- The genre of Field Effect Transistors (**FET**) comprises of two types, namely (a) The Junction Field Effect Transistors (**JFET**) and (b) The Metal Oxide-Semiconductor Field Effect Transistors (**MOSFET**).
- Whereas, the **BJT** is a “**Current Controlled**” device (**Output current is a function of the Input Current**), and hence it is essentially a “**Current Amplifier**”, the **FETs are “Voltage Controlled” devices, (Output current is a function of the Input Voltage )** hence “**Voltage Amplifiers**”.
- A BJT has a couple of drawbacks.
  1. The first, the **BJT requires an Input Current to function. The input current has a “Loading Effect” on the signal source, resulting in power loss.**
  2. The second drawback is that, the current through the BJT has to flow through two P-N junctions, the forward biased Emitter-Base junction and the reverse biased Collector—Base junction. **A P-N junction has an internal capacitance in either kind of bias. Switching a current through a capacitance result in switching delays.**
- Both of these drawbacks are overcome in FETs, since they **do not require any Input Current, and the signal current of an**

### **FET does not pass through a P-N junction.**

- However, in general, BJT amplifiers provide greater power gain compared to JFET amplifiers.

**Table : 1. :- Comparison between BJT and FET**

Sl.No.	<b>FET</b>	<b>BJT</b>
1.	<p>FET is a Unipolar device, in that, the Current flow is due to only either Electrons of the Conduction Band or Holes of the Valence Band.</p>	<p>BJT is a Bipolar device. In both NPN and PNP transistor, the current flow consists of both CB Electrons and VB Holes.</p>
2.	<p>FET is a Voltage Controlled device. In this the output current is a function of the input voltage.</p>	<p>BJT is a Current Controlled device. In this the output current is a function of the input current.</p>
3.	<p>The Input Impedance of JFET is very high. It is in the order of a few Mega Ohms.</p>	<p>Input Impedance of BJT is in the order of a Few Kilo Ohms.</p>
4.	<p>JFET amplifiers are more stable w.r.t. temperature variations.</p>	<p>BJT amplifiers are inherently temperature Dependent.</p>
5.	<p>FETs occupy lesser amount of space. Hence, they are more suitable for ICs.</p>	<p>In general, BJT occupies more space.</p>
6.	<p>JFET amplifiers provide lesser voltage gain Compared to BJT amplifiers.</p>	<p>BJT amplifiers provide greater power gain Compared to JFET amplifiers.</p>
	MOSFETs require sensitive	

7.

physical handling due to the presence of the thin metal strip in its construction.

BJT are more robust to handle.

## Section-1

### *JFET*

#### 8.1 CONSTRUCTION AND WORKING PRINCIPLE

##### CONSTRUCTION :-

- ❖ The Junction Field Effect Transistor (JFET) can be of two types, namely, N-Channel JFET and P-Channel JFET.
- ❖ N-Channel JFET is constructed by encircling an N-type bar of silicon with a P-type ring.
- ❖ P-Channel JFET is constructed by encircling a P-type bar of silicon with a N-type ring.
- ❖ The construction of JFET and its transverse section is shown in the Fig- 1 below.
- ❖ Note that, even though, the transverse section appears to be consisting of two P-N junctions, in reality, **it is actually just one single P-N junction**.

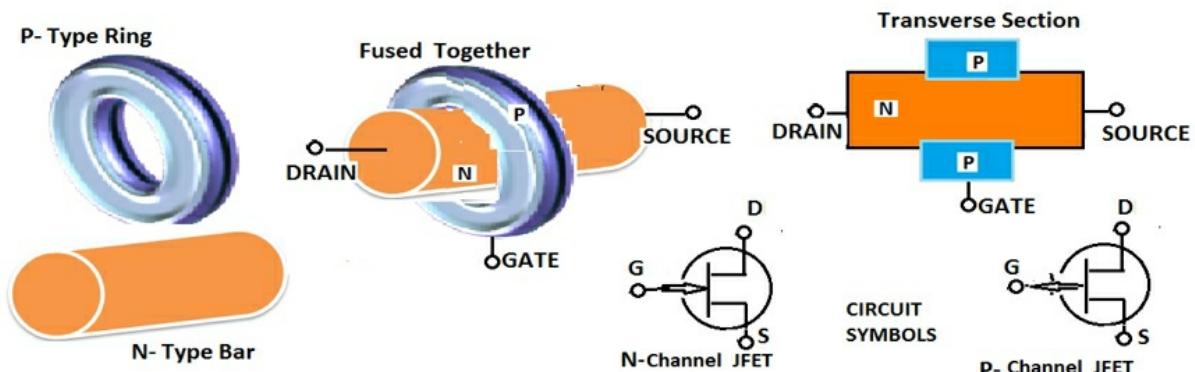
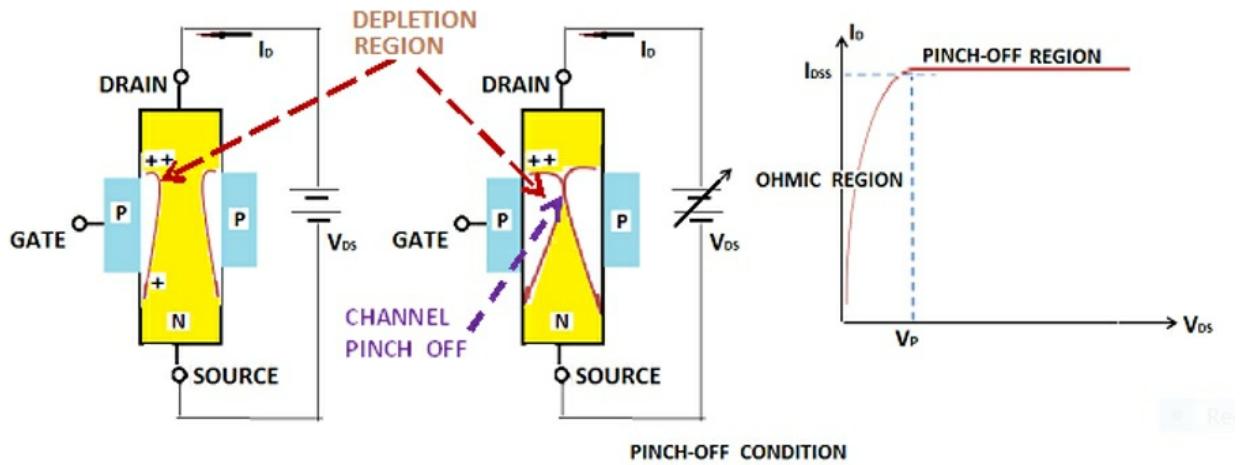


Fig- 1

## **PRINCIPLE of OPERATION : -**

- Consider the N-Channel JFET applied with a DC Bias  $V_{DS}$  as shown in the Fig- 2. Since the **N-Channel, i.e., the N-Type bar** has a low resistance; the current  $I_D$  through the channel increases rapidly corresponding to a very small change in applied voltage  $V_{DS}$ . This is shown in the graph alongside.
- Due to this flow of current there **occurs a potential drop** across it, in such a manner that **the upper portions of the channel are more positive compared to the lower portions**.
- In the P-N junction exists between the **bar and the ring**, since the ring is at zero potential and the N-Type channel is at a positive potential, the P-N junction **is at a reverse bias**. Due to the reverse bias, a depletion region is formed.
- Since the positive potential on the N-Type channel is more at the upper portions compared to the lower portions, the reverse bias is more at the upper portions compared to the lower ones. The width of the depletion region is proportional to the reverse bias. Thus, the depletion region is wider at the top than at the bottom.
- As the current  $I_D$  increases, the voltage dropped in the channel increases. Consequently, the potential difference between the P and the N regions also increase. Thus, the reverse bias also increases.
- This results in the increase in the width of the depletion region. Since the width of the depletion region increases, the effective cross-sectional area of channel decreases. This results in the increase in the resistance of the channel.
- In the graph between  $I_D$  vs  $V_{DS}$ , since **resistance is the reciprocal of the slope of the V-I graph**, the slope of the V-I graph goes on decreasing progressively with the increase of the applied bias  $V_{DS}$ . This gradual decrease in the slope of the graph between  $I_D$  and  $V_{DS}$  is shown in the figure.
- In this situation the device is following Ohm's Law, hence this portion of the graph is named as "**Ohmic Region**".



**Fig- 2 : - Pinch-Off Condition and Ohmic Region in the Drain Characteristic of a JFET.**

#### Pinch-Off Condition :-

- As the Drain Current  $I_D$  is increasing, the width of the depletion region is increasing consequently. As a result, the effective channel width is decreasing, thereby increasing the channel resistance.
- At a certain value of applied voltage,  $V_{DS} = V_p$  the depletion region is so wide that the **effective channel width tends to zero**. This condition is known as "**Pinch-Off**". Drain Current corresponding to this condition is  $I_{DSS}$ .
- Since at "**Pinch-Off**" the effective cross-sectional area of the channel is zero, **the resistance of the channel tends to be infinity**. In other words, the **slope of the V-I graph tends to be zero**. That is to say, the graph becomes horizontal.
- In this situation the Drain Current saturates at the value  $I_{DSS}$  (**Drain-Source Saturation current**).
- The Drain-Source voltage  $V_{DS} = V_p$ , at which Pinch-Off occurs is known as the **Pinch-Off voltage**.

#### **JFET Characteristics**

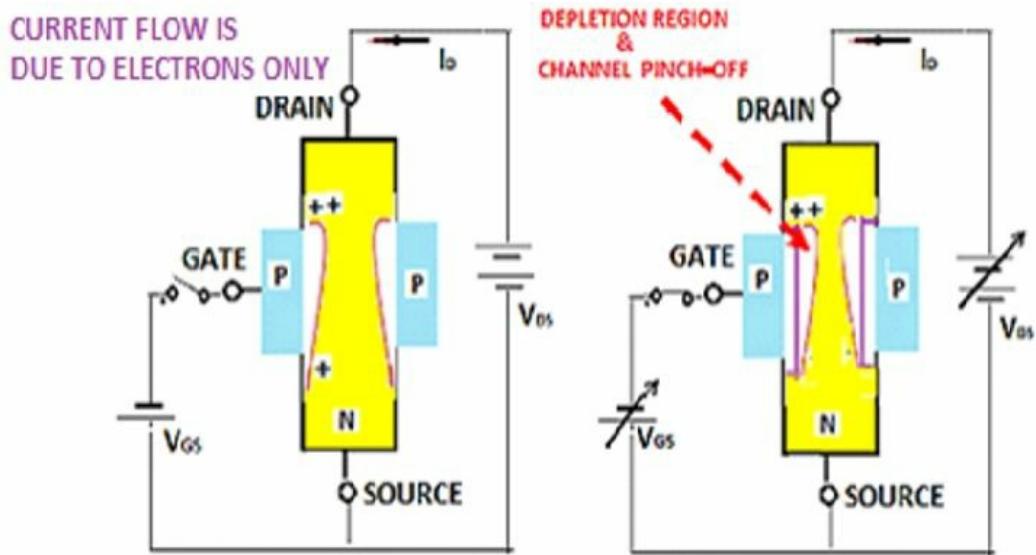
- ✓ The performance of any electrical device is studied with the help of its V-I Characteristics. The V-I Characteristic of a device is the graph showing the variation of current w.r.t. applied voltage. These in turn are dependent on the constructional features and working

principle of the device.

- ✓ In case of the JFET two sets of V-I Characteristics, namely, The Drain Characteristics and The Transfer Characteristics The circuit required to plot the V-I Characteristics of the JFET is shown in the figure below (Fig -3) .

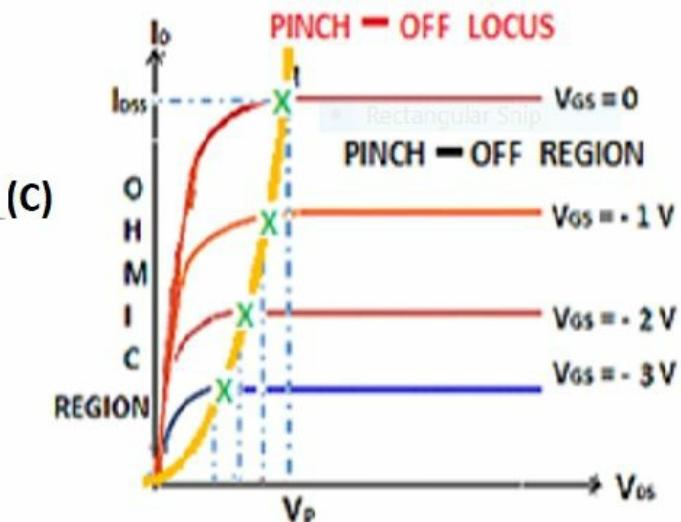
- 1). **DRAIN CHARACTERISTICS :-** The Drain Characteristics of a JFET is the graph between the Drain Current  $I_D$  as a function of the Drain-Source voltage  $V_{DS}$ . Refer to the circuit in Fig -3 (A).

Since the Gate-Source circuit is open circuited, the applied voltage at the Gate terminal  $V_{GS} = 0$ . The situation is similar to the circuit in Fig-2.



(A)

(B)



**Fig-3.: -** The circuit for plotting JFET Characteristics. Fig (C) shows the Drain Characteristics.

- Initially the resistance of the N-channel is low. As the Drain-Source voltage  $V_{DS}$  is gradually increased, the Drain Current  $I_D$  increases rapidly. In this process the voltage drop across the channel is also increasing, so that the positive potential in the N-Type channel region is increasing.
- As a result, the reverse bias between the Channel and Gate P-N junction is going on increasing. This results in the increase in the

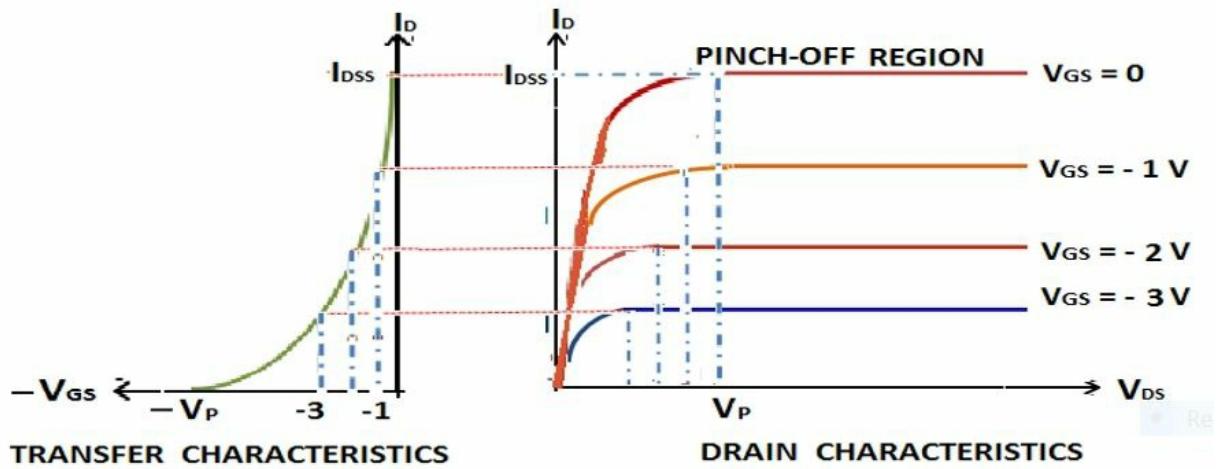
width of the depletion region.

- This in turn results in the decrease in the effective cross sectional area of the channel, which leads to the increase in the channel resistance.
- As the channel resistance increases the rate of rise of the Drain Current w.r.t. Drain-Source voltage decreases.
- As  $V_{DS}$  is further increased, the reverse bias also increases accordingly channel width decreases, accompanied by increase in channel resistance. This results in further reduction in the rate of rise of  $I_D$ .
- At a value of  $V_{DS} = V_p$  Pinch-Off occurs. In this situation the channel resistance tends to infinity and the Drain Current begins to saturate at the level  $I_{DSS}$ .
- Further increase in  $V_{DS}$  does not affect the value of Drain Current.
- Now consider Fig -3 (B). In this a reverse bias  $V_{GS}$  (say  $V_{GS} = -1$  V) is applied to the Gate terminal. This results in an initially uniform depletion region.
- If the Drain-Source voltage  $V_{DS}$  is now increased, the drain current is flowing through an already constricted channel. This constricted channel has a higher resistance.
- Therefore, the initial rate of rise of the Drain Current  $I_D$ , w.r.t. the applied voltage  $V_{DS}$  is rather less.
- As the voltage  $V_{DS}$  is further increased, the voltage drop in the channel also increases, thereby further increasing the reverse bias across the Channel-Gate P-N junction and consequent increase in the width of the depletion region, resulting in the constriction of the channel further.
- Thus Pinch-Off occurs at a lesser value of  $V_{DS}$  and the Drain Current saturates at a lower value.
- If this experiment is repeated with higher and higher initial values of reverse bias  $V_{GS}$  ( say  $V_{GS} = -2$  V, - 3 V, - 4 V etc.), the process of Pinch-Off occurs at progressively lower values and consequently, Drain Current also saturates at progressively lower values. Hence we get a graph as shown in Fig- 3 (C). This is the Drain Characteristics of a JFET.

PINCH-OFF LOCUS : - In the Fig- 3 (C), if we mark the points at which Pinch-Off occurs and join these points, we get the Pinch-Off Locus. This is in the **shape of a Parabola** touching the origin.

2). TRANSFER CHARACTERISTICS :- The Transfer Characteristics of a JFET is the graph between the Drain Current  $I_D$  as a function of the Gate-Source voltage  $V_{GS}$ .

- Refer to the Fig-3 (C). When the Gate-Source reverse bias  $V_{GS} = 0$ , the Drain Current saturates at  $I_{DSS}$ , irrespective of the value of Drain-Source voltage, provided,  $V_{DS} \geq V_p$ .
- If we keep Drain-Source voltage constant at some value  $V_{DS} \geq V_p$  and progressively increase the Gate-Source reverse bias  $V_{GS}$ , the Drain Current will get saturated at progressively lower values.
- When  $V_{GS} = -V_p$ , the initial depletion region in the channel will be so wide as to completely constrict the channel, so that the Drain Current will remain at zero irrespective of the Drain-Source voltage.



**Fig-4.: -** The Transfer Characteristics of a JFET is plotted by setting  $V_{DS} \geq V_P$  and plotting the variation of  $I_D$  w.r.t. the applied reverse bias  $V_{GS}$  at the Gate terminal.

- Thus, we get a graph between  $I_D$  and  $V_{GS}$  as shown in the Fig. – 4. This is the **Transfer Characteristic** of the JFET.
- The shape of the Transfer Characteristic shows a “Square Law” shape, as will be explained later. This graph is drawn on the second quadrant since the quantity  $V_{GS}$  is a reverse a reverse bias, while  $I_D$  is positive.

### JFET as a Voltage Controlled Resistance

- ✓ In the Drain Characteristic of the JFET shown in Fig -3 (C), the portion of the graph to the left of the Pinch Off parabola represents a current that is directly proportional to the applied voltage  $V_{DS}$ .
- ✓ Hence, in this portion of the graph, the device is following Ohm's Law. And hence the name “Ohmic Region”. The reciprocal of the slope of the any V-I Characteristic graph of any device represents the resistance of that device. It is observed that the graph has a varying slope in this region.
- ✓ This has been explained earlier in terms of the constriction of the channel width due to the growth of the depletion region as a function of the applied voltage  $V_{DS}$ .

- ✓ Further we note that the rate of decrease of the slope (which means the rate of increase of the resistance) is a function of the reverse bias  $V_{GS}$  applied at the Gate terminal also.
- ✓ When the reverse bias  $V_{GS}$  is less the rate of decrease of the slope of the graph is more and the vice-versa. In other words, the resistance of the channel is also a function of the applied reverse bias  $V_{GS}$ .
- ✓ Hence, the JFET behaves as a “Voltage Controlled Resistance” in the Ohmic Region, in which, the controlling voltage is  $V_{GS}$ .
- ✓ The resistance of the JFET in the Ohmic Region is represented by the expression given below

$$r_d = \frac{r_o}{(1 - V_{GS}/V_p)^2} \quad \dots(1)$$

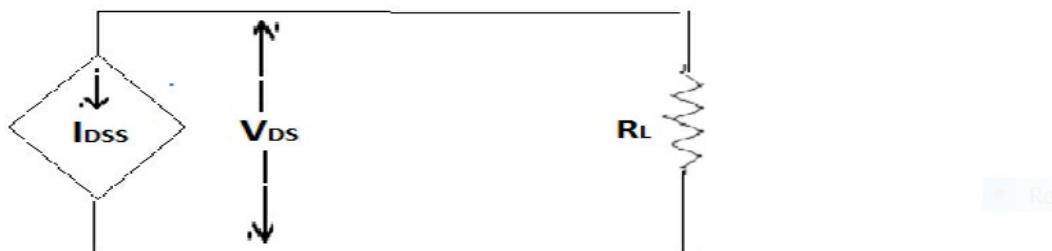
where  $r_o$  is the resistance of the JFET when  $V_{GS} = 0$ . Typically for a N

- Channel JFET  $r_o$  is of the order of  $10 \text{ K}\Omega$ .

### JFET as a Constant Current Source

In the Pinch-Off region the Drain Current is at a constant value  $I_{DSS}$  irrespective of the value of the applied voltage  $V_{DS}$ . Hence the JFET behaves as a “Constant Current Source”.

For  $V_{GS} = 0$ , the JFET can be represented by the equivalent circuit shown in Fig-5.



**Fig-5:** - Representation of JFET as a Constant Current Source.

### Shockley's Equation & JFET Transfer Characteristic.

The JFET is a “Voltage Controlled” device, where the output current is controlled by an input voltage. The Output Current is the Drain Current  $I_D$  and its Input Voltage is  $V_{GS}$ . William Shockley devised

an expression for the JFET to represent its output current  $I_D$  as a function of the control voltage  $V_{GS}$ . This is known as the Shockley's Equation for JFET (Recall that we had another expression by the same name for describing the current in a P-N junction as a function of the applied voltage. **This expression is different, and is specifically applicable to the JFET only.**). Without going into the specific steps of derivation the Shockley's Equation for JFET is presented as follows. This expression can be used to plot the Transfer Characteristic of the JFET without the help of a laboratory set up.

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \quad \underline{\dots}(2)$$

**Steps for plotting Transfer Characteristics :** — From the Shockley's Equation, a method for plotting the Transfer Characteristics is obtained, as follows—

1. Substituting  $V_{GS} = 0$  in Eq. 2 – we get

$$I_{D1} = I_{DSS} \left( 1 - \frac{0}{V_P} \right)^2$$

$$I_{D1} = I_{DSS}$$

Hence we get the co-ordinates of the first point as  $(0, I_{DSS})$ .

2. Substituting  $V_{GS} = | -\frac{1}{2} V_P |$  we get

$$I_{D2} = I_{DSS} \left( 1 - \left| -\frac{V_P}{2} \right| \right)^2 / V_P$$

$$I_{D2} = I_{DSS} \left( 1 - \frac{1}{2} \right)^2 = I_{DSS}/4$$

Hence we get the co-ordinates of the second point as  $(-\frac{1}{2} V_P, I_{DSS}/4)$ .

1. Substituting  $V_{GS} = | -0.3 V_P |$  we get

$$I_{D3} = I_{DSS} \left( 1 - \frac{|-0.3V_P|}{V_P} \right)^2$$

$$I_{D3} = I_{DSS} (1 - 0.3)^2 \cong I_{DSS}/2$$

Hence we get the co-ordinates of the third point as  $(-0.3V_P, I_{DSS}/2)$ .

2. Substituting  $V_{GS} = | - V_P |$  we get

$$I_{D4} = I_{DSS} \left( 1 - \frac{|-V_P|}{V_P} \right)^2 = 0$$

Hence we get the co-ordinates of the fourth point as  $(-V_P, 0)$ .

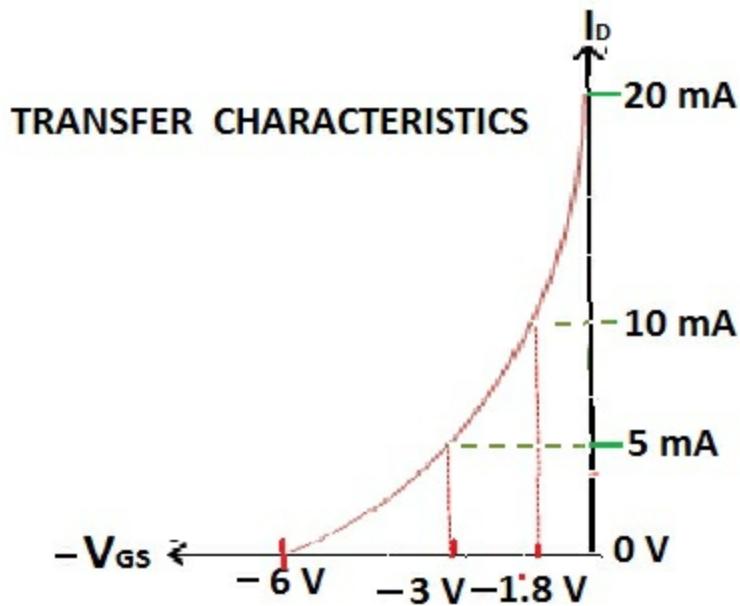
### TUTORIAL-1

**Example 1.** Plot the Transfer Characteristics of a JFET whose parameters are  $I_{DSS} = 20 \text{ mA}$ ,  $V_P = -6 \text{ V}$ .

**SOLUTION :** If we follow the steps as enumerated above, we get

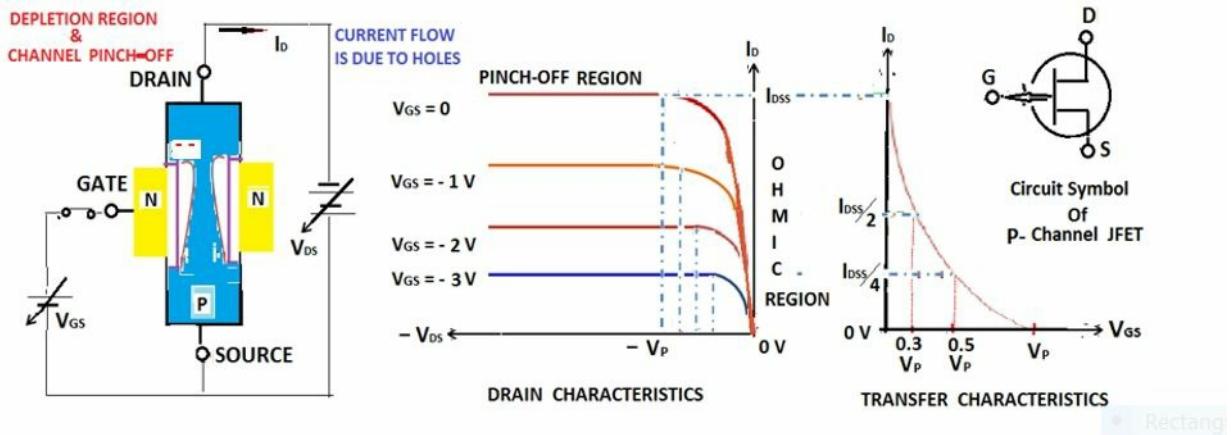
1. At  $V_{GS} = 0$ , we have  $I_D = I_{DSS}$   $\therefore$  the coordinates of **first point is (0V, 20mA)**.
2. At  $V_{GS} = -1/2 V_P = -3V$ , we have  $I_D = I_{DSS}/4$   $\therefore$  the coordinates of **second point is (-3V, 5mA)**.
3. At  $V_{GS} = -0.3V_P = -1.8V$ , we have  $I_D = I_{DSS}/2$   $\therefore$  the coordinates of **third point is (-1.8V, 10mA)**.
4. At  $V_{GS} = -V_P = -6 \text{ V}$ , we have  $I_D = 0$   $\therefore$  the coordinates of **fourth point is (-6 V, 0)**.

With these four points we can sketch the Transfer Characteristics as follow



## P<sup>-</sup> CHANNEL JFET

The construction of the P<sup>-</sup> Channel JFET is just the opposite of that of the N<sup>-</sup> Channel JFET. In the P<sup>-</sup> Channel JFET the channel is of a P<sup>-</sup> Type material, whereas the ring is of the N<sup>-</sup> Type material. The working principle and circuit behavior are just the same as the N<sup>-</sup> Channel JFET. However, the polarities of the biasing voltages and the directions of the Drain Current are opposite. In other words, the N<sup>-</sup> Channel and P<sup>-</sup> Channel JFET are duals of each other, just as the NPN and PNP Transistors are. The circuit diagram for plotting the characteristic graphs is as shown in the Fig- 6 below. Even though the Drain Characteristics and the Transfer Characteristic graphs are shown in opposite quadrants, w.r.t. that of the N<sup>-</sup> Channel JFET, in practice, they need not be shown as such. In fact, they can be shown in the same orientation, just as is the convention for PNP and NPN transistors.



**Fig- 6:** -The circuit diagram for plotting the characteristics of the P-Channel JFET. It is to be noted that, even though the characteristic graphs have been shown in opposite quadrants compared to the N- Channel JFET, in practice, it need not be so. The P-Channel JFET & N-Channel JFET are in fact duals of each other.

## 8.2 JFET Parameters

The JFET as a circuit component has the following circuit parameters. Their definitions are given as under—

1. **Drain-Source Saturation Current  $I_{DSS}$**  is defined as the value at which the Drain Current saturates under the condition when the Gate is open circuited ( $V_{GS} = 0$ ).
2. **Pinch-Off Voltage  $V_p$**  is defined as the value of Drain-Source voltage ( $V_{DS} = V_p$ ) at which channel is effectively “Pinched-Off” by the depletion region (so that the channel width tends to zero), so as to saturate the Drain Current at the value  $I_{DSS}$  under the condition of open circuited Gate.
3. **Forward Transfer Admittance ‘ $g_m$ ’ (Also denoted as ‘ $Y_{fs}$ ’)** is defined as the rate of change of Drain Current  $I_D$  w.r.t. Gate-Source voltage  $V_{GS}$  under the condition when  $V_{DS} > V_p$ . In fact  $g_m$  defines the slope of the Transfer Characteristics. Typical values of  $g_m$  are of the order of a few thousand  $\mu\text{S}$  (micro Siemen, say 3000

$\mu\text{S}$ ).

4. **Output Admittance  $Y_{OS}$  (sometimes denoted as  $1/r_D$ )** is defined as the rate of change of Drain Current w.r.t. Drain-Source voltage  $V_{DS}$  when  $V_{DS} > V_P$ . In other words  $Y_{OS}$  is the slope of the Drain Characteristics in the Pinch-Off region. (Consequently the Drain-Source resistance  $r_D$  is the reciprocal of the slope of the Drain Characteristics). Typical values of  $Y_{OS}$  are of the order of a few tens of  $\mu\text{S}$  (say 20 to 50  $\mu\text{S}$ ). Consequently, the typical values of  $r_D$  will range from 50  $\text{K}\Omega$  to 20  $\text{K}\Omega$ .
5. **AC Drain-Source resistance  $r_{ds}$**  is defined as the resistance of the JFET in the Ohmic Region, when the depletion region has been created. This is given by the expression of Eq. 6.1. Typical value of this quantity is about 10  $\text{K}\Omega$ .
6. **DC Drain-Source Resistance  $R_{DS}$**  is defined as the resistance of the JFET channel when the depletion region is absent. The typical value of this quantity is about 50 to 60  $\Omega$ .
7. **Gate Cut-Off Current  $I_{GSS}$**  is defined as the reverse saturation current of the reverse biased Gate-Channel P-N junction. Typical values of this can range from 5 nA to 100 nA.
8. **Gate Input Resistance  $R_{GS}$**  is defined as the resistance of the reverse biased Gate-Channel junction. Typical values of this parameter can range from  $10^7 \Omega$  to  $10^9 \Omega$ .
9. **Gate-Source Breakdown Voltage  $BV_{GSS}$**  is defined as the reverse voltage at which the Gate-Source junction breaks down. Typical value of this parameter is 25 V.
10. **Drain-Source Breakdown Voltage  $BV_{DS}$**  is defined as the maximum voltage that can be applied across the Drain and the Source terminals under the condition when Gate is open circuited, before the depletion region responsible for the Pinch-Off condition breaks down. This parameter is of the order of about 25 to 35 V.
11. **Gate-Source Capacitance  $C_{GS}$  (or Input Capacitance  $C_{iss}$ )** is defined as the capacitance associated with the depletion region of the reverse biased Gate-Source junction, under the condition when the Drain terminal is short circuited to the

**Source. Since the Gate is the input terminal of the JFET, it is also the Input Capacitance. The typical value of this parameter is about 7 pF.**

12. **Gate-Drain Capacitance  $C_{GD}$  (or Shunt Capacitance  $C_{rSS}$ )** is defined as the capacitance between the Gate and the Drain terminals when the Drain terminal is short circuited to the Source. Since the Drain terminal is the output terminal of the JFET, this capacitance has the effect of shunting the input signal directly to the output without being amplified. The typical value of this parameter is about 3 pF.

## **Section-2**

### **MOSFET**

#### **8.3 E-MOSFET and D-MOSFET**

- The JFET is used both as a small signal amplifier as well as a switch.
- The MOSFET is used as a Power Amplifier and Power Switch, and sometimes as a large current source.
- The acronym MOSFET stands for ‘Metal Oxide Semiconductor Field Effect Transistor’. There are three classes of MOSFETs, namely,
  - a) **E-MOSFET, or Enhancement MOSFET .**
  - b) **D-MOSFET, or Depletion MOSFET .**
  - c) **V-MOSFET.**

Each of these has different constructions and working principles. And each is used for specific purposes.

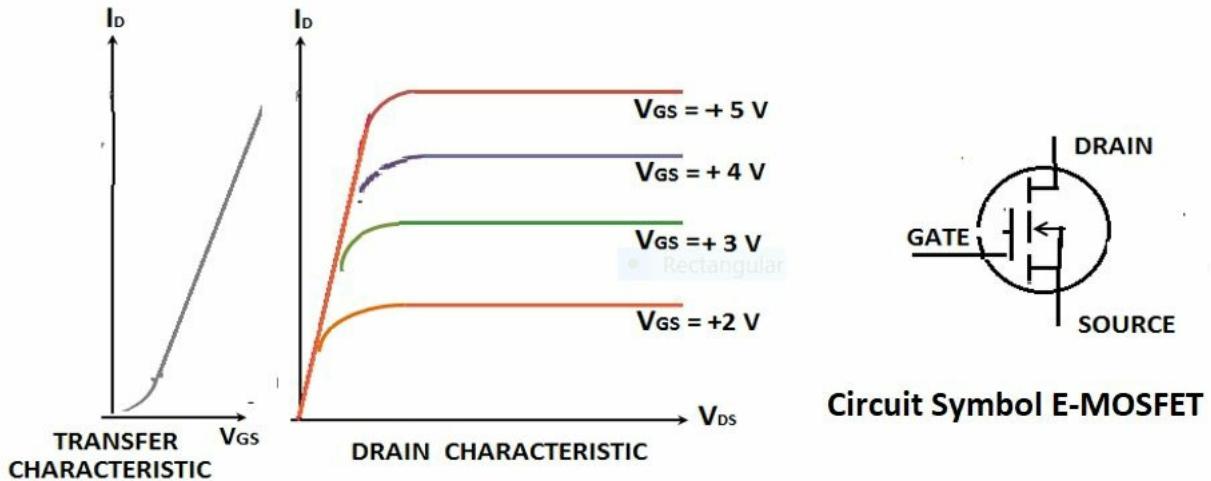
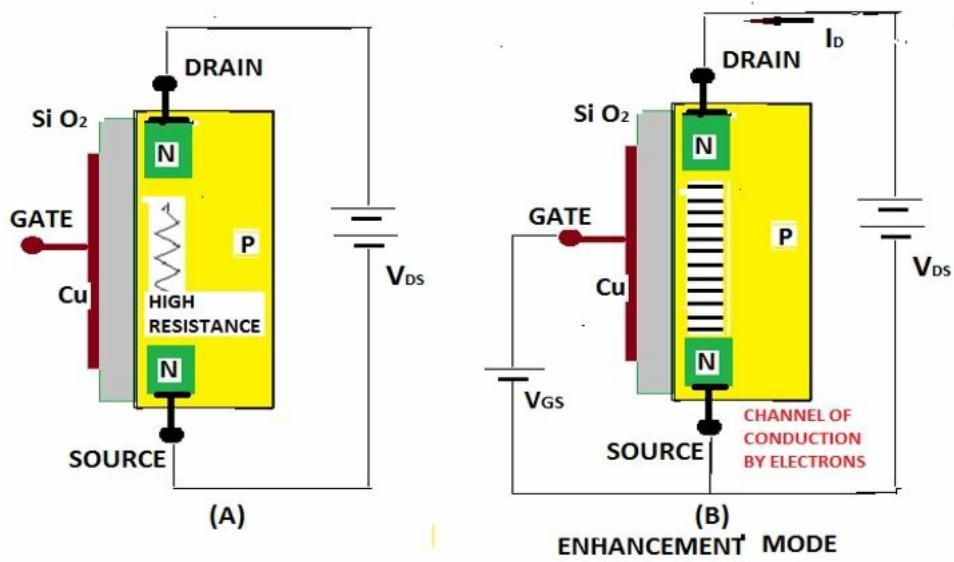
#### **E-MOSFET**

## **COSTRCTION and PRINCIPLE: -**

The constructional features and characteristics of an N-Channel E-MOSFET are shown in the **Fig- 7** below.

The current flow in the device is due to electrons only.

The P-Channel dual is just the opposite in construction and the current being comprising solely of holes, **while working on the same principle.**



**Fig-7:** - Constructional features of E-MOSFET and the Characteristic graphs.

➤ N-Channel E-MOSFET consists of a **highly resistive P-Substrate**, (i.e., a slab of lightly doped P-Type material,) **embedded with two highly doped N-regions on both ends**. One end is the Source terminal and the other is the Drain terminal. In the middle portion a layer of Silicon Di-oxide ( $\text{Si O}_2$ ) insulating layer is deposited. Over this a Cu strip is soldered, which is the Gate terminal. Hence the name “Metal” –“Oxide” –“Semiconductor” FET. (MOSFET)

## DRAIN CHARACTERISTICS

- In the circuit in part (A). the channel is biased with  $V_{DS}$ . The P-Substrate has a very low level of doping; hence it has a very high resistance. Therefore, current flow is negligible.
- In the circuit in part (B). A positive potential  $V_{GS}$  is applied to the Gate terminal. This has the tendency to attract the valence electrons of the semiconductor material. But due to the presence of the insulating  $Si O_2$  layer these electrons cannot flow out to the positive end of the battery  $V_{GS}$ .
- **These electrons form an induced N-Channel inside the P-Substrate.** and they flow out to the positive end of  $V_{DS}$ , resulting in the **Drain Current  $I_D$** .
- Initially when  $V_{DS}$  is low, the current  $I_D$  has a low magnitude. As  $V_{DS}$  increases, the current increases rapidly.
- The number of electrons in the **N-channel** is a function of the Gate bias  $V_{GS}$ . Hence at a constant value of  $V_{GS}$  the Drain Current quickly saturates.
- Now, if we apply a higher amount of Gate bias, the number of valence electrons increase and consequently the saturation level of the Drain Current is also higher.
- Hence, we have the **Drain Characteristic** of MOSFET as shown in the Fig-7 above.

## TRANSFER CHARACTERISTICS

- As explained above, the Drain Current is a function of the Gate bias  $V_{GS}$ . When  $V_{GS}$  is low, the Drain Current is also low and as  $V_{GS}$  increases,  $I_D$  also increases in **an almost exponential manner**. Hence we have the shape of the Transfer Characteristic as shown in the figure.

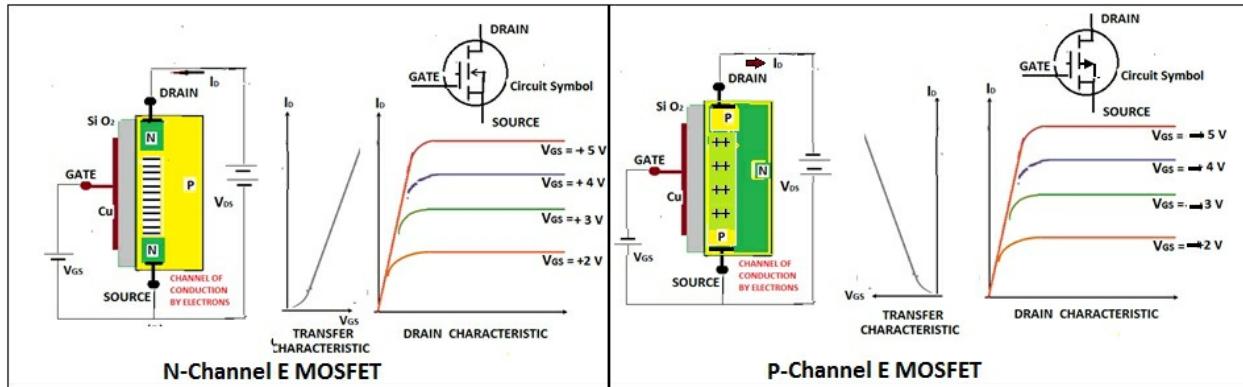
## CIRCUIT SYMBOL OF MOSFET

( N-Channel & P-Channel )

The circuit symbol of the N-Channel E-MOSFET device in Fig-7 indicates that the P-Substrate is initially non-conducting. Hence it is

shown by a broken line. As the Gate Bias is applied, as indicated by the small arrow at the Gate terminal, the device goes into conduction. The Gate terminal is shown detached from the P-Substrate, since it is actually so due to the presence of the insulating  $\text{Si O}_2$  layer.

The construction of the P-Channel E-MOSFET is just the opposite. It has an N-Substrate and P-Type Source and Drain regions. Hence the polarities of all the bias voltages are opposite. However, the working principle is just the same as described above, but the Drain Current is constituted of holes and consequently, has an opposite direction of flow. The circuit symbol of the P-Channel E-MOSFET has the arrow pointing outwards.



## D-MOSFET

### CONSTRUCTION & PRINCIPLE :-

A lightly doped N-Type channel is embedded between the Source and Drain regions. This region has a high resistance. **The device can work in both Enhancement Mode as well as Depletion Mode.**

#### **Depletion Mode:-**

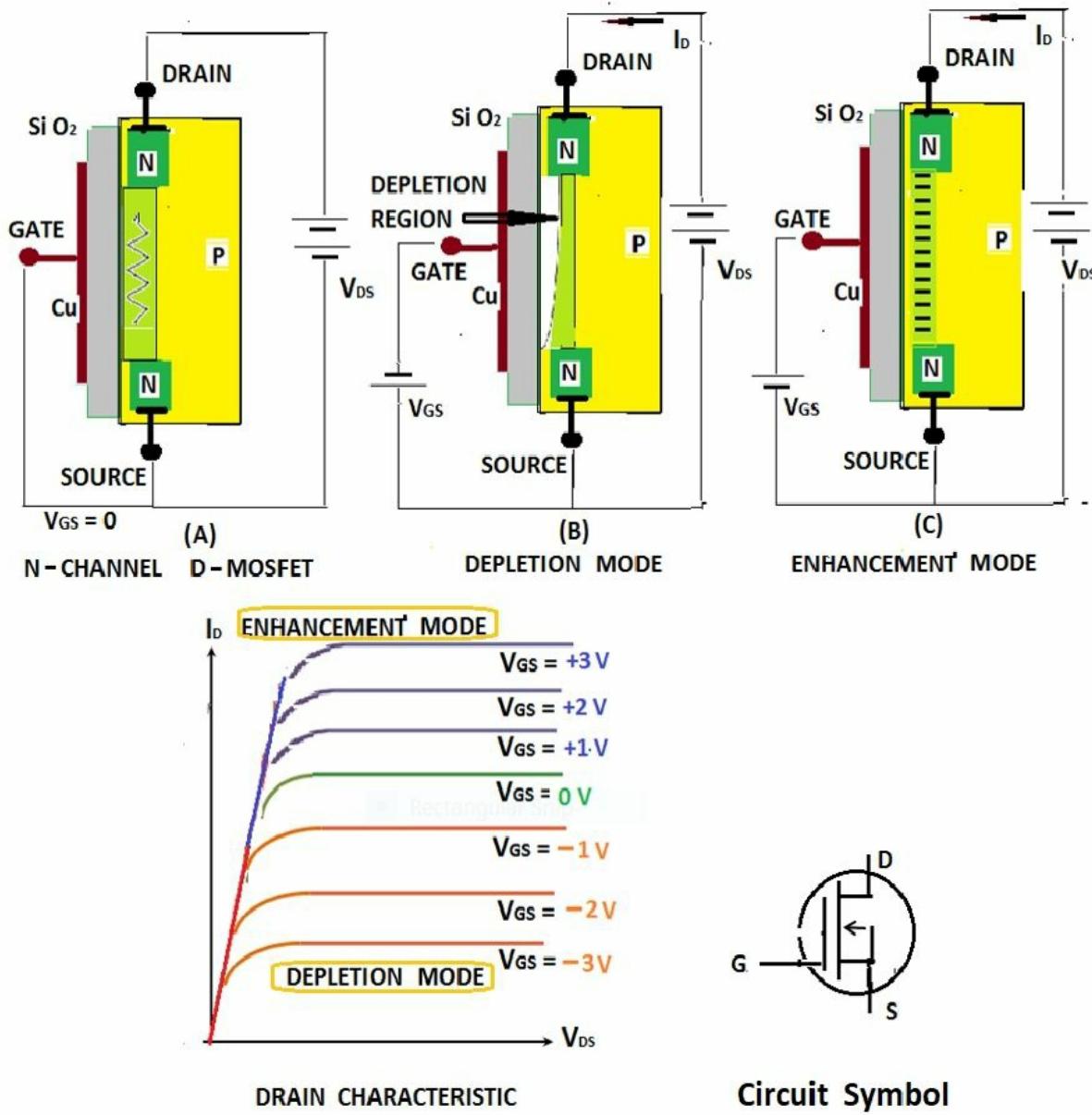
- Consider a situation when a bias  $V_{DS}$  is applied but the Gate potential is zero, as shown in part (A) of Fig-8.
- As  $V_{DS}$  is increased, the Drain Current increases rapidly. But in this process, there appears an internal positive potential in the N-

Channel, due to which a reverse bias condition exists.

- Due to this reverse bias, the channel gets constricted, just as it happened in case of the JFET. Eventually Pinch-Off occurs and the Drain Current saturates at a certain value.
- If an external negative  $V_{GS}$  is applied, as shown in part (B) of the figure, the depletion region grows more rapidly and the Drain Current saturates at a lower value. When a larger negative Gate bias is applied, the Drain Current saturates at a still lower value, and so on.
- **Thus, in the Depletion Mode, the D-MOSFET is essentially behaving as a JFET.**

### **Enhancement Mode: -**

- When a positive Gate bias is applied, as shown in part (C) of the figure, the device behaves just as in an E-MOSFET. Thus, Drain Current gets saturated at higher and higher values as the applied Gate bias becomes more positive.
- Since the device works in **both Depletion Mode as well as Enhancement Mode**, it is often called **DE-MOSFET** also.
- Since there occurs conduction even when the Gate bias is zero, the circuit symbol of the device shows the channel as a solid line, unlike the D-MOSFET.

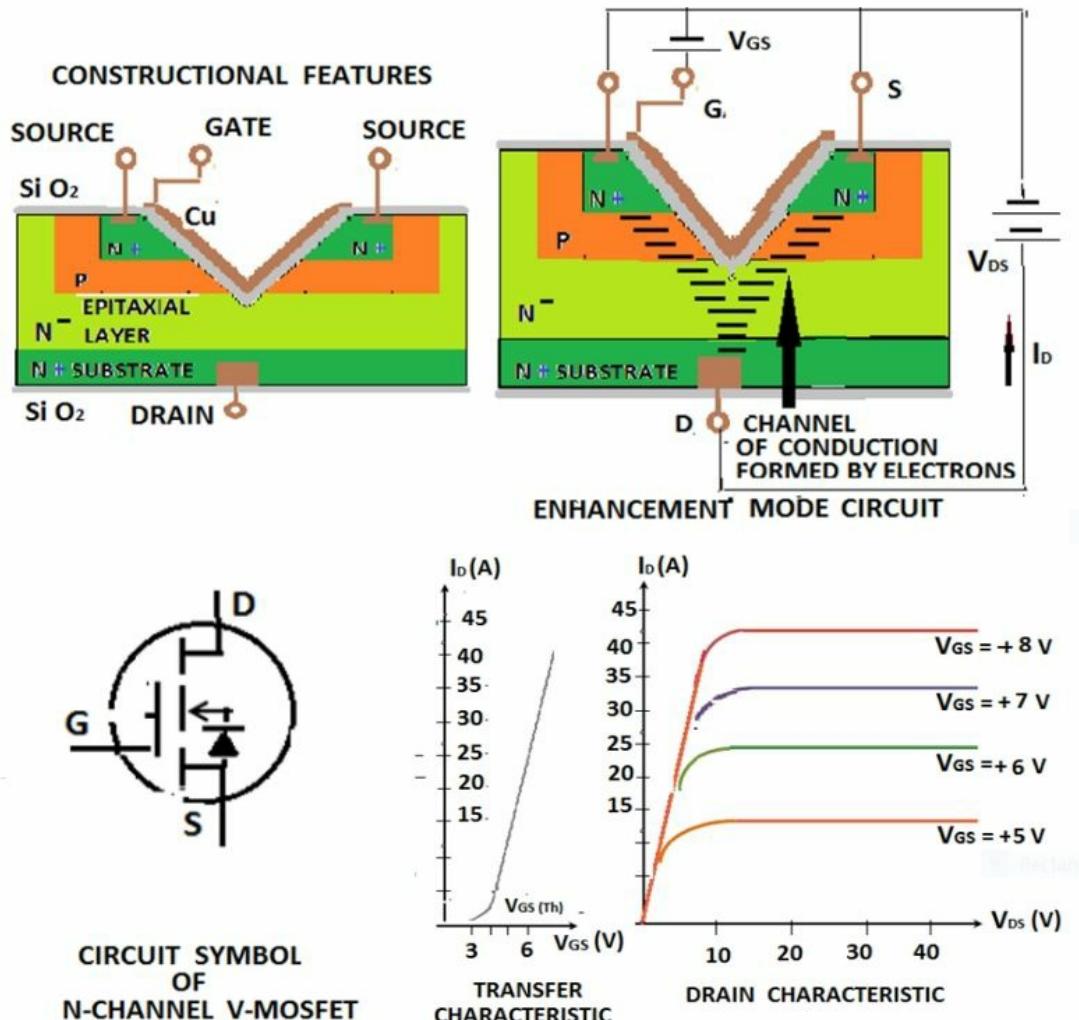


**Fig -8: - Constructional Features and Drain Characteristics of N-Channel**

### V-MOSFET

- ❖ **The E-MOSFET and D-MOSFET are Low power devices**, in that, the power dissipation in these devices range in the order from a few hundred milli Watt to a few Watts at the best.
- ❖ **The V-MOSFET is designed to handle large power levels**. Thus, these are used in large power applications like control equipment for electrical power systems. The constructional features and

typical characteristic graphs are shown in the Fig- 9.



**Fig 9:** - Constructional Features and Characteristic graphs of N-Channel V-MOSFET. Along with the Circuit Symbol.

## **CONSTRUCTION & PRINCIPLE :-**

- A compound crystal is formed by growing a **lightly doped N-Type Epitaxial layer** over a heavily doped N-Type substrate.
  - Over this a P-Type layer is grown.
  - On top of that another heavily doped N-Type layer is grown.
  - The **heavily doped N-Type layers are shown as  $N^+$**  and the **lightly doped N-Type layer is shown as  $N^-$**

- A deep V-cut is made on this compound crystal in such a manner that the vertex of the ‘V’ almost touches the N<sup>+</sup> substrate. The upper and lower surfaces of the crystal are covered by an insulating Si O<sub>2</sub> layer and a Cu coating is soldered over the V-cut. **The copper contacts are embedded into the substrate.**
- The two upper N<sup>+</sup> parts containing the “V”, **form the Source terminals**. And the lower N<sup>+</sup> **forms the Drain**.
- **The Cu layer over the V-cut forms the Gate terminal.**

### WORKING PRINCIPLE

- ✓ **The V-MOSFET works only in the Enhancement Mode.**
- ✓ If a Drain-Source potential V<sub>DS</sub> is applied, in the absence of a **Gate bias**, the device does not conduct appreciably since the lightly doped N<sup>-</sup> epitaxial layer has a very high resistance. **It remains non-conducting even when a small positive potential is applied at the Gate.**
- ✓ When a positive potential V<sub>GS</sub>  $\geq$  V<sub>GS(Th)</sub> is applied, it begins to attract some electrons from the N<sup>+</sup> layer, which now form a conducting N-Channel between the substrate and the upper N<sup>+</sup> layer. Thus a Drain Current I<sub>D</sub> starts to flow.
- ✓ As we increase the Drain bias V<sub>DS</sub> the current rises sharply up to a certain value. At a certain value of V<sub>DS</sub> the channel begins to saturate and the current I<sub>D</sub> becomes constant.
- ✓ If a larger value of Gate bias V<sub>GS</sub> is applied, more electrons are attracted into the channel. Thus value of saturation current is higher and so on.

### SPECIAL NATURE OF V-MOSFET

- ✓ This device can support a large current as the channel resistance is very low. **This low resistance is due to two factors.** Firstly, the channel length is much shorter and secondly the cross-sectional area of the channel is large.

- ✓ Due to the geometry of the crystal, the **device can withstand a large potential difference across the Drain and the Source terminals. Thus, the power rating of the device is also large compared to the JFET, D-MOSFET and E-MOSFET.**
- ✓ Due to the low resistance-high voltage combination **this device is capable of very fast switching.**
- ✓ The Transfer Characteristic is almost linear and has a sharper slope. As a result this device offers a **much larger value of “Forward Transfer Conductance”  $g_m$ .**
- ✓ Since voltage gain is proportional to  $g_m$ , the **V-MOSFET amplifier provides a much larger voltage gain compared to JFET amplifier.**
- ✓ Note that the circuit symbol of the device **includes the symbol of a diode** between the Source and the gate. This represents the P-N

$N^-$  junction formed by the P and the  $N^-$  layer of the crystal. This diode has a parasitic effect. **The biasing of the V-MOSFET must be such as to always reverse bias this parasitic diode.**

### Section-3 JFET Amplifiers

#### 8.4 FET Biasing Circuits

A JFET is a three-terminal device just as the BJT. Thus, it can be connected in three configurations, namely,

1. **Common-Source Configuration.**
2. **Common-Drain Configuration.**
3. **Common-Gate Configuration.**

Out of these it can be shown that only the Common-Source (CS) configuration provides substantial voltage gain. Hence all biasing circuits to be discussed herein will have the JFET in the CS configuration.

In order to use the JFETs as amplifiers **they have to be biased in the Pinch-Off region** of the Drain Characteristics. The Pinch-Off region

is the region of the characteristic where the Drain Current becomes constant (saturated). The Load Resistance determines the operating point Q. The Q-Point is obtained from the Transfer Characteristics, from which, the operating values of the Drain Current  $I_{DQ}$  and the Gate-Source bias  $V_{GSQ}$  is obtained. The value of Drain Current is substituted in the Load Line equation to obtain the operating value of the Drain-Source bias voltage  $V_{DSQ}$ . Two biasing circuits are most commonly used for FETs, namely,

(i) Self-Bias Circuit

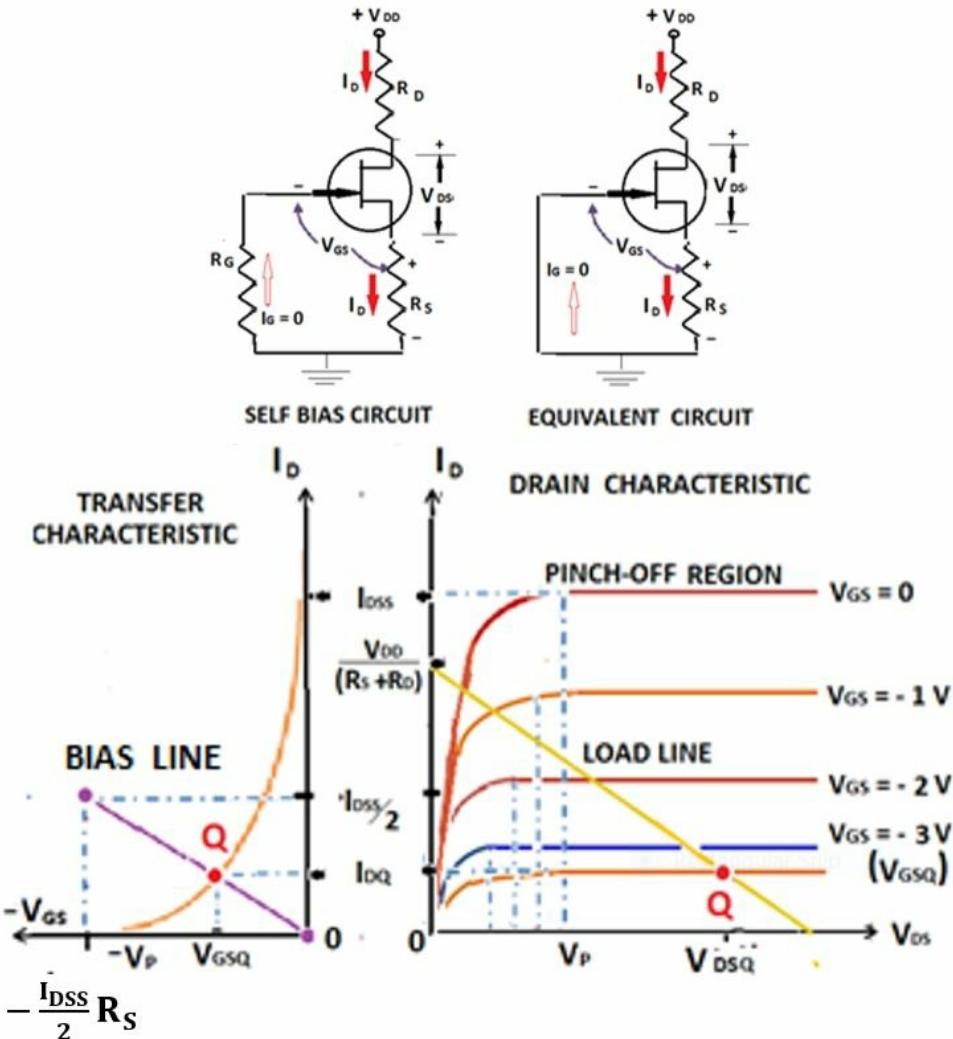
and

(ii) Voltage Divider Bias Circuit.

All types of FETs, i.e., JFET, E-MOSFET, D-MOSFET and V-MOSFET can use the same circuits. Hence a common analysis is sufficient for all types of FETs.

### **Self-Bias Circuit**

The Self Bias circuit for an N-Channel JFET is shown in the Fig-10. For the P-Channel JFET the polarities of the biasing potential and the direction of current will be just the opposite. The same steps of analysis will work for both N-Channel and P-Channel devices, since they are Duals of each other (just like NPN and PNP transistors).



**Fig. 10:** - The Self Bias Circuit of JFET, the DC Load Line and the Operating Point.

#### WORKING PRINCIPLE :-

Consider an N-Channel JFET. The bias potential between the Drain and the Source must be positive at the Drain and negative at the Source (this is provided by  $+V_{DD}$ ), whereas the bias potential between the Gate and the Source must be negative at the Gate and positive at the Source. In a JFET, the Gate is reverse biased. Therefore, it has a very high resistance and the current  $I_G$  flowing into the Gate is negligible. Hence, we can assume the resistance  $R_G$  as a short circuit and the Gate terminal to be shorted to the Source in the equivalent circuit. Since Source is at ground, which is relatively negative to  $+V_{DD}$ , the potential  $V_{GS}$  appears as a negative potential. The current in the channel is  $I_D$ ,

which flows in at the Drain and flows out at the Source. Thus, the same current flows through the resistances  $R_D$  and  $R_S$ . When a single DC source  $V_{DD}$  is used, the circuit should be so designed that the voltage drop at these two resistances leave enough potential difference  $V_{DS}$

between the Drain and the Source terminals so that  $V_{DS} \geq V_p$ . In fact,  $V_{DS}$  must be significantly greater than  $V_p$ . Thus, the JFET gets the required bias to be operating in the Pinch-Off region of its characteristic.

ANALYSIS :- The Kirchhoff's Voltage Law equation of the Gate-Source loop in the equivalent circuit in the Fig.-10 above is given by

$$I_D R_S - V_{GS} = 0$$

$$\therefore I_D = \frac{V_{GS}}{R_S} \quad \dots(3)$$

This is a first order equation of the variable  $I_D$  as a function of  $V_{GS}$ . Thus the plot of this equation is a straight line on the Transfer characteristics. This line is known as **The Bias Line**. In order to plot any straight line the coordinates of any two points on the line are required.

- (i) For the first point, substituting  $V_{GS} = 0$  in Eq. 3 we get the value of  $I_D = 0$ . Thus the **first point is the origin ( 0 : 0 )**.
- (ii) For the second point we may take any value of  $I_D$ . As a matter of convenience, if we substitute  $I_D = I_{DSS}/2$  in Eq. 6.3, we get  $V_{GS} = \frac{I_{DSS} \cdot R_S}{2}$ . Thus we get the coordinates of the **second point as  $(I_{DSS} \cdot R_S/2 : I_{DSS}/2)$** .

These two points are plotted on the  $I_D : V_{GS}$  plane and joined as a straight line. This is the plot of the Bias Line described by Eq. 3. This line is the locus of all the possible values the current  $I_D$  can take in terms of the equivalent circuit of Fig.-10. On the other hand, the transfer characteristic describes all the possible values of current  $I_D$  that can flow through the JFET. Thus, the point of intersection 'Q', of these two plots represents the point at which the JFET is biased. In other words, the point 'Q' is the operating point of the Self Bias circuit. The coordinates of the operating point are  $(V_{GSQ} : I_{DQ})$ .

DC LOAD LINE :- The KVL equation of the Drain-Source loop of

the Self Bias circuit of Fig.- 10 is given by

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S = V_{DS} + I_D \cdot (R_S + R_D)$$

$$\therefore V_{DD} - V_{DS} = I_D (R_D + R_S)$$

$$\therefore I_D = \frac{V_{DD}}{(R_S + R_D)} - \frac{V_{DS}}{(R_S + R_D)} \quad \dots(4)$$

This equation describes all the possible values of the current  $I_D$  that can flow through the DC load resistance  $(R_D + R_S)$ . This is a first order equation of the variable  $I_D$  as a function of  $V_{DS}$ , thus the plot of this equation is a straight line on the Cartesian plane of  $I_D$  and  $V_{DS}$ . Hence it is called the **DC Load Line**. This line is plotted over the Drain Characteristic of the JFET. This line has the following properties –

- The slope of the DC Load line is negative and given by the second term of the Eq. 4 as  $[-1/(R_S + R_D)]$ .
- The Vertical Intercept is obtained by substituting  $V_{DS} = 0$  in Eq. 4. Thus, it is given by

$$I_D = I_{D(OHMIC)} = \frac{V_{DD}}{(R_S + R_D)} \quad \dots(5)$$

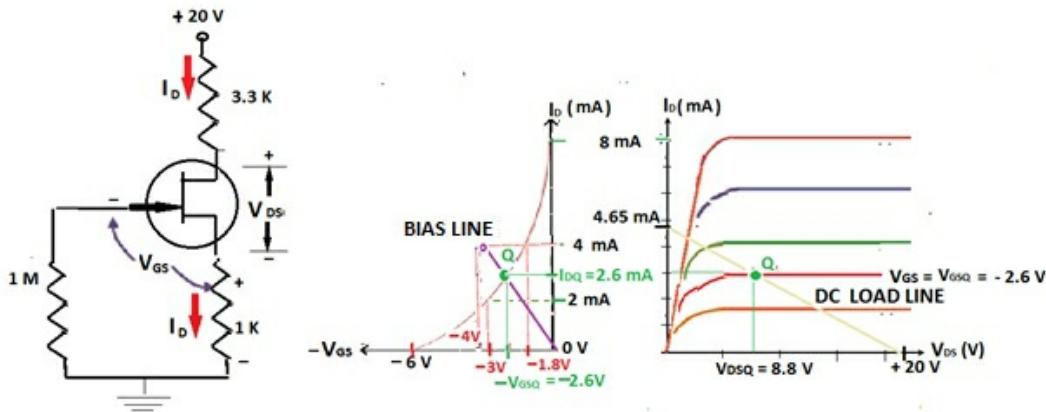
- The Horizontal Intercept is obtained by substituting  $I_D = 0$  in Eq. 6.4. This is a point in the Cut-Off region, and is given by

$$V_{DS(CUT-OFF)} = V_{DD} \quad \dots(6)$$

Since the DC Load Line is a straight line, it requires just two points to plot this line. These two points can be conveniently chosen as the Vertical Intercept and the Horizontal Intercept. Thus, by joining the Vertical Intercept given by Eq.6.5 and the Horizontal Intercept given by Eq.6, we get the DC Load Line. The point of intersection of the DC Load Line with the plot of the Drain Characteristic corresponding to the value of  $V_{GS} = V_{GSQ}$  has a Y-Coordinate exactly equal to  $I_{DQ}$  (which was obtained as the point of intersection of the Bias Line and the Transfer Characteristic). Thus, this point is nothing but the Operating point Q in terms of the Drain Characteristics. The X-Coordinate of this point is  $V_{DSQ}$ .

## TUTORIAL-2

**Example 2.: – Locate the Q Point of the Self Bias circuit in the figure and plot the DC Load Line. The parameters of the JFET are  $I_{DSS} = 8 \text{ mA}$  and  $V_P = 6 \text{ V}$**



### SOLUTION :-

#### (A) Transfer Characteristic and Q-Point

**The Transfer Characteristics** can be approximately plotted by using the Shockley's Equation as follows-

Shockley's equation given by Eq. 2 is

$$I_D = I_{DSS} \left\{ 1 - \frac{V_{GS}}{V_P} \right\}^2$$

Given  $I_{DSS} = 8 \text{ mA}$  &  $V_P = 6 \text{ V}$ , Thus we have the following points .

- (i) At  $V_{GS} = 0$ ;  $I_D = I_{DSS} = 8 \text{ mA}$ . Therefore coordinates of the point is **(0 V: 8 mA)**
- (ii) At  $V_{GS} = -0.3 V_P = -0.3 \times 6 = -1.8 \text{ V}$ ;  $I_D = I_{DSS} / 2 = 4 \text{ mA}$ . Therefore coordinates of the point is **(-1.8V: 4 mA)**.
- (iii) At  $V_{GS} = -0.5 V_P = -0.5 \times 6 = -3 \text{ V}$ ;  $I_D = I_{DSS} / 4 = 2 \text{ mA}$ . Therefore coordinates of the point is **(-3 V: 2 mA)**.
- (iv) At  $V_{GS} = -V_P = -6 \text{ V}$ ;  $I_D = 0$ . Therefore coordinates of the point is **(-6 V: 0 mA)**.

Plotting these points on the second quadrant of the Cartesian plane on a graph paper and joining them, we get the Transfer Characteristic of the JFET.

As discussed earlier, the **Bias Line** described by the Eq. 3, is a

straight line **starting at the origin** and extending up to the point whose coordinates are  $((- I_{DSS} \cdot R_S / 2) : (I_{DSS} / 2))$ .

Given  $R_S = 1 \text{ K}$  &  $I_{DSS} = 8 \text{ mA}$ . Thus  $- I_{DSS} \cdot R_S / 2 = - 4 \text{ V}$  &  $I_{DSS} / 2 = 4 \text{ mA}$ . Thus the coordinates of the point are  $(- 4 \text{ V} : 4 \text{ mA})$ .

Joining this point with the origin we get the plot of the Bias Line.

**The Q-Point is the point of intersection of the Transfer Characteristic and the Bias Line.** Thus, the coordinates of the Q-Point, which is obtained from a graph are the following

$$V_{GSQ} = - 2.6 \text{ V} \quad \& \quad I_{DQ} = 2.6 \text{ mA.}$$

(B) DC Load Line and Q-Point

The DC Load Line is described by the Eq. 4. This is a straight line on the first quadrant of the Cartesian Plane. For plotting the DC Load Line, the Vertical Intercept and Horizontal intercept are given in Eq. 5 & Eq. 6 respectively. Using these equations, we have

(i) Vertical intercept given by Eq. 5 is

$$\begin{aligned} I_{D(OHMIC)} &= \frac{V_{DD}}{(R_S + R_D)} \\ &= \frac{20 \text{ V}}{(3.3 + 1) \text{ K}} \end{aligned}$$

$$I_{D(OHMIC)} = 4.65 \text{ mA.}$$

(ii) Horizontal Intercept is  $V_{DS}(\text{CUT-OFF}) = V_{DD} = 20 \text{ V}$ .

Joining these two points on the graph paper we get the plot of the DC Load Line. The Load Line intersects the Drain Characteristic graph corresponding to the  $V_{GSQ} = - 2.6 \text{ V}$  at the point Q. The coordinates of this point are as follows-

$$V_{DSQ} = 8.8 \text{ V} \quad \& \quad I_{DQ} = 2.6 \text{ mA.}$$

**VERIFICATION :-** Rearranging Eq. 4 and substituting  $I_D = I_{DQ} = 2.6 \text{ mA}$  we get

$$\begin{aligned} V_{DSQ} &= V_{DD} - I_{DQ} (R_S + R_D) \\ &= 20 - 2.6 \times 10^{-3} \cdot (3.3 + 1) \times 10^3 \end{aligned}$$

$$V_{DSQ} = 8.82 \text{ V}$$

### **Voltage Divider Bias Circuit**

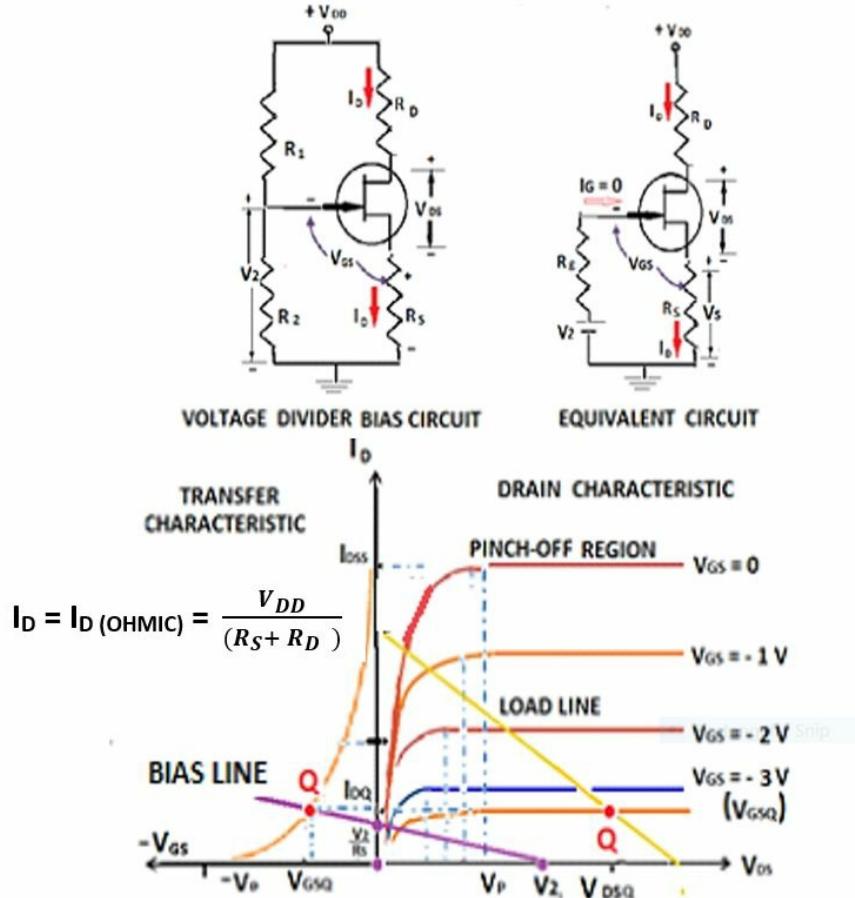
Readers are to recall that we encountered the Voltage Divider Bias

circuit in connection with the BJT, wherein this circuit was also termed as an Universal Bias Circuit. The qualifier ‘Universal’ stands for the fact that this circuit is applicable to all types of amplifiers, which include all types of FETs also. The circuit in Fig.-11 shows a Voltage Divider Bias Circuit for a JFET amplifier. The working principle and the steps of analysis are as follows.

#### WORKING PRINCIPLE :-

The two resistances  $R_1$  and  $R_2$  form a Voltage Divider network and impart a voltage  $V_2$  across the resistance  $R_2$ . This voltage and the equivalent resistance  $R_g$  represent the Thevenin’s equivalent at the Gate terminal. The circuit should be so designed such that the magnitude of the voltage  $V_2$  should be less than the voltage  $V_S$  across the resistance  $R_s$ . Now, since the Gate Current  $I_G$  is zero in a JFET, there is no voltage drop across  $R_g$ . Thus, since  $|V_2| < |V_S|$ , the potential difference  $V_{GS}$  is positive at the Source terminal and less positive (i.e., relatively negative) at the Gate terminal. Therefore Gate is reverse biased, which is the requirement for a JFET. Due to the bias potential  $V_{DD}$  a current  $I_D$  flows in the Drain-Source circuit. This current produces the voltage drop of  $V_S$  of the required magnitude, across the resistance  $R_S$ . The circuit design must also be such that the voltage drop across the two resistances  $R_D$  and  $R_S$  must leave enough potential difference  $V_{DS}$  between the Drain

and the Source terminals so that  $V_{DS} \geq V_p$ . In fact,  $V_{DS}$  must be significantly greater than  $V_p$ . Thus the JFET gets the required bias to be operating in the Pinch-Off region of its characteristic.



**Fig. 11:** - The Voltage Divider Bias Circuit of JFET, the DC Load Line and the Operating Point.

**ANALYSIS :-** In the voltage Divider network, the voltage across  $R_2$  is given by

$$V_2 = \frac{R_2 \cdot V_{DD}}{(R_1 + R_2)} \quad \dots(7)$$

The Gate circuit is Thevenized and we obtain the Equivalent circuit in the figure. The voltage  $V_2$  is the Thevenin's Equivalent voltage at the Gate-Source loop. The Thevenin's Equivalent resistance  $R_g$  is the parallel combination of  $R_1$  and  $R_2$  given by

$$R_g = \frac{R_1 \cdot R_2}{(R_1 + R_2)} \quad \dots(8)$$

Assuming  $I_G = 0$  in the equivalent circuit, we have the KVL equation of the Gate-Source loop as

$$V_2 = V_{GS} + I_D R_S$$

$$\therefore V_{GS} = V_2 - I_D R_S \dots(9)$$

This is the expression for the Bias Line. This is an equation of a straight line, and this line is to be plotted on the second quadrant since  $V_{GS}$  is a negative quantity for an N-channel JFET. In order to plot this line we need two points. Conveniently these two points can be taken as the Horizontal Intercept and the Vertical Intercept.

- Substituting  $I_D = 0$  in Eq. 9 we get the Horizontal intercept as

$$V_{GS} = V_2.$$

- Substituting  $V_{GS} = 0$  in Eq. 9 we get the Vertical intercept as

$$I_D = V_2/R_S.$$

Plotting these points on the Cartesian plane and joining them with a straight line we get the plot of the Bias Line (Eq. 9). This intersects the Transfer Characteristics of the JFET at the point Q. This is the Operating Point. The coordinates of the Q-Point are  $V_{GSQ}$  and  $I_{DQ}$ .

DC LOAD LINE EQUATION is obtained from the KVL equation of the Drain-Source circuit. The equation is

$$\begin{aligned} V_{DD} &= I_D R_D + V_{DS} + I_D R_S \\ &= V_{DS} + I_D (R_D + R_S) \end{aligned}$$

Rearranging we have the expression of the DC Load Current  $I_D$  as a function of the Drain-Source bias  $V_{DS}$  as

$$I_D = \frac{V_{DD}}{(R_S + R_D)} - \frac{V_{DS}}{(R_S + R_D)} \dots(10)$$

This equation describes all the possible values of the current  $I_D$  that can flow through the DC load resistance ( $R_D + R_S$ ). This is a first order equation of the variable  $I_D$  as a function of  $V_{DS}$ , thus the plot of this equation is a straight line on the Cartesian plane of  $I_D$  and  $V_{DS}$ . Hence it is called the DC Load Line. This line is plotted over the Drain Characteristic of the JFET. This line has the following properties –

- The slope of the DC Load line is negative and given by the second term of the Eq. 4 as  $[-1/(R_S + R_D)]$ .
- The Vertical Intercept is obtained by substituting  $V_{DS} = 0$  in Eq. 4. Thus, it is given by Eq. 4 as

$$I_D = I_{D(\text{OHMIC})} = \frac{V_{DD}}{(R_S + R_D)} \quad \dots(11)$$

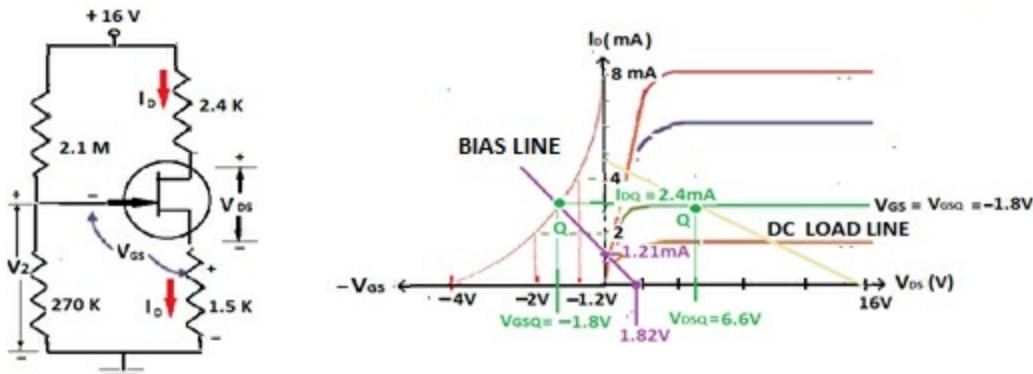
- The Horizontal Intercept is obtained by substituting  $I_D = 0$  in Eq. 6.4. This is a point in the Cut-Off region, and is given by

$$V_{DS(\text{CUT-OFF})} = V_{DD} \quad \dots(12)$$

Since the DC Load Line is a straight line, it requires just two points to plot this line. These two points can be conveniently chosen as the Vertical Intercept and the Horizontal Intercept. Thus by joining the Vertical Intercept given by Eq. 5 and the Horizontal Intercept given by Eq. 6.6, we get the DC Load Line. The point of intersection of the DC Load Line with the plot of the Drain Characteristic corresponding to the value of  $V_{GS} = V_{GSQ}$  has a Y-Coordinate exactly equal to  $I_{DQ}$ . Thus this point is nothing but the Operating point Q in terms of the Drain Characteristics. The X-Coordinate of this point is  $V_{DSQ}$ .

### TUTORIAL-3

**Example 3.:** – Locate the Q Point of the Voltage Divider Bias circuit in the figure and plot the DC Load Line. The parameters of the JFET are  $I_{DSS} = 8 \text{ mA}$  and  $V_P = 4 \text{ V}$



**SOLUTION :-** The Transfer Characteristics can be approximately plotted by using the Shockley's Equation as follows- Shockley's equation given by Eq. 6.2 is

$$I_D = I_{DSS} \left\{ 1 - \frac{V_{GS}}{V_P} \right\}^2$$

Given  $I_{DSS} = 8 \text{ mA}$  &  $V_P = 6 \text{ V}$ , Thus we have the following points .

- (i) At  $V_{GS} = 0$  ;  $I_D = I_{DSS} = 8 \text{ mA}$ . Therefore coordinates of the point is (**0 V: 8 mA**)
- (ii) At  $V_{GS} = -0.3 \text{ V}$  ;  $I_D = I_{DSS} / 2 = 4 \text{ mA}$ . Therefore, coordinates of the point is (**-1.2V: 4 mA**).
- (iii) At  $V_{GS} = -0.5 \text{ V}$  ;  $I_D = I_{DSS} / 4 = 2 \text{ mA}$ . Therefore coordinates of the point is (**-2 V: 2 mA**).
- (iv) At  $V_{GS} = -V_P = -4 \text{ V}$  ;  $I_D = 0$ . Therefore coordinates of the point is (**-4 V: 0 mA**).

Plotting these points on the second quadrant of the Cartesian plane on a graph paper and joining them, we get the Transfer Characteristic of the JFET.

For plotting the Bias Line given by Eq. 9 we have to calculate the Horizontal Intercept and the Vertical Intercept from Eq. 7 and Eq. 8.

Horizontal Intercept is  $V_2$ , given by

$$V_2 = \frac{R_2 \cdot V_{DD}}{(R_1 + R_2)} = \frac{270 \times 10^3 \times 16}{(2.1 \times 10^6 + 270 \times 10^3)}$$

$$V_2 = 1.82 \text{ V}$$

Vertical Intercept is  $I_D$ , given by

$$I_{D(OHMIC)} = V_2 / R_S = \frac{1.82}{1.5 \times 10^3} = 1.21 \times 10^{-3}$$

$$I_{D(OHMIC)} = 1.21 \text{ mA}$$

Joining these two points with a straight line we get the plot of the Bias Line (Eq. 9). The Q-Point is the point of intersection of the Transfer Characteristic and the plot of the Eq. 9. Thus, the coordinates of the Q-Point, which is obtained from a graph are the following

$$V_{GSQ} = -1.8 \text{ V} \quad \& \quad I_{DQ} = 2.4 \text{ mA}$$

(B) DC Load Line and Q-Point

The DC Load Line is described by the Eq. 6.10. This is a straight

line on the first quadrant of the Cartesian plane. For plotting the DC Load Line the Vertical Intercept and Horizontal intercept are given in Eq. 11 & Eq. 12 respectively. Using these equations we have

(i) Vertical intercept given by Eq. 11 is

$$I_{D(OHMIC)} = \frac{V_{DD}}{(R_S + R_D)}$$

$$= \frac{20 V}{(3.3 + 1) K}$$

$$I_{D(OHMIC)} = 4.65 \text{ mA.}$$

(ii) Horizontal Intercept given by Eq. 12 is

$$V_{DS(CUT-OFF)} = V_{DD} = 16 \text{ V.}$$

Joining these two points on the graph paper we get the plot of the DC Load Line. The Load Line intersects the Drain Characteristic graph corresponding to the  $V_{GSQ} = -1.8 \text{ V}$  at the point Q. The coordinates of this point are as follows-

$$V_{DSQ} = 6.6 \text{ V} \quad \& \quad I_{DQ} = 2.4 \text{ mA.}$$

**VERIFICATION :-** Rearranging Eq. 10 and substituting  $I_D = I_{DQ} = 2.4 \text{ mA}$  we get

$$V_{DSQ} = V_{DD} - I_{DQ} (R_S + R_D)$$

$$= 16 - 2.4 \times 10^{-3} \times (2.4 + 1.5) \times 10^3 = 6.64 \text{ V.}$$

## 8.5 Small Signal JFET Amplifier

JFET is a transistor, which is primarily designed to function as an amplifier. Recall that we analyzed Small Signal Amplifiers based on BJTs. In order to analyze these, we used a Small Signal Model, such as the r-parameter Model or the h-parameter Model. In order to analyze the performance of JFET amplifier too we need a Model. The commonly used JFET Model is the ‘Trans-Conductance Model’.

### Small Signal Trans-Conductance Model of JFET

- A JFET will work as an amplifier when it is biased in the Pinch-Off Region of its characteristics.

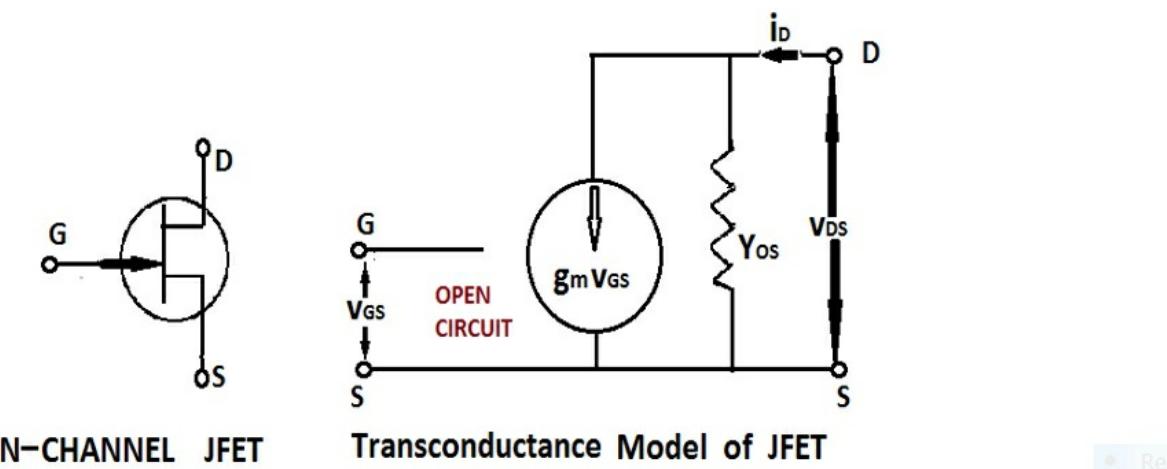
- In order to bias an N-Channel JFET in the Pinch-Off Region, the potential  $V_{DS}$  to be applied between the Drain and the Source terminals must be positive and the potential  $V_{GS}$  between the Gate and the Source terminal must be negative.
- In the N-Channel JFET, the gate region is P-Type. Hence a negative potential at this terminal will reverse bias the Gate region. In general, a reverse biased P-N Junction is represented by an Open Circuit, thus the gate terminal will be represented as an open circuit in our model.
- The Drain Current  $I_D$  saturates at a constant value for a given magnitude of  $|V_{GS}|$ , but, for a different magnitude of  $|V_{GS}|$ , the current  $I_D$  saturates at a different level. In other words,  $I_D$  is controlled by the Gate potential  $V_{GS}$ . (In fact this is the reason why the JFET is classified as a ‘Voltage Controlled Device’). Hence, in our model, the current  $I_D$  in the Drain-Source circuit is represented by a Current Source ‘ $g_m v_{GS}$ ’. This appears in parallel with a resistance “ $r_D$ ”.
- The Transfer Characteristic graphs define the ‘Transconductance Parameter’  $g_m$  of the JFET (defined in section-1), which is obtained from the plot of the Transfer Characteristic as the slope of the graph. Thus

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{i_D}{v_{GS}}$$

The Transconductance Parameter is also given by an empirical formula as

$$| \quad g_m = \frac{2 I_{DSS}}{V_P} \left( 1 - \frac{V_{GS}}{V_P} \right) \quad \dots(13)$$

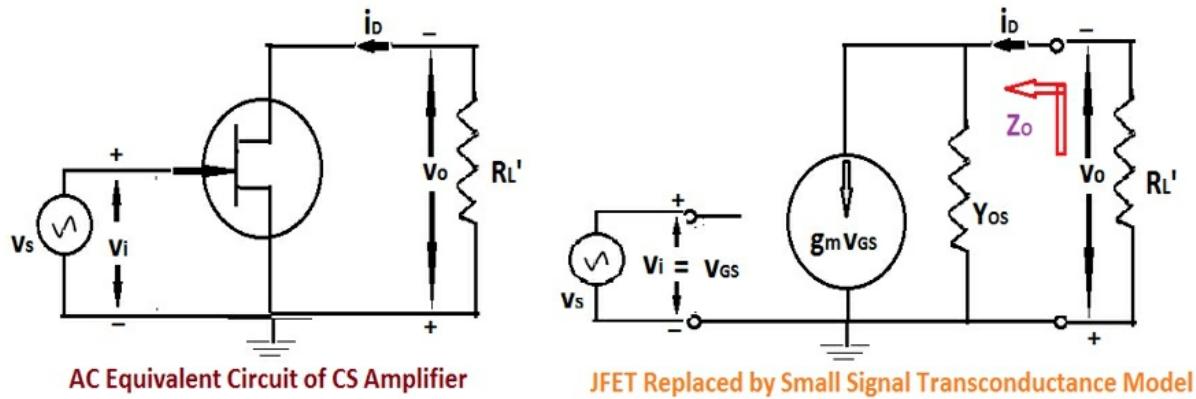
The Drain Current has been so far described as a constant value in the Pinch-Off region. But in practice, the graph of  $I_D$  as a function of  $V_{DS}$  does have a slight upward slope. This slope of the Drain Characteristic graph is due to the admittance parameter ‘ $Y_{OS}$ ’ (defined in the section -1). The resistance ‘ $r_D$ ’ in the model is the reciprocal of the admittance parameter ‘ $Y_{OS}$ ’.



**Fig. 12:** - The N-Channel JFET and its Small Signal Transconductance Model.

### AC ANALYSIS :-

Any amplifier is analyzed by replacing the JFET device with the Small Signal Model in the AC Equivalent circuit. This is shown for a JFET amplifier in the Common Source (CS) configuration in the Fig. 13 below.



**Fig. 13:** - AC Equivalent Circuit of Common Source JFET amplifier. The equivalent circuit formed by replacing the JFET with the Small Signal Transconductance Model of the device.

### Voltage Gain $A_V$

Voltage Gain of an amplifier is the ratio of the AC signal Output Voltage to the AC Input Voltage. Thus

$$A_V = \frac{v_o}{v_i}$$

Where, Input signal voltage  $v_i$  is the AC signal  $v_{GS}$  between the input terminal Gate and the common Source terminal.

$$v_i = v_{GS}$$

The Output Voltage  $v_o$  is the voltage developed across the Load Resistance  $R_L'$  due to the Output Current  $i_O$ . But the Output Current is in the direction opposite to the AC Drain Current  $i_D$ . Hence,

$$v_o = i_O R_L' = -i_D R_L'$$

Here, the AC Drain Current is the current driven by the current source in the Equivalent Circuit. Hence,

$$i_D = g_m v_{GS}$$

$$\therefore v_o = -g_m v_{GS} \cdot R_L'$$

Thus

$$A_V = -g_m R_L' \dots (14)$$

The Negative sign in this expression represents the fact that the Output Voltage and the Input Voltage are opposite in phase. The phase reversal of the output signal w.r.t. the input signal is shown in the Fig.13 as opposite signs at the respective terminals for the input voltage and the output Voltage.

### INPUT IMPEDANCE $Z_i$

The Input Impedance  $Z_i$  is the impedance of the amplifier looking into the Input terminal, i.e. the Gate terminal. The Gate terminal in JFET is at a reverse bias. Hence the Input impedance looking into the Gate tends to be infinity. However, since the JFET is connected via a biasing circuit, the input impedance  $Z_i$  will depend on the biasing circuit.

- In case of the Self Bias Circuit  $Z_i \approx R_G$ .
- In case of Voltage Divider Biasing Circuit  $Z_i$  is the parallel combination of the biasing resistances  $R_1$  and  $R_2$ , defined as  $R_g$  and expressed by the Eq. 8.

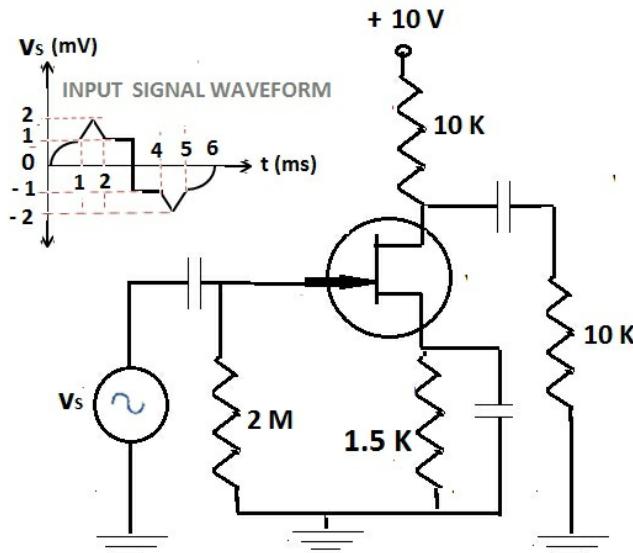
## OUTPUT IMPEDANCE $Z_O$

The Output Impedance is the impedance of the amplifier looking into the Output terminal. From the Small Signal Model given in Fig. 13, the impedance of the amplifier looking into the Output terminal is  $r_D$ , where  $r_D$  is the reciprocal of the JFET parameter 'Y<sub>OS</sub>'.

$$Z_O = 1/Y_{OS} = r_D \dots (15)$$

## TUTORIAL-4

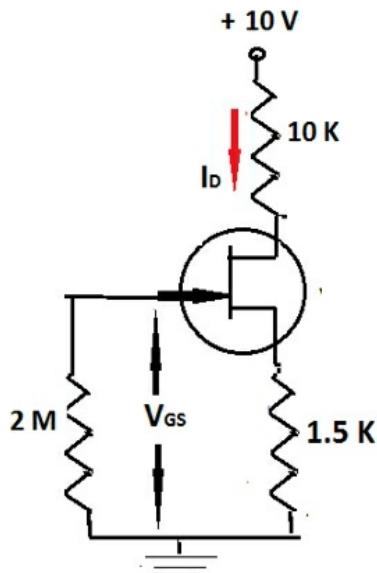
**Example 8.4.:** – Analyze the JFET amplifier circuit shown in the figure below and calculate  $A_V$ ,  $Z_i$  and  $Z_O$ . Sketch the output voltage waveform, the input signal waveform is as shown in the figure. The JFET in the amplifier circuit has the following parameters ,  $I_{DSS} = 15$  mA ;  $V_P = 3.5$  V and  $Y_{OS} = 35 \mu S$ .



## SOLUTION :-

### (A) Transfer Characteristic and Q-Point (DC Analysis)

**DC Equivalent Circuit :-** DC Equivalent Circuit is obtained by open circuiting all capacitors and neglecting the AC signal source.



The Transfer Characteristics can be approximately plotted by using the Shockley's Equation for JFET, (given by Eq. 6.2) as follows-

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

Using the given parameters of the JFET

$$I_{DSS} = 15 \text{ mA} \quad \& \quad V_P = 3.5 \text{ V}$$

Substituting these numerical values in the Shockley's equation we can have a pot of the following points on a graph paper .

- (i) At  $V_{GS} = 0$  ;  $I_D = I_{DSS} = 15 \text{ mA}$ . Therefore coordinates of the point is **( 0 V: 8 mA)**
- (ii) At  $V_{GS} = - 0.3 \text{ V}$   $V_P = - 0.3 \times 3.5 = - 1.05 \text{ V}$  ;  $I_D = I_{DSS} / 2 = 7.5 \text{ mA}$ . Therefore coordinates of the point is **(- 1.05V: 7.5 mA)**.
- (iii) At  $V_{GS} = - 0.5 \text{ V}$   $V_P = - 0.5 \times 3.5 = - 1.75 \text{ V}$  ;  $I_D = I_{DSS} / 4 = 3.75 \text{ mA}$ . Therefore coordinates of the point is **(- 1.75 V: 3.75 mA)**.
- (iv) At  $V_{GS} = - V_P = - 3.5 \text{ V}$  ;  $I_D = 0$ . Therefore coordinates of the point is **(- 3.5 V: 0 mA)**.

Plotting these points on the second quadrant of the Cartesian plane on a graph paper and joining them, we get an approximate plot the Transfer Characteristic of the JFET.

The Bias Line given by Eq. 3 gives the relationship between  $I_D$  and  $V_{GS}$  in the DC Equivalent circuit. The equation is reproduced below, from this we see that this is the equation of a straight line.

$$I_D = \frac{-V_{GS}}{R_S}$$

The locus of a straight line can be plotted by substituting numerical values of the coordinates of any two points.

1. **If we let  $I_D = 0$ , we get  $V_{GS} = 0$ .**

Thus the first point is the origin(**0 : 0**).

- ii. If we let  $I_D = \frac{I_{DSS}}{4}$ , rearrange and substitute the numerical values in the expressions we get

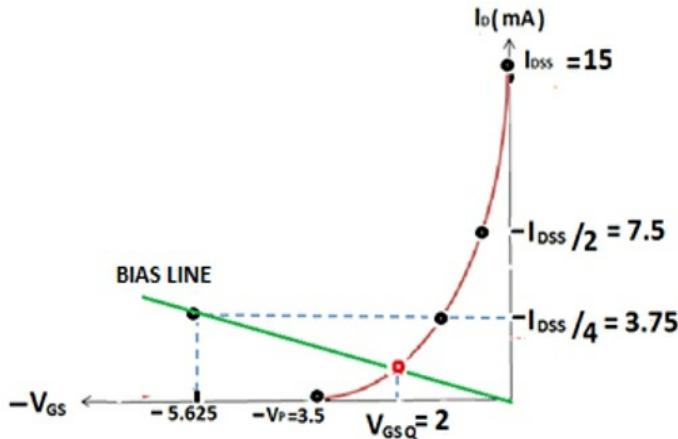
$$V_{GS} = \frac{-I_{DSS} \cdot R_S}{4} = \frac{-15 \times 1.5}{4}$$

$$V_{GS} = 5.625 \text{ V}$$

$$I_D = \frac{I_{DSS}}{4} \quad \therefore \quad I_D = \frac{15}{4} = 3.75 \text{ mA}$$

Thus the coordinates of the second point are (**-5.625 V : 3.75 mA**)

Joining this point with the origin we get the plot of the Bias Line (Eq. 3).

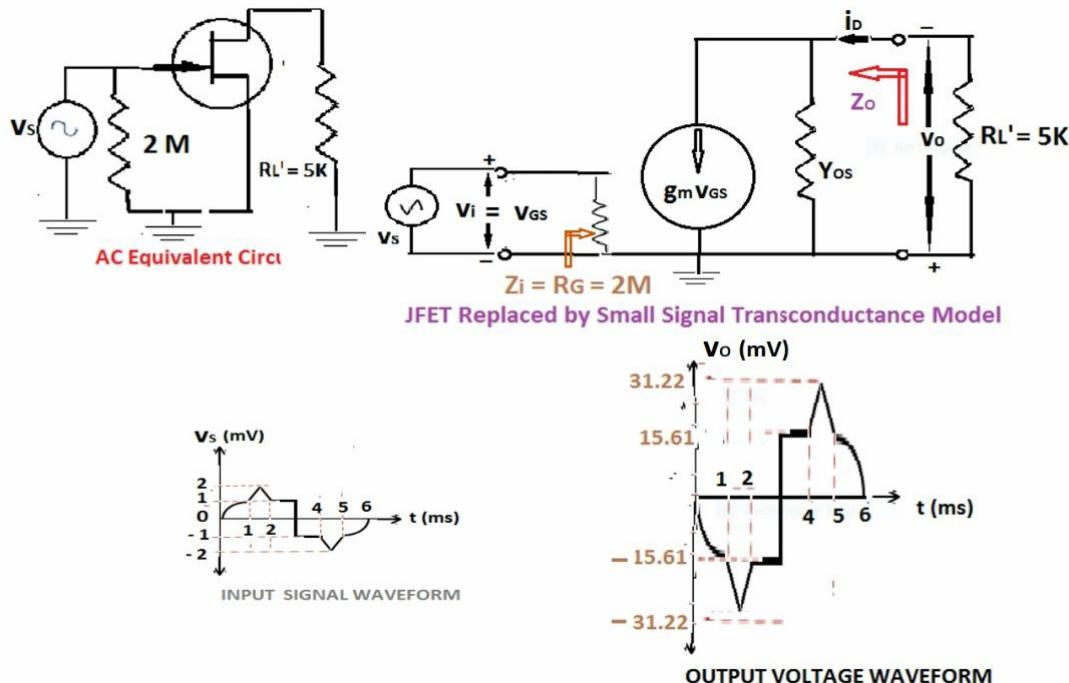


The Q-Point is the point of intersection of the Transfer Characteristic and the Bias Line. Thus, from the graph

$$V_{GSQ} = 2 \text{ V.}$$

## AC Analysis

AC Equivalent Circuit :- AC Equivalent Circuit is obtained by short circuiting all capacitors and neglecting the DC biasing source.



AC Analysis provides us the quantity Voltage Gain in the form of Eq. 6.14 as shown earlier and reproduced below as

$$A_V = -g_m R_D'$$

Where  $g_m$  is the Transconductance Parameter of the JFET and it is given by Eq. 13. Substituting the numerical values of the parameters of the given JFET and using the value of  $V_{GSQ}$  as obtained from DC Analysis in the expression we get the numerical value of  $g_m$  as follows

$$g_m = \frac{2 I_{DSS}}{V_P} \left( 1 - \frac{V_{GS}}{V_P} \right)$$

$$\therefore g_m = \frac{2 \times 15}{3.5} \left( 1 - \frac{2}{3.5} \right) = 3.67 \text{ mS}$$

Here  $R_D'$  is the AC Load resistance of the amplifier, which is the parallel combination of the JFET Parameter  $r_D'$  and the net Load Resistance  $R_L'$ .

Substituting the expression for  $r_D$  from Eq.15 and using the numerical value of the  $Y_{OS}$  Parameter of the given JFET as  $Y_{OS} = 35 \mu\text{S}$

we have

$$r_D = 1/Y_{OS} = 1/35 \times 10^{-6} = 28571 \Omega = 28.57 K$$

From the given circuit the net Load Resistance  $R_L'$  of the amplifier is  
 $R_L' = 10 K \parallel 10 K = 5 K$

$$\therefore R_{D'} = R_L' \parallel r_D = \frac{5 \times 28.57}{5 + 28.57} = 4.255 K$$

Substituting the calculated numerical values of  $g_m$  and  $R_D'$  in the expression of Voltage Gain we have

$$A_V = -g_m R_D'$$

$$A_V = -3.67 \times 10^{-3} \times 4.255 \times 10^3 = -15.61$$

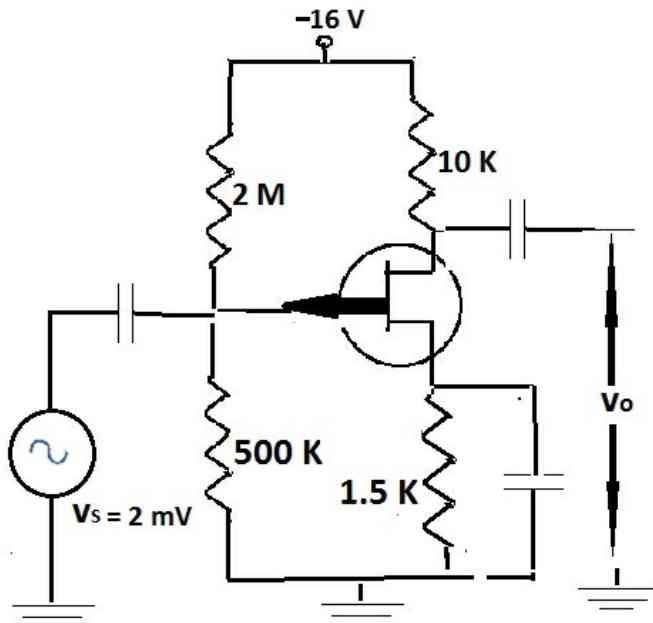
The negative sign implies that The Output Voltage Waveform is INVERTED, i.e., the output waveform is at a phase shift of  $180^\circ$  w.r.t. the Input Signal. (This is the same situation that occurs in case of a single stage BJT amplifier also ).

From Eq. 15 we have

$$Z_O = r_D = 28.57 K.$$

### TUTORIAL-5

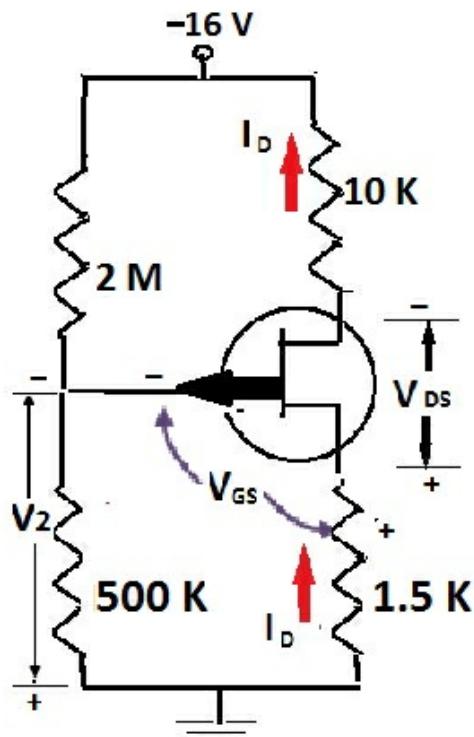
**Example 5.:** – Analyze the P-Channel JFET amplifier circuit shown in the figure below and calculate  $A_V$ ,  $Z_i$  and  $Z_O$ . Calculate the output voltage and the output power. The JFET in the amplifier circuit has the following parameters,  $I_{DSS} = 10 mA$ ;  $V_P = 5 V$  and  $Y_{OS} = 25 \mu S$ .



## SOLUTION :-

(A) Transfer Characteristic and Q-Point Analysis) (DC Analysis)

DC Equivalent Circuit :- DC Equivalent Circuit is obtained by open circuiting all capacitors and neglecting the AC signal source. The steps of analysis for the N-Channel JFET as well as the P-Channel JFET are exactly the same.



The Transfer Characteristics can be approximately plotted by using the Shockley's Equation with the steps as follows-

Shockley's equation given by Eq. 2 is

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

Given

$$I_{DSS} = 10 \text{ mA} \quad \& \quad V_P = 5 \text{ V}$$

Substituting these numerical values in the Shockley's equation we can have a plot of the following points on the third quadrant of a graph paper. Joining these points gives an approximation of the Transfer Characteristics of the JFET.

- (i) At  $V_{GS} = 0$  ;  $I_D = I_{DSS} = 10 \text{ mA}$ . Therefore coordinates of the point is (**0 V: 10 mA**)

- (ii) At  $V_{GS} = -0.3$  V  $V_P = -0.3 \times 5 = -1.5$  V ;  $I_D = I_{DSS}$   
 $/2 = 5$  mA. Therefore coordinates of the point is (- 1.5 V: 5 mA).
- (iii) At  $V_{GS} = -0.5$  V  $V_P = -0.5 \times 5 = -2.5$  V ;  $I_D = I_{DSS}/4$   
 $= 2.5$  mA. Therefore, coordinates of the point is (- 2.5 V: 2.5 mA).
- (iv) At  $V_{GS} = -V_P = -5$  V ;  $I_D = 0$ . Therefore coordinates of the point is (- 5 V: 0 mA).

For plotting the Bias Line the expression to be used is given by Eq.  
 9. From this we have to calculate the Horizontal Intercept and the Vertical Intercept from Eq. 7 and Eq. 8.

Horizontal Intercept is  $V_2$ , given by

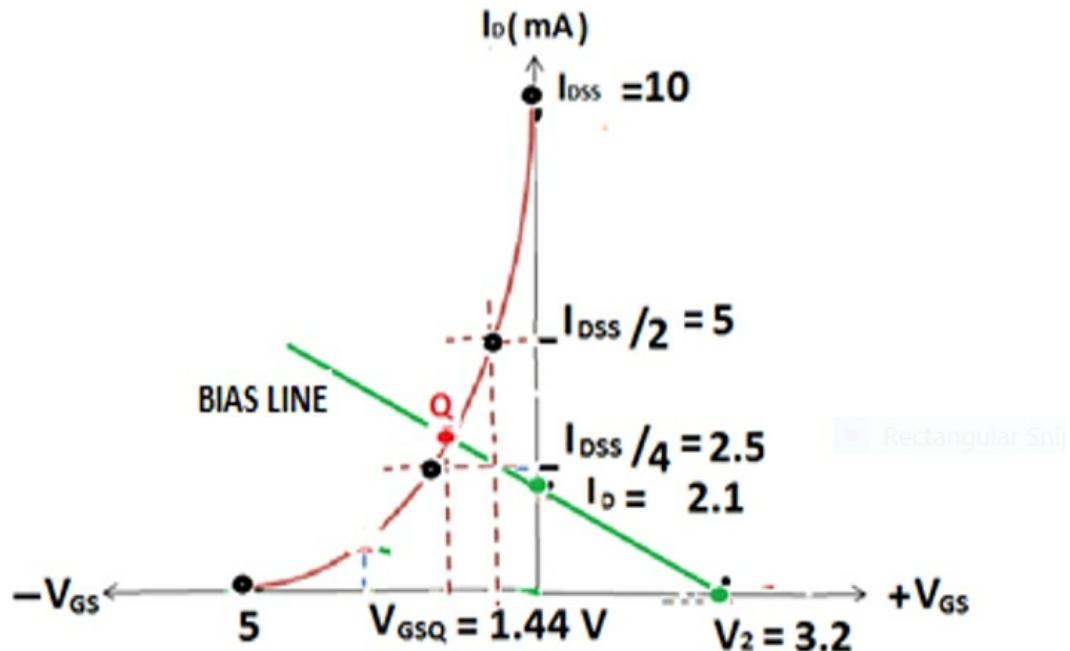
$$V_2 = \frac{R_2 \cdot V_{DD}}{(R_1 + R_2)} \\ = \frac{500 \times 10^3 \times 16}{(2 \times 10^6 + 500 \times 10^3)} = 3.2 \text{ V}$$

Vertical Intercept is  $I_D$ , given by

$$I_D = V_2 / R_S = \frac{3.2}{1.5 \times 10^3} = 2.1 \times 10^{-3} = 2.1 \text{ mA}$$

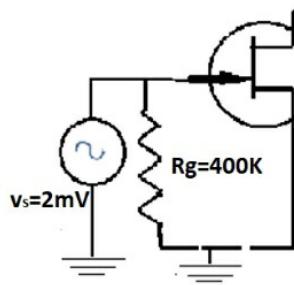
Joining these two points with a straight line we get the plot of the Bias Line. The Q-Point is the point of intersection of the Transfer Characteristic and the Bias Line. The x- coordinate of the Q-Point is

$$V_{GSQ} = 1.44 \text{ V}$$

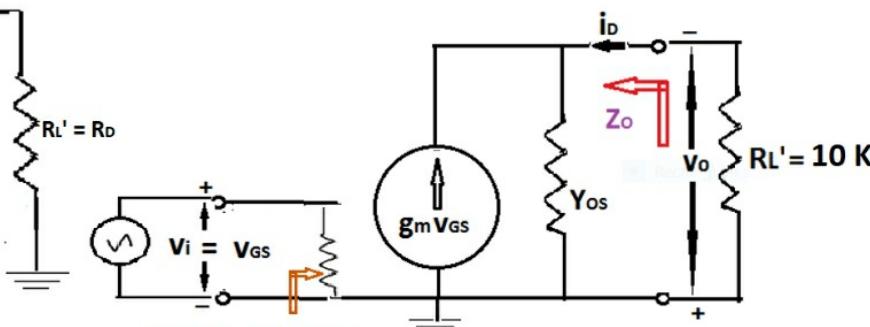


### AC Analysis

AC Equivalent Circuit :- AC Equivalent Circuit is obtained by short circuiting all capacitors and neglecting the DC biasing source. The JFET is replaced by the small signal Transconductance model. The formulae for the quantities are the same as those used for N-Channel JFET.



AC Equivalent Circuit



JFET Replaced by Small Signal Transconductance Model

Form of Eq. 14

$$A_V = - g_m R_D'$$

Where  $g_m$  is the Transconductance Parameter of the JFET and it is given by Eq. 13. Substituting the numerical values of the various quantities in the expression,

$$\underline{g_m} = \frac{2 I_{DSS}}{V_P} \left( 1 - \frac{V_{GS}}{V_P} \right)$$

$$\therefore g_m = \frac{2 \times 10}{5} \left( 1 - \frac{1.44}{5} \right) = 2.85 \text{ mS}$$

Since there is no external load resistance, the AC resistance at the output drain Terminal is  $\underline{R_L}' = R_D = 10 \text{ K}$

$$r_D = 1/Y_{os} = 1/25 \times 10^{-6} = 40000 \Omega = 40 \text{ K}$$

The Net Resistance at the output terminal is the parallel combination of  $R_L'$  and  $r_D$

Hence

$$\therefore R_{D'} = R_L' || r_D = \frac{10 \times 40}{10 + 40} = 8 \text{ K}$$

Thus

$$A_V = -g_m R_D'$$

$$A_V = -2.85 \times 10^{-3} \times 8 \times 10^3 = -22.8$$

And

$$Z_O = r_D = 40 \text{ K.}$$

Again

$$|v_o| \approx |A_V| v_s$$

( Since source resistance  $R_S$  has been neglected )

Or

$$v_o = 22.8 \times 2 = 45.6 \text{ mV (rms)}$$

$$\therefore P_o = \frac{v_o^2}{R_L'} = \frac{(45.6 \times 10^{-3})^2}{10 \times 10^{-3}}$$

$$= 2.07 \times 10^{-7} \text{ W.}$$

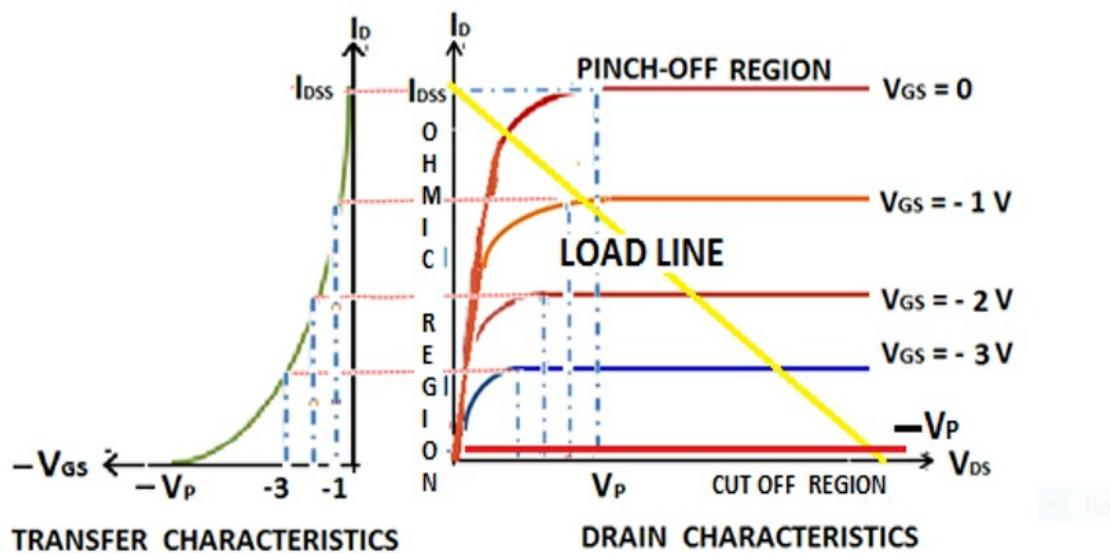
## 8.6 FET Switch

In the Chapter VII, we studied the application of the BJT as an electronic switch. The JFETs and MOSFETs can also be configured as switches as discussed below. In fact, the FET switches are more efficient than the BJT switch. This is because of

the fact that the switching operation from On State to Off State in a BJT is rather slow. The time delay in the process can be as much as a few hundred nano seconds. Whereas in case of FET switches, the switching operation is almost instantaneous. Therefore the FET switch is preferred over BJT switch.

### JFET Switch

Recall that a Closed Switch in an electrical circuit is a Short Circuit and an Open Switch is an Open Circuit between two terminals of that circuit. In a Short Circuit, the voltage across the terminals is zero and in an Open Circuit the current between the terminals is zero. Recall the V-I Characteristic of a N-Channel JFET, reproduced below for convenience.

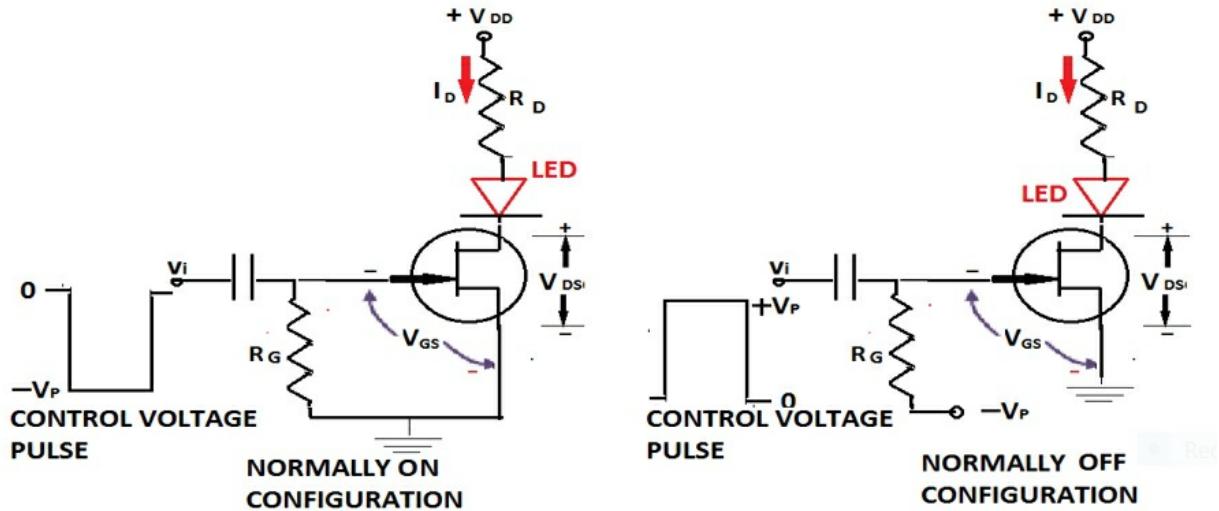


**Fig. 14: - The V-I Characteristics of a N-Channel JFET**

A JFET is a Voltage Controlled Device, that is, the output current is controlled by the input voltage. This relationship is expressed by means of the Transfer Characteristics. On the other hand, the Drain Characteristics and the Load Line express how the output current changes with respect to the output voltage. Referring to the Transfer Characteristics, when the input voltage  $V_{GS}$  equals  $-V_P$ , the output current  $I_D$  becomes zero. Again, when the input voltage is zero, the output current attains the highest possible value  $I_{DSS}$ .

Referring this on to the Load Line and the Drain Characteristics, the voltage  $V_{DS}$  between the output terminal (Drain) and the common

terminal (Source) is maximum when the control voltage  $V_{GS}$  equals  $-V_p$ , whereas the Output Current  $I_D$  is negligible. This situation refers to the Cut Off region of the characteristic and the JFET is behaving as an Open Switch. On the other hand, when the control voltage  $V_{GS}$  equals zero, the Output Current  $I_D$  is maximum and the voltage  $V_{DS}$  between the D and S terminals is zero. This situation refers to the Ohmic region of the characteristic and the JFET is behaving as a Closed Switch. Thus, by applying zero voltage to the Gate the device can be operated as a Closed Switch and by driving the Gate terminal by means of a Negative pulse, the device can be operated as an Open Switch. On the basis of this, we can have two configurations of a JFET switch as described below.



**Fig. 15: - The two configurations of N-Channel JFET switch.**

**Normally On Configuration:** - Refer to the circuit for the Normally On Configuration. When the control signal is at 0 V level, the Gate-Source voltage applied to the device is  $V_{GS} = 0$ . Thus, the JFET will be operating at the top of the Transfer Characteristic as well as the top of the load line, where the Load Current  $I_D = I_{DSS}$  and  $V_{DS} = 0$ . Thus, there is a short circuit between the Drain and Source terminals, in other words, the JFET is acting as a Closed Switch. In this case the Load (LED) is at the ON state. Next, when a negative going Control Voltage pulse is applied, the applied voltage at the Gate terminal is  $V_{GS} = -V_p$ . This will drive the

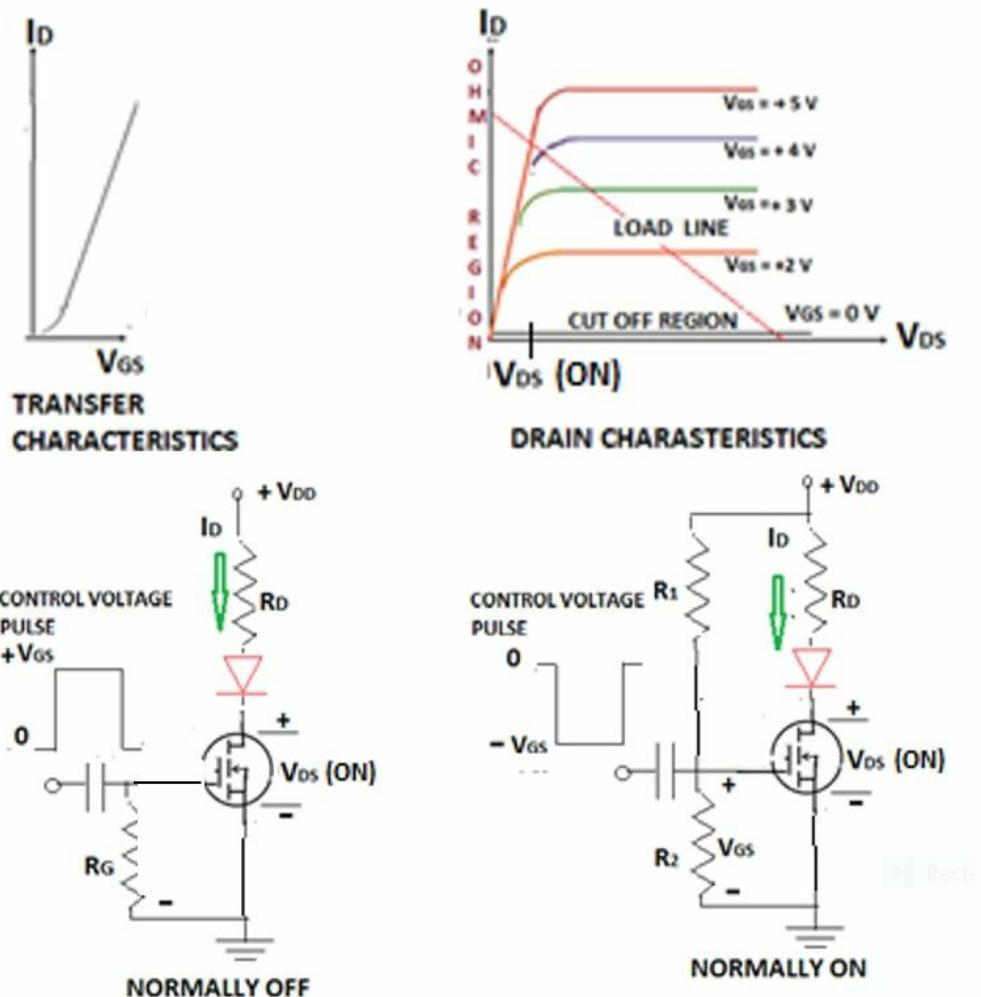
JFET to the bottom of the Transfer Characteristic as well as the bottom of the Load Line. Thus Load Current  $I_D = 0$  and  $V_{DS}$  becomes the maximum possible value, that is  $V_{DS} = V_{DD}$ . Thus there is an Open Circuit between the D and S terminals, in other words the JFET is acting as an Open Switch and the Load (LED) is switched off.

**Normally Off Configuration:** - Refer to the circuit for the Normally Off Configuration. In this case there is the negative voltage  $-V_P$  normally keeps the JFET in the Cut-Off region as long as the control voltage is at the 0 V level. Thus the JFET is operating as an OPEN switch. Thus the Load (LED) is in the OFF state. Next, when a positive going Control Voltage pulse is applied, the net voltage at the Gate terminal is  $V_{GS} = 0$ . This will drive the JFET to the top of the Transfer Characteristic as well as the top of the Load Line. Thus Load Current  $I_D = I_{DSS}$  and  $V_{DS}$  becomes zero. Thus there is a Short Circuit between the D and S terminals, in other words the JFET is acting as a Closed Switch and the Load (LED) is switched ON.

### **MOSFET Switch**

The V-I Characteristic of the MOSFET is shown in the figure below. This is quite similar to that of the JFET, but with the following differences -

- ❖ The Control Voltage  $V_{GS}$  is positive.
- ❖ The transfer Characteristic is plotted in the First Quadrant.



**Fig. 16:** - *N-Channel MOSFET Characteristics and the two configurations of switches.*

**Normally Off Configuration :** - The N-Channel MOSFET is normally at the Off State when the voltage at the gate  $V_{GS} = 0$ . Thus in this case the MOSFET is an Open switch and the Load (LED) is not glowing. When a positive voltage pulse is applied as the Control Signal at the Gate, it drives the MOSFET into the Ohmic Region, wherein the voltage between the Drain and Source terminals  $V_{DS}$  is (approximately) zero while the current is maximum, in other words, the MOSFET is operating as a Closed Switch. Thus the Load (LED) glows.

**Normally On Configuration :** - In the Normally On configuration, the Voltage Divider network of  $R_1$  and  $R_2$  provides a positive voltage

$V_{GS}$ . This keeps the MOSFET in the On State and the Load (LED) is glowing. When a negative voltage pulse is applied as the Control Signal at the Gate, it drives the MOSFET into the Cut Off Region, wherein the voltage between the Drain and Source terminals  $V_{DS} = V_{DD}$  while the current is zero, in other words, the MOSFET is operating as an Open Switch. Thus the Load (LED) turns off.

## TUTORIAL-6

**Example 6 : Design Problem (JFET Switch) :** - Design a Normally On JFET switch to drive a DC load so that the maximum allowable voltage between the Drain and Source at the ON State is  $V_{DS(ON)} = 120 \text{ mV}$ . The JFET to be used in the switch has the following parameters,  $r_{ds} = 10 \Omega$ ,  $V_P = 7 \text{ V}$ . Given  $V_{DD} = 15 \text{ V}$ .

### SOLUTION

In the ON State, the JFET is operating in the Ohmic region.

Given, resistance of the JFET in the Ohmic Region is  $r_{ds} = 10 \Omega$ . The maximum Drain-Source voltage in the ON State must be  $V_{DS(ON)} = 120 \text{ mV}$ .

Thus

$$\begin{aligned} I_D(\text{MAX}) &= \frac{V_{DS(ON)}}{r_{ds}} \\ &= \frac{120 \text{ mV}}{10 \Omega} = 12 \text{ mA} \\ \therefore R_D &= \frac{V_{DD}}{I_D(\text{MAX})} \\ &= \frac{15 \text{ V}}{12 \text{ mA}} = 1.25 \text{ K} \end{aligned}$$

(Use standard value resistance of 1.2 K)

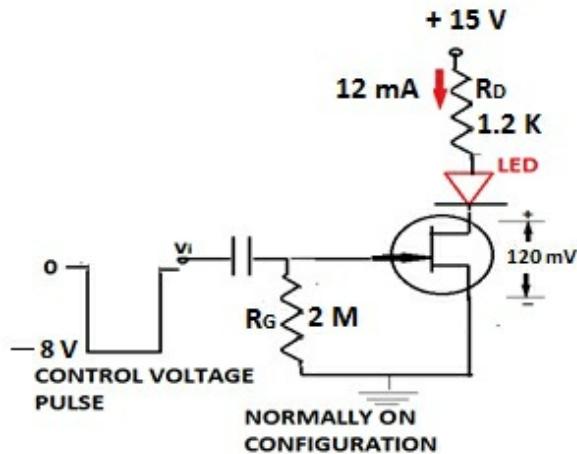
To switch the JFET Normally On Switch we require a negative voltage pulse whose amplitude must be slightly greater than  $-V_P$

Choose  $v_i = -(V_P + 1) = -(7 + 1) = -8 \text{ V}$

In order to properly reverse bias the Gate-Channel junction the Resistance  $R_G$  must be very high.

Choose  $R_G = 2 \text{ M}\Omega$ .

The designed circuit is shown in the figure below



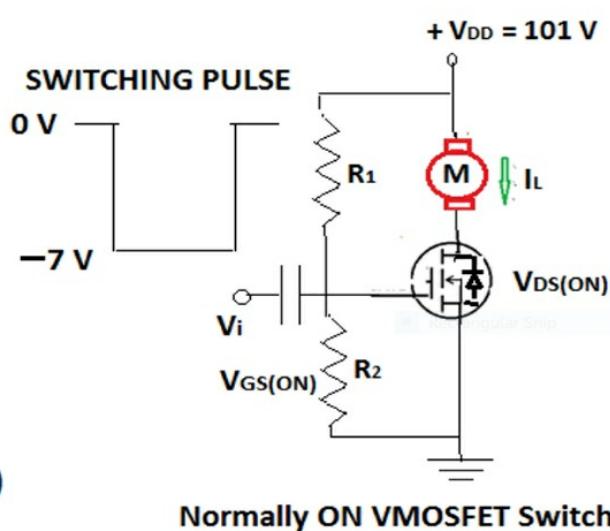
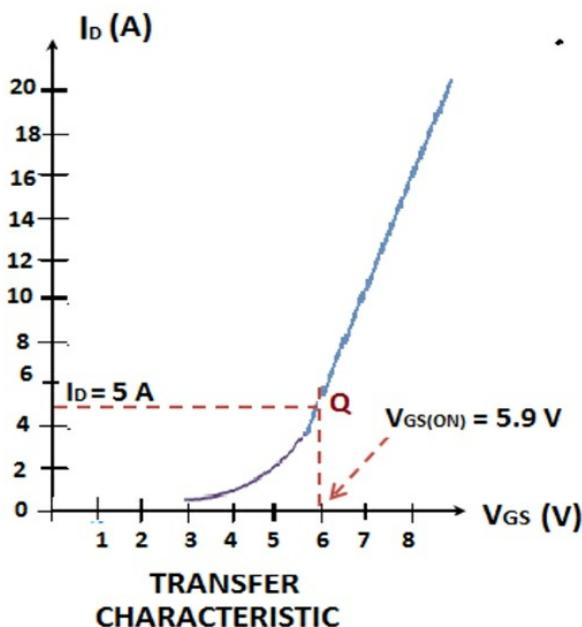
**Example 7 : Design Problem (MOSFET Switch) :** - Design a Normally On EMOSFET Switch to control a 100 V; 500 W DC motor using an appropriate MOSFET whose Transfer Characteristic graph is shown in the figure. Given the value of  $r_{DS(ON)} = 0.2 \Omega$ .

**Solution ::**

Given  $P = 500 \text{ W}$  and  $V_{DD} = 100 \text{ V}$ .

$$\therefore I_L = I_D = \frac{500}{100} = 5 \text{ A}$$

Using the Transfer Characteristic graph shown in the figure, the Bias Point is obtained as follows.



Normally ON VMOSFET Switch

Projecting a horizontal line at  $I_D = 5 \text{ A}$  to the Transfer Characteristic we get the point of intersection as 'Q'.

The X-Coordinate of this point is found from the graph as  $V_{GS(ON)} = 5.9 \text{ V}$

When the MOSFET is conducting the voltage drop across the Drain and Source terminals is

$$V_{DS(ON)} = I_D \cdot r_{DS(ON)} = 5 \times 0.2 = 1 \text{ V}$$

Thus

$$V_{DD} = 100 + 1 = 101 \text{ V}$$

$$\therefore R_D = \frac{(V_{DD} - V_{DS(ON)})}{I_D} = \frac{(101 - 1)}{5} \Omega$$

$$R_D = 20 \Omega.$$

#### (i) Use of Load Resistance instead of $R_D$

We had Load Current,  $I_D = I_L = 5 \text{ A}$  and Rated Voltage of the Load as  $V_L = 100 \text{ V}$

$$\therefore R_L = \frac{V_L}{I_L} = \frac{100}{5} = 20 \Omega$$

Since the calculated value of the Bias Resistance  $R_D$  and the Load Resistance  $R_L$  is the same, we need not connect a separate resistance  $R_D$ . The Load resistance of the motor will itself provide the necessary bias.

#### (ii) Calculation for Bias Resistance $R_1$ & $R_2$

The Bias resistance  $R_g$  is the parallel combination of  $R_1$  and  $R_2$ . The Voltage Divider combination of  $R_1$  and  $R_2$  is employed to provide the switching voltage  $V_{GS(ON)}$  from the DC Supply voltage  $V_{DD}$

Thus

$$V_{GS(ON)} = \frac{V_{DD} \cdot R_2}{(R_1 + R_2)} \quad \& \quad R_g = \frac{R_1 \cdot R_2}{(R_1 + R_2)}$$

Since  $V_{GS(ON)} \ll V_{DD}$  the resistance  $R_2 \ll R_1$

Therefore their parallel combination

$$R_g \approx R_2$$

MOSFETs are very high input resistance devices. Thus the bias resistance  $R_g$  must be very high.

$$\therefore \text{Let us choose } R_2 = 2 \text{ M}\Omega$$

From the Voltage Divider network we have

$$R_1 = \frac{(V_{DD} - V_{DS(ON)}) \times R_2}{V_{GS(ON)}}$$

$$= \frac{(101 - 5.9) \times 2}{5.9}$$

**R<sub>1</sub> = 32.23 MΩ**

**(iii) Calculation for Switching Voltage Pulse**

In order to switch the state of the N-Channel MOSFET a negative pulse greater than V<sub>GS(ON)</sub> has to be employed, and it should be negative enough to hold the MOSFET in OFF state even when the DC source is trying to force a current I<sub>D</sub> through the load.

Thus |V<sub>i</sub>| = | - (V<sub>GS(ON)</sub> + V<sub>DS(ON)</sub>) | = 5.9 + 1 = 6.9 V

We use V<sub>i</sub> ≈ - 7 V

**NOTE :: - At such high voltage ratings of V<sub>DD</sub> ≈ 100 V we must use a VMOSFET .**

**The designed circuit is shown in the figure.**

**xxxxxxxx-FET-FET-FET-xxxxxx**

# **CHAPTER – IX**

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## **FEEDBACK IN AMPLIFIERS**

## **POWER AMPLIFIERS**

**and**

## **OSCILLATOR**

*FEEDBACK in AMPLIFIERS POWER AMPLIFIERS AND OSCILLATORS*

### **INTRODUCTION**

- Each stage of a Cascaded Pre-Amplifier is a “Small Signal Amplifier”. It is called a Small Signal Amplifier because the power output of each stage is only a few micro watts, or, at best a few milli watt.
- These are analyzed with the help of any of the “Small Signal Models”, viz, r-parameter model or h-parameter model.
- In the Pre-Amplifier stage, the output voltage is of a magnitude suitable enough for use by the later stages. Hence the Pre-Amplifier is essentially a “Voltage Amplifier”. In this part, the voltage level of the signal source is amplified up to a few volts.
- In the practical field, an amplifier is often required to drive a large power rated load such as a motor. Power ratings of such loads can be in the range of a few watts to hundreds of Watts.
- Thus, Power Amplifiers are required. Power Amplifiers use Power Transistors, which are either BJT or MOSFETs. The current

ratings of these devices are of the order of a few Amperes.

- A composite amplifier system consists of the “Cascaded Pre-Amplifier” for the initial stage, followed by a Power Amplifier as the Output Stage.
- Power Amplifiers are susceptible to various types of Noise and Distortions. They are also susceptible to instability due to temperature variations. The Bandwidth of these amplifiers is also quite poor. All of these shortcomings are addressed by using “Negative Feedback” to the amplifier.
- By applying a “Positive Feedback”, an amplifier is converted into an Oscillator.

## **Section-1**

### **POWER AMPLIFIER**

#### **DEFINITION OF POWER AMPLIFIER**

**An Amplifier is called a Power Amplifier if the output power delivered to the load is Greater than or Equal to 1 W.**

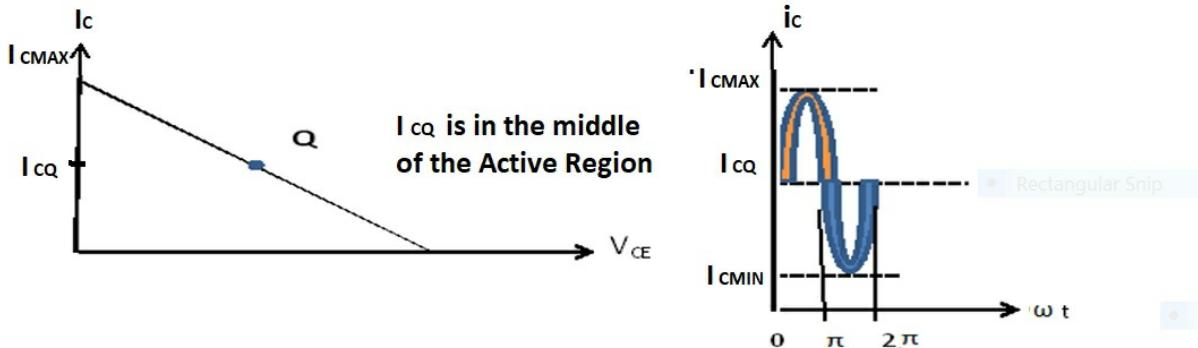
### **9.1 CLASSIFICATION OF POWER AMPLIFIERS**

Power Amplifiers are classified as CLASS-A, CLASS-B, CLASS-C and CLASS-AB in terms of 2 factors

- (1) On the basis of the location of the Q-Point on the AC Load Line.
- (2) In terms of the duration of flow of Load Current  $i_C$  w.r.t. the complete cycle of input signal.

## CLASS -A

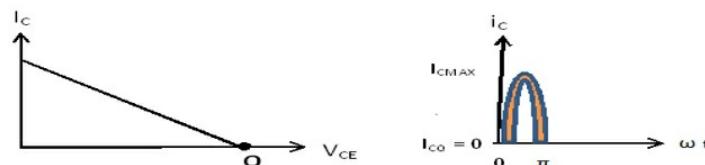
1. In Class-A Power Amplifier, the Q-Point is located exactly in the middle of the AC Load-Line.
2. In Class-A Power Amplifier, the load current  $i_C$  flows through the transistor for the complete cycle.



**Fig. 1:-** In a Class-A Power Amplifier, the Q-Point is located in the middle of the AC Load line and the signal current flows for the complete cycle.

## CLASS – B

- (a) In a Class – B Power Amplifier, the Q-Point is located the bottom of the AC Load Line.
- (b) In a Class – B Power Amplifier,  $i_C$  flows for alternate Half Cycle through either transistor.

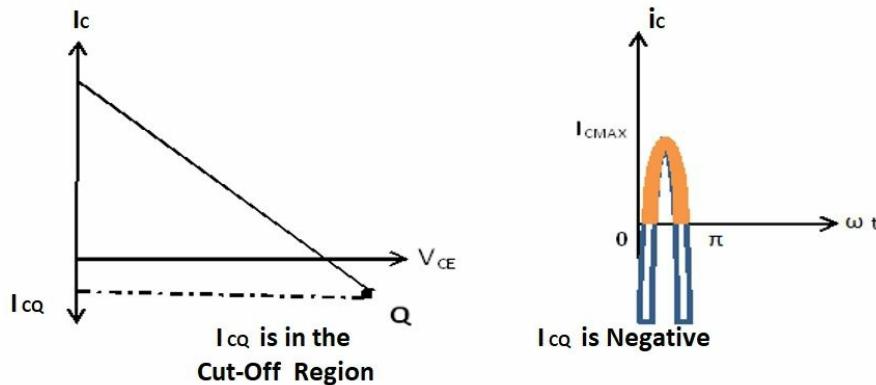


**Fig. 2: -** In a Class-B Power Amplifier, the Q-Point is located at the bottom of the AC Load line and the signal current flows for only one-half cycle.

## CLASS – C

1. In a Class – C Power Amplifier, the Q-Point is located well inside the Cut-Off region obtained by extending the AC Load Line into the Cut-Off region.
2. In a Class – C Power Amplifier, the Load Current  $i_C$  flows

for only a small pulse during the Positive Half Cycle.

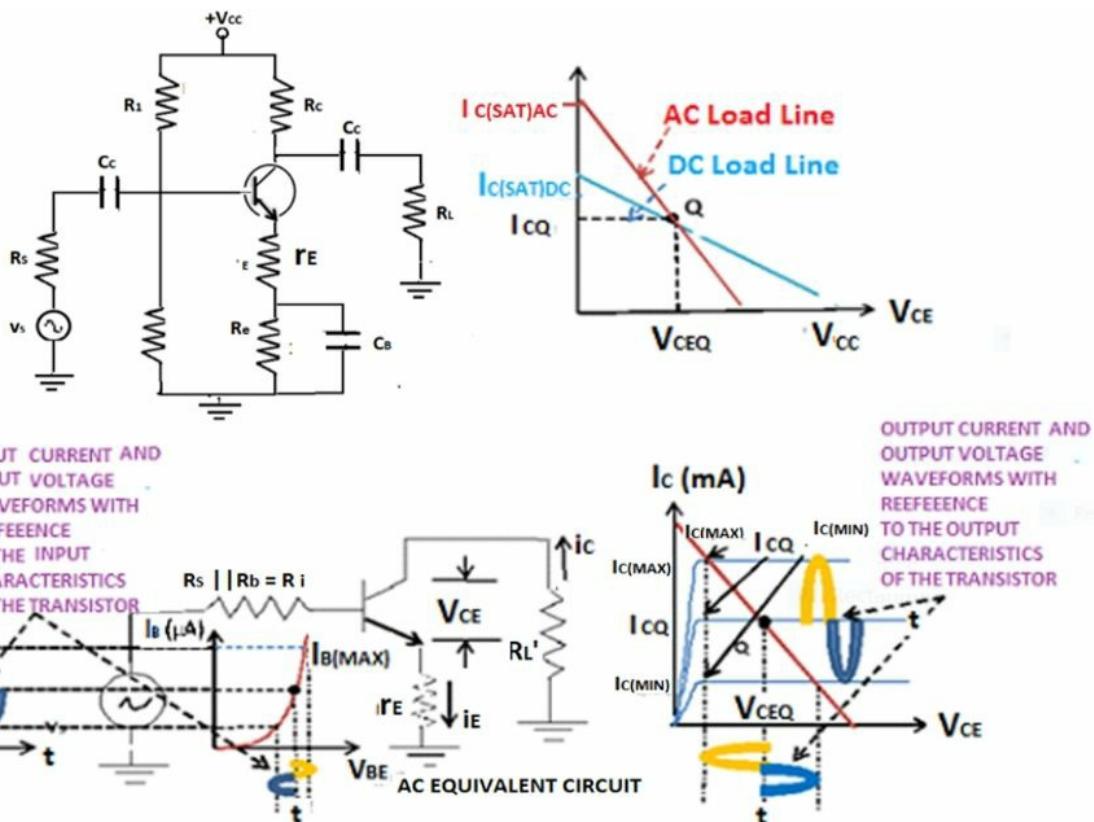


**Fig. 3:** - Collector current  $i_c$  flows for a short duration, in the form of a pulse during the top part of each positive half cycle (shown in yellow shading). During the blue part of the cycle the transistor is in the cut-off region, hence current doesn't flow.

## 9.2 Analysis of Class-A Power Amplifier

### R-C Coupled Class-A Power Amplifier

- As discussed earlier, the Class-A Power Amplifier has a Q-Point in the middle of the load line. Fig. 4 shows the circuit diagram, the AC equivalent circuit, the AC Load Line and the associated waveforms of the signal in a Class-A Power Amplifier.
- The action of amplification is determined by the Input and Output characteristics of the transistor.
- The output current and voltage signals in the transistor is determined by the AC Load Line.
- When the signal source is switched off, the transistor is at equilibrium condition, and it is operating at the Q-Point. In this case only the Biasing DC source is driving the transistor and only DC signals are present. The quantities, input current (Base Current  $I_{BQ}$ ), the input voltage ( $V_{BEQ}$ ), output current (Collector Current  $I_{CQ}$ ) and output voltage ( $V_{CEQ}$ ) are all constant and DC quantities.



**Fig. 4:** - For class –A amplifier output current flows for the complete cycle of the input current. Figure shows that output voltage is  $180^\circ$  ( $\pi$  radian) out of phase w.r.t. input voltage. Positive half cycle is marked yellow and negative half cycle is marked blue.

- When the input signal is switched on, the AC quantity gets superimposed over the DC signal. In the positive half cycle, the net Base Current and Base Voltage become greater than  $I_{BQ}$  and  $V_{BEQ}$  respectively. At the peak of the input signal, the Base Current becomes a maximum value  $I_{B(MAX)}$ . Similarly, the Base Voltage becomes  $V_{BE(MAX)}$ . During the negative half cycle, the net Base Current and Base Voltage become less than  $I_{BQ}$  and  $V_{BEQ}$  respectively. At the negative peak of the signal, the Base Current becomes a minimum value  $I_{B(MIN)}$ . Similarly, the Base Voltage becomes  $V_{BE(MIN)}$ .
- The output current and voltage are determined by Transistor Action, and controlled by the AC Load Line. By Transistor Action, the Collector Current is given by the following expression **for the**

**entire cycle.**

$$I_C = \beta i_B$$

- When the input signal current is  $i_B = I_{BQ}$ , the output signal current is

$$I_C = \beta I_{BQ} = I_{CQ}$$

The corresponding output voltage is  $V_{CEQ}$ .

- As soon as the input current reaches the maximum  $I_{B(MAX)}$ , in the positive half cycle, the output current also reaches the maximum value  $I_{C(MAX)}$ . And in the negative half cycle, when the input current attains the minimum value  $I_{B(MIN)}$ , the output current also becomes minimum  $I_{C(MIN)}$ .
- This variation of the output current is along the AC Load Line. The Load line has a negative slope, as shown in the figure. Therefore, when the **load current is increasing the load voltage will decrease and vice-versa**. This can be observed in the figure.
- When the input voltage is increasing from  $V_{BEQ}$  to  $V_{BE(MAX)}$ , the output voltage is decreasing from  $V_{CEQ}$  to  $V_{CE(MIN)}$  (yellow), and when the input voltage is decreasing from  $V_{BEQ}$  to  $V_{BE(MIN)}$ , the output voltage is increasing from  $V_{CEQ}$  to  $V_{CE(MAX)}$  (blue). Thus, it is observed that the output voltage is lagging the input voltage by  $180^\circ$  ( $\pi$  radian).
- In a Class-A Power Amplifier, the output current and voltage oscillates (swings) sinusoidally over the respective equilibrium values  $I_{CQ}$  and  $V_{CEQ}$ . In other words, the output signal in the transistor flows for the complete cycle.
- **In order for a Power Amplifier to produce maximum output power, the output current and voltage swing should be as high as possible.**

## EQUATION OF AC LOAD LINE

- ✓ The DC equivalent Circuit gives the Biasing values of the input and output quantities of a transistor amplifier. These are,  $I_{BQ}$  &  $V_{BEQ}$  and  $I_{CQ}$  &  $V_{CEQ}$ .
- ✓ In the AC Equivalent Circuit, the **Output Current (Collector**

**Current)  $i_C$  and Output Voltage  $v_{CE}$**  are due to the **instantaneous superimposition** of the AC signal on the Biasing Values  $I_{BQ}$  and  $V_{BEQ}$  respectively. The action of amplification is shown as the superimposition over  $I_{CQ}$  and  $V_{CEQ}$  respectively on the output side.

- ✓ Thus, the AC collector current ‘ $i_C$ ’ and AC output voltage ‘ $v_{CE}$ ’ are the respective differences of the instantaneous values of these quantities from their respective biasing values.

$$i_C = I_C - I_{CQ} \quad \& \quad v_{CE} = V_{CE} - V_{CEQ} \quad \dots(1)$$

- ✓ The KVL equation of the collector-emitter part of the AC equivalent circuit is

$$v_{CE} + i_E r_E + i_C R_L' = 0$$

with  $i_C \approx i_E$  we get

$$v_{CE} + i_C (r_E + R_L') = 0$$

$$\therefore i_C = \frac{-v_{CE}}{(r_E + R_L')} \quad \dots(2)$$

substituting in (1)

$$I_C - I_{CQ} = \frac{-(V_{CE} - V_{CEQ})}{(r_E + R_L')} = \frac{(V_{CEQ} - V_{CE})}{(r_E + R_L')}$$

$$\therefore I_C = I_{CQ} + \frac{V_{CEQ}}{(r_E + R_L')} - \frac{V_{CE}}{(r_E + R_L')} \quad \dots(3)$$

**Equation (3) is the equation of the AC Load Line.**

- ✓ This is a First Order equation with  $V_{CE}$  as the independent variable and with the slope of  $(-1/(r_E + R_L'))$ . If we put  $V_{CE} = 0$ , we get the “Vertical Intercept” as

$$I_{C(SAT)AC} = I_{CQ} + (V_{CEQ}/(r_E + R_L')) \dots(4)$$

If we put  $I_C = 0$  we get the “Horizontal Intercept” as

$$V_{CE(CUT-OFF)} = V_{CEQ} + I_{CQ} \cdot (r_E + R_L') \dots(5)$$

Joining these two points we get the AC Load Line.

1. Note that the Collector-Emitter circuit resistance of the DC

Equivalent circuit is  $(R_C + R_E)$ . THIS IS GREATER THAN that of the AC Equivalent circuit, which is  $(r_E + R_L')$ .

2. Recall that the slope of the DC load Line was  $\{ -1 / (R_C + R_E) \}$
3. While the slope of the AC load Line =  $\{ -1 / (r_E + R_L') \}$ .
4. Also,  $I_{C(SAT)DC} = V_{CC} / (R_C + R_E)$
5. While  $I_{C(SAT)AC} = I_{CQ} + (V_{CEQ} / (r_E + R_L'))$
6.  $V_{CE(CUT-OFF)DC} = V_{CC}$ ,
7. While the value of  $V_{CE(CUT-OFF)AC} = V_{CEQ} + I_{CQ} \cdot (r_E + R_L')$ .

**The above-mentioned points prove that the slope of the AC Load Line is GREATER THAN the slope of the DC Load Line. This is illustrated in the figure shown above.**

### CONDITION FOR CENTERED Q-POINT

The Class-A Power Amplifier must have the Q-Point in the middle of the AC Load Line.

Thus

$$I_{C(SAT)AC} = 2 I_{CQ} \text{ and } V_{CE(CUT-OFF)AC} = 2 V_{CEQ}$$

Using Eq-(5)

$$2 V_{CEQ} = V_{CEQ} + I_{CQ} \cdot (r_E + R_L')$$

$$V_{CEQ} = I_{CQ} \cdot (r_E + R_L')$$

$$\therefore (r_E + R_L') = V_{CEQ} / I_{CQ} \quad \dots(6)$$

From equation (6) :: CONDITION THAT THE Q-POINT LIES IN THE CENTRE OF THE AC LOAD LINE IS THAT “THE AC RESISTANCE OF THE COLLECTOR-EMITTER CIRCUIT (i.e. resistance of the collector-emitter circuit of the AC equivalent circuit) MUST BE EQUAL TO THE RATIO OF THE CO-ORDINATES OF THE Q-POINT”.

### OUTPUT POWER & EFFICIENCY

Considering Sinusoidal Signal

$$i_{c(t)} = I_{CQ} + I_m \sin \omega t$$

$$v_{C(t)} = V_{CEQ} + V_m \sin \omega t$$

$$\text{Also } v_{C(t)} = V_{CC} - i_{c(t)} R_L'$$

Where

$$I_m = (I_{C(MAX)} + I_{C(MIN)}) / 2$$

$$V_m = (V_{C(MAX)} + V_{C(MIN)}) / 2$$

Substituting for  $i_{C(t)}$  we have

$$v_{C(t)} = V_{CC} - \{ I_{CQ} + I_m \sin \omega t \} R_L'$$

Instantaneous power delivered at the load on the output terminal is

$$P_O = i_C^2 R_L' \dots (7)$$

Average Power at the load is

$$P_{OAV} = \frac{1}{2\pi} \int_0^{2\pi} i_C^2 R_L' d\omega t$$

$$P_{OAV} = \frac{1}{2\pi} [\left\{ \int_0^{2\pi} I_{CQ}^2 R_L' d\omega t \right\} + \left\{ \int_0^{2\pi} I_m^2 R_L' \sin^2 \omega t d\omega t \right\}]$$

Using

$$\sin^2 \omega t = \frac{1}{2} \{ 1 - \cos 2\omega t \}$$

and integrating within these limits we get

$$P_{OAV} = \frac{1}{2\pi} I_{CQ}^2 R_L' \{ 2\pi \} + \frac{1}{2\pi} I_m^2 R_L' [(\frac{1}{2}) \{ 2\pi \} - \frac{1}{2} \{ (\sin 2\omega t)_0^{2\pi} \}]$$

We have  $\sin 0 = \sin 2\pi = 0$ . And  $2\pi$  at numerator and denominator is cancelled. Hence

$$P_{OAV} = I_{CQ}^2 R_L' + \frac{1}{2} I_m^2 R_L' \dots (8)$$

In equation (7) if AC signal is switched off then  $I_m = 0$ . Hence the output power is only due to the DC biasing source.

$$P_{OAV(DC)} = I_{CQ}^2 R_L' \dots (9)$$

And

$$P_{OAV(AC)} = \frac{1}{2} I_m^2 R_L'$$

$$P_{OAV(AC)} = \frac{1}{2} V_m I_m \dots (10)$$

$$\text{Since } I_m R_L' = V_m$$

$$\text{And } V_m/\sqrt{2} = V_{RMS}$$

$\therefore$

$$P_{OAV(AC)} = V_{RMS} I_{RMS} \dots (11)$$

Again, Instantaneous power dissipated at the collector (load) is

$$P_C(t) = v_{C(t)} i_{C(t)}$$

$$P_{C(t)} = [V_{CC} - \{ I_{CQ} + I_m \sin \omega t \} R_L'] \cdot [I_{CQ} + I_m \sin \omega t]$$

Average Power dissipated at the collector (load) is the integration of this expression within the limits 0-to-  $2\pi$ . Thus  $P_{CAV}$  is given by –

$$P_{CAV} = \frac{1}{2\pi} \int_0^{2\pi} v_{c(t)} \cdot i_{c(t)} d\omega t$$

$$P_{CAV} = \frac{1}{2\pi} \int_0^{2\pi} [\{ V_{CC} - (I_{CQ} + I_m \sin \omega t) R_L' \} \cdot \{ I_{CQ} + I_m \sin \omega t \}] d\omega t$$

In this the term within the square bracket is evaluated as

$$V_{CC} I_{CQ} + V_{CC} I_m \sin \omega t - I_{CQ}^2 R_L' - 2 I_{CQ} I_m R_L' \sin \omega t - I_m^2 R_L' \sin^2 \omega t$$

Using  $\sin^2 \omega t = \frac{1}{2} \{ 1 - \cos 2\omega t \}$ , and using the limits, the integration of the term above results in the following expression. In this we have used the property that the integration of a ‘sine’ or a ‘cosine’ function in the limits 0 – to -  $2\pi$  results in 0.

Thus we have Average Power Dissipated at the collector as—

$$P_{CAV} = V_{CC} I_{CQ} - I_{CQ}^2 R_L' - \frac{1}{2} I_m^2 R_L' \dots (12)$$

From this expression, the DC Power supplied by the Battery is  $P_S$  and AC Power due to the signal source is  $P_{OAV(AC)}$  given by equations (12) and (13) below

$$P_S = V_{CC} I_{CQ} \dots (13)$$

$$P_{OAV(AC)} = \frac{1}{2} I_m^2 R_L' = \frac{1}{2} V_m I_m \dots (14)$$

### **EFFICIENCY OF RC COUPLED CLASS-A POWER AMPLIFIER**

Power supplied by the Battery remains constant irrespective of whether the AC signal source is switched on or not. Efficiency of an amplifier is defined as the “Ratio of AC Power Output at the load to the DC Power Input from the battery”.

$$\text{Efficiency} = \eta = \frac{P_{OAV(AC)}}{P_S}$$

These quantities are given by equations (13 ) and (14) above.

Substituting we have—

$$\eta = \frac{\frac{1}{2} V_m I_m}{V_{CC} I_{CQ}} = \frac{V_m I_m}{2 V_{CC} I_{CQ}}$$

We had

$$I_m = (I_{C(MAX)} + I_{C(MIN)}) / 2$$

$$V_m = (V_{C(MAX)} + V_{C(MIN)}) / 2$$

For maximum efficiency the amplifier must be driven to produce the maximum output power. For this purpose, the output current and output voltage must have the maximum swing. In other words,

$$I_{C(MIN)} = 0 \quad \& \quad V_{C(MIN)} = 0$$

$$I_{C(MAX)} = 2 I_{CQ} \quad \& \quad V_{C(MAX)} = V_{CC}$$

Thus

$$\therefore I_m = \frac{I_{C(MAX)}}{2} = \frac{2 I_{CQ}}{2} = I_{CQ}$$

And

$$V_m = \frac{V_{C(MAX)}}{2} = \frac{V_{CC}}{2}$$

Substituting

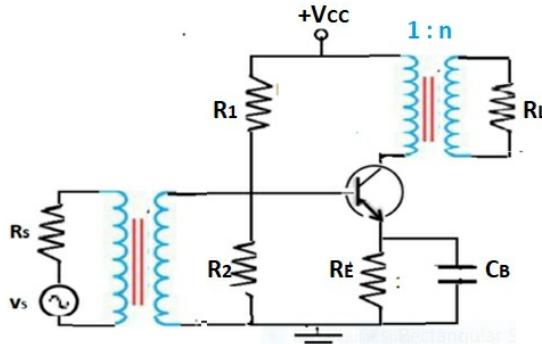
$$\eta = \frac{V_{CC} \cdot I_{CQ}}{4 V_{CC} \cdot I_{CQ}}$$

$$\eta = \frac{1}{4} = 0.25 = 25\% \quad \underline{\dots(15)}$$

**THUS, MAXIMUM EFFICIENCY OF A RC COUPLED CLASS-A POWER AMPLIFIER IS 25 % ONLY.**

### Transformer Coupled Class-A Power Amplifier

- ❖ One of the advantages of Transformer Coupled amplifier is that it can handle a larger amount of power. Thus, the output signal power  $P_{OAC}$  is greater.
- ❖ Again, in a Transformer Coupled Amplifier, the DC Collector Resistance is the internal resistance of the primary coil of the transformer. Since DC resistance of a coil is quite low, the value of  $R_C$  is low. Hence DC power dissipation in the circuit is low.
- ❖ Since on the one hand, AC power output is high and on the other hand the DC power dissipation is low, therefore the Efficiency of the Transformer Coupled Amplifier is quite high compared to the RC Coupled Amplifier. The circuit in the Fig. 5 shows the Transformer Coupled Class-A Power Amplifier.



**Fig.5 : - Transformer coupled Class-A Power Amplifier**

## EFFICIENCY

It can be proved that Efficiency of Transformer Coupled Amplifier is 50 %.

**Proof :-**

With centered Q--Point

$$I_{C(MAX)} = 2 I_{CQ} \quad \& \quad V_{CE(MAX)} = 2 V_{CEQ} = 2 V_{CC}$$

$$\frac{P_{OAC(AC)}}{P_S}$$

$$\text{Efficiency} = \eta = \frac{P_{OAV(AC)}}{P_S}$$

$$\text{Where } P_{OAV(AC)} = \frac{1}{2} V_m I_m \quad \& \quad P_S = V_{CC} I_{CQ}$$

With

$$V_m = \frac{V_{CE(MAX)} - V_{CE(MIN)}}{2} \quad \& \quad I_m = \frac{I_{C(MAX)} - I_{C(MIN)}}{2}$$

$$\text{Putting } V_{CE(MIN)} = 0 = I_{C(MIN)}$$

we have

$$V_m = V_{CE(MAX)}/2 = V_{CC} \quad \& \quad I_m = I_{C(MAX)}/2 = I_{CQ}$$

$$P_{OAV(AC)} = \frac{1}{2} V_m I_m = \frac{1}{2} V_{CC} I_{CQ}$$

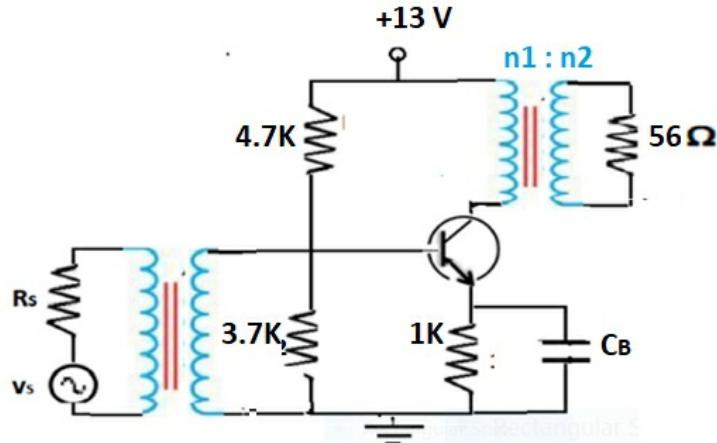
$$\text{Putting } P_S = V_{CC} I_{CQ} \text{ we have}$$

$$\eta = \frac{\frac{1}{2} V_{CC} \cdot I_{CQ}}{V_{CC} \cdot I_{CQ}} = \frac{1}{2} = 0.5 = 50 \% \quad \underline{\dots(16)}$$

## TUTORIAL-1

**Example 1 :-** Draw the AC and DC load Line of the Class-A power amplifier. The silicon transistor in the circuit has  $\beta = 150$  and the

*coupling transformer has a primary coil resistance of  $40 \Omega$  and a turns ratio of 74 : 14.*



**SOLUTION :-**

#### DC Load Line

Using the method employed in Chapters IV, V and VI

$$V_2 = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{3.7 \times 13}{4.7 + 3.7} = 5.7 \text{ V} ; R_b = \frac{R_1 R_2}{R_1 + R_2} = \frac{4.7 \times 3.7}{4.7 + 3.7} = 2.07 \text{ K}$$

$$I_{BQ} = \frac{V_2 - V_{BE}}{(R_b + (1+\beta)R_E)} = \frac{5.7 - 0.7}{(2.07 + (151 \times 1))} = 0.03 \text{ mA}$$

$$I_{CQ} = \beta I_{BQ} = 150 \times 0.03 = 4.9 \text{ mA} \approx 5 \text{ mA}$$

DC resistance at the Collector is the resistance of the primary coil of the transformer,  $R_C = 40 \Omega$  ( 0.04 K).

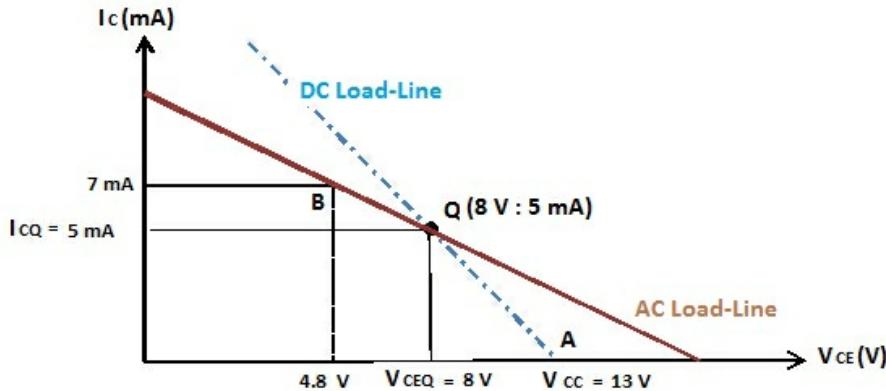
$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E) = 13 - 4.9 \times 1.04 = 7.9 \text{ V} \approx 8 \text{ V}$$

From this, the Q-Point is plotted at the co-ordinates, (8 V, 5 mA).

The DC Load line is a straight line joining the  $I_{C(SAT)}$  point with the  $V_{CE(CUT-OFF)}$  point and passing through the Q-Point. Thus the DC Load-Line can be plotted by joining the Q-Point with the  $V_{CE(CUT-OFF)}$  point.

$$V_{CE(CUT-OFF)} = V_{CC} = 13 \text{ V}.$$

Let this point be shown as the point-A.



### AC Load-Line

The AC Load-Line is also a straight line passing through the Q-Point.

The AC Load-Line indicates the AC signal current in the amplifier, which uses the AC Collector Resistance  $R_{AC}$ . AC collector current is oscillations over the  $I_{CQ}$  value. This is denoted by  $\Delta I_C$ . This oscillation corresponds to an oscillation of the collector voltage denoted by  $\Delta V_{CE}$ , given by

$$\Delta V_{CE} = \Delta I_C R_{AC}$$

The AC resistance  $R_{AC}$  is the sum of the resistance of the primary added with the Load Resistance reflected on to the primary side of the transformer.

$$\therefore R_{AC} = 40 + \left( \frac{n_1}{n_2} \right)^2 = R_L$$

$$\therefore R_L = 40 + (74/14)^2 \times 56$$

$$= 1600 \Omega = 1.6 K$$

Let us take  $\Delta I_C = 2 \text{ mA}$

Thus we have

$$\Delta V_{CE} = 2 \times 1.6 = 3.2 \text{ V}$$

Since the AC Load-Line is also line with a negative slope, we can draw the AC Load-Line by joining the Q-Point with a point B whose co-ordinates are  $\Delta I_C$  greater than  $I_{CQ}$  and  $\Delta V_{CE}$  lesser than  $V_{CEQ}$ .

Thus co-ordinates of the point B are

$$(8-3.2 : 5+2) = (4.8 \text{ V} : 7 \text{ mA})$$

The AC Load-Line and DC Load-Line are shown in the figure.

**Example 2 :-** Calculate the efficiency of the amplifier shown in the

*Example 9.1, given transformer efficiency is 85 %.*

**SOLUTION ::**

$$\text{Input DC Power } P_S = V_{CC} I_{CQ}$$

Substituting

$$P_S = 13 \times 5 = 65 \text{ mW}$$

Output AC Power

$$P_{AC} = \frac{1}{2} V_m \cdot I_m$$

Since this is a Class-A amplifier, the Q-Point is in the middle of the AC Load-Line

For maximum output power and maximum efficiency, the peak-to-peak signal swing must be such that  $V_{CE(MAX)} = 2 V_{CEQ}$  and  $I_{C(MAX)} = 2 I_{CQ}$ .

In other words,  $V_m = V_{CEQ}$  and  $I_m = I_{CQ}$

In Example 8.1 we had solved that

$$V_{CEQ} = 8 \text{ V} \quad \& \quad I_{CQ} = 5 \text{ mA}$$

$$\therefore P_{AC} = \frac{1}{2} 8 \times 5 = 20 \text{ mW}$$

Since transformer efficiency is 85 %, the output power delivered to the load is

$$P_o' = 0.85 P_{AC} = 0.85 \times 20 = 17 \text{ mW}$$

Thus Efficiency of the amplifier is

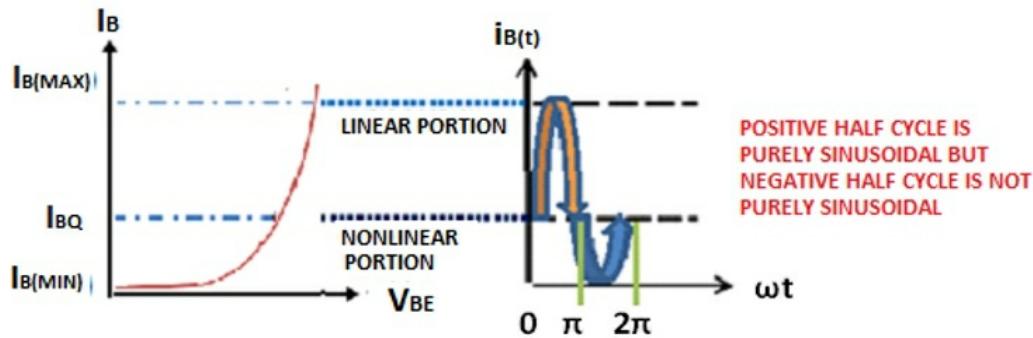
$$\eta = \frac{17}{65} \times 100 = 26.15 \%$$

### 9.3 Distortion in Class-A power Amplifier

#### 1. NON-LINEAR DISTORTION OR SECOND HARMONIC DISTORTION

The output current  $i_C$  equals  $\beta i_B$ . The Input current  $i_b$  follows the input characteristic curve. Recall that, for maximum efficiency we assumed  $I_{CMN} = 0$ . If  $I_{CMN}$  must be zero the  $I_{BMN}$  must also be zero.

But the Input Characteristic Curve of a transistor is Non-Linear near the lower side of the graph. Thus the variation of  $I_B$  w.r.t.  $V_{BE}$  is Non-Linear. Thus the waveform of current  $i_B$  is not purely sinusoidal in the negative half cycle. Thus the waveform of output current  $i_C$  also will be similarly distorted. This type of distortion is called Non-Linear Distortion. This is illustrated in the Fig.-6 below.



**Fig. 6: - Non-Linear Distortion or Second harmonic Distortion.**

At the lower side of the input characteristic the shape of the curve is Parabolic. For a parabolic curve, the output current will be

$$i_C = I_{CQ} + \beta i_B + \beta i_B^2 \quad \text{Let } i_B = I_{Bm} \sin \omega t$$

$$i_C = I_{CQ} + \beta I_{Bm} \sin \omega t + \beta I_{Bm}^2 \sin^2 \omega t$$

Or

$$i_C = C_0 + C_1 \sin \omega t + C_2 \sin^2 \omega t$$

$$i_C = C_0 + C_1 \sin \omega t + \frac{1}{2} C_2 - \frac{1}{2} C_2 \cos 2\omega t$$

Or

$$i_C = B_0 + B_1 \sin \omega t - B_2 \cos 2\omega t$$

This shows that the output contains two **unwanted terms**  $B_0$  and  $B_2 \cos 2\omega t$ . We assumed that the input signal is  $i_B = I_{Bm} \sin \omega t$ , which is purely sinusoidal. Whereas, at the output we have  $B_0$ , which is a DC quantity and  $B_2 \cos 2\omega t$ , which is a term at twice the signal frequency. This term  $B_2 \cos 2\omega t$  is called the "**Second Harmonic Component**".

These two terms are the Distortions at the output due to Non-Linearity of the Input Characteristic Curve.

We define a term “Distortion Coefficient” as

$$D_2 = |B_2 / B_1| \dots (17)$$

where  $B_2$  and  $B_1$  are the amplitudes of the “Second Harmonic”

term, ‘ $\cos 2\omega t$ ’ which is at twice the signal frequency, and the expected output signal term ‘ $\sin \omega t$ ’, which is at the actual signal frequency, respectively.

2.

**HIGHER HARMONIC DISTORTIONS** :-- The half cycles of the sinusoidal input current ‘ $i_B$ ’ is symmetrical about the Biasing value of base Current  $I_{BQ}$ . The Output current ‘ $i_C$ ’ is proportional to the input current since  $i_C = \beta i_B$ . Thus half cycles of the output current will be symmetrical about the Biasing Value of output current  $I_{CQ}$ . In a Power Amplifier maximum efficiency is achieved when the input signal drives the input current all along the Linear Portion of the input Characteristic. Assume that in the process of driving the amplifier, the input current stays in the linear portion of the input characteristic. Thus the output current is expected to be distortion less. However, the Output Characteristic is divided into the (a) ‘Saturation Region’, (b) ‘Active Region’ and (c) ‘Cut-Off Region’. The collector current  $I_C$  must assume values only on the AC Load Line (since Load Line is the Locus of the Load Line Equation). Again, the maximum value of collector current cannot exceed  $I_{C(SAT)AC}$  and the minimum value cannot be less than  $I_{C(CUT-OFF)} \approx 0$ . Now, if the input current had driven the Base Current to positive and negative extremities in such a way that the maximum value of collector current is required to be of a value

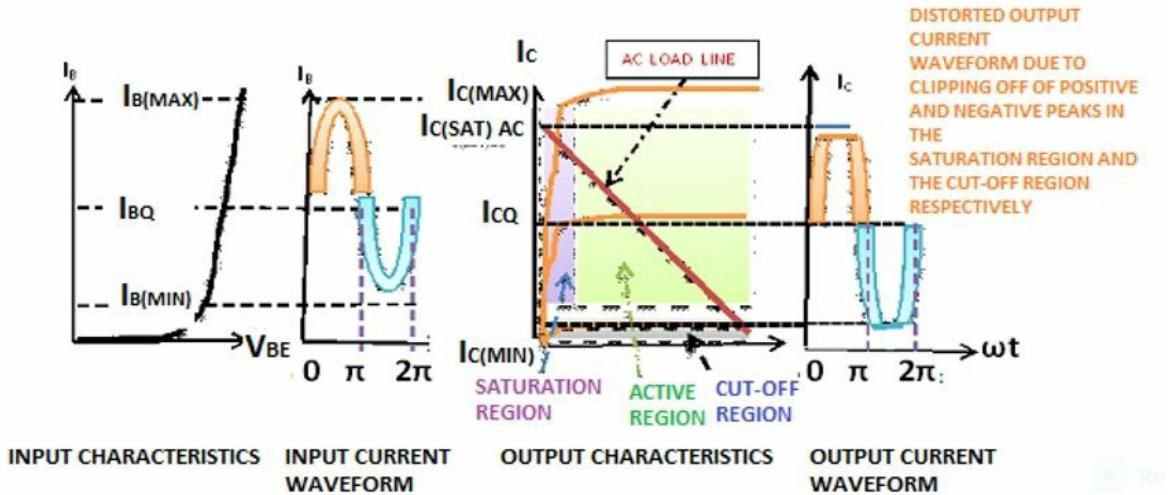
$$I_{CMAX} = \beta I_{BMAX} > I_{C(SAT)AC}$$

and the minimum value of collector current is required to be of a value

$$I_{C(CUT-OFF)} < 0,$$

then the output current waveform will be distorted. This is because, the maximum collector current will saturate at  $I_{C(SAT)AC}$  and minimum collector current will not be less than zero. This is shown in the Fig. 7. below.

From the waveform of the input and output current , it is observed that both input and output current have the same frequency, which is the signal frequency  $f_S$  , with the time period being  $T_S = 1 / f_S$  . The output signal waveform is not sinusoidal but all the same it is periodic with the same periodicity as the input signal. Thus the output waveform may be expressed as a Fourier Series , given by Eq. 18



**Fig. 7.: - Higher Harmonic Distortion is caused when the current waveform is clipped off at the positive and negative peaks.**

$$i_{C(t)} = B_0 + \sum_{n=0}^{\infty} B_n \cos(2\pi n f_s t + \phi_n) \quad \dots(18)$$

Where  $B_0$  and each  $B_n$  are the Fourier Coefficients.

From the equation (18) we observe that the output current consists of the DC term  $B_0$  , a term at  $n=1$  having amplitude  $B_1$  and a frequency  $f_S$  and an infinite number of Harmonic Components having amplitude  $B_n$  and frequency  $n.f_S$  . The term at  $n=1$  having amplitude  $B_1$  and a frequency  $f_S$  is called the ‘Fundamental Component’. This is the required output signal. We also have an infinite number of distortion coefficients given by

$$D_1 = |B_2 / B_1| : D_2 = |B_3 / B_1| : D_3 = |B_4 / B_1| \text{ etc.} \quad \dots(19)$$

## 9.4 Class – B Push-Pull Power Amplifier

For Class – B operation the Q-Point is at the bottom of the Load Line.

Hence

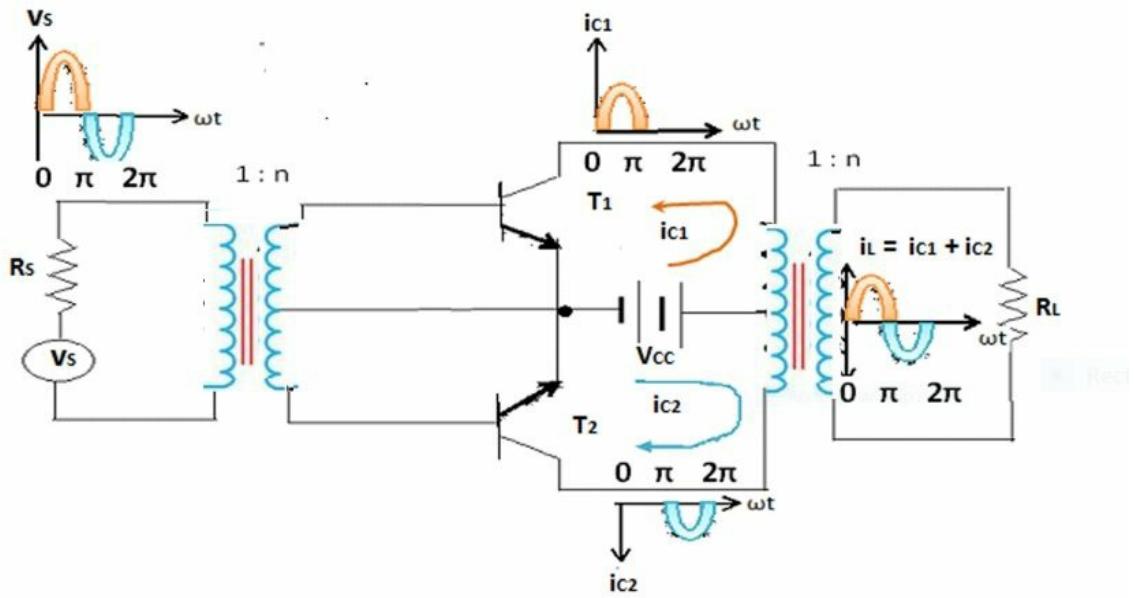
$$V_{CEQ} = V_{CC} \text{ and } I_{CQ} = 0.$$

Thus, a transistor will operate only in the positive half cycle. The Class –B Push-Pull amplifier has 2 transistors, each operating in either half cycle, so that the output current flows for the complete cycle. The circuit of a Transformer Coupled Class-B Push-Pull Amplifier is shown in the circuit.

This has a number of advantages over the Class-A Power Amplifier as enumerated below

1. Supports a larger input current swing, therefore output power level is higher.
2. Second harmonic and other Higher Even harmonic Distortion is eliminated.
3. Output at the load is free from a DC Component.
4. Has a greater efficiency of 78.5 %.

The input signals to  $T_1$  and  $T_2$  are  $180^\circ$  out of phase due to the center-tapped secondary of the transformer at the source side. Thus,  $T_1$  operates during the positive half cycle of the input signal while  $T_2$  is switched off since, at this instant of time the potential at the Base is negative. Thus, the current  $i_{C1}$  flows in the direction as shown in the figure. During the negative half cycle of the input signal the potential at the Base of  $T_1$  is negative, hence  $T_1$  is switched off. But during this time the potential at the Base of  $T_2$  is positive. Hence  $T_2$  operates and the current  $i_{C2}$  flows in the direction as shown in the figure 8. The currents  $i_{C1}$  and  $i_{C2}$  are in opposite directions. They flow in the two separate halves of the center-tapped primary of the transformer at the load side. Thus, at the primary they add up to form a complete cycle of load current  $i_L$  as shown in the figure.



**Fig. 8:** - Class-B Amplifier is in Push-Pull configuration. Current in each transistor flows in alternate half cycles, while the current in the load gets added up to form a complete cycle.

## EFFICIENCY

Since only one transistor is operating in each half cycle while the other is switched off, hence DC Biasing current flows during only one half cycle in each transistor. Hence DC power dissipation is much reduced. Since the output current at the load is in a complete cycle, the output AC power remains the same as the Class-A amplifier. Since AC output power remains the same while the DC input power is reduced, the efficiency is much greater. This is proved as follows.

Since AC output current flows for only one half cycle, the RMS current is same as that for H.W. rectifier.

Thus

$$I_{CRMS} = I_{CMAX} / 2 \quad \& \quad V_{CRMS} = V_{CMAX} / 2$$

$$\text{with } I_{CMAX} = V_{CC}/R_L' \quad \& \quad V_{CMAX} = V_{CC}$$

Where  $R_L'$  is the resistance of the secondary, reflected on the primary

$$R_L' = (n/2)^2 R_L = n^2 R_L/4$$

Assume  $n = 1$

Therefore Output AC Power of each transistor is

$$\begin{aligned} P_{OAV(AC)} &= I_{CRMS} V_{CRMS} \\ &= \frac{I_{C(MAX)} V_{CE(MAX)}}{4} = \frac{V_{CC}^2}{4 R'_L} \end{aligned}$$

Since there are 2 transistors, the total output AC power is

$$P_{ACT} = 2 P_{OAV(AC)} = \frac{V_{CC}^2}{2 R'_L}$$

Input DC power supplied by the battery to one transistor is

$$P_S = V_{CC} I_{OAV}$$

When output current flows for half cycle, the Average value of the current will be the same as that for H.W. rectifier, as explained earlier. Thus

$$I_{OAV} = I_{CMAX} / \pi \text{ where } I_{CMAX} = V_{CC} / R_L'$$

Thus total DC input power supplied to the two transistors is

$$\begin{aligned} P_{ST} &= 2 V_{CC} I_{OAV} = 2 V_{CC} I_{CMAX} / \pi \\ &= 2 V_{CC}^2 / \pi R_L' \end{aligned}$$

$$\eta = P_{ACT} / P_{ST} = \{ V_{CC}^2 / 2 R_L' \} / \{ 2 V_{CC}^2 / \pi R_L' \}$$

$$\therefore \eta = \pi / 4 = 0.785 = 78.5 \% \quad \dots(20)$$

### CANCELLATION OF DISTORTIONS

If Second harmonic Distortion is present then output current of one transistor , say  $T_1$  is

$$i_{C1} = B_0 + B_1 \sin \omega t - B_2 \cos 2 \omega t$$

For the second transistor, the collector current is  $180^\circ$  ( $\pi$ ) out of phase . Thus

$$i_{C2} = B_0 + B_1 \sin (\omega t + \pi) - B_2 \cos 2 (\omega t + \pi)$$

$$i_{C2} = B_0 - B_1 \sin \omega t - B_2 \cos 2 \omega t$$

Since the current at the load is the sum of  $i_{C1}$  and  $i_{C2}$  , but again since  $i_{C1}$  and  $i_{C2}$  out of phase by  $180^\circ$  , we have

$$| i_L | = i_{C1} - i_{C2}$$

$$| i_L | = \{ B_0 + B_1 \sin \omega t - B_2 \cos 2 \omega t \} - \{ B_0 - B_1 \sin \omega t - B_2 \cos 2 \omega t \}$$

$$| i_L | = 2 B_1 \sin \omega t$$

From the above the following observations can be made—

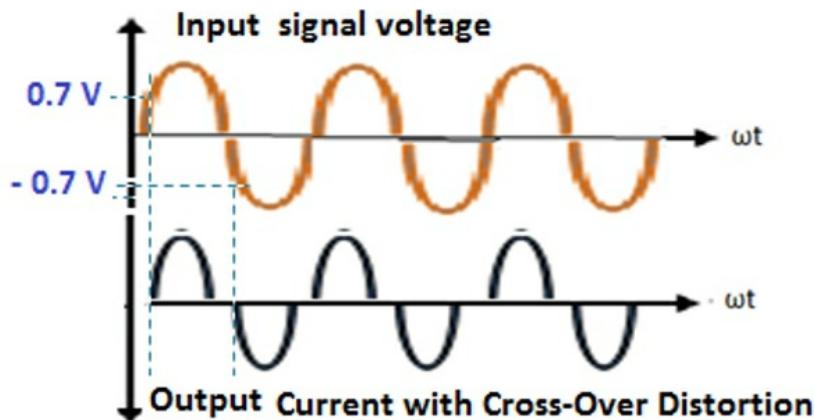
- The output is free of Second Harmonic Distortion.
- Output is free of the DC component.

- The output current swing has double the magnitude compared to Class –A amplifier. Thus the output power level is higher.
- Class-B Power Amplifier has higher efficiency compared to Class-A Amplifier.

### Cross-Over Distortion and Class – AB Amplifier

Even though the Class-B Push-Pull configuration eliminates Non-Linear Distortion and Higher Harmonic Distortions, it introduces a kind of distortion, called Cross-Over Distortion.

Recall that a transistor goes into Active Region only when the forward bias at the Emitter-Base junction is greater than the Cut-in-voltage  $V_Y$ . Therefore, the transistor does not operate as long as the input voltage is less than  $V_Y$ . In other words, the current does not flow for the duration of time in each half cycle, till the instant the input voltage crosses the value of  $V_Y$  of the transistor. For Si, the quantity  $V_Y$  equals 0.7 V. Thus, the current waveform of the Class-B Push-Pull amplifier will have a distorted shape as shown in the Fig. 8.9. This distortion is named as **Cross-Over Distortion**.

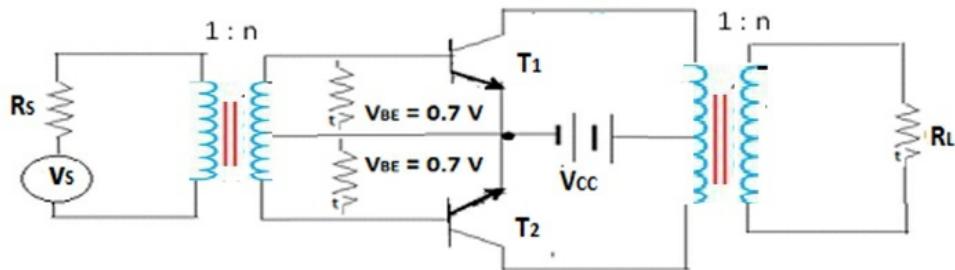


**Fig. 9.: - Cross-Over Distortion in Class-B Push-Pull configuration.**

### Class-AB Push-Pull Amplifier

In order to overcome the Cross-over Distortion, the two transistors of the Push-Pull configuration need to be biased at a point which is 0.7 V above the X-Axis. This is achieved by adding a resistor in the Base-Emitter circuit. The value of the resistor is calculated in such a manner that there exists a voltage drop equal to 0.7 V across the resistor, so that the Emitter-Base junction is applied with a forward bias

of the same value. The circuit is as shown in the Fig.- 10 below. Due to the current flow in the resistor, there exists a power loss. This results in the fact that the efficiency of the Class-AB configuration is slightly less than that of the Class-B configuration.

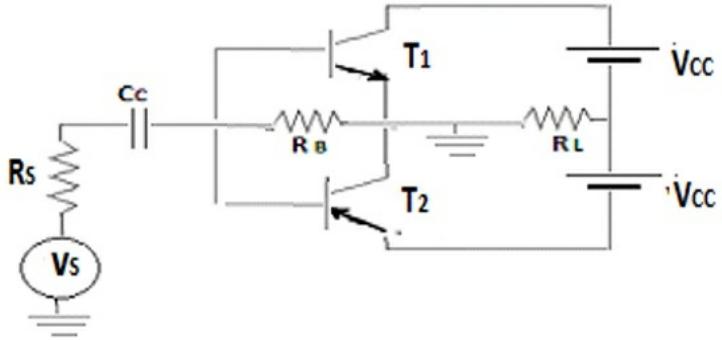


**Fig. 10: - Class-AB Push-Pull configuration.**

Ref

### Complementary Symmetry Class AB Push-Pull Amplifier

The Push-Pull amplifiers discussed so far require two transformers, one at the input and the other at the output. The function of the input transformer is to split the input signal in such a way as to apply the positive half cycles of the input signal to the upper transistor and the negative half cycles to the lower transistor. The transformer at the output combines the amplified half-cycles and applies the added up complete cycle to the load across the secondary winding. However, transformers are bulky. Hence these circuits would not conform to one of the design goals of an electronic engineer, namely that, the circuit to be designed should be as light weight as possible. Due to transformers there will be some power loss also, resulting in lower efficiency. The complementary symmetry circuit shown in the Fig. 11 does not use transformers.



**Fig. 11:** - Push-Pull Amplifier circuit with complementary symmetry transistors.

In the positive half cycle of the input signal, the bases of the transistors are at a positive potential. This will pull the transistor  $T_1$  into active region while pushing  $T_2$  into cut-off. The positive half cycle will be amplified by  $T_1$ . The reverse will happen in the negative half cycle and the negative half cycle will be amplified by  $T_2$ . The amplified signal will be added up half cycle by half cycle at the load resistance  $R_L$ . Thus, transformers will not be required at the input and the output for the signal splitting function. The resistance  $R_B$  at the base is used to bias the transistors slightly above the x-axis, so that we have Class-AB operation.

## Section – 2

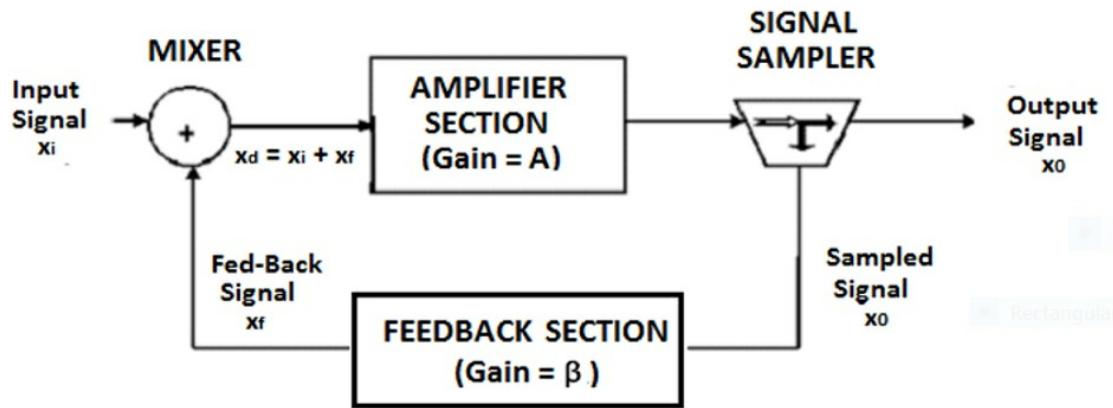
### Feedback in Amplifiers

## INTRODUCTION

- In literature, the meaning of the task of taking a “Feed-Back” is extracting some portion of the outcome of some work and taking it back to the source in order to evaluate the quality of the outcome, with the purpose of investigating whether some measures can be taken to improve or modify the performance.
- This is applicable to amplifiers also. In an amplifier a portion of the output signal is fed back at the input point.
- Various aspects of the performance of an amplifier such as stability of operation, impedance matching with source and load or working band-width may be improved with the help of feedback.
- Some additional hardware is used as the Feedback path to modify the performance to the expected quality. This is shown schematically in the Fig-1 below.

## **9.5 Type of Feedback: Negative Feedback and Positive Feedback.**

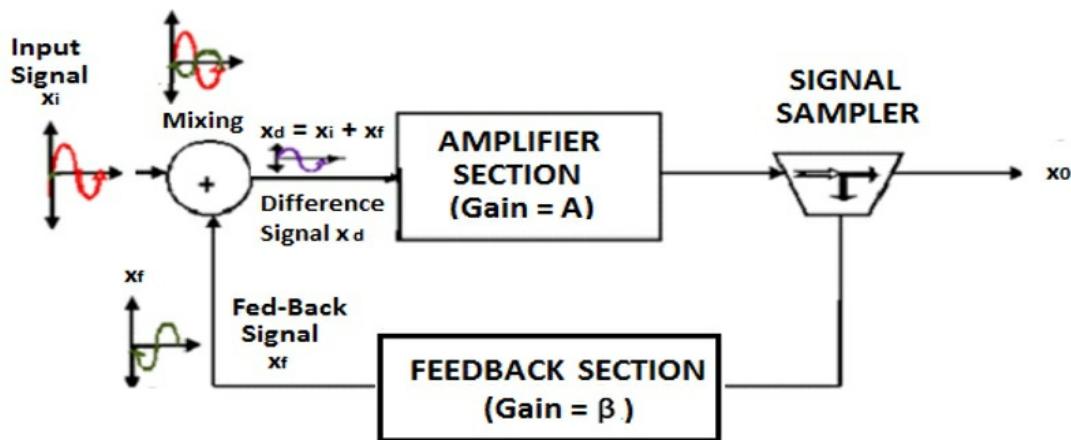
- The input to the system is provided by a signal source in the form of the input signal  $x_i$ . This is mixed with the fed back signal  $x_f$  in the Mixer section.
- These two signals are **either added or subtracted** to or from one another to generate the basic input signal  $x_d$  of the amplifier.
- This signal  $x_d$  is amplified as  $x_o$ . A portion of the output signal is sampled by the sampler and applied to the feedback section.
- The feedback section generates  $x_f$ , which is the fed back component of the output signal. **The phase angle of  $x_f$  with respect to that of the input signal  $x_i$**  determines the classification of the system as either a Positive Feedback system or a Negative Feedback system.



**Fig.- 1: - Schematic of a Feedback System.**

### Analysis of Negative Feedback

- ❖ The word “Negative” in the term Negative Feedback does not have the usual “negative” meaning of literature. Nor does the word “Positive” mean something exceptionally good.
- ❖ By the term Negative Feedback we simply mean that the Feedback signal  $x_f$  is fed back in a phase angle which is negative w.r.t. to the input quantity.
- ❖ In case of Positive Feedback the Feedback signal  $x_f$  is fed back in phase w.r.t. to the input quantity  $x_i$ .
- ❖ The schematic shown in Fig.-1 is reproduced in the figure below with the feedback signal being applied in a phase angle of  $180^0$  w.r.t the input signal. When these two signals are mixed instant by instant we find that since the amplitude of  $x_i$  is positive in the first half cycle, that of  $x_f$  is negative and vice –versa, thus, at every instant of time the amplitude of the signal  $x_d$  is less than the input signal  $x_i$ . Hence the system is classified as a Negative feedback system.



**Fig.- 2: - Schematic of a Negative Feedback System.**

• Rec

- ✓ Because of the phase relationship between the signals  $x_i$  and  $x_f$  as shown in the figure we have,

$$x_d = x_i - x_f$$

$$\therefore x_i = x_d + x_f$$

- ✓ The signal  $x_d$  is the input signal for the amplifier section. The amplifier gain is 'A'.
- ✓ The feed back component of signal  $x_f$  is generated by the Feedback Network from the sampled output signal  $x_o$ . The feedback network has a gain given by ' $\beta$ '.

Thus  $x_o = A x_d$

$$x_f = \beta x_o = \beta A x_d$$

Now, considering the complete system, the overall gain is

$$A_f = \frac{x_o}{x_i}$$

Substituting

$$A_f = \frac{A x_d}{x_d + x_f}$$

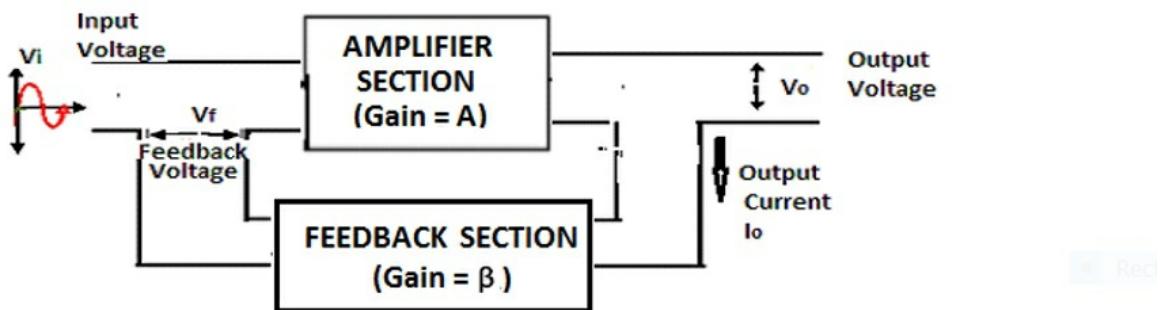
$$A_f = \frac{A x_d}{x_d(1 + \beta A)}$$

Thus, the overall gain of the Negative Feedback system is

$$| \quad \underline{A_f} = \frac{A}{(1 + \beta A)} \quad \dots(1)$$

### Type of Negative Feedback Systems

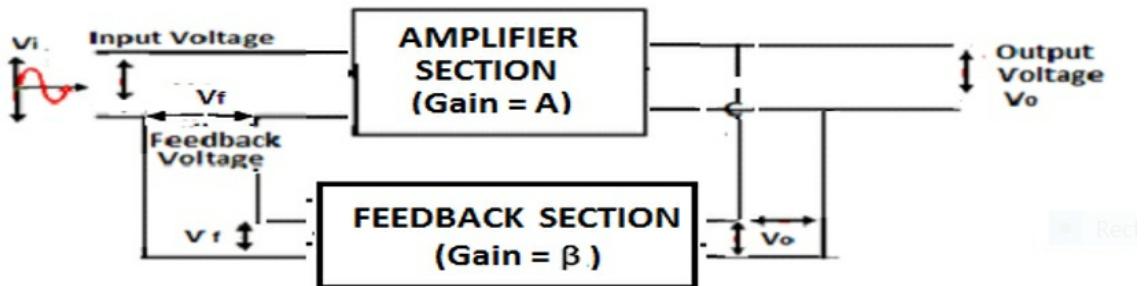
1. **Current Series Feedback** :- In this type of feedback system, the output current is sampled and the quantity fed back is a voltage  $V_f$ , which is generated by the Feedback Network in such a way that it is proportional to the sampled current. This quantity  $V_f$  is fed back in series. The schematic is shown in the figure below.



**Fig.- 3:** - Schematic of Current – Series Negative Feedback System.

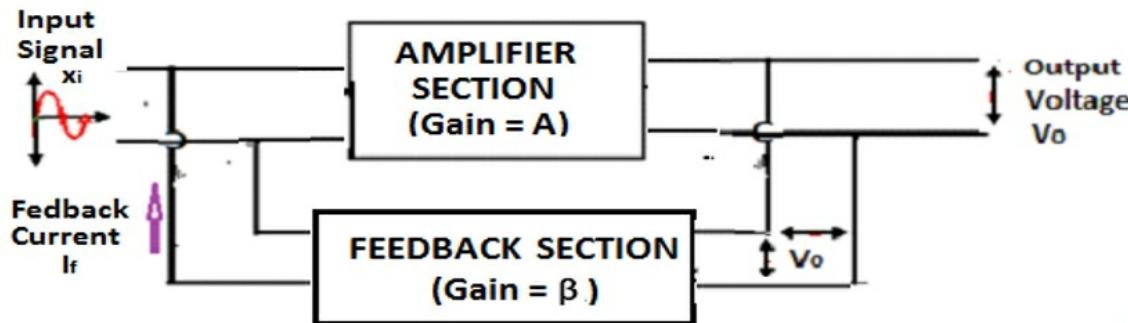
2. **Voltage-Series Feedback** :- In this type of feedback system,

the output voltage is sampled. The quantity fed back is a voltage  $V_f$ , proportional to the sampled voltage, which is generated by the Feedback Network and is fed back in series. The schematic is shown in the figure below.



**Fig.- 4:** - Schematic of Voltage – Series Negative Feedback System.

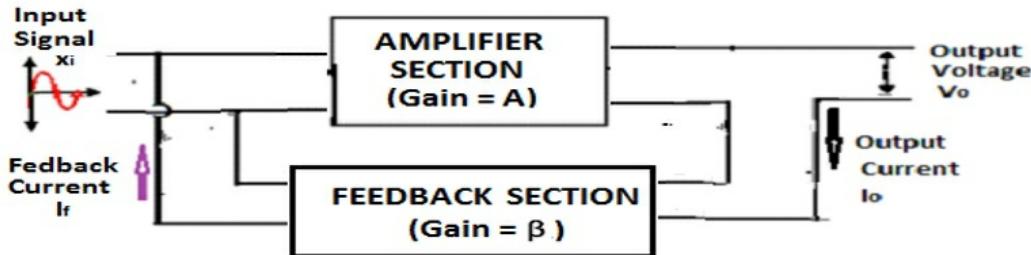
3. **Voltage-Shunt Feedback** :- In this type of feedback system, the output voltage is sampled. The quantity fed back is a current  $I_f$ , which is generated by the Feedback Network in such a way that it is proportional to the sampled voltage. The current  $I_f$  is fed back in shunt (parallel) at the input point. The schematic is shown in the figure below.



**Fig.- 5:** - Schematic of Voltage– Shunt Negative Feedback System.

4. **Current-Shunt Feedback** :- In this type of feedback system, the output voltage is sampled. The quantity fed back is a current, proportional to the sampled voltage, which is generated by the Feedback Network and is fed back in shunt (parallel) at the input

point. The schematic is shown in the figure below.



**Fig.- 6:** - Schematic of Current – Shunt Negative Feedback System.

## 9.6 Advantages of Negative Feedback Systems

The general analysis of a Negative Feedback system is given in the previous section shows that the quantity “Overall Gain With Feedback”, given by Eq. (1) is

$$A_f = \frac{A}{(1 + \beta A)}$$

Thus, the overall gain of the feedback system  $A_f'$  is less than that of the basic amplifier ( $A$ ).

This obvious disadvantage is offset by some very important improvements in the performance of an amplifier when it is operating with Negative Feedback. These points are analyzed below.

1. **Stability of operation** :- We had seen that the various performance characteristics of an amplifier is a function of its internal parameters,( h-parameters or r-parameters, in case of BJT and  $g_m$ -parameter in case of JFET. These internal parameters are highly temperature dependent. Thus, **the performance characteristics of the basic amplifier is also temperature dependent.**

Gain of an amplifier with negative feedback is given by Eq. 1 as

$$A_f = \frac{A}{(1 + \beta A)}$$

Taking the first derivative of this expression we get the rate of change of gain of the negative feedback system as

$$\frac{dA_f}{A_f} = \frac{1}{(1 + \beta A)} \frac{dA}{A} \quad \dots(2)$$

**The expression 2 shows that the rate of change of gain of a negative feedback system caused by any environmental factor is reduced by a quantity  $(1 + \beta A)$  w.r.t. that without feedback. In other words, the gain of a negative feedback system tends to get stabilized.**

This can be understood in another way.

Consider a negative feedback system where

$$\beta A \gg 1$$

$$\therefore A_f \approx \frac{1}{\beta} \quad \dots(3)$$

Where  $\beta$  is the gain of the feedback network.

If we construct the feedback network with components whose characteristics are stable w.r.t. temperature variations, the gain of the entire feedback system will also be stable w.r.t. temperature.

In fact Passive Components such as Resistance, Capacitors and Inductors have fairly stable characteristics w.r.t. temperature variations. Hence, the feedback network is composed of such passive elements in order to make the gain of the system stable.

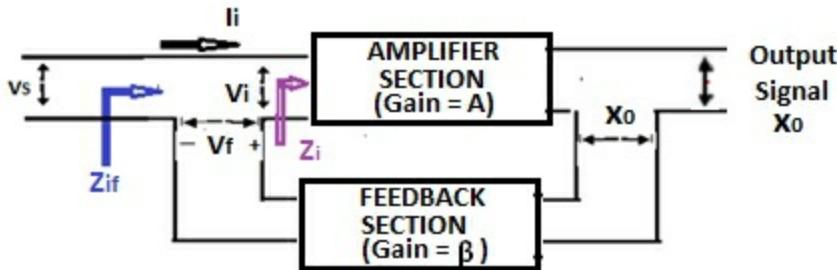
2. **Increase in Input Impedance with Series Feedback** :- Input impedance of an amplifier can be increased when a negative feedback system is employed, with the feedback quantity being a voltage applied in series. Consider the input section of a Current –Series Negative Feedback system depicted in Fig 3. This is reproduced below.

For the Basic Amplifier input impedance is

$$Z_i = \frac{V_i}{I_i}$$

Whereas, for the system with feedback, the overall input impedance is

$$Z_{if} = \frac{V_s}{I_i}$$



Since feedback is in series, we have

$$V_s = V_i + V_f$$

The feedback quantity is generated by the feedback network. This has a gain of ' $\beta$ '

$$\text{Hence } V_f = \beta V_o$$

The Basic Amplifier has a gain of 'A'. Hence output voltage is given by

$$V_o = A V_i$$

Hence

$$V_f = \beta A V_i$$

Rearranging and substituting in the expression for  $Z_{if}$  we have

$$Z_{if} = \frac{V_i (1 + \beta A)}{I_i}$$

$$\text{Where } \frac{V_i}{I_i} = Z_i$$

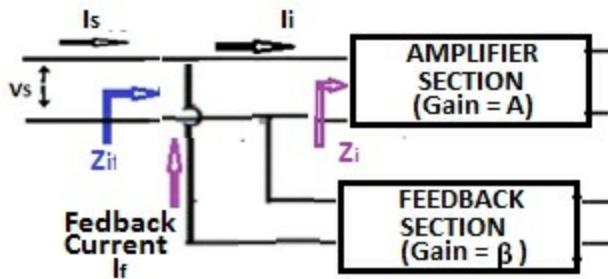
Thus

$$Z_{if} = Z_i (1 + \beta A) \dots (4)$$

**The expression given by 4 shows that the Input impedance of a feedback system with Series Feedback increases by a factor of  $(1 + \beta A)$ .**

### 3. Decrease in Input Impedance with Shunt Feedback :- Input

impedance of an amplifier can be decreased when a negative feedback system is employed, with the feedback quantity being a current appearing in shunt (in parallel to) with the input current. Consider the input section of a Current –Shunt Negative Feedback system depicted in Fig 6. This is reproduced below.



For the Basic Amplifier input impedance is

$$Z_i = \frac{V_s}{I_i}$$

Whereas, for the system with feedback, the overall input impedance is

$$Z_{if} = \frac{V_s}{I_s}$$

Where

$$I_s = I_i + I_f$$

$$\text{Where } I_f = \beta I_o \quad \& \quad I_o = A I_i$$

Substituting in the expression for  $Z_{if}$  we have

$$Z_{if} = \frac{V_s}{I_i(1 + \beta A)}$$

Where

$$\frac{V_s}{I_i} = Z_i$$

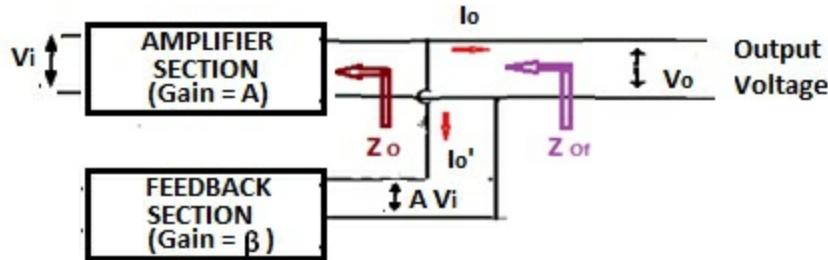
Thus

$$Z_{if} = \frac{Z_i}{(1 + \beta A)} \quad \dots(5)$$

The expression given by 9.5 shows that the Input impedance of a feedback system with Shunt Feedback decreases by a factor of  $(1 + \beta A)$ .

#### 4. Decrease in Output Impedance when output voltage is

**sampled**:- Output impedance of an amplifier can be decreased when a negative feedback system is employed, with the sampled quantity being the output voltage. Consider the output section of a Voltage–Shunt Negative Feedback system depicted in Fig 5. This is reproduced below.



Output impedance of an amplifier is determined by open circuiting the source as well as the load.

Hence

$$V_s = 0.$$

We had

$$V_s = V_i + V_f$$

$$\therefore V_i = -V_f = -\beta V_o$$

The current flowing into the feedback network is  $I_o'$  , given by

$$I_o' = \frac{V_o - A V_i}{Z_o}$$

Substituting and simplifying

$$I_o' = \frac{V_o(1 + \beta A)}{Z_o}$$

The overall Output Impedance of the amplifier with the feedback system is given by

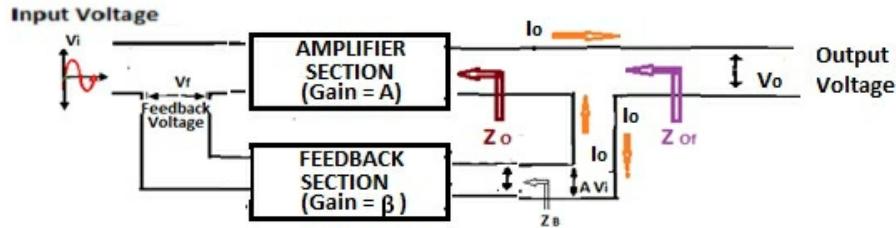
$$Z_{of} = \frac{V_o}{I_o'}$$

Substituting and simplifying we have

$$Z_{of} = \frac{Z_o}{(1 + \beta A)} \quad \underline{\dots(6)}$$

**The expression given by 6 shows that the Output impedance of a feedback system where output voltage is sampled, is decreased by a factor of  $(1 + \beta A)$ .**

5. **Increase in Output Impedance when output current is sampled** :- Consider the output section of a Current-Series Negative Feedback system depicted in Fig 3. This is reproduced below.



The KVL equation of the output side of the feedback amplifier is

$$V_o = I_o Z_{of} + I_o Z_B$$

Where  $Z_B$  is the impedance of the feedback network and is given by

$$Z_B = \frac{A V_i}{I_o}$$

With  $V_i = -V_f = -\beta V_o$  we have

$$V_o = I_o Z_{of} - A \beta V_o$$

$$\therefore I_o Z_{of} = V_o (1 + A \beta)$$

$$\therefore Z_{of} = \frac{V_o (1 + A \beta)}{I_o}$$

Where

$$\frac{V_o}{I_o} = Z_o$$

$$\therefore Z_{of} = Z_o (1 + A \beta) \quad \dots(7)$$

The expression given by 7 shows that the Output impedance of a feedback system where output current is sampled, is increased by a factor of  $(1 + \beta A)$ .

6. **Increase in Band Width** :- The band width of an amplifier is the range of frequencies in which the amplifier has a constant gain.

The Band Width of an amplifier increases when a negative feedback of any configuration is employed. This is proven as follows. We had analyzed the RC Coupled amplifier in the previous chapter. Gain of an RC Coupled amplifier at low frequencies is denoted by  $A_L$  and that at high frequencies is denoted by  $A_H$ . These are respectively given by the following expressions.

$$A_L = \frac{A}{1 - j \left( \frac{f_L}{f} \right)}$$

$$A_H = \frac{A}{1 + j \left( \frac{f}{f_H} \right)}$$

Band Width of the amplifier is defined as the range of frequencies between  $f_L$  and  $f_H$ , between which the gain remains within the maximum value and  $1/\sqrt{2}$  times the maximum value.

When Negative Feedback is employed, the gain of the amplifier is reduced by the factor  $(1 + \beta A)$  as shown by Eq. 1. Thus the quantities  $A_L$  and  $A_H$  will also be reduced due to feedback and be given by

$$A_{Lf} = \frac{A_L}{1 + \beta A_L} \quad \& \quad A_{Hf} = \frac{A_H}{1 + \beta A_H}$$

Substituting and simplifying we have,

$$A_{Lf} = \frac{\frac{A}{1 - j \left( \frac{f_L}{f} \right)}}{1 + \left( \frac{\beta A}{1 - j \left( \frac{f_L}{f} \right)} \right)} = \frac{A / \left\{ 1 - j \left( \frac{f_L}{f} \right) \right\}}{\left[ \left\{ 1 - j \left( \frac{f_L}{f} \right) \right\} + \beta A \right] / \left\{ 1 - j \left( \frac{f_L}{f} \right) \right\}}$$

$$A_{Lf} = \frac{A}{(1 + \beta A) - j \left( \frac{f_L}{f} \right)}$$

Dividing throughout by  $(1 + \beta A)$  we have

$$\underline{A_{Lf}} = \frac{A / (1 + \beta A)}{1 - j \left\{ f_L / f (1 + \beta A) \right\}}$$

---

In this the numerator is the gain of the negative feedback system as expressed by Eq. 1 as ' $A_f$ '. We can denote the low frequency cut-off

point of the negative feedback system as

$$f_{Lf} = \frac{f_L}{(1 + \beta A)} \quad \dots(8)$$

Using this the Low Frequency gain of the negative feedback system is

$$A_{Lf} = \left\{ \frac{A_f}{1 - j \left( \frac{f_{Lf}}{f} \right)} \right\} \quad \dots(9)$$

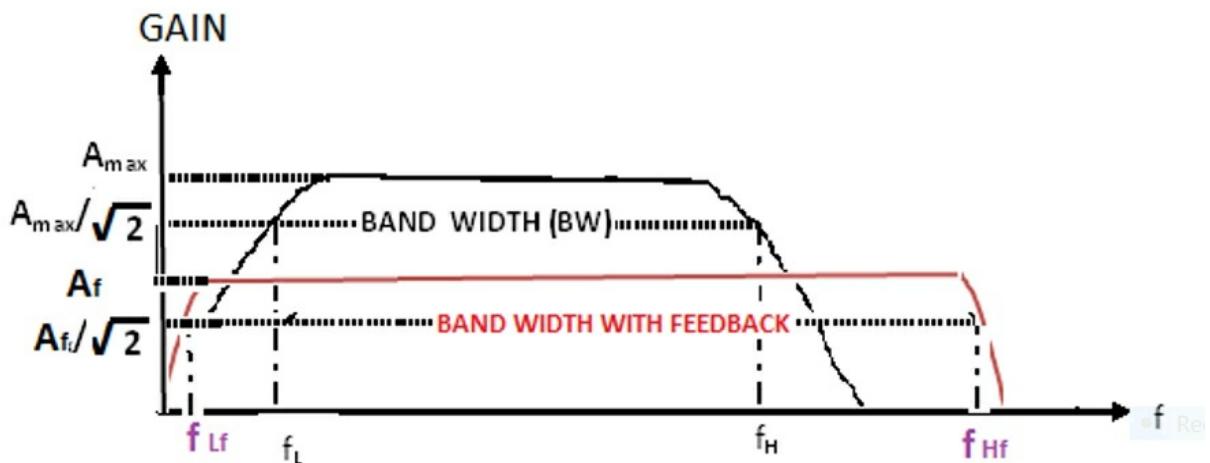
Proceeding in a similar way we can derive the high frequency cut-off point of the negative feedback system as

$$f_{Hf} = f_H (1 + \beta A) \quad \dots(10)$$

And High Frequency gain of the negative feedback system is

$$| \quad A_{Hf} = \left\{ \frac{A_f}{1 + j \left( \frac{f}{f_{Hf}} \right)} \right\} \quad \dots(11)$$

The expressions 8 and 10 show that, while the ‘Low Frequency cut-off point’ of a negative feedback system is decreased by a factor of  $(1 + \beta A)$ , the ‘High Frequency cut-off point’ of a negative feedback system is increased by the same factor of  $(1 + \beta A)$ . In other words, the Band Width of the negative feedback system is increased by the factor  $(1 + \beta A)$ . This increase in Band Width is associated with a corresponding decrease in gain (as given by Eq.1). This is depicted in the figure below.



**Fig.- 7: - Increase in Band Width of a Negative Feedback System.**

**G. Reduction of Noise and Distortion** :– There exist various sources of electromagnetic radiation in our environment. These include various industrial processes such as arc welding, switching of current in various applications, current flow across P–N junctions and certain natural causes such as lightning. All these produce randomly radiating electromagnetic waves. Whenever these come in contact with any electrical or electronic circuit, a current is induced. This current superimposes over the signal being processed by the circuit. In case of an audio system these disturbances will appear as random noise. In fact any electromagnetic disturbance on a signal in any electrical or electronic system is called Electrical Noise. In various electrical and electronic systems, noise gives rise to error.

Quite often various electrical devices distort the shape of the signal being processed. One of the most common causes of distortion is signal clipping. Whenever a signal is distorted, various harmonic components come into existence. The characteristic of harmonic components is that higher order harmonics have progressively decreasing amplitudes. Thus only some of the lower order harmonics play a significant role in signal distortion. Particularly harmful is the Second Harmonic. The second harmonic has a frequency twice that of the signal and an amplitude just slightly less than that of the fundamental. There are certain methods by means of which the even harmonics can be eliminated. But the

higher order odd harmonics are difficult to eliminate.

We had seen earlier that the gain of a system applied with negative feedback reduces by a factor  $1/(1 + \beta A)$ , as shown by Eq.9.1. This is applicable to all signals including Noise and Higher Order Odd Harmonics.

**Table 9.1 :: Advantages of Negative Feedback**

QUANTITY		TYPE OF FEEDBACK SCHEME			
		Voltage-Series	Current-Series	Current-Shunt	Voltage-Shunt
A	$Z_{of}$	Decreases	Increases	Increases	Decreases
B	$Z_{if}$	Increases	Increases	Decreases	Decreases
C	Stability of	Voltage Gain $A_{vf} = \frac{V_o}{V_i}$ Gain $G_{mf} = \frac{I_o}{V_i}$	Trans Conductance Gain $G_{mf} = \frac{I_o}{V_i}$	Current Gain $A_{lf} = \frac{I_o}{I_i}$	Trans Resistance Gain $R_{mf} = \frac{V_o}{I_i}$
D	Improvement in Characteristic of	Voltage Amplifier e.g. Common Collector Amplifier	Trans-conductance Amplifier e.g. JFET amplifier	Current Amplifier e.g. Common Base Amplifier	Trans Resistance Amplifier e.g. CE Amplifier with Collector Feedback.
E	Band Width	Increases	Increases	Increases	Increases
F	Noise	Decreases	Decreases	Decreases	Decreases
G	Distortion	Decreases	Decreases	Decreases	Decreases

**Both Noise and Harmonic Distortions is reduced by a factor  $1/(1 + \beta A)$  when negative feedback is employed.**

The various advantages of Negative Feedback Systems are summarized and tabulated as above.

### TUTORIAL

**Example. 1 :-** In a negative feedback system the basic amplifier has a gain of 600 and the upper cut-off frequency is 15 kHz, while the

*overall gain of the system is 30. Calculate the upper cut-off frequency. If the input signal has a 10% harmonic component, calculate the harmonic content at the output of the feedback amplifier.*

**SOLUTION :-**

The gain of a negative feedback system is given by Eq. 1 as

$$A_f = \frac{A}{(1 + \beta A)}$$

Where  $A_f = 600$  and  $A = 30$

From this

$$\beta = \frac{A - A_f}{A \cdot A_f}$$

Substituting

$$\beta = \frac{600 - 30}{600 \cdot 30} = 0.032$$

Upper cut-off frequency of the basic amplifier is  $f_H = 15$  kHz

$\therefore$  Upper cut-off frequency of the feedback system, given by Eq. 10 is

$$f_{Hf} = (1 + \beta A) f_H = (1 + 0.032 \times 600) \times 15 = 303 \text{ kHz.}$$

As given by point (G) in section 2,

Harmonic Distortion is reduced by a factor

$$1 / (1 + \beta A)$$

$\therefore$  Harmonic Distortion at the output of the feedback system is

$$D_f = \frac{D}{(1 + \beta A)} = \frac{10 \%}{(1 + 0.032 \times 600)} = 0.495 \%$$

**Example. 2 :-** The Open Loop gain of a Voltage-Series negative feedback amplifier is 100000 and the feedback factor is 0.001. If the open loop input and output impedances are 1 kΩ and 84 kΩ respectively, calculate the input and output impedances of the feedback

system. If the open loop gain changes by  $\pm 25\%$  due to instability, calculate the change in the closed loop gain.

**SOLUTION :-**

For series feedback the input impedance is given by Eq. 4 as

$$Z_{if} = Z_i(1 + \beta A)$$

$$\text{Given } Z_i = 1 \text{ k}\Omega, \quad A = 100000\beta = 0.001$$

$$\therefore Z_{if} = 1 \times (1 + 0.001 \times 100000) = 101 \text{ k}\Omega$$

For voltage as sampled quantity the output impedance is given by Eq. 6 as

$$Z_{of} = \frac{Z_o}{(1 + \beta A)} \quad \underline{\text{Given } Z_o = 84 \text{ k}\Omega}$$

$$\therefore Z_{of} = \frac{84000}{(1 + 0.001 \times 100000)} = 831.68 \Omega$$

Stability of gain is given by Eq. 2 as

$$\frac{dA_f}{A_f} = \frac{1}{(1 + \beta A)} \frac{dA}{A}$$

Given that, in the open loop the rate of change of gain is 25 %

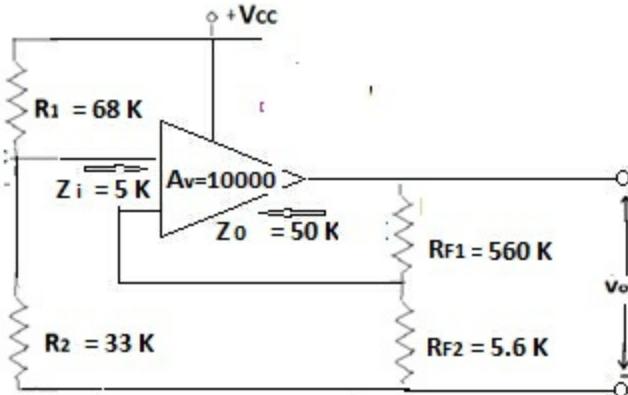
$$\frac{dA}{A} = 0.25$$

$\therefore$  Rate if change of gain in Closed Loop is

$$\frac{dA_f}{A_f} = 0.25 \times \frac{1}{(1 + 0.001 \times 100000)} = 0.00247 \approx 0.0025$$

Thus with feedback the change in gain is as low as 0.025 %

**Example. 3 :-** The Voltage-Series Negative feedback system shown in the figure uses an open-loop gain of 10000, input impedance of 5 K and output impedance of 25 K. Calculate Closed -Loop Gain, input Impedance and Output Impedance.



### SOLUTION ::

From the figure, the Feedback Ratio is

$$\beta = \frac{R_{F2}}{R_{F1} + R_{F2}} = \frac{5.6}{560 + 5.6} = 0.0099$$

Closed Loop Gain is

$$A_{CL} = A_F = \frac{A_v}{(1 + \beta A_v)} = \frac{10000}{(1 + 0.0099 \times 10000)} = 100$$

Closed Loop input impedance is

$$Z_{ICL} = Z_{IF} = Z_i (1 + \beta A_v)$$

$$Z_{ICL} = 5 (1 + 0.0099 \times 10000) = 500 \text{ K}$$

Closed Loop Output Impedance is

$$Z_{OCL} = Z_{OF} = \frac{Z_o}{(1 + \beta A_v)}$$

$$Z_{OCL} = \frac{25}{(1 + 0.0099 \times 10000)} = 0.25 \text{ K} = 250 \Omega$$

Rectangular Snip

## 9.7 Current-Series Negative Feedback Amplifier

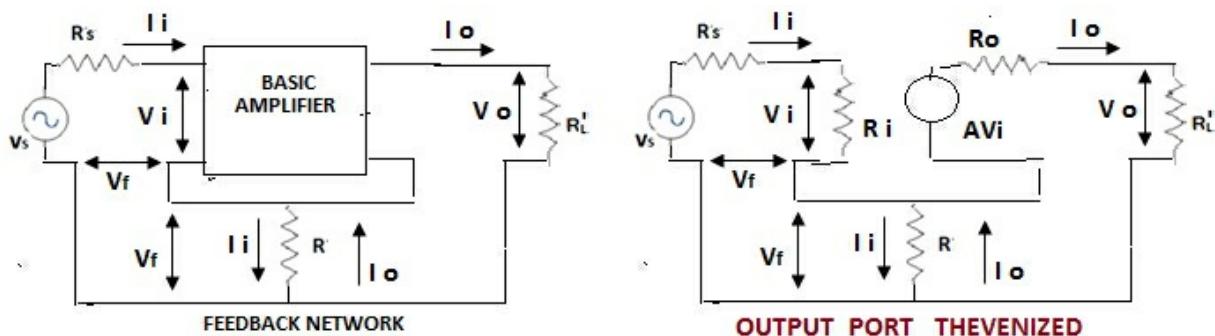
- Current-Series Negative Feedback is employed to improve **the transconductance gain** of an amplifier. Transconductance Gain refers to the “Ratio of Output Current to Input Voltage”. This is , in fact, a very important parameter for an amplifier, since the Input Signal is best represented as a Voltage Source, rather than a

Current Source.

- It also converts a voltage amplifier into a transconductance amplifier.
- **A Common Emitter amplifier with an Emitter Swamping resistance** is an example of a Current-Series Negative Feedback amplifier.
- Consider the schematic of the Current-Series Negative Feedback amplifier, shown in the Fig.-8 below. In this it is shown that the output current is sampled by a resistance R. This resistance constitutes the feedback network. The sampled output current produces a voltage drop  $V_f$  across the resistance R and this voltage is fed back in series at the input point.
- For the purpose of analysis, the input port is replaced with the input resistance  $R_i$  and the output port is Thevenized as a voltage source in series with a resistance. The voltage source has a value  $V_0$ , where

$$V_0 = A V_i$$

where 'A' is the open-loop voltage gain of the basic amplifier.



**Fig. 8 :- Schematic of Current-Series Negative Feedback amplifier. Feedback network consist of a single resistor. Feedback voltage  $V_f$  is proportional to the sampled output current.**

- Feedback voltage is the voltage developed across R due to the currents  $I_i$  and  $I_o$ . Since  $I_i$  and  $I_o$  flow in opposite directions, thus

$$V_f = (I_i - I_o) R$$

- In a transistor output current is  $I_C$  and input current is  $I_B$ . Since the base current is negligible compared to the collector current, we can take

$$V_f = -I_o R$$

Hence the Feed Back Ratio is

$$\beta = \frac{V_f}{I_o} = -R \quad \dots(12)$$

The KVL equation at the output port is

$$V_o = A V_i + I_i R - I_o (R_o + R)$$

At the input port  $V_i = I_i R$

$$\therefore V_o = (A R_i + R) I_i - I_o (R_o + R) \dots(13)$$

- Output Impedance**

The KVL equation at the input port is

$$V_s = I_i (R_s + R_i + R) - I_o R$$

$$\therefore I_i = \frac{V_s + I_o R}{(R_s + R_i + R)} \quad \dots(14)$$

Substituting in the expression for  $V_o$  above we have

$$V_o = \frac{(A R_i + R)(V_s + I_o R)}{(R_s + R_i + R)} - I_o (R + R_o)$$

Rearranging, we have

$$V_o = \frac{(A R_i + R)}{(R_s + R_i + R)} V_s + \frac{(A R_i + R)}{(R_s + R_i + R)} I_o R - I_o (R + R_o)$$

In this expression, the coefficient of the first and second terms is the voltage gain of the amplifier when the source resistance is taken into consideration. In other words,

$$A_{vs} = \frac{(A R_i + R)}{(R_s + R_i + R)} \quad \dots(15)$$

$$\therefore V_o = A_{vs} V_s + A_{vs} I_o R - I_o (R + R_o)$$

$$V_o = A_{vs} V_s - I_o (R_o + R(1 - A_{vs}))$$

In this expression, the quantity within the brackets represent an impedance which reduces the output voltage. Hence this is the output impedance of the amplifier with the feedback system

$$Z_{of} = (R_o + R(1 - A_{vs})) \dots (16)$$

$$\therefore V_o = A_{vs} V_s - I_o Z_{of}$$

- Transconductance Gain**

Output voltage also equals the voltage drop across the load resistance

$$V_o = I_o R_L$$

Substituting we have

$$A_{vs} V_s = I_o (R_L + Z_{of})$$

$$\therefore I_o = \frac{A_{vs} V_s}{(R_L + Z_{of})} \dots (17)$$

From this we get the Trans Conductance Gain of the amplifier as

$$G_{mf} = \frac{I_o}{V_s} = \frac{A_{vs}}{(R_L + Z_{of})}$$

Substituting for Z<sub>of</sub> we have

$$G_{mf} = \frac{A_{vs}}{(R_L + R_o + (R(1 - A_{vs})))}$$

$$\text{Rearranging } G_{mf} = \frac{A_{vs}}{(R_L + R_o + R) - R A_{vs}}$$

Using expression 12 where the quantity (- R) = β, where 'β' is the Feedback Ratio, we get

$$G_{mf} = \frac{A_{vs}}{(R_L + R_o + R) - \beta A_{vs}}$$

In general, in case of an amplifier the open loop gain A<sub>vs</sub> is quite large. Thus we can take

$$(R_L + R_o + R) \ll \beta A_{vs}$$

$$\therefore G_{mf} \approx 1/\beta = - \frac{1}{R} \dots (18)$$

The expression 18 shows that the Transconductance Gain of the

amplifier is independent of signal frequency and h-parameter values.  
**Hence it is stabilized.**

- **Voltage Gain**

Voltage Gain of the feedback system is given by

$$A_{vf} = \frac{V_o}{V_s}$$

Where  $V_o = I_o R_L$  &  $V_s = I_o / G_{mf}$

$$V_s = I_o \cdot (-R)$$

Substituting

$$A_{vf} = \frac{I_o \cdot R_L}{-I_o R}$$

Or  $A_{vf} = -\frac{R_L}{R}$  ....(19)

- The expression 19 shows that the Voltage Gain of the amplifier is independent of signal frequency and h-parameter values. Hence it is stabilized.

- **Input Impedance**

The Input Impedance of the feedback system is given by

$$Z_{if} = \frac{V_s}{I_i} - R_s$$

Input Current  $I_i$  is given by Eq. 14 as

$$I_i = \frac{V_s + I_o R}{(R_s + R_i + R)}$$

$$\therefore R_s + R_i + R = \frac{V_s}{I_i} + \frac{I_o \cdot R}{I_i}$$

But the expression  $\frac{I_o}{I_i}$  gives the Current gain  $A_I$  of the amplifier.

Substituting and rearranging, we have

$$\frac{V_s}{I_i} = R_s + R_i + R - A_I R$$

Using this in the expression for  $Z_{if}$  we have

$$Z_{if} = \cancel{R_s} + R_i + R - \underline{A_I R} - \cancel{R_s}$$

$$\therefore Z_{if} = R_i + R (1 - A_I) \dots (20)$$

### Example of Current-Series Feedback

- ✓ The Common Emitter amplifier with the emitter swamping resistance is an example of Current-Series negative feedback amplifier. The circuit of the CE Amplifier with emitter swamping resistance is shown in the Fig.9 below. This was analyzed in Chapter-II with both r-parameter model as well as with h-parameter model.
- ✓ This is now being analyzed as a Current-Series negative feedback amplifier and it will be seen that we obtain the same results as we got in Chapter-II.
- ✓ The transistor is replaced with the simplified h-parameter equivalent circuit and modified and rearranged for the purpose of analysis, as follows.

1. The voltage source  $h_{re} v_{CE}$  is neglected.
2. The Norton's equivalent at the collector terminal is replaced with a Thevenin's equivalent by converting the current source  $h_{fe} i_B$  into an equivalent Thevenin's voltage source  $(h_{fe} i_B)$

- / $h_{oe}$ ) ; where  $i_B = I_i = v_i /h_{ie}$
3. The shunt admittance  $h_{oe}$  is replaced by a series resistance  $1/h_{oe}$ .
- ✓ The Emitter Swamping resistance ' $r_E$ ' constitutes the Feedback Network. The output current of a transistor is  $i_C$ , and this is approximately equal to the Emitter Current  $i_E$ . This current flows through the resistance ' $r_E$ '. Thus this process samples the output current and produces the feedback quantity  $v_f$ .
  - ✓ The feedback voltage appears in series with the source voltage  $v_s$  in opposite polarity. Hence the feedback system is a current-series negative feedback system.

### **Input Impedance**

In this case

$$R_i = h_{ie} ; \quad R = r_E \quad \& \quad A_I = (-h_{fe})$$

Substituting these in the expression for  $Z_{if}$  given by Eq. 20, we have

$$Z_{if} = h_{ie} + r_E (1 + h_{fe}) \dots(21)$$

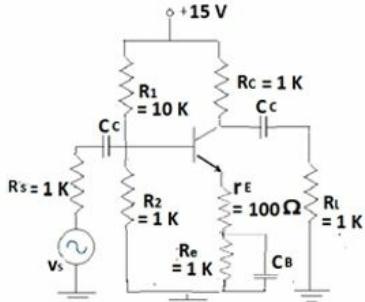
### **Voltage Gain**

We had the expression for voltage gain with source impedance given by Eq. 15 as

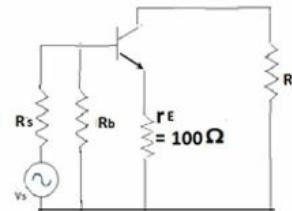
$$A_{vs} = \frac{(A R_i + R)}{(R_s + R_i + R)}$$

Where 'A' is the Voltage Gain of the Basic Amplifier. From the figure,

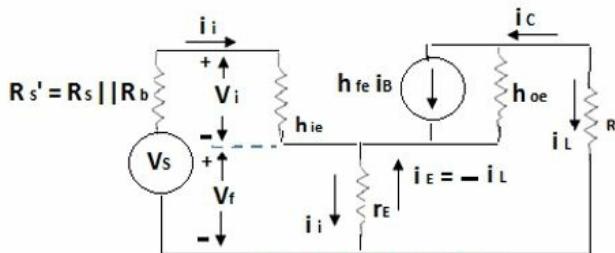
$$A = \frac{-h_{fe}}{h_{oe} \cdot h_{ie}}$$



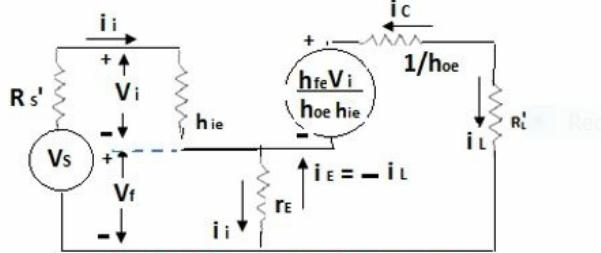
AMPLIFIER WITH  
EMITTER SWAMPING RESISTANCE ' $r_E$ '



AC EQUIVALENT CIRCUIT



TRANSISTOR REPLACED BY  
SIMPLIFIED  $h$ -parameter model



NORTON'S EQUIVALENT AT COLLECTOR  
REPLACED BY THEVENIN'S EQUIVALENT

$$(V_T = h_{fe} i_B / h_{oe} \text{ & } R_T = 1 / h_{oe} \text{ with } i_B = V_i / h_{ie})$$

**Fig. 9:** – The Common Emitter Amplifier with Emitter Swamping Resistance can be analyzed as a Current-Series negative feedback amplifier.

Substituting for  $R_i$  and  $R$  for the CE amplifier from above we have

$$A_{vs} = \frac{\frac{-h_{fe}}{h_{oe}} + r_E}{(R_s + h_{ie} + r_E)}$$

$$A_{vs} = \left[ \frac{\left\{ \frac{1}{h_{oe}} (h_{oe} r_E - h_{fe}) \right\}}{(R_s + h_{ie} + r_E)} \right]$$

$$A_{vs} = \frac{(h_{oe} r_E - h_{fe})}{h_{oe}(R_s + h_{ie} + r_E)}$$

Substituting  $A_{vs}$  in the expression for output current  $I_o$  given by Eq. 17 and using the expression for  $Z_{of}$  given by Eq. 16, in which,  $R_o = 1/h_{oe}$ , we have

$$I_o = \frac{A_{vs} V_s}{(R_L + R_o + r_E (1 - A_{vs}))}$$

$$= \frac{A_{vs} V_s}{(R_L + \frac{1}{h_{oe}} + r_E (1 - A_{vs}))}$$

$$I_o = \frac{\left\{ \frac{(h_{oe} r_E - h_{fe})}{h_{oe}(R_s + h_{ie} + r_E)} \right\} V_s}{R_L + \frac{1}{h_{oe}} + r_E \left( 1 - \left\{ \frac{(h_{oe} r_E - h_{fe})}{h_{oe}(R_s + h_{ie} + r_E)} \right\} \right)}$$

$$I_o = \frac{\frac{1}{h_{oe}} \left( \frac{(h_{oe} r_E - h_{fe})}{(R_s + h_{ie} + r_E)} \right) V_s}{\frac{1}{h_{oe}} \left( \frac{(R_L h_{oe} + 1)(R_s + h_{ie} + r_E) + r_E(h_{oe}(R_s + h_{ie} + r_E)) - R_s h_{oe} - h_{fe}}{(R_s + h_{ie} + r_E)} \right)}$$

$$I_o = \frac{(h_{oe} r_E - h_{fe}) V_s}{((R_L h_{oe} + r_E h_{oe} + 1)(R_s + h_{ie} + r_E) - r_E(r_E h_{oe} - h_{fe}))}$$

$$I_o = \frac{(h_{oe} r_E - h_{fe}) V_s}{(h_{oe}(R_L + r_E) + 1)(R_s + h_{ie} + r_E) - r_E(r_E h_{oe} - h_{fe})}$$

In this expression we can make the following approximations

$$h_{oe}(R_L + r_E) \ll 1 \quad \& \quad h_{fe} r_E \gg (R_s + h_{ie} + r_E)$$

$$\therefore I_o = \frac{-h_{fe} V_s}{(R_s + h_{ie} + r_E) + h_{fe} r_E}$$

Neglecting  $(R_s + h_{ie} + r_E)$  w.r.t.  $h_{fe} r_E$

$$I_o \approx \frac{-V_s}{r_E}$$

$$\therefore V_s = -I_o r_E$$

$$\text{We had } V_o = I_o R_L$$

Thus Voltage Gain of the amplifier is

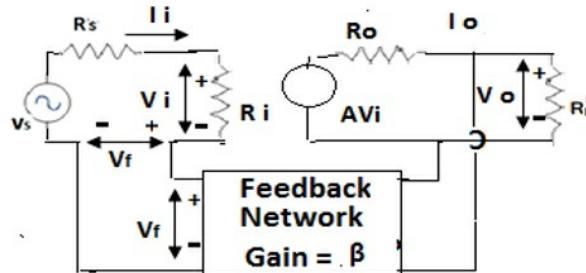
$$A_{vf} = -\frac{R_L}{r_E} \quad \underline{\dots}(22)$$

This is the same expression as we had derived for the CE amplifier with the Emitter Swamping Resistance when we used  $r$ -parameter analysis as well as  $h$ -parameter analysis.

## 9.8 Voltage-Series Negative Feedback Amplifier

- ❖ **Voltage-Series Negative Feedback is employed to improve the performance of a voltage amplifier and to convert BJT current amplifiers into voltage amplifiers.**
- ❖ A Common Collector amplifier, which is also known as an Emitter Follower, is an example of a Voltage-Series Negative Feedback amplifier.
- ❖ Consider the general schematic of the Voltage-Series Negative Feedback amplifier, shown in the Fig.-10 below. In this it is shown that the output voltage is sampled by a feedback network and converted into a voltage  $V_f$ , which is fed back in series at the input point.
- ❖ For the purpose of analysis, the input port is replaced with the input resistance  $R_i$  and the output port is Thevenized as a voltage source  $A V_i$ , in series with a resistance  $R_o$ .

- The input impedance and the output impedance of the feedback system are shown as  $Z_{if}$  and  $Z_{of}$  respectively.



IN THE BASIC AMPLIFIER THE INPUT PORT IS  
REPLACED BY THE INTERNAL RESISTANCE  $R_i$  AND THE  
OUTPUT PORT IS THEVENIZED AS THE SERIES  
COMBINATION OF THE VOLTAGE  $AV_i$  AND THE  
RESISTANCE  $R_o$

**Fig. 10: – The Schematic of the Voltage-Series Negative Feedback Amplifier.**

- The effects of the resistances  $R_o$  at the output and  $R_i$  at the input are to reduce the respective voltages at the output and input ports as follows.

$$V_o = A V_i - R_o I_o (a)$$

$$V_i = \frac{R_s}{(R_i + R_s)} (V_s - V_f) = \frac{R_s}{(R_i + R_s)} (V_s - \beta V_o)$$

- Substituting for  $V_i$  in the expression for  $V_o$  we get

$$V_o = \left( \frac{A R_i}{(R_i + R_s)} \right) (V_s - \beta V_o) - I_o R_o$$

$$\text{Or } V_o = \left( \frac{A R_i}{(R_i + R_s)} \right) V_s - \beta \left( \frac{A R_i}{(R_i + R_s)} \right) V_o - I_o R_o$$

- In this expression the term within the brackets represent the Voltage Gain of the feedback system with consideration of the source resistance.

$$\therefore \frac{A R_i}{(R_i + R_s)} = A_{vs}$$

Substituting and rearranging we have

$$V_o (1 + \beta A_{vs}) = A_{vs} V_s - I_o R_o$$

$$\therefore V_o = \frac{A_{vs}}{(1 + \beta A_{vs})} V_s - \frac{R_s}{(1 + \beta A_{vs})} I_o \quad \underline{\text{(b)}}$$

- The expression represented by Eq. (a) gives the output voltage of the basic amplifier and the Eq. (b) gives the output voltage with Voltage-Series negative feedback. If we compare the coefficients of the variables for the Input Voltage and Output Current of the two circuits, we get that

1. Voltage Gain of the feedback amplifier is

$$A_{vf} = \frac{A_{vs}}{(1 + \beta A_{vs})} \quad \underline{\text{....(23)}}$$

ii. Output Impedance of the feedback amplifier is

$$Z_{of} = \frac{R_s}{(1 + \beta A_{vs})} \quad \underline{\text{....(24)}}$$

iii. Input impedance of the feedback amplifier will be

$$Z_{if} = \frac{V_s}{I_i} - R_s \quad \underline{\text{(c)}}$$

- From the figure the KVL equation of the input circuit is

$$V_s = I_i (R_s + R_i) + V_f = I_i (R_s + R_i) + \beta V_o$$

At the output port we get

$$V_o = A V_i \left\{ \frac{R_L}{(R_L + R_O)} \right\}$$

$$\therefore V_s = I_i (R_s + R_i) + \beta \left\{ \frac{A V_i R_L}{(R_L + R_O)} \right\}$$

$$\therefore \frac{V_s}{I_i} = R_s + R_i + \beta \left\{ \frac{A R_L}{(R_L + R_O)} \right\} \frac{V_i}{I_i}$$

Where the term  $\frac{V_i}{I_i}$  represents the input impedance of the Basic Amplifier

$$\text{Or } \frac{V_i}{I_i} = R_i$$

$$\therefore \frac{V_s}{I_i} = R_s + R_i \left\{ 1 + \beta \frac{A R_L}{(R_L + R_o)} \right\}$$

- Substituting for  $\frac{V_s}{I_i}$  in Eq. (c) and simplifying we get the Input Impedance of the Voltage-Series Negative Feedback Amplifier is

$$Z_{if} = R_i \left\{ 1 + \beta \frac{A R_L}{(R_L + R_o)} \right\} \quad \dots (25)$$

**OBSERVATIONS :-** From the discussion above we observe the following..

- Voltage Gain given by Eq. 23 would be stable if the Feedback Network consists of passive elements like resistance, capacitance etc. and under the condition that the voltage gain of the Basic Amplifier is high enough, so that  $\beta A_{vf} \gg 1$  so that

$$A_{vf} \approx \frac{1}{\beta}$$

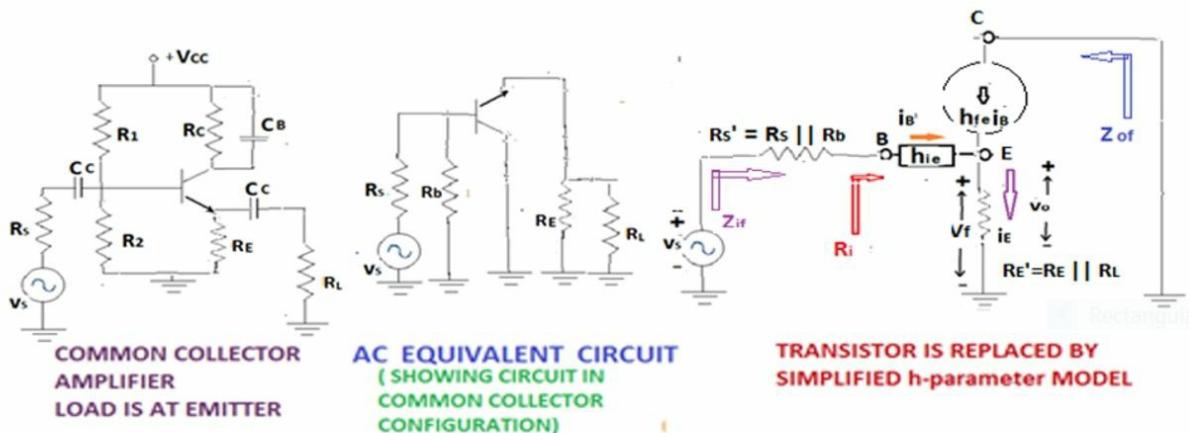
- Output impedance of the Feedback Amplifier is less than that of the Basic Amplifier, as given by Eq. 24.
- Input impedance of the Feedback Amplifier is greater than that of the Basic Amplifier, as given by Eq. 25.

### Example of Voltage-Series Feedback Amplifier

- The Common Collector amplifier, also known as the Emitter Follower is an example of the Voltage-Series Negative Feedback Amplifier. This amplifier was described and analyzed

with h-parameter model in Chapter-II.

- In this section it is shown that when the CC Amplifier is analyzed as a Voltage-Series Negative Feedback system and the same results as in Chapter - II is obtained.
- The transistor acts as the Basic Amplifier. The output voltage of the amplifier is across the external bias resistance  $R_E$  at the emitter terminal.
- This voltage also appears in series with the signal source  $V_S$  at the input terminal. However, the polarities of the source voltage and the feedback voltage are opposite in phase. Hence we have Voltage-Series Negative Feedback.



**Fig. – 11:** – Common Collector Amplifier (Emitter Follower) as an example of Voltage-Series Negative Feedback Amplifier.

### Analysis

#### ➤ Voltage gain

- As discussed earlier, we have

$$V_f = V_o$$

$$\therefore \beta = 1$$

From Eq. 23 we had the voltage gain of the Voltage –Series Negative feedback amplifier as

$$A_{vf} = \frac{A_{vs}}{1 + \beta A_{vs}} \quad \dots(a)$$

In this, the term  $A_{vs}$  represents the voltage gain of the Basic Amplifier.

i.e.  $A_{vs} = \frac{V_o}{V_s}$

Here  $V_o = h_{fe} i_B R_E'$

And  $V_s = (R_s + h_{ie}) i_B$

Substituting we have

$$A_{vs} = \frac{h_{fe} R'_E}{R_s + h_{ie}} \quad \dots(b)$$

Substituting in the expression (a) and using the value of  $\beta = 1$  we have

$$A_{vf} = \left[ \frac{\left\{ h_{fe} R'_E / (R_s + h_{ie}) \right\}}{\left\{ 1 + \left( h_{fe} R'_E / (R_s + h_{ie}) \right) \right\}} \right]$$

Simplifying, we have

$$A_{vf} = \frac{h_{fe} R'_E}{(R_s + h_{ie} + h_{fe} R'_E)} \quad \dots(26)$$

Rectangular Snip

### Input Impedance

The general expression for Input Impedance of Voltage-Series Feedback system is

$$Z_{if} = R_i (1 + \beta A_V)$$

Where  $A_V$  is the voltage gain of the amplifier when source resistance  $R_s$  is not considered and  $R_i$  is the input impedance of the basic amplifier.

Thus  $R_i = h_{ie}$

In the expression (b), putting  $R_s = 0$  and substituting for  $R_i$ , we have

$$A_{vs} = \frac{h_{fe} R'_E}{h_{ie}}$$

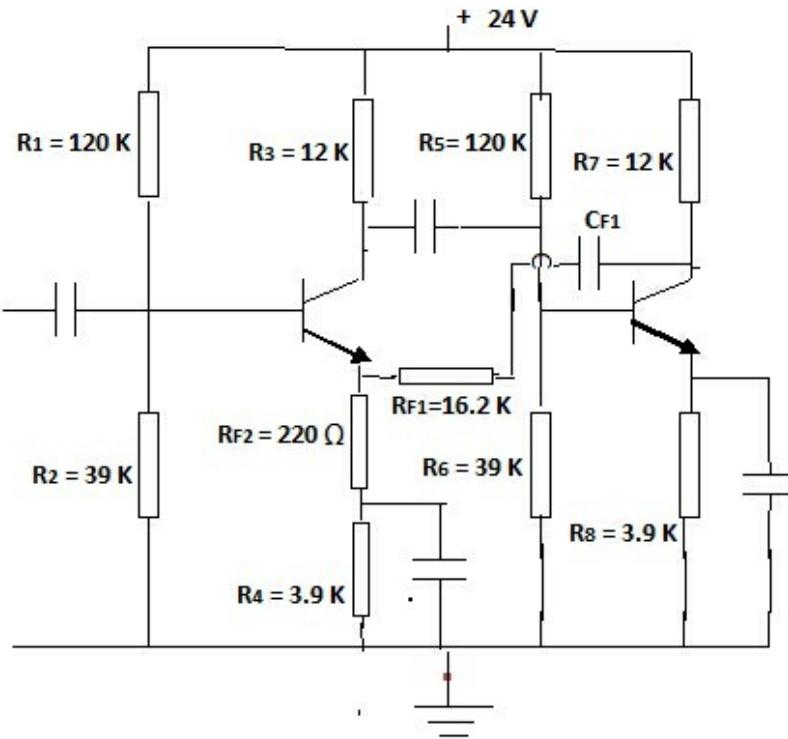
Substituting this in the expression for  $Z_{if}$  we have

$$Z_{if} = h_{ie} \left( 1 + \frac{h_{fe} R'_E}{h_{ie}} \right)$$

Or

$$Z_{if} = h_{ie} + h_{fe} R'_E \quad \dots(27)$$

**Example 4 :- Calculate the Closed-Loop Voltage Gain, Input Impedance and Output Impedance of the amplifier shown in the circuit. The transistors circuit has identical silicon transistors with  $h_{fe} = 100$  and  $h_{oe} = 15 \mu\text{V}$**



### SOLUTION ::

In this circuit, the resistance combination  $R_{F1}$  and  $R_{F2}$  constitute the feedback network. The capacitor  $C_{F1}$  simply couples the output signal from the collector to the feedback path. Hence in the AC equivalent circuit this capacitor will be a short circuit. The feedback voltage is the voltage developed across the resistance  $R_{F2}$  and this is fed back in series at the input terminal.

The circuit will be first analyzed in Open-Loop to obtain  $A_V$ ,  $Z_i$  and  $Z_o$ . The Closed-Loop calculations will be based on these values.

### OPEN-LOOP CONDITION

Since only two h-parameter values are known, and since  $h_{fe} \approx \beta$ , it is convenient to use r-parameter analysis. The technique for solving cascaded amplifiers, explained in Chapter VII will be used.

### DC Analysis ::

DC Equivalent circuit can be analyzed by considering the two stages as independent. The two stages are almost identical if we neglect the

effect of the small resistance  $R_{F2}$  in the first stage. Thus it is sufficient to analyze just one stage.

$$V_2 = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{39 \times 24}{120+39} = 5.89 \text{ V}$$

$$R_b = \frac{R_1 R_2}{R_1 + R_2} = \frac{39 \times 120}{120+39} = 29.4 \text{ K}$$

$$I_{BQ} = \frac{V_2 - V_{BE}}{R_b + (1+\beta)R_E}$$

where  $R_E = R_4 = 3.9 \text{ K}$ . For Si  $V_{BE} = 0.7 \text{ V}$ . Substituting the numerical values

$$I_{BQ} = \frac{5.89 - 0.7}{29.4 + (1+100) \cdot 3.9} = 0.012 \text{ mA}$$

$$I_{CQ} = \beta I_{BQ} = 100 \times 0.012 = 1.2 \text{ mA}$$

$$r_e' = \frac{25}{I_E \text{ mA}} = 25/1.2 = 20.83 \Omega$$

**AC Analysis ::** As explained in Chapter VII, AC analysis is started from the last stage and proceeds backwards. Starting with the 2<sup>nd</sup> stage, since this stage does not have 'Emitter Swamping Resistance' we have

$$|A_{V2}| = \frac{R_{L2}'}{r_e'}$$

$$\text{Where } R_L' = R_C = R_7 = 12 \text{ K} = 12000 \Omega$$

$$\therefore |A_{V2}| = \frac{12000}{20.83} = 576$$

$$Z_{iB2} = \beta r_e' = 100 \times 20.83 = 2083 \Omega = 2.083 \text{ K}$$

$$Z_{iT2} = Z_{iB2} || R_{b2} = \frac{2.083 \times 29.4}{2.083+29.4} = 1.94 \text{ K}$$

For the 1<sup>st</sup> stage Load Resistance is

$$R'_{L1} = Z_{iT2} \quad | \quad R_{C1} = \frac{1.94 \times 12}{1.94+12} = 1.67 \text{ K}$$

(Where  $R_{C1} = R_3 = 12 \text{ K}$ )

In the First Stage  $R_F$  acts as the 'Emitter Swamping Resistance'.

$$\therefore |A_{V1}| = \frac{R'_{L1}}{(R_F + r'_e)} = \frac{1670}{220+20.83} = 6.9$$

And

$$Z_{iB1} = \beta (R_F + r'_e) = 100 \times (220 + 20.83) = 24083 \Omega = 24.083 \text{ K}$$

$$Z_{iT1} = Z_{iB1} \parallel R_b = \frac{24.083 \times 29.4}{24.083+29.4} = 13.24 \text{ K}$$

Net Voltage Gain for the Cascaded Amplifier is

$$A_V = A_{V1} A_{V2} = 576 \times 6.9 = 3975$$

### CLOSED-LOOP CONDITION (Final Calculation for Feedback System)

In the Closed-Loop, the Feedback Factor is

$$B = \frac{R_{F2}}{R_{F1} + R_{F2}} = \frac{220}{16200 + 220} = 0.0134$$

Voltage Gain with Feedback

$$A_{vf} = \frac{A_v}{(1 + BA_v)} = \frac{3975}{1 + 0.0134 \times 3975} = 73.63$$

Input Impedance with Feedback

$$Z_{if} = Z_{iT1} (1 + BA_v) = 13.24 (1 + 0.0134 \times 3975) = 718.46 \text{ K}$$

In the Open-Loop condition output impedance is

$$Z_o = 1 / h_{oe} = \frac{1}{15 \times 10^{-6}} = 66666 \Omega = 66.67 \text{ K}$$

Output Impedance with Feedback

$$Z_{of} = \frac{Z_o}{(1 + BA_v)} = \frac{66.67}{1 + 0.0134 \times 3975} = 1.23 \text{ K}$$

Net Output Impedance is

$$Z_{out} = Z_{of} || R_7 = \frac{1.23 \times 12}{1.23 + 12} = 1.116 \text{ K}$$

## ***Section – 3***

### ***OSCILLATORS***

**(INCLUDES DESIGN PROCEDURE OF BJT AMPLIFIERS)**

**Definition:** - An Electronic oscillator is a circuit that **spontaneously** produces sustained sinusoidal oscillations with a constant amplitude & constant frequency.

- Spontaneous output means a sinusoidal output without any apparent input signal.
- Variable frequency, variable waveform signal generators are often required in the electronics industry and in the laboratory. Such Signal Generators are all based on an oscillator.
- If we provide Positive Feedback to an amplifier, and fulfill a certain condition, called **Barkhausen Criterion**, we can have **sustained spontaneous sinusoidal oscillation**.

## 9.9 Difference between Oscillator & AC Generator

- ✓ The following table highlights the differences between a generator and an electronic oscillator.

Table 1 :- Differences between AC Generator and Oscillator

<ul style="list-style-type: none"> <li>• AC Generator is an Electro-Mechanical device AND it requires a Prime Mover.</li> <li>• A Generator is designed to produce large levels of electrical power.</li> <li>• A generator is usually a 3 phase device.</li> </ul>	<ul style="list-style-type: none"> <li>• An Electronic Oscillator is an Electronic device AND it works spontaneously, i.e. without any input energy.</li> <li>• An Electronic Oscillator is capable of producing only small power level signals.</li> <li>• An Electronic Oscillator is always a Single phase device.</li> </ul>
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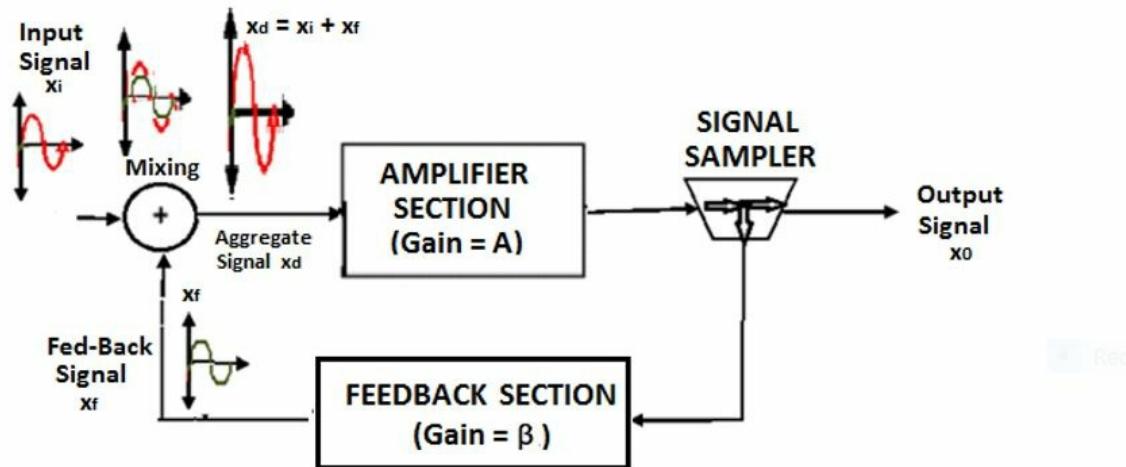
## 9.10 Positive Feedback and Spontaneous Oscillation

In the previous chapter we studied about Negative Feedback systems. In these, a portion of the output signal of a Basic Amplifier is applied as an additional input at the input port. In case of negative feedback systems, the phase of the feedback signal is opposite to that of the input signal. As a result, the amplitude of the signal at the Mixer is less than the input signal.

**Definition :-** A Positive Feedback System is defined as a feedback

system in which the phase of the feedback signal is in the same phase as the input signal.

Schematic of such a system is shown in the Fig. 1 below. Since the phase of the feedback signal is the same as the input signal, these two signals get added to each other instant by instant at the mixer stage. Thus, the output of the mixer has an amplitude greater than the input signal as well as the fed-back signal.



**Fig. 1:** – Schematic of a Positive Feedback System. In this, the feedback signal gets added with the input signal so that the output of the Mixer is the aggregate of the input and the feedback signals.

### Analysis

The fed back quantity  $x_f$  is in the same phase as the input quantity  $x_i$ . THUS they add together and we have the Aggregate signal as

$$x_d = x_i + x_f$$

∴

$$x_i = x_d - x_f$$

Where  $x_f$  is the Feedback Signal. Since the gain of the Feedback Network is ' $\beta$ ' and gain of the Basic Amplifier is ' $A$ ', we have

$$x_f = \beta x_o \quad \& \quad x_o = A x_d$$

∴

$$x_i = (1 - \beta A) x_d$$

Thus we get the Overall Gain of the feedback system is

$$A_f = x_o / x_i$$

$$A_f = A x_d / (1 - \beta A) x_d$$

OR

$$A_f = A / (1 - \beta A) \quad \dots \quad (1)$$

In order to have sustained oscillation, the output  $x_o$  must be non-zero in the absence of any apparent input. Thus  $x_o \neq 0$ , while the input  $x_i = 0$ . Thus in equation 1 the denominator  $(1 - \beta A)$  must tend to zero.

That is  $(1 - \beta A)$  must tend to 0

$$\beta A \rightarrow 1$$

Hence we get two conditions for oscillation, known as “BARKHAUSEN CRITERIA”, as follows

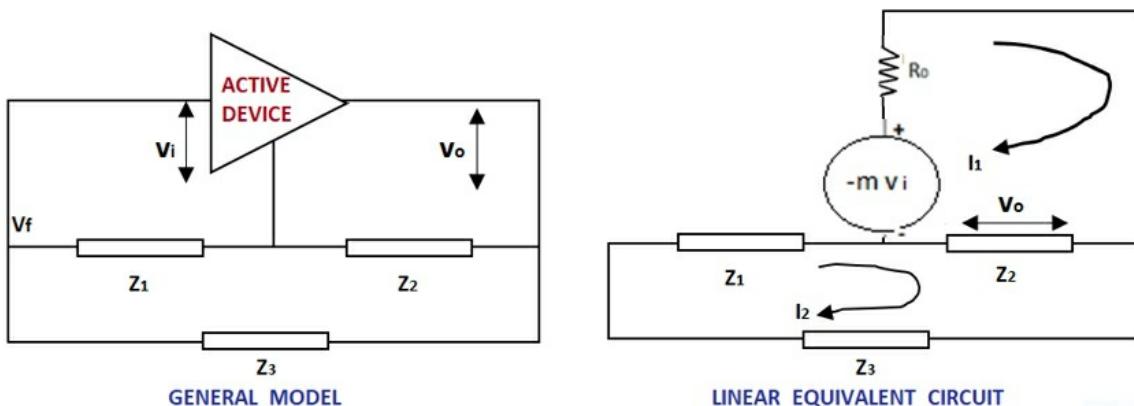
### BARKHAUSEN CRITERIA

- **Total gain around the loop must be Unity, i.e.  $\beta A = 1$ .**
- **Phase shift around the loop must be 0 or  $2\pi$  i.e.,  $360^\circ$ .**

This is the essential condition for sustained oscillation and is applicable to all types of oscillators.

### General Model of Oscillator

The general model of an oscillator as shown in the Fig. 2 below. The Active Device is the amplifier, which may be either a BJT or an FET or OPAMP with a voltage gain of “m”. It must be assumed that the device must have a very high input impedance. The equivalent circuit is also shown along with.



**Fig. 2:** - General configuration for LC Resonant Circuit Oscillators and it's Linear Equivalent Circuit.

Assuming the amplifier to be single stage, the gain of the amplifier without feedback will have a negative sign, given by the following expression.

$$A = \frac{-m Z_L}{Z_L + R_o}$$

Here the load impedance is the parallel combination of  $Z_2$  with the series combination  $(Z_1 + Z_3)$ .

The Feedback Factor is given by

$$\beta = \frac{Z_1}{Z_1 + Z_3}$$

Thus the loop gain  $A\beta$  will be

$$A\beta = \frac{-m Z_L}{Z_L + R_o} \cdot \frac{Z_1}{Z_1 + Z_3}$$

Where

$$Z_L = \frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}$$

Substituting

$$A\beta = \frac{\left\{ -m \frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3} \right\}}{\left\{ R_o + \frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3} \right\}} \cdot \frac{Z_1}{Z_1 + Z_3}$$

Rectangular Snip

OR

$$A\beta = \frac{\left\{ -m \frac{Z_2(Z_1+Z_3)}{(Z_1+Z_2+Z_3)} \right\}}{\left\{ \frac{R_o(Z_1+Z_2+Z_3) + Z_2(Z_1+Z_3)}{(Z_1+Z_2+Z_3)} \right\}} \cdot \frac{Z_1}{(Z_1+Z_3)}$$

Simplifying

$$A\beta = \frac{-m Z_1 Z_2}{R_o(Z_1+Z_2+Z_3) + Z_2(Z_1+Z_3)}$$

If these impedances are pure reactances, i.e if  $Z_1 = j X_1$  ;  $Z_2 = j X_2$  and  $Z_3 = j X_3$ , and since some of these reactances are inductive , i.e.  $X_L = \omega L$  and some others capacitive, i.e.  $X_C = -1/\omega C$  , we may express the loop gain as

$$A\beta = \frac{-m X_1 X_2}{j R_o(X_1+X_2+X_3) + X_2(X_1+X_3)}$$

In order for the oscillator to function, the loop gain must be real. Thus in the above expression, the imaginary part must be zero.

Thus

$$X_1 + X_2 + X_3 = 0 \quad \dots(2)$$

$$\therefore A\beta = \frac{-m X_1}{(X_1+X_3)}$$

From the Eq. (2) we have

$$\begin{aligned} X_1 + X_3 &= -X_2 \\ \therefore A\beta &= \frac{m X_1}{X_2} \quad \dots(3) \end{aligned}$$

Since the loop gain must be positive, and nearly equal to unity, the **two reactances  $X_1$  and  $X_2$  must be of the same kind and  $X_3$  must be of the opposite kind**. In other words, if  $X_1$  and  $X_2$  are both inductive, then  $X_3$  must be capacitive.

## 9.11 Classification of Oscillators: -

Electronic oscillators are classified in terms of the following –

- ❖ The electrical circuit elements that constitute the Feedback Network, for example, Resistance, Capacitance or Inductance.
- ❖ The frequency range of the output signal, for example, Audio Frequency, Radio Frequency or Microwave Frequency.

- ❖ The type of waveform of the output signal.

The following table summarizes the classification of electronic oscillators

**Table 2 :- Classification of Oscillators**

Sl. No.	Feed Back Path Components/Type	Frequency Range/Type	Type of Waveform	Major Applications
1.	R & C ( RC Oscillator )	Audio Frequency AF (1KHz–10mHz)	Sinusoidal	Industrial Applications & Lab Purpose
2.	L & C ( LC Oscillator )	Radio Frequency RF (50MHz–40GHz)	Sine or Square	Communication Devices
3.	Piezoelectric Crystal	100MHz to GHz and above	Sine or Square	Clock of digital systems

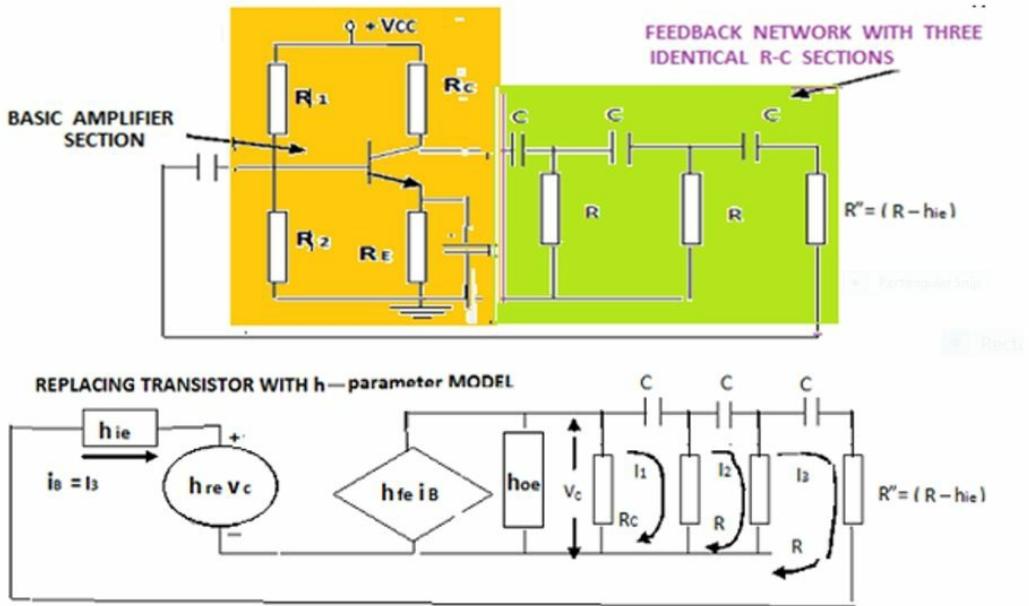
## R C Oscillators

- An Oscillator consists of two main components, namely,
  - (a) The Basic Amplifier with a gain of  $A_V$
  - (b) The Feedback path with a gain of  $\beta$ .
- These must be designed to satisfy Barkhausen Criteria.
- In this, the feedback path is analyzed **to obtain the frequency and condition of oscillation.**
- In general, when the feedback path components consist of resistors and capacitors, the frequency of oscillation comes out to be in the Audio Frequency range.
- (i) **Phase Shift Oscillator** and (ii) **Wien Bridge Oscillator** are two of the most commonly used RC Oscillators.

### 1 : Phase Shift Oscillator

- ✓ A single stage BJT Common Emitter Amplifier provides a voltage gain of  $A_V$  greater than 1 along with a phase shift of  $-\pi$  or  $-180^\circ$  (Lagging).

- ✓ Thus, **in order to satisfy Barkhausen Criteria**, the Feedback Path must be designed to provide an attenuation of  $1/A_V$  (Gain less than 1 is called Attenuation), and a further Phase Shift of  $\mp\pi$  (or  $\mp 180^\circ$ ).
- ✓ This is achieved using a RC network. Each R-C section provides attenuation of  $\frac{x_c}{\sqrt{(R^2 + x_c^2)}}$  which must be made equal to  $A_V / 3$  and a leading phase shift of  $+\pi/3$  ( $+60^\circ$ ). Thus total gain around the Loop is 1 and total phase shift in the three R-C sections is  $+\pi$ , so that the Net Phase Shift around the Loop is zero.
- ✓ Thus **BARKHAUSEN CRITERIA** is satisfied. The standard circuit is as shown in the Fig. 3 below.

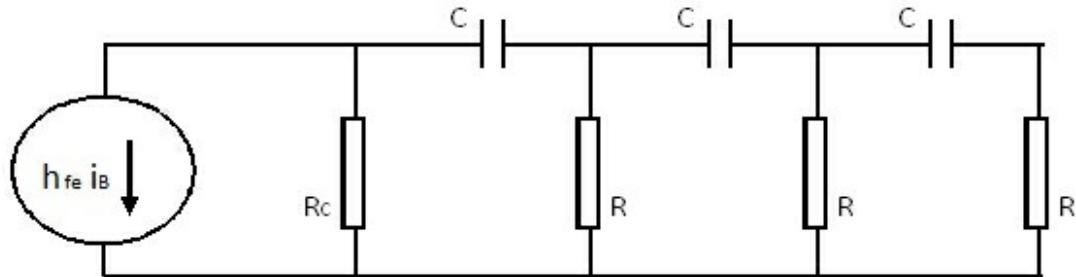


**Fig. 3:** – The Phase Shift Oscillator consists of a **Basic Amplifier**, which is a CE amplifier with a gain of  $A_V$  and a phase shift of  $-\pi$ . The **Feedback Path** consists of three RC sections, each providing a leading phase shift of  $\pi/3$  and together provide a net gain (attenuation) of  $1/A_V$ . Thus, net gain around the loop is unity and the net phase shift is zero. This ensures that Barkhausen Criteria is satisfied. The circuit is analyzed by replacing the transistor with the h-parameter model.

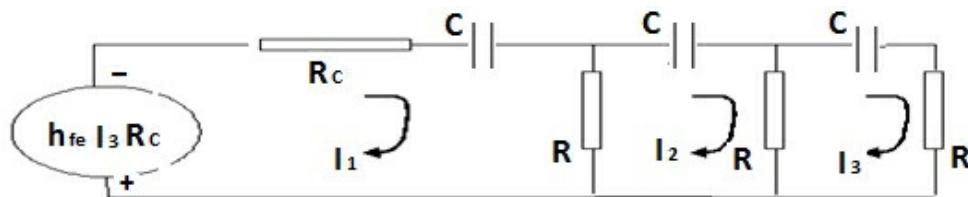
### Analysis

- ❖ For the purpose of analysis we have to reduce the circuit to an equivalent circuit with the following assumptions.
- ❖ The assumption in the general model of the oscillator (Fig – 2) was that, the amplifier must have a very high input resistance. Thus we make the approximation that  $R_b \gg h_{ie}$
- ❖ Further, in this circuit we may assume  $h_{re} \ll 1$  therefore the voltage source  $h_{re} V_C$  is negligible. For a BJT we also have current  $i_B = I_3$ .
- ❖ Further, assuming  $R_C \ll (1/h_{oe})$  such that the parallel combination of the admittance  $h_{oe}$  (reciprocal of which is  $1/h_{oe}$ ) and the resistance  $R_C$  is replaceable with  $R_C$  alone, and using the value of  $R'' = (R - h_{ie})$ , so that the net resistance in the Loop – 3

becomes  $R'' + h_{fe} = R$ , we have the equivalent circuit



Now, replacing the Norton's equivalent of the Current Source “ $h_{fe} i_B$ ” in parallel with the impedance “ $R_C$ ”, with the equivalent Thevenin’s circuit of the Voltage source “ $h_{fe} i_B R_C$ ”, in series with the impedance  $R_C$ , we have --



Now the Kirchhoff's Voltage Law (KVL) equations of the three loops are --

1.  $\{(R_C + R) - j(1/\omega C)\}.I_1 - R.I_2 + h_{fe}R_C.I_3 = 0$
2.  $-R.I_1 + \{(2R - j(1/\omega C))\}.I_2 - R.I_3 = 0$
3.  $0 - R.I_2 + \{(2R - j(1/\omega C))\}.I_3 = 0$

By Kramer's Rule, the solution of these set of simultaneous equations is obtained by equating the Determinant of the Co-efficient Matrix to zero.

**In this we make a further assumption that  $R_C = R$ ,** Thus using Kramer's Rule we have --

$$\begin{vmatrix} \{2R - j(1/\omega C)\} & -R & h_{fe}R \\ -R & \{2R - j(1/\omega C)\} & -R \\ 0 & -R & \{2R - j(1/\omega C)\} \end{vmatrix} = 0$$

Thus solving the Determinant, we have –

$$\{2R - j(1/\omega C)\} \{ \{2R - j(1/\omega C)\}^2 - R^2 \] + R [(-R) \{2R - j(1/\omega C)\} + h_{fe} R^2 ] = 0$$

Factorizing the 1<sup>st</sup> term we have

$$(2R - j(1/\omega C)) \{ (2R - j(1/\omega C)) + R \} \{ (2R - j(1/\omega C)) - R \}$$

1 st term

$$(2R - j(1/\omega C)) (3R - j(1/\omega C)) (R - j(1/\omega C))$$

For the ease of simplification,

$$\text{Let } 2R = a : 1/\omega C = b : 3R = c : \& R = d$$

$$1 \text{ st term} = (a - jb)(c - jb)(d - jb)$$

$$= \{d(ac - b^2) - b^2(a + c)\} - jb(ad + ac + cd - b^2)$$

$$= \{acd - b^2(a + c + d)\} - jb\{d(a + c) + ac - b^2\}$$

$$\text{Where } acd = 6R^3$$

$$b^2 = 1/(\omega C)^2$$

$$a + c + d = 6R$$

$$d(a + c) + ac - b^2 = 11R^2 - 1/(\omega C)^2$$

Therefore 1 st term

$$\{6R^3 - 6R/(\omega C)^2\} - j(1/(\omega C)) \{11R^2 - 1/(\omega C)^2\}$$

Now the 2<sup>nd</sup> term is

$$R[(-R)\{2R - j(1/\omega C)\} + h_{fe} R^2] = R\{-2R^2 + jR/\omega C + h_{fe} R^2\} = R^3(h_{fe} - 2) + jR^2/\omega C$$

Adding the 1 st term & the 2nd term we get , the Determinant "D" of the Co-efficient Matrix as

$$D = \{6R^3 - 6R/(\omega C)^2 + R^3(h_{fe} - 2)\} - j\{11R^2/(\omega C) - 1/(\omega C)^3 - R^2/\omega C\}$$

Simplifying and equating the determinant to zero we have

$$D = \{6R^3 - 6R/(\omega C)^2 + R^3(h_{fe} - 2)\} - j\{10R^2/(\omega C) - 1/(\omega C)^3\} = 0$$

Now equating the Imaginary part of this expression to zero, we get the "frequency of oscillation" as --

Imaginary Part

$$\{10R^2/(\omega C) - 1/(\omega C)^3\} = 0$$

$$[\{10R^2(\omega C)^2 - 1\}/(\omega C)^3] = 0$$

$$\{10R^2(\omega C)^2 - 1\} = 0$$

$$10R^2\omega^2C^2 = 1$$

$$\text{OR } \omega^2 C^2 = 1/10R^2$$

Therefore  $\omega = \frac{1}{\sqrt{10} RC}$

And

$$f = \frac{1}{2\pi\sqrt{10}RC} \dots(2)$$

AND

Equating the real part to zero we get the “condition of oscillation” as

Real Part

$$\{6R^3 - 6R / (\omega C)^2 + R^3(h_{fe} - 2)\} = 0$$

Substituting for  $\omega^2 C^2 = 1/10 R^2$  from the expression above, we have

$$6R^3 - 6R / \{1/10 R^2\} + R^3(h_{fe} - 2) = 0$$

$$6R^3 - 60R^3 + R^3(h_{fe} - 2) = 0$$

$$R^3 h_{fe} = 56R^3$$

OR

$$h_{fe} = 56 \dots(3)$$

THUS

1. “Frequency of oscillation” given by eq (2) &
2. “Condition of oscillation” by eq (3).

## Design Considerations

1. In order to set up oscillations with a Phase Shift Oscillator, we need to have a transistor having the h-parameter “ **$h_{fe}$** ” of the exact value “56”.
2. The feedback circuit must be designed with appropriate values of “R” and “C” using eq (2), depending on the required frequency of the desired output signal.
3. The resistance R” in the third RC loop must be equal to (R –  $h_{ie}$  ).

Such stringent conditions are a bit difficult to meet in practice. Hence the Phase Shift Oscillator made of BJT is not a preferred choice of the electronics engineer. However, a phase shift oscillator based on an OPAMP is quite common, since the design with OPAMP does not present such difficulties.

## 2 : Wien Bridge Oscillator

The practical difficulties presented by the design of a Phase Shift Oscillator are overcome by using a Wien Bridge Oscillator. The circuit diagram is shown in the Fig- 4 below.

The constructional features of the Wien Bridge oscillator as enumerated below.

- The Basic Amplifier consists of a 2 stage Common Emitter amplifier. And the Feedback path consists of a RC Wien Bridge, operating at balance conditions .
- The net gain of the amplifier is A. At balance condition the input and output voltage of the bridge are very small. Hence the gain of the feedback path is  $\beta < 1$ . The amplifier and the bridge network is designed in such a manner that net gain in the loop,  $A\beta = 1$ .
- In each stage of a CE amplifier the phase shift is  $180^\circ$ . Since there are two stages, net phase shift in the amplifier is  $360^\circ$ .At balance condition, in the Wien Bridge, the phase difference between the input and output voltage is zero. hence net phase shift in the loop is  $360^\circ$ .
- Thus Barkhausen criteria is satisfied.
- It can be proved that the frequency of oscillation is given by

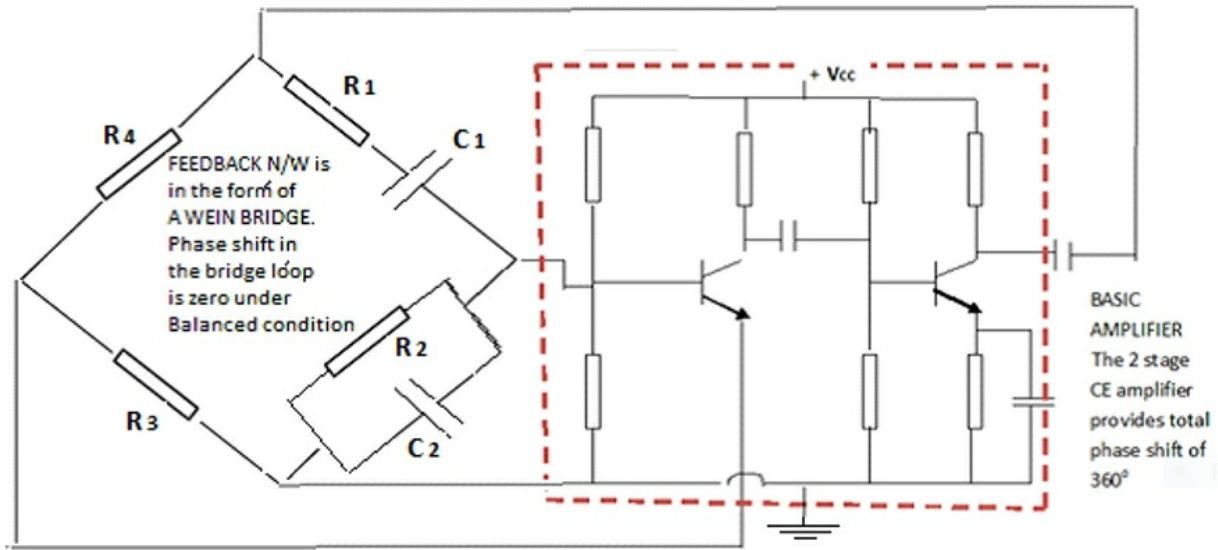
$$\underline{f} = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$$

If  $R_1 = R_2 = R$  &  $C_1 = C_2 = C$

Then

$$\underline{f} = 1/(2\pi R C)$$

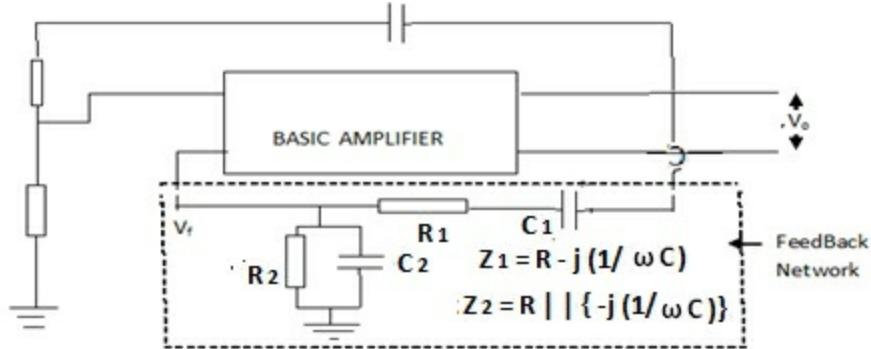
And Condition of oscillation is that the Gain of the Basic Amplifier is  $A = 3$ .



**Fig. 4: – Circuit diagram of Wien Bridge**

### ANALYSIS

The basic Amplifier and the feedback circuit may be redrawn as follows



In this circuit, the parallel RC combination is designated as the impedance  $Z_2$  and the series RC combination is designated as  $Z_1$

Thus,

$$Z_2 = \frac{R \cdot (-j(1/\omega C))}{R - j(1/\omega C)} = \frac{R \cdot (1/j\omega C)}{R + (1/j\omega C)}$$

$$Z_2 = \frac{R/j\omega C}{(j\omega C R + 1)/j\omega C}$$

OR

$$Z_2 = R / (1 + j\omega RC)$$

And

$$Z_1 = R - j(1/\omega C) = R + 1/j\omega C$$

The voltage developed across the parallel impedance is applied as the Feedback quantity  $V_f$ . By Voltage Divider Rule we have

$$V_f = \frac{Z_2 V_o}{Z_1 + Z_2}$$

Thus, the gain of the Fed Back Network

$$\beta = V_f / V_o = \frac{Z_2}{Z_1 + Z_2}$$

Substituting for  $Z_1$  and  $Z_2$  we have

$$\beta = \frac{R/(1+j\omega RC)}{(R+1/j\omega C)+\{R/(1+j\omega RC)\}}$$

Simplifying

$$\beta = \frac{R/(1+j\omega RC)}{\left(\frac{1+j\omega RC}{j\omega C}\right)+\left\{\frac{R}{(1+j\omega RC)}\right\}}$$

$$\beta = \frac{R\{j\omega C.(1+j\omega RC)\}}{(1+j\omega RC).\{(1+j\omega RC)^2+j\omega RC\}}$$

$$\beta = \frac{j\omega RC.(1+j\omega RC)}{(1+j\omega RC).\{(1+j\omega RC)^2+j\omega RC\}}$$

$$\beta = \frac{j\omega RC}{j\omega RC + (1+j\omega RC)^2}$$

$$\beta = \frac{j\omega RC}{j\omega RC + 1 + j\omega RC^2 + j2\omega RC}$$

$$\therefore \beta = \frac{j\omega RC}{1 + j\omega RC^2 + j3\omega RC}$$

In order to satisfy Barkhausen Criteria  $A\beta = 1$

$$A\beta = \frac{j\omega ARC}{1 + j\omega RC^2 + j3\omega RC} = 1$$

$$\therefore 1 - \frac{j\omega ARC}{1 + j\omega RC^2 + j3\omega RC} = 0$$

$$\therefore \frac{(1+j\omega RC^2+j3\omega RC)-j\omega ARC}{1+j\omega RC^2+j3\omega RC} = 0$$

OR       $1 + (j\omega RC)^2 + j3\omega RC - jA\omega RC = 0$   
 $1 + (j\omega RC)^2 + j(3 - A)\omega RC = 0$

Equating the Real part to zero we obtain the frequency of oscillation as

$$1 - (\omega RC)^2 = 0$$

$$\therefore (\omega RC)^2 = 1$$

$$\therefore (\omega)^2 = 1 / (RC)^2$$

$$\therefore f = 1 / 2\pi RC \quad \dots (4)$$

Equating Imaginary Part to zero we obtain the Condition of Oscillation as

$$(3 - A)A\omega RC = 0$$

OR

$$3\omega RC = A\omega RC$$

$$\therefore A = 3 \quad \dots (5)$$

THUS we get “frequency of oscillation” given by eq (4) & “condition of oscillation” by eq (5).

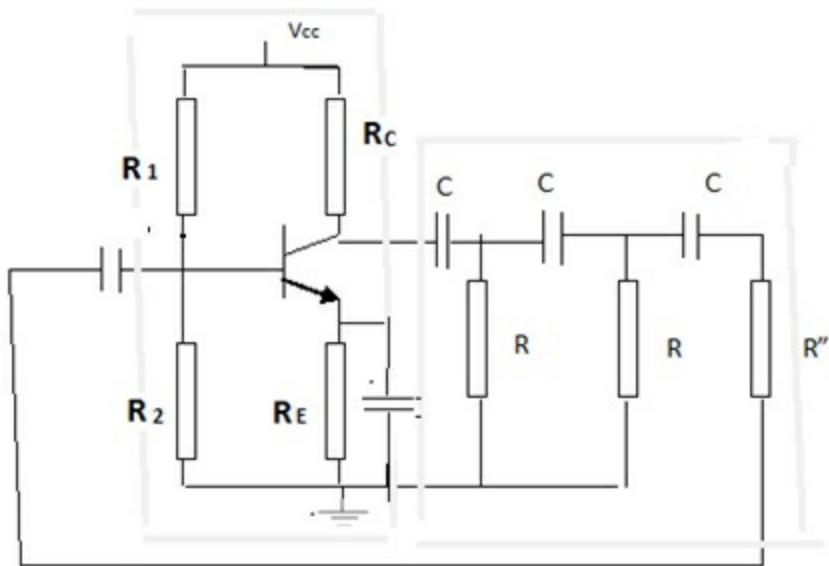
**Table 3 : Comparison Between Phase Shift Oscillator and Wien Bridge Oscillator**

<b>Phase Shift Oscillator</b>	<b>Wien Bridge Oscillator</b>
Difficult to establish condition of oscillation since the transistor to be used must have the exact value of $h_{fe}$ specified by equation (3) as $h_{fe} = 56$ . This value must be exact.	Comparatively easier to establish the condition of oscillation since the Basic Amplifier circuit is to be designed with the value of gain specified as $A = 3$ by eq. (6)
Once oscillations are set up, it is difficult to change the frequency of oscillation since three capacitors and/or resistors have to be adjusted in tandem.	Easier to change the frequency of oscillation since only two capacitors need to be varied. This task becomes simpler by using "Ganged Capacitors".
Due to ageing of transistors, the value of $h_{fe}$ deteriorates in the long run. In this case the circuit will gradually fail to oscillate.	The problem of ageing is overcome since the condition of oscillation is independent of the transistor parameters. The value of Amplifier Gain is controlled by the resistors $R_3$ & $R_4$ of the Wien Bridge.
The circuit is best implemented using OPAMPS since the problems of Frequency Stability and Ageing can be dynamically adjusted.	Circuit can be implemented with both BJTs and OPAMPS, with the condition of oscillation as well as the frequency remaining the same.

## TUTORIAL

**Example – 1 :-** Calculate the resistances in feedback loop of a Phase Shift oscillator for a BJT having  $h_{ie} = 2.035 K$  so that the frequency of the output signal is 1 K Hz. Use a standard value capacitor  $C = 0.01 \mu F$ .

**SOLUTION :-** Circuit Diagram



Frequency of oscillation of a Phase Shift oscillator is given by Eq. 2 as

$$f = 1 / 2\pi \sqrt{10} RC$$

Given

- a)  $f = 1 \text{ K Hz}$
- b)  $C = 0.01 \mu\text{F}$
- c)  $h_{ie} = 2.035 \text{ K}$

Substituting in the equation we have

$$\begin{aligned} R &= \frac{1}{2\pi \sqrt{10} \times 1000 \times 0.01 \times 10^{-6}} \\ &= 5035.5 \approx 5035 \Omega \end{aligned}$$

In this circuit the resistance in the third loop  $R'' = R - h_{ie}$

Substituting the value of  $h_{ie} = 2.035 \text{ K} = 2035 \Omega$ , we have

$$R'' = 5035 - 2035 = 3000 \Omega = 3 \text{ K.}$$

**NOTE :-** 3 K is a standard value resistor available in the market. Thus a 3K resistor will be used for  $R''$ . But  $5035 \Omega$  is not a standard value. Therefore, either a preset potentiometer of 6 K adjusted at the required value can be used, or a combination of standard value resistors giving the required value in the combination may be used.

### Design Problem

**Example – 2 :-** Using the values of the feedback path components as calculated in Example 10.1, design the amplifier part of the circuit by taking a Q-Point in the middle of the load line. Assume  $V_{CC} = 10 \text{ V}$ . Design the amplifier for a stability factor of  $S = 5$ .

**SOLUTION :** Requirements in the design problem are as follows

1. The Condition of oscillation in a Phase Shift oscillator is that  $h_{fe} = 56$ .
2. The Loop Gain must be at least equal to unity.
3. The Base Resistance  $R_b$  of the amplifier circuit must be very high.

**In designing the circuit we shall use the formulae described in**

## Chapter IV.

Using the values of the Feedback Circuit components  
Each RC is identical. Impedance of each RC Section is

$$Z_s = \frac{X_c}{\sqrt{(R^2 + X_c^2)}}$$

where  $X_c = \frac{1}{2\pi f C}$

and f is the frequency of oscillation.

Given  $f = 1 \text{ kHz}$  : and :  $C = 0.01 \mu\text{F}$

$$\therefore X_c = \frac{1}{2 \times 3.14 \times 1000 \times 0.01 \times 10^{-6}} = 15924 \Omega = 15.924 \text{ K}$$

In Ex. 10.1 we calculated

$$R = 5.035 \text{ K}$$

Substituting

$$Z_s = \frac{15.924}{\sqrt{(5.035^2 + 15.924^2)}} = 0.95 \text{ K} \approx 1 \text{ K}$$

**There are three R-C sections in parallel.**

Thus, net impedance of the Feedback Path, which is also the load impedance for the amplifier is

$$Z_L = Z_f = \frac{Z_{s1} + Z_{s2} + Z_{s3}}{Z_{s1}Z_{s2} + Z_{s2}Z_{s3} + Z_{s1}Z_{s3}}$$

$$Z_f = \frac{1+1+1}{1\times 1 + 1\times 1 + 1\times 1} = 1/3 = 0.333 \text{ K}$$

Net Load impedance is the parallel combination of  $R_C$  and  $Z_L$

Assume  $R_C = 1 \text{ K}$

$$\therefore Z_L' = \frac{1 \times 0.333}{1+0.333} = 0.25 \text{ K} = 250 \Omega$$

Attenuation introduced by the Feedback Circuit is

$$g = \frac{Z_L}{R_C + Z_L} = \frac{0.333}{1+0.333} = 0.25$$

Loop Gain is  $A_{VG}$ . In terms of Barkhausen Criteria

$$A_{VG} = 1$$

$$\therefore A_V = 1/g = 1/0.25 = 4$$

For a CE amplifier we have

$$|A_V| = \frac{R_C}{(r_E + r_e')}$$

Where  $r_E$  is the un-bypassed resistance in the Emitter terminal, and  $r_e'$  is the internal resistance of the forward biased Emitter-Base junction.

Substituting for  $R_C$  and  $A_V$ , we have

$$r_E + r_e' = 1000/4 = 250 \Omega$$

In this Let  $r_E = 220 \Omega$

$$\therefore r_e' = 30 \Omega$$

The empirical formula for  $r_e'$  is

$$r_e' = \frac{25}{I_E(\text{mA})}$$

where  $I_E$  is the Biasing Current at the Emitter terminal in mA scale.

$$\therefore I_E = 25/30 = 0.83 \text{ mA}$$

Let  $I_{CQ} = I_E$

$$\therefore I_{CQ} = 0.83 \text{ mA}$$

Given  $V_{CC} = 10 \text{ V}$

Assuming Q-Point to be mid-point of Load Line we have

$$V_{CEQ} = \frac{1}{2} V_{CC} = 5 \text{ V} \quad \text{and} \quad I_{C(Sat)} = 2 I_{CQ} = 1.67 \text{ mA}$$

Where

$$I_{C(Sat)} = \frac{V_{CC}}{(R_C + R_E)}$$

Where  $R_E$  is the total resistance at the Emitter.

$$\therefore (R_C + R_E) = \frac{V_{CC}}{I_{C(Sat)}}$$

$$= \frac{10}{1.67} = 6.024 \text{ K}$$

We had assumed  $R_C = 1 \text{ K}$

$$\therefore R_E = 6.024 - 1 = 5.024 \text{ K}$$

This is the total resistance at the Emitter terminal. Out of this the Un-bypassed resistance was calculated as

$$r_E = 220 \Omega \text{ ( } 0.22\text{K})$$

Therefore, the Bypassed resistance at the Emitter is

$$R_E' = 5.024 - 0.22 = 4.8 \text{ K}$$

We shall use the standard value resistor

$$R_E' = 4.7 \text{ K}$$

For a Voltage Divider Bias Circuit we have

$$\frac{R_b}{R_E} = \frac{(S-1)(1+\beta)}{1+\beta-S}$$

Where  $R_b$  is the Thevenin's equivalent resistance at the base terminal and 'S' is the Stability Factor.

$$\text{Given } S = 5 \text{ and } \beta = 56$$

Substituting

$$\frac{R_b}{R_E} = \frac{(5-1)(1+56)}{1+56-5} = 4.4$$

$$\therefore R_b = 4.4 \times 5.024 = 22.1 \text{ K}$$

In the biasing circuit, the biasing voltage  $V_2$ , across the Base and ground is given by

$$V_2 = I_{BQ} R_b + V_{BE} + (I_{CQ} + I_{BQ}) R_E$$

Assuming a Si transistor  $V_{BE} = 0.7 \text{ V}$ .

$$I_{BQ} = I_{CQ}/\beta = 0.83/56 = 0.015 \text{ mA}$$

Substituting

$$V_2 = 0.015 \times 22.1 + 0.7 + (0.83+0.015) \times 5.024$$

$$V_2 = 5.277 \text{ V}$$

The resistances in the voltage divider part of the biasing circuit are

given by

$$R_1 = \underline{R_b} \frac{V_{CC}}{V_2} \quad \text{AND} \quad R_2 = \frac{R_1 V_2}{V_{CC} - V_2}$$

Substituting

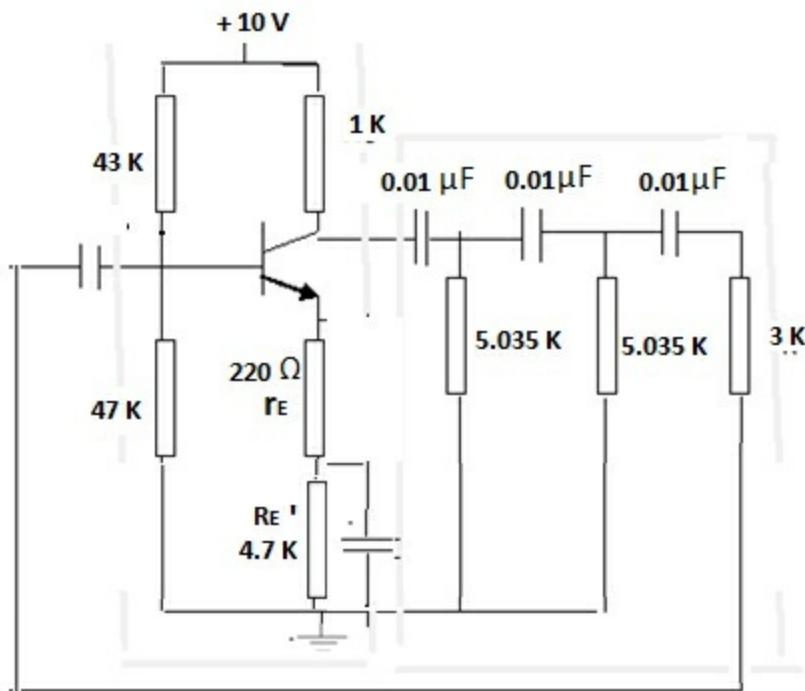
$$R_1 = 22.1 \frac{10}{5.277} = 41.88 \text{ K}$$

AND

$$R_2 = \frac{41.88 \times 5.277}{(10 - 5.277)} = 46.8 \text{ K}$$

Again we shall use the standard value resistors as

$$R_1 \approx 43 \text{ K} \quad \text{AND} \quad R_2 \approx 47 \text{ K.}$$



**Example – 3 :-** Calculate the resistances and capacitances in feedback loop of a Wien Bridge oscillator so that the frequency of the output signal is 105 K Hz. Use Standard Value components. Make convenient assumptions.

**SOLUTION :-**

Frequency of oscillation for a Wien Bridge oscillator is given by

Eq.10.4 as

$$f = 1 / 2\pi RC$$

For frequency of 105 KHz we have

$$RC = 1/ 2\pi \times 105 \times 10^3$$

$$RC = 1.5 \times 10^{-6}$$

**A suitable standard value resistance is 1.5 K**

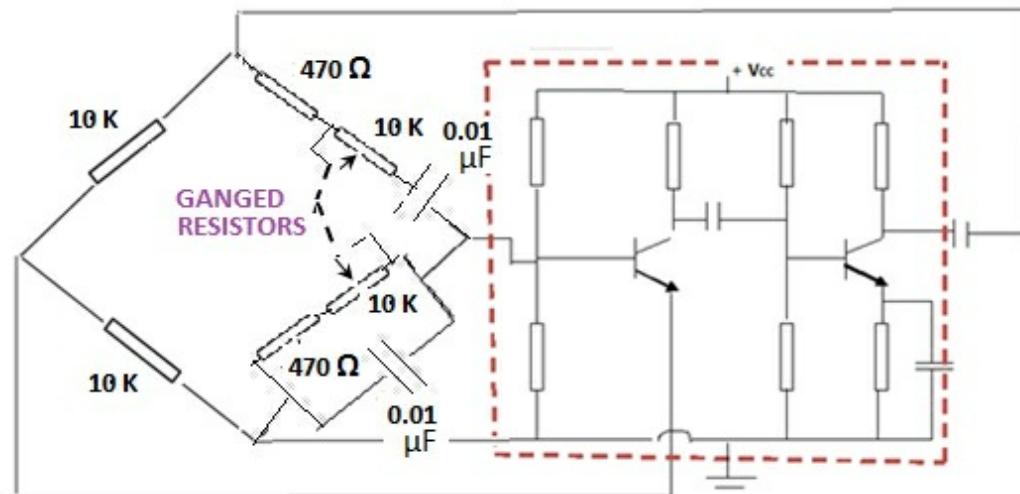
Using  $R = 1.5$  K we have

$$C = \frac{1.5 \times 10^{-6}}{1.5 \times 10^3} = 1 \times 10^{-9}$$

This corresponds to a standard value capacitance of

$$C = 1000 \text{ pF.}$$

**Example – 4 :-** Calculate the maximum and minimum frequencies of oscillation of the Wien Bridge oscillator shown in the figure below. (This uses “Ganged Resistors”. In a pair of ganged variable resistors, the resistances change together and have the same value for any wiper position. A similar mechanism is also employed for a pair of Air–Core Capacitors.)



### SOLUTION

Using the Eq. 4 for the frequency of oscillation of the Wien Bridge oscillator, the Maximum and Minimum Frequencies of oscillation are as follows

Minimum resistance is  $470 \Omega$  and maximum resistance is  $10470 \Omega$ . In the expression for frequency of oscillation, resistance ‘R’ comes in the denominator. Hence, the maximum frequency of oscillation occurs when the resistance is set at the minimum value and vice-versa.

$$\therefore f_{\text{MAX}} = \frac{1}{2\pi \times 470 \times 0.01 \times 10^{-6}} = 33879.9 \text{ Hz} \approx 34 \text{ KHz}$$

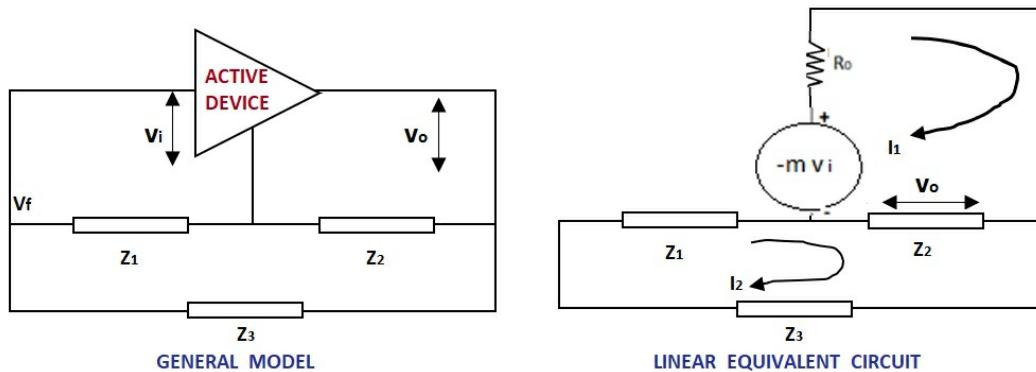
AND

$$f_{\text{MIN}} = \frac{1}{2\pi \times 10470 \times 0.01 \times 10^{-6}}$$

$$= 1520.1 \text{ Hz} \approx 1.5 \text{ KHz}$$

## LC Oscillators

- L C Oscillators are used at higher frequencies compared to the RC Oscillators.
- Typical range of working frequencies is of the order of a few Mega Hertz to a few Giga Hertz. Hence they are classified as Radio Frequency (RF) Oscillators.
- Recall the General Form of the Oscillator, reproduced in the figure below.



From this figure we derived the General Form of the Loop Gain as

$$\therefore A \beta = \frac{m X_1}{X_2} \quad \dots(6)$$

And a condition to be satisfied by the General Form was, the reactances must be such that,

$$X_1 + X_2 = -X_3$$

- In order to satisfy Barkhausen Criterion, the loop gain must be positive, and equal to unity, therefore, the **two reactances  $X_1$  and  $X_2$  must be of the same kind and  $X_3$  must be of the opposite**

kind.

- Thus, if  $X_1$  and  $X_2$  are both inductive, then  $X_3$  must be capacitive. If the impedances of the feedback network are of this combination then the oscillator is called a Hartley Oscillator.
- On the other hand, if  $X_1$  and  $X_2$  are capacitive and  $X_3$  is inductive, the resulting oscillator is called a Colpitts Oscillator.
- LC Oscillators are based on either of the two standard configurations, namely, The Hartley Oscillator and The Colpitts Oscillator.
- In fact the sinusoidal oscillators using crystals, which are used at even higher frequencies are also based on these two configurations.
- In an LC Oscillator the feedback path consists of a LC parallel circuit. Such an arrangement, is called an LC Tank Circuit. The LC Tank circuit has a resonant frequency given by

$$f = \frac{1}{2\pi\sqrt{LC}} \quad \dots (7)$$

- Initially, as soon as the circuit is switched on, transients are produced. These are sinusoidal oscillations at the resonant frequency.
- The transients are fed-back to the amplifier input, which amplifies it every cycle. It has to be ensured by the feedback path that the feedback is positive, i.e. the instantaneous phase angle of the feedback signal is the same as the input signal.
- In general, when the conditions for satisfying Barkhausen Criteria is implemented the circuit will continue to produce stable sinusoidal oscillations at the resonant frequency of the LC Tank circuit in the feedback path.

## Hartley Oscillator

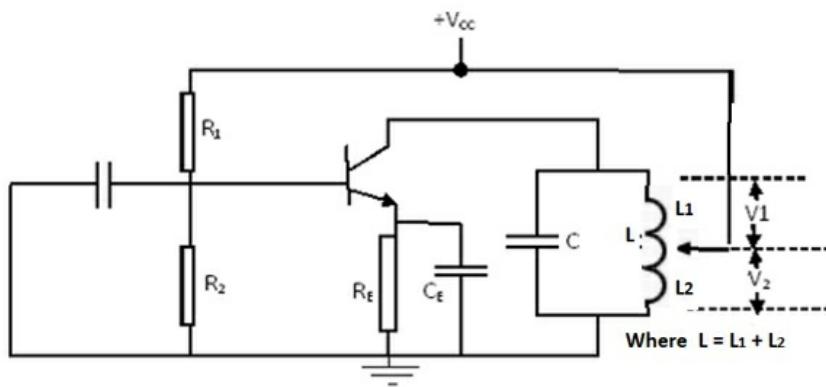
- The circuit diagram of the Hartley oscillator is shown in the Fig. 5.
- It consists of a single stage CE amplifier. The LC Tank circuit is

connected at the collector terminal, in such a way that the internal resistance of the part  $L_1$  of the coil becomes the biasing resistance  $R_C$  of the amplifier.

- This internal resistance also happens to be the Load Resistance  $R_L'$ . Since this internal resistance of the coil is generally a small value, the Voltage Gain,  $A_V$  of the amplifier will be quite as low as unity.

$$|A_V| = \frac{R_{L'}}{r_e'}$$

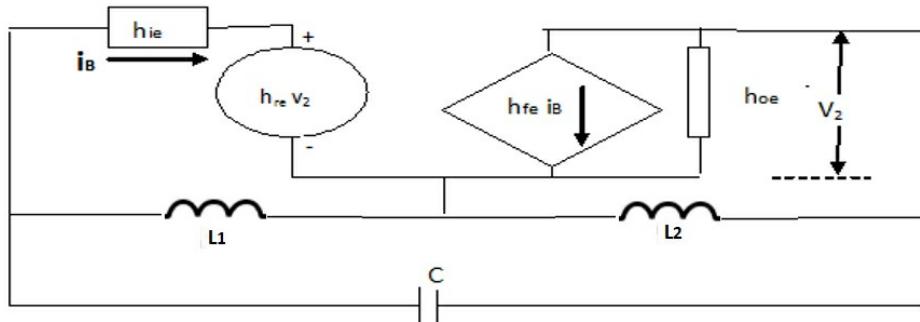
- The portion of the voltage  $V_2$  developed across the  $L_2$  part of the coil is fed back as the signal  $V_f$ . By adjusting the variable point of the inductance, the magnitude of  $V_f$  can be adjusted so as to be of the appropriate value to set up sustained oscillations.
- The frequency of oscillation is pre-determined by the values of  $C$  and  $L$ , which is to be substituted in Eq. 6 to get the frequency of oscillation.
- The condition of oscillation is obtained by analyzing the circuit.



**Fig. 5: – Hartley Oscillator**

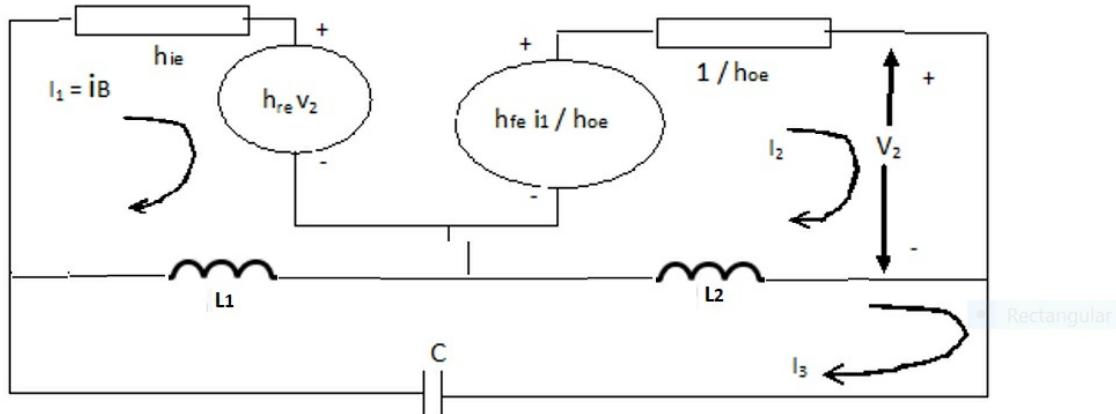
### ANALYSIS

- ❖ We may redraw the circuit by replacing the BJT with the h-parameter equivalent model. In this we may make an approximation  $R_b \gg h_{ie}$ . Thus we have the following circuit.



- ❖ We now replace the Norton's equivalent at the collector terminal by an equivalent Thevenin's network. For this the Current Source & parallel admittance combination of  $h_{fe} \cdot i_B$  &  $h_{oe}$  is replaced with an equivalent Voltage Source & Series Resistance combination of  $h_{fe} \cdot i_B / h_{oe}$  &  $1 / h_{oe}$ .
- ❖ Next we substitute the Base Current  $i_B$  with the Loop Current  $I_1$  in the Loop-1. Hence the voltage source becomes

$$\frac{h_{fe} \cdot i_B}{h_{oe}} = \frac{h_{fe} \cdot I_1}{h_{oe}}$$



- ❖ Now the KVL Equations of the three loops are as follows –

**Loop 1 :**  $(h_{ie} + j\omega L_1) I_1 - j\omega L_1 I_3 = h_{re} V_2$

In the Loop 2, the voltage  $V_2$  is given by

$$V_2 = \left( \frac{h_{fe} \cdot i_1}{h_{oe}} \right) - \frac{i_2}{h_{oe}}$$

Substituting we have

$$(h_{ie} + j\omega L_1) I_1 - j\omega L_1 I_3 = h_{re} \left\{ \left( \frac{h_{fe} \cdot i_1}{h_{oe}} \right) - \frac{i_2}{h_{oe}} \right\}$$

Re-arranging , for Loop – 1:

$$\{ h_{ie} + j\omega L_1 - \left( \frac{h_{fe} \cdot h_{re}}{h_{oe}} \right) \} I_1 + \left( \frac{h_{re}}{h_{oe}} \right) I_2 - j\omega L_1 I_3 = 0 \quad \dots(a)$$

$$\text{Loop 2 : } 1 / h_{oe} I_2 + j\omega L_2 I_2 - j\omega L_2 I_3 = h_{fe} I_1 / h_{oe}$$

$$\left( \frac{1}{h_{oe}} \right) I_2 + j\omega L_2 I_2 - j\omega L_2 I_3 = \left( \frac{h_{fe}}{h_{oe}} \right) I_1$$

Re-arranging ,

$$-\left( \frac{h_{fe}}{h_{oe}} \right) I_1 + \left( \frac{1}{h_{oe}} + j\omega L_2 \right) I_2 - j\omega L_2 I_3 = 0 \quad \dots(b)$$

Loop 3 :

$$- j\omega L_1 I_1 - j\omega L_2 I_2 + \{ j\omega L_1 + j\omega L_2 - j/\omega C \} I_3 = 0 \quad \dots(c)$$

❖ In order to solve this set of simultaneous equations by Kramer's rule, we equate the Determinant of the coefficient matrix to zero.

Thus we have ---

$$\begin{vmatrix} \{ h_{ie} + j\omega L_1 - \left( \frac{h_{fe} \cdot h_{re}}{h_{oe}} \right) \} & \left( \frac{h_{re}}{h_{oe}} \right) & - j\omega L_1 \\ -\left( \frac{h_{fe}}{h_{oe}} \right) & \left( \frac{1}{h_{oe}} + j\omega L_2 \right) & - j\omega L_2 \\ - j\omega L_1 & - j\omega L_2 & \{ j\omega L_1 + j\omega L_2 - (j/\omega C) \} \end{vmatrix} = 0$$

❖ In this we have  $(L_1 + L_2) = L$ , where  $L$  is the net inductance of the L C Tank circuit. The L C Tank circuit is at resonance , thus net Inductive Reactance  $j\omega L$  equals net Capacitive Reactance  $j/\omega C$ .

❖ Thus the last term of the coefficient matrix is zero i.e.  
 $\{ j\omega L_1 + j\omega L_2 - j/\omega C \} = 0$

Thus we have

$$\begin{vmatrix} \{ h_{ie} + j\omega L_1 - \left( \frac{h_{fe} \cdot h_{re}}{h_{oe}} \right) \} & \left( \frac{h_{re}}{h_{oe}} \right) & - j\omega L_1 \\ - \left( \frac{h_{fe}}{h_{oe}} \right) & \left( \frac{1}{h_{oe}} + j\omega L_2 \right) & - j\omega L_2 \\ - j\omega L_1 & - j\omega L_2 & 0 \end{vmatrix} = 0$$

Solving --

$$\{ h_{ie} + j\omega L_1 - (h_{re} h_{fe} / h_{oe}) \} \cdot (-j\omega L_2)^2 - (h_{re} / h_{oe}) \cdot \{ (-j\omega L_1) \cdot (-j\omega L_2) \} - (j\omega L_1) \cdot \{ (-h_{fe} / h_{oe}) \cdot (-j\omega L_2) - (-j\omega L_1) \cdot (1 / h_{oe} + j\omega L_2) \} = 0$$

Re-arranging

$$[(\{h_{ie} h_{oe} - h_{re} h_{fe}\} / h_{oe}) - j\omega L_1] \omega^2 L_2^2 - (h_{re} / h_{oe}) \omega^2 L_1 L_2 + \omega^2 L_1 L_2 (h_{fe} / h_{oe}) - (j\omega L_1) \{j\omega L_1 / h_{oe} - \omega^2 L_1 L_2\} = 0$$

Putting  $(h_{ie} h_{oe} - h_{re} h_{fe}) = \Delta h_e$  we have

$$(\Delta h_e / h_{oe}) \omega^2 L_2^2 - j \omega^3 L_1 L_2^2 - (h_{re} / h_{oe}) \omega^2 L_1 L_2 + (h_{fe} / h_{oe}) \omega^2 L_1 L_2 + (\omega L_1)^2 / h_{oe} + j \omega^3 L_1^2 L_2 = 0$$

Re-arranging

$$[(\Delta h_e \cdot \omega^2 L_2^2) / h_{oe}] + \{\omega^2 L_1 L_2 (h_{fe} / h_{oe} - h_{re} / h_{oe})\} + \{\omega^2 L_1^2 / h_{oe}\} + j \omega^3 L_1 L_2 (L_1 - L_2) = 0$$

❖ Now equating the real part to zero we get the "Condition for Oscillation" as follows -

$$[(\Delta h_e \cdot \omega^2 L_2^2) / h_{oe} + \omega^2 L_1 L_2 (h_{fe} / h_{oe} - h_{re} / h_{oe}) + \omega^2 L_1^2 / h_{oe}] = 0$$

$$\{\Delta h_e L_2^2 + L_1 L_2 (h_{fe} - h_{re}) + L_1^2\} \omega^2 = 0$$

Assuming  $h_{re} \ll h_{fe}$  we have

$$\Delta h_e L_2^2 + h_{fe} L_1 L_2 + L_1^2 = 0$$

- ❖ This is in the form of a quadratic equation. If we assume  $L_1$  is known, we can evaluate  $L_2$  in terms of  $L_1$  as

$$L_2 = \frac{-h_{fe} \cdot L_1 - \sqrt{(h_{fe} L_1)^2 - 4 \Delta h_e L_1^2}}{2 \Delta h_e}$$

Assuming  $h_{fe}^2 \gg 4 \Delta h_e$  we have the “Condition of Oscillation” as Equation 8 (a)

$$\begin{aligned} L_2 &= \frac{-2 h_{fe} L_1}{2 \Delta h_e} = \frac{-h_{fe} L_1}{\Delta h_e} \\ \therefore \frac{L_2}{L_1} &= \left| \frac{-h_{fe}}{\Delta h_e} \right| \quad \dots (8(a)) \end{aligned}$$

- ❖ Since  $L_1$  and  $L_2$  are components of the feedback loop, their ratio represents the feedback factor ‘ $\beta$ ’.

$$\frac{L_2}{L_1} = \left| \frac{-h_{fe}}{\Delta h_e} \right| = \beta \quad \dots (8(b))$$

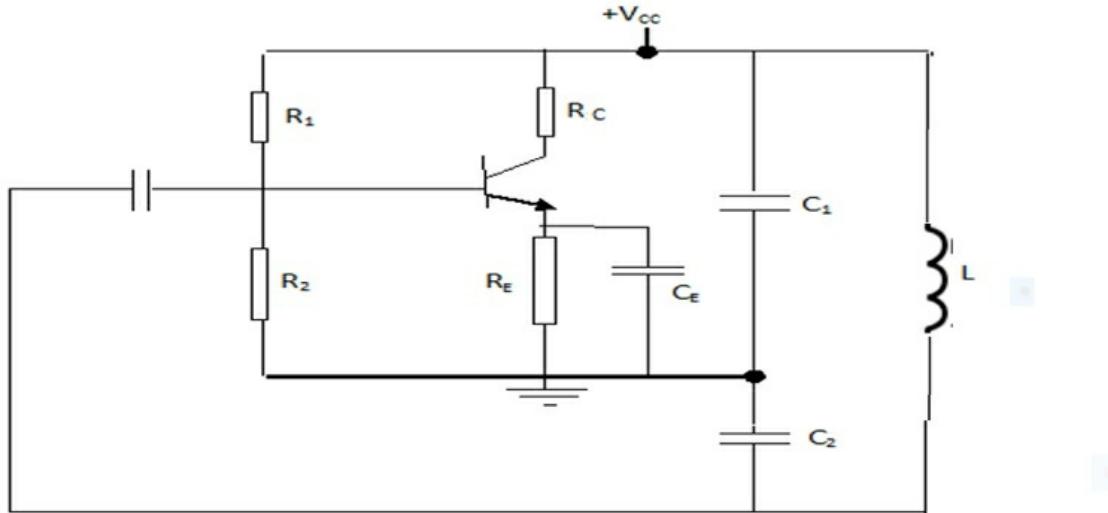
- ❖ Again, since the loop gain  $A \beta = 1$ , we will have the gain of the amplifier as

$$A = \frac{L_1}{L_2} \quad \dots (8(c))$$

- ❖ This “Condition for Oscillation” can be easily set up by adjusting the setting of the variable inductance of the collector circuit. A Transistor of any value of  $h_{fe}$  can be used.
- ❖ Since the condition is independent of the specific value of  $h_{fe}$ , thus the Ageing Factor of the transistor does not play any role in the operation of the circuit.

### Colpitts Oscillator

- In the Colpitts Oscillator, the Capacitance of the L C tank circuit is in the form of a series combination of two capacitors  $C_1$  and  $C_2$  as shown in the Fig. 6 below.



**Fig. 6: - Colpitts Oscillator**

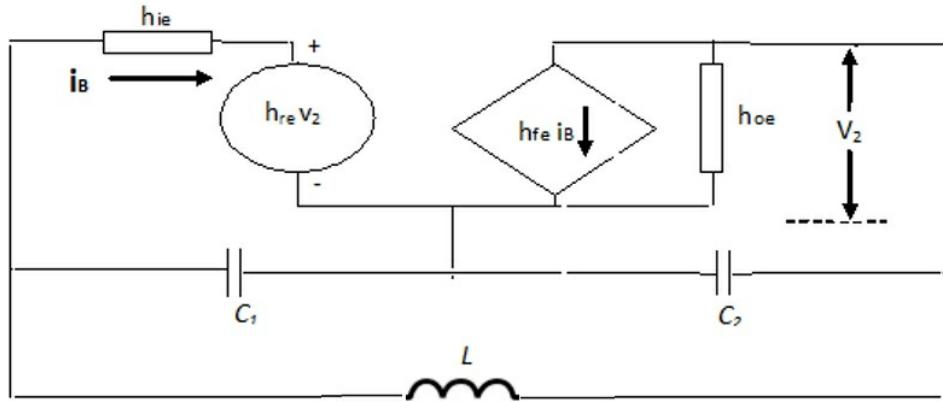
- As in case of the Hartley Oscillator, the frequency of oscillation is pre-determined by the values of the net capacitance,  $C$  of the series combination of  $C_1$  and  $C_2$  and the value of  $L$ , which is to be substituted in Eq. 6.
- The condition of oscillation is obtained by analyzing the circuit.

### ANALYSIS

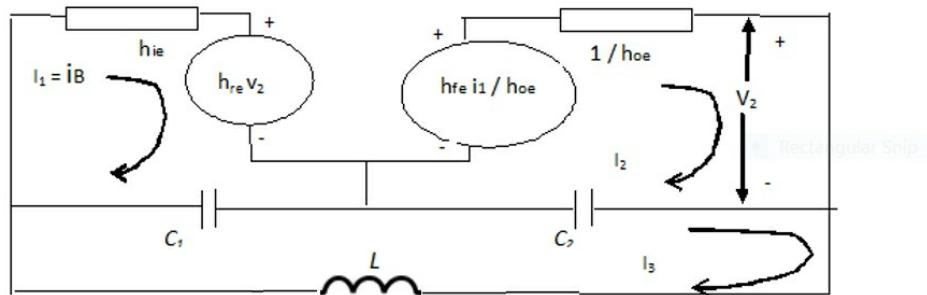
- Now redrawing the circuit by replacing the BJT with the h-parameter equivalent model with the Approximation that

$R_b \gg h_{ie}$ , we have,

- Replacing the Norton's equivalent at the collector terminal by the equivalent Thevenin's network, by replacing the Current Source with the equivalent Voltage Source  $h_{fe} i_B / h_{oe}$ .



- Since Base Current of the transistor is also the current  $I_1$  of the Loop-1, we can rewrite the voltage source as  $h_{fe} I_1 / h_{oe}$ . The parallel Admittance  $h_{oe}$  is replaced with the equivalent series Impedance  $1 / h_{oe}$  we have the above circuit being redrawn as follows



- Now the KVL Equations of the loops are as follows –

LOOP -1 :

$$(h_{ie} - j/\omega C_1) I_1 + (j/\omega C_1) I_3 = h_{re} V_2$$

Substituting for  $V_2$  as

$$V_2 = V_2 = \left( \frac{h_{fe} I_1}{h_{oe}} \right) - \left( \frac{I_2}{h_{oe}} \right)$$

We have

$$(h_{ie} - j/\omega C_1) I_1 + (j/\omega C_1) I_3 = h_{re} \{ (h_{fe} I_1 / h_{oe}) - (I_2 / h_{oe}) \}$$

Rearranging and simplifying we have

$$\{ h_{ie} - h_{re} h_{fe} / h_{oe} - (j/\omega C_1) \} I_1 + (h_{re} / h_{oe}) I_2 + (j/\omega C_1) I_3 = 0$$

$$\{ (h_{ie} h_{oe} - h_{re} h_{fe}) / h_{oe} - (j/\omega C_1) \} I_1 + (h_{re} / h_{oe}) I_2 + (j/\omega C_1) I_3 = 0$$

$$\{ (\Delta h_e / h_{oe}) - (j/\omega C_1) \} I_1 + (h_{re} / h_{oe}) I_2 + (j/\omega C_1) I_3 = 0 \quad \dots(a)$$

LOOP - 2 :

$$\{ (1/h_{oe}) - (j/\omega C_2) \} I_2 + (j/\omega C_2) I_3 = (h_{fe} / h_{oe}) I_1$$

$$- (h_{fe} / h_{oe}) I_1 + \{ 1/h_{oe} - (j/\omega C_2) \} I_2 + (j/\omega C_2) I_3 = 0 \quad \dots(b)$$

LOOP - 3 :

$$(j/\omega C_1) I_1 + (j/\omega C_2) I_2 + \{ j\omega L \} - (j/\omega C_1) - (j/\omega C_2) I_3 = 0 \quad \dots(c)$$

- In order to solve this set of simultaneous equations by Kramer's rule , we equate the Determinant of the coefficient matrix to zero.

Thus we have the Determinant of the coefficient matrix as follows ---

$$\begin{vmatrix} \{(\Delta h_e / h_{oe}) - (j/\omega C_1)\} & (h_{re} / h_{oe}) & (j/\omega C_1) \\ - (h_{fe} / h_{oe}) & \{1/h_{oe} - (j/\omega C_2)\} & (j/\omega C_2) \\ (j/\omega C_1) & (j/\omega C_2) & \{ (j\omega L) - (j/\omega C_1) - (j/\omega C_2) \} \end{vmatrix} = 0$$

- The L C Tank circuit is at resonance , thus net Inductive Reactance  $j\omega L$  equals net Capacitive Reactance  $(j/\omega C_1) - (j/\omega C_2)$  .

Thus the last term of the coefficient matrix is zero i.e.

$$\{ (j\omega L) - (j/\omega C_1) - (j/\omega C_2) \} = 0$$

- Thus we have ---

$$\begin{vmatrix} \{\Delta h_e / h_{oe}\} - (j/\omega C_1) & (h_{re}/h_{oe}) & (j/\omega C_1) \\ - (h_{fe}/h_{oe}) & \{1/h_{oe} - (j/\omega C_1)\} & (j/\omega C_2) \\ (j/\omega C_1) & (j/\omega C_2) & 0 \end{vmatrix} = 0$$

Solving the determinant

$$\{(\Delta h_e/h_{oe}) - (j/\omega C_1)\}.(j/\omega C_2)^2 - (-h_{fe}/h_{oe}).\{-(j/\omega C_1).(j/\omega C_2)\} + (j/\omega C_1).[(h_{re}/h_{oe}).(j/\omega C_2) - \{1/h_{oe} - (j/\omega C_1)\}.(j/\omega C_1)] = 0$$

⊕ Simplifying

$$[\Delta h_e / (h_{oe} \omega^2 C_2^2) + \{ (h_{fe} - h_{re}) / h_{oe} \omega^2 C_1 C_2 \}] + \\ 1 / h_{oe} \omega^2 C_1^2] - \{ j / \omega^3 C_1 - j / \omega^3 C_1^2 C_2 \} = 0$$

- Now Equating the Real Part to zero we get the “Condition of Oscillation” as follows

$$\Delta h_e / (h_{oe} \omega^2 C_2^2) + \{ (h_{fe} - h_{re}) / h_{oe} \omega^2 C_1 C_2 \} + 1 / h_{oe} \omega^2 C_1^2 = 0$$

⊕ Removing the common denominator  $h_{oe} \omega^2$  we have

$$\Delta \underline{h_e} / C_2^2 + \{ (h_{fe} - h_{re}) / C_1 C_2 \} + 1 / C_1^2 = 0$$

⊕ Multiplying throughout by  $C_1^2$  & neglecting  $h_{re}$  w.r.t.  $h_{fe}$

$$\Delta h_e (C_1 / C_2)^2 + h_{fe} (C_1 / C_2) + 1 = 0$$

⊕ Solving for  $(C_1 / C_2)$  we have

$$\frac{C_1}{C_2} = \frac{-h_{fe} \sqrt{h_{fe}^2 - 4\Delta h_e}}{2\Delta h_e}$$

Now taking  $h_{fe}^2 \gg 4\Delta h_e$  we have

$$(C_1 / C_2) = (-h_{fe} / \Delta h_e)$$

The **“Condition of Oscillation”** is

$$\frac{C_1}{C_2} = \left| \frac{-h_{fe}}{\Delta h_e} \right| \quad \dots(9(a))$$

In this case, the ‘Condition Of Oscillation’ represents the ‘Reciprocal of Feedback Factor’  $1/\beta$ .

Thus

$$\frac{1}{\beta} = \left| \frac{-h_{fe}}{\Delta h_e} \right| \quad \dots(9(b))$$

Since loop gain ‘A  $\beta$ ’ must be unity, we have the value of the Gain of the amplifier as

$$A = \frac{1}{\beta} = \frac{C_1}{C_2} \quad \dots(9(c))$$

- This Condition for oscillation is also easy to set up since this is independent of the individual h-parameter value but rather on the ratio.
- Usually one or both the capacitors are made variable and they are adjusted in such a manner that the circuit begins to show sustained sinusoidal oscillation at the predetermined frequency, when observed on CRO.

**Hence in practice both Hartley & Colpitts’s Oscillator are widely used.**

### Crystal Oscillators

While analyzing RC oscillators and LC oscillators, it was seen that the frequency of oscillation is a function of the values of the components of the feedback path. That is, the frequency of oscillation of a Phase Shift oscillator or a Wien Bridge oscillator would depend on the values of the resistors R and the capacitors C in the feedback loop ; whereas in

a Hartley or Colpitts oscillator it would depend on the values of the inductor L and the capacitor C. The values of these components as available in the market are not constant. A batch of a certain component

may have approximately  $\pm$  10 % variation in values. Further, these components' values change with both ambient temperature as well as operating temperature. Hence output of these oscillators is not absolutely stable.

When a piezoelectric crystal is used as the feedback path component, absolutely stable oscillation is possible.

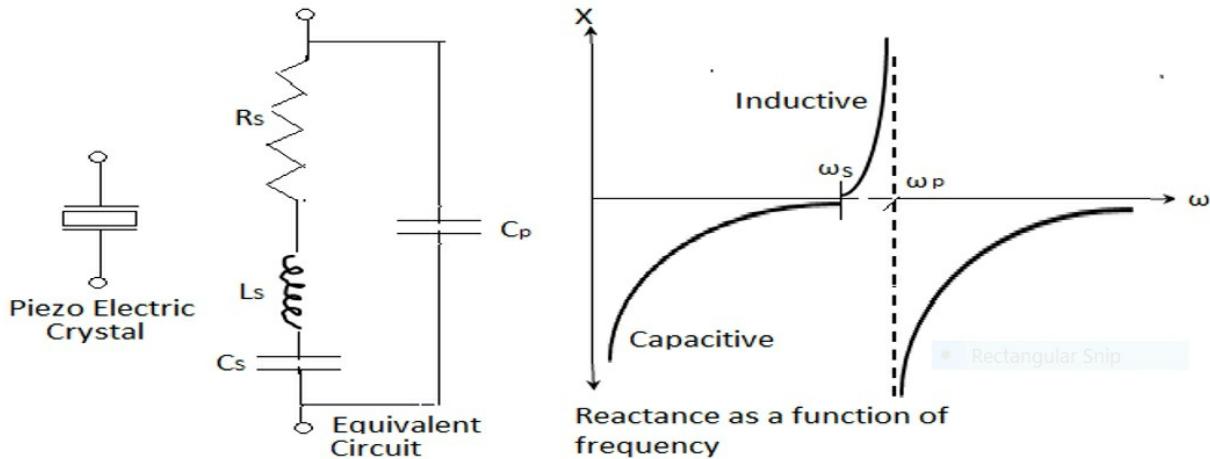
The property of a piezoelectric crystal is that, when such a crystal is subjected to mechanical pressure, an electric potential is developed across its surface, and vice versa. The frequency of the electrical signal is a function of the geometry and shape of the crystal. Since the shape and geometry of a piezoelectric crystal does not vary with temperature and other environmental factors, the frequency of oscillation remains stable over a long period of time, and under various operating and ambient temperatures.

Crystal oscillators are also based on the general configuration. The Feedback path contains a piezoelectric crystal. When the DC bias is switched on, the crystal produces a square wave pulse train. The frequency of oscillation is determined by the geometry of the crystal. When this is fed-back to the amplifier, the signal is amplified. The collector circuit of the amplifier contains a tuned circuit, which is tuned at the fundamental frequency of the square wave signal. Thus sustained sinusoidal oscillations are produced. Even though, theoretically, a crystal oscillator can be designed to oscillate at any frequency, in practice the practical dimensions at which a crystal can be fabricated, predetermines the frequency of oscillation to be very high. Crystal oscillators are designed to produce highly stable oscillations at a high frequency ranging from hundreds of Mega Hertz to hundreds of Giga Hertz.

### **Properties of Quartz Crystal**

Quartz is a naturally occurring piezoelectric crystal. For the purpose of using it in an electronic circuit it is packaged as either a hermetically sealed or vacuum sealed capsule with two leads being mounted

internally across the opposite faces of the crystal. Such a package will be represented by an electrical equivalent circuit as shown in the Fig. 7 below. The figure also shows the variation of impedance of the crystal as a function of frequency. In the equivalent circuit, the capacitance  $C_p$  is the ‘Parasitic Capacitance’ between the terminals, with the piezoelectric material as the di-electric. The series elements,  $R_s$ ,  $L_s$  and  $C_s$  respectively, are analogs of the mechanical parameters of the crystal.



**Fig. 7: - (a) Symbol of a Piezoelectric Crystal: (b) The Electrical Equivalent Circuit and (c) Reactance as a function of working frequency (Assuming  $R_s \rightarrow 0$ ).**

Hence these parameters depend upon the physical geometry of the crystal. The physical geometry also determines the resonant frequency of the crystal. For a 90 kHz crystal, the typical values are ;  $R_s = 15 \text{ K}$  ,  $L_s = 137 \text{ H}$  ,  $C_s = 0.023 \text{ pF}$  and  $C_p = 3.5 \text{ pF}$ . A quantity known as ‘Q-Factor’ is associated with a resonant circuit, which is defined as the ratio of Reactance to Resistance. The higher the value of Q , the lesser is the variance in the resonant frequency. Piezoelectric crystals have a very high Q-Factor. Therefore, the frequency of oscillation of the signal produced by the crystal is highly stable.

### Series Resonant Frequency and Parallel Resonant Frequency

If we neglect the resistance, the reactance as a function of frequency is expressed as

$$jX = -\frac{j}{\omega C_p} \cdot \frac{(\omega^2 - \omega_s^2)}{(\omega^2 - \omega_p^2)}$$

Where,  $\omega_S^2$  is the resonant frequency associated with the series combination of  $L_S$  and  $C_S$ , assuming impedance is zero, so that

$$\omega_S^2 = 1 / L_S C_S \dots(10)$$

And  $\omega_P^2$  is the resonant frequency associated with the series-parallel combination of  $L_S$ ,  $C_S$  and  $C_P$ , assuming impedance is infinity, so that

$$\omega_P^2 = (1/L_S) \cdot (1/C_S + 1/C_P) \dots(11)$$

Since the typical values of the crystal parameters are such as illustrated above, that  $C_P \gg C_S$ , we will have  $\omega_S \approx \omega_P$ . This is seen in the Fig. 7.

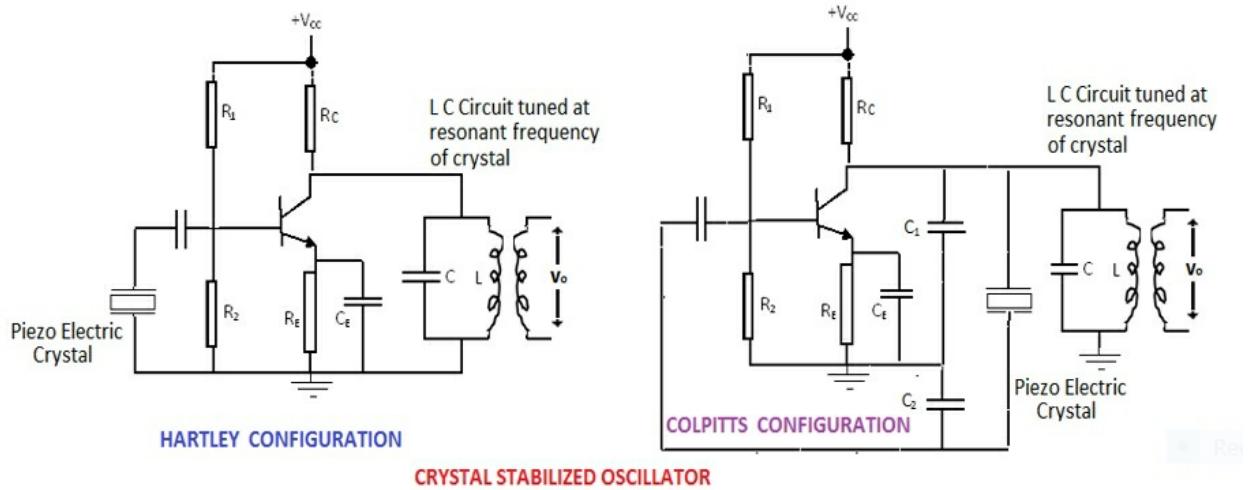
In case of any resonant circuit, a quantity known as ‘Critical Frequency’ exists, above which, the reactance is Inductive and below this, the reactance is Capacitive. This is applicable to the quartz crystal also, as seen in the graph of Reactance (X) versus Frequency (f), in the Fig. 7. In case of the Quartz Crystal, the Series Resonant frequency  $\omega_S$  is the Critical Frequency. However, due to the special physical characteristics required to be imparted to the crystal during the process of manufacturing, the Parasitic Capacitance  $C_P$  appears in parallel. Due to this the quantity  $\omega_P$  comes into the picture. For frequencies above  $\omega_P$ , the reactance becomes Capacitive. It is convenient to use the crystal in the range of the Inductive reactance, rather than that of the Capacitive reactance. Thus we have a certain range of working frequencies defined as

$$\omega_S < \omega < \omega_P \dots(12)$$

### **Crystal Controlled Oscillator Circuit**

Either a Hartley Oscillator or a Colpitts Oscillator with a crystal in the feedback loop is a ‘Crystal Stabilized’ oscillator. Such configurations with either a BJT or a JFET is commonly used in practice. Two circuits, one with a Hartley configuration and the other with a Colpitts configuration are shown in the Fig.8 below. The crystal is connected in parallel in the Feedback Loop. Since the working frequency range is chosen for the crystal to operate as an inductive reactance, it is used in place of the inductor in both the configurations. The use of the crystal stabilizes the frequency of oscillation near the series resonant frequency of  $\omega_s$  ( $f_S$ ). The output terminal contains a LC tuned circuit tuned at the desired frequency of oscillation. It is primarily

for the purpose of coupling the output signal to the external load.



**Fig.8.: - Crystal Controlled Oscillators in Hartley and Colpitts Configurations**

### TUTORIAL

**Example 5 :-** Design the feedback path of a Hartley Oscillator to produce 5V peak sinusoidal output at 100 kHz frequency. The Amplifier part has a gain of  $|A|=10$  and uses a transistor with  $h_{oe} = 40 \text{ micro-mho}$ . Neglect mutual inductance  $e$  between the two parts of the inductor.

#### **SOLUTION ::**

In a Hartley Oscillator it is required that the inductive reactance of the second part of the inductor be much larger than the output impedance of the amplifier.

$$X_{L2} \ll Z_0.$$

$$\text{Where } Z_0 = 1 / h_{oe}$$

Substituting for  $h_{oe} = 40 \times 10^{-6} \text{ mho}$ , we have

$$Z_0 = 25000 \Omega = 25 \text{ K.}$$

$\therefore$  Let  $X_{L2} = 1 \text{ K.}$

For the desired frequency of oscillation of 100 kHz we have

$$L_2 = \frac{1 \times 10^3}{2 \pi \times 100 \times 10^3} = 1.59 \text{ mH}$$

Given A = 10

In a Hartley Oscillator, the gain is given by Eq. 9(b) as

$$A = \frac{L_1}{L_2}$$

$$\therefore L_1 = A L_2 = 10 \times 1.59 = 15.9 \text{ mH}$$

Total Inductance is  $L_T = L_1 + L_2 = 15.9 + 1.59 = 17.49 \text{ mH}$

The expression for frequency of oscillation is given by Eq. 6 as

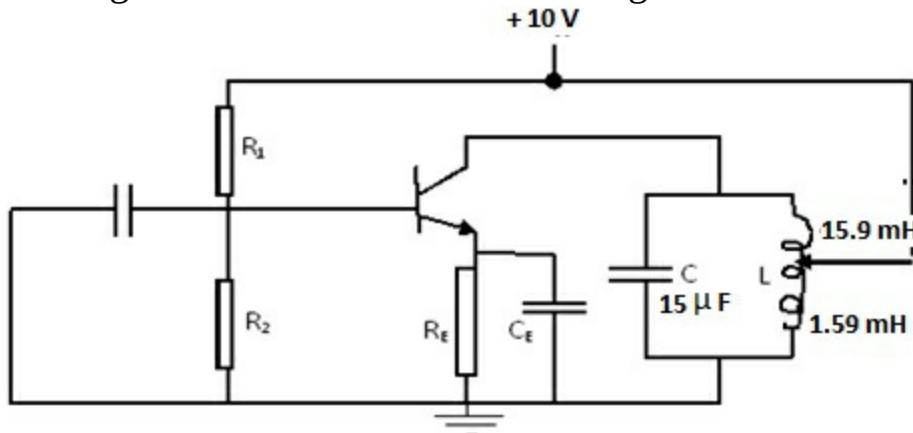
$$f = \frac{1}{2\pi\sqrt{(L_T C)}}$$

From this we get

$$C = \frac{1}{4\pi^2 f^2 L_T} = \frac{1}{4\pi^2 \times 100000^2 \times 17.49 \times 10^{-3}}$$

$$= 1.5 \times 10^{-5} \text{ F} = 15 \mu\text{F}.$$

The designed circuit is as shown in the figure below



**Example 6:** – Design a Colpitts Oscillator to produce 500 kHz sinusoidal oscillation with 6V peak value using a coil of inductance 1mH and a transistor having h-parameter values  $h_{ie} = 11 \text{ K}$ ,  $h_{re} = 5 \times 10^{-5}$ ,  $h_{fe} = 100$ ,  $h_{oe} = 46 \times 10^{-6} \text{ mho}$ .

**SOLUTION ::**

Rearranging the expression for frequency of oscillation given by Eq. 6 we have

$$C_T = \frac{1}{4\pi^2 x (500 \times 10)^2 \times 1 \times 10^{-3}} = 1.01 \times 10^{-10} F \approx 100 \text{ pF}$$

Further, condition of oscillation in a Colpitts Oscillator given by Eq. 10.10(a) is

$$\frac{C_1}{C_2} = \frac{h_{fe}}{\Delta h_e}$$

Where

$$\Delta h_e = h_{ie} h_{oe} - h_{fe} h_{re}$$

Substituting the given h-parameter values

$$\Delta h_e = 11 \times 10^3 \times 46 \times 10^{-6} - 100 \times 5 \times 10^{-5} = 0.501$$

$$\therefore \frac{C_1}{C_2} = \frac{100}{0.501} = 199$$

$$\therefore C_1 = 199 C_2$$

Since  $C_1$  and  $C_2$  are in series,

$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$

$$\therefore C_T \approx C_2$$

$$\text{Or } C_2 = 100 \text{ pF}$$

And

$$C_1 = 100 \times 10^{-12} \times 199 = 0.0000000199 \text{ F}$$

$$\text{Or } C_1 \approx 0.02 \mu\text{F}.$$

To produce a 6V peak sinusoid, the amplifier part has to be designed as a Class-A amplifier driven by  $V_{CC} = 12 \text{ V}$  and having a gain given by

Eq. 10.11(c) as

$$A_V = \frac{C_1}{C_2} = 199$$

$$\text{Let } A_V \approx 200$$

Load impedance on the amplifier is the parallel combination of  $X_L$  and  $X_{CT}$

$$\text{At the frequency of } f = 500 \text{ kHz}$$

$$X_L = 2 \pi \times 500 \times 10^3 \times 1 \times 10^{-3}$$

$$= 3141 \Omega = 3.14 \text{ K}$$

And  $X_{CT} = 1 / (2 \pi \times 500 \times 10^3 \times 100 \times 10^{-12})$

$$= 3184 \Omega = 3.18 \text{ K}$$

$$\therefore |Z_L| = \frac{3.14 \times 3.18}{3.18 - 3.14} = 249.6 \approx 250 \text{ K}$$

Net Load impedance is the parallel combination of  $R_C$  and  $Z_L$

Assume a "Standard Value Resistance"  $R_C = 470 \Omega = 0.47 \text{ K}$

$$\therefore Z_L' = \frac{0.47 \times 250}{0.47 + 250} = 0.469 \text{ K} \approx 470 \Omega$$

We need an amplifier with a gain  $A_V = 200$

For a CE amplifier we have

$$|A_V| = \frac{R_C}{r_e'}$$

Where  $r_e'$  is the internal resistance of the forward biased Emitter –Base junction.

Substituting for  $R_C$  and  $A_V$ , we have

$$r_e' = 470/200 = 2.35 \Omega$$

In this, Let  $r_E = 2.7 \Omega$  ( Standard Value )

The empirical formula for  $r_e'$  is

$$r_e' = \frac{25}{I_E(\text{mA})}$$

where  $I_E$  is the Biasing Current at the Emitter terminal in mA scale.

$$\therefore I_E = 25/2.7 = 9.26 \text{ mA}$$

Let  $I_{CQ} = I_E$

$$\therefore I_{CQ} = 9.26 \text{ mA}$$

Given  $V_{CC} = 12 \text{ V}$

Assuming Q-Point to be mid-point of Load Line we have

$$V_{CEQ} = \frac{1}{2} V_{CC} = 6 \text{ V} \quad \text{and} \quad I_{C(Sat)} = 2 I_{CQ} = 18.5 \text{ mA}$$

Where  $I_{C(Sat)} = \frac{V_{CC}}{(R_C + R_E)}$  ; Where  $R_E$  is the total resistance at the Emitter.

$$\therefore (R_C + R_E) = \frac{V_{CC}}{I_{C(Sat)}} = \frac{12}{18.5} = 0.6487 \text{ K} = 648.7 \Omega$$

We had assumed  $R_C = 470 \Omega$

$$\therefore R_E = 648.7 - 470 = 178.7 \approx 180 \Omega \quad (\text{Standard Value})$$

This resistance is to be Bypassed with a capacitor.

For a Voltage Divider Bias Circuit we have

$$\frac{R_b}{R_E} = \frac{(S-1)(1+\beta)}{1+\beta-S}$$

Where  $R_b$  is the Thevenin's equivalent resistance at the base terminal and 'S' is the Stability Factor.

Let  $S = 5$  and  $\beta \approx h_{fe} = 100$

Substituting

$$\frac{R_b}{R_E} = \frac{(5-1)(1+100)}{1+100-5} = 4.2$$

$$\therefore R_b = 4.2 \times 180 = 756 \Omega = 0.756 \text{ K}$$

In the biasing circuit, the biasing voltage  $V_2$ , across the Base and ground is given by

$$V_2 = I_{BQ} R_b + V_{BE} + (I_{CQ} + I_{BQ}) R_E$$

Assuming a Si transistor  $V_{BE} = 0.7 \text{ V}$ . With  $R_E = 180 \Omega = 0.18 \text{ K}$

$$I_{BQ} = I_{CQ}/\beta = 9.26/100 = 0.093 \text{ mA}$$

Substituting

$$V_2 = 0.093 \times 0.756 + 0.7 + (9.26 + 0.093) \times 0.18 = 2.45 \text{ V}$$

The resistances in the voltage divider part of the biasing circuit are given by

$$R_1 = R_b \frac{V_{CC}}{V_2} \quad \text{AND} \quad R_2 = \frac{R_1 V_2}{V_{CC} - V_2}$$

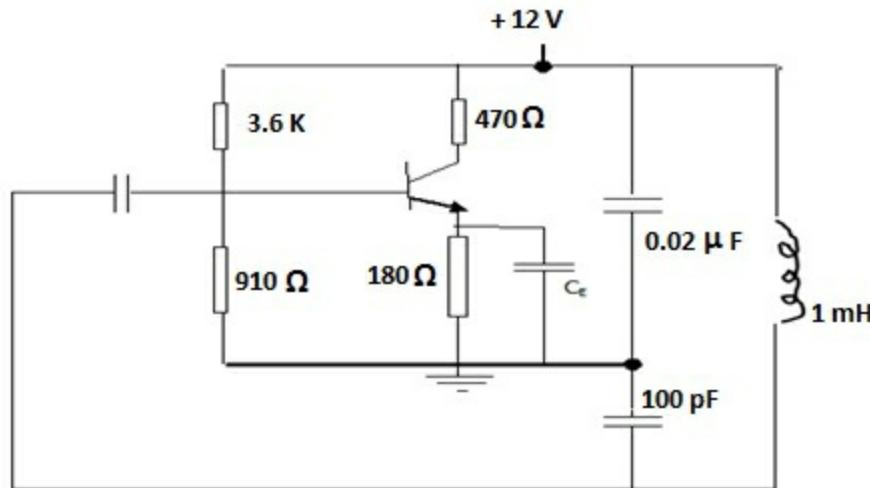
Substituting

$$R_1 = 756 \frac{12}{2.45} = 3702.86 \Omega = 3.7 \text{ K} \approx 3.6 \text{ K} \quad (\text{Standard Value})$$

AND

$$R_2 = \frac{3.6 \times 2.45}{(12 - 2.45)} = 0.923 \text{ K} \approx 910 \Omega \quad (\text{Standard Value})$$

Thus, the complete circuit is as shown in the figure below



XXXXXXXXXXXX OOOO XXXXXXXXXXXX

# **UNIT - 3**

## **OPAMP THEORY AND APPLICATIONS**

# **CHAPTER – X**

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# **ELECTRONICS OF ANALOG INTEGRATED CIRCUITS**

*Introduction to OPAMPS*

## **INTRODUCTION**

Various applications of discrete electronic devices, namely Diodes, BJT and FET had been studied in the previous chapters. In these circuits, the various Electronic Devices and passive circuit elements, such as Resistors, Capacitors and Inductors were interconnected by wires, with the help of soldered joints. Modern day electronics industry has evolved up to a level wherein it has become possible to “Integrate” millions of active electronic components as well as some passive elements within a tiny wafer of silicon and interconnect them into a complete circuit by means of “Micro-Joints”. These are called Integrated Circuits, abbreviated as ICs. This has multiple practical advantages, as enumerated below. Hence the ICs are quickly dominating various applications in modern day electronic industry. The technology is such that exactly identical ICs can be designed to perform a specific task and these can be mass produced within predetermined global standards. This feature has made it possible to drastically reduce both the physical size as well as production cost of various electronic gadgets, at the same time increasing sophistication levels in them.

### **Why ICs ?**

Electronics as a branch of Engineering plays two vital roles, namely,

1. Enable the working of various Communication Engineering Operations.
2. Monitoring and Control of various other complex Engineering and Physical Systems such as Electrical, Mechanical, Chemical, Bio-Medical or Civil Engineering systems.

Quite often these two tasks are combined in an Electronic System. For example, in the field of Electrical Power Engineering, the functioning of a Grid has to be constantly monitored and any fault that may occur need to be predicted as well as corrected. Similarly, a vehicle can run most effectively if an electronic controller is installed to provide an optimal fuel supply to the engine. In the Transportation Sector, efficient control of traffic is a vital necessity. Modern Space Science and Defense Operations require sophisticated monitoring and control operations. Most of these tasks also require sophisticated calculations, which need to be performed in a span of microseconds or less. Hence these tasks cannot be performed manually. Electronics Industry developed on this very necessity.

Digital computers started to emerge in the 1940s. The earliest computers were huge in size and used to require an enormously large amount of electrical energy to operate. With the increasing use of Semiconductor devices, the circuits became much smaller in size and much more efficient. Thereafter, a complete circuit, consisting of thousands of transistors and associated components and capable of performing a specific task, , could be integrated in a single microchip (wafer) of Silicon. This complex Electronic Micro Circuit is sealed within a small plastic or metal capsule. Only the electrical leads for electrical connections are visible outside. Thus a complex circuit can be represented as a block, with only the external connections shown outside. The following points summaries the answer to the question – “Why ICs ?”

### **Advantages of using ICs**

1. Complex Electronic Systems can be integrated and assembled within a very small physical space.

2. Absence of ‘Parasitic Capacitance’ makes the operations involving ICs very fast.
3. Since the ICs require very little amount of Electrical power, they can be operated with small DC Batteries and hence can be operated for very long time even in Remote Outer Space or the Deep Sea.
4. Complex Electronic systems can be designed by using a block diagram to represent a specific task, without actually designing the internal circuitry of every subsystem.
5. Manufacturing process of ICs have been so highly standardized that any specific IC manufactured for a specific application by each and every manufacturer worldwide, have exactly the same characteristics. Hence ICs can be mass produced. This results in a very low cost of production and highly reliable operation.

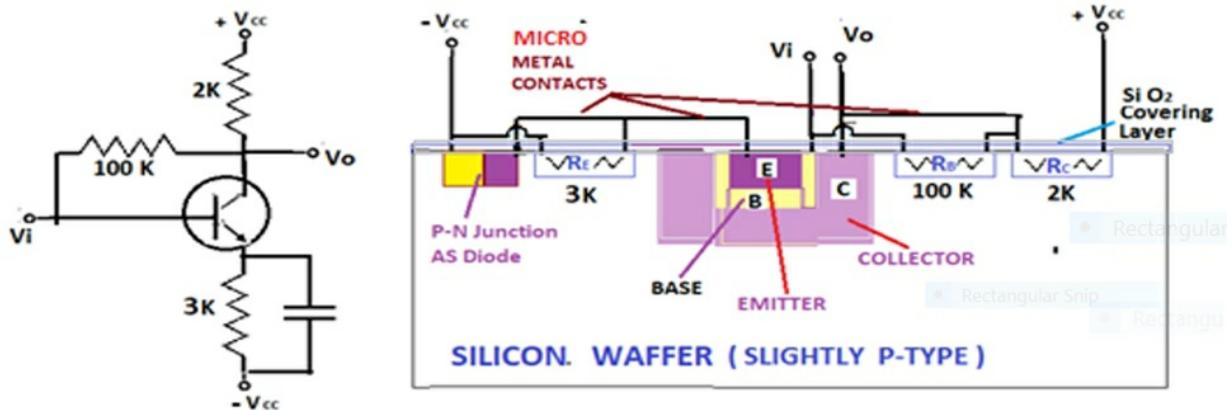
## 10.1 Fabrication of IC

The reader will recall that a pre-determined number of trivalent or pentavalent impurities can be doped into a piece of Intrinsic Silicon to obtain P-Type and N-Type semiconductors, of a desired conductivity, respectively. For this, the piece of Silicon is heated to melting point and subjected to a vapor of the dopant so that a desired amount of dope atoms diffuse into the molten silicon. Thereafter the mixture of the desired concentration of the dope and liquid silicon is cooled to form a solid crystal. One portion of the piece of silicon can be doped with P-Type dope and the other with N-Type dope. This will result in the formation of a P-N Junction. In a similar way, one region of silicon, say, N-Type, may be sandwiched between two P-Type regions to form a PNP Transistor, or, vice-versa, as an NPN Transistor. The process can be used to form P-N Junctions with any desired concentration of dopes on either side. Readers will recall that a P-N Junction also has the properties of “Diffusion Capacitance” and “Transition Capacitance”. In other words, the P-N junction also behaves as a Capacitor (**Chapter II**). Again, the concentration of dopes in a piece of silicon also determines the Conductivity (**Chapter I**). Thus

it is possible to integrate “Resistors” of any desired values of resistance.

By this process, any number of P-N Junctions (Either as Diodes, Capacitors or Transistors), and Resistors can be Integrated on a single chip of silicon, to form an IC. To understand this, let us consider a simple circuit and it's form as an Integrated Circuit as shown in Fig-1. The steps for fabrication of this simple IC is as follows.

- A thin wafer of Silicon, which is slightly doped with P-Type dope is taken. This is called a “Substrate”. A portion “C” of a pre-calculated dimension is heated with a LASER so as to bring this portion to melting point. A vapour of N-Type impurity of a pre-calculated concentration is blown into the molten portion “C” of the wafer. Next, a very low concentration vapour of P-Type dope is injected into the portion “B” and a much higher concentration of N-Type vapour is injected into the portion “E”. After cooling, the Portion “E” becomes a highly doped N-Region and Portion “C” becomes a slightly less doped N-Region, with a very thin and very lightly doped P-Region sandwiched in between the “E” and “C” regions. This forms an NPN transistor.
- A certain pre-calculated portion of the wafer, marked “ $R_C$ ” is doped with a certain pre-calculated concentration of N-Type dope so that the resistance of this portion becomes 2K. Another portion “ $R_B$ ” is doped with a lesser concentration of N-Type dope so that the resistance of this portion is much higher, at 100K. Similarly a resistor of 3K is created the portion marked “ $R_E$ ”. Again, by doping a portion of the wafer with a desired concentration of N-Type dope and the adjacent portion with P-Type dope, a P-N Junction is created.



**Fig. 1:** - A simple amplifier circuit and A Simplified Layout of components in an IC.

- Aluminum “Micro Joints” are used to interconnect the various portions to complete the circuit. An Aluminum lead connected to one end of the resistance  $R_C$  to form the terminal to connect  $+V_{CC}$ . The other end of this 2K resistor is connected the Collector of the NPN transistor and one of the ends of the resistor  $R_B$ . The other end of this resistor  $R_B$  is then connected to the Base of the transistor. The Emitter of the transistor is connected to one end of the 3K resistor  $R_E$  as well as the N-Region of the P-N Junction. The other end of the resistor  $R_E$  and the P-Region of the P-N Junction are connected to the external lead for  $-V_{CC}$ . The connections for the input and output signals are connected to the Base and the Collector portions respectively. In this way, the P-N Junction will come in parallel, across the resistor  $R_E$  and will operate in Reverse Bias. Thus it will be equivalent to a Capacitor across  $R_E$ .
- After all the interconnections are completed, the upper surface of the wafer is sealed with an insulating layer of  $Si\ O_2$  . The complete package has a very small physical dimension of the order of only a few micrometers or nanometer. The wafer is now hermetically sealed in a small plastic or metal container, with the external leads kept outside. With modern technology, it is possible to integrate hundreds of thousands of transistors in a single chip of

silicon. Hence, we have the various families of ICs, classified as SSI (Small Scale Integration), MSI, LSI, VLSI, ULSI to GSI (Gigantic Scale Integration). The table below presents a summary of history and application of various IC families

**Table 1:** - Classification of ICs

Family	Number of Transistors per Chip	Year of Introduction	Typical Applications
SSI	10 -100	1963	Logic gates and OPAMPS and other Linear ICs.
MSI	100 - 1000	1966	Filters, Flip-Flops, Registers and Counters.
LSI	1000 – 100,000	1975	8-bit Microprocessors, 64kbit RAM/ROM and ADC.
VLSI	100,000 – 500,000	1986	16/32 bit Microprocessors, 256 kbit RAM/ROM and Signal Processors.
ULSI	> 500,000	1994	64 bit Microprocessors, 8 Mb RAM and Real Time Image Processors.
GSI	> 10,000,000	2000	Integrated Multiprocessors with 64 Mbit RAM

## 10.2A Digital IC and An Analog IC

Let us now look at the internal circuit diagrams of two commonly used ICs. The TTL IC 7400 is a commonly used Digital IC containing four identical NAND Gates. The other one, namely, 741 is a common Analog IC, functionally called The OPAMP. The detailed internal circuit diagram and the commercial IC Packages with their external terminals are shown in Fig. 2(a) . These two are examples of typical ICs that are very widely used in their respective fields and are manufactured by various manufacturers all over the world, with exactly identical standard specifications and characteristics. For this purpose, all the circuit elements in the circuits of the respective manufacturers have to have exactly the same value of resistors and the same dimension and doping concentration in the corresponding transistors and diodes. Such a stringent requirement

can only be met using a strictly controlled and highly sophisticated standard manufacturing process.

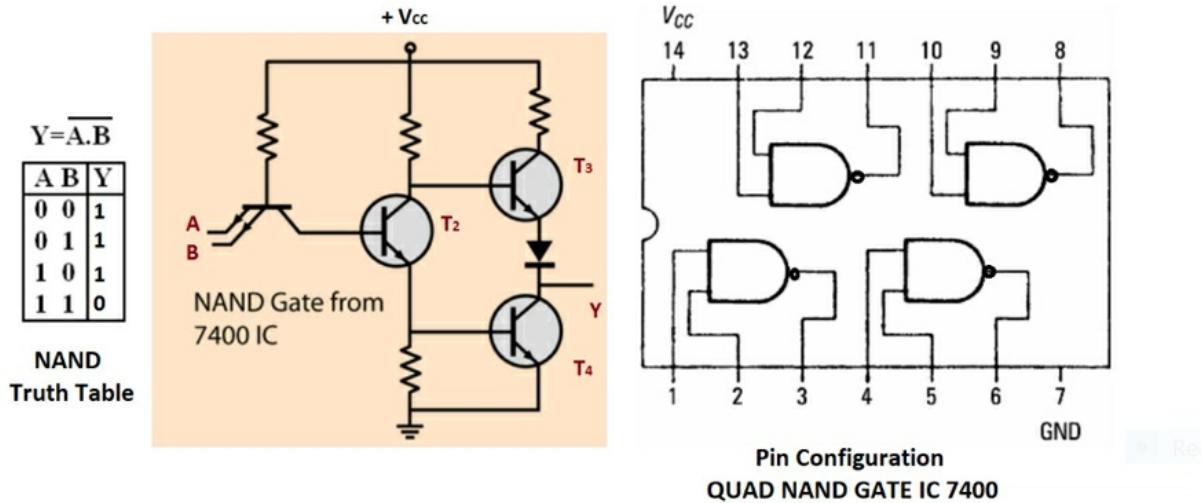


Fig. 2(a)

**TTL NAND Gate (IC 7400):** - The reader is to note that Digital Logic gate circuits are built with Analog Electronic components. The family of ICs based on circuits comprising of BJT and biasing resistors belong to a category of ICs designated as the **TTL Family** (Transistor-Transistor Logic). There is another family of Digital Logic ICs comprising of complementary pairs of N-Channel and P-Channel MOSFETS, named as the **CMOS Family** (Complementary Symmetry MOSFET).

A NAND Gate is a Digital Circuit to implement the Logical Function described by the Truth Table shown in the figure. It is one of a category of Gates, known as Universal Gates, a set of which can be configured to implement any Boolean Logic Expression. The other one being the NOR gate. Hence these can be considered to be the heart of any Digital System.

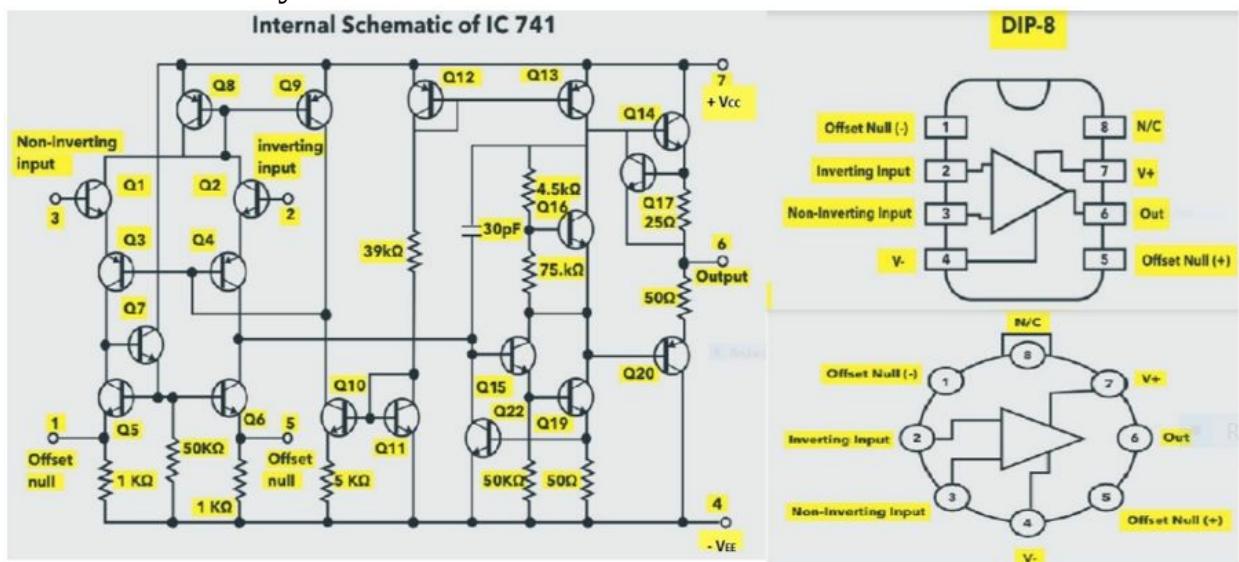
An inspection of the NAND Gate circuit (Fig. :- 2) reveals that it contains a ‘Special’ NPN Transistor,  $T_1$ , having **two independent Emitter terminals**. The Logic inputs, ‘A’ and ‘B’ are applied as the input to these terminals. Consider a situation in which Logic ‘0’ is applied to either or both of these input terminals. Logic state of ‘0’ corresponds to an electrical potential of 0 V. The Base terminal of  $T_1$  is at a potential of + 5 V. A potential of + 5 V at the base

and 0 V at the emitter of an NPN Transistor drive it into ‘Hard Saturation’. Recall that, at Saturation condition, the collector potential ( $V_{CE(SAT)}$ ) of the transistor is driven to 0 V. This potential is now applied to the base of  $T_2$ . A potential of 0 V at the base of an NPN Transistor drives it into ‘Cut-Off’. At Cut-Off, the collector potential is  $+V_{CC}$  and the emitter potential is 0 V. The 0 V emitter potential of  $T_2$  is the base potential of  $T_4$  and the +5 V collector potential of  $T_3$  is the base potential of  $T_3$ . Thus  $T_3$  driven into Hard Saturation and  $T_4$  is driven into Cut-Off. A transistor at Cut-Off is an Open Switch and at Hard Saturation, it is a closed switch. Thus the output terminal ‘Z’ is disconnected from Ground and short circuited to +5 V through the forward biased Diode. Since an electrical potential of +5 V is Logic ‘1’, we have the Logic ‘1’ as the output when **either or both** of the inputs ‘A’ and ‘B’ are at Logic ‘0’. This corresponds to the implementation of the first three rows of the Truth Table. Next, consider that Logic ‘1’ is applied to both the input terminals A & B. Since Logic ‘1’ is +5 V, we have a positive potential at the emitter of a NPN transistor, which represents a Reverse Bias. When Emitter of a transistor is reverse biased, it goes into Cut-Off. Therefore the collector potential of  $T_1$  is at  $+V_{CC}$ , i.e. +5 V. In other words, the base of  $T_2$  is at +5 V. This drives  $T_2$  into ‘Hard Saturation’. This drives the collector of  $T_2$  to 0 V. The emitter potential of a transistor always equals the potential at the base. Hence we have +5 V at the emitter of  $T_2$ . This results in the application of a potential of 0 V at the base of  $T_3$  and +5 V at the base of  $T_4$ . This condition will drive  $T_3$  into ‘Cut-Off’ and  $T_4$  into ‘Hard Saturation’. Since a transistor in Saturation is a Closed Switch and that in Cut-Off is an open switch, we have the output terminal **disconnected from  $+V_{CC}$  and short circuited to ground**. In other words, the logic at the output is Logic ‘0’. This corresponds to the implementation of the last row of the Truth Table.

**OPAMP (IC 741) :-** As the Electronic Industry evolved, a need was felt of a circuit to be able to compare a given voltage level with a

reference level. Another requirement was of a circuit to amplify the difference of two voltage signals. An urgent need was to isolate a faint signal from stronger Noises in the ambience. Later a need was felt for a system to be able to perform various Mathematical Operations. The answer to all of these requirements was the OPAMP (Operational Amplifier). The OPAMP evolved over time from being constructed with Vacuum Tube Devices to miniature transistorized circuits contained in a capsule, to the modern form of the IC. A typical general purpose OPAMP is the OPAMP IC 741. The internal circuit diagram and the IC Package is shown in the Fig.- 2(b) .

The OPAMP IC consists of a Difference Amplifier section consisting of Q<sub>1</sub> and Q<sub>2</sub>, with the input points being at the Pins 2 and 3 respectively. The output is taken from a Push-Pull section at Pin 6. The rest of the circuit consists of various Biasing and Feedback arrangements to improve the quality of the signal processing. A Difference Amplifier requires a Bipolar DC Power supply with +V<sub>CC</sub> and -V<sub>EE</sub>. A difference amplifier has a problem of Offset Condition. Hence two Pins, namely Pins 1 & 5 are provided to “Nullify the Offset”.



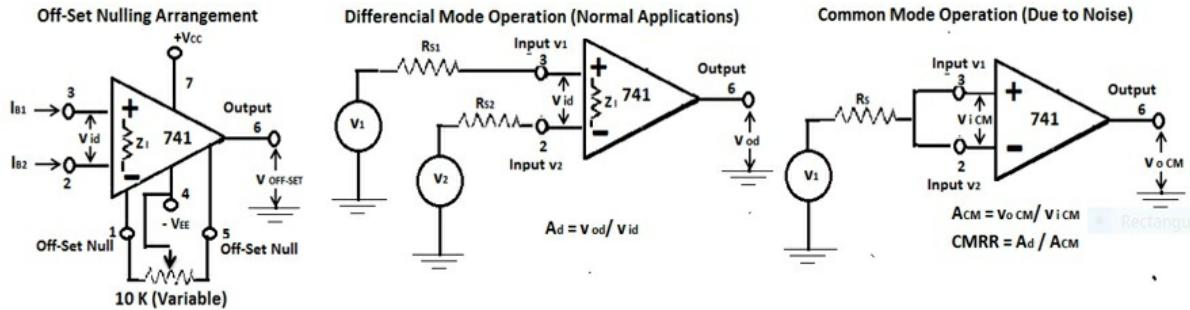
**Fig. 2 (b)**

**Using Block Diagram Representation of ICs :-** As described earlier, the circuit of the Digital NAND Gate, and the Analog OPAMP are rather quite complicated. The detailed working of the NAND Gate

circuit was explained and it was seen that the circuit performs a Basic Function of implementing a certain Logic Function described by a Truth Table. There are other such circuits for implementing other Logic Functions, such as NOT, AND, OR, NOR etc. A complex Digital Application is implemented by various combinations of these Logic Gates. Using a detailed Circuit Diagram with all these details of each Logic Gate is not practical. Thus the practice is to use Block Diagrams for each individual Logic Function. As we will explore in the subsequent sections, the OPAMP, being a versatile entity, also has widespread applications. Similarly, it is impractical to use the complete circuit diagram and instead use a Block Diagram. In fact, for any applications using ICs, the convention is to use the Block Diagram. The details of the functioning of the IC is “encapsulated” within the ‘Block’. The terminals for Input, Output and Biasing functions are shown outside. The Functional Block Diagram of the OPAMP is as shown in Fig. 3. The figure also shows two different modes of operation of the OPAMP, namely, Differential Mode and Common Mode.

### 10.3 Characteristics of Ideal OPAMP

During the process of evolution of the Electronic Industry, a need for a “Device” was felt, which could perform certain mathematical and logical operations. A set of desired characteristics of such a device was listed out and the development/improvisation of the device continued with reference to these desired characteristics. The present form of the OPAMP IC has been able to achieve most of these goals. The Ideal Characteristics of OPAMP are listed as follows, with brief explanation wherever necessary. Along with this, the numerical values of these quantities achieved in the most advanced OPAMP ICs is also given.



**Fig. 3: - (a) Block Diagram of OPAMP IC 741 with 'Offset-Nulling Circuit'  
(b) Differential Operation and (c) Common Mode Operation.**

1. **Infinite Voltage Gain** :- In practice, it is not possible to achieve this goal. Any OPAMP with a Voltage Gain of the order of  $10^5$  serves all practical purposes.
2. **Infinite Input Impedance** :- It is desired that the OPAMP should not draw any current in the input terminals. In practice, it is not possible to achieve this goal. BJT based OPAMP ICs show a value of Input Impedance of the order of Megaohms and those based on MOSFETS, this can be as high as Giga-ohms.
3. **Zero Output Impedance** :- It is desired that there should be no voltage drop in the output terminals. In practice, it is not possible to achieve this goal. Any OPAMP with Output Impedance of the order of a few tens of ohms (20 to 70  $\Omega$ ) serves all practical purposes.
4. **Infinite Bandwidth** :- It is desired that the OPAMP should be able to amplify DC as well as AC signals with a wide range of frequencies. However, in practice the Open Loop Bandwidth is about 15 KHz.
5. **Infinite Slew Rate** :- Slew Rate is defined as the rate at which the output voltage changes with respect to time, as soon as the desired input signal is applied. In practice Slew Rate of 10 V/ $\mu$ S is achievable.
6. **Zero Input Bias Current** :- Since the desired value of Input Impedance is infinity, it implies that the Input Bias Current should be zero. However OPAMPS made of BJT cannot have a zero current at the base terminal. Even in OPAMPS made of MOSFETS there appears some Input Bias Current. In case of BJT based

OPAMPS, the typical value of Input Bias Current is 100 nA, whereas in case of MOSFET based OPAMPs this is as low as 10 pA (1 picco Ampere is  $1 \times 10^{-12}$  A).

7. **Zero Offset Voltage** :- OPAMP has two Input terminals. It is desired that each of them be identical. In practice slight non-idealities exist, which means that the Input Bias Current at the two terminals is not equal. This results in a “Differential” input voltage due to difference in the voltage drop created by the Input Bias Current. Since the Voltage Gain of the OPAMP is so high, this results in an output voltage of around 10 mV, even in the absence of any external input signal. This is defined as the Offset Voltage.
8. **Infinite CMRR** :- Common Mode Rejection Ratio (CMRR) is defined as the ratio of Voltage Gain when the OPAMP is driven in the “Normal” Differential Input Mode, to the Voltage Gain when it is driven in the ‘Hidden’ Common Mode. The typically achievable value of CMRR is 120 dB. Higher the value of the CMRR of an OPAMP, better is its performance in presence of noise.

### **Significance of Off-Set Nulling**

The ‘Normal’ operation of the OPAMP is in Differential Mode. Two signals  $v_1$  and  $v_2$  are to be applied at the two input terminals, Pin-3 and Pin-2 respectively. Let there be no signals applied at “ $t = 0$ ”. Before any input is applied, the OPAMP needs to be biased (By application of  $+V_{CC}$  and  $-V_{EE}$ ). When the OPAMP gets the bias voltage, the Input Bias Current starts to flow. Assume that the Input Bias currents at two the Input Pins are slightly different. Let Input Bias current at Pin-3 be 100 nA and that at Pin-2 be 99.999 nA. Let the Input Impedance of the OPAMP be 100 KΩ. Since the directions of these two currents at the Input Impedance  $Z_I$  are opposite, there will appear a “Differential Input Voltage” of  $V_{id}$  even in the absence of any input signal.

$$V_{id} = (I_{B1} Z_I) - (I_{B2} Z_I)$$

$$V_{id} = (100 \times 10^{-9} \times 1 \times 10^5) - (99.999 \times 10^{-9} \times 1 \times 10^5)$$

$$V_{id} = 1 \times 10^{-7} V$$

Let the Open Loop Voltage Gain ( $A_D$ ) of the OPAMP be  $10^5$ . This

will give rise to an output voltage of

$$\begin{aligned} V_o &= A_D \cdot V_{id} = (1 \times 10^5 \times 1 \times 10^{-7}) \\ &= 0.01V = 10mV \end{aligned}$$

**The significance** of this statement is that, **even when** INPUT signal is zero, there still appears an OUTPUT voltage. This “Unwanted” voltage is called The Off-Set Voltage.

For the proper operation of the OPAMP, this Off-Set Voltage has to be nullified. The “Offset Nulling” circuit for the OPAMP IC 741 is shown in the Fig. 3 (a). The method is as follows.

**Method of Off-Set Nulling** :- A 10 K variable resistor (potentiometer) is connected between the Pin-1 and Pin-5 before connecting any input signal at either Pin-2 or Pin-3. The variable point is connected to the  $-V_{EE}$  point at Pin-4. The voltage at the output point Pin-6 is measured. Now, the variable point is adjusted, so that, the output reads 0 V in the absence of any actual input signal. The variable point is kept “Fixed” at this position for all subsequent operation of the OPAMP.

### Significance of High CMRR

In the previous section, it was stated that the “Normal” Mode of operation of the OPAMP is the Differential Mode. In the differential mode, two independent signal sources,  $v_1$  and  $v_2$  are connected to the two Input Pins, Pin-2 and Pin-3. The output is proportional to  $v_{id}$ , which is the “Difference” of the two input voltages. The Voltage Gain of the OPAMP in this case is denoted by  $A_D$ , given by –

$$A_D = \frac{V_o}{V_{id}} \quad \dots(1)$$

where  $V_{id} = v_1 - v_2$

$$\therefore V_o = A_D \cdot V_{id}$$

The numerical value of the quantity  $A_D$  is of the order of  $10^5$  or more for an OPAMP. Hence the output voltage is very high.

Now, if the two input points Pin-2 and Pin-3 are shorted and driven by a single signal source (Fig. 3.(c)), we call this as **Common Mode** operation. In this case we have

$$v_1 = v_2 \therefore v_{iCM} = 0$$

Since  $v_{idCM}$  is zero, the output voltage  $v_{oCM}$  should be zero. However, due to the non-idealities of the OPAMP IC, there will appear a certain amount of output voltage, i.e.

$$v_{oCM} \neq 0$$

Since  $v_{oCM}$  is non-zero, we can define a quantity to denote the Voltage Gain in Common Mode operation as  $A_{CM}$ , given by

$$A_{CM} = \frac{v_{oCM}}{v_{iCM}}$$

The output voltage in the Common Mode operation will be very low. Hence the quantity  $A_{CM}$  also will be very low.

Now, the point is that an OPAMP is **not meant** to operate in Common Mode operation. However, there are **real life** situations when an OPAMP gets driven in Common Mode. A **frequently occurring situation is unwanted signals, called “Noise”**, which are caused by spurious electromagnetic interference due to environmental causes. An electromagnetic interference induces an emf across a conductor, and as a result a current flows. If any such electromagnetic interference does occur, it will **produce equal signals** at the two input terminals of the OPAMP. In other words, the OPAMP will get driven in Common Mode.

A desirable **quality** of an OPAMP is measured by its ability to reject signals driven in Common Mode. This is defined by a ratio of the “Desirable” gain of Difference Mode operation to the “Undesirable” gain in the “Undesirable” Common Mode operation. This ratio is called “Common Mode Rejection Ratio” (**CMRR**), given by,

$$CMRR = \frac{A_D}{A_{CM}} \quad \dots (2)$$

Since the quantity  $A_{CM}$  is **very low**, and the quantity  $A_D$  is **very high**, the ratio CMRR tends to be extremely high.

Since CMRR is dimensionless, it is often expressed in dB as

$$CMRR_{dB} = 10 \log \left( \frac{A_D}{A_{CM}} \right) \quad \dots (3)$$

Typical value of CMRR for common OPAMPS is 100 dB. This means that the gain in the “Desirable” Difference Mode, viz,  $A_D$  is  $10^{10}$  times greater than the gain in the “Undesirable” Common Mode. In other words, it means that the strength of the “Undesirable” Noise

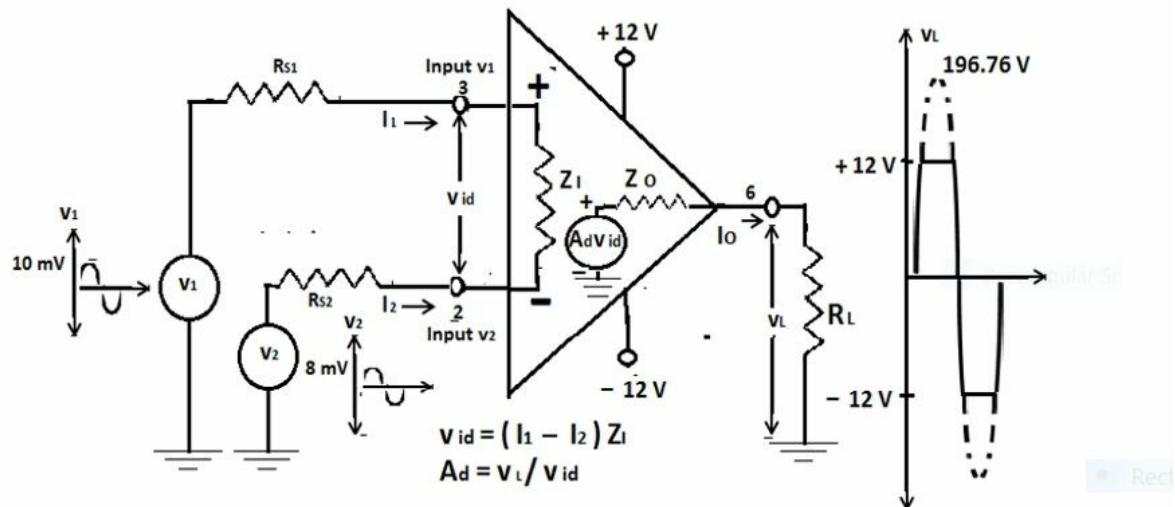
signals are  $10^{-10}$  times the strength of the Desirable Signal.

**Hence, “The higher the value of CMRR, the better is the quality of the OPAMP”.**

## 10.4 Open Loop and Closed Loop operation of OPAMPS

### Open Loop Operation

In the previous section we learnt that the “Normal” operation of the OPAMP is in Differential Mode. The circuit for the Differential mode is shown in Fig. 3 (b). This is shown again in the Fig. 4. below.



**Fig. 4:** - Equivalent circuit of OPAMP in Differential Mode. Input Difference Voltage is  $v_{id}$ . This is proportional to the ‘Difference’ of the two Input Signals  $v_1$  &  $v_2$ . Hence the output is also proportional to the Input Differential Voltage.

The OPAMP has two input terminals at Pin-2 and Pin-3. The figure shows the OPAMP being driven by two Input Signal Sources  $v_1$  and  $v_2$ , along with their Internal Resistances  $R_{s1}$  and  $R_{s2}$ , respectively. The

Input Impedance  $Z_i$  appears between these two input terminals. The output is depicted by a Thevenin's Equivalent, with a voltage source,  $A_d v_{id}$  and the Output impedance  $Z_o$  in series. The Thevenin Voltage Source is proportional to the Input Differential Voltage.

In the circuit, the input currents  $I_1$  and  $I_2$  flow in opposite directions through the Impedance  $Z_i$ . Thus, the voltage across  $Z_i$  is given by

$$v_{id} = (I_1 - I_2) \cdot Z_i$$

The currents,  $I_1$  and  $I_2$  are obtained by Superposition Theorem.

Assuming  $v_2 = 0$ , we have

$$I_1 = \frac{v_1}{(R_{s1} + R_{s2} + Z_i)}$$

Assuming  $v_1 = 0$ , we have

$$I_2 = \frac{v_2}{(R_{s1} + R_{s2} + Z_i)}$$

Substituting in the expression for  $v_{id}$  we have

$$v_{id} = \frac{(v_1 - v_2)}{(R_{s1} + R_{s2} + Z_i)} \cdot Z_i$$

In the equivalent circuit, the Output Current  $I_o$  will be given by

$$I_o = \frac{A_d v_{id}}{(Z_o + R_L)}$$

The voltage across the load will be

$$v_L = I_o \cdot R_L$$

Since  $I_o$  is proportional to  $v_{id}$  and  $v_{id}$  is proportional to the difference of the two input voltages, we have

$$v_L = \frac{A_d Z_i R_L}{(Z_o + R_L)(R_{s1} + R_{s2} + Z_i)} (v_1 - v_2) \quad \dots (4)$$

From Eq.(4), we observe that the output voltage given by an OPAMP is proportional to the "Difference" of the Input Voltages applied to the device. Hence an OPAMP is essentially a "Difference Amplifier".

However, there is a serious problem from the practical point of view. This can be brought to light with the help of a numerical problem, as follows.

**Example 1 :-** Consider an OPAMP IC 741. The numerical values of the quantities for this are,  $Z_i = 2 M\Omega$ ,  $Z_o = 70 \Omega$ ,  $A_d = 10^5$ .  $V_{CC} = +12 V$  and  $V_{EE} = -12 V$ . The OPAMP is driven by two voltage sources

$v_1 = 10 \text{ mV}$  and  $v_2 = 8 \text{ mV}$ . The Internal Resistance of the two signal sources are  $R_{s1} = 2 \text{ K}\Omega$  and  $R_{s2} = 3 \text{ K}\Omega$ . If the external load resistance connected to the circuit is  $5 \text{ K}\Omega$ , calculate the voltage across the load.

**Solution :-** Substituting the numerical values of the physical quantities in the formula for  $v_L$ , given by Eq. 4 we get.

$$v_L = \frac{1 \times 10^5 \times (10 \times 10^{-3} - 8 \times 10^{-3}) \times 2 \times 10^6 \times 5 \times 10^3}{(70 + 5 \times 10^3) \times (2 \times 10^3 + 3 \times 10^3 + 2 \times 10^6)}$$

$$= 196.75 \text{ V}$$

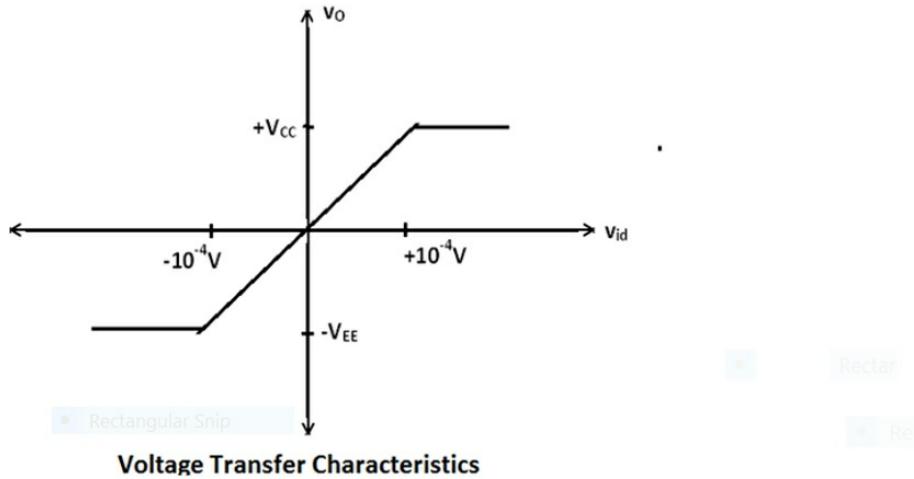
Assuming the input voltages were sinusoidal, with equal frequency, the output should have been a sinusoid of peak value 196.75 V.

**Here is the “Catch”.** The maximum voltage swing the OPAMP IC can have is from + 12V to – 12V **only**. Therefore the output voltage will be “Clipped” at these two values. In other words, the output will be seriously distorted. This means, that the amplitude of the Input Quantity, “ $v_{id}$ ” must be such that the “Peak” of the Output Voltage remains within the limits of  $+V_{CC}$  and  $-V_{EE}$ . The output voltage swing of OPAMPS in “Open Loop” configuration is determined by a graph called “Voltage Transfer Characteristic”, shown in Fig- 5.

**Voltage Transfer Characteristic :-** Fromm the Eq. 9.4, it is observed that, the output voltage of the OPAMP is proportional to the difference of the input signals

$$v_o \propto A_d(v_1 - v_2) \quad \text{or} \quad v_o \propto A_d v_{id}$$

The numerical value of  $A_d$  is of the order of  $10^5$  or more. Thus, in order for the output voltage to remain within the limits of  $+V_{CC}$  and  $-V_{EE}$ , the quantity  $v_{id}$  must be of the order of  $10^{-4}$  or less. When  $v_{id}$  exceeds this very small range, the output saturates at  $+V_{CC}$  or  $-V_{EE}$ . This is shown in the graph of Fig. 5.



**Fig. 5:** - *Voltage Transfer Characteristics of OPAMP at Open Loop configuration, showing the limited range of Input Voltage.*

From Fig. 5 , it is observed that “Working Range” of possible “Input Voltage Swing” is quite small. If this range is exceeded, the output voltage saturates at  $+V_{CC}$  or  $-V_{EE}$  as the case may be.

**Due to this reason, OPAMPS are seldom used in Open Loop.**

### **OPAMPS in Feedback Configurations (Closed-Loop Application of OPAMP)**

Recall the General Advantages of Negative Feedback....

1. **Voltage Gain is reduced, but it gets stabilized w.r.t. environmental variations.**
2. **Input Impedance is increased when a voltage in series is used as the feedback quantity.**
3. **Output Impedance is reduced when output current is drawn out to produce the feedback quantity.**
4. **Bandwidth is increased with all types of Negative Feedback.**
5. **Noise and Distortions are reduced with all types of Negative Feedback.**

**Therefore, Negative Feedback is a desirable feature in any amplifier.**

An OPAMP available in the market do not possess any of the “**Ideal Characteristics**” of OPAMPS, as listed earlier. However we shall see that some of these characteristics are implemented by the use of Negative Feedback.

In addition, the various arrangements of Feedback Elements in the various “Closed Loop Configurations” of the OPAMP results in various **operations** such as the following..

- a) As Non-Inverting Amplifier
- b) As Inverting Amplifier.
- c) As a Difference Amplifier (Analog Subtractor).
- d) As an Analog Adder.
- e) As Analog Multiplier and Analog Divider
- f) As Analog Integrator and Differentiator.
- g) As Comparator of two analog signals.
- h) Current to Voltage and Voltage to Frequency converters.
- i) As Active Filters of various configurations..

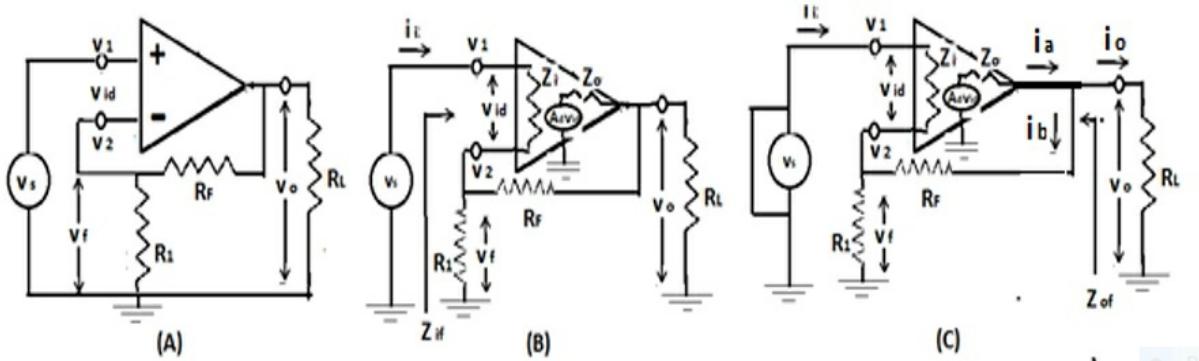
## **10.5 Non-Inverting Configuration**

### **(Voltage-Series Feedback Amplifier)**

An OPAMP Amplifier with Voltage-Series Negative Feedback arrangement is shown in the figure below.. **This results in a Non-Inverting Amplifier.**

#### **Refer to Part (A) for Voltage Gain**

In the Fig (A) the output voltage  $v_o$  appears across the series combination of  $R_F$  and  $R_1$  of the feedback path. The voltage developed across  $R_1$  is the “Feedback Voltage”  $v_f$ . This is in series with the Input Difference Voltage  $v_{id}$ . Hence we have Voltage-Series Negative Feedback.



**Fig. 6**

Overall Voltage Gain in the Feedback Configuration is

$$A_f = \frac{V_o}{V_s}$$

Gain of the Feedback Network is

$$B = \frac{V_f}{V_o} \quad \& \quad B = \frac{R_1}{(R_F + R_1)} \quad \dots (5)$$

For the OPAMP in the circuit we have

$$V_o = A_d V_{id} \quad \& \quad V_{id} = V_s - V_f$$

$$\therefore V_f = \frac{R_1 \cdot V_o}{(R_F + R_1)}$$

$$\therefore V_o = A_d \left( V_s - \frac{R_1 \cdot V_o}{(R_F + R_1)} \right)$$

$$V_o = A_d \left\{ \frac{(R_F + R_1)V_s - R_1 \cdot V_o}{(R_F + R_1)} \right\}$$

Or

$$(R_F + R_1 + A_d R_1) V_o = A_d (R_F + R_1) V_s$$

$$\therefore A_f = \frac{A_d (R_F + R_1)}{(R_F + R_1 + A_d R_1)} \quad \dots (6)$$

In this expression, the quantity Open Loop Gain of the OPAMP,  $A_d$  is of the order of  $10^5$ . Whereas, the resistances of the circuit will be of the order of a few Kilo ohms ( $10^3$ ). Thus in the Denominator, we can assume that,

$$(R_F + R_1) \ll A_d R_1$$

$$\therefore A_f \approx \left( \frac{R_F + R_1}{A_d R_1} \right) = \left( 1 + \frac{R_F}{R_1} \right) \quad \dots (7)$$

From the Eq.(7) we infer that the **Net Voltage Gain** of the OPAMP with Voltage Series Feedback is **Equal to the “Ratio” of resistances of the Feedback Network.**

From Eq. (5), we had the **Gain of the Feedback Network**. Comparing (5) and (6) we get that the **Net Voltage gain is the reciprocal of the Gain of the Feedback Network.**

$$A_f = \frac{1}{B} \quad \dots (8a)$$

Rearranging Eq.(6) we get

$$A_f = \frac{\frac{A_d(R_F + R_1)}{(R_F + R_1)}}{\frac{(R_F + R_1) + (A_d R_1)}{(R_F + R_1)}} = \frac{A_d}{1 + \frac{A_d R_1}{(R_F + R_1)}}$$

$$\therefore A_f = \frac{A_d}{1 + A_d B} \quad \dots (8b)$$

Equation (8b) is the General Form of the expression for Voltage Gain of a Voltage-Series Negative Feedback System.

Equations (7) & (8a) indicates that the **Net Voltage Gain** of the OPAMP with Voltage Series Feedback is **Equal to the “Ratio” of resistances of the Feedback Network and independent of the Open Loop gain of the OPAMP.**

Hence Voltage Gain is STABLE w.r.t. variations of temperature and other external factors.

**Relationship between the potentials at the two input terminals of the OPAMP**

In the figure, for the OPAMP

$$v_{id} = v_1 - v_2 = v_s - v_f$$

For the OPAMP

$$A_d = \frac{v_o}{v_{id}} \therefore v_{id} = \frac{v_o}{A_d}$$

For the OPAMP. The peak of the output voltage  $v_o$  can be only as much as  $\pm V_{CC}$ . On the other hand the magnitude of  $A_d \rightarrow \infty$

$$\therefore v_{id} \rightarrow 0 \quad \text{or} \quad v_1 \cong v_2$$

$$\text{OR } v_s \cong v_f$$

**This implies that the potentials at the two input terminals of the OPAMP are equal when Negative Feedback is applied.**

**NOTE :-** The expression for Net Voltage Gain, given by Eq.(7) is a function of the “Ratio of Resistances”. Since the “sign” of the expression is +ve, Output Voltage will also have a “+ve sign”. In other words, the phase of the Output voltage is the same as that of the Input voltage. HENCE THIS IS A “NON-INVERTING” AMPLIFIER.

### Refer to Fig (B) for Input Impedance

Figure (B) shows the internal equivalent circuit of the OPAMP.  $Z_I$  is the “Open Loop Input Impedance” of the OPAMP IC. When Voltage-Series Negative Feedback is applied, the **Net Input Impedance is given by**

$$Z_f = \frac{v_s}{i_i} = \frac{v_s}{\left(\frac{v_{id}}{Z_I}\right)} = \frac{Z_I \cdot v_s}{v_{id}}$$

$$\text{But } v_{id} = \frac{v_o}{A_d} \quad \& \quad v_o = \frac{A_d}{1+A_d B} v_s \quad \therefore v_{id} = \frac{v_s}{1+A_d B}$$

$$\text{Substituting } Z_f = \frac{Z_I \cdot v_s}{\left(\frac{v_s}{1+A_d B}\right)}$$

$$\text{Or } Z_f = Z_I (1 + A_d B) \quad \dots (9)$$

In an OPAMP, the Open Loop input impedance  $Z_I$  is of the order of  $10^6$  and Open Loop Voltage Gain  $A_d$  is of the order of  $10^5$ . Hence the Input Impedance becomes ENORMOUSLY HIGH when Voltage-

**Series Negative Feedback is applied.**

**Refer to Fig (C) for Output Impedance**

Output Impedance of an amplifier circuit is defined with the Source Short Circuited. For the Voltage-Series Negative Feedback System shown in Fig ( C ) we have the **Net Output Impedance** as

$$Z_f = \frac{v_o}{i_o} \mid_{v_s=0}$$

The Kirchhoff's Current Law at the output is

$$i_o = i_a + i_b$$

In an OPAMP. The Open Loop Output Impedance  $Z_o$  is less than  $100 \Omega$  whereas, the Open Loop Input impedance  $Z_I$  is of the order of  $10^6$ . The resistances of the Feedback Network are a magnitude of a few  $K\Omega$ . Hence we can assume that the net impedance of the path of the current  $i_b$  is very high compared to the Open Loop Impedance  $Z_o$ .

That is,  $(R_F + R_1 \parallel Z_I) \gg Z_o$

$$\therefore i_a \gg i_b \quad \text{OR} \quad i_o \approx i_a$$

From the circuit, in Fig. (C) we have

$$i_o = \frac{v_o - A_d v_{id}}{Z_o}$$

Where  $v_{id} = v_s - v_f$

But since the Source is Short Circuited, by definition  $v_s = 0$

$$\therefore v_{id} = -v_f$$

Earlier we had the expression for  $v_f$  and the Gain of the Feedback Network  $B$  as

$$v_f = \frac{R_1 \cdot v_o}{(R_F + R_1)} \quad \& \quad B = \frac{R_1}{(R_F + R_1)}$$

$$\therefore v_{id} = -B v_o$$

Substituting in the expression for  $i_o$  we have

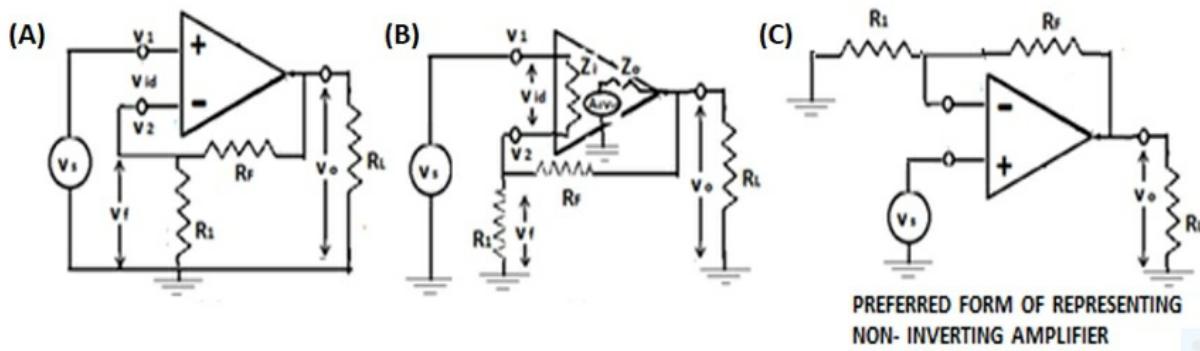
$$i_o = \frac{v_o(1 + A_d B)}{Z_o}$$

Earlier we had  $\frac{v_o}{i_o} = Z_f$

$$\therefore Z_f = \frac{Z_o}{(1 + A_d B)} \quad \dots (10)$$

Since in an OPAMP, the Open Loop output impedance  $Z_o$  is only a

few ohm, and Open Loop Voltage Gain  $A_d$  is of the order of  $10^5$ . Hence the Output Impedance becomes EXTREMELY LOW when Voltage-Series Negative Feedback is applied.



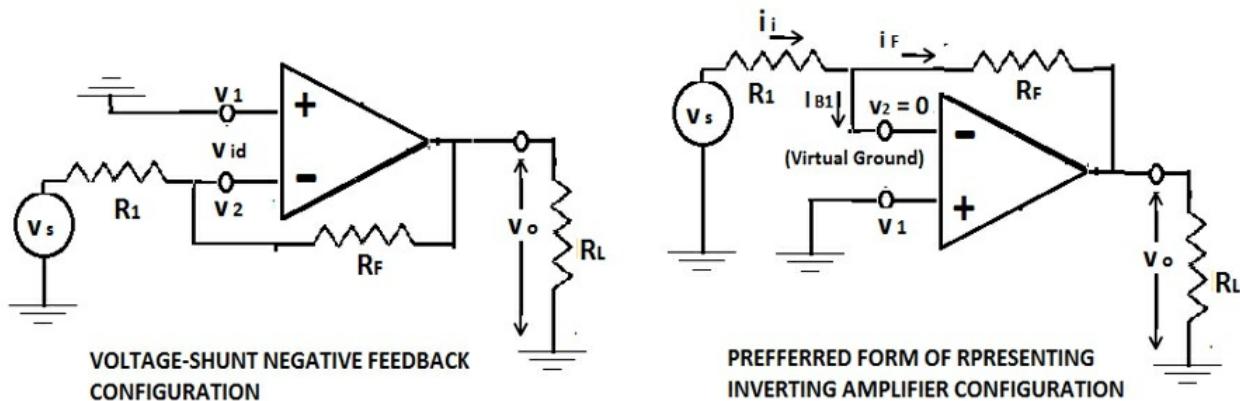
**Fig. 7**

**PREFERRED FORM OF REPRESENTING NON-INVERTING AMPLIFIER :-** The OPAMP amplifier with Voltage-Series Negative Feedback results in an amplifier whose output is in the same phase as the input. Hence this is a “Non-Inverting” configuration of OPAMP amplifier. This is a very useful configuration. The circuit shown in the form of the Fig. (C), above, is the most preferred form for representing the Non Inverting amplifier.

## 10.6 Inverting Configuration

(Voltage-Shunt Feedback Amplifier)

The other most useful configuration of OPAMP amplifier is the “**Inverting Configuration**”. For this purpose, the Negative Feedback arrangement is in Voltage-Shunt configuration. This is shown in the figure below.



**Fig. 8**

The Input Current gets “Shunted” into  $I_{B1}$  and  $i_F$ . However, the current in the Feedback Path,  $i_F$  is a function of the Output Voltage  $v_o$ . Thus we have Voltage-Shunt Feedback arrangement.

KCL at the Input Node gives

$$i_i = i_F + I_{B1}$$

Input Bias Current in an OPAMP is negligible,

$$\therefore I_{B1} \cong 0 \quad \therefore i_i = i_F$$

From the figure,

$$i_i = \frac{(v_s - v_2)}{R_1} \quad \& \quad i_F = \frac{(v_2 - v_o)}{R_F}$$

$$\text{Where } v_o = A_d (v_1 - v_2)$$

Since, the Non-Inverting terminal is connected to ground, we have

$$v_1 = 0 \quad \therefore v_o = -A_d v_2$$

$$\text{or } v_2 = \frac{-v_o}{A_d}$$

$$\text{We had } i_i = i_F$$

Substituting for  $v_2$  in the expressions for  $i_i$  &  $i_F$  above and equating , we have

$$\frac{(v_s + v_o/A_d)}{R_1} = -\frac{(v_o/A_d + v_o)}{R_F}$$

$$\therefore v_s + \frac{v_o}{A_d} = \frac{-v_o R_1 (1 + A_d)}{A_d R_F}$$

Rearranging,

$$v_s A_d R_F = -v_o (R_F + R_1 + A_d R_1)$$

From this, we get the Voltage Gain of the Voltage Shunt Negative Feedback amplifier as

$$A_f = \frac{v_o/v_s}{(R_F + R_1 + A_d R_1)} = \frac{-A_d R_F}{(R_F + R_1 + A_d R_1)}$$

As we had earlier, the Open-Loop Voltage Gain  $A_d$  of an OPAMP is of the order of  $10^5$ , while resistances in the circuit are in  $\text{K}\Omega$  range. Hence we may assume—

$$(R_F + R_1) \ll A_d R_1$$

Using this assumption in the above expression, we get the Voltage Gain of the Voltage Shunt Negative Feedback amplifier as

$$A_f = \frac{-R_F}{R_1} \quad \dots (11)$$

**Note :-** From the above expression, we see that the Voltage Gain in the Voltage-Shunt Negative Feedback configuration is simply the “Ratio” between the resistances in the Feedback Network. Also, that the Voltage Gain has a –ve sign. This means that the output voltage in a phase opposite to the Input voltage. THUS, THIS IS AN “INVERTING AMPLIFIER”.

**Concept of “Virtual Ground” :-** It was seen earlier, that, when a Negative feedback is applied to an OPAMP we have the condition that potential at the Inverting Terminal equals the potential at the Non-Inverting Terminal. Thus--

$$v_1 = v_2$$

In this “Inverting Configuration”, the Non-Inverting Terminal of the OPAMP is at Ground, thus

$$v_1 = 0 \quad \therefore v_2 = 0$$

Therefore, the Inverting Terminal is said to be at “Virtual Ground”.

**The concept of Virtual Ground is very useful in analyzing all of**

## the OPAMP applications in the Inverting Configuration.

Let us apply the **Virtual Ground** concept to the Voltage-Shunt configuration.

We started with the assumption that

$$i_i = i_F :$$

wherein

$$i_i = \frac{(v_s - v_2)}{R_1} \quad \& \quad i_F = \frac{(v_2 - v_o)}{R_F}$$

Using the **Virtual Ground** concept, we have

$$v_2 = 0$$

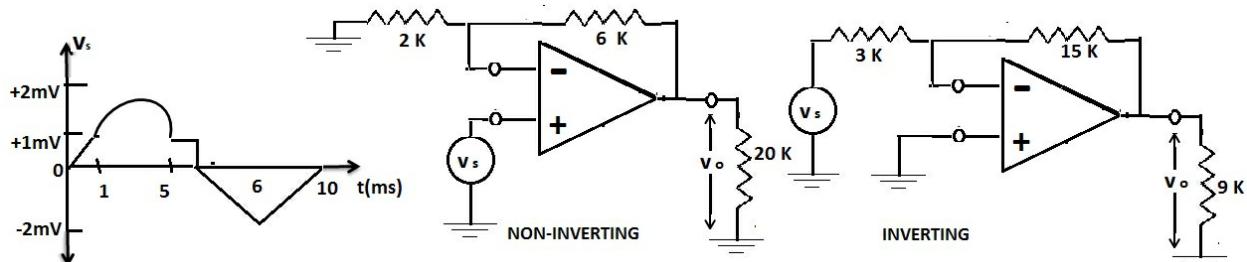
Equating  $i_i$  &  $i_F$  we have

$$\begin{aligned} \frac{(v_s)}{R_1} &= \frac{(-v_o)}{R_F} \\ \therefore A_f &= \frac{v_o}{v_s} = \frac{-R_F}{R_1} \end{aligned}$$

This is the same expression as Eq.(11) derived earlier.

**IN GENERAL, THE VOLTAGE GAIN, or THE RELATIONSHIP BETWEEN THE INPUT AND THE OUTPUT QUANTITY OF AN OPAMP IN ANY FEEDBACK ARRANGEMENT IS A FUNCTION OF THE “ENTITIES IN THE FEEDBACK PATH” AND INDEPENDENT OF THE “OPEN-LOOP GAIN” OF THE OPAMP IC.**

**Example 2 :-** Calculate the output voltage in the two circuits shown in the figure and sketch the output voltage.



**Solution :-**

**Non-Inverting Amplifier**

For the Non-Inverting amplifier, the expression for voltage gain is given by Eq.(7) as

$$A_f = \left(1 + \frac{R_F}{R_1}\right)$$

In the circuit,  $R_F = 6\text{ K}$  &  $R_1 = 2\text{ K}$

$$\text{Substituting } A_f = \left(1 + \frac{6}{2}\right) = 4$$

(Or  $A_f = +4$ )

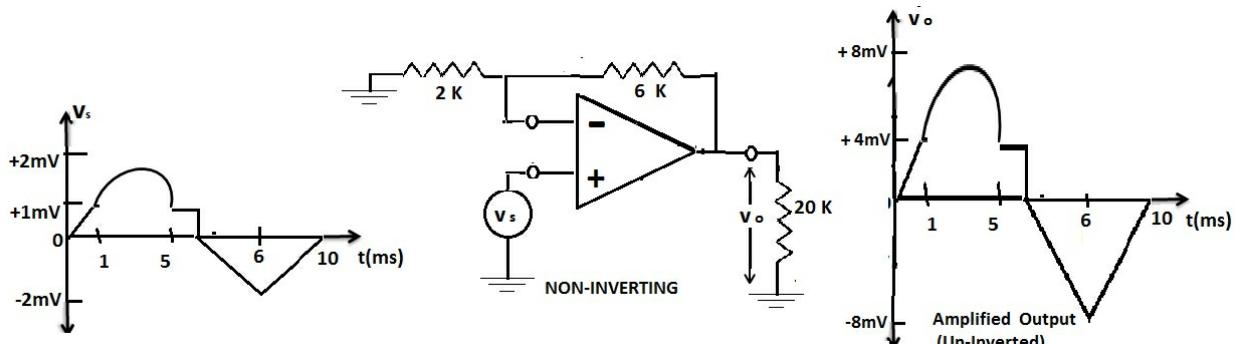
Output voltage is **4 times** the input voltage. Again, "sign" of  $A_f$  is +ve.

$\therefore$  (i) When  $v_s = +1\text{mV}$ ,  $v_o = (+4) \times 1 = +4\text{ mV}$

(ii) When  $v_s = +2\text{mV}$ ,  $v_o = (+4) \times 2 = +8\text{ mV}$

(iii) When  $v_s = -2\text{mV}$ ,  $v_o = (+4) \times (-2) = -8\text{ mV}$

From this calculation, the output voltage waveform can be drawn as follows.



### Inverting Amplifier

For the Inverting amplifier, the expression for voltage gain is given by Eq.(11) as

$$A_f = \left(-\frac{R_F}{R_1}\right)$$

In the circuit,  $R_F = 15\text{ K}$  &  $R_1 = 5\text{ K}$

Substituting

$$A_f = \left(-\frac{15}{5}\right) = -5$$

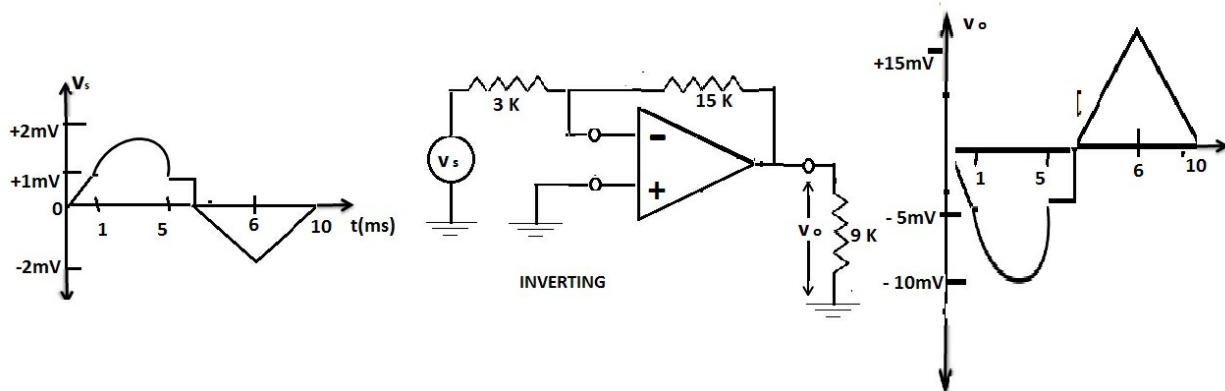
(Or  $A_f = -5$ )

Output voltage is **5 times** the input voltage And, "sign" of  $A_f$  is -ve.

$\therefore$  (i) When  $v_s = +1\text{mV}$ ,  $v_o = (-5) \times 1 = -5\text{ mV}$

- (ii) When  $v_s = +2\text{mV}$ ,  $v_o = (-5) \times 2 = -10 \text{ mV}$   
 (iii) When  $v_s = -2\text{mV}$ ,  $v_o = (-4) \times (-2) = +10 \text{ mV}$

From this calculation, the output voltage waveform can be drawn as follows.



## 10.7 Linear OPAMP Applications

### (1) ADDITION and SUBTRACTION

**1. Differential Amplifier (Analog Subtractor) :-** The circuit shown in the figure below has such feedback arrangements on the OPAMP that it is a combination of a Non-Inverting and Inverting configurations discussed above. This constitutes a Difference Amplifier. The output voltage is proportional to the “Difference” of the input voltages. In fact, the circuit can be said to be “**Performing the Arithmetic Operation of Subtraction**”.

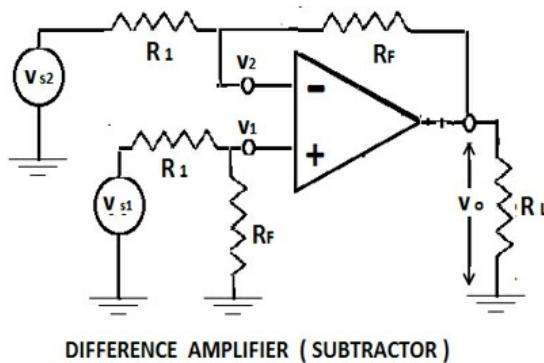


Fig. 9

**Analysis :-** Whenever any circuit has more than one source, the Superposition Principle is used for analysis.

Assuming the source “ $v_{s2}$ ” at ground, we have the Equivalent Circuit (A). This is a circuit in the configuration of a Non-Inverting amplifier. In this circuit, the potential at the Non-Inverting terminal, “ $v_1$ ” is given by Voltage Divider Rule as –

$$v_1 = \frac{v_{s1} \cdot R_F}{R_F + R_1}$$

For the Non-Inverting configuration, the Voltage Gain is given by Eq.(7) as

$$A_{f1} = \left(1 + \frac{R_F}{R_1}\right)$$

Let the Output Voltage in the Non-Inverting configuration (Due to Superposition Principle ) be denoted as “ $v_{o1}$ ”. This will be

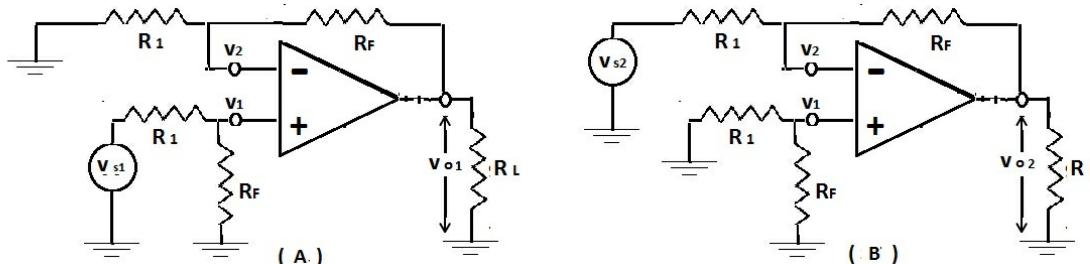
$$v_{o1} = A_{f1} \cdot v_1$$

Using these expressions from above, we have –

$$v_{o1} = \left(1 + \frac{R_F}{R_1}\right) \cdot \left(\frac{v_{s1} \cdot R_F}{R_F + R_1}\right)$$

$$\therefore v_{o1} = \left(\frac{(R_F + R_1)}{R_1}\right) \cdot \left(\frac{v_{s1} \cdot R_F}{(R_F + R_1)}\right)$$

$$\therefore v_{o1} = \frac{v_{s1} \cdot R_F}{R_1} = \frac{R_F}{R_1} v_{s1} \quad (a)$$



Assuming the source “ $v_{s1}$ ” at ground, we have the Equivalent Circuit (B). This is a circuit in the configuration of an Inverting amplifier. For the Inverting configuration, the Voltage Gain is given by Eq.(11) as

$$A_{f2} = \left( -\frac{R_F}{R_1} \right)$$

Let the Output Voltage in the Inverting configuration (Due to Superposition Principle ) be denoted as “ $v_{o2}$ ”. This will be

$$v_{o2} = A_{f2} \cdot v_{s2}$$

Using these expressions from above, we have –

$$v_{o2} = \left( -\frac{R_F}{R_1} \right) v_{s2} \quad (b)$$

**By Superposition**, the Final Output Voltage will be the “**Summation**” of expressions (a) and (b).

Thus we have

$$v_o = v_{o1} + v_{o2}$$

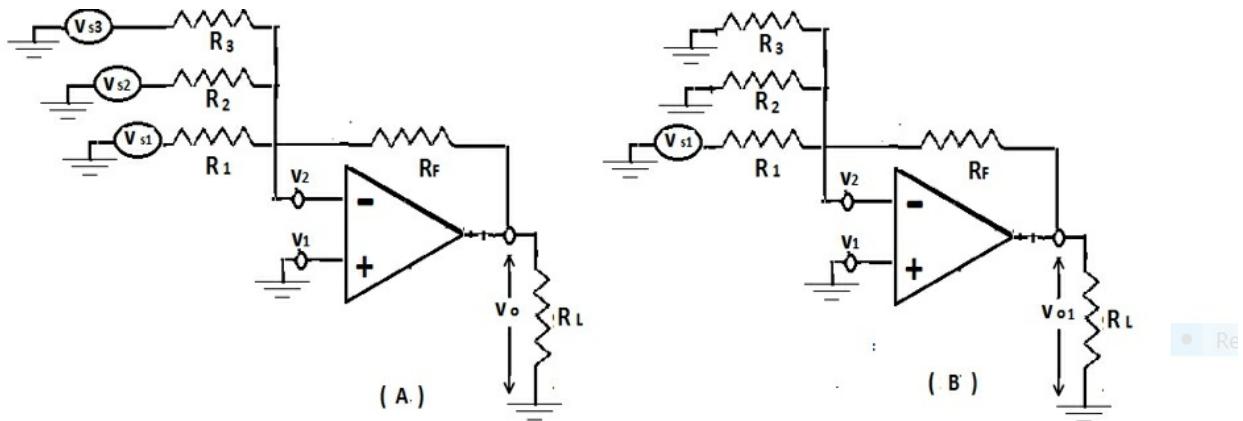
Using (a) & (b) we have

$$v_o = \left\{ \left( \frac{R_F}{R_1} \right) v_{s1} + \left( -\frac{R_F}{R_1} \right) v_{s2} \right\}$$

$$\therefore v_o = \left( \frac{R_F}{R_1} \right) [v_{s1} - v_{s2}] \quad \dots(12)$$

The Output Voltage of the circuit is **The Analog Difference** between the two input signals. Hence we have a “**Difference Amplifier**” or “**Analog Subtractor**”.

3. **Summing Amplifier (Analog Adder ) in Inverting Configuration** :- The circuit in the figure below is an “**Analog Adder**” in Inverting Configuration. In other words, it is a “**Summing Amplifier**”.



**Fig. 10**

Using Superposition Principle, assuming the sources “ $V_{s2}$ ” & “ $V_{s3}$ ” **at ground**, we have the Equivalent Circuit (B). This is a circuit in the configuration of an Inverting amplifier. For the Inverting configuration, the Voltage Gain is given by Eq.(11) as

$$A_{f1} = \left( -\frac{R_F}{R_1} \right)$$

Let the Output Voltage in the Inverting configuration (Due to Superposition Principle ) be denoted as “ $V_{o1}$ ”. This will be

$$V_{o1} = A_{f1} \cdot V_{s1}$$

Using these expressions from above, we have –

$$V_{o1} = \left( -\frac{R_F}{R_1} \right) V_{s1} \quad (a)$$

Next assuming the sources “ $V_{s1}$ ” & “ $V_{s3}$ ” **at ground**, we have a similar Equivalent Circuit. The source “ $V_{s2}$ ” is now connected to the amplifier through  $R_2$  . This results in the Output Voltage to be denoted by “ $V_{o2}$ ” as

$$v_{o2} = A_{f2} \cdot v_{s2}$$

Using these expressions from above, we have –

$$v_{o2} = \left( -\frac{R_F}{R_2} \right) v_{s2} \quad (b)$$

Similarly, assuming the sources “ $v_{s1}$ ” & “ $v_{s2}$ ” at ground, we have the Output Voltage to be denoted by “ $v_{o3}$ ” as.

$$v_{o3} = A_{f3} \cdot v_{s3}$$

$$v_{o3} = \left( -\frac{R_F}{R_3} \right) v_{s3} \quad (c)$$

Applying Superposition Principle, adding up the expressions (a) , (b) & (c), we have the Final Output Voltage as

$$v_o = \left[ \left( \left( -\frac{R_F}{R_1} \right) v_{s1} \right) + \left( \left( -\frac{R_F}{R_2} \right) v_{s2} \right) + \left( \left( -\frac{R_F}{R_3} \right) v_{s3} \right) \right]$$

If we assume that the three resistances at the input points of the three sources are equal, i.e. the three resistances are equal to some value  $R_i$ , we have,

$$\text{If } R_1 = R_2 = R_3 = R_I$$

$$\therefore v_o = \left( -\frac{R_F}{R_I} \right) \{v_{s1} + v_{s2} + v_{s3}\} \quad \dots(13)$$

The Eq. (13) shows that the circuit in the figure is a **Summing Amplifier OR Analog Adder, in Inverting Configuration.**

**This configuration is used for calculating the sum of any number of input signals.**

4. **Average Operation :-** The circuit given above can be configured to produce the “**Analog Average**” of any number of input signals. In the circuit above, if we use resistances such that

$$R_1 = 3 R_F ,$$

We will have the ratio

$$\left(-\frac{R_F}{R_I}\right) = \left(-\frac{1}{3}\right)$$

And the output as

$$v_o = \left(-\frac{1}{3}\right)\{v_{s1} + v_{s2} + v_{s3}\}$$

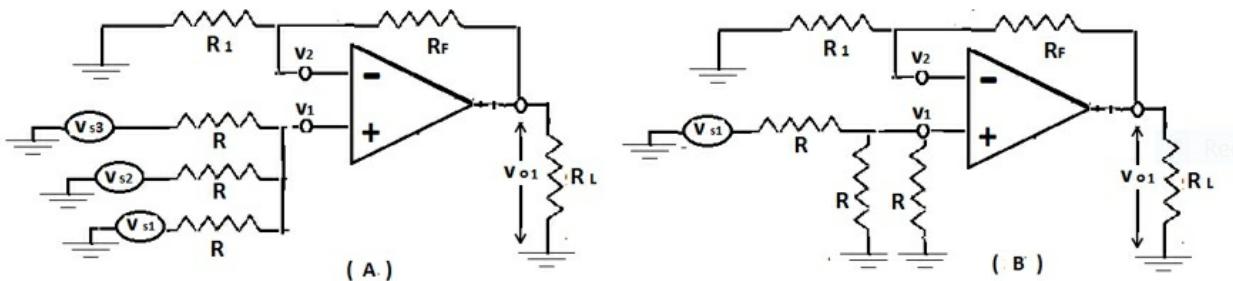
In general, for 'n' number of Input Signals, we should have

$$R_I = n R_F$$

So that the output is

$$v_o = \left(-\frac{1}{n}\right)\{v_{s1} + v_{s2} + v_{s3} \dots \dots + v_{sn}\} \quad \dots(14)$$

4. **Non-Inverting Adder :-** The circuit in the figure below will produce an output proportional to the "Analog Addition" of the input signals in Non-Inverting configuration. As usual, the circuit is analyzed using Superposition Principle.



**Fig. 11**

In order to use Superposition Principle, we "ground" two out of the three sources, " $v_{s2}$ " & " $v_{s3}$ " and use the equivalent circuit of Fig (B), where only a single source " $v_{s1}$ " is active. This is in the form of a Non-Inverting amplifier. Output voltage in Non-Inverting Configuration is given by

$$v_{o1} = A_f \cdot v_1$$

Where, " $v_1$ " is the potential at the Non-Inverting input terminal. In the circuit in Fig (B), when two of the sources are grounded, the resistances appear in parallel. The potential at the Non-Inverting terminal due to the source  $v_{s1}$  is obtained by voltage divider rule as the voltage developed across the parallel combination of these two resistances. The value of the parallel combination of two equal resistances is the half of each resistance. Applying Voltage Divider rule, we will have.

$$v_1 = \frac{(R/2)v_{s1}}{\{(R/2) + R\}} = \frac{\frac{v_{s1}R}{2}}{\frac{3R}{2}} = \frac{v_{s1}}{3}$$

For Non-Inverting amplifier, the Voltage Gain is given by Eq. (7).

Using this we get

$$v_{o1} = \left(1 + \frac{R_F}{R_1}\right) \cdot \frac{v_{s1}}{3} \quad (\text{a})$$

Similarly, using the other two sources in turn, we get

$$v_{o2} = \left(1 + \frac{R_F}{R_1}\right) \cdot \frac{v_{s2}}{3} \quad (\text{b})$$

$$v_{o3} = \left(1 + \frac{R_F}{R_1}\right) \cdot \frac{v_{s3}}{3} \quad (\text{c})$$

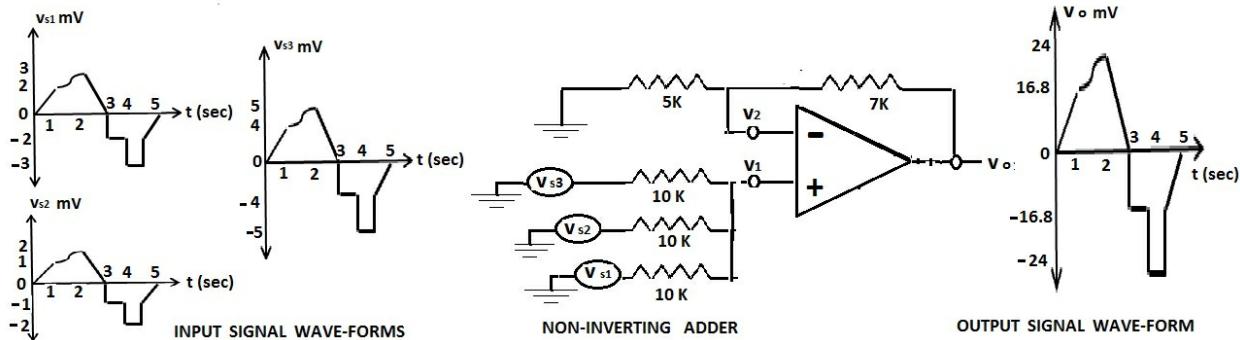
Now, using Superposition, by adding up the expressions (a), (b) and (c), we get the Final Output of the circuit as

$$v_o = \left(1 + \frac{R_F}{R_1}\right) \cdot [(v_{s1}) + (v_{s2}) + (v_{s3})] \quad \dots(15)$$

## **TUTORIAL**

**Example 1 :- (Non-Inverting Adder)** Calculate and sketch the output voltage of the circuits for the given input voltages.

(A)



**Solution (A) :-** The wave-forms of the three signals are of the same shape. Thus the output can be evaluated point-to-point, as follows.

Overall Voltage Gain of the circuit is

$$A_f = \left(1 + \frac{R_f}{R_1}\right) = \left(1 + \frac{7}{5}\right) = 2.4$$

Output voltage at every point is  $A_f$  times the sum of the input voltages at that point.

- a) At the point  $t = 1$ , the magnitudes of the three input signals are  
 $v_{s1} = 2 \text{ mV} : v_{s2} = 1 \text{ mV} : v_{s3} = 4 \text{ mV}$

$\therefore$  Output voltage at  $t = 1$  is

$$v_o = A_f (v_{s1} + v_{s2} + v_{s3}) = 2.4 (2 + 1 + 4) = 16.8 \text{ mV}$$

- b) At the point  $t = 2$ , the magnitudes of the three input signals are  
 $v_{s1} = 3 \text{ mV} : v_{s2} = 2 \text{ mV} : v_{s3} = 5 \text{ mV}$

$\therefore$  Output voltage at  $t = 2$  is

$$v_o = A_f (v_{s1} + v_{s2} + v_{s3}) = 2.4 (3 + 2 + 5) = 24 \text{ mV}$$

- c) At the point  $t = 3$ , the magnitudes of the three input signals are  
 $v_{s1} = -2 \text{ mV} : v_{s2} = -1 \text{ mV} : v_{s3} = -4 \text{ mV}$

$\therefore$  Output voltage at  $t = 3$  is

$$v_o = A_f (v_{s1} + v_{s2} + v_{s3}) = 2.4 \{(-2) + (-1) + (-4)\} = -16.8 \text{ mV}$$

- d) At the point  $t = 4$ , the magnitudes of the three input signals are  
 $v_{s1} = -3 \text{ mV} : v_{s2} = -2 \text{ mV} : v_{s3} = -5 \text{ mV}$

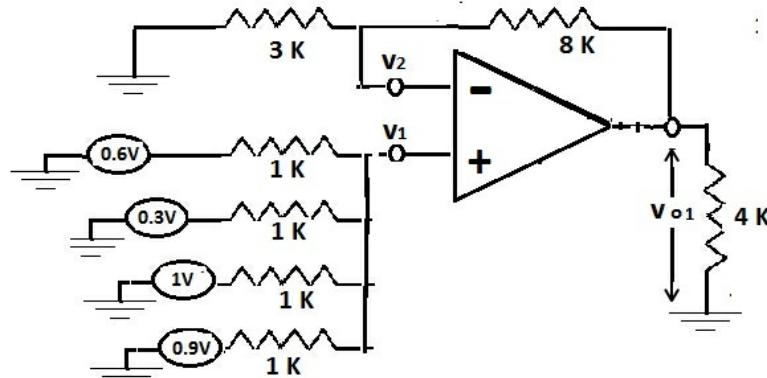
$\therefore$  Output voltage at  $t = 4$  is

$$\begin{aligned} v_o &= A_f (v_{s1} + v_{s2} + v_{s3}) = 2.4 \{(-3) + (-2) + (-5)\} \\ &= -24 \text{ mV} \end{aligned}$$

**From these calculations, the output voltage wave-form is**

sketched as shown in the figure above.

**(B)** In the circuit below, the input signal is represented by their r.m.s. values. Calculate the power developed across the external load.



**Solution (B) :-** The input voltages are represented by their r.m.s. values

Overall Voltage Gain of the circuit is

$$A_f = \left(1 + \frac{R_F}{R_1}\right) = \left(1 + \frac{8}{3}\right) = 3.67$$

∴ Output r.m.s. voltage is

$$v_o = A_f (v_{s1} + v_{s2} + v_{s3} + v_{s4}) = 3.67(0.6 + 0.3 + 1 + 0.9)$$

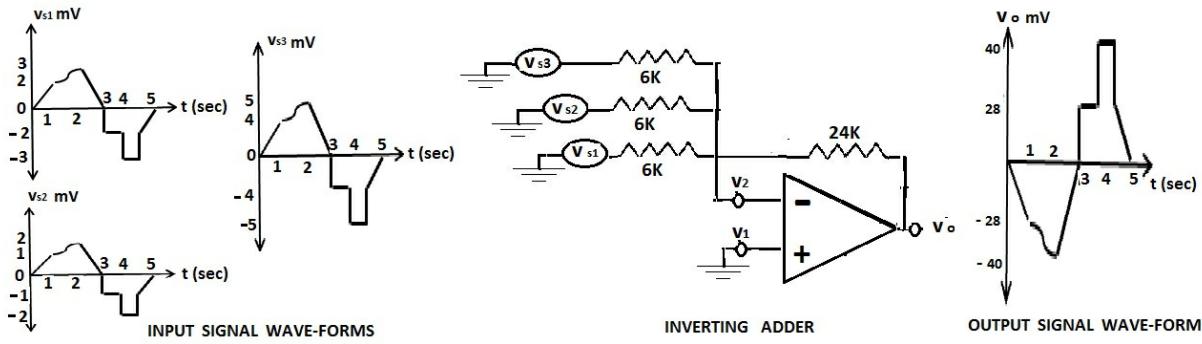
$$v_o = 10.276 \text{ V (r.m.s.)}$$

∴ Output Power across the load of  $R_L = 4 \text{ K}$  is

$$P_o = \frac{v_o^2}{R_L} = \frac{10.276^2}{4 \times 10^3} = 0.0264 \text{ W}$$

**Example 2 :- (Inverting Adder)** Calculate and sketch the output voltage of the circuits for the given input voltages.

**Solution (C) :-** The wave-forms of the three signals are of the same shape. Thus the output can be evaluated point-to-point, as follows.



Overall Voltage Gain of the circuit is

$$A_f = \left( -\frac{R_F}{R_1} \right) = \left( -\frac{24}{6} \right) = -4$$

Output voltage at every point is  $A_f$  times the sum of the input voltages at that point.

a) At the point  $t = 1$ , the magnitudes of the three input signals are

$$v_{s1} = 2 \text{ mV} : v_{s2} = 1 \text{ mV} : v_{s3} = 4 \text{ mV}$$

$\therefore$  Output voltage at  $t = 1$  is

$$v_o = A_f (v_{s1} + v_{s2} + v_{s3}) = (-4) \times (2 + 1 + 4) = -28 \text{ mV}$$

b) At the point  $t = 2$ , the magnitudes of the three input signals are

$$v_{s1} = 3 \text{ mV} : v_{s2} = 2 \text{ mV} : v_{s3} = 5 \text{ mV}$$

$\therefore$  Output voltage at  $t = 2$  is

$$v_o = A_f (v_{s1} + v_{s2} + v_{s3}) = (-4) \times (3 + 2 + 5) = -40 \text{ mV}$$

c) At the point  $t = 3$ , the magnitudes of the three input signals are

$$v_{s1} = -2 \text{ mV} : v_{s2} = -1 \text{ mV} : v_{s3} = -4 \text{ mV}$$

$\therefore$  Output voltage at  $t = 3$  is

$$\begin{aligned} v_o &= A_f (v_{s1} + v_{s2} + v_{s3}) = (-4) \times \{(-2) + (-1) + (-4)\} \\ &= +28 \text{ mV} \end{aligned}$$

d) At the point  $t = 4$ , the magnitudes of the three input signals are

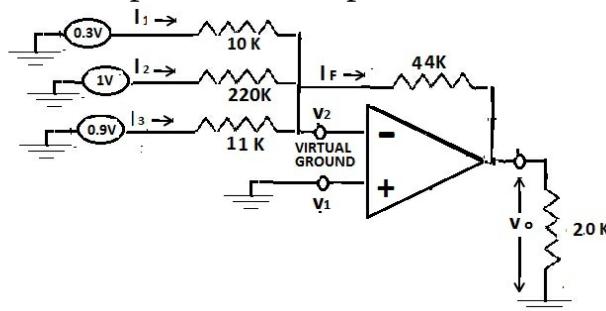
$$v_{s1} = -3 \text{ mV} : v_{s2} = -2 \text{ mV} : v_{s3} = -5 \text{ mV}$$

$\therefore$  Output voltage at  $t = 4$  is

$$\begin{aligned} v_o &= A_f (v_{s1} + v_{s2} + v_{s3}) = (-4) \times \{(-3) + (-2) + (-5)\} \\ &= +40 \text{ mV} \end{aligned}$$

**From these calculations, the output voltage wave-form is sketched as shown in the figure above.**

**(D)**In the circuit below, the input signal is represented by their r.m.s. values. Calculate the power developed across the external load.



**Solution (D) :-**

**(Solution using Virtual Ground Concept)**

The input voltages are represented by their r.m.s. values.

Due to KCL, the current equation at the “Node” of the Inverting Terminal is

$$I_F = I_1 + I_2 + I_3$$

Where,

$$I_F = \frac{(v_2 - v_o)}{R_F} : I_1 = \frac{(v_{s1} - v_2)}{R_1} : I_2 = \frac{(v_{s2} - v_2)}{R_2} : I_3 = \frac{(v_{s3} - v_2)}{R_3} :$$

In the Inverting Configuration, the “Inverting Terminal” is at “VIRTUAL GROUND” .

In other words, the potential at this terminal is

$$v_2 = 0$$

Substituting for  $v_2 = 0$  in the expressions above, we have--

$$I_F = \frac{(0 - v_o)}{R_F} = \frac{-v_o}{R_F}; \quad I_1 = \frac{(v_{s1} - 0)}{R_1} = \frac{v_{s1}}{R_1}; \quad I_2 = \frac{v_{s2}}{R_2}; \quad I_3 = \frac{v_{s3}}{R_3}$$

Substituting for these expressions for the currents in the KCL equation we have

$$\begin{aligned} \frac{v_{s1}}{R_1} + \frac{v_{s2}}{R_2} + \frac{v_{s3}}{R_3} &= \frac{-v_o}{R_F} \\ \therefore v_o &= -R_F \left[ \frac{v_{s1}}{R_1} + \frac{v_{s2}}{R_2} + \frac{v_{s3}}{R_3} \right] \end{aligned}$$

Substituting for numerical values of these from the circuit we have

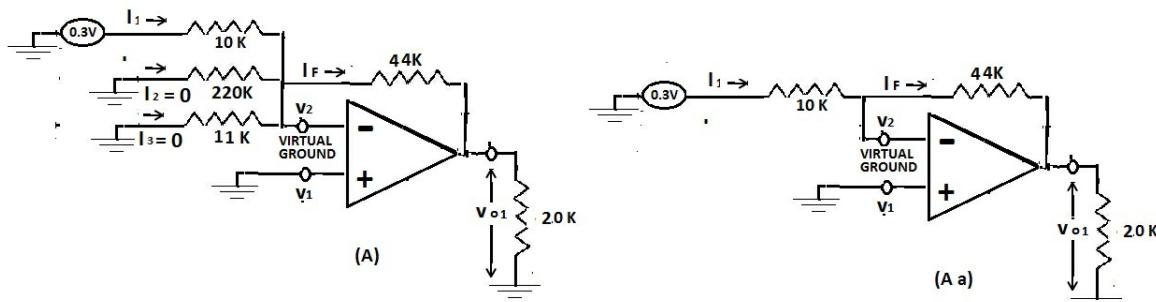
$$\begin{aligned} v_o &= 44 \times 10^3 \left[ \frac{0.3}{10 \times 10^3} + \frac{1}{220 \times 10^3} + \frac{0.9}{11 \times 10^3} \right] \\ v_o &= -5.12 \text{ V} \quad (\text{X}) \end{aligned}$$

$\therefore$  Output Power across the load of  $R_L = 4 \text{ K}$  is

$$P_o = \frac{v_o^2}{R_L} = \frac{5.12^2}{20 \times 10^3} = 0.000131 \text{ W}$$

### Solution Using Superposition Principle :---

- a) When the two sources “ $v_{s2}$ ” & “ $v_{s3}$ ” are grounded, we have the equivalent circuit (A). In this circuit, since the resistances  $R_2$  &  $R_3$  are connected between “Virtual Ground” and “Actual Ground”, the current flowing through them is 0. Hence these resistances may be neglected. Therefore, the equivalent circuit of (A) can be reduced to the form (A a).



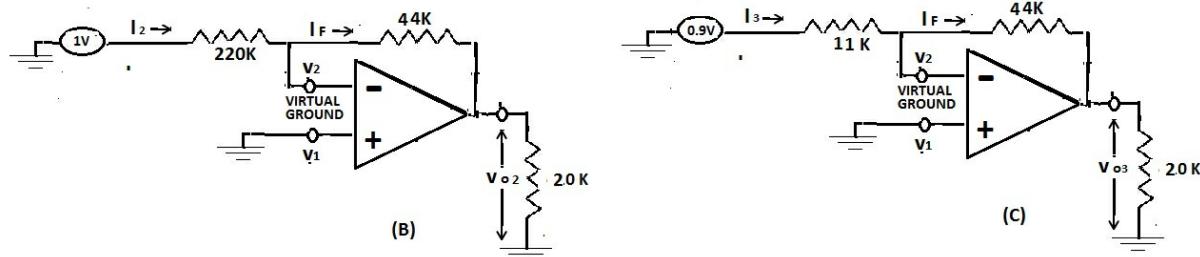
This is simply an Inverting Amplifier , with a Voltage Gain of “ $A_f$ ”, given by Eq.(11), as

$$A_{f1} = -\frac{R_F}{R_1} \quad \& \quad v_{o1} = A_f v_{s1}$$

Using the numerical values from the circuit (A a) we have,

$$\begin{aligned} A_{f1} &= -\frac{R_F}{R_1} = -\frac{44 \times 10^3}{10 \times 10^3} = -\frac{44 K}{10 K} = -\frac{44}{10} = -4.4 \\ v_{o1} &= -4.4 \times 0.3 = -1.32 \text{ V} \end{aligned}$$

- b) When the two sources “ $v_{s1}$ ” & “ $v_{s3}$ ” are grounded, the resistances  $R_1$  &  $R_3$  are connected between “Virtual Ground” and “Actual Ground”, the current flowing through them is 0. Hence these resistances may be neglected. Therefore, the equivalent circuit is (B).



In this, Voltage Gain of “ $A_f$ ”, given by

$$A_{f2} = - \frac{R_F}{R_2} \quad \& \quad v_{o2} = A_{f2} v_{s2}$$

Using the numerical values from the circuit (B) we have,

$$A_{f2} = - \frac{44 \times 10^3}{220 \times 10^3} = - \frac{44}{220} = -0.2$$

$$v_{o2} = -0.2 \times 1 = -0.2 \text{ V}$$

- c) When the two sources “ $v_{s1}$ ” & “ $v_{s2}$ ” are grounded, the resistances  $R_1$  &  $R_2$  are connected between “Virtual Ground” and “Actual Ground”. Therefore, the equivalent circuit is (C).

In this, Voltage Gain of “ $A_f$ ”, given by

$$A_{f3} = - \frac{R_F}{R_3} \quad \& \quad v_{o3} = A_{f3} v_{s3}$$

Using the numerical values from the circuit (B) we have,

$$A_{f3} = - \frac{44 \times 10^3}{11 \times 10^3} = - \frac{44}{11} = -4 \quad \& \quad v_{o3} = -4 \times 0.9 = -3.6 \text{ V}$$

**Now, by Superposition, the Final Output Voltage is**

$$v_o = v_{s1} + v_{s2} + v_{s3} = (-1.32) + (-0.2) + (-3.6)$$

$$v_o = -5.12 \text{ V} \quad (\text{Y})$$

**TO NOTE THAT, ANSWERS (X) & (Y) OBTAINED BY THE TWO METHODS IS JUST THE SAME .**

**Inverting Amplifier as an Amplitude Scaler :-** In general, the function of the amplifier is to increase the amplitudes of the input signal. Hence these can be considered as “Amplitude Scaler”. The “Scaling” of the amplitude is the “ratio” of the resistances “ $R_F$ ” & “ $R_I$ ”.

- a) If  $R_F > R_I$ , the output amplitude is greater than the input amplitude. This is the situation in (A) and (C) in the circuit above. The Output Voltage is greater than the Input voltage.
- b) If  $R_F < R_I$ , the output amplitude is lesser than the input amplitude. This is the situation in (B) in the circuit. The Output Voltage is lesser than the Input voltage.

**Example 2 “Scaler – Adder” :-** Inverting Adder with “Inequal Gain” for each input. (Inequal Scaling).

**Solution :-**

In view of the above, the three Inverting Configurations of the previous example can be represented as Fig. (X), (Y) & (Z), as follows. Following this same convention, the Inverting Adder, having “In-equal Gains” for the three input signals can also be represented as in the Fig. (W).

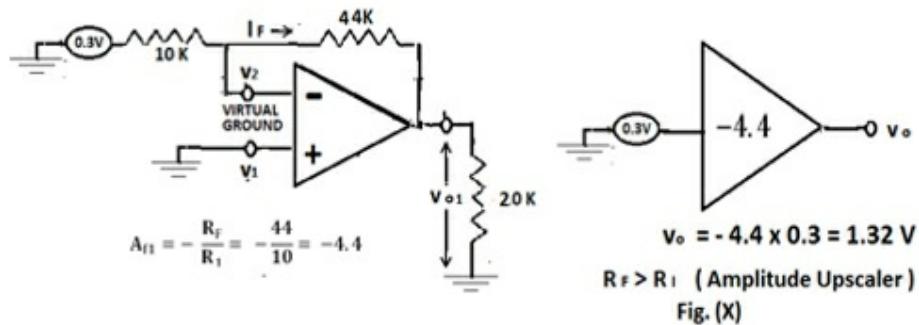


Fig. (X)

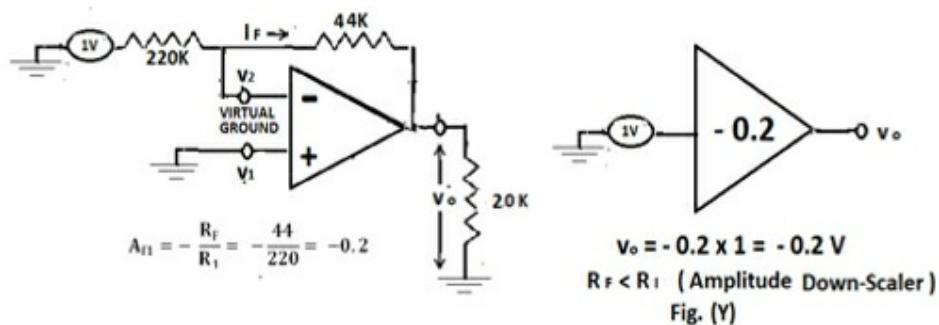


Fig. (Y)

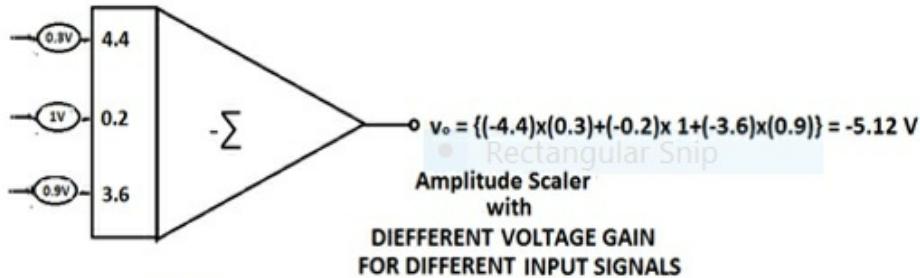
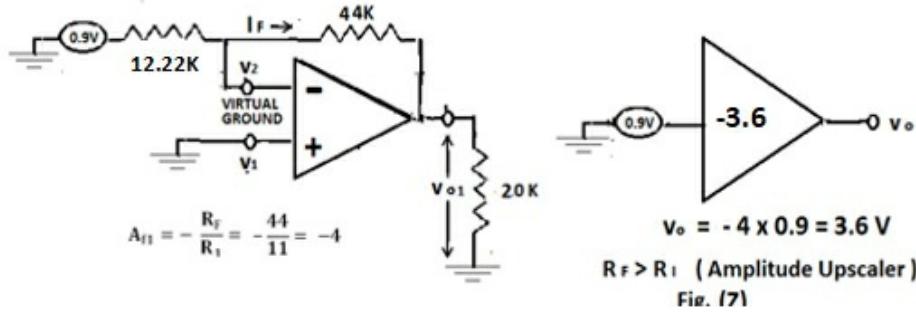


Fig. (W)

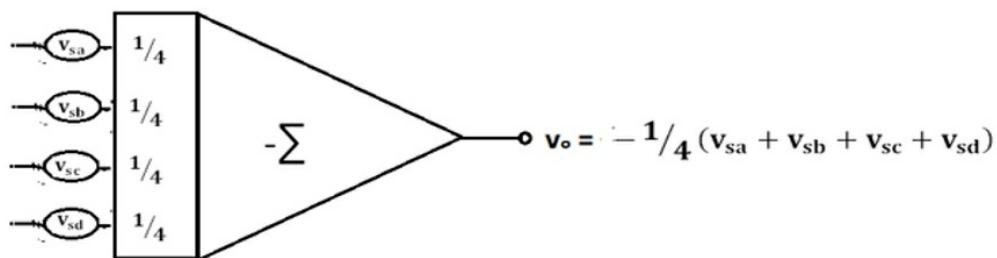
**Example 3 :- (Design Problem)** Design a circuit to calculate the average of four analog input signals.

**Solution :-**

The average of 4 signals “ $v_{sa}$ ”, “ $v_{sb}$ ”, “ $v_{sc}$ ” & “ $v_{sd}$ ” will be

$$v_{AV} = \frac{(v_{sa} + v_{sb} + v_{sc} + v_{sd})}{4} = \frac{1}{4} (v_{sa} + v_{sb} + v_{sc} + v_{sd})$$

This can be configured as A Scaler-Adder in the form of Fig.(W) as follows.



In terms of Circuit Diagram, this will be of the form as shown below. In this, the Voltage Gain must be ,

$$A_{f1} = -\frac{R_F}{R_I}$$

Therefore, the ratio of the resistance “ $R_F$ ”, in the Feed Back Path to each of the resistances “ $R_I$ ” in the Input Path must be

$$\frac{R_F}{R_I} = \frac{1}{4} \quad \therefore R_I = 4 R_F$$

Since “Only” ratio of the resistance matter, the NUMERICAL

VALUES of these resistances could be ANY VALUE.

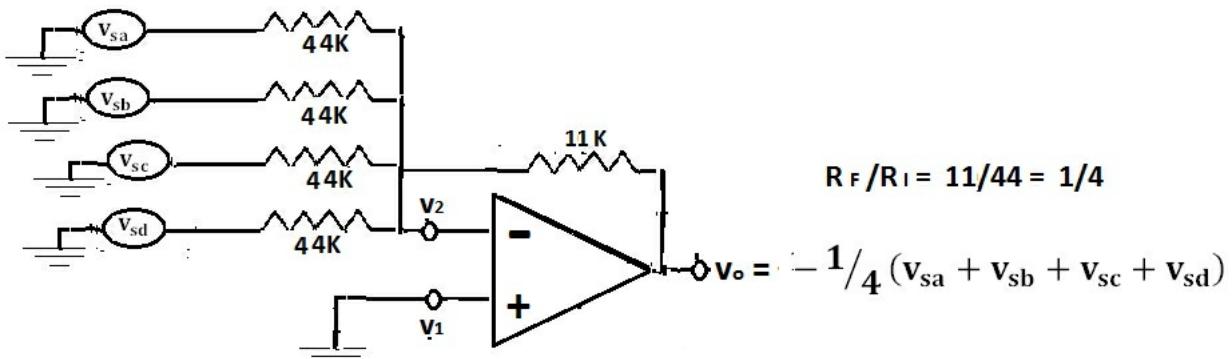
However, it is **TO BE NOTED** that, since the Input Resistance of the OPAMP is VERY HIGH (of the order of  $10^5 \Omega$ , or more), the resistance connected in the Input Path must be also HIGH so that the source **DOES NOT GET OVERLOADED**.

**HENCE, IT IS A NORM TO USE HIGH VALUE RESISTANCES IN THE FEEDBACK ARRANGEMENTS OF THE OPAMPS.**

Following this **Design Thumb Rule**, Let us chose

$$R_F = 11 \text{ K} \quad \therefore R_I = 4 \times 11 = 44 \text{ K}$$

From this, the **Circuit Design** for the “Averager” will be as follows....



**Example 4 :- (Design Problem)** Design a Two Input Summing Amplifier in Inverting Configuration to produce an output voltage of **6V** amplitude, given, the amplitudes of the two Input Signals are  $v_{s1} = 0.5 \text{ V}$  and  $v_{s2} = 0.7 \text{ V}$

**Solution :-** The “Sum” of the two Input Voltages is

$$v_{s1} + v_{s2} = 0.5 + 0.7 = 1.2 \text{ V}$$

The Magnitude of the Output Voltage is required to be **6 V** and the expression for the same is

$$| v_o | = | A_f | \cdot (v_{s1} + v_{s2}) = | A_f | \times 1.2 = 6 \text{ V}$$

$$\therefore | A_f | = \frac{v_o}{(v_{s1} + v_{s2})} = \frac{6}{1.2} = 5$$

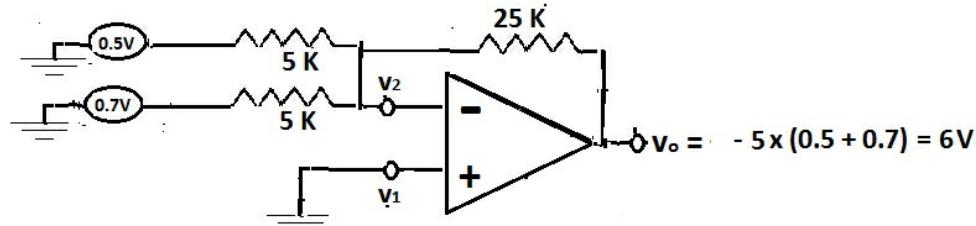
For the Inverting Adder , we have

$$| A_f | = \frac{R_F}{R_I} = 5 \quad \therefore R_F = 5 R_I$$

Following the **Design Thumb Rule**, let us choose

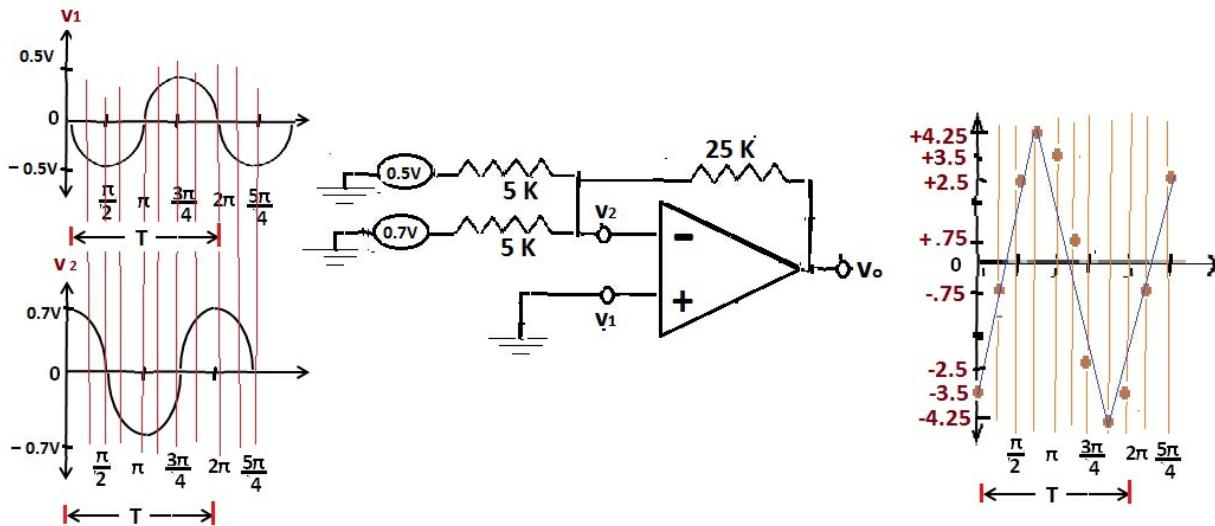
$$R_I = 5 \text{ K} \quad \therefore \quad R_F = 5 \times 5 = 25 \text{ K}$$

Using these resistances, the **circuit design** is as follows –



**Example 5 :-** If the input signals for the circuit in Example 4 are equal frequency sinusoids with different phase, as shown in the figure below, calculate and sketch the Output Voltage waveform and the r.m.s. value.

**Solution :-** The Inverting Configuration of the Amplifier in Example-4 has a gain of -5. At each instant of time, the output is the **Sum of the instantaneous values of the input multiplied by (-5)**. Some Sample Calculations at a few sample points within a half cycle are shown below. Using these the calculation for the complete waveform can be done.



- At  $t = 0$  sum of the instantaneous values of the input signals is  $(.7 + 0) = .7 \text{ V}$

Output at  $t = 0$  is  $(-5) \times 0.7 = -3.5 \text{ V}$ .

2. At  $t = \pi/4$  sum of the instantaneous values of the input signals is  
 $(.5 + (-.35)) = -.15 \text{ V}$

Output at  $t = \pi/4$  is  $(-5) \times (-.15) = -0.75 \text{ V}$ .

3. At  $t = \pi/2$  sum of the instantaneous values of the input signals is  
 $(0 + (-.5)) = -.5 \text{ V}$

Output at  $t = \pi/2$  is  $(-5) \times (-.5) = + 2.5 \text{ V}$ .

4. At  $t = 3\pi/2$  sum of the instantaneous values of the input signals is  
 $((-.35) + (-.5)) = -.85 \text{ V}$

Output at  $t = 3\pi/2$  is  $(-5) \times (-.85) = + 4.25 \text{ V}$ .

5. At  $t = \pi$  sum of the instantaneous values of the input signals is  
 $(0 + (-.7)) = -.7 \text{ V}$

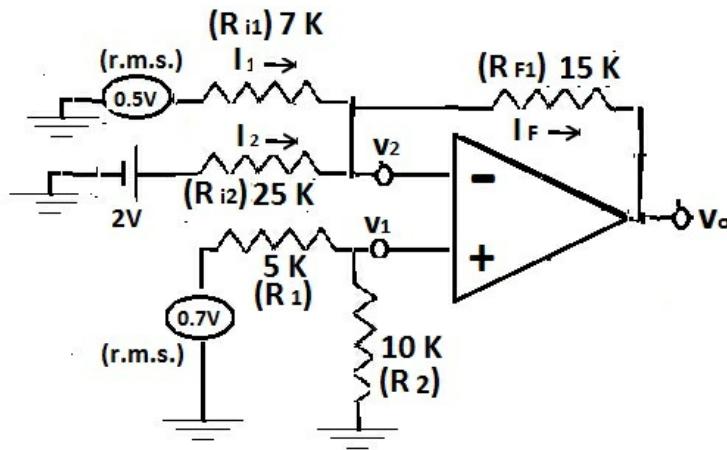
Output at  $t = \pi$  is  $(-5) \times (-.7) = + 3.5 \text{ V}$ .

**From these calculations, the Output Waveform can be sketched, as shown in the diagram.**

**Since the Waveform is a TRIANGULAR Waveform, r.m.s. value is**

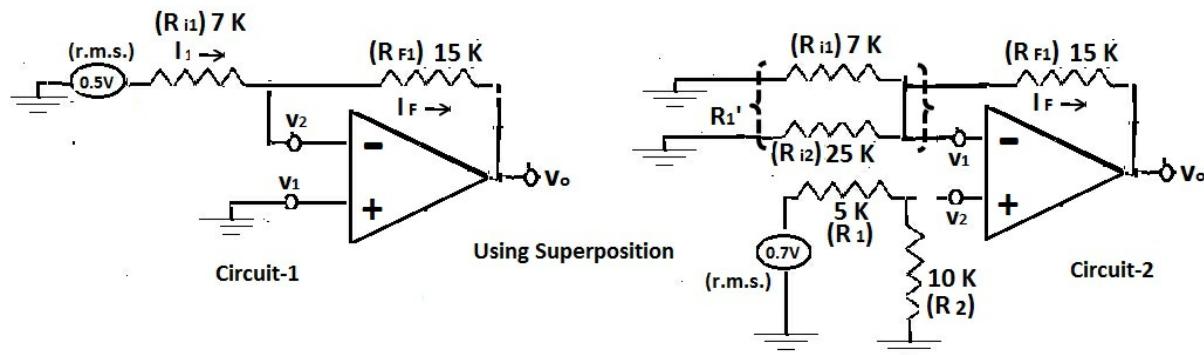
$$V_o(\text{rms}) = 1/\sqrt{3} V_{\text{MAX}} = 0.577 \times 4.25 = 2.45 \text{ V}$$

**Example – 6 (Combined Adder-Subtractor) :-** Calculate the output voltage for the circuit .



**Solution :-**

Using Superposition Principle, using each voltage source one at a time, we have –



- With **Only  $v_{s1}$  (Grounding  $v_{s2}$  &  $v_{s3}$ )**, we have the Circuit -1. This is an Inverting Amplifier.

$$\therefore v_{o1} = -\left(\frac{R_{F1}}{R_{i1}}\right)v_{s1} = -\frac{15}{7} \times 0.5$$

$$v_{o1} = 1.07 \text{ V(r.m.s.)} \quad (\text{a})$$

- ii. With **Only  $v_{s2}$  (Grounding  $v_1$  &  $v_{s3}$ )**, we have the circuit similar as Circuit -1, with the condition, ( $R_{i2} = 25 \text{ K}$ ).

$$\therefore v_{o2} = -\left(\frac{R_{F1}}{R_{i2}}\right)v_{s1} = -\frac{15}{25} \times 2$$

$$v_{o2} = 1.2 \text{ V (DC)} \quad (\text{b})$$

- iii. With **Only  $v_{s3}$  (Grounding  $v_{s1}$  &  $v_{s2}$ )**, we have the Circuit -2. This is Non-Inverting Amplifier. In this the potential  $v_1$  at the Non-Inverting terminal is given by the Voltage Divider Rule as

$$v_1 = \frac{R_2}{(R_1 + R_2)} \cdot v_{s3} = \frac{5}{(5+10)} \times 0.7 = 0.233 \text{ V}$$

In the Non-Inverting Configuration, the output will be

$$v_{o3} = \left(1 + \frac{R_{F1}}{R'_1}\right) v_1$$

$$R'_1 = \frac{R_{i1} \cdot R_{i2}}{(R_{i1} + R_{i2})} = \frac{7 \times 25}{(7+25)} = 5.5 \text{ K}$$

$$\therefore v_{o3} = \left(1 + \frac{15}{5.5}\right) \times 0.233 = 0.87 \text{ V(r.m.s.)} \quad (\text{c})$$

Note that, R.M.S. value of an AC is a constant, which can be added with a DC

Using Superposition Principle, the Final Output Voltage is

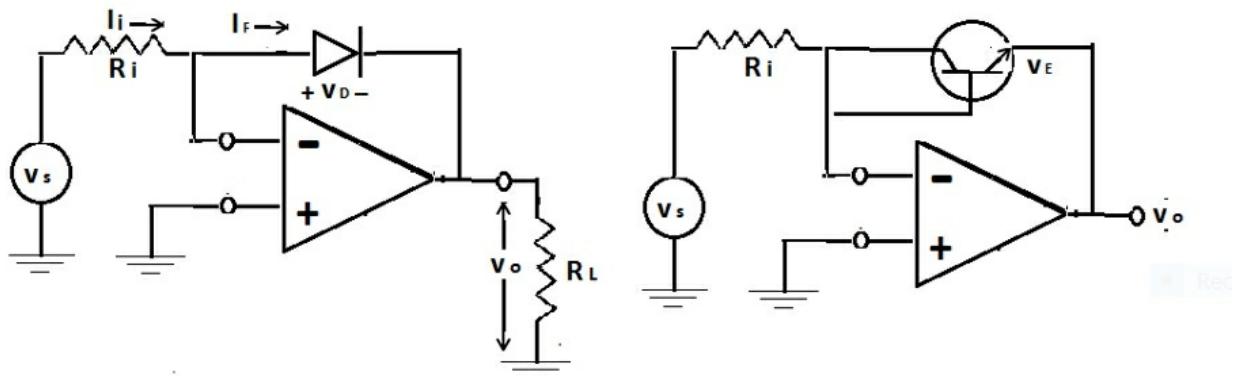
$$v_o = v_{o1} + v_{o2} + v_{o3} = 1.07 + 1.2 + 0.87 = 3.14 \text{ V}$$

## (2) MULTIPLICATION and DIVISION

The operations of Multiplication and Division cannot be performed directly by OPAMPS. However, the OPAMP can be configured as A Logarithmic Amplifier. Multiplication and Division operations are performed with these.

**(A) Logarithmic Amplifier :-** In the previous section we had seen that various operations could be performed by different configurations of the Feedback Arrangement the OPAMP circuit.

**If a P-N Junction is used in the Feedback Path, we have a Log Amplifier.**



**Fig. 12**

When the P-N Junction is fully forward biased the current is given by Shockley's Equation as

$$I_D = I_o \cdot e^{\left(\frac{q \cdot v_D}{kT}\right)}$$

Where

**$I_o$  = Reverse Saturation Current :**

**$q$  = Electron Charge :**

**$v_D$  = Voltage across diode :**

**$k$  = Boltzmann Constant**

**$T$  = Room Temperature in  $^0\text{K}$ .**

The current flowing into the OPAMP in a Negative Feedback Configuration is 0.

$$\therefore I_i = I_F \text{ & From the figure } I_F = I_D$$

For the Inverting OPAMP Configuration, the Inverting terminal is at "Virtual Ground" ( $v_2=0$ )

$$\therefore I_i = \frac{v_s}{R_i} = I_o \cdot e^{\left(\frac{q \cdot v_D}{kT}\right)}$$

$$\therefore v_s = R_i \cdot I_o \cdot e^{\left(\frac{q \cdot v_D}{kT}\right)}$$

Taking Natural Logarithm of this equation we have

$$\log_e(v_s) = \log_e(R_i \cdot I_o) - \frac{q \cdot v_D}{kT}$$

$$\log_e\left(\frac{v_s}{R_i \cdot I_o}\right) = -\frac{q \cdot v_D}{kT}$$

Since we have  $v_2 = 0$  due to Virtual Ground, the voltage across the diode is

$$v_D = v_2 - v_o = -v_o$$

Substituting this in the equation above we get

$$\log_e\left(\frac{v_s}{R_i \cdot I_o}\right) = -\frac{q \cdot (-v_D)}{kT} = \frac{q \cdot v_o}{kT}$$

$$\therefore v_o = \frac{kT}{q} \log_e\left(\frac{v_s}{R_i \cdot I_o}\right)$$

Changing the “Base” of logarithm to “10” we have

$$v_o = 2.3 \frac{kT}{q} \log_{10}\left(\frac{v_s}{R_i \cdot I_o}\right)$$

When we substitute Boltzmann constant  $k = 1.32 \times 10^{-23} \text{ J/K}$ ,  $q = 1.6 \times 10^{-19} \text{ C}$  and assume a room temperature of  $T = 300 \text{ K}$ , and solve the dimensional equation we get a quantity in the dimension of “Volt” as follows. When we use this numerical value we get the output voltage of the Log Amplifier as --

$$\frac{kT}{q} = 0.026 \text{ V}$$

$$v_o = 0.06 \log_{10}\left(\frac{v_s}{R_i \cdot I_o}\right) \quad \dots(15)$$

**Use of Transistor :-** The Reverse Saturation current of a Diode is highly sensitive w.r.t. temperature variations. Therefore, instead of a Diode, a transistor is used with the collector potential held at 0 V, by connecting the collector to Virtual Ground and short circuiting it to the base. This is as shown in the figure above. The expression for the output voltage remains the same, only with  $I_o$  replaced by  $I_{EO}$ .

**Example – 7 :-** If input signal is 10 mV, the resistance  $R_i = 10 \text{ K}$  and the Diode has a Reverse Saturation Current of 10 nA, Calculate the

output voltage magnitude.

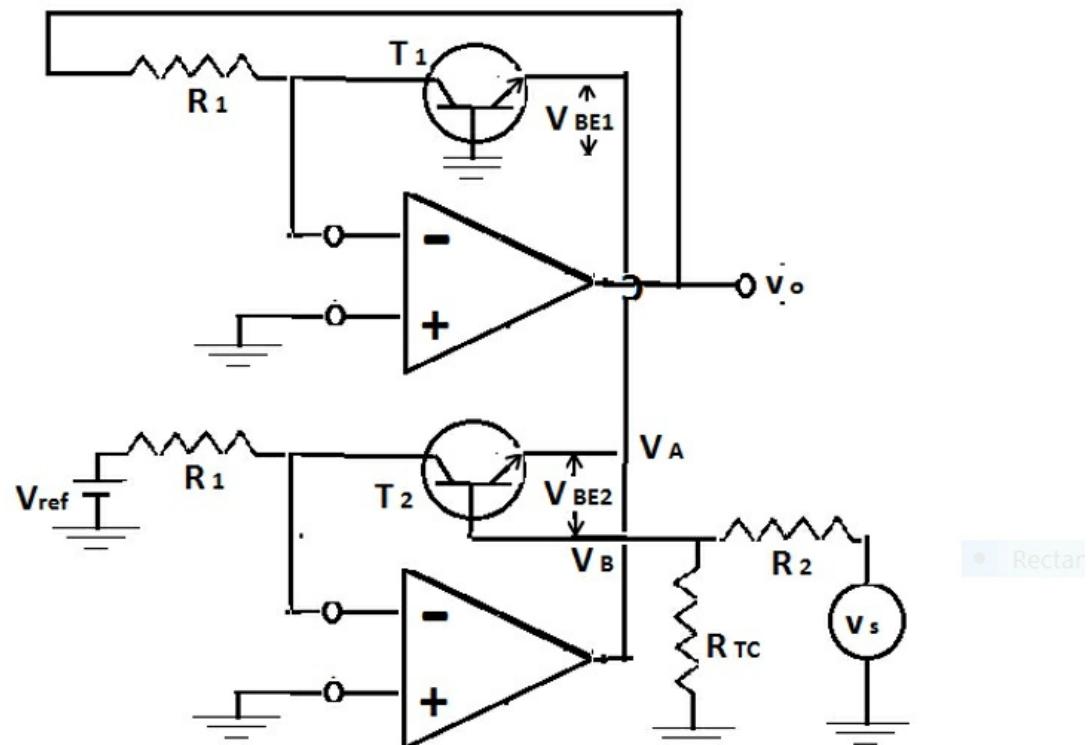
**Solution :-**

Substituting the given numerical values of the quantities in the Eq.(15) we have,

$$v_o = 0.06 \log_{10} \left( \frac{10 \times 10^{-3}}{10 \times 10^3 \times 10 \times 10^{-9}} \right) = 0.12 \text{ V}$$

$$v_o = 120 \text{ mV}$$

**(B) Anti-Log Amplifier :-** The circuit shown in the figure below produces an output proportional to the Anti-Log of the input voltage.



**Fig. 13**

In the circuit input to the first OPAMP is  $v_o$ . Therefore the potential at the other end of the Feedback path is

$$V_{BE1} = \frac{kT}{q} \log_e \left( \frac{v_o}{R_1 \cdot I_{EO}} \right)$$

Where  $I_{EO}$  is the Open Circuit Emitter Current

For the second OPAMP, the input voltage is a DC Reference Voltage  $V_{ref}$

$$V_{BE2} = \frac{kT}{q} \log_e \left( \frac{V_{ref}}{R_1 \cdot I_{EO}} \right)$$

The potential at the Point  $V_A$  is the potential between the Emitter and Base of the transistor  $T_1$

$$\therefore V_A = -V_{BE1} = -\frac{kT}{q} \log_e \left( \frac{v_o}{R_1 \cdot I_{EO}} \right) \quad \dots(X)$$

Base Voltage  $V_B$ , of the transistor  $T_2$  is obtained from the Signal Source  $v_s$ , through a Voltage Divider Network, given by the Voltage Divider Rule as

$$V_B = \left( \frac{R_{TC}}{(R_2 + R_{TC})} \right) \cdot v_s$$

Emitter voltage of  $T_2$  is  $V_{EB2} = V_B - V_{BE2}$

Using the expressions for  $V_B$  and  $V_{EB2}$ , where  $V_{EB2} = -V_{BE2}$ , we have

$$V_{EB2} = \left\{ \frac{R_{TC}}{(R_2 + R_{TC})} \right\} \cdot v_s - \frac{kT}{q} \log_e \left( \frac{V_{ref}}{R_1 \cdot I_{EO}} \right) \quad \dots(Y)$$

But the Emitter Potential of the transistor  $T_2$  shown as the potential  $V_A$ .

Therefore equating the expressions (X) and (Y), we have

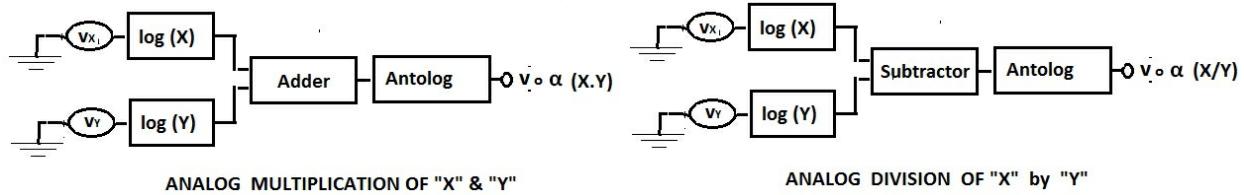
$$-\frac{kT}{q} \log_e \left( \frac{v_o}{R_1 \cdot I_{EO}} \right) = \left[ \left\{ \frac{R_{TC}}{(R_2 + R_{TC})} \right\} \cdot v_s - \frac{kT}{q} \log_e \left( \frac{V_{ref}}{R_1 \cdot I_{EO}} \right) \right]$$

Rearranging ,

$$\begin{aligned} \left\{ \frac{R_{TC}}{(R_2 + R_{TC})} \right\} \cdot v_s &= -\frac{kT}{q} \left[ \left\{ \log_e \left( \frac{v_o}{R_1 \cdot I_{EO}} \right) \right\} - \left\{ \frac{kT}{q} \log_e \left( \frac{V_{ref}}{R_1 \cdot I_{EO}} \right) \right\} \right] \\ \therefore \left\{ \frac{R_{TC}}{(R_2 + R_{TC})} \right\} \cdot v_s &= -\frac{kT}{q} \log_e \left( \frac{v_o}{V_{ref}} \right) \\ \therefore \log_e \left( \frac{v_o}{V_{ref}} \right) &= -\frac{q}{kT} \left\{ \frac{R_{TC}}{(R_2 + R_{TC})} \right\} \cdot v_s \\ \therefore \log_{10} \left( \frac{v_o}{V_{ref}} \right) &= -0.43 \frac{q}{kT} \left\{ \frac{R_{TC}}{(R_2 + R_{TC})} \right\} \cdot v_s \\ \therefore v_o &= V_{ref} \text{ Antilog} \left[ -0.43 \frac{q}{kT} \left\{ \frac{R_{TC}}{(R_2 + R_{TC})} \right\} \cdot v_s \right] \quad \dots(16) \end{aligned}$$

From Eq.(16), the Output Voltage is proportional to the Antilog of the Input. Using Log Amplifiers, Adders and Antilog Amplifier the process

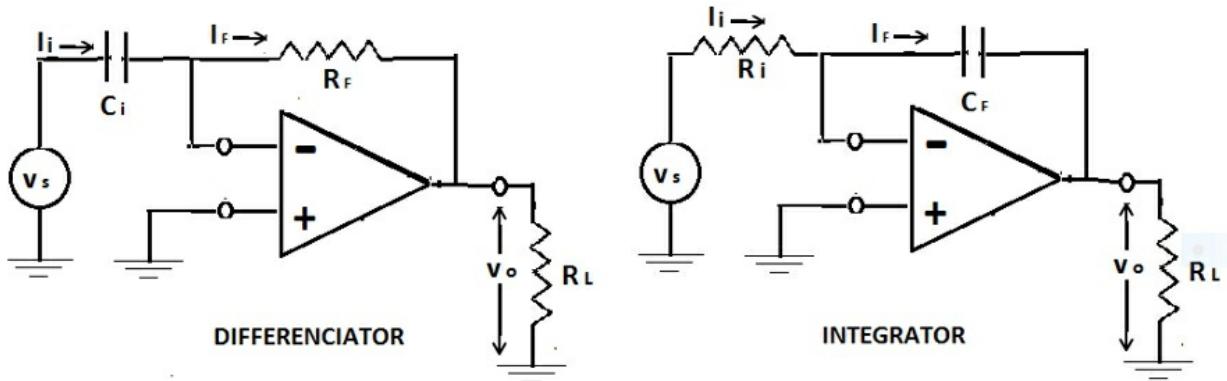
of Analog Multiplication is possible. Similarly, with a Subtractor stage, we can have Analog Division. The schematic is shown in the figure below.



**Fig. 14**

### (3) DIFFERENTIATION and INTEGRATION

It is also possible to perform Integration And Differentiation of Analog Voltage Signals. The circuits are in Inverting Configuration. When the Impedance Element in the Input Path is a Capacitor, we have a Differentiator. On the other hand, if the Impedance Element in the Feedback Path is a Capacitance, we have an Integrator.



**Fig. 15**

**Differentiator :-** In the OPAMPS with Negative Feedback the Input Current into the OPAMP is considered as 0.

$$\therefore I_i = I_F$$

Where

$$I_i = C_i \frac{d}{dt} (v_s - v_2) \quad \& \quad I_F = \frac{(v_2 - v_o)}{R_F}$$

In the Inverting Configuration the Inverting Terminal is at Virtual Ground

$$\therefore v_2 = 0$$

$$\therefore I_i = C_i \frac{d}{dt} (v_s) \quad \& \quad I_F = \frac{(-v_o)}{R_F}$$

$$\therefore v_o = -C_i R_F \frac{d v_s}{dt} \quad \dots(17)$$

From Eq(17) we infer that the Output Voltage is First Derivative of the Input Signal.

The process of Differentiation also interpreted as Calculation of the instantaneous slope of the Input Signal Waveform.

Since the circuit is in Inverted Configuration, the Calculated Slope will be with a Negative Polarity. In other words, if the instantaneous amplitude of the Input Signal is Positive, the output of the differentiator will be negative and vice-versa.

**Integrator :-** As we know, in the Inverting Configuration, we have

$$I_i = I_F \quad \& \quad v_2 = 0$$

$$\therefore I_i = \frac{(v_s)}{R_i} \quad \& \quad I_F = -C_F \frac{dv_o}{dt}$$

Equating  $I_i$  and  $I_F$  we have

$$\frac{v_s}{R_i} = -C_F \frac{dv_o}{dt} \quad \text{Or} \quad -\frac{1}{R_i C_F} v_s = \frac{dv_o}{dt}$$

Integrating both sides w.r.t. we have

$$v_o = -\frac{1}{R_i C_F} \int v_s dt + A \quad \dots(18)$$

Where “A” is the “initial Condition”. In practical terms, the Initial Condition is the potential across the capacitor plates due to the “Stored Charges” due to a previous action.

The process of INTEGRATION is also interpreted as Calculation of the instantaneous area under the curve of the Input Signal Waveform.

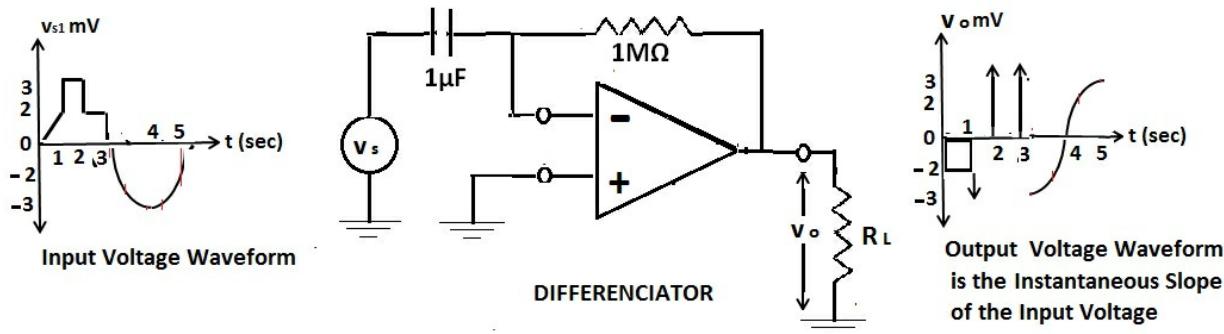
Since the circuit is in Inverted Configuration, the Calculated Area will be with a Negative Polarity. In other words, if the instantaneous amplitude of the Input Signal is Positive, the output of the integrator will

be negative and vice-versa.

## TUTORIAL

**Example 8 :-** In a Differentiator Circuit,  $C_i = 1 \mu F$  and  $R_F = 1 M\Omega$ . For the given Input Voltage, evaluate the Output Voltage Waveform.

**Solution :-** From Eq. (17) we get the output as the "Negative" of the First Derivative of the Input. Since First Derivative is Instantaneous Slope, and since the product  $- C_i \cdot R_F$  is the Net Gain of the Differentiator, we have the final output waveform as shown in the figure.  
 $- C_i \cdot R_F = 1 \times 10^{-6} \times 1 \times 10^6 = -1$



**Explanation for this solution :-** Before we proceed note two points

- The circuit is in Inverting Configuration. Which means, that the output voltage is going to be at the "Opposite" phase of that which is the function of the circuit is.
- The process of Differentiation, or the process of evaluating the First Derivative, is the process of calculating the Instantaneous Slope of the applied input signal waveform.

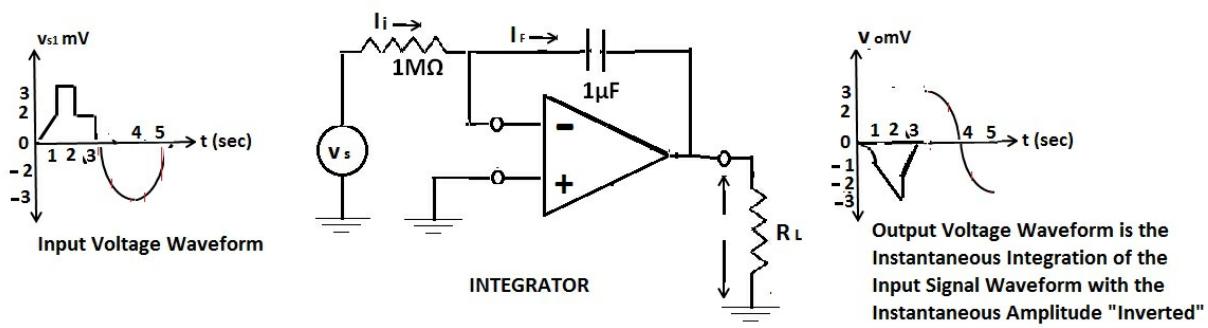
Using this we get the Output Voltage Waveform—

1. Between the time instant 0 to 1 the slope of the Input Signal is a constant at  $2 \text{ mV/sec}$ . Therefore the Output during this time interval is of magnitude  $2 \text{ mV}$ . Since the circuit is I Inverting Configuration, this  $2 \text{ mV}$  will have a negative amplitude.
2. At the instant 1 the input instantly becomes  $3 \text{ mV}$ . Therefore slope is 'Infinity'. Since we have an Inverting Configuration, the "Infinite Impulse" representing this event is in the negative

- direction.
3. In the time interval 1 to 2 the input voltage remains constant. Therefore it's slope is 'Zero'. Therefore, the output voltage is also 0.
  4. At the instant 2 the input instantly reduced to 2mV. Therefore slope is 'Infinity' in the decreasing direction. Since we have an Inverting Configuration, the "Infinite Impulse" representing this event is in the positive direction.
  5. In the time interval 2 to 3 the input voltage remains constant. Therefore it's slope is 'Zero'. Therefore, the output voltage is also 0.
  6. At the instant 3 the input instantly reduced to 0 . Therefore slope is 'Infinity' in the decreasing direction. Since we have an Inverting Configuration, the "Infinite Impulse" representing this event is in the positive direction.
  7. In between the interval 3 to 5 the input waveform is a "Sine" function of 3mV peak amplitude. The First Derivative of Sine is Cos. Since we have an Inverting Configuration, the output is a Cosine of "inverted amplitude" of 3mV.

**Example 9 :-** In a Integrator Circuit,  $C_F = 1 \mu\text{F}$  and  $R_i = 1 \text{ M}\Omega$  . For the given Input Voltage, evaluate the Output Voltage Waveform.

**Solution :-** From Eq. (18) we get the output as the" Negative" of the Integration of the Input. Since Integration is "Calculation of Instantaneous Area Enclosed" by the Input Voltage Waveform, and since the term  $(-1/ C_i \cdot R_F)$  is the Net Gain of the Differentiator, and this evaluates to (-1)) we have the final output waveform as shown in the figure.



**Explanation for this solution :-** Before we proceed note two points

- The circuit is in Inverting Configuration. Which means, that the output voltage is going to be at the “Opposite” phase of that which is the function of the circuit is?
- The process of Integration can also be interpreted as the process of evaluating the Instantaneous Area Enclosed by the input signal waveform.

Using this we get the Output Voltage Waveform—

1. In the interval 0 to 1 the Input function is  $v(t) = 2t$ . Therefore integration is  $2 \cdot (t^2/2) = t^2$ . Since we have an inverting Configuration, the output is a  $t^2$  function with Negative Amplitude of -1.
2. In the interval 1 to 2 the Input function is  $v(t) = 3$ . Therefore integration is  $3t$ . the output is the Negative of this,  $-3t$ .
3. At the instant  $t=2$  the Input signal drops to 2 and thereafter in the interval 2 to 3 the Input function is  $v(t)=2$ . Integration is  $2t$  and the output is  $-2t$ .
4. In the interval from 3 to 5 the Input function is a  $\sin(t)$  function. Therefore the integration is  $-\cos(t)$ . But due to Inverting Configuration, the output is the inversion of this.

## **10.8 NON-LINEAR APPLICATION OF OPAMPS**

In the context of Electrical Signals, Linearity refers to applications where the output of a system may be represented by a Linear Function of the Input or Inputs. In other words, a **Linear system obeys the Principle of Superposition**.

All the application of OPAMP, studied so far are Linear Systems.

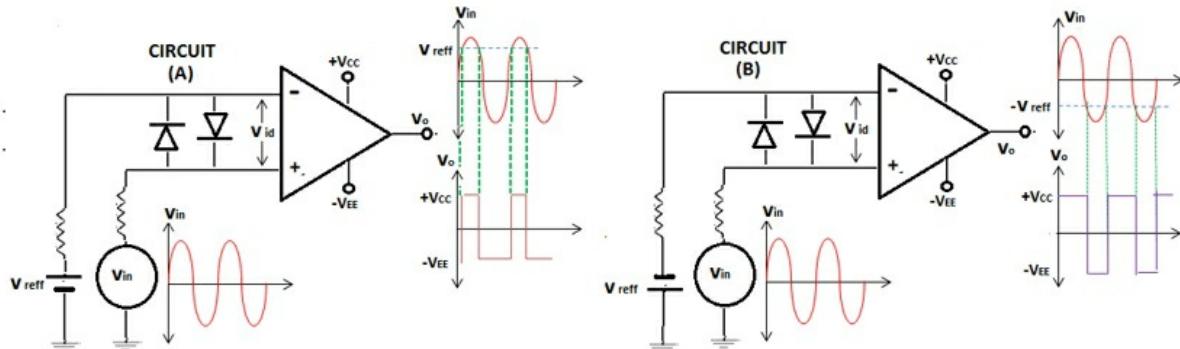
In Non-Linear applications of OPAMPS the output signal cannot be described as the function of the input signal(s).

### **(A) Comparator**

The purpose of a Comparator is to compare the instantaneous value of an Input signal with a Reference voltage and produce a Pulse as output to indicate whether the instantaneous value of the input signal is Greater or Lesser than the Reference value.

### **Positive Comparator (Non-Inverting Comparator)**

In the Circuit (A),  $V_{\text{ref}}$  is positive, and in the Circuit (B)  $V_{\text{ref}}$  is negative. Both the circuits are Positive Comparators. A Positive Comparator is one that produces a Positive Pulse whenever the instantaneous input signal amplitude is Greater than  $V_{\text{ref}}$ . The Diodes at the input terminals are for Over Voltage Protection.



**Fig. 16**

### **Principle of Operation :-**

The Input Difference Voltage  $v_{\text{id}}$  to the OPAMP is given by the expression-

$$v_{\text{id}} = (v_{\text{in}} - V_{\text{ref}})$$

### **Circuit (A)**

A sinusoidal input is shown, but the input signal can be of any waveform. The reference voltage  $V_{\text{ref}}$  is a positive DC. As long as the instantaneous value of the input signal is less than  $V_{\text{ref}}$ , the Input Difference Voltage  $v_{\text{id}}$  to the OPAMP is negative. Since the OPAMP is in Open-Loop Configuration, any input voltage greater than a small fraction of a microvolt will drive it into saturation. Since  $v_{\text{id}}$  is negative as long as instantaneous  $v_{\text{in}}$  remains less than  $V_{\text{ref}}$ , the output will be saturated at

$$-V_{\text{EE}}$$

As soon as instantaneous amplitude of  $v_{\text{in}}$  crosses the limit  $V_{\text{ref}}$ ,

the Input Difference Voltage  $v_{id}$  becomes positive. Thus as soon as  $v_{in}$  is a few fraction of a microvolt greater than the limiting value  $V_{ref}$  the output of the OPAMP will be driven to the Positive Saturation  $+V_{CC}$ . This sequence will repeat in every cycle.

Thus, in this circuit, as soon as the input signal amplitude crosses the limiting value  $V_{ref}$  we get a positive pulse and as soon as input signal amplitude is less than the limiting value  $V_{ref}$ , we get a negative pulse.

### Circuit (B)

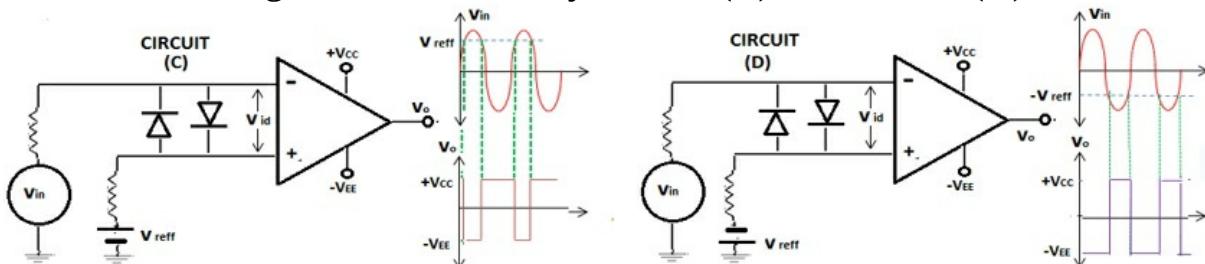
The reference voltage  $V_{ref}$  is a negative DC. In this case

$$v_{id} = \{v_{in} - (-V_{ref})\} = \{v_{in} + V_{ref}\}$$

Therefore, as long as the amplitude of  $v_{in}$  is Positive or “Less Negative” than  $V_{ref}$ , the Input Difference Voltage  $v_{id}$  is positive. Therefore the output is saturated at  $+V_{CC}$ . As soon as the amplitude of  $v_{in}$  becomes “More Negative” than  $V_{ref}$ ,  $v_{id}$  becomes negative. Thus the output of the OPAMP goes to negative saturation  $-V_{EE}$ .

### Negative Comparator (Inverting Comparator)

A Negative Comparator is one that produces a Negative Pulse whenever the instantaneous input signal amplitude is Greater than  $V_{ref}$ . A negative comparator will have the input signal at the Inverting terminal and  $V_{ref}$  at the Non-Inverting terminal. The Inverting Comparator also has two configurations, shown by Circuit (C) and Circuit (D).



**Fig. 17**

### (B) Zero Crossing Detector

A zero-crossing detector is used to generate a pulse whenever an AC voltage phase angle becomes 0, 180, and 360 degrees within each successive cycle.

At these points in the wave, the amplitude equals 0 V. This can be used for generating a timing signal, which is most often used to control an

AC switch. By turning the switch on or off when the voltage is 0 there is less stress on the switching device and less distortion of the output signal.

A zero-crossing detector is simply a Positive Comparator in which the reference voltage is zero. Therefore, a narrow positive pulse will be generated at the points of the Input Waveform when the amplitude becomes 0.

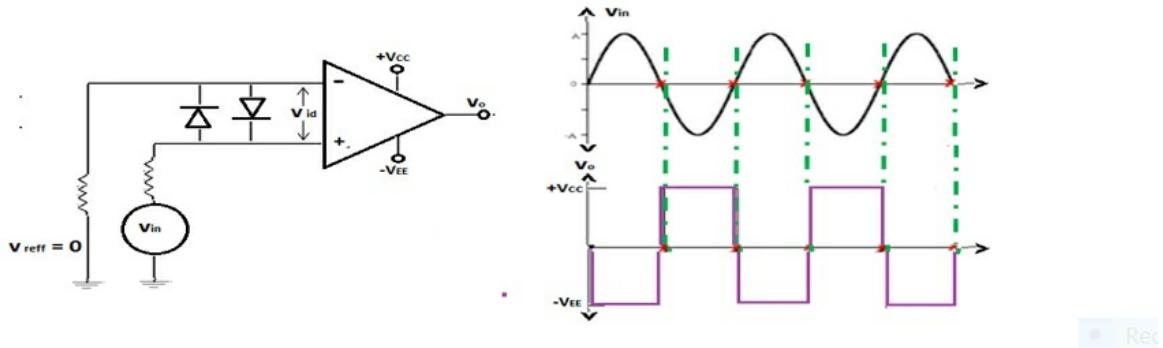


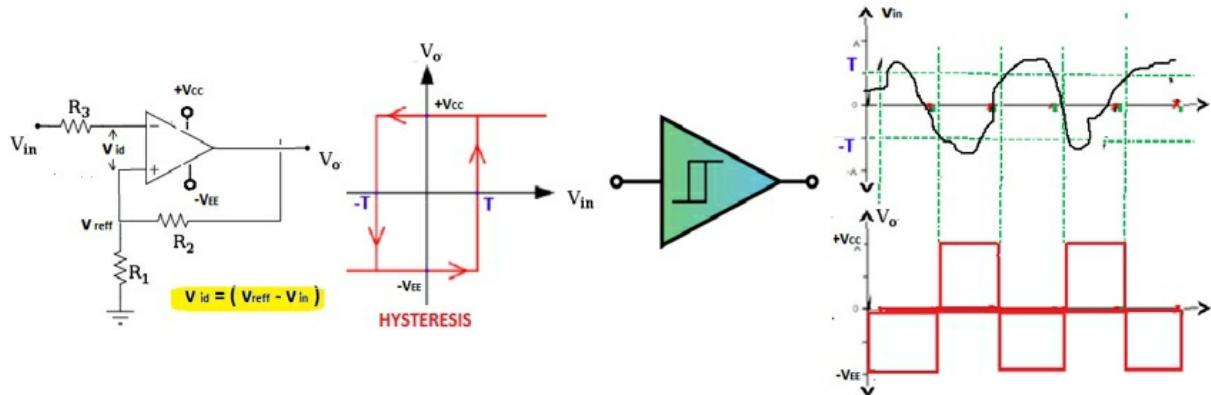
Fig. 18

### (C) Schmitt Trigger

**Definition :-** Schmitt trigger is a comparator circuit with hysteresis implemented by applying positive feedback to the non-inverting input of a comparator or differential amplifier. It is an active circuit which converts an analog input signal to a digital output signal.

### Applications

- To convert Sine waves into Square waves.
- To eliminate Noise in Comparators.
- They can also act as simple ON / OFF Controllers (for example, temperature based switches).



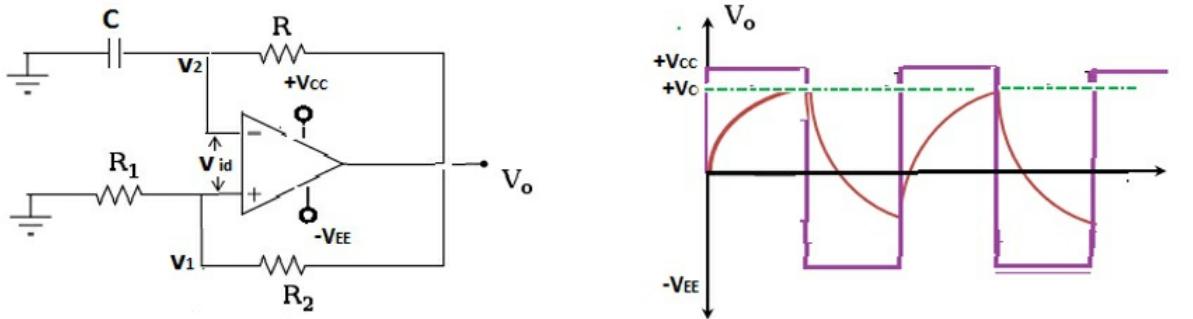
**Fig. 19**

The circuit has a Positive Feedback at the Non-Inverting terminal. The output voltage switches between the limits  $+V_{CC}$  &  $-V_{EE}$ . The Switching occurs at the Input Signal Thresholds  $+T$  &  $-T$  respectively. Operation of the circuit is controlled by the Hysteresis Loop. When the Output attains a certain saturation level, say  $+V_{CC}$ , it remains at this voltage until and unless the Input reaches the Lower Threshold Level  $-T$ . As soon as input equals this Threshold Level, the output switches to the Lower Saturation voltage  $-V_{EE}$ . It remains at this voltage again, until the input signal attains the Upper Threshold value  $+T$ . When this happens, the output switches to the Upper Saturation Voltage  $+V_{CC}$ . This cycle repeats. Such a cycle is called a Hysteresis Loop.

#### **(D) Astable Multivibrator or**

#### **Square wave Generator**

Astable Multivibrator is a circuit that spontaneously produces a Square Wave Output. Spontaneous output refers to the situation where there is no apparent input. Astable Multivibrators are also called “Free Running Multivibrator”.



**Fig. 20**

Assume that, at  $t = 0$ , the charge on the Capacitor is 0. Thus at  $t = 0$ ,  $V_C = 0$ . Since the Inverting terminal voltage is shown as  $v_2$ , have  $v_2 = 0$  at  $t = 0$ . The Output Offset Voltage of the OPAMP feeds back the quantity  $v_1$  at the Non-Inverting terminal.

$$v_1 = \frac{R_2 \cdot V_{OFFSET}}{(R_1 + R_2)}$$

Since  $v_1$  is positive, the Input Differential Voltage  $v_{id}$  is also positive. Therefore the output of the OPAMP is driven to the Positive Saturation value  $+V_{CC}$ . Now the voltage  $v_1$  is still positive, as

$$v_1 = \frac{R_2 \cdot V_{CC}}{(R_1 + R_2)}$$

Since  $v_1$  is still positive, output remains at  $+V_{CC}$ . Thereafter the Capacitor begins to charge up towards  $+V_{CC}$  through the resistance  $R$ . Capacitor charging follows an exponential graph, as shown in the diagram above. As soon as voltage across the capacitor  $V_C$  slightly exceeds  $v_1$ , and since  $v_2 = V_C$ , the Input Differential Voltage  $v_{id}$  is now negative, as

$$v_{id} = (v_1 - v_2) \quad \& \quad v_2 = V_C \quad \& \quad V_C > v_1$$

Since  $v_{id}$  is now negative, the output of the OPAMP is driven into the saturation value  $-V_{EE}$ . From this point onwards the feedback voltage  $v_1$  is negative, as

$$v_1 = \frac{R_2 \cdot (-V_{EE})}{(R_1 + R_2)} = -v_1$$

This negative feedback voltage keeps the output fixed at  $-V_{EE}$ . Now the Capacitor quickly discharges, and recharges towards the negative voltage. As soon as the voltage across the Capacitor is more negative

than  $v_1$ , the Input Differential Voltage  $v_{id}$  becomes positive and drives the output of the OPAMP back to  $+V_{CC}$ . This cycle keeps repeating at the frequency  $f_O$ , given by

$$f_O = \frac{1}{2 R C \ln[(2 R_1 + R_2)/R_2]} \quad \dots(19)$$

Using a value of resistance  $R_2 = 1.16 R_1$

We can simplify the expression for frequency as

$$f_O = \frac{1}{2 R C} \quad \dots(19(a))$$

#### **(E) Triangular Wave Generator & Saw-Tooth Wave Generator.**

Integration of a square wave is a Triangular Wave. Thus, when the output of an Astable Multivibrator is passed through an Integrator, we shall get a Triangular wave. However, the Integrator is in Inverting configuration, it would produce an output whose amplitude is negative. This can be “Re-Inverted” by an Inverter. (However, student is to note that there exists a configuration for Non-Inverting Integrator too).

A Saw-Tooth Wave Generator can be produced by a slight modification of the Integrator circuit. When the wiper of the potentiometer is towards  $+V$ , the Rising Time of the waveform is more than the Falling Time and vice-versa.

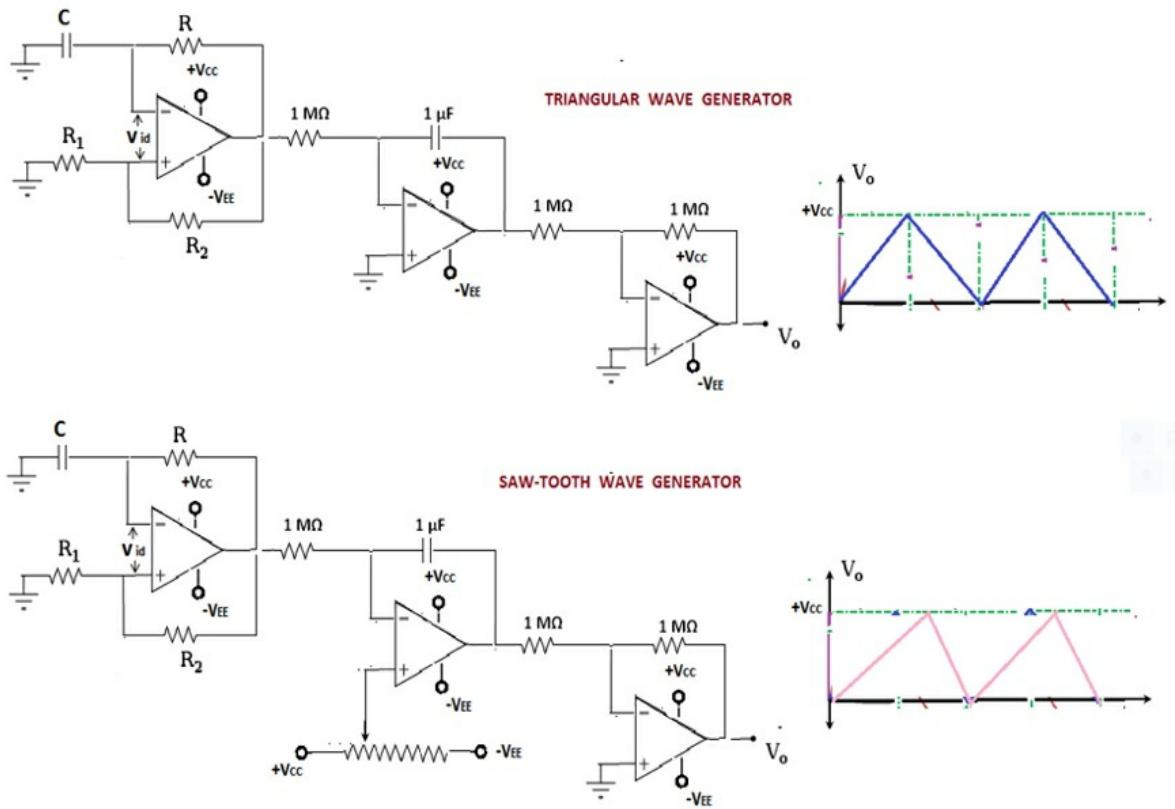


Fig. 21

### (F) Rectangular Pulse-Train Generator.

The Square Wave output of an Astable Multivibrator contains oscillations between Positive and Negative Half Cycles. If the Negative Half cycle is removed, we have a pulse-Train. This is simply achieved by adding a Diode at the output terminal of the Astable Multivibrator. Pulse-Train waveform is used as the Clock Pulses in Digital Electronics applications.

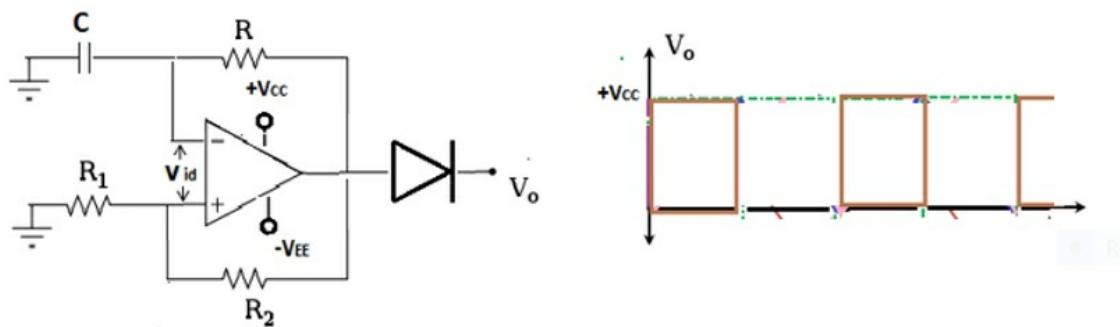
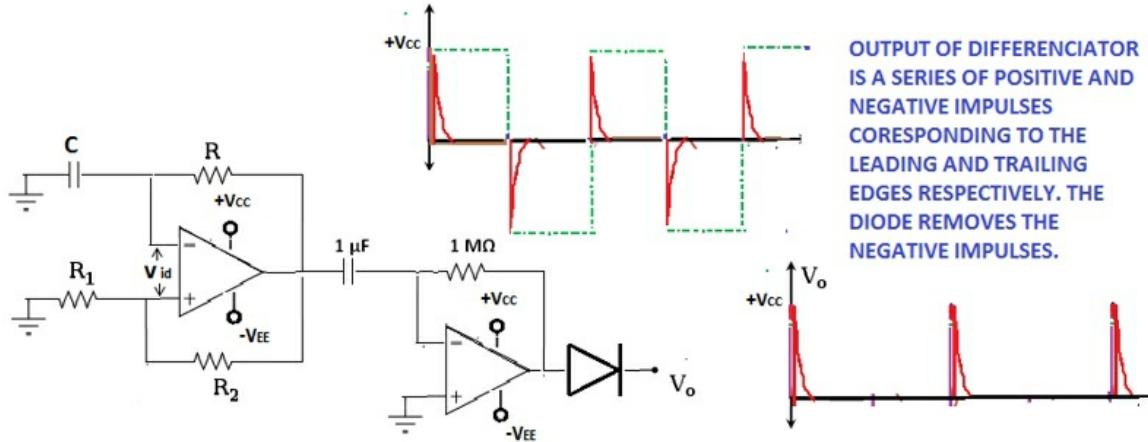


Fig. 22

### (G) Impulse-Train Generator or Delta Function Generator

Theoretically, an Impulse Function is defined as a Rectangular Pulse whose Pulse Width **tends to zero**. In practice, it is a Very Narrow Pulse. An Impulse can be obtained by extracting the **Leading or Trailing Edge** of a Rectangular Pulse. An edge of a pulse is the point at which the amplitude of the function makes a transition. A transition can be defined as **Rate of Change of Amplitude**. Mathematically, rate of change of amplitude is determined by taking the First Derivative of the function.

Hence, when we pass the output of an Astable Multivibrator through a Differentiator, we obtain a series of Impulses at each Leading and Trailing Edge of the square wave output of the Astable Multivibrator. If the negative Impulses are removed by a Diode, we have an Impulse-Train as the output signal.



**Fig. 23**

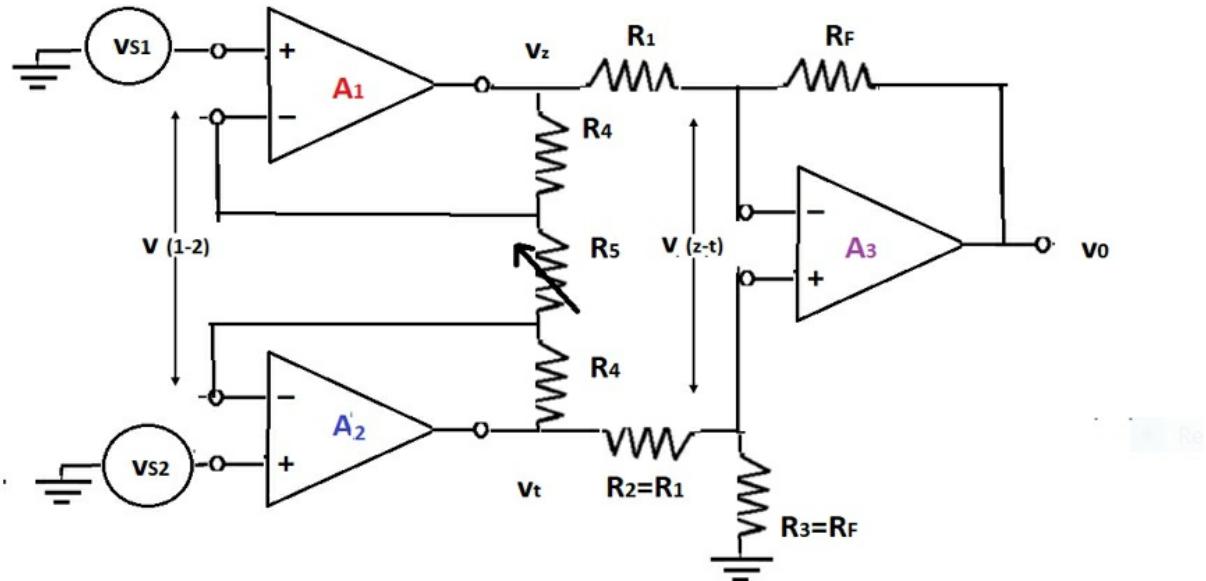
## 10.9 ANALOG ELECTRONIC APPLICATIONS BASED ON OPAMPS

### (1) INSTRUMENTATION AMPLIFIER

- In the field of Instrumentation Engineering, often very weak signals are encountered. In order to make these signals useful, a very large amount of amplification must be provided.
- If a single amplifier is used, it will be vulnerable to noise and instability.

- In order to avoid this, a Difference Amplifier is used. In a Difference Amplifier, instead of amplifying the weak signal by itself, its difference with a 0V ‘Reference Signal’ is amplified. A 0V reference is the Ground Point of the circuit.
- A simple Difference Amplifier, in the ‘Subtractor Configuration’ has two disadvantages, namely-
  - a) The Input Impedance at the two input terminals are not equal.
  - b) The Gain and Input Impedance of the Difference Amplifier are not adjustable.

The Difference Amplifier used in the field of Instrumentation Engineering is called an '**Instrumentation Amplifier**'.



**Fig. 24**

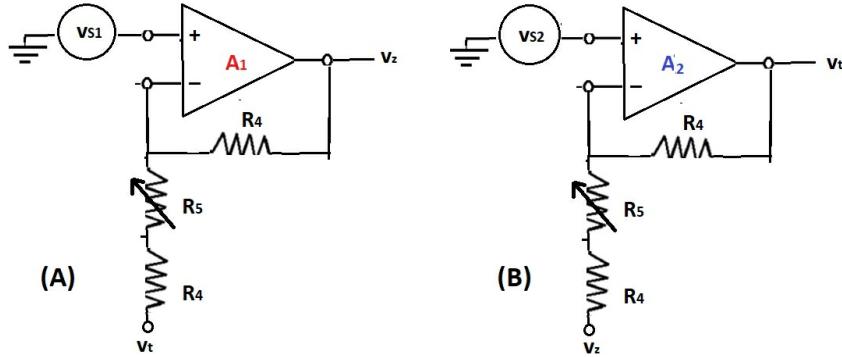
## ANALYSIS

- The first stage is shown separately for each of the sources. Both the stages are analyzed with Law of Superposition.
- From Part (A), assuming  $v_t = 0$ , we have a ‘Non-Inverting Amplifier’. Hence the output for this case is

$$v_{z1} = \frac{(2R_4 + R_5)}{(R_4 + R_5)} v_{s1} \quad (A)$$

- Next, in Part (A), assuming  $v_{s1} = 0$ , we have an ‘Inverting Amplifier’. Hence the output for this case is

$$v_{z2} = \frac{(-R_4)}{(R_4 + R_5)} v_t \quad (B)$$



- Therefore, by Superposition, we have

$$v_z = v_{z1} + v_{z2}$$

$$v_z = \frac{(2R_4 + R_5)}{(R_4 + R_5)} v_{s1} - \frac{(R_4)}{(R_4 + R_5)} v_t \quad (C)$$

- Similarly, from Part (B), we have case is

$$v_{t1} = \frac{(2R_4 + R_5)}{(R_4 + R_5)} v_{s2}$$

$$v_{t2} = \frac{(-R_4)}{(R_4 + R_5)} v_z$$

$$v_t = \frac{(2R_4 + R_5)}{(R_4 + R_5)} v_{s2} - \frac{(R_4)}{(R_4 + R_5)} v_z \quad (D)$$

- The output of the First Stage is given by  $v_{zt}$ . This is obtained from (C) & (D) as

$$v_{zt} = v_z - v_t$$

$$v_{zt} = \frac{(2R_4 + R_5)}{(R_4 + R_5)} (v_{s1} - v_{s2}) + \frac{(R_4)}{(R_4 + R_5)} (v_z - v_t)$$

$$v_{zt} = \frac{(2R_4 + R_5)}{(R_4 + R_5)} (v_{s1} - v_{s2}) + \frac{(R_4)}{(R_4 + R_5)} v_{zt}$$

Rearranging,

$$\left\{1 - \frac{(R_4)}{(R_4 + R_5)}\right\} v_{zt} = \frac{(2R_4 + R_5)}{(R_4 + R_5)} (v_{s1} - v_{s2})$$

$$\therefore \left\{\frac{(R_5)}{(R_4 + R_5)}\right\} v_{zt} = \frac{(2R_4 + R_5)}{(R_4 + R_5)} (v_{s1} - v_{s2})$$

From this we get the **Differential Gain** of the First Stage as

$$A_{D1} = \frac{v_{zt}}{(v_{s1} - v_{s2})}$$

Substituting and simplifying,

$$A_{D1} = \frac{(2R_4 + R_5)}{(R_5)} \quad (E)$$

- The second stage is a Difference Amplifier, with the input 'v<sub>zt</sub>'. Gain of the Second Stage is given by

$$A_{D2} = \frac{-R_F}{R_1} \quad (F)$$

- From (E) and (F) the overall gain of the circuit is

$$A_D = A_{D1} \cdot A_{D2}$$

$$\therefore A_D = - \left[ \frac{(2R_4 + R_5)}{(R_5)} \right] \cdot \left[ \frac{R_F}{R_1} \right]$$

$$\therefore A_D = - \left[ 1 + \frac{(2R_4)}{(R_5)} \right] \cdot \left[ \frac{R_F}{R_1} \right] \quad (20)$$

- The Gain can be made adjustable by the use of the potentiometer R<sub>5</sub>.
- Since the figures in Part (A) and Part (B), used in the analysis are exactly the same, the Input Impedance at the two input terminals is BALANCED and ADJUSTABLE.

## (2) PRESION RECTIFIER

- ❖ A general-purpose rectifier is designed to convert 230V, 50Hz domestic AC into a DC. In this case the ‘Forward Voltage Drop’ of 0.7V across the diodes can be neglected. The internal Transition Capacitance and Diffusion Capacitance of the diodes can also be neglected at low frequency operation.
- ❖ In the fields of Communication Engineering and Instrumentation Engineering, often the circuits have to work with very low power signals of magnitudes of a few milli volts or less. These signals are often of very high frequencies, in the range of KHz to MHz.
- ❖ In such cases, the 0.7 V drop across the diode is significantly greater than the signal amplitude itself. The Transition and Diffusion Capacitances of the diode also impairs the High Frequency Response of the circuit.
- ❖ An ‘Ideal Diode’ is one in which the Forward Dynamic Resistance is ‘0’ and Reverse Resistance is ‘ $\infty$ ’. There is no internal capacitance and Due to this there is no effect of the internal capacitances of the diode.
- ❖ An ‘Ideal Diode’ or a ‘Super Diode’ is simulated using the two standard diodes with the OPAMP, as shown in the diagram below.

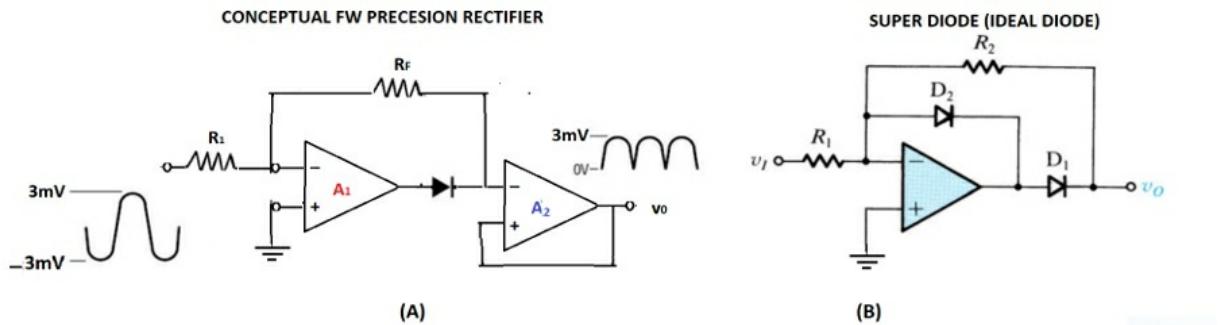


Fig. 25

### WORKING PRINCIPLE

- **Ideal Diode (Super Diode) :-** Ideal Diode is simulated with the two diodes connected in the feedback path of the Inverting Configuration of the OPAMP. This is shown in part (B) of the Fig. 25 above. If the input ‘ $v_i$ ’ is positive, the OPAMP inverts it into a negative voltage at its output point. This will reverse bias the ‘real

diode'  $\mathbf{D}_1$ . The Final Output will be '0'. If the input ' $v_i$ ' is negative, the 'real diode'  $\mathbf{D}_2$  will not conduct. But the Inverting Feedback combination of  $\mathbf{R}_2$  and  $\mathbf{R}_1$  will produce a positive voltage at the Final Output. The Forward Voltage Drops of the two real diodes will be ineffective due to the OPAMP. Again, since the real diodes are not included in the circuit operation when it is functioning as the inverting amplifier, the internal capacitances of the real diodes do not come into the picture.

- **Full Wave Precision Rectifier**

- The Conceptual circuit is shown in the part (A) of the **Fig. 25**, above. The first OPAMP  $A_1$  is in Inverting Configuration.
- At the negative half cycle, the output produced by the OPAMP  $A_1$  would be positive. This will forward bias the diode and the output would be the 'inversion' of the negative half cycle.
- The second OPAMP  $A_2$  is in 'Voltage Follower' configuration. Thus, the positively inverted signal would be 'Buffered' to the output.
- At the positive half cycle, the output produced by the OPAMP would be negative. This would reverse bias the diode and the output at the cathode of the diode is '0'. This is the right hand side of the feedback path resistance  $R_F$ . The left end of this resistance is already at 'virtual zero'. In other words, voltage drop across  $R_F$  is 0, hence,  $R_F$  is a 'virtual short circuit'.
- The virtual short circuit would transfer the positive half cycle to the Buffer and this will therefore be reproduced at the output.

### (3) **POWER AMPLIFIER**

#### WORKING PRINCIPLE

- ✓ The circuits in the Figures (A) and (B) and (C) are general purpose Power Amplifiers with a large working bandwidth. They work on the principle of the Class AB Push-Pull Power Amplifier.
- ✓ In circuits (A) and (B), the OPAMP at the Input Stage is a Broad

## Band Voltage Amplifier in Non-Inverting Configuration.

- ✓ This is followed by the Complementary Symmetry Class-AB Push-Pull amplifier with either BJT or MOSFET.

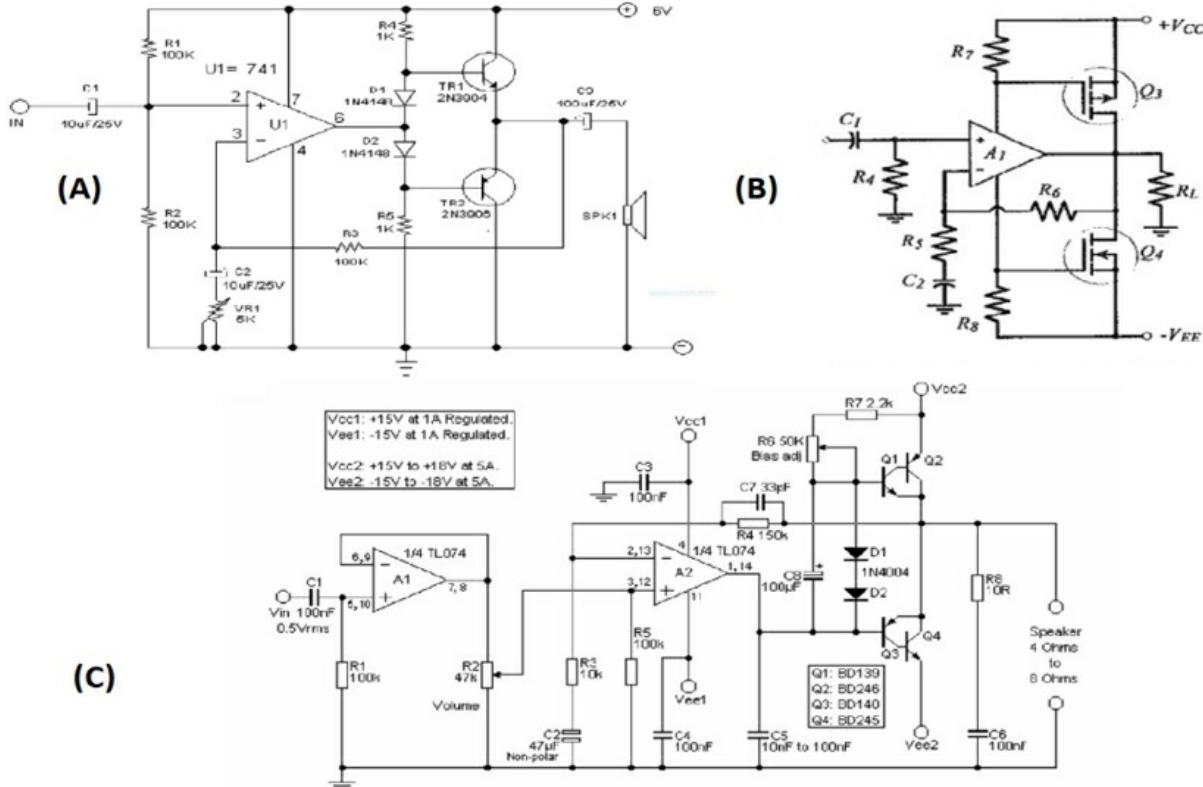


Fig. 26

- ✓ The circuits use RC coupling with source and load.
- ✓ The diodes in the base of the transistors stabilize the Base Bias at 0.7 V to ensure Class-AB operation, so that cross over distortion is eliminated.
- ✓ The circuit in Figure (C) is an improvement of the same principle. This provides a very large Power Gain and large Output Power.
- ✓ The first OPAMP is in Voltage Follower Configuration to provide a large bandwidth and reduce noise.
- ✓ The second OPAMP is in Non-Inverting Configuration. The Feed-Back is taken from final the output point of the circuit, so as to further eliminate noise and distortions that may creep in at the Push-Pull stage.
- ✓ There are additional capacitors at the V<sub>CC</sub> input to further reduce DC Power Supply Ripples.

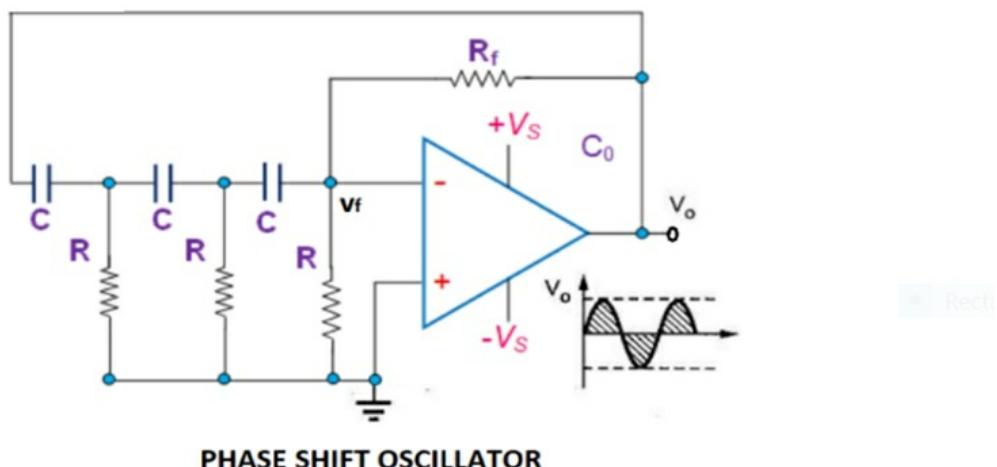
- ✓ The Push-Pull stage uses Darlington Configuration to generate a very large power gain and support a large current rated load.
- ✓ All these circuits have a potentiometer either at the feed-back path or at the input point to adjust the gain.

#### (4) RC OSCILLATOR

- The Electronic Oscillator consists of an Amplifier and a Positive Feedback Network. In order to obtain sustained sinusoidal oscillation, Barkhausen Criteria need to be satisfied.
- RC oscillators with Transistor as amplifying device have certain problems of stability, linearity and difficulty in adjustment for condition oscillation.
- RC Oscillators can be configured easily with OPAMP. The circuit for the two most commonly used RC Oscillator configurations are

1. Phase-Shift Oscillator
2. Wien Bridge Oscillator.

- The circuits of both of them are shown below, along with the **Condition of oscillation and Frequency of oscillation**. The method for deriving condition of oscillation and frequency of oscillation are the same as we those as in the case of the Transistor oscillator.



**Fig. 27**

## WORKING PRINCIPLE PHASE SHIFT OSCILLATOR

- OPAMP is in Inverting Amplifier Configuration. Thus, it imparts a  $-180^0$  phase Shift. The three cascaded RC sections in the Feedback Path imparts an equal amount of phase shift, so that the net phase shift around the loop is 0. This is one part of the Barkhausen Criteria.
- From the figure above we can evaluate “B”, the Gain of the Feedback Loop as

$$B = \frac{V_f}{V_o} = \frac{-j(\omega R C)^3}{[1 - 6(\omega R C)^2] - j\{(\omega R C)^3 - 5(\omega R C)\}} \quad \dots(A)$$

- For the OPAMP in Inverting configuration, the Gain of the amplifier section is

$$A = -\frac{R_F}{R_1} \quad \dots(B)$$

- In order to fulfill Barkhausen Criteria we have

$$A \cdot B = 1$$

From equations (A) & (B) we have

$$-\frac{R_F}{R_1} \cdot \frac{-j(\omega R C)^3}{[1 - 6(\omega R C)^2] - j\{(\omega R C)^3 - 5(\omega R C)\}} = 1$$

- Simplifying and rearranging, we have

$$\{1 - 6(\omega R C)^2\} + j \left[ \left( \frac{R_F}{R_1} + 1 \right) (\omega R C)^3 + 5(\omega R C) \right] = 0$$

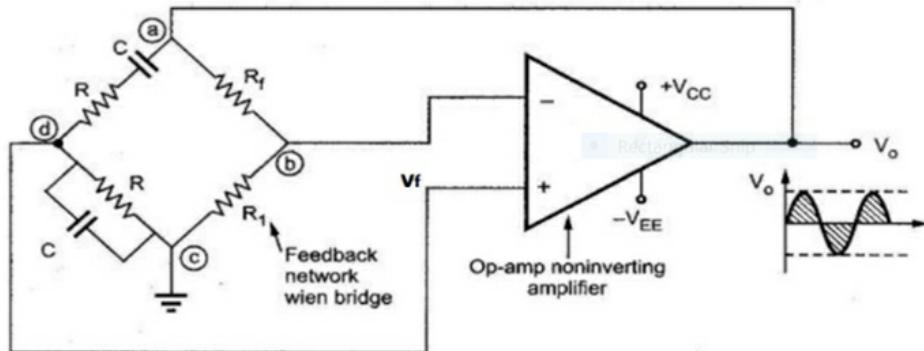
- Equating the Real Part to 0 and simplifying, we obtain the frequency of oscillation as

$$f_0 = \frac{1}{2\pi\sqrt{(6)R C}} \quad \dots(21)$$

- Equating the Imaginary Part to 0 and simplifying, we obtain the Condition of oscillation as

$$\frac{R_F}{R_1} = 29 \quad \dots(22)$$

## WIEN BRIDGE OSCILLATOR



WIEN BRIDGE OSCILLATOR

Fig. 28

- OPAMP is in Non-Inverting Amplifier Configuration. In this the resistances  $R_1$  &  $R_f$  are those associated with the amplifier section. The series and parallel combination of the couple of equal resistance and capacitance,  $R$  &  $C$  constitute the Positive Feedback path for the oscillator.
- From the circuit, the Gain of the Feedback Network is

$$B = \frac{j(\omega R C)}{[1 - (\omega R C)^2] + j 3(\omega R C)} \quad \dots(A)$$

And the gain of the Non-Inverting amplifier is

$$A = \left(1 + \frac{R_f}{R_1}\right) \quad \dots(B)$$

- In order to satisfy Barkhausen Criteria, we must have  $A B = 1$
- Substituting from equations (A) & (B)

$$\left(1 + \frac{R_f}{R_1}\right) \cdot \left\{ \frac{j(\omega R C)}{[1 - (\omega R C)^2] + j 3(\omega R C)} \right\} = 1$$

Simplifying and rearranging, we have

$$[1 - (\omega R C)^2] + j \left[ (3(\omega R C)) - \left(1 + \frac{R_f}{R_1}\right)(\omega R C) \right] = 0 \quad \dots(C)$$

- Equating the Real part to 0 we get the **frequency** of oscillation as

$$f_0 = \frac{1}{2\pi R C} \quad \dots(23)$$

Equating the Imaginary part to 0 we get the **Condition** of oscillation as

$$\left(1 + \frac{R_f}{R_1}\right) = 3 \quad \dots(24)$$

## (5) ANALOG ELECTRONIC SIMULATION

- Physical systems can be modeled by means of Differential Equations. Solution of the differential equation of the system enables an evaluation of the system performance under various operating conditions.
- A differential equation is a combination of various mathematical operations such as Integration, Differentiation, Multiplication, Addition and Subtraction.
- We had studied in the previous sections that OPAMPS are capable of performing these operations electronically. Therefore, these OPAMP based circuits can be used for the simulation of a differential equation.
- Digital Simulation is Off Time Simulation. Therefore, effect of Dynamic Disturbances may not be accurately studied. This is overcome by Analog Simulation.

### Differential Equation of an Electrical System

An Electrical Circuit, consisting of Resistances, Inductances, Capacitances, Current Source and Voltage Source is such a Physical System.



The Loop Equation of this circuit can be expressed as a Differential Equation as -

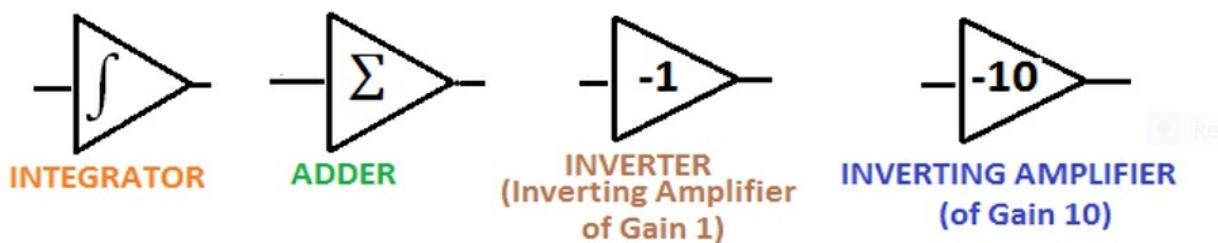
$$\begin{aligned}v_{(t)} &= R i + L \frac{di}{dt} + C \int i dt \\ \therefore L \frac{d^2i}{dt^2} + R \frac{di}{dt} + Ci &= \dot{v}_{(t)} = u(t)\end{aligned}$$

The Response of this circuit for different Forcing Functions and for different values of the Resistance, Inductance and Capacitance can be studied **with the help of Simulation**, instead of **wiring up the circuit**

each time for the different components to be used.

### Simulation

The modules used for analog electronic simulation of differential equations are the following analog OPAMP blocks we studied earlier. By convention, only Inverting Configuration is used. Again by convention, all the blocks must have a gain of either (-1) or (-10). Instead of using all the circuit details, only the block diagram representation is used. These are as shown below.



**Fig. 29**

Consider a 2<sup>nd</sup> order Differential Equation

$$A \frac{d^2x}{dt^2} + B \frac{dx}{dt} + C x = u(t)$$

Where 'A', 'B' & 'C' are constants. For simplicity, we assume these constants as '1'

$$\frac{d^2x}{dt^2} + \frac{dx}{dt} + x = u(t)$$

**Steps of Simulation are as follows**

1) Rewriting as –

$$\ddot{x} + \dot{x} + x = u(t)$$

$$\ddot{x} = u(t) - \dot{x} - x \quad \dots (a)$$

..

2) Assuming the second derivative,  $\ddot{x}$  is “available” as a signal at a certain point “A”, in a circuit, we can integrate it there to obtain  $-x$ . Negative sign appears, since the integrator is in

**Inverting Configuration.** Similarly,  $\dot{x}$  can be obtained by integrating  $-\ddot{x}$ .

- 3) Assuming that the Forcing Function “ $u(t)$ ” is available (from a Signal Generator), the signal  $\ddot{x}$  can be simulated by generating the RHS of Eq (a) with the help of an “Adder”. Since the Adder is in Inverting Configuration, the input to the Adder must be “Negative” of the RHS of the equation (a). In other words, we must apply the following signals as the input to the Adder.

(i)  $-u(t)$ ,

(ii)  $+x$

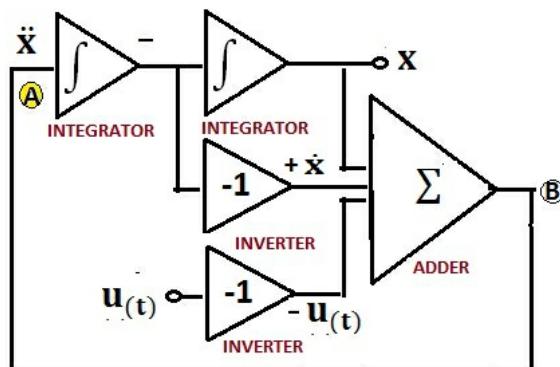
and

(iii)  $+ \dot{x}$

For this purpose, the Forcing Function  $u(t)$  and the signal  $-x$  from the output of the Integrator have to be Inverted before applying to the Adder.

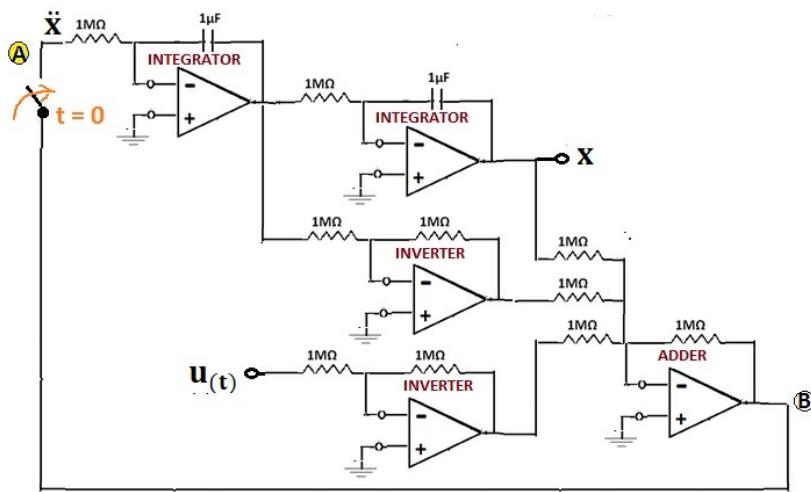
- 4) Thus at the output of the Adder,(Point “B”), we get the RHS of the equation (a). Thus the Point “B” has the same signal as that was assumed to be at Point “A”. Hence these two points are joined together to complete the simulation.

Using this principle, the Simulation of the differential equation (a) will be as follows—



This diagram above is known as “**Simulation Diagram**”. This is not a Circuit Diagram. The Circuit Diagram with details of the circuit elements used, will be as follows . Simulation will begin at the instant “ $t$

= 0” .



### Differential Equation with Numerical Coefficients

Consider an equation, such as

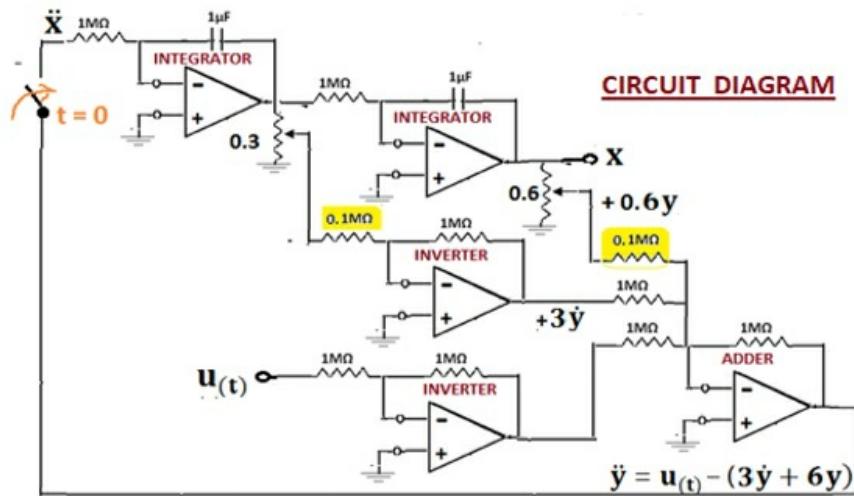
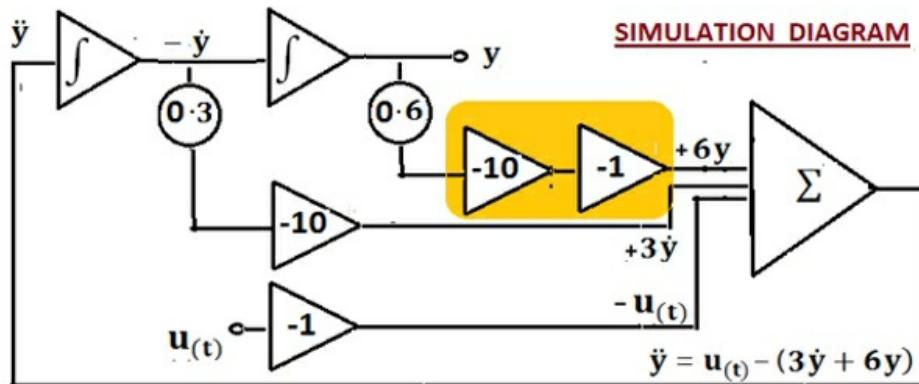
$$\ddot{y} + 3\dot{y} + 6y = u(t)$$

$$\therefore \ddot{y} = u(t) - (3\dot{y} + 6y) \quad (\text{RHS})$$

The RHS is to be “simulated by “adding” the “negative” of  $(3\dot{y} + 6y)$

with the “negative” of  $u(t)$  . This is shown with the Simulation Diagram, as follows—

In this, the circular block with the decimal fraction (e.g. **0.3** enclosed in a circle) represents a “Potentiometer” set at that value.



**Fig. 30**

The input resistance-feedback resistance combination in the “Inverting Amplifier” is  $0.1 \text{ M}\Omega - 1 \text{ M}\Omega$ . This combination imparts a gain of  $\left| \frac{0.1}{1} \right| = |10|$  to the signal obtained as  $-0.3 y$  from the potentiometer that is set at 0.3, so that the output of the Inverting Amplifier is  $+3y$ .

The signal from the second potentiometer is  $+0.6y$ . This line is imparted a gain of  $|10|$  with the same combination of input resistance-feedback resistance, in that line of the Adder.

### Optimization of Simulation Using Adding Integrator

In these simulations, the RHS of the given differential equation is generated by an Adder. The function of Addition can be combined with

the Integrator itself . This further optimizes the Simulation, and use of the number of OPAMPS is reduced. However, the RHS of the equation to be simulated has to be generated with the following modifications.

The differential equation that we had taken as example was—

$$\ddot{y} + 3\dot{y} + 6y = u_{(t)}$$

Rewriting the RHS as

$$\ddot{y} = u_{(t)} - 3\dot{y} - 6y \text{ (RHS)}$$

The justification for the use of “Adder-Integrator” in the Simulation Diagram will be as follows—

- (i) In Fig. 30, we see that the path corresponding to “ $-6y$ ” passes through two inverting stages, followed by another ‘Inversion’ at the adder. This could be implemented by using a single inversion. The required gain of  $|10|$  will have to be introduced by the “Adder Integrator” stage.
- (ii) The path corresponding to “ $-3\dot{y}$ ” has a “Double Inversion”, with a gain of  $|10|$ . This can also be implemented in the “Adder Integrator” stage.

The resulting Simulation Diagram and the Physical Circuit Diagram is also shown in Fig. 31.

## Initial Condition

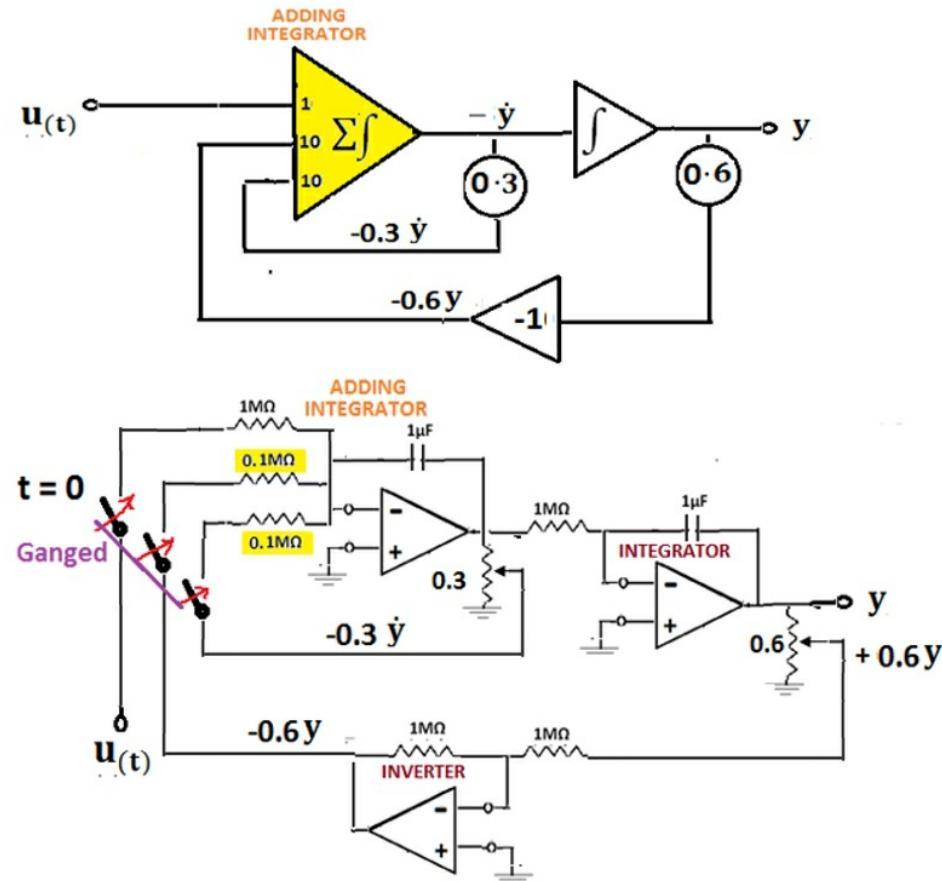
Differential equations, often, have Initial Conditions. Initial Condition is the “Initial State” of the system, at  $t = 0$ . This instant “ $t=0$ ” is that instant of time when the system starts. Using the same equation as in the previous examples, if we introduce Initial Conditions, we have the representation as follows –

$$\ddot{y} + 3\dot{y} + 6y = u_{(t)}$$

**Initial Conditions**     $\dot{y}_{(0)} = 4.7$      $y_{(0)} = -3.24$

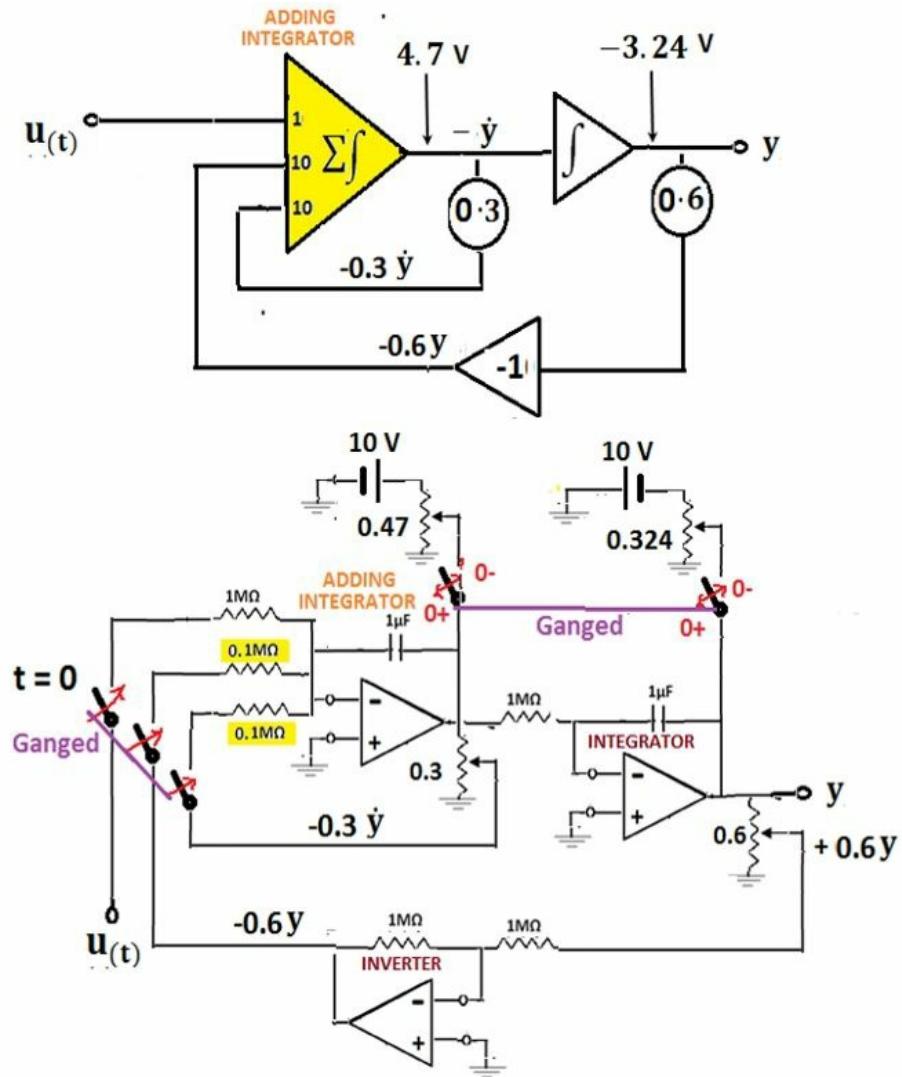
In case of the simulation of the process, Initial Condition means the DC voltage existing at the instant ‘ $t=0$ ’, at the respective point of the circuit, where that function is to be generated. This is implemented by “Introducing” the appropriate DC voltage at the relevant point of the

circuit. This is done using a DC voltage source and a Potentiometer, set at the predetermined position. This DC voltage is to be introduced, momentarily, exactly at an instant just before the “start” of simulation, i.e. “ $t = 0_-$ ” and switched off immediately after, exactly at the instant “ $t = 0_+$ ”



**Fig. 31**

The Simulation Diagram and the circuit for the differential equation with Initial Condition is shown in Fig. 32, below –



**Fig. 32**

## 10.10 Active Butterworth Filter

An Electronic Filter is a circuit that selects signals within a certain range of frequencies to pass through and rejects the signals whose frequency is outside this range. **The range of frequencies allowed is The Bandwidth or Pass-Band of the filter.**

**Bandwidth of a Filter** is defined as the range of frequencies that a filter passes with a voltage gain greater than or equal to  $1/\sqrt{2}$  times the Maximum Gain.

According to this definition the following types of filters are used in practice. The shape of the Voltage Gain vs Frequency graph shown in

the diagram pertain to a specific class of filters called “Butterworth Filters”. The Butterworth characteristic is the most desired form of filters, since the Gain in the Pass band is constant. Since OPAMPS provide a constant Voltage Gain, their use results in Butterworth filters.

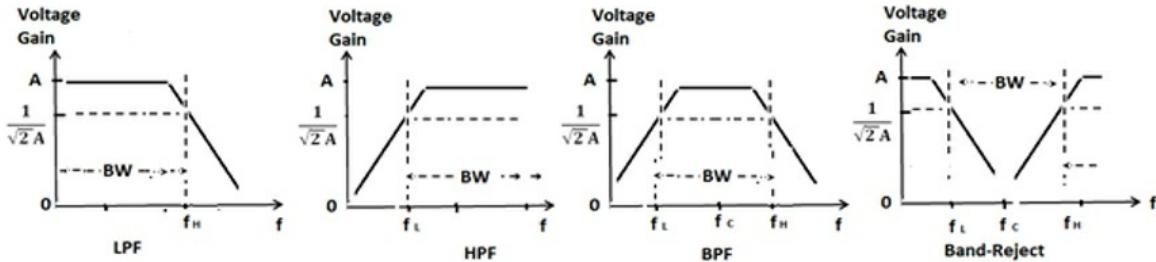


Fig. 33

• Rec

**(A) Low Pass Filter (LPF) :-** A filter which passes a range of frequencies from 0 to a certain “Higher Cutoff Frequency” ( $f_H$ ) is called a Low Pass Filter, abbreviated as LPF. The circuit in Fig (A) is a LPF.

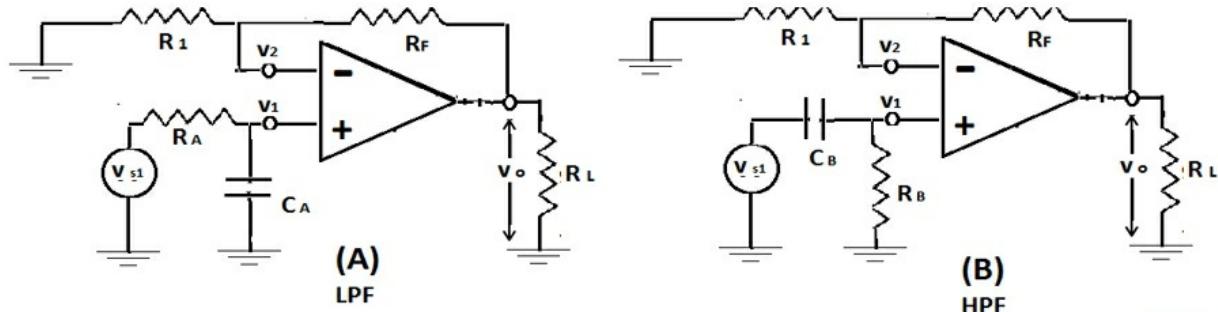


Fig. 34

• Rec

The circuit in the Fig.(A) is in Non-Inverting Configuration. The potential at the Non-Inverting Terminal is given by the Voltage Divider Rule as

$$V_1 = \frac{jX_{CA}}{(R_A - jX_{CA})} V_s$$

Where  $X_{CA}$  is the Capacitive Reactance of the capacitor  $C_A$ , given by

$$X_{CA} = \frac{1}{2\pi f C_A}$$

$$\therefore -j X_{CA} = \frac{1}{j 2\pi f C_A}$$

Substituting in the expression for  $V_1$  we have

$$\mathbf{v}_1 = \frac{\left(\frac{1}{j 2\pi f C_A}\right)}{\left\{R_A + \left(\frac{1}{j 2\pi f C_A}\right)\right\}} \mathbf{v}_s$$

$$\mathbf{v}_1 = \frac{\left\{\mathbf{v}_s / j 2\pi f C_A\right\}}{\left\{(1+j 2\pi f R_A C_A) / j 2\pi f C_A\right\}}$$

Simplifying we have

$$\mathbf{v}_1 = \frac{\mathbf{v}_s}{1+j 2\pi f R_A C_A}$$

In this expression the term  $R_A C_A$  is the “Time Constant” of the frequency sensitive network connected with the source. This has the dimension of “Time”. The reciprocal of time has the dimension of frequency.  $2\pi$  is dimensionless. Let the reciprocal of  $2\pi R_A C_A$  be denoted by a frequency term “ $f_H$ ”, so that

$$f_H = \frac{1}{2\pi R_A C_A} \quad \dots(25)$$

The frequency  $f_H$  is the “Upper Cut-Off Frequency”. The filter does not work at frequencies higher than this.

$$\therefore \mathbf{v}_1 = \frac{\mathbf{v}_s}{1+j(f/f_H)}$$

The circuit in Fig.(A) is a Non-Inverting Amplifier with a Voltage Gain given by Eq.(7) and the output voltage as

$$\mathbf{A}_F = \left(1 + \frac{R_F}{R_1}\right) \quad \& \quad \mathbf{v}_o = \mathbf{A}_F \cdot \mathbf{v}_1$$

$$\text{Or} \quad \mathbf{v}_o = \mathbf{A}_F \cdot \frac{\mathbf{v}_s}{1+j(f/f_H)}$$

The overall Voltage Gain for the circuit is

$$\frac{\mathbf{v}_o}{\mathbf{v}_s} = \frac{\mathbf{A}_F}{1+j(f/f_H)}$$

This quantity is a Complex Quantity. The Magnitude of the Voltage gain is

$$\left| \frac{\mathbf{v}_o}{\mathbf{v}_s} \right| = \frac{\mathbf{A}_F}{\sqrt{1 + (f/f_H)^2}} \quad \dots(26)$$

Free-form Snip

1. In this expression, at a frequency  $f \ll f_H$  the term  $(f/f_H)$  in the denominator of the Eq.(26) tends to 0. Therefore the quantity Voltage Gain will be-

$$\left| \frac{v_o}{v_s} \right| = A_F = \left( 1 + \frac{R_F}{R_1} \right)$$

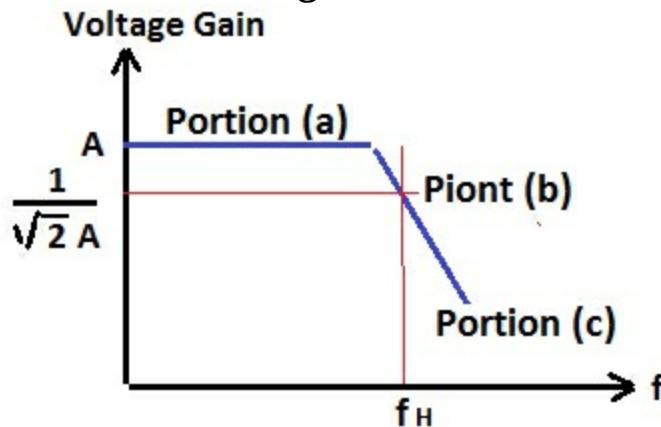
Since the ratio of the resistances is a constant, the overall Voltage Gain of the circuit is a constant when the circuit is driven by a low frequency source.

2. At a frequency  $f = f_H$  the magnitude of the Voltage Gain of the circuit will be

$$\left| \frac{v_o}{v_s} \right| = \frac{A_F}{\sqrt{2}}$$

3. At very high frequencies , when  $f \gg f_H$  the term  $(f/f_H)$  in the denominator of the Eq.(20) tends to Infinity. Therefore the quantity Voltage Gain will be 0.

**When we plot a graph between ‘A’ and ‘f ’ in view of the calculations above, we get the LPF characteristic.**



**(B) High Pass Filter (HPF) :-** A filter which passes a range of frequencies starting from certain Low Cutoff Frequency point ( $f_L$ ) to higher frequencies is called a High Pass Filter, abbreviated as HPF.. The circuit in Fig (B) is a HPF.

The circuit in the Fig.(B) is in Non-Inverting Configuration. The potential at the Non-Inverting Terminal is given by the Voltage Divider Rule as

$$\mathbf{V}_1 = \frac{R_B}{(R_B - jX_{CB})} \mathbf{V}_s$$

Substituting for  $X_{CB}$

$$X_{CB} = \frac{1}{2\pi f C_B}$$

$$\therefore -j X_{CB} = \frac{1}{j 2\pi f C_B}$$

Substituting in the expression for  $v_1$  we have

$$\begin{aligned}\mathbf{V}_1 &= \frac{R_B}{R_B + \frac{1}{j 2\pi f C_B}} \mathbf{V}_s \\ \mathbf{V}_1 &= \frac{R_B v_s}{\left\{ (1 + j 2\pi f R_B C_B) / j 2\pi f C_B \right\}}\end{aligned}$$

$$\text{Simplifying we have } \mathbf{V}_1 = \left[ \frac{j 2\pi f R_B C_B v_s}{1 + j 2\pi f R_B C_B} \right]$$

In this  $R_B C_B$  is the “Time Constant” of the frequency sensitive network connected with the source. Let the reciprocal of this be denoted by a frequency term “ $f_L$ ”, so that

$$f_L = \frac{1}{2\pi R_B C_B} \quad \dots(27)$$

The frequency  $f_L$  is the “Lower Cut-Off Frequency”. The filter does not work at frequencies lower than this.

$$\therefore \mathbf{V}_1 = \frac{j(f/f_L)v_s}{1+j(f/f_L)}$$

The output voltage for the circuit in Fig.(B) is

$$\text{Or } v_o = A_F \cdot \frac{v_s}{1+j(f/f_H)}$$

$$\text{Where } A_F = \left(1 + \frac{R_F}{R_1}\right)$$

The overall Voltage Gain for the circuit is

$$\frac{v_o}{v_s} = \frac{A_F(f/f_L)}{1+j(f/f_L)}$$

This quantity is a Complex Quantity. The Magnitude of the Voltage gain is

$$\left| \frac{v_o}{v_s} \right| = \frac{A_F(f/f_L)}{\sqrt{1+(f/f_L)^2}} \quad \dots(28)$$

1. In this expression, at a frequency  $f \ll f_L$  the term  $(f/f_L)$  in the numerator of the Eq.(28) tends to 0. Therefore the quantity Voltage Gain will be-

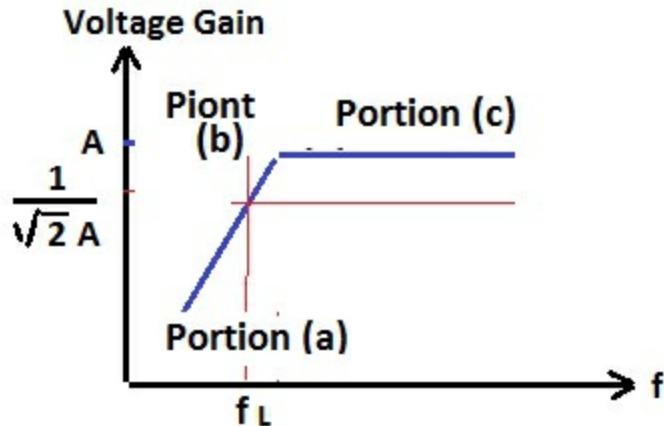
$$\left| \frac{v_o}{v_s} \right| = 0$$

- b. At a frequency  $f = f_L$  the magnitude of the Voltage Gain of the circuit will be

$$\left| \frac{v_o}{v_s} \right| = \frac{A_F}{\sqrt{2}}$$

3. At very high frequencies , when  $f \gg f_L$  the term  $(f/f_L)$  in the denominator will be such that  $(f/f_L) \gg 1$  . Therefore R.H.S. of the Eq.(28) tends to  $A_F$

**When we plot a graph between 'A' and 'f' in view of the points above, we get the HPF characteristic.**



**(C) Band Pass Filter (BPF) :-** A Band Pass Filter works between two Cut-Off frequencies,  $f_L$  and  $f_H$ . Within this “Pass Band” the gain of the filter is a constant. Beyond these two Cut-Off frequencies the gain drops sharply.

Such a filter can be obtained by the ‘Cascade’ connection of a HPF followed by a LPF. These two must be so designed with Resistors and Capacitors of such values that the Cut-off frequencies given by Eq.(25) and Eq.(27) evaluate to

$$f_L < f_H \dots (29)$$

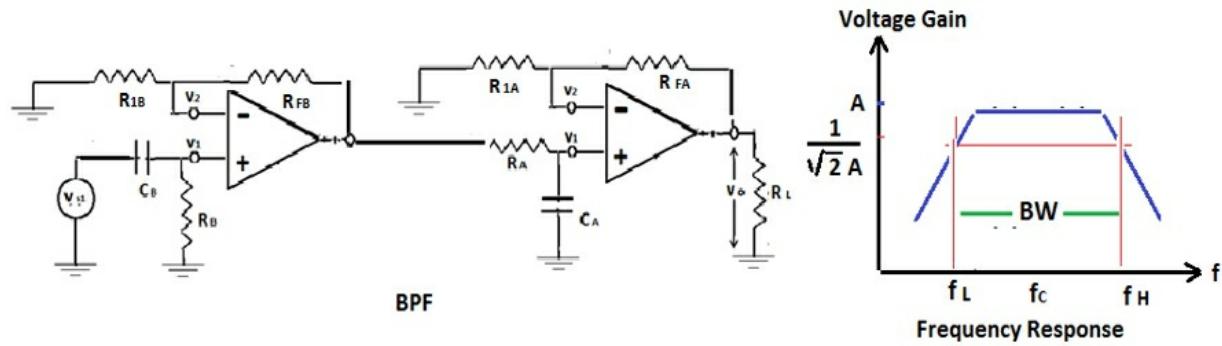
The “Centre Frequency” of the Pass Band is defined as the Geometric Mean of  $f_L$  and  $f_H$ .

$$f_c = \sqrt{f_L \cdot f_H} \quad \dots (30)$$

The Overall Gain of the BPF is the product of the Gains of the HPF and LPF stages.

$$\begin{aligned} A_F &= A_{FB} A_{FA} \\ A_F &= \left\{ 1 + \left( \frac{R_{FB}}{R_{1B}} \right) \right\} \cdot \left\{ 1 + \left( \frac{R_{FA}}{R_{1A}} \right) \right\} \quad \dots (31) \end{aligned}$$

The Circuit Diagram and The Frequency Response of the BPF is shown in the Fig. 35.



**Fig. 35**

**(D) Band Stop Filter :-** The purpose of a Band Reject Filter is to “Reject” a certain range of frequencies and Pass the signals of frequencies outside this range. The Band Reject Filter can be configured as a Parallel Combination of a LPF and a HPF followed by an ADDER, such that the Cut-Off frequencies of the two sections are

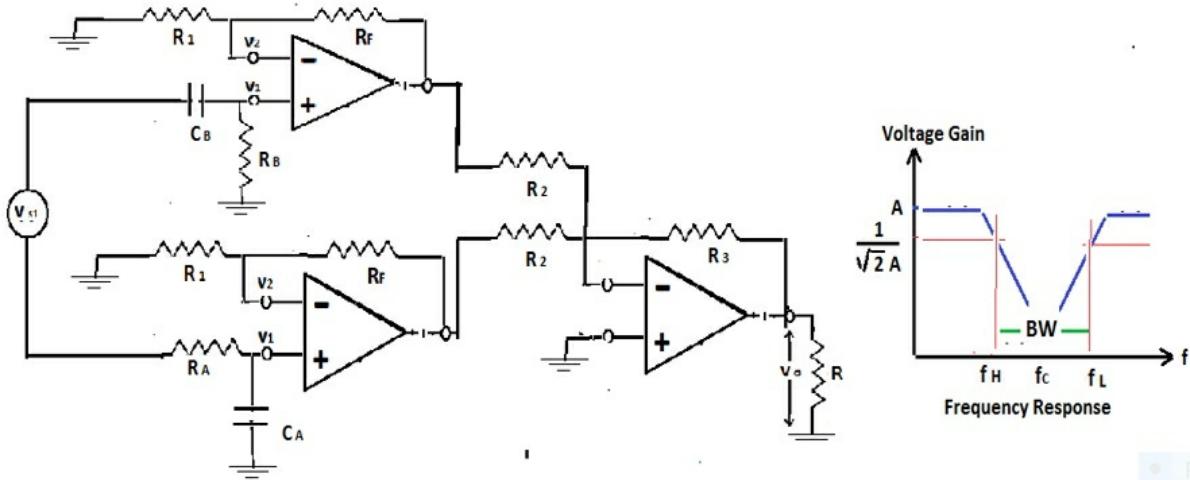
$$f_H < f_L \dots (32)$$

In the Band Reject Filter, the LPF and the HPF sections must have equal gains.

$$\therefore R_{1A} = R_{1B} = R_1 \quad \& \quad R_{FA} = R_{FB} = R_F \quad \dots (33)$$

With Overall Gain

$$|A_F| = \left| \left( \frac{-R_3}{R_2} \right) \right| \left\{ 1 + \left( \frac{R_F}{R_1} \right) \right\} \quad \dots (34)$$



**Fig. 36**

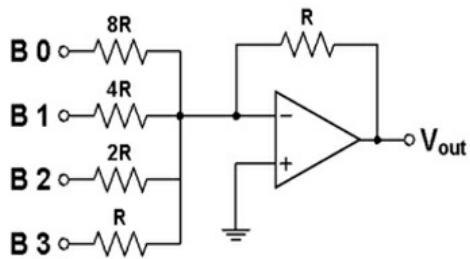
## 10.11 HYBRID ICs

**Hybrid ICs** are those whose constituents are both Analog as well as Digital in nature. Various Hybrid ICs are used in the field of electronics industry. A few of them are discussed in this section.

### **(1) Digital to Analog Converter (DAC)**

- A Digital signal consists of a string of Bits. These bits are arranged in Bytes. The byte represents a Binary Number.
- The ‘Value’ of the binary number is determined by the ‘Place Value’ of the bits and the ‘Decimal’ conversion of the binary number is the ‘Magnitude’ of the given Digital Signal.
- From the Hardware point of view, a Bit ‘1’ is a + 5 V pulse and a Bit ‘0’ is a 0 V pulse.
- The circuit used to convert the Binary number into the Decimal Value represents the conversion of the Digital Signal into Analog.
- There are various types of DAC. Out of these we discuss two types as follows-
  1. Adder Type DAC
  2. R-2R Ladder Type DAC.

#### **1. Adder Type DAC**



Digital Input Code				Analog Output Voltage
B3	B2	B1	B0	(V)
0	0	0	0	0.000
0	0	0	1	-0.625
0	0	1	0	-1.250
0	0	1	1	-1.875
0	1	0	0	-2.500
0	1	0	1	-3.125
0	1	1	0	-3.750
0	1	1	1	-4.375
1	0	0	0	-5.000
1	0	0	1	-5.625
1	0	1	0	-6.250
1	0	1	1	-6.875
1	1	0	0	-7.500
1	1	0	1	-8.125
1	1	1	0	-8.750
1	1	1	1	-9.375

Fig. 37

- Consider a 4-bit Binary number as an example. The four bits are **B<sub>3</sub>, B<sub>2</sub>, B<sub>1</sub>, B<sub>0</sub>**. Each of these bits can be either ‘1’ or ‘0’.
- The ‘Magnitude’ of the Binary number will be the summation of the ‘Place values’ of the bits. This is given by

$$\text{Magnitude} = B_3 \cdot 2^3 + B_2 \cdot 2^2 + B_1 \cdot 2^1 + B_0 \cdot 2^0 \quad (\text{A})$$

- Since this corresponds to a summation, it can be physically implemented by a process of addition, using an OPAMP adder circuit.
- In the circuit above, the OPAMP is in the Inverting Adder Configuration. Each individual unit of Binary Signal input to the circuit are the set of bits **B<sub>3</sub>, B<sub>2</sub>, B<sub>1</sub>, B<sub>0</sub>**. Each of these bits is either + 5 V or 0 V. Thus the output will be

$$v_o = -R \left( \frac{B_3}{R} + \frac{B_2}{R} + \frac{B_1}{R} + \frac{B_0}{R} \right)$$

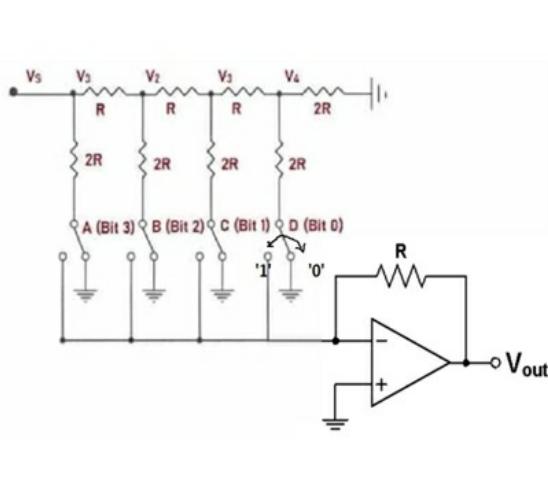
$$v_o = -(B_3 \cdot 2^0 + B_2 \cdot 2^{-1} + B_1 \cdot 2^{-2} + B_0 \cdot 2^{-3}) \quad (\text{B})$$

The expression (B) is equivalent to the expression (A). Hence, **the output of the Summing Amplifier is equal to the Analog Equivalent of the Binary signal.**

The use of this expression results in the adjoining table that shows the calculation of the magnitudes of the entire 4-bit Binary Count Sequence.

## 2. R-2R - Ladder Type DAC.

- Instead of using ‘Weighted Resistors’ as in the previous case, we can configure a circuit using a number of equal value resistors. This is known as the ‘R – 2R’ Network.



Digital Input Code				Analog Output Voltage (V)
A	B	C	D	
0	0	0	0	0.000
0	0	0	1	-0.625
0	0	1	0	-1.250
0	0	1	1	-1.875
0	1	0	0	-2.500
0	1	0	1	-3.125
0	1	1	0	-3.750
0	1	1	1	-4.375
1	0	0	0	-5.000
1	0	0	1	-5.625
1	0	1	0	-6.250
1	0	1	1	-6.875
1	1	0	0	-7.500
1	1	0	1	-8.125
1	1	1	0	-8.750
1	1	1	1	-9.375

Fig. 38

- The solution of this circuit is given by the following expression—

$$V_0 = -R \cdot \left\{ \frac{A}{2R} + \frac{B}{4R} + \frac{C}{8R} + \frac{D}{16R} \right\} \quad \dots(C)$$

- Using this expression the table of conversion of the 4-bit Binary count sequence into Analog is as shown above.

## (2) Analog to Digital Converter (ADC)

- For the purpose of conversion, the Analog signal is first ‘**Raised**’ (Clamped) to a positive level, above the x-axis. Next, it is “**Quantized**” (approximated) into a step function.
- Next, the instantaneous amplitude of the analog signal is compared with the “Quantized” value at successive instants of time.
- The outcome of this comparison is coded into a Binary Number, whose magnitude is proportional to the instantaneous amplitude of

the Analog Signal.

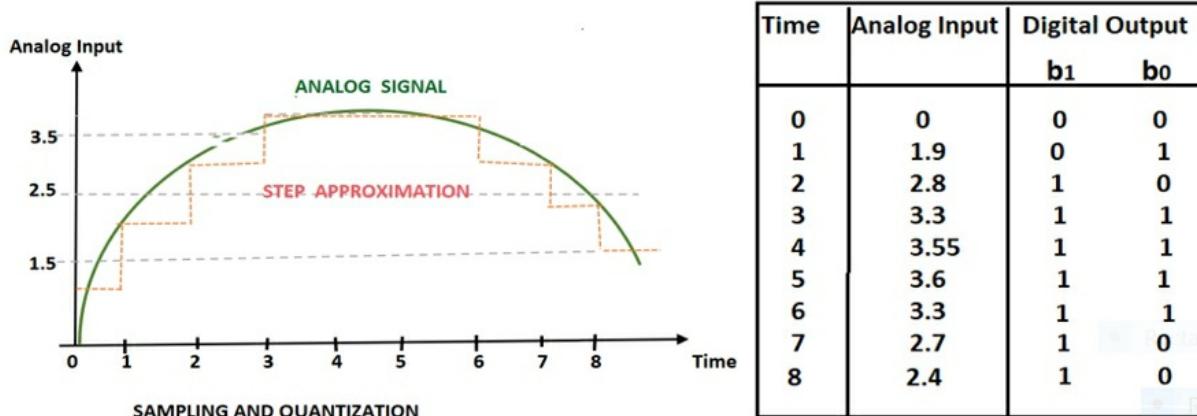
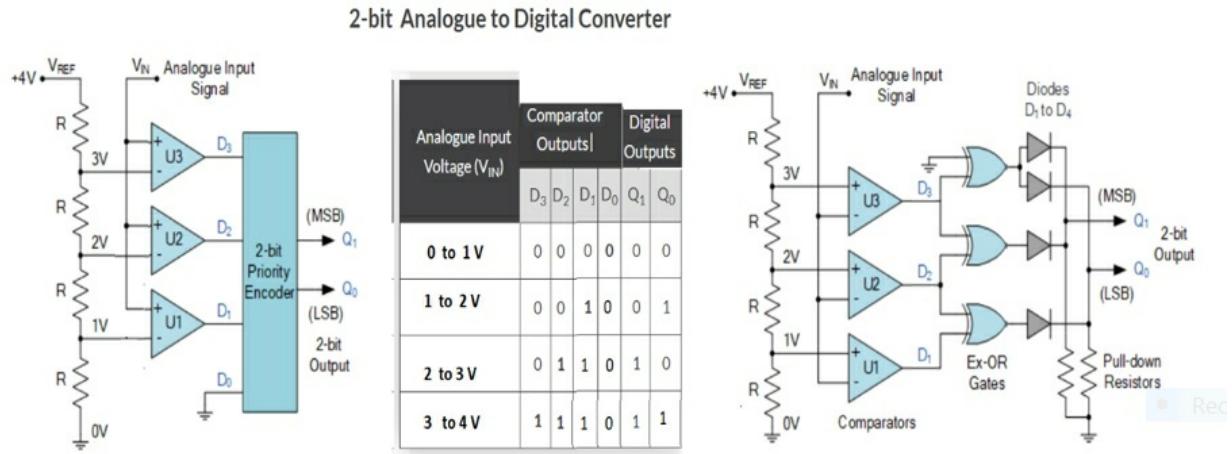


Fig. 39

- Using this principle, various types of ADC available in the industry. Two of the common types are the following-
  - Flash ADC
  - Successive Approximation ADC

### 1. Flash ADC

The principle of working of the Flash ADC is as follows-

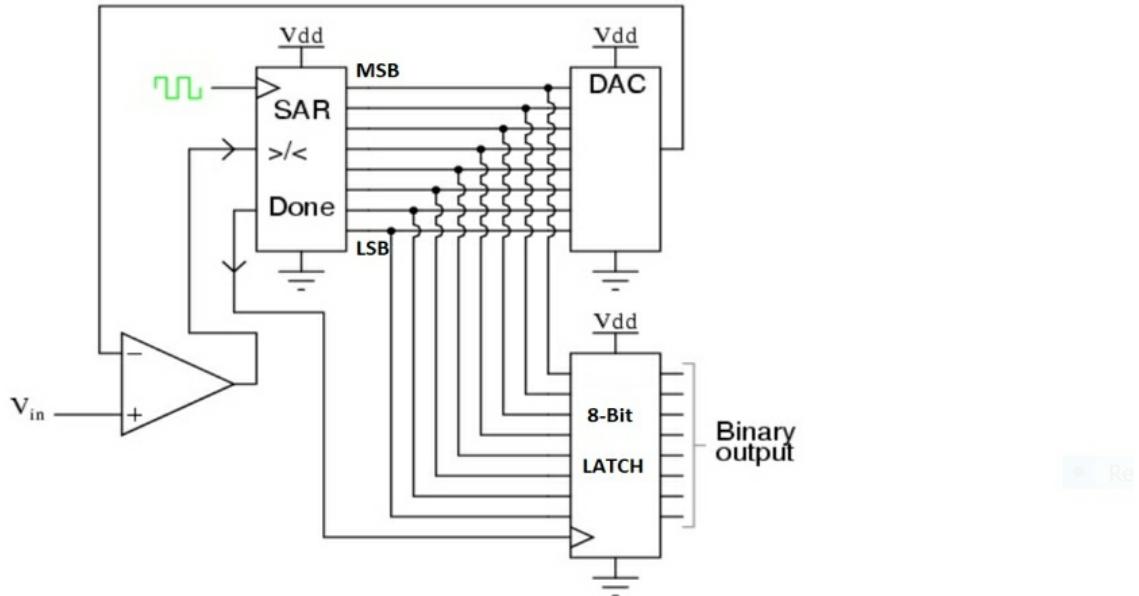


**Fig. 40**

- Consider a 2-bit system for simplicity. For a 2-bit system  $n = 2$  and hence we can have
- $2^n = 2^2 = 4$  levels of quantization. The maximum amplitude of the Analog Signal is assumed to be less than or equal to 4 V.
- For simplicity, a 4 V DC reference voltage is taken. This is divided into 4 equal voltage levels of 1 V each, with the four equal resistors 'R'.
- The Analog signal is shown to be steadily increasing. At the instant '0', the Analog amplitude is 0 V. When this is compared in the three OPAMP Comparators, all three of them produce a '0' output.
- When the Analog signal is between 1V to 2V, the Comparator U1 produce an output '1' and all other comparators produce '0'.
- When Analog signal is between 2 V to 3 V, the comparators U1 and U2 produce output of '1' while output of U3 is '0'.
- When Analog signal is between 3 V to 4 V, all three of them produce a '1' output.
- These are then coded into a 2-bit Binary code by means of the EXOR-Diode combination.

**This principle is used in practical devices to convert Analog Signals into 8-bit, 16-bit, 32-bit or 64-bit Binary values, as required.**

## 2.

**Successive Approximation ADC****Fig. 41**

- At the beginning of the operation, both the SAR (Successive Approximation Register) and the 8-bit latch are reset to a '0' byte (Set of 8 zeros).
- At the first clock pulse, the SAR is set with a byte '**1 0 0 0 0 0 0 0**'. The 'Analog' corresponding to this is obtained by the DAC and it is 'Compared' with the instantaneous Analog Input. If the analog of the set byte is equal to the Analog Input, the byte is transferred to the 8-Bit Latch and to the output.
- If the **analog of the set byte were to be less than the Analog Input**, the SAR is '**decremented**' by resetting the MSB and setting it up at a byte '**0 1 0 0 0 0 0 0**'. The comparison of the Analog Input is done and the earlier step is repeated. This continues cycle by cycle of the Clock, till the byte set in the SAR equals the Instantaneous Analog Input.
- If, on the other hand, the **analog of the set byte was to be more than the Analog Input**, the SAR is '**incremented**' by setting it up at a byte '**1 1 0 0 0 0 0 0**'. The comparison of the Analog Input is done and the earlier step is repeated. This continues cycle by cycle of the Clock, till the byte set in the SAR equals the Instantaneous Analog Input.

### (3) NE 555 Timer IC and Applications

The 555 Timer IC is a very commonly used Hybrid IC, which is used in a number of applications. The conceptual block diagram is shown in the figure below.

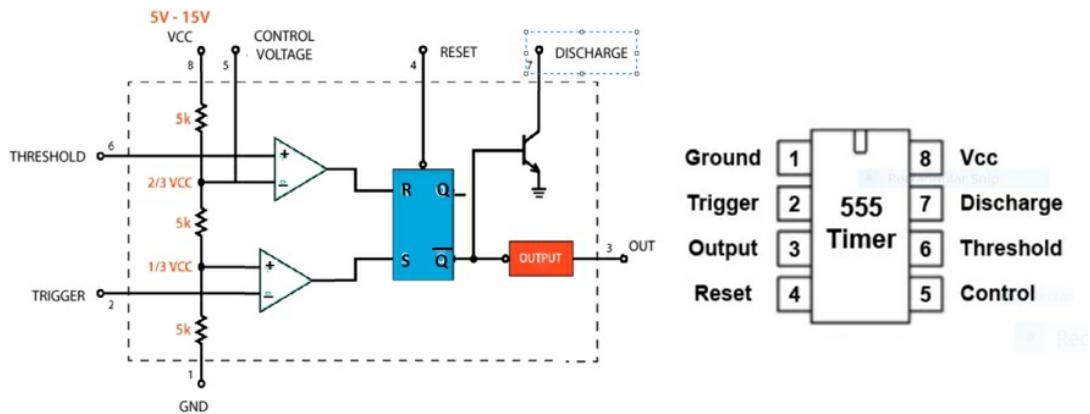


Fig. 42

#### FUNCTIONAL DESCRIPTION

1. Pin-1 is Ground, Pin-3 is the Output pin and Pin – 8 is V<sub>CC</sub>. The functions of the rest of the pins are as follows.
2. Pin – 2 TRIGGER. This compares 1/3 rd V<sub>CC</sub> with a negative, external ‘Trigger’ pulse. As soon as the trigger becomes more negative than 1/3 rd V<sub>CC</sub>, the comparator output is ‘1’. This ‘Sets’ the F/F, so that  $\bar{Q}$  is ‘0’ and the output buffer produces + V<sub>CC</sub> as the output voltage. This corresponds to a Logic ‘1’.
3. Pin – 4 RESET. A negative pulse at this point resets the IC irrespective of any other condition. When in active use for other operations, this pin is connected to V<sub>CC</sub>, at Pin – 8.
4. Pin – 5 CONTROL. The Threshold and Trigger levels are controlled by this pin. This pin is used to control the width of the output pulse. When not in use, this pin is by-passed to ground with a small capacitor.
5. Pin – 6 THRESHOLD. The Threshold voltage is compared with a reference of 2/3 rd V<sub>CC</sub>. As soon as the voltage at this point crosses this threshold, the Comparator-1 goes high. This resets the

**Q̄**

F/F and **Q̄** becomes ‘1’. This is reproduced as ‘0’ by the output buffer.

6. Pin – 7 DISCHARGE. This pin is used to reset the IC in between cycles of its operation. It is connected to Ground with the Timing Capacitor. When the base of this transistor is high, it saturates and this discharges the charge stored in the capacitor to ground through the transistor. When the base is low, the transistor is cutoff from ground and the capacitor charges up from  $V_{CC}$  through an external Resistor network.

## APPLICATIONS

Various applications can be designed with this common IC. Most of these are based on two basic configurations, namely,

- Monostable Configuration.
- Astable Configuration.

### (A) Monostable Configuration

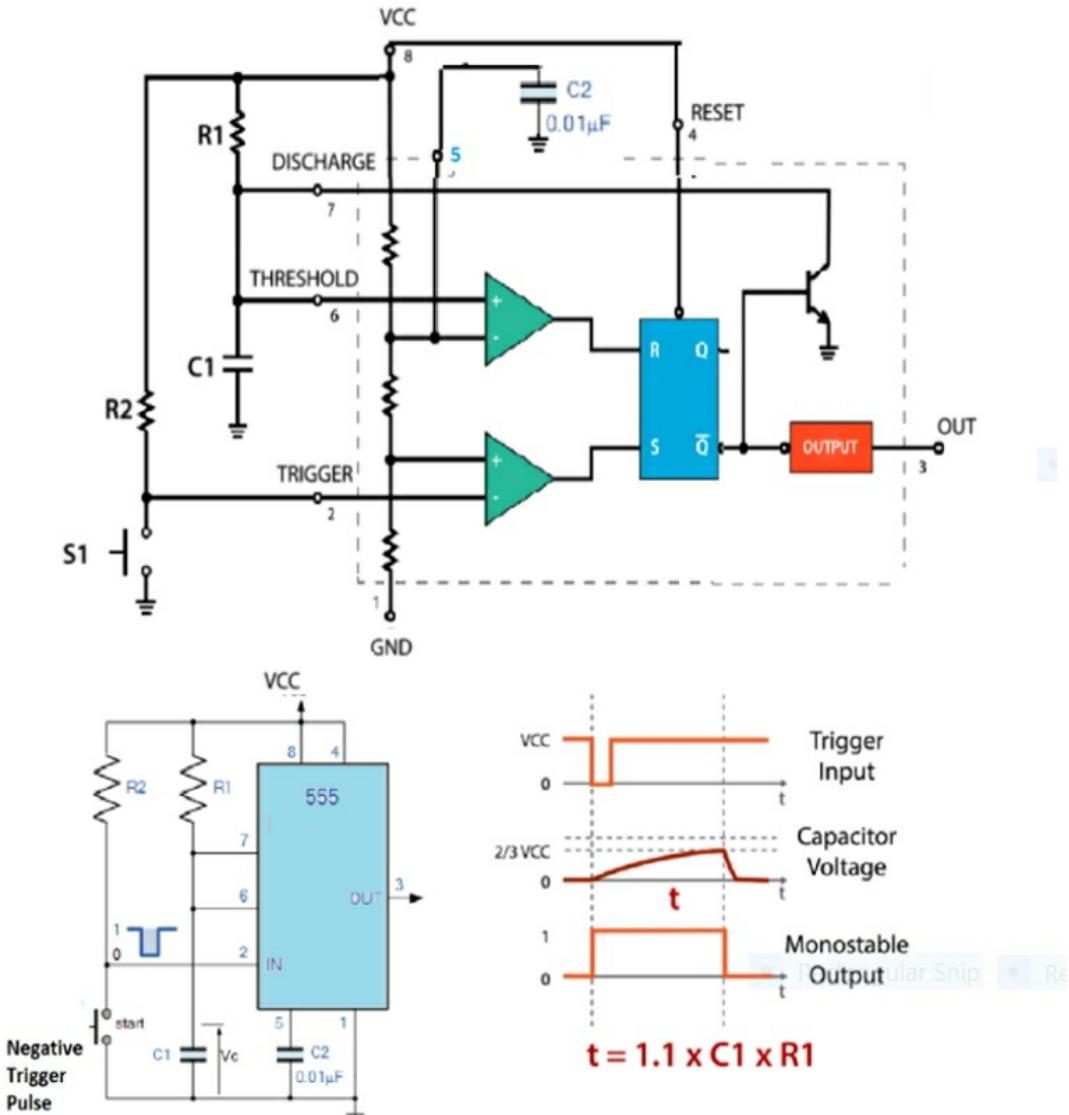


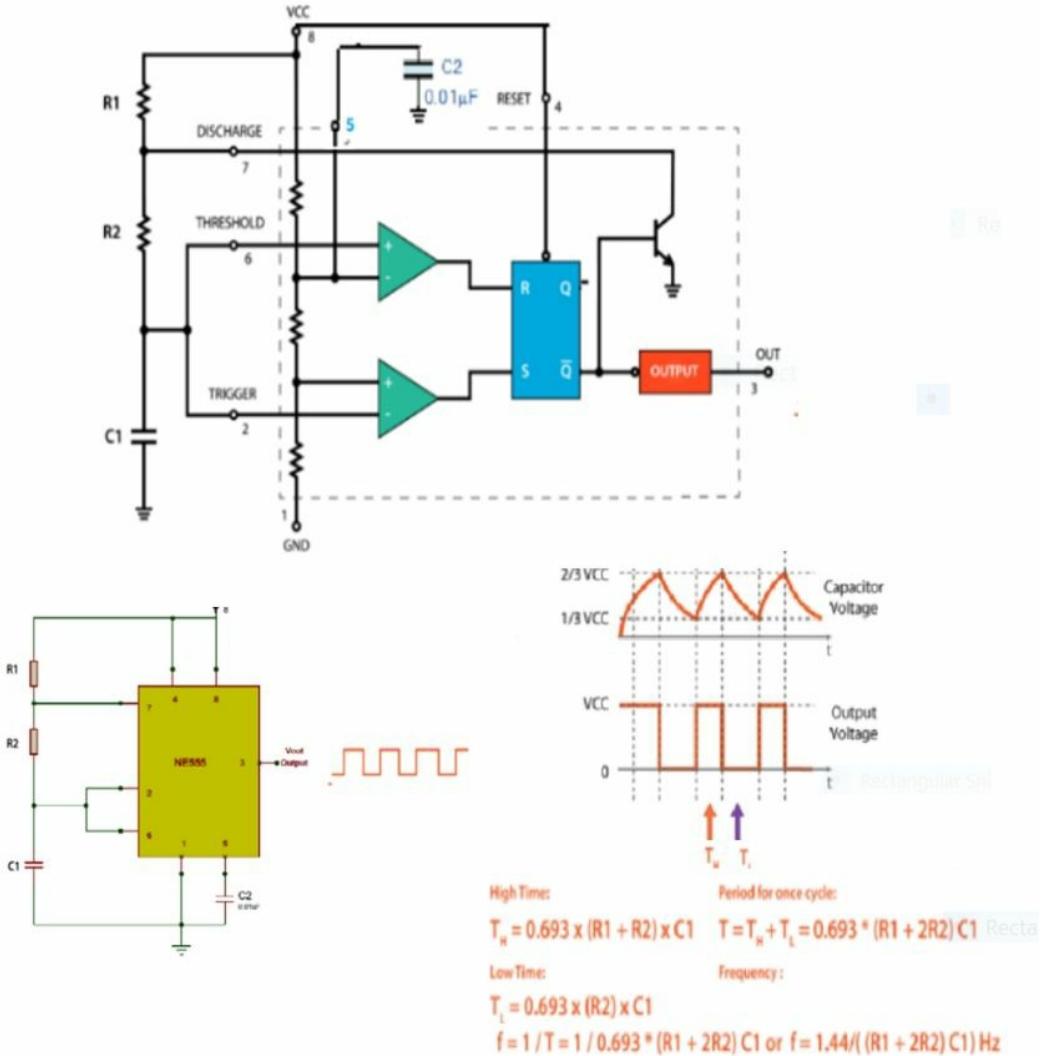
Fig. 43

- Assume that at the beginning, the device is ‘Reset’ so that output voltage and the voltage across the Timing Capacitor  $C_1$  is zero.
- As soon as the negative Trigger voltage is more than a negative DC of  $1/3$  rd  $V_{CC}$ , the comparator -2 ‘Sets’ the  $\bar{Q}$  output of the F/F at ‘0’. This is converted as logic ‘1’ or  $+V_{CC}$  by the output Buffer.
- A 0V at the base of the Discharge Transistor puts it in Cut-Off. Hence the capacitor charges up towards  $V_{CC}$ .

- As soon as voltage across capacitor crosses the threshold limit of  $2/3$  rd  $V_{CC}$ , Comparator -1 ‘sets’ the F/F at  $\overline{Q} = 1$ . At this instant, the output buffer makes the output logic ‘0’.
- A Logic ‘1’ at the transistor base saturates it and this discharges the Timing Capacitor.
- **This operation completes a cycle.**
- In this process, a narrow negative going Trigger Pulse is ‘Broadened’ and reproduced as a positive going pulse. The duration of the output pulse is given by the expression

$$t = 1.1 (R_1 C_1)$$

## (B) Astable Configuration



- Assume that, at the beginning, the output is at Logic '1' ( $+V_{CC}$ ). For this, the  $\bar{Q}$  of the F/F is at logic '0'.
- A 0V at the base of the Discharge Transistor cuts it off. Therefore, the Timing Capacitor C<sub>1</sub> is disconnected from ground. Consequently, it begins to charge up through the resistances, R<sub>1</sub> & R<sub>2</sub>. The output remains at Logic '1'. When the Capacitor C<sub>1</sub> charges up to 1/3<sup>rd</sup> V<sub>CC</sub>, the comparator-2 puts a logic '1' at R input of the F/F. This has the effect of keeping the output at '1'.
- As soon as the capacitor C<sub>1</sub> charges up to 2/3V<sub>CC</sub>, the comparator-1 produces a Logic '1' at the R input of the F/F. This

makes the  $\bar{Q}$  of the F/F is at logic '1'.

- The inversion by the output buffer makes the output '0'.
- The base of the Discharge transistor is high. Hence it goes into saturation. This will connect the Timing Capacitor to ground, and it will discharge through  $R_2$ .
- While discharging, as soon as the voltage across the capacitor becomes  $1/3V_{CC}$ , the comparator -2 is triggered and this makes the output to get back to Logic '0'.
- **This completes one cycle of operation.** The charging time corresponds to when the output is at logic 'High' ( $T_H$ ) and the discharging time correspond to the time when output is 'Low' ( $T_L$ ).
- These are calculated using the expressions as shown in the figure. From this we get the 'Periodicity' and Frequency of the output waveform.
- **Charging Time Constant is greater than the Discharging Time Constant.**
- Duty Cycle is defined as

$$\text{Duty Cycle} = \frac{T_H}{(T_H + T_L)} \%$$

#### (4) LM 565 PLL IC and Applications

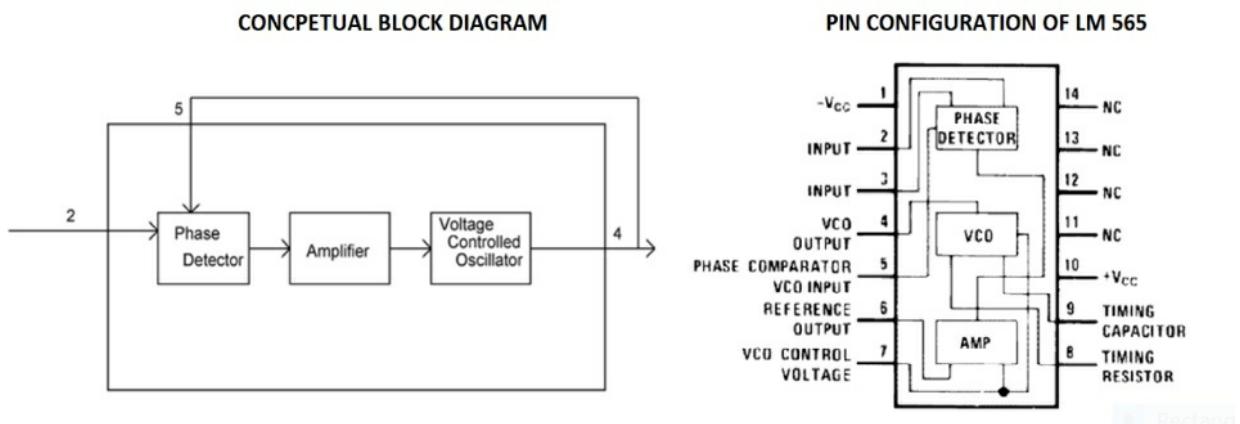


Fig. 45

- **PLL stands for “Phase Lock Loop”.** It is a Control System that generates a sinusoidal output signal whose instantaneous phase angle is compared with that of an incoming sinusoidal signal.
- The ‘Voltage Controlled Oscillator’ (VCO) generates this output signal and the ‘Phase Detector’ compares the phase angles of these two signals.
- The amplifier tracks the output signal at the ‘Difference Frequency’ and uses this to adjust the instantaneous phase angle of the VCO output signal so that it matches the frequency and phase of the incoming signal.
- One of the simplest implementations of this concept is the **IC LM 565**. This device is in widespread use in various applications, as enumerated below.
  1. FSK and FM demodulation
  2. Data synchronization
  3. Modems
  4. Frequency synthesizer
  5. Tone decoding
  6. Frequency multiplication and division
  7. Telemetry receivers
  8. Coherent demodulators

**&&&&&---OPAMP-OPAMP-OPAMP---&&&&&**

# PRACTICE PROBLEMS

## Chapter III

1. A FW Center Tapped Rectifier fitted with a Shunt Capacitor filter is to supply 24 V DC , with a rated load current of 200 mA at a maximum ripple voltage of  $\pm$  500 mV. Calculate the capacitance of the capacitor required to be fitted. Assume a AC supply frequency of 50 Hz. Calculate the specifications of the diodes required. Calculate the surge limiting resistance in this circuit (Assume  $I_{F(Surge)} = 10$  A).

(Ans :  $C = 3818 \mu F$  :  $V_R > 26$  V :  $R_s > 2.5 \Omega$ )

2. Repeat Problem 1 for a Bridge Rectifier.

3. Design a FW Bridge Rectifier to supply 18 V DC load , with a rated load current of 300 mA so as to limit the ripple voltage at  $\pm$  10 % of the rated load voltage. Calculate (i) the capacitance of the capacitor required, (ii) Specifications of the diodes (assuming Si diodes ), (iii) specifications of the transformer and (iv) value of the surge limiting resistance, assuming  $I_{F(Surge)} = 20$  A . Assume a AC supply frequency of 50 Hz.

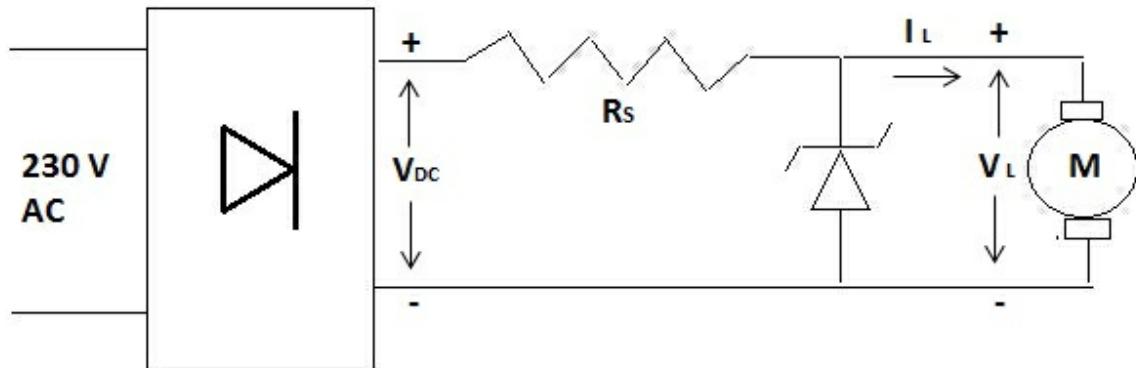
(Ans :  $C = 163 \mu F$  :  $V_R > 22$  V :  $R_s > 1.1 \Omega$ )

4. The output ripple of a single capacitor shunt filter in a rectifier, having  $C_1 = 200 \mu F$  is a 5 V peak-to-peak triangular voltage. The load is rated at 30 V, 120 mA. Calculate the output ripple when the filter is modified as a RC- $\pi$  filter by using a resistance  $R = 15 \Omega$  and another capacitor  $C_2 = C_1 = 200 \mu F$ .

(Ans :  $v_{0(r)} = 0.74$  V )

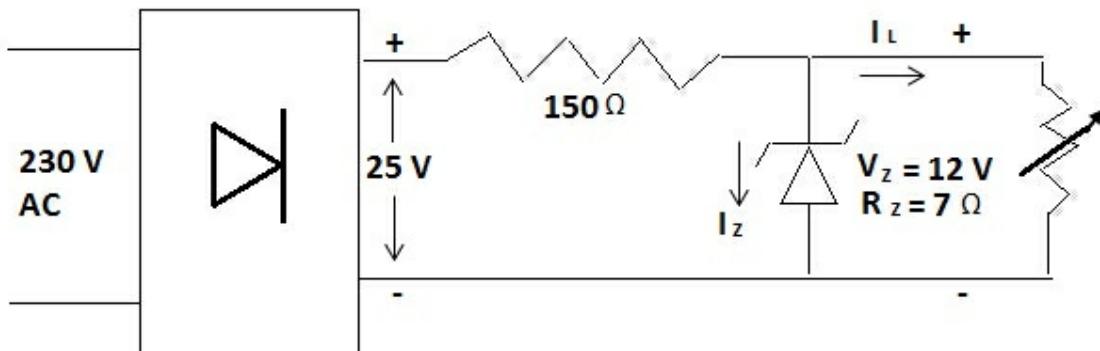
5. A Rectifier produces an unregulated DC output varying from 25

V to 20 V. This is to be regulated with a 15 V, 12 Ω Zener Diode to supply a DC motor rated at 100 mA. Calculate the value of the series resistance to be used in this circuit.



**(Ans :  $R_s = 50 \Omega$ )**

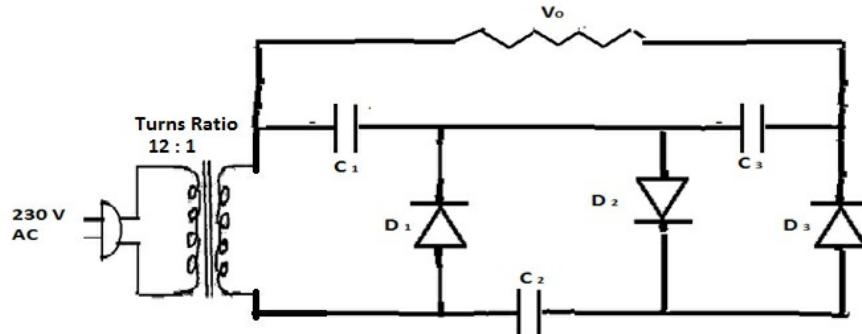
- Calculate the voltage regulation across the load in the circuit, when the load resistance varies from  $300 \Omega$  to  $1 M\Omega$ .



**(Ans :  $VR = 2.22 \%$ )**

## Chapter IV

- Calculate the output voltage of the Voltage Tripler circuit shown in figure.



(Ans :  $V_0 = 81.33 \text{ V}$ )

## Chapter V

1. The Base Current in a NPN transistor is  $25\mu\text{A}$ , while the Minority Carrier Current at the Collector-Base junction is  $10\mu\text{A}$  at the working temperature. The transistor has a value of  $\alpha = 0.98$ . Calculate the Collector Current and the Emitter Current of the device.

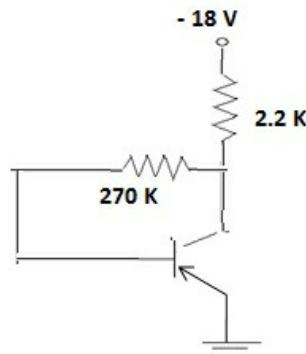
(Ans:  $I_C = 1.725 \text{ mA} :: I_E = 1.75 \text{ mA}$ )

2. In a PNP transistor, the measured values of the Base and Collector Currents were  $I_B =$

$200\mu\text{A}$  and  $I_C = 12.42 \text{ mA}$ . Calculate  $I_E$ ,  $\alpha$  and  $\beta$  of the device.

(Ans :  $I_E = 12.62 \text{ mA} : \alpha = 0.984 : \beta = 49.2$ )

3. Sketch the DC Load Line and calculate the Stability Factor of the Collector Feedback bias circuit shown in the figure. The circuit contains a Silicon transistor with  $\beta = 100$ .



(Ans :  $I_{C(SAT)} = 8.18 \text{ mA}$  (Sketch Load Line joining  $I_{C(SAT)}$  and  $V_{CC}$ )

:  $S = 55.86$  )

4. Sketch the DC Load line and locate the Q-Point of the Voltage-Divider biasing circuit of a Ge PNP transistor with the following component values :  $R_C = 2\text{ K}$ ,  $R_E = 1.5\text{ K}$ ,  $R_1 = 15\text{ K}$ ,  $R_2 = 2\text{ K}$ . Given Si transistor having  $\beta = 200$ , driven by  $V_{CC} = 12\text{ V}$ . Calculate the stability factor of the circuit.

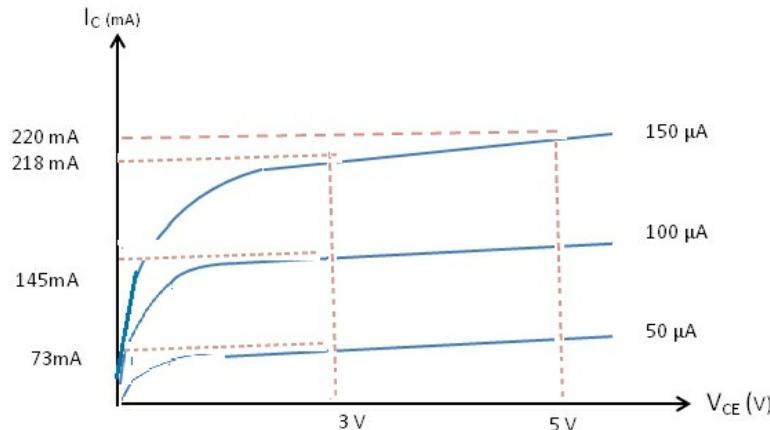
(Ans :  $I_{CQ} = 0.73\text{ mA}$  :  $V_{CEQ} = 9.43\text{ V}$  :  $S = 2.16$ )

5. Design a Voltage-Divider Biasing circuit for a Silicon NPN transistor having  $\beta = 100$ , so that it is able to drive a  $1\text{ K}$  Collector Load with a stability factor of  $S \leq 8$ . The transistor is to be biased by a DC battery of  $15\text{ V}$  at an operating point of  $V_{CEQ} = 5\text{ V}$ ;  $I_{CQ} = 5\text{ mA}$ .  
(Ans :  $R_E = 1\text{ K}$  :  $R_1 = 18.6\text{ K}$  :  $R_2 = 12.8\text{ K}$ )

6. Repeat the design for a Ge transistor having  $\beta = 150$ .

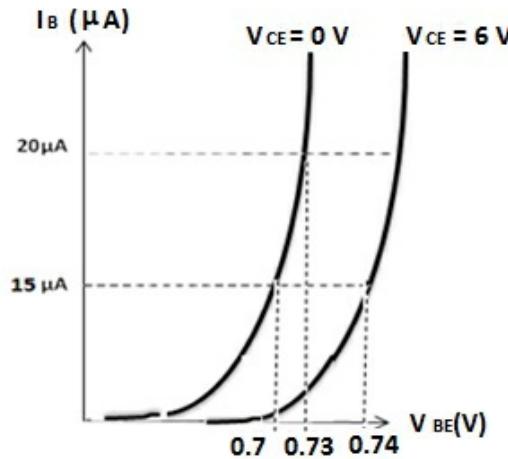
## Chapter VI

1. Calculate  $h_{fe}$  and  $h_{oe}$  from the output characteristics of a transistor shown in the figure. All the required data are available in the sketch.



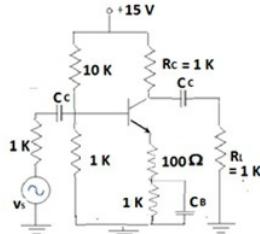
(Ans :  $h_{fe} = 1440$  :  $h_{oe} = 1 \times 10^{-3}\text{ mho}$  )

2. Calculate  $h_{ie}$  and  $h_{re}$  from the input characteristics of a transistor shown in the figure. All the required data are available in the sketch.



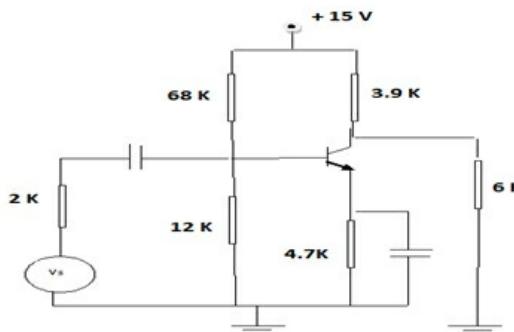
$$(\text{Ans : } h_{ie} = 6 \text{ K} : h_{re} = 6.67 \times 10^{-3})$$

3. Use the simplified h-parameter Model to analyze the performance of the amplifier given in the circuit. The relevant h-parameters of the transistor are  $h_{ie} = 1.1 \text{ K}$  and  $h_{fe} = 100$ .



$$(\text{Ans : } A_V = -4.46 : A_I = -7.5 : Z_{I(B)} = 11.2 \text{ K} : Z_{I(T)} = 841 \Omega)$$

4. Analyze the circuit shown in the figure below. Given,  $h_{ie} = 2.1 \text{ K} : h_{fe} = 75 : h_{re} = 3.4 \times 10^{-4} : h_{oe} = 10 \times 10^{-6} \text{ mho.}$



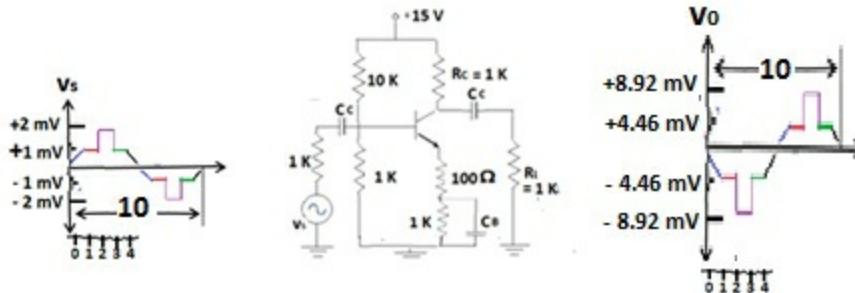
$$(\text{Ans : } A_V = -86.76 : A_I = -74.999 : Z_{I(B)} = 2.04 \text{ K} : Z_{I(T)} = 1.7 \text{ K} : A_{VS}$$

= 34.86 :

$$A_{IS} = -40.54 : G = 1615.9$$

5. Analyze the amplifier given in the circuit using r-parameter model and sketch the output voltage waveform. The circuit is made using a Si transistor with  $\beta = 100$ .

**Ans.**



$$(\text{Ans} : A_V = -4.46 : A_I = -7.5 : Z_{I(B)} = 11.2 \text{ K} : Z_{I(T)} = 841 \Omega)$$

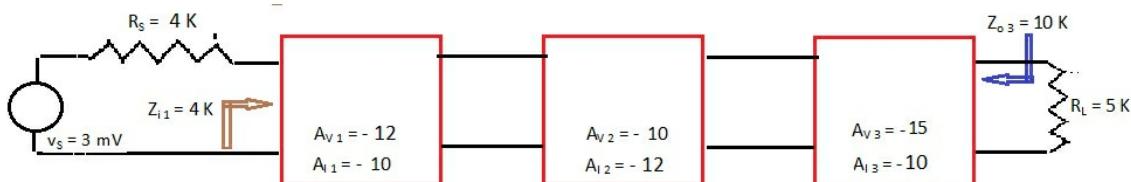
## Chapter VII

1. Calculate the Power gain of a 3 stage cascaded amplifier and express it in dB. Given  $A_{V1} = -15$ ,  $A_{I1} = -25$ ,  $A_{V2} = -30$ ,  $A_{I2} = -10$ ,  $A_{V3} = -20$  and  $A_{I3} = -25$ .

$$(\text{Ans.} : G = 5.625 \times 10^7 : G_{\text{dB}} = 77.5)$$

2. Calculate the Output Power, Input Impedance and Output Impedance of the Cascaded Amplifier. Express the Power Gain in dB.

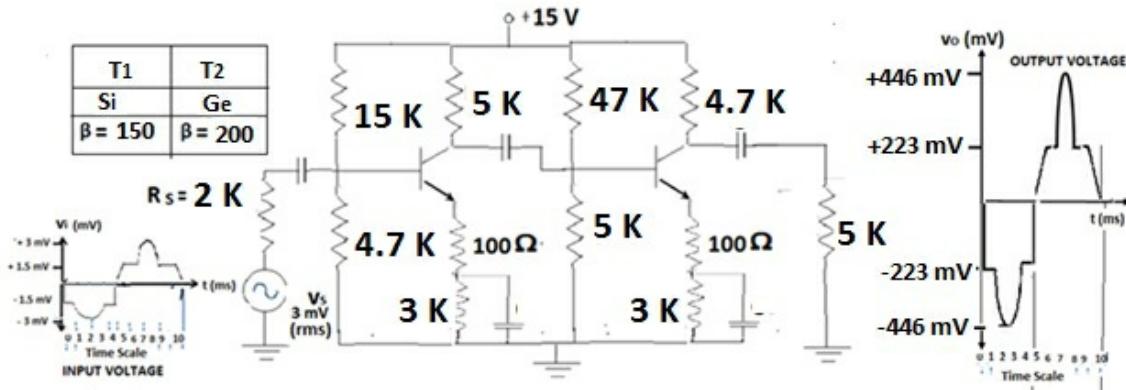
$$(\text{Ans.: } P_o = 202.5 \mu\text{W} : Z_I = 4 \text{ K} : Z_o = 10 \text{ K} : G = 5.4 \times 10^5 : G_{\text{dB}} = 57.52)$$



3. Evaluate the Output Voltage, Output Power and Output Voltage Waveform (use r-parameter analysis).

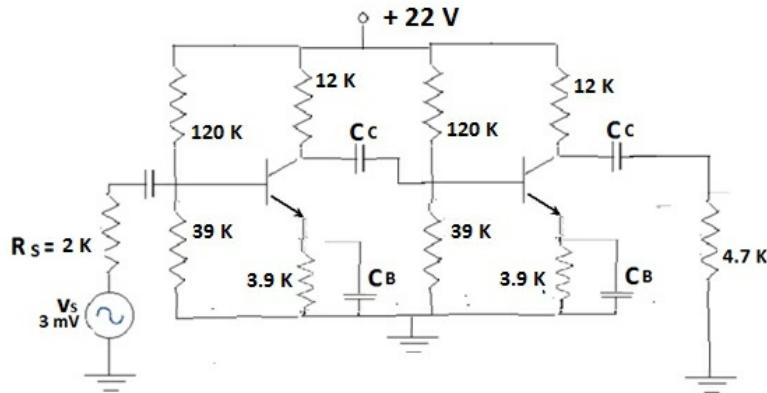
$$(\text{Ans. } V_o = 446 \text{ mV}_{(\text{rms})} : P_o = 39.8$$

$\mu\text{W}$ )

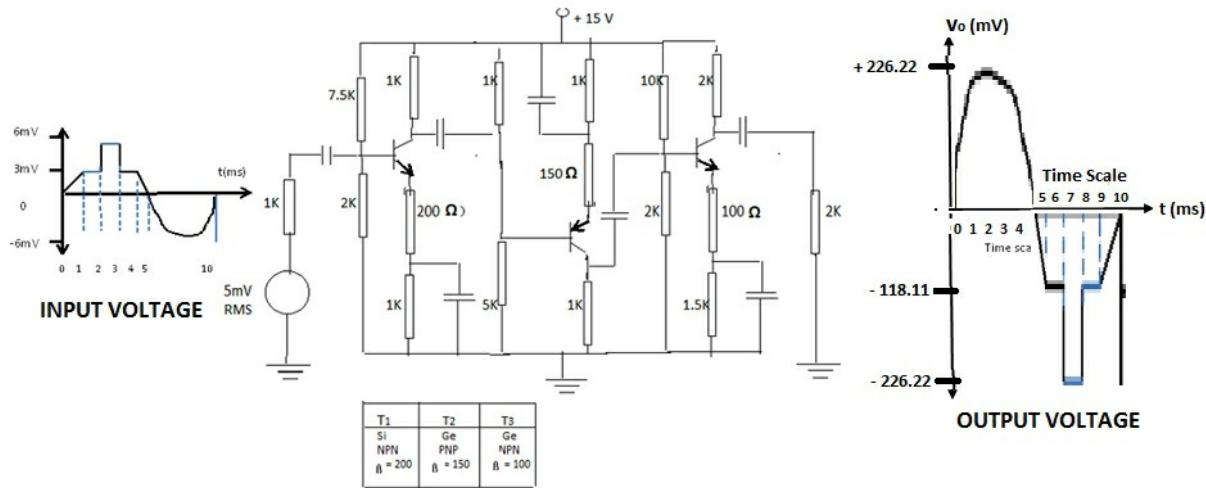


3. Analyze the amplifier in the circuit and calculate output voltage and output power. Assume identical Ge transistors with  $h_{ie} = 2 \text{ K}$  and  $h_{fe} = 100$ .

(Ans.  $V_O = 13.15 \text{ V}$  :  $P_O = 36.8 \text{ mW}$  )

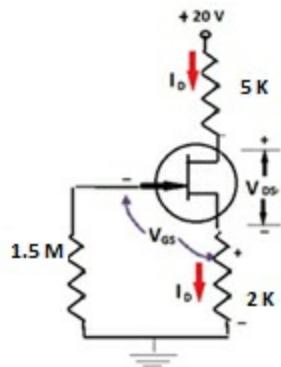


5. Using r-parameter analysis solve the following amplifier problem and justify the shape of the output waveform shown in the figure. Also calculate power delivered to the load. (Ans.  $P_O = 19 \mu\text{W}$ )

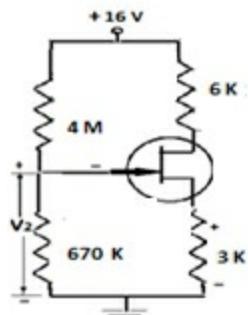


## Chapter VIII

1. Locate the Q Point of the Self Bias circuit in the figure and plot the DC Load Line. The parameters of the JFET are  $I_{DSS} = 14 \text{ mA}$  and  $V_P = 5 \text{ V}$

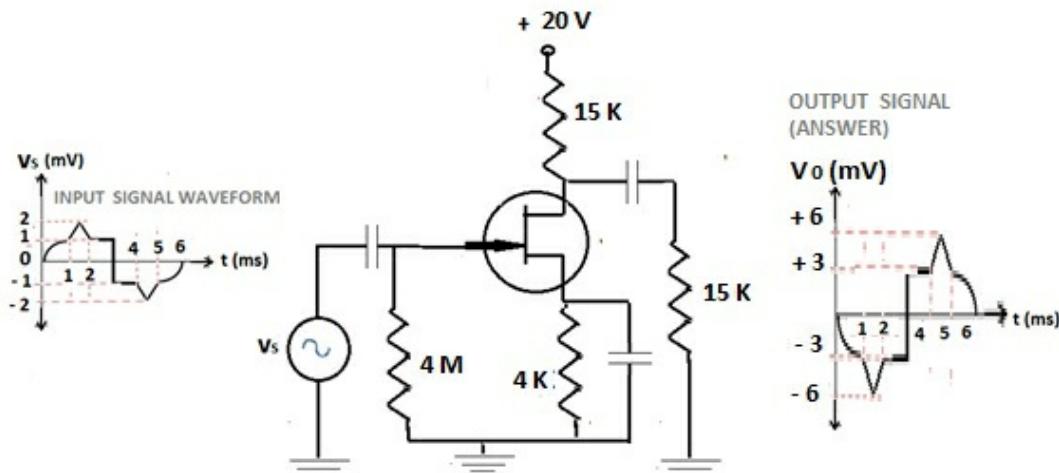


2. Locate the Q Point of the Voltage Divider Bias circuit in the figure and plot the DC Load Line. The parameters of the JFET are  $I_{DSS} = 12 \text{ mA}$  and  $V_P = 4 \text{ V}$



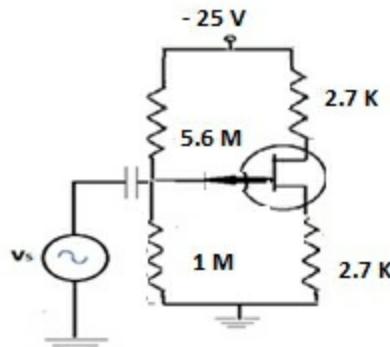
3.A P-Channel JFET has  $Y_{OS} = 36 \mu S$ ,  $|V_P| = 6 V$  and  $|I_{DSS}| = 8 mA$ . It is biased by a DC Bias of  $|V_{DD}| = 25 V$ , with a Voltage Divider Bias circuit with  $R_1 = 3.8 M\Omega$ ,  $R_2 = 1 M\Omega$ ,  $R_D = R_S = 2.5 K\Omega$ . Sketch the complete circuit and locate the Q-Point.

4.Analyze the JFET amplifier circuit shown in the figure below and calculate  $A_V$ ,  $Z_i$  and  $Z_o$ . Sketch the output voltage waveform, the input signal waveform is as shown in the figure. The JFET in the amplifier circuit has the following parameters ,  $I_{DSS} = 16 mA$  ;  $V_P = 4 V$  and  $Y_{OS} = 30 \mu S$ . **(Ans.:  $A_V = - 3 : Z_0 = 33.33 K : Z_I = 4 M$  )**



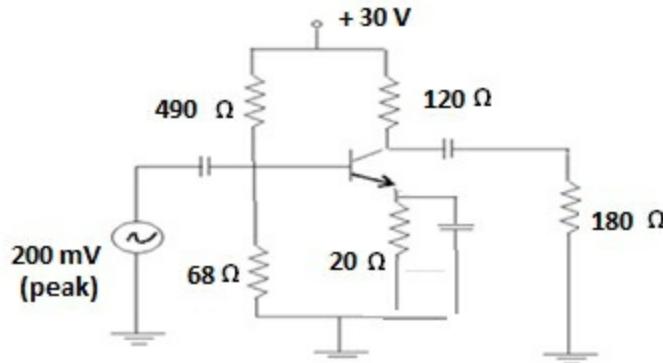
5.Analyze the CS amplifier shown in the circuit and calculate the voltage gain. The P-Channel JFET in the circuit has  $Y_{OS} = 40 \mu S$ ,  $V_P = 4 V$  and  $I_{DSS} = 8 mA$ .

**(Ans.  $A_V = - 5.11$  )**



## Chapter IX

1. Plot the AC and DC Load-Lines of the amplifier and calculate the output power and efficiency of the Class-A power amplifier shown in the circuit. Assume a silicon transistor with  $\beta=100$ .



2. In a Class-A transformer coupled power amplifier  $V_{CC} = 15$  V,  $R_1 = 3.9$  K,  $R_2 = 2.2$  K,  $R_E = 1.5$  K. The transformer used in the circuit has a primary coil with a resistance of  $33\ \Omega$  and turns ratio of 80 : 35 and has an efficiency of 78 %. The load resistance is  $100\ \Omega$ . Draw the AC and DC Load-Line and calculate the efficiency of the amplifier.

3. A Class-B amplifier has an output transformer with a turns ratio of 5 : 1, connected to a load resistance of  $8\ \Omega$ . The  $V_{CC}$  used in the circuit is 45 V. Calculate the maximum output voltage, Output Power and efficiency.

4. The open-loop gain of a BJT amplifier varies from 2240 to 1400 due to environmental variations. If the amplifier is fed back with a negative feedback path of gain  $B = 0.025$ , calculate the closed loop gain.

5. The open-loop input and output impedances of an amplifier are  $3.5$  K and  $300\ \Omega$  respectively. If voltage series negative feed back is applied with a feedback path having a gain of 0.03, calculate input and output impedances of the closed loop system.

6. If current series feedback system is used in an amplifier having open

loop input and output impedances of 4.2 K and 100 K respectively, calculate closed loop impedances at the input and output terminals assuming a feedback ratio of 0.035.

7. Repeat the calculation for voltage-shunt and current-shunt feedback systems for the amplifiers described in problem 2 and problem 3.

**xxxx-THE END-xxxx**

# About The Author

## **DEEPTARKA DEKA**

### **ABOUT THE BOOK**

The author, with 3 decades of teaching experience with Engineering Undergraduates feels that the average student is comfortable with a bit of Hand Holding in his foray into the world of Electronics. They tend to feel somewhat intimidated with the heavy dose of Physics and Math in most of the available Text Books. To this end, the author made it a practice to mail elaborate notes to his students at the end of each lesson. This book is essentially derived from these notes. Since the focus of the author has been the AICTE Model Curriculum, it is expected that this book will be highly useful as a Supplementary Text Book to the students in all Indian Universities. The aspirants of Competitive Exams and the working professionals as well as PG students too, can use this book as a refresher.

### **ABOUT THE AUTHOR**

The author is an alumnus of NIT Calicut and IIT Delhi. He has the experience of teaching this course for over three decades at Jorhat Engineering College and Assam Engineering College.