

# IPNC RDK Nand ECC for DM812x/DM385

## App Notes



Applicable to IPNC RDK Version  $\geq$  03.00

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## ***Revision History***

<b>Version</b>	<b>Date</b>	<b>Revision History</b>
0.1	June 18, 2012	Draft

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# 1. NAND ECC App Notes

## 1.1 Introduction

In LSP Version - 04.04.00.01, the default ECC scheme used across Uboot, Kernel and File System is changed to 8-bit BCH ECC.

UBIFS file system support has been enabled by default in the kernel.

IPNC RDK release version – 3.00 uses LSP - 04.04.00.01.

## 1.2 JFFS2 Vs BCH-8

Supporting BCH8 with JFFS2 is not possible because of shortage of OOB area.

- Total OOB Bytes - **64 Bytes** (for every 2048 bytes ( $512 * 4$ ))
- JFFS2 clean marker requires **8** bytes. Remaining OOB Bytes = **56 bytes** ( $64 - 8$ )
- ECC requires 14 bytes for every 512 bytes of data. Total ECC bytes = **56 Bytes** ( $14 * 4$ ).
- Remaining OOB Bytes = 0 byte ( $56 - 56$ )
- Manufactures bad block marking requires 2 bytes which is not available.

This shortage (-2) is the main reason is the issue with using JFFS2 + 8-Bit BCH ECC.

## 1.3 Solution for using JFFS2 with LSP - 04.04.00.01

We need to roll back to using 1Bit 1-bit HW HAMMING to use JFFS2.

U-Boot min still uses BCH-8.

U-Boot min should be still flashed using BCH-8 <nandecc hw 2>.

U-Boot, uImage, iffs2 image etc should be written after switching to 1-bit HW HAMMING CODE <nandecc hw 0>.

Kernel & Uboot should be patched to roll back to 1Bit Hamming code.

## 1.4 Patches to Apply

### 1.4.1 U-Boot Patching

- `cd u-boot-04.04.00.01`

- `patch -R -p1 < 0001-ti81xx-nand-make-default-ecc-scheme-as-BCH8.patch`
- Rebuild U-Boot images

### **U-Boot Patch**



0001-ti81xx-nand-make-default-ecc-sche

### **1.4.2 Kernel Patching**

- `cd linux-04.04.00.01`
- `patch -p1 < ti81xx_make_hamming_code_ecc_1.patch`
- `patch -p1 < ti81xx_make_hamming_code_ecc_2.patch`
- Rebuild kernel image

### **Kernel Patch**



ti81xx\_make\_hamming\_code\_ecc\_1.patcl



ti81xx\_make\_hamming\_code\_ecc\_2.patcl

## **1.5 Flashing Instructions**

### **1.5.1 U-Boot**

```
mw.b 0x81000000 0xFF 0x30000;nand erase 0x0 0x20000;tftp 0x81000000 u-boot.min.nand;nandeccl hw 2;nand write.i 0x81000000 0x0 0x20000;nandeccl hw 0
```

```
mw.b 0x81000000 0xFF 0x60000;nand erase 0x20000 0x60000;tftp 0x81000000 u-boot.bin;nandeccl hw 0;nand write.i 0x81000000 0x20000 0x60000
```

### **1.5.2 Kernel**

```
tftp 81000000 uImage;nand erase 0x00280000 0x00300000;nandeccl hw 0;nand write 0x81000000 0x00280000 0x00300000
```

### **1.5.3 FileSystem**

```
mw.b 0x81000000 0xFF 0x0C820000;tftp 0x81000000 jffs2_ipnc.bin;nand erase 0x006C0000 0x0C820000;nandeccl hw 0;nand write 0x81000000 0x006C0000 0x4000000
```

### **Note**

Boot arguments remain the same. Refer the Install Guide.

#### **1.5.4 Summary of Changes**

- Revert the patch that makes BCH8 as default ECC in the Uboot (so now the Uboot has 1bit ECC as default). Set the default ECC in kernel as 1-bit HW HAMMING (so that Uboot and Kernel ECCs are aligned).
- When in the Uboot, change the ECC scheme to BCH8 (using `'nandeccl hw 2'` command). Flash the uboot image on partition 0 (so that ROM code can read it correctly using BCH8 ECC).
- Use 1-bit HW ECC for other purposes (`'nandeccl hw 0'`).