

5

4

3

2

1

REV	Description	DATE	BY
C	1. Improved layout for the USB PHY. 2. Removed unused parts from the design. 3. Added current measurement function to the TWL4030. 4. Added filter caps to the VBUS rail input and output. 5.Changed U9 & U11 package to the QFN.	8/14/08	GC
C1	1. Added J12 and J13 to provide access to the RGB TTL signals on the LCD. 2. Added 5 filter caps. 3. Moved the USB Host port from Port1 to Port2. 4. Deleted R1. 5. Added 10K pulldown to USB reset signal. 6. Added 10K pulldown resistors as ID function to determine board type by reading these pins. 7. Added series resistor, R53, in the CLK line of the HSUSB clock line. May be removed after testing.	10/1/08	GC
C2	1. Moved the McBSP3_DX signal to pin AB26. 2. Moved the McBSP3_DR signal to pin AB25. 3. Moved the McBSP3_CLKX signal to pin AD25. 4. Changes were to allow access to three PWM signals from OMAP3530.	12/16/08	GC
C3	1. Added series resistor to BKBAT. 2. Added TP to BKBAT to allow access for battery. 3. Added a 47pf CAP and 3.3uH inductor to the S-Video feedback resistors.	2/11/2009	GC
C3A	1. Switched to TPS65950 based on the availability of the parts. 2. Made the battery an installed component. Removed parallel resistor.	4/21/2009	GC
C3B	1. Corrected J4 and J5 symbol for the RGB interface. No electrical changes were made. 2. Removed battery as an installed component due to availability issues.	4/30/2009	GC
C4	1. Added C141, 22uF in parallel with C97. 2. Added option to allow the USB PHY and CLKOUT to be powered from the VIO_1V8 rail or the VAUX2 rail from the TPS65950. Default is VIO_1V8 rail. 3. Changed 1.8V filter CAP on USB PHY to 22uF. 4. Made R113 a DNI and installed R112.	10/5/2009	GC
C4A	1. Made R67 an installed inductor and made R68 a DNI. Switched to LDO powered EHCI USB PHY.	11/5/2009	GC
C4B	1. Made R112 as a install and a value of 510 ohms. 2. Made R113 a DNI.	12/15/2009	GC
C4C	1. Changed R72 and R70 to 1.2K to match BOM. 2. Changed R71 and R73 to 1K to match BOM.	11/25/2010	GC
C5	No changes to design other than the use of a new POP memory device due to availability.	7/18/2011	GC

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Title

Beagle-Cover Page

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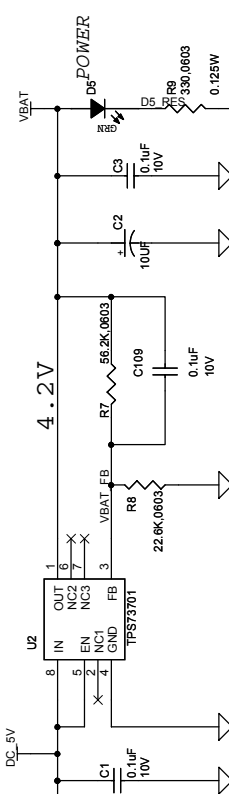
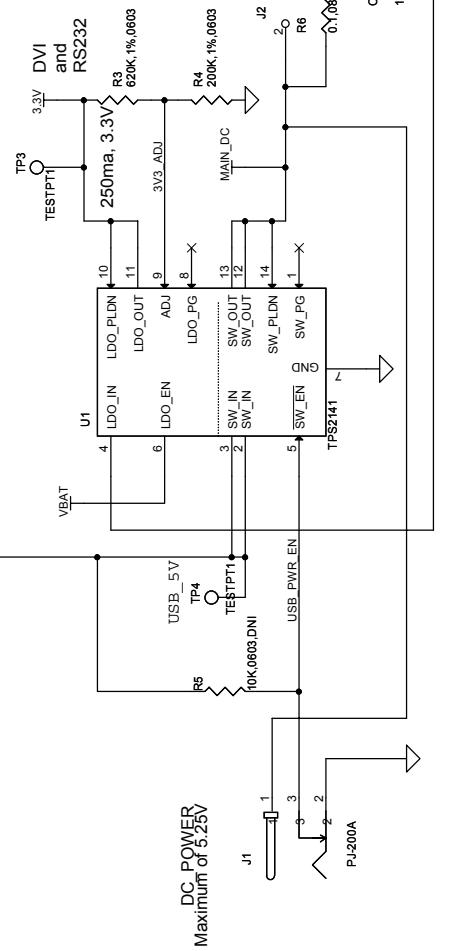
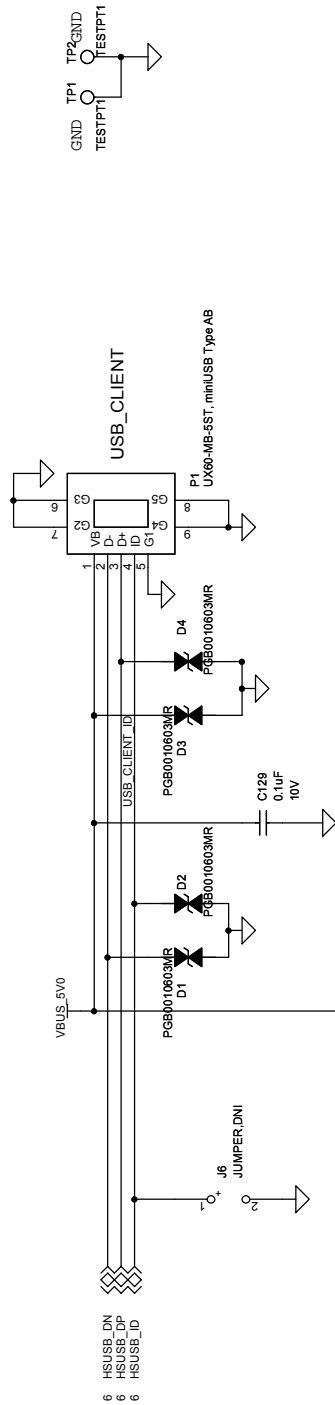
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6	TPS65950 1 of 2, AUDIO JACKS, LED, 26MHZ, 32KHZ
7	TPS65950 2 of 2, Power Rails
8	USB HOST AND EXPANSION
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10	DVI-D

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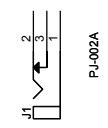
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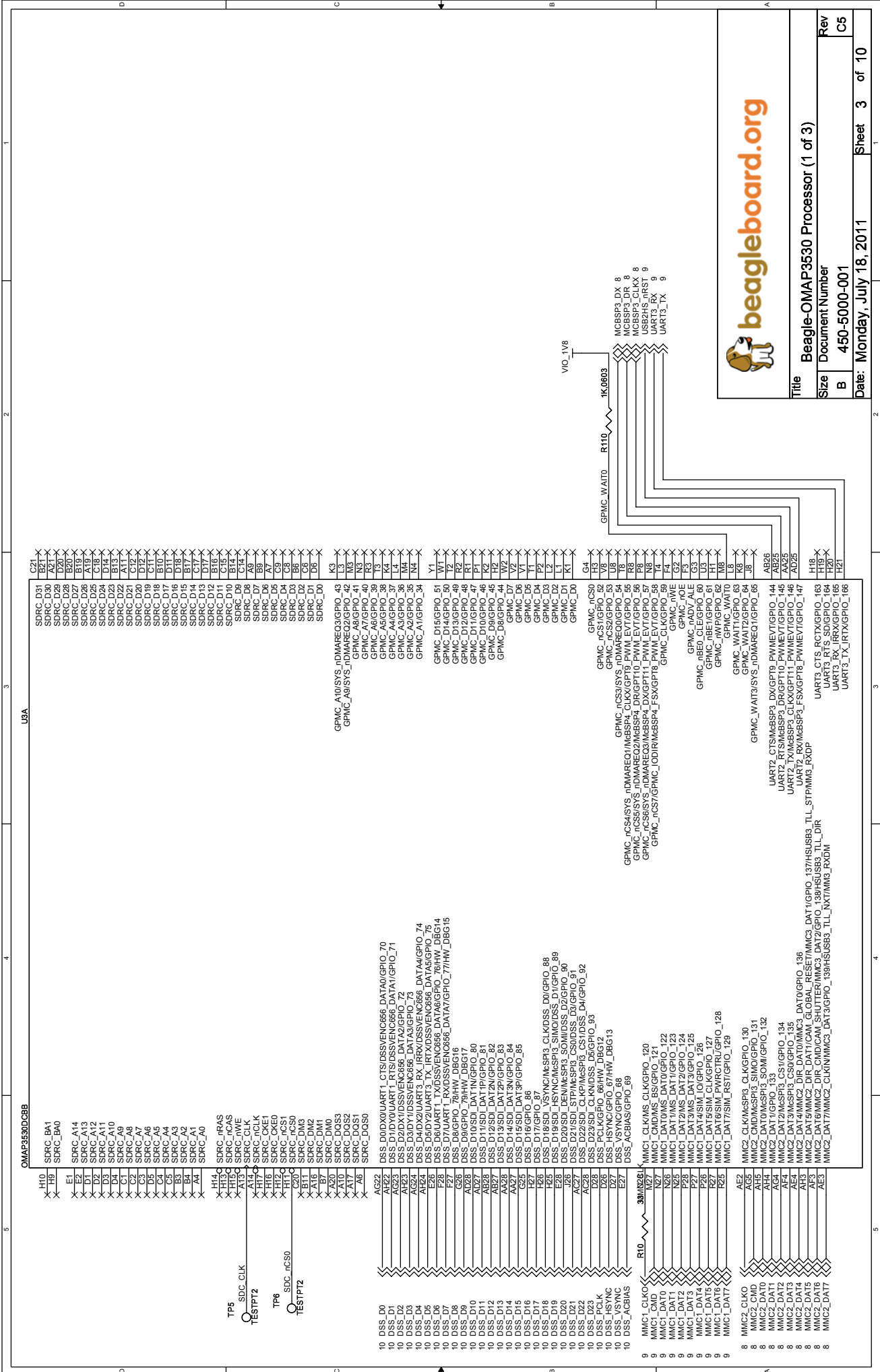
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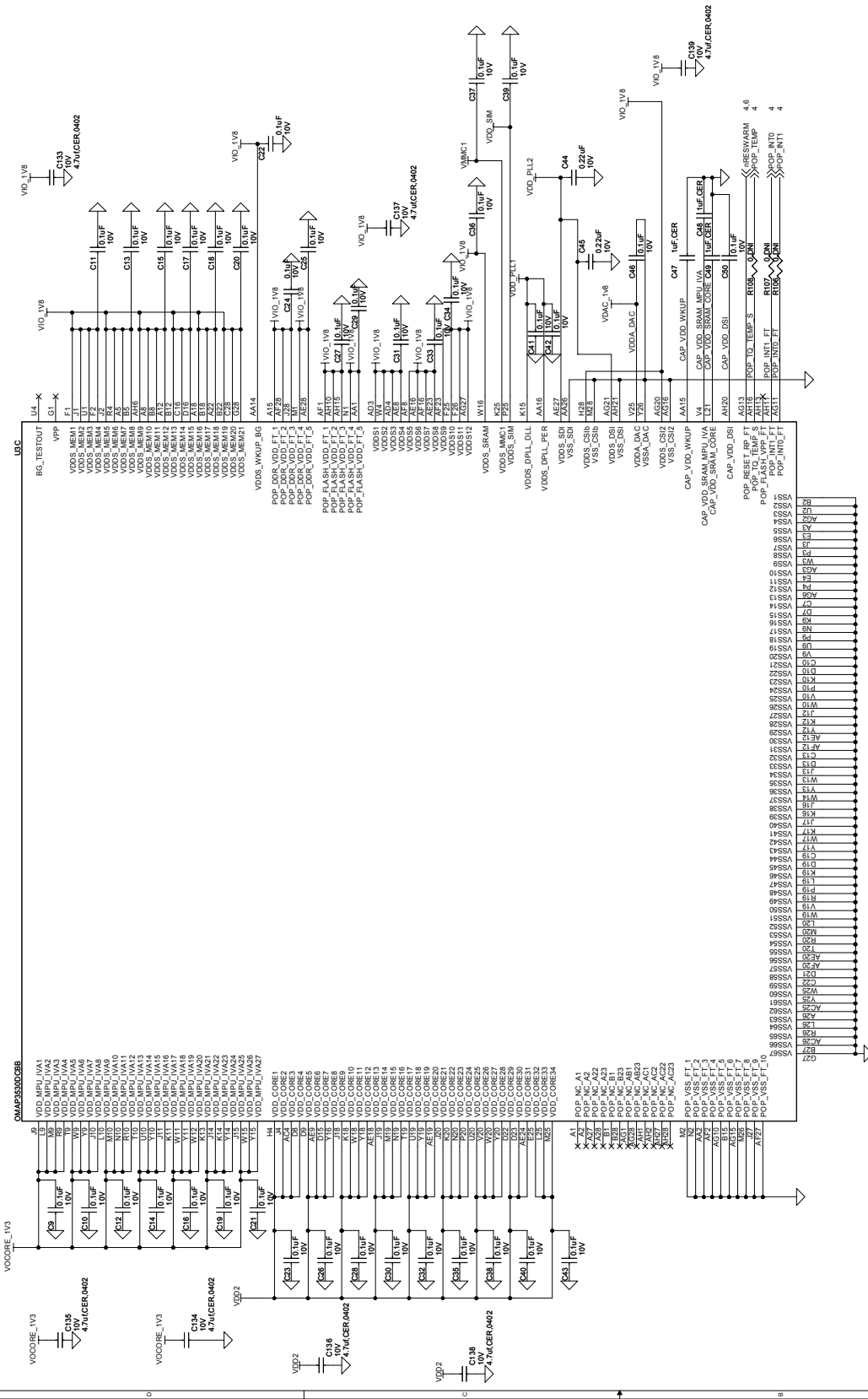


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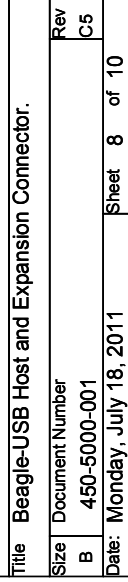
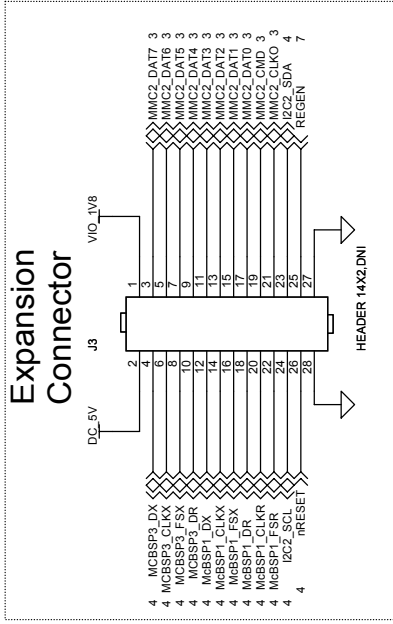


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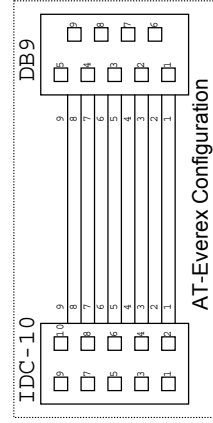
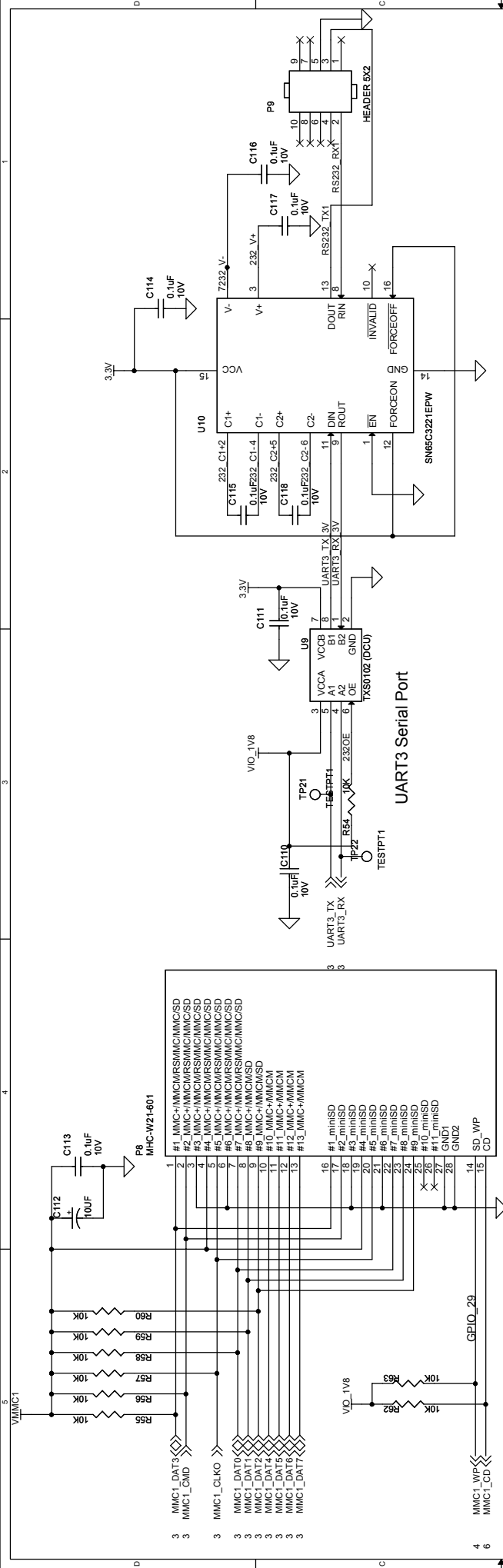
### Power



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24BIT MODE ONLY

REFER TO SECTION 15.2 OF THE  
OMAP3530 TECHNICAL REFERENCE MANUAL  
FOR OTHER MODES

BLUE

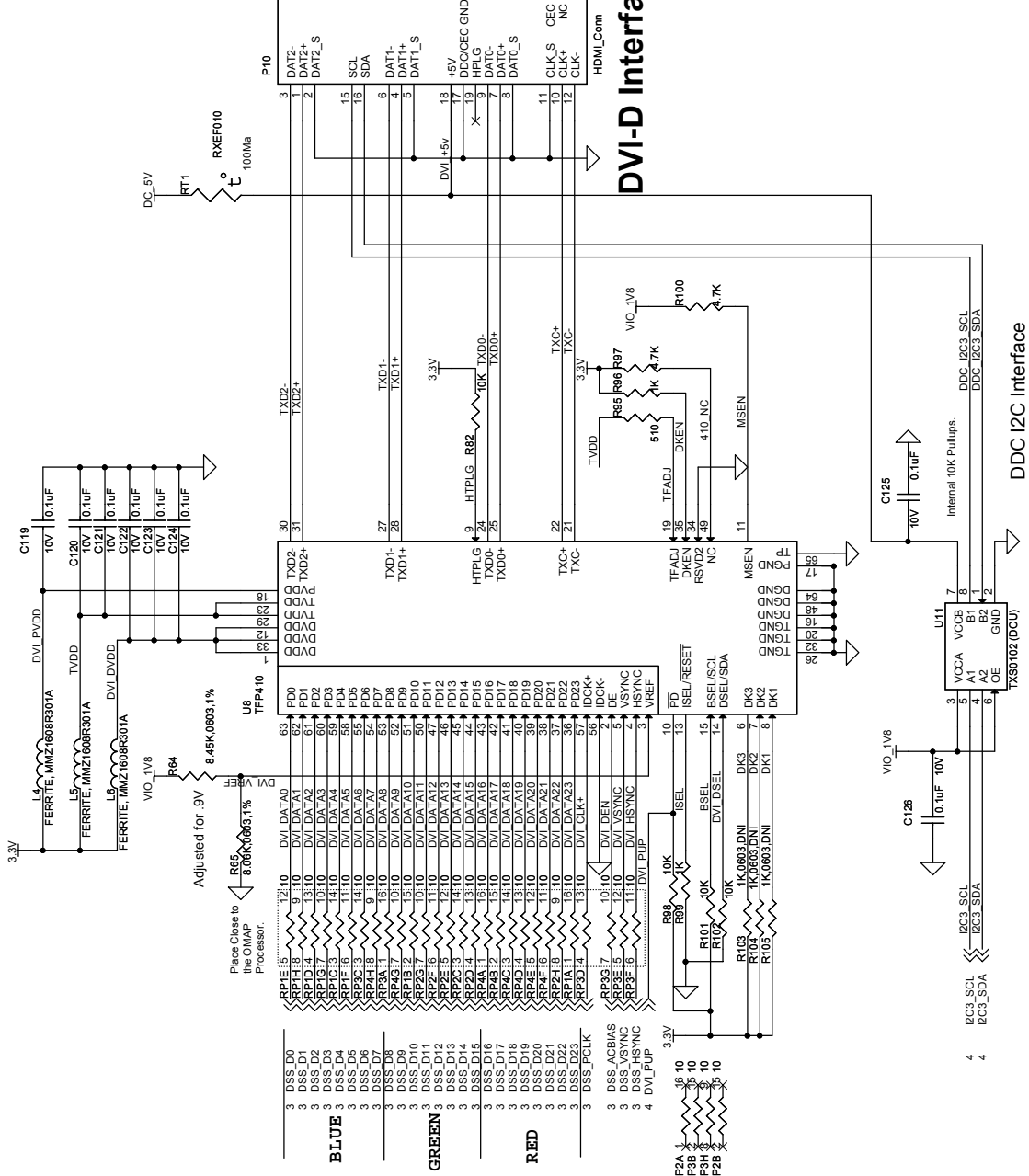
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3	DSS_D1
3	DSS_D2
3	DSS_D3
3	DSS_D4
3	DSS_D5
3	DSS_D6
3	DSS_D7
3	DSS_D8
3	DSS_D9
3	DSS_D10
3	DSS_D11
3	DSS_D12
3	DSS_D13
3	DSS_D14
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3	DSS_D18
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GREEN

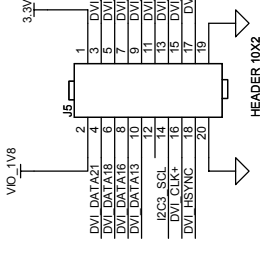
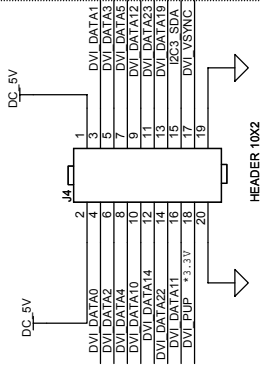
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3	DSS_G1
3	DSS_G2
3	DSS_G3
3	DSS_G4
3	DSS_G5
3	DSS_G6
3	DSS_G7
3	DSS_G8
3	DSS_G9
3	DSS_G10
3	DSS_G11
3	DSS_G12
3	DSS_G13
3	DSS_G14
3	DSS_G15
3	DSS_G16
3	DSS_G17
3	DSS_G18
3	DSS_G19
3	DSS_G20
3	DSS_G21
3	DSS_G22
3	DSS_G23
3	DSS_G24

RED

3	DSS_R0
3	DSS_R1
3	DSS_R2
3	DSS_R3
3	DSS_R4
3	DSS_R5
3	DSS_R6
3	DSS_R7
3	DSS_R8
3	DSS_R9
3	DSS_R10
3	DSS_R11
3	DSS_R12
3	DSS_R13
3	DSS_R14
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3	DSS_R19
3	DSS_R20
3	DSS_R21
3	DSS_R22
3	DSS_R23
3	DSS_R24



LCD RGB Interface



DVI-D Interface

DDC I2C Interface



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