Op Amp Design Project
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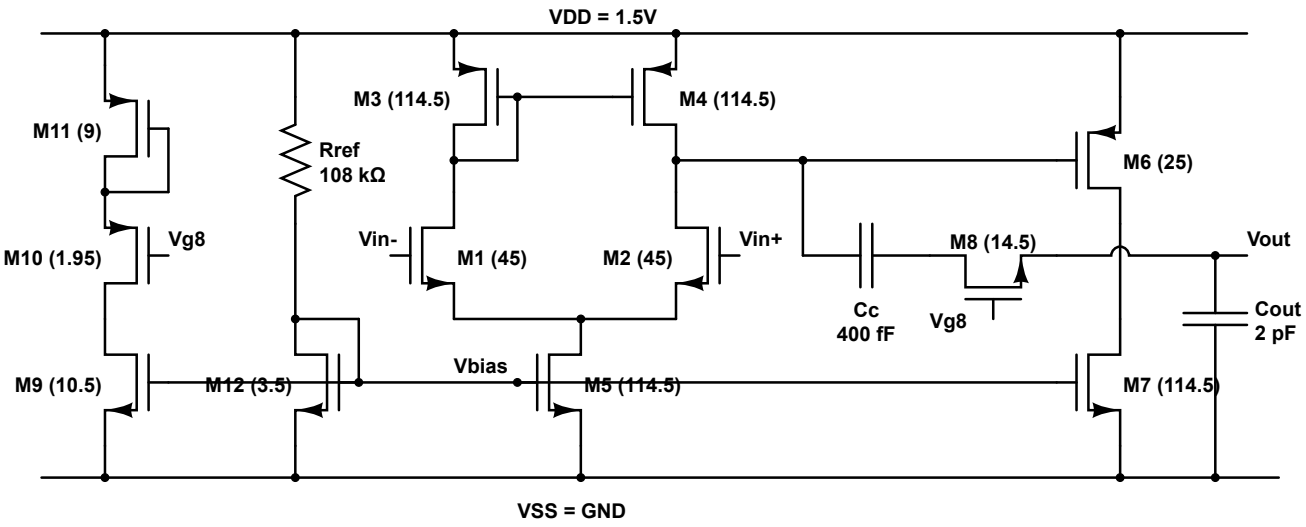
1 Overview



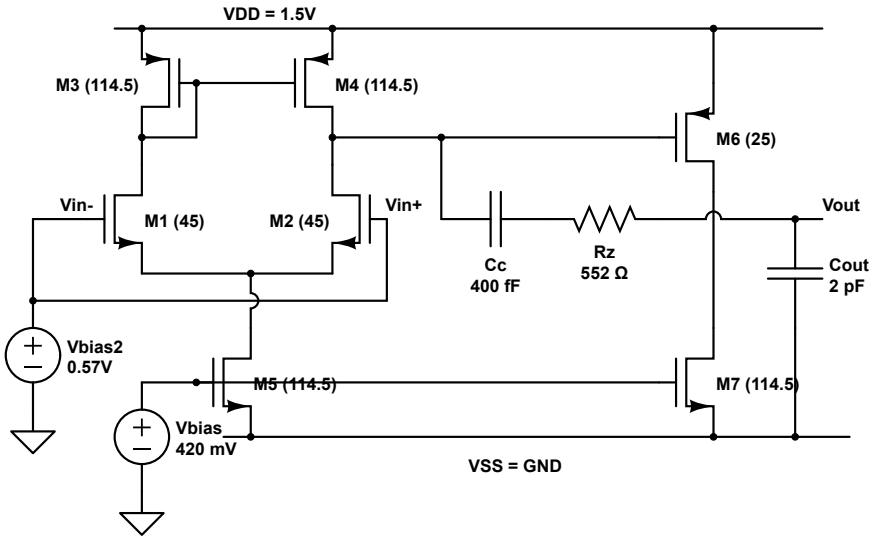
The op amp consists of two gain stages and two biasing branches.

- In the first biasing branch, Vbias is generated by a simple current source comprised of M12 and Rref.
- The first gain stage is the NMOS differential pair M1 and M2 loaded with a PMOS current source, M3 and M4. M5 sources the tail current for this stage and is biased by M12.
- The second gain stage consists of a PMOS common source amplifier M6 loaded by a current source M7 also biased by M12.
- A compensation capacitor and nulling resistor are added to the second gain stage to stabilize the op amp. M8, which acts as the nulling resistor, is biased via replica biasing by M10, which is itself biased by M9 and M11.

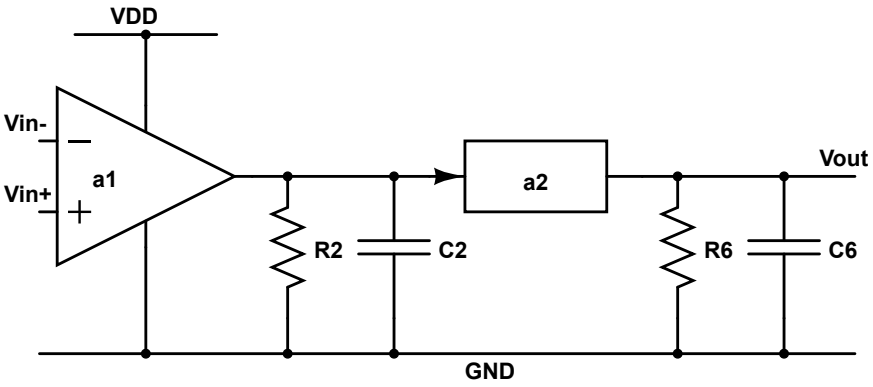
2 Design

2.1 Design Approach

To simplify the problem, we can take out the biasing branches and focus on the gain stages. The simplified circuit looks like this:



When thinking about the frequency response of the op amp, it will be helpful to simplify even further, and represent the circuit as two ideal amplifiers with all resistances and capacitances lumped together at two nodes.



Based on the specification, the following restrictions are placed on the design:

1. $Gain = gm_2(r_{o2}||r_{o4})gm_6(r_{o6}||r_{o7}) \geq 1500$
2. To design for an output swing within $0.15V$ of the rails, we require $Vov_6 = Vov_7 \leq 0.15V$. When we write the gain of the second stage, $a2$, as $gm6(r_{o6}||r_{o7}) = \frac{2I_{d6}}{Vov_6}\frac{1}{I_{d6}(\lambda_n+\lambda_p)}$, the current Id_6 drops out and we obtain $a2 \geq \frac{2}{Vov_6}\frac{1}{\lambda_n+\lambda_p}$. Plugging in values we have the restriction $a2 > 44$.
3. To ensure that the unity gain frequency w_{ult} is at least $600MHz$, we require that the product of the DC gain with the frequency of the first pole is at least $600MHz$ (this assumes our second pole will occur after w_{ult}). $w_{p1} = \frac{1}{gm_6R_2R_6C_c}$ combined with the gain equation reduces to $w_{ult} \leq \frac{gm_2}{C_c}$.
4. To meet the settling time spec, we use the approximation that $SlewRate = \frac{2V_0}{T_s}$. For $V_0 = 0.4V$ and $T_s = 8ns$ (to 0.1% of the final value), we obtain the restriction that $SlewRate \geq 100V/\mu s$. Since C_L is fairly large, we can guess that the slew rate will be limited by the second gain stage, so we can write $\frac{I_{d6}}{C_L} \geq 100V/\mu s$.

In this design, we ignore channel length modulation and the body effect for hand calculations to make the process simpler and more iterable. To start the design process, we choose a reasonable $\boldsymbol{C_c = 0.4pF}$. Choosing a conservative $w_{ult} = 800$MHz, from restriction #3 we get $gm_2 \geq 2mS$.
From #2 we know that $a2 \geq 44$, which implies $a1 \geq 35$ (design for 38).
Choosing $gm_2 = 2$mS and $a1 = 38$, and since $a1 = gm_2\frac{1}{I_{d2}(\lambda_n+\lambda_p)}$, we get $I_{d2} = 150\mu A$.
Solving $gm_2 = \sqrt{2k_nI_{d2}(\frac{W}{L})_2}$ gives $\boldsymbol{(\frac{W}{L})_2 = 40}$.

With the first stage designed, we guess a resonable value for the second stage bias current I_{d6}, design the second stage, check if specs are met, and iterate if necessary.
From #4, $I_{d6} \geq 200\mu A$. Choose $I_{d6} = 350\mu A$. Then because $a2 = 44 = \sqrt{2k_p(\frac{W}{L})_6I_{d6}}\frac{1}{I_{d6}(\lambda_n+\lambda_p)}$, we can solve for $\boldsymbol{(\frac{W}{L})_6 = 256}$.

Next we size M7 to meet the swing requirement.
$Vov_7 = \sqrt{\frac{2I_{d7}}{k_n(\frac{W}{L})_7}} = 0.13V -> \boldsymbol{(\frac{W}{L})_7 = 108}$.
M5 is sized proportionally to M7. Because they share the same V_{gs}, $(\frac{W}{L})_5 = I_{d5}\frac{(\frac{W}{L})_7}{I_{d7}}$. So $\boldsymbol{(\frac{W}{L})_5 = 95}$.
Size M3 and M4 for Vov = 0.13V to accomodate input swing spec.
$Vov_4 = \sqrt{\frac{2I_{d4}}{k_n(\frac{W}{L})_4}} = 0.13- > \boldsymbol{(\frac{W}{L})_4 = 110}$.

We are now able to fill in values for $R2$, $R6$, $C2$, and $C6$ in the system diagram.
$R2 = r_{02}||r_{04} = 19.0k\Omega$
$R6 = r_{06}||r_{07} = 9.52k\Omega$
$C2 = C_{gd4} + C_{gd2} + C_{gd6} = 17.6fF.(C_{gd} = L_{diff}C_{ox}W)$
$C6 = C_{out} + C_{db6} + C_{db7} \approx C_{out} = 2pF$

At this point, we can calculate the pole frequencies.

$f_{p1} = \frac{1}{2\pi} \frac{1}{gm_6 R_2 R_6 C_c} = 492kHz$
$f_{p2} = \frac{1}{2\pi} \frac{gm_6 C_c}{C_2 C_6 + C_c(C_2+C_6)} = 338MHz$

Since the second pole is below 600MHz, we have two options. First, we can try to move the second pole up by increasing gm_6 by increasing Id_6 ($(\frac{W}{L})_6$ must remain constant else the parasitic capacitance $C2$ will incerase and push the second pole down). However, a better solution that requires much less power is to cancel the second pole with the zero created by the nulling resistor R_z.

To cancel the second pole, we need $f_{p2} = f_{z1}$.
$\frac{gm_6 C_c}{C_2 C_6 + C_c(C_2+C_6)} = \frac{1}{C_c(\frac{1}{gm_6} - R_z)}$
Solving and plugging in values, $R_z = 552\Omega$.

Now, we have to size M8 and its biasing branch to achieve this value for R_z. The idea is to make M10 a replica of M8. To achieve this, we need $Vgs_{11} = Vgs_6$. Assuming equal Vt, $Vov_{11} = Vov_6$. Plugging in the Vov equation, this relation simplifies to $(\frac{W}{L})_{11} = (\frac{W}{L})_6 \frac{I_{d10}}{I_{d6}}$. We pick $I_{d10} = 30\mu A$, which gives $\mathbf{(\frac{W}{L})_{11} = 25.6}$. We also need $Vgs_{10} = Vgs_8$ which again implies $Vov_{10} = Vov_8$. Plugging the expression for Vov_8 into the equation for on-resistance of a MOS in triode region, we have $Rz = \frac{1}{k_n(\frac{W}{L})_8 \sqrt{\frac{2I_{d10}}{k_n(\frac{W}{L})_{10}}}}$. From this equation we can see that the sizes of M8 and M10 are proportional, so to minimize the size of M8 we pick a small $\mathbf{(\frac{W}{L})_{10} = 3 -> (\frac{W}{L})_8 = 22}$.

Finally, we size M12 and R_{ref} to generate the correct Vbias for M5, M7, and M9. Choose $I_{d12} = 10\mu A$. Because M12 and M5 share the same V_{gs}, $(\frac{W}{L})_{12} = I_{d12} \frac{(\frac{W}{L})_5}{I_{d5}}$. So $\mathbf{(\frac{W}{L})_{12} = 3.6}$.

2.2 Modifications

1. The transistor dimensions derived with respect to L_{eff}, so they will differ from the $(\frac{W}{L})$ ratios given later that are with respect to L. The dimensions were also modified slightly from the design above to achieve the correct bias points in SPICE and to conform to the lambda design rule. The final dimensions are in the Transistor and Biasing Summary section.

2. In order to decrease A_{cm} to meet spec, we increased r_{o5} by doubling the length of M5. To maintain the same drain current (and thus the same $(\frac{W}{L})$ ratio) the width had to be increased as well.

3 Transistor and Bias Summary

$Transistor$	$Length$	$Width$	(W/L)	$Ibias$	Vgs	gm	gds
M1	130n	5.85u	45	157uA	.426V	2.9mS	33.6u
M2	130n	5.85u	45	157uA	.426V	2.9mS	33.6u
M3	130n	14.885u	114.5	157uA	.416V	2.7mS	24.9u
M4	130n	14.885u	114.5	157uA	.416V	2.7mS	24.9u
M5	260n	39.06u	114.5	314uA	.405V	6.0mS	38.5u
M6	130n	32.5u	25	344uA	.411V	6.2mS	59.1u
M7	130n	14.885u	114.5	344uA	.405V	6.5mS	78.7u
M8	130n	1.885u	14.5	0uA	.838V	0mS	1.5u
M9	130n	1.365u	10.5	30uA	.405V	.56mS	6.2u
M10	130n	.195u	1.95	30uA	.771V	.14mS	5.0u
M11	130n	1.17u	9	30uA	.477V	.33mS	4.8u
M12	130n	.455u	3.5	10uA	.405V	.19mS	2.2u

4 Performance

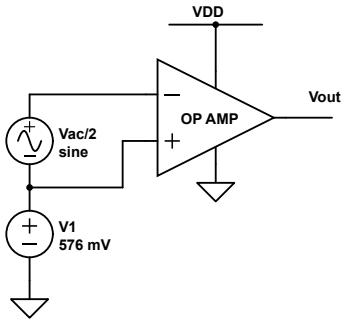
Parameter	***Spec***	***Design***
Gain	≥ 1500	2239
Unity Gain Bandwidth	$\geq$ 600MHz	669MHz
Common Mode Input Range	$\geq$ 0.8V	1.45V
Output Swing	$\geq$ 1.2V	1.43V
CMRR at DC	$\geq 75db$	78.2db
PSRR at DC	$\geq 60db$	75.0db
PSRR at 1MHz	$\geq 50db$	68.6db
Settling Time to within 0.1% of final value	$\leq$ 8ns	2.2ns (up), 6.4ns (down)
Power Dissipation	$\leq$ 1.5mW	1.05mW

5 Discussion

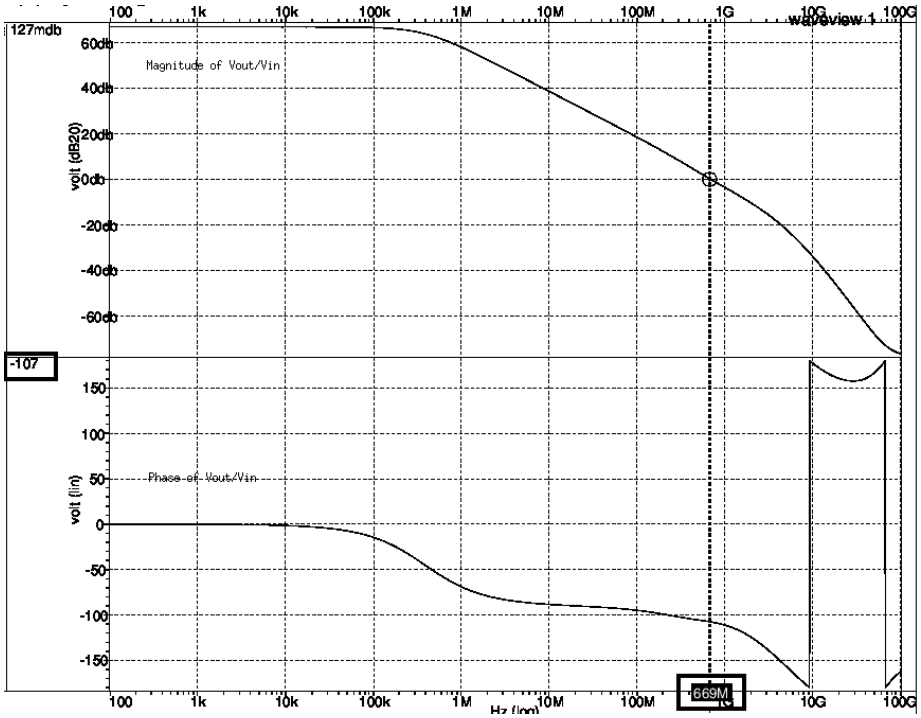
5.1 Gain, Bandwidth, and Phase Margin

Calculate
$Gain = gm_2(r_{o2}||r_{o4})gm_6(r_{o6}||r_{o7}) = 1995$.
Assuming the $w_{ult} = 800$MHz we designed for and that the second pole is exactly canceled by the zero, $PM = 180° - \arctan\frac{w_{ult}}{w_{p1}} + \arctan\frac{w_{ult}}{w_{p3}} = 85°$.

Measure
To determine the gain at low frequencies and the unity gain frequency, we apply a differential sinusoidal signal Vac to the input of the op amp.



The resulting Bode magnitude and phase plots are shown below. From the plot we can see that the gain is 67db (about 2239), the unity gain bandwidth is 669MHz, and the phase margin is about 73°. The phase margin is lower than estimated because the zero did not end up exactly on top of the second pole in the SPICE simulation.



5.2 Common Mode Input Range

Calculate

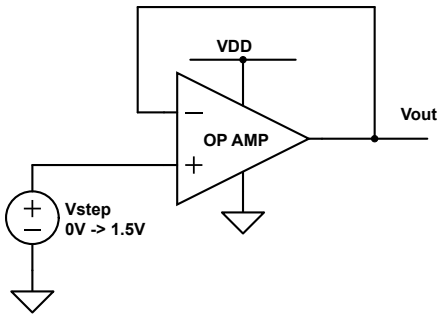
The lower bound on the common mode input range is determined by the input voltage that puts M5 out of saturation. $Vcm_{low} = Vov_5 + Vgs_2 = 0.55\text{V}$

The upper bound is determined by the input voltage that puts M6 out of saturation. $Vcm_{high} = VDD - Vov_6 = 1.36\text{V}$

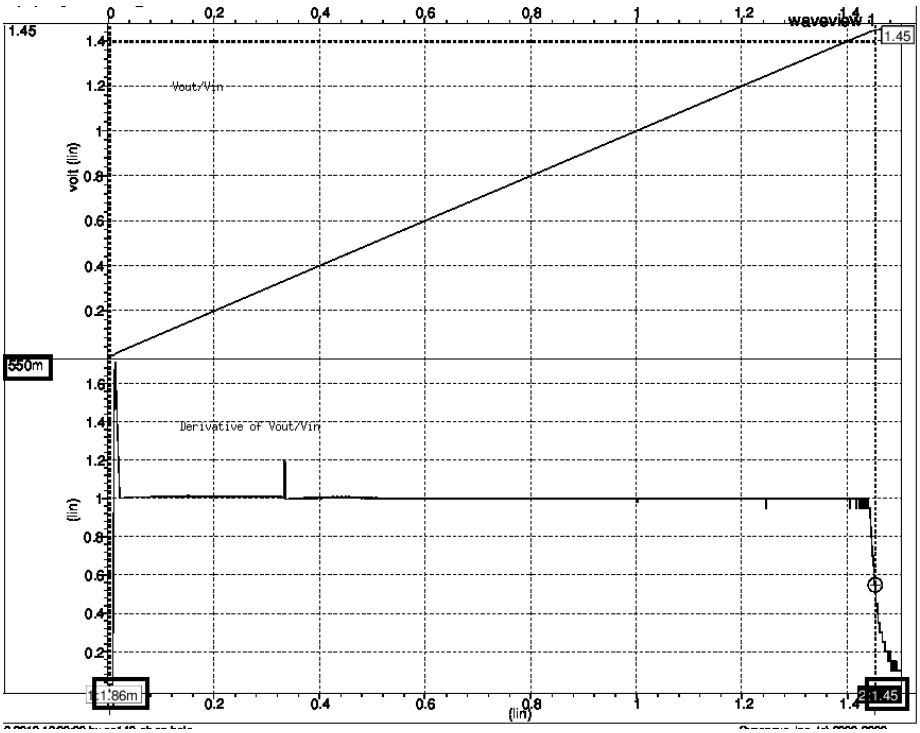
$Vcm_{range} = 0.81\text{V}$

Measure

To measure the common mode input range, we first put the op amp into unity gain feedback (short the output to the negative input terminal). Then we sweep the other input from 0 to VDD, and take the derivative of the output voltage.



Input range is defined as the DC input voltages for which dV_{out}/dV_{in} becomes 1/2. From the plot below, the common mode input range is 1.45V. This value is higher than the estimated swing because even when the transistors go out of saturation, they still provide more than 1/10 the nominal gain.



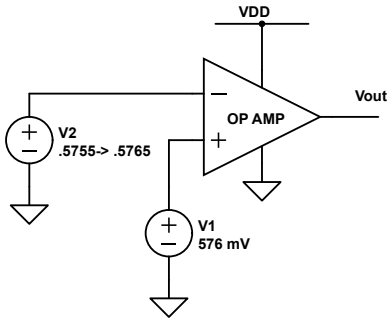
5.3 Output Swing

Calculate

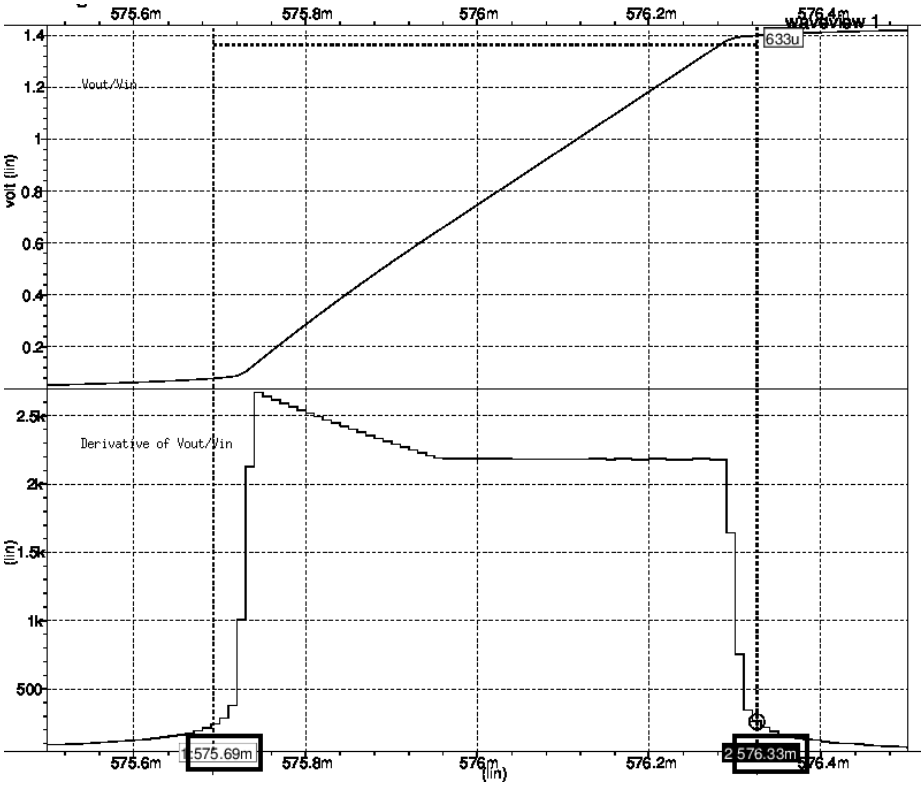
The lower bound on the output swing is determined by the output voltage that puts M7 out of saturation. $Vout_{low} = Vov_7 = 0.13$V.
The upper bound is determined by when M6 goes out of saturation. $Vout_{high} = VDD - Vov_6 = 1.37$V.
$Vout_{swing} = 1.24$V.

Measure

To measure the output swing of the op amp, we hold one of the inputs steady and sweep the other input around its bias point.



Output swing range is defined as the range of DC output voltages for which dV_{out}/dV_{in} becomes 1/10 the nominal differential gain. On the plot below, the input range for $dV_{out}/dV_{in} = \frac{1}{10}2239 = 223.9$ is 576.33mV - 575.69mV. Looking at the corresponding values for Vout, we have $V_{swing(out)} = 1.385V$.



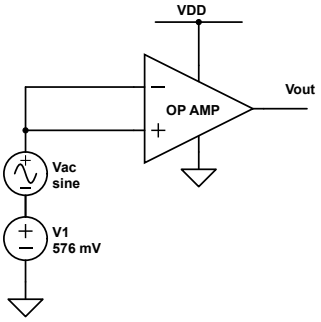
5.4 CMRR

Calculate

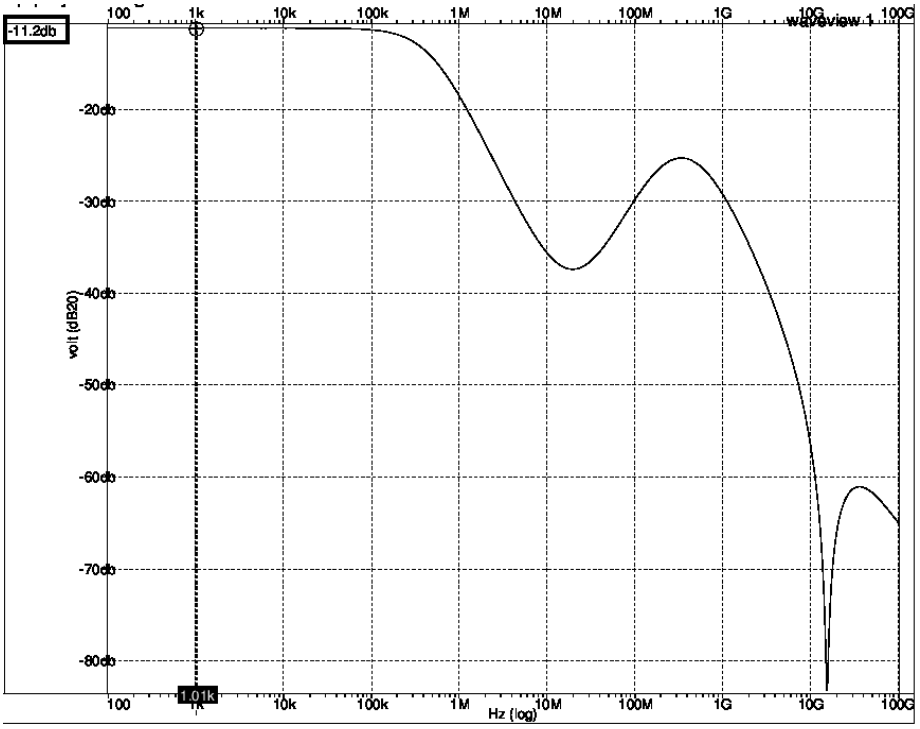
The common mode gain is the common mode gain of the differential pair multiplied by the gain of the second gain stage. $A_{cm} = \frac{2gm_2\frac{1}{2gm_4}}{1+2gm_2r_{o5}}gm_6(r_{o6}||r_{o7}) = 0.23$

$CMRR = \frac{A_{dm}}{A_{cm}} = 79db$

Measure
To find CMRR, we first have to determine A_{cm}, by applying a positive AC signal V_{ac} to both inputs and measuring the signal at V_{out}.



From the Bode magnitude plot below, at low frequencies $A_{cm} = 0.275$. $CMRR = \frac{A_{dm}}{A_{cm}} = 78.2db$

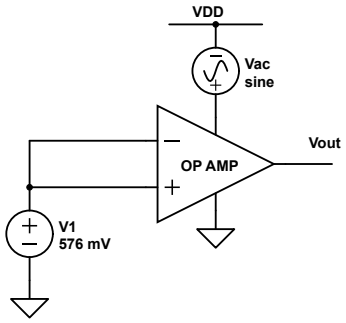


5.5 PSRR

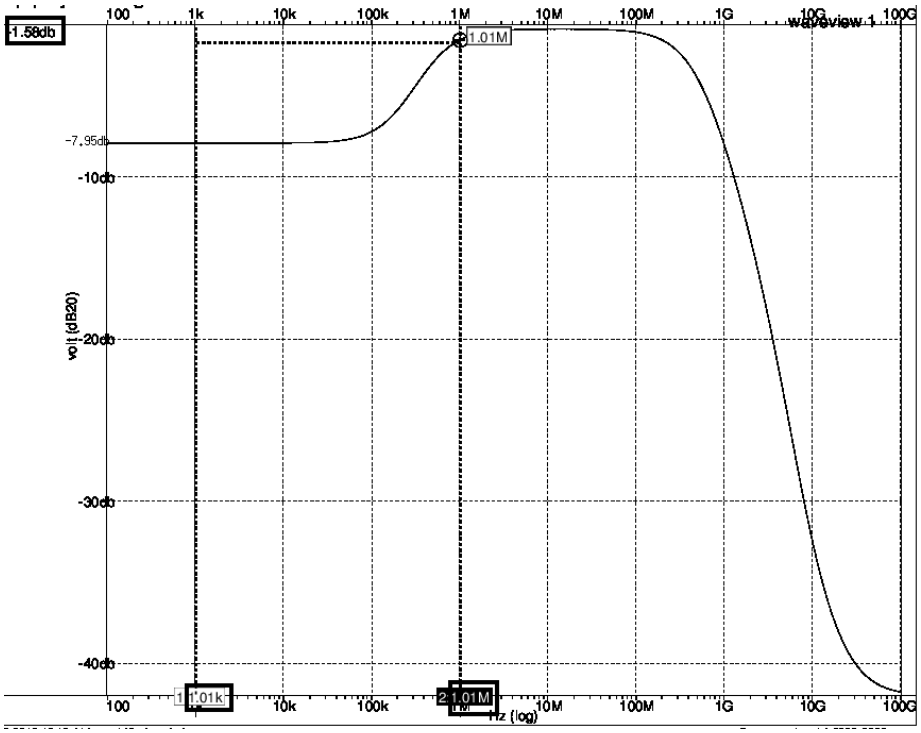
Calculate
Since $\frac{vo}{vdd} \approx 1, PSRR \approx Av = 66$db at DC. The PSRR should be slightly lower at 1MHz due to the gain roll off.

Measure

To find the PSRR, we first have to determine A_{vdd}, which is the gain of a differential signal from vdd to V_{out}. We turn off the AC signal at the input, apply anhttps://wlan.berkeley.edu/cgi-bin/login/cookie.cgi?proxy=

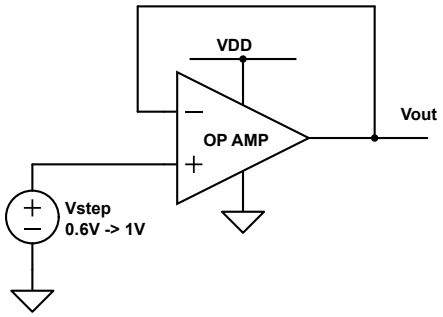


From the Bode magniude plot below, $A_{vdd\_DC} = 0.40$ and $A_{vdd\_1MHz} = 0.83$.
$PSRR_{DC} = \frac{A_{dm}}{A_{cm\_DC}} = 75.0db$
$PSRR_{1MHz} = \frac{A_{dm}}{A_{cm\_1MHz}} = 68.6db$

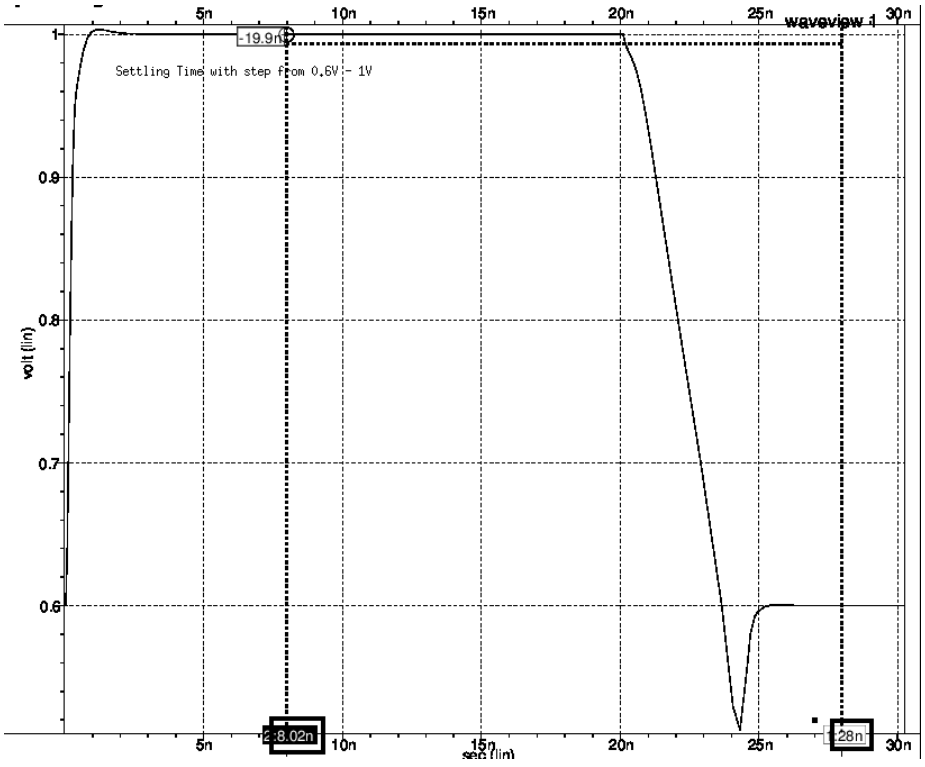


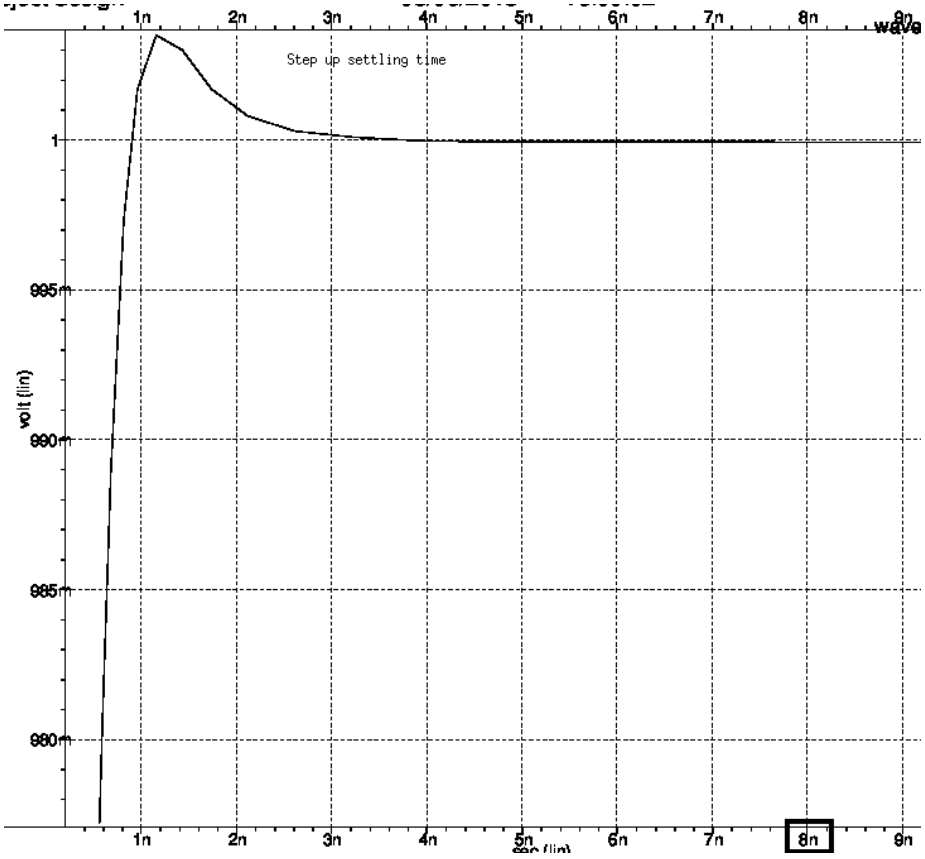
5.6 Settling Time

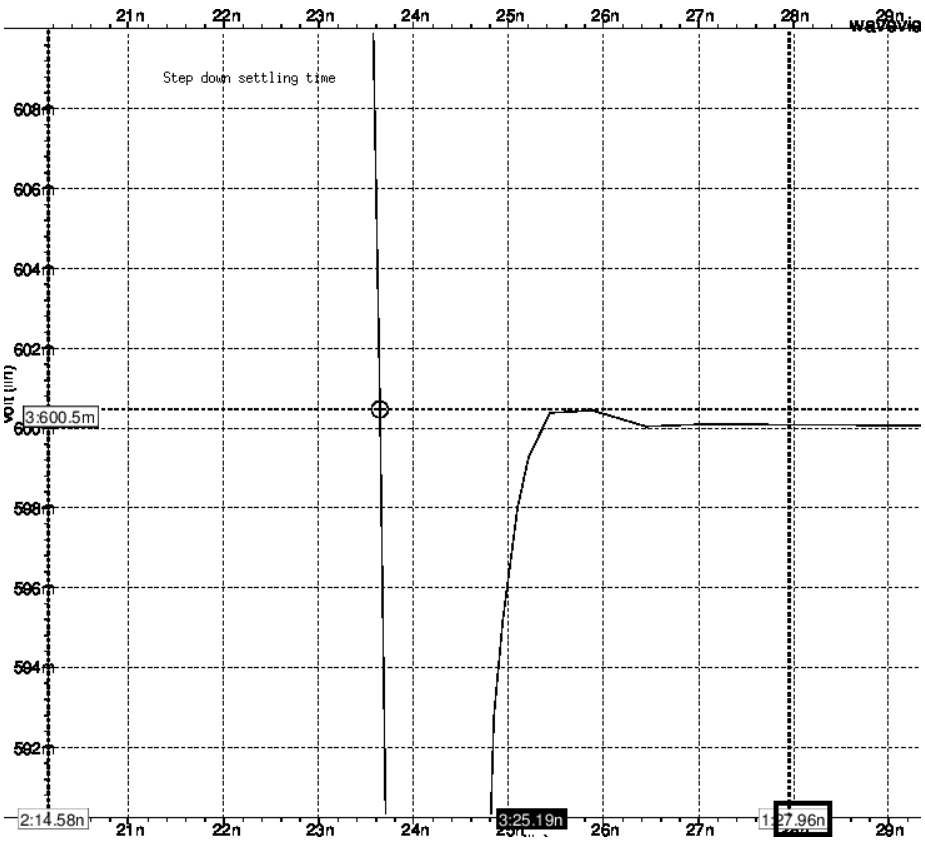
Calculate
Using the approximation $SlewRate \approx \frac{2Vo}{Ts_{0.1\%}}$, and plugging in $Vout = 0.4$V and $SlewRate = \frac{Id_6}{C_c} = 150V/\mu s$, we obtain an estimate for Ts = 5.5ns.
Measure
To measure settling time, we put the op amp in unity gain feedback, apply a 0.4V step input at the positive input, and then observe V_{out}.



In the plot below, the pulse starts at 0.6V, rises to 1V, and lasts 20ns before returning to 0.6V. The few oscillations indicate that the system is overdamped. From the plot below, the step-up settling time is 2.2ns and the step-down settling time is 6.4ns.




Step up settling time
1n
2n
3n
4n
5n
6n
7n
8n
9n
1
995m
990m
985m
980m
volt (lin)



5.7 Power Dissipation

Calculate
Power = VDD x (sum of biasing currents) = 0.96mW.

Measure
The SPICE output file gives the total power dissipated in the circuit, including all biasing branches.
P = 1.05mW.

6 Conclusion

We designed the op amp to meet specifications by using two gain stages, biased by a simple current source, and compensated using a capacitor and nulling MOS resistor. Through performing this design, I became much more aware of the tradeoffs involved in circuit design. For one small change to a parameter, multiple charactersitics may change in different ways and by different amounts. Learning to hold all the characteristics and their equations in my head and anticipating how they changed if I changed a parameter was a valuable skill I gained doing this project. When starting this project, I made the mistake of attempting to design and validate completely on paper before simulating. Unfortunately, some things that did not work on paper worked on SPICE and vice versa. It would have saved a lot of time and effort to just simulate my first design and see what specs I was actually meeting. However, the intuition I built re-doing the designs on paper helped me tweak the SPICE model to make it work. Overall, I found this project useful for building intuition, although I did not enjoy the tedium of iteratively plugging in numbers. Some more guidance on the basic tradeoffs of the design parameters as well as advice on where to start the design would have helped me learn more from this project. The biggest improvement would be to make this a parter project. I find it incredibly helpful and productive to have a partner to discuss ideas with and to error check each other.