

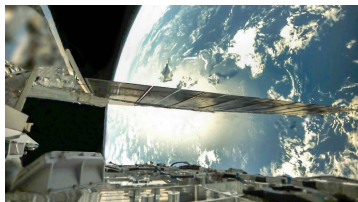
Portfolio

Andrew Fearing

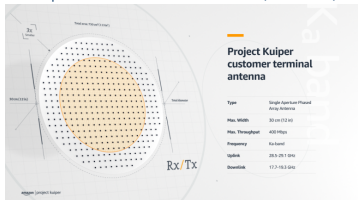
June 2024

Digital Beamforming ASICs

Amazon.com Project Kuiper, Jun 2020 – Aug 2020, May 2021 – Aug 2021, Feb 2022 – Present



KuiperSat in Low Earth Orbit (Amazon)

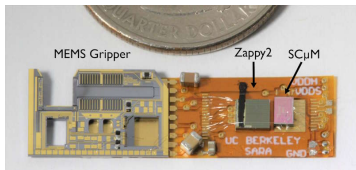


(Amazon)

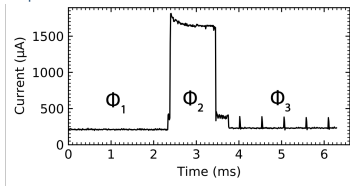
Project Kuiper is a LEO satellite constellation for broadband internet access. As part of the ASIC Systems team, I develop the MATLAB signal processing model for our digital beamforming (DBF) chips. I support the design verification team by providing reference data for bitmatching. I've contributed to bring-up of the customer terminal (CT) DBF ASIC by writing and debugging the firmware, both pre-tapeout on the Palladium Z2 emulator and post-tapeout in lab. I own the nightly regression testing for the MATLAB DBF model and have written unit tests for the DBF firmware CI/CD infrastructure.

Single-chip Micro Mote (SC μ M) applications

UC Berkeley Autonomous Microsystems Lab, August 2019 -- December 2021



MEMS gripper, Zappy2 solar cell, and SC μ M on SARA board



VBAT current during wireless 802.15.4 receive. Φ_1 : Low power ($F_{\text{cortex}}=78$ kHz), Φ_2 : RX with radio on, Φ_3 : periodic wake up to $F_{\text{cortex}}=5$ MHz

SC μ M is a crystal-less CMOS SoC which features an ARM Cortex-M0, standards-compatible 2.4 GHz RF communication, contact-free optical programming, and requires only a power supply to run. I tested integration of SC μ M into the Small Autonomous Robot Actuator (SARA) system. SC μ M microrobots, 2020 GOMACTech

SARA uses a Zappy2 chip to provide solar power to SC μ M. Because the solar cell does not provide enough power to run SC μ M's radio, I programmed and validated the low-power mode for SC μ M. The low-power mode reduces the CPU clock from 5 MHz to 78 MHz to charge a capacitor. Once the capacitor is charged, SC μ M wakes up and increases the clock speed back to 5 MHz for transmit/receive.

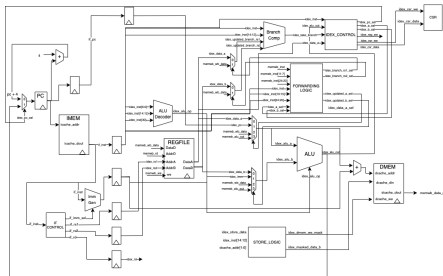
SC μ M as wireless thermometer, 2020 IEEE Sensors

SARA also includes a pad to mount MEMS actuators. Using the same low-power mode to charge a capacitor as described above, SC μ M wakes up to send a square wave signal to a MEMS actuator. The MEMS gripper uses an electrostatic inchworm motor to move the jaw up to 3 mm. SARA with MEMS Gripper, 2021 ICRA

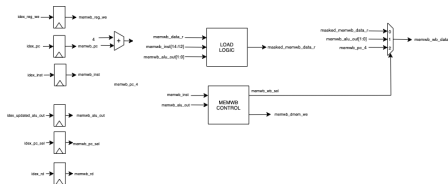
RISC-V CPU

Final Project for EECS 151LA: Application Specific Integrated Circuits Laboratory

Teammate: Eduardo Diaz



IF and IDEX stages



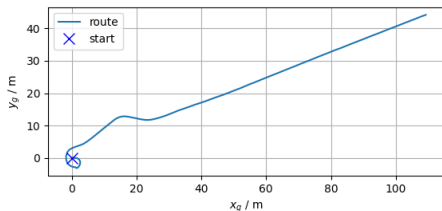
MEMWB stage

In this project we implemented a 3-stage CPU in Verilog HDL. The CPU uses the RISC-V instruction set architecture. For the front-end, we designed our pipeline diagram and verified its implementation using Synopsys VCS simulation. We wrote unit tests and test vectors for verification of each module. We also built a direct-mapped cache for our CPU. For the back-end, we synthesized our design using Cadence Genus. We used Cadence Innovus for PAR. Our submitted CPU design's maximum frequency was 2.4 MHz and could run a suite of C and Assembly scripts.

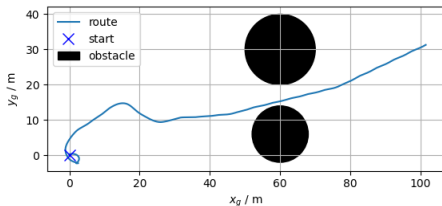
Sailboat Control and Path Planning

Final project for EECS 106B: Robotic Manipulation and Interaction, Spring 2021 (link)

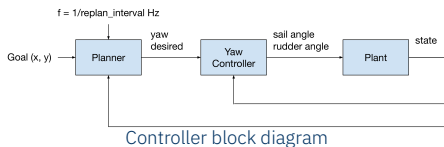
Teammates: Neelay Junnarkar, Hamza Khawaja



Sailing on open seas



Sailing through a narrow channel



In this project we developed a planning and control method for a sailboat to maneuver autonomously through obstacles. The path planner is implemented using CasADi and the IPOPT solver. We used the Python stda-sailboat-simulator to model the dynamics of our sailboat.