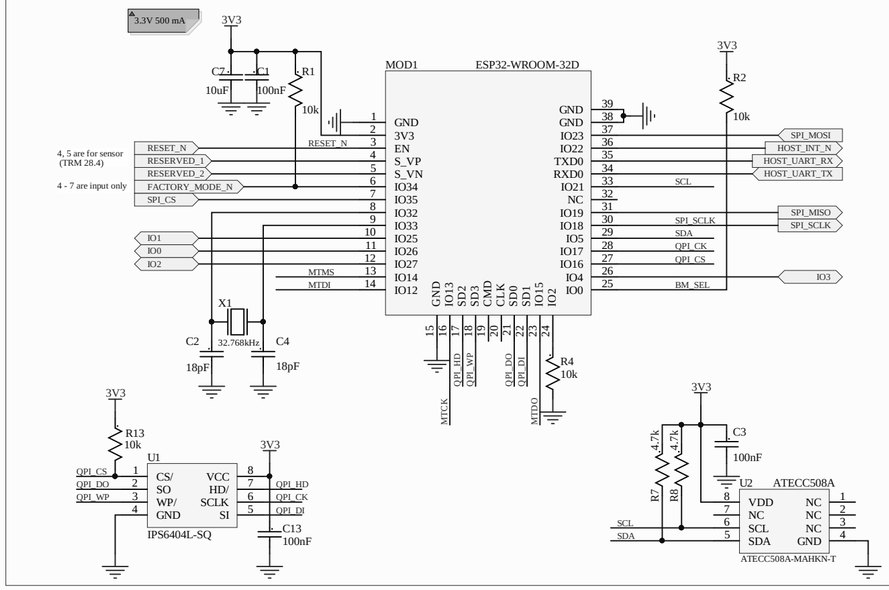
Minimum Circuit needed for production.

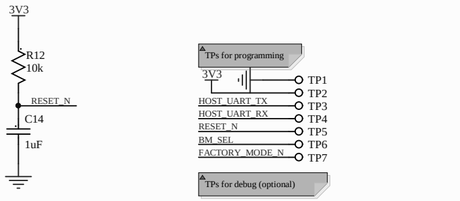


Bootstrap

pin	gpio	func_bootstrap	func_operation	on-chip-default-pull
25	0	Boot Mode. 1:SPI 0:Dnld	BM_SEL	pull-up
24	2	Boot Mode. 1:NC 0:Dnld		pull-down
14	12	V_SPI. 1:1.8V 0:3.3V	MTDI	pull-down
23	15	Debug log. 1:on 0:off	MTDO	pull-up
29	5	SDIO slave clk pol	SDA	pull-up
		*SDIO clk pol can be changed later after booting		

Required setting for serial programming
pin 25 : 0 pin 24 : 0 pin 14 : 0

Required setting for normal operation after production
pin 25 : 1 pin 14 : 0 pin 23 : 0



Design Notes:
ASR-2DF Reference Design can be used in 2 different ways:
As a Module soldered down to a carrier board or as a Connectorized Module connected via cable to end product control board.

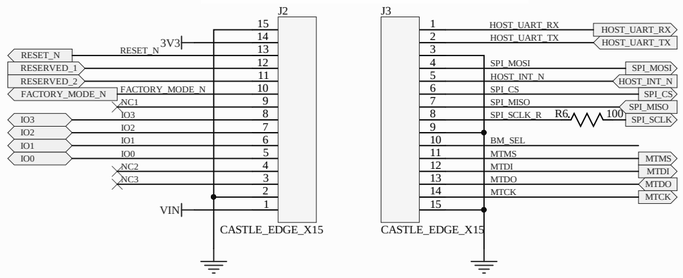
Soldered Down Module:
- Customer will use castellated pads (J2 and J3) to solder down ASR-2DF to the carrier board.
- Signals associated with TP1 through TP7 (eg. HOST_UART_TX/RX, BM_SEL, ...) should have corresponding test points on the customer carrier board to allow for programming.
- 3V3 : Design requires 3.3V at 500mA. 3v3 supply can be supplied off-board on the carrier board OR via the on-board regulator.
- Care should be taken when using these pins on the carrier board for other purposes:
  * HOST_UART_TX, HOST_UART_RX, FACTORY_MODE_N, MTDI, MTDO, SDA, MTMS, BM_SEL
- In this configuration, components for the stand alone, Connectorized Module can be no stuffed.

Stand Alone, Connectorized Module:
- Customer will use 6pin cable to connect ASR-2DF to their controller board.
  * Pin2 of the cable should be connected to GND (pin1) for normal operation.
  * Pin3 is an active high RESET signal.
  * VIN : 4.5V to 18V
- Customer will use [H1 - H4] and/or 4 slots (2mm x 0.7mm) to mount ASR-2DF to their housing. H1 through H4 are 80mils in diameter.
  * Customer can use M2 or #2 screws to screw down ASR-2DF. Or
  * Customer can use Teardrop style PCB support. (eg. https://www.essentracomponents.com/en-us/pcb-electronics-hardware/supports/standard-snap-lock-supports/pcb-supports-locking-teardrop/mdlsp3-1-01)

Change Notes:
[EVT2]
- Fix RC time constants for RESET_N and power supply EN to fix reboot reason issue
- Add 32kHz crystal
- Change pinmap to match updated default pinmap for Plumo-2D
- Change to new Factory Mode scheme
  * Ground FACTORY_MODE_N (ne “CTS”) to force factory mode
  * Added pullup
- Reorganize to regroup functions
- Removed reserved I2C bus (SCL/SDA) from external connector
- Change pinout of J2 and J3 to make routing easier
- Rename SHIELD pins to RESERVED
- Revised testpoints needed for programming
- Added testpoints to back-side (coincident with corresponding pins on J2 and J3)
- Added BM_SEL to J3
- Added mounting pins to schematic symbol of 6 pin connector
- Shifted J4 up from board edge to give more clearance from castellated pads
- Added bom variants for connectorized module and module form factors
- Added extra ground vias to fill in ground pour gaps
- Updated ESP32 footprint to fix GND pad location
- Fixed ESP-32 GND pad via locations and sizes.
- Added pin1 mark to castellation "connectors"
- Updated documentation on schematic to more clearly define build variants
- Changed R11 from DNS to 10K resistor and updated variants to correctly stuff that part.

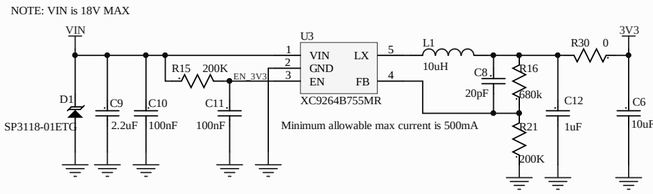
[DVT/PVT]
- Released under Apache2.0 Open Source License.

J2 and J3 are not actual components to be stuffed.
These are castellated pads, a mechanical part of the board.

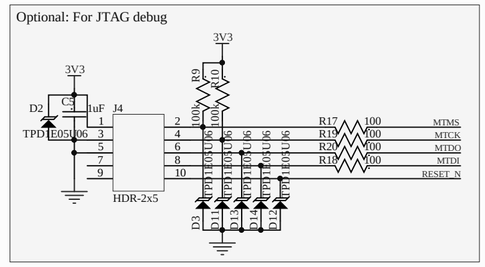


RESET_N is connected to MOD1 pin3 EN pin(and ESP32 CHIP_PU pin).
Holding RESET_N low will put the module in reset state.

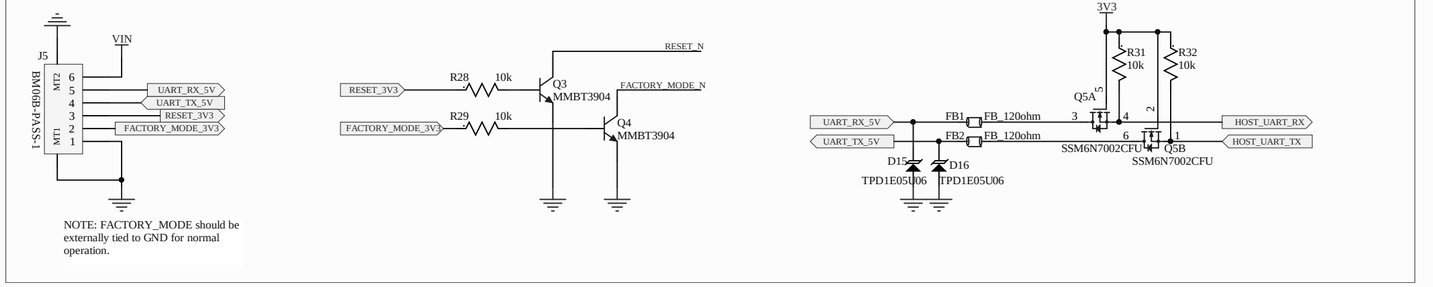
NEEDED for Connectorized Module variant, Optional otherwise



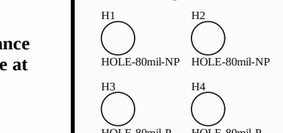
Optional: For JTAG debug



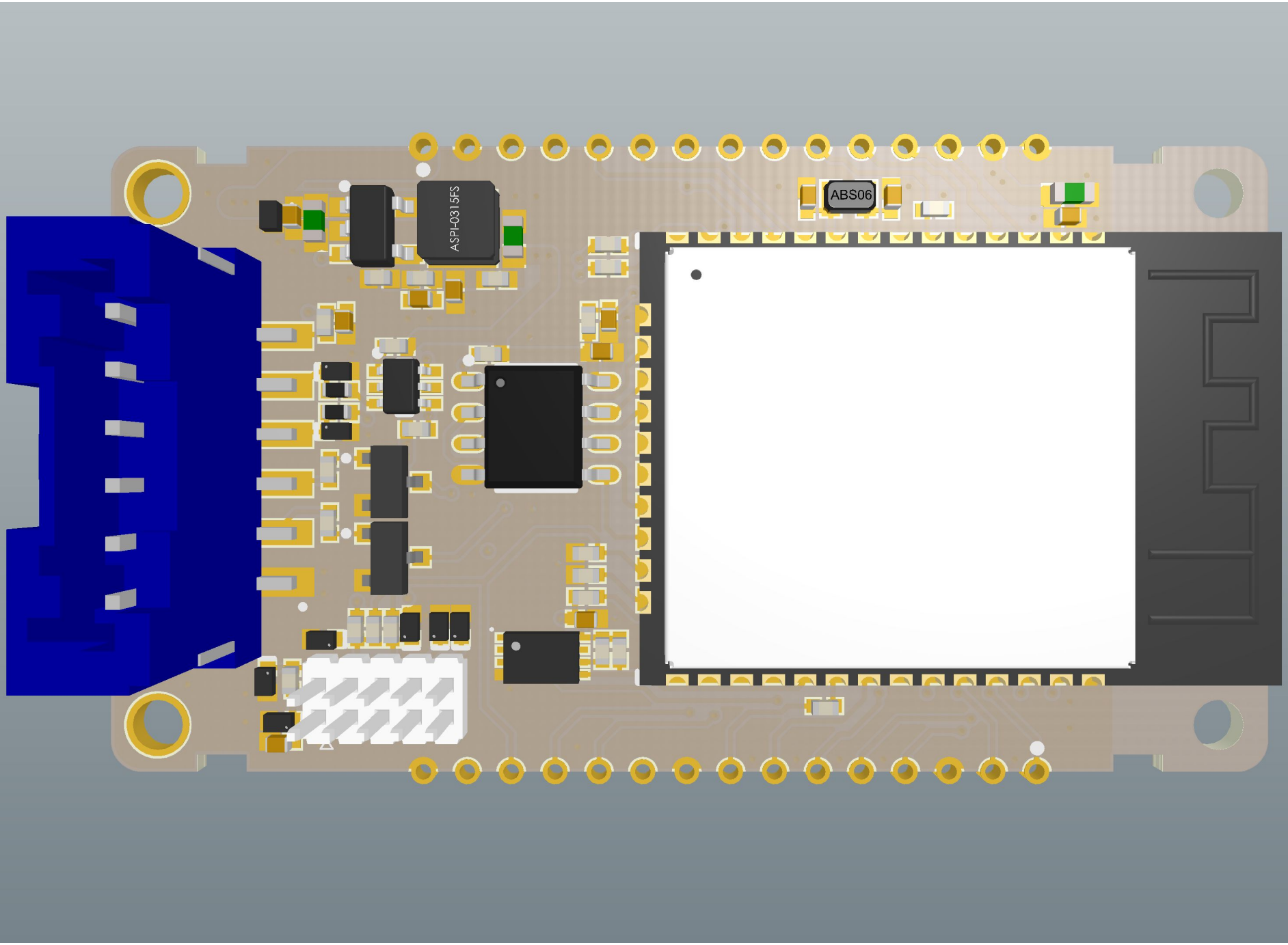
Parts needed for the Connectorized Module application

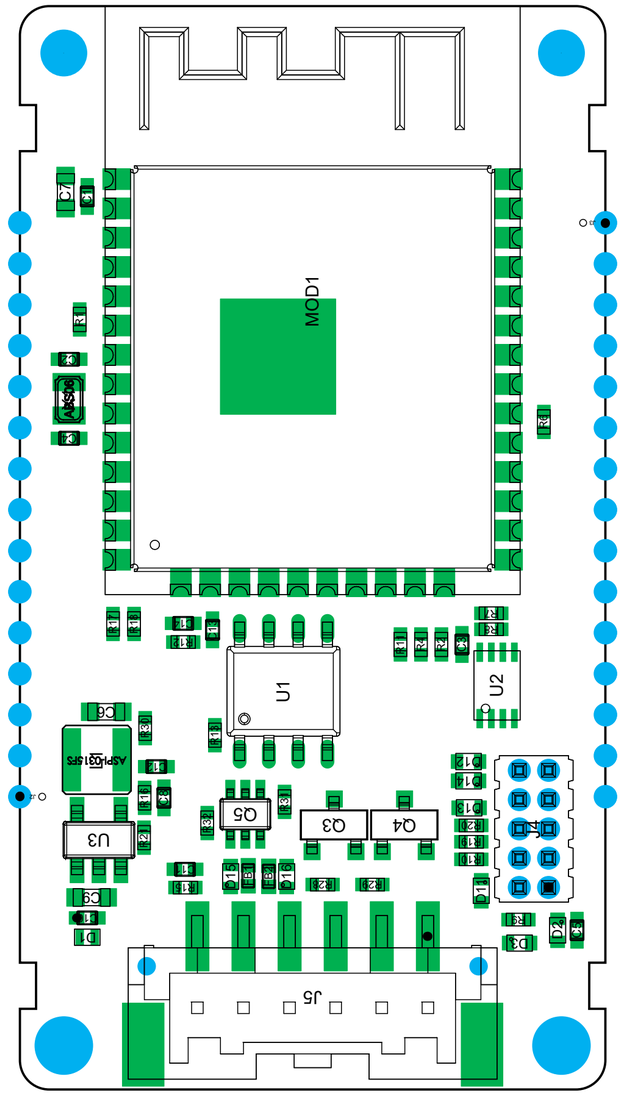


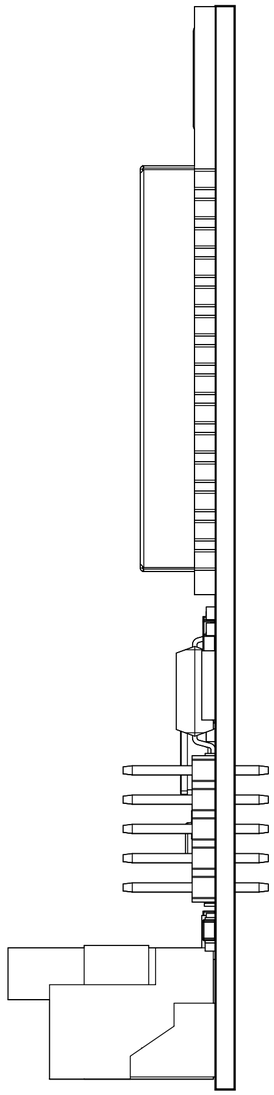
Mounting Holes

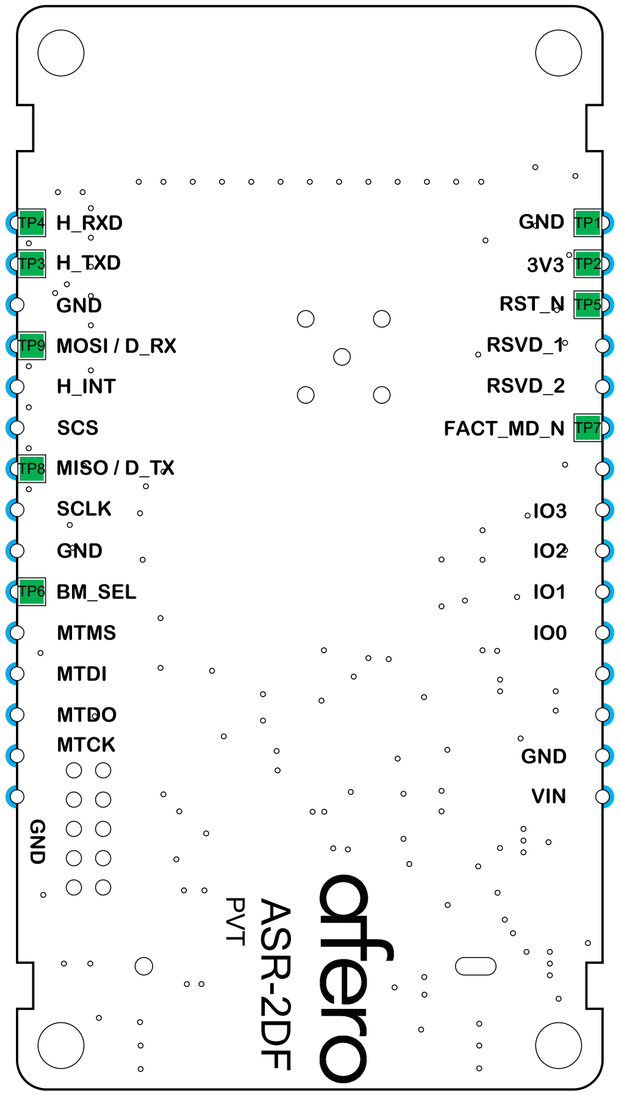


Title: ASR-2DF		Afero, Inc.
Size: C	Number:	Revision: PVT
Date: 12/13/19		Sheet of 1 1
File: Z:\wrk\..\ASR-2DF.SchDoc		Drawn By: SWR / RSB


ASPI-0315FS
ABS06







J2 and J3 have been placed in the current location intentionally so that after the board is routed, the edge will be castellated.

NEXT ASSY	*USED ON*	
APPLICATION		

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
FRACTIONAL±
ANGULAR: MACH± BEND±
TWO PLACE DECIMAL ±
THREE PLACE DECIMAL ±
INTERPRET GEOMETRIC TOLERANCING PER:
MATERIAL
FINISH
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN	*SR/RSB*	*12/13/19*
CHECKED		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:
PVT

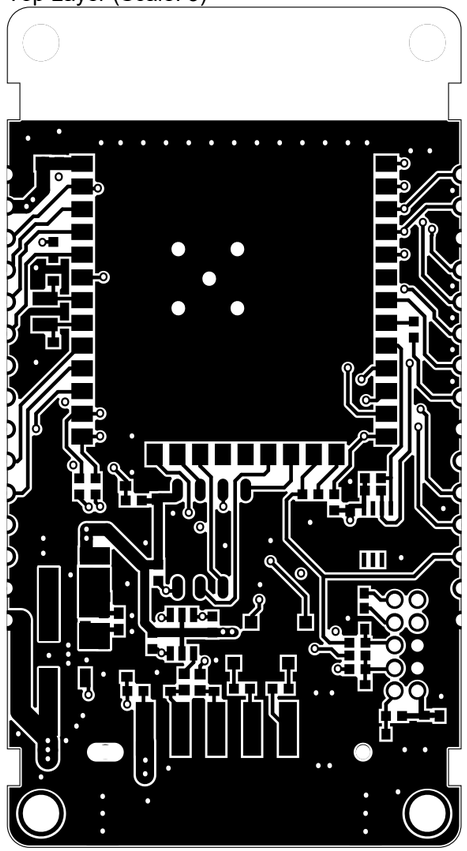
Afero, Inc.

TITLE
ASR-2DF Assy Drawing

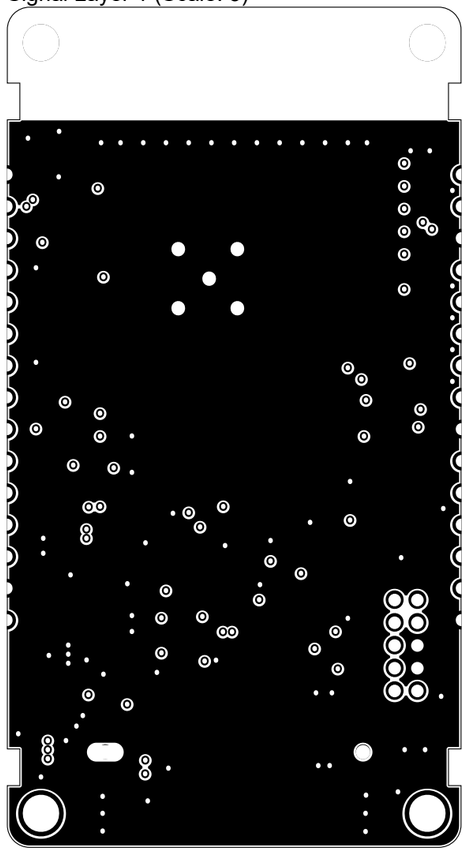
SIZE	*DWG. NO.*	

SCALE: 1:1	*WEIGHT:*	*SHEET 1 OF 1*

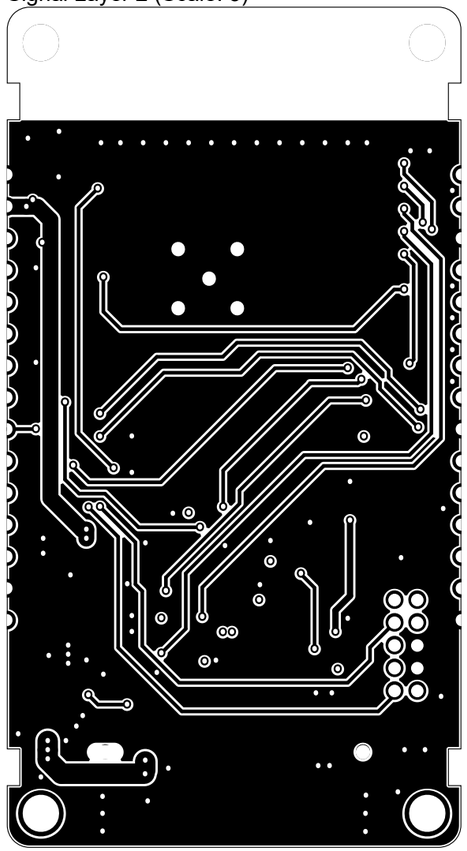
Top Layer (Scale: 3)



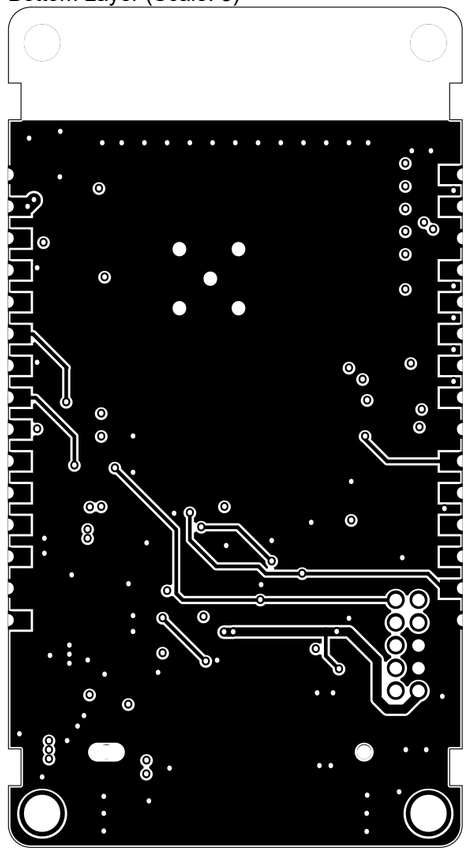
Signal Layer 1 (Scale: 3)



Signal Layer 2 (Scale: 3)



Bottom Layer (Scale: 3)



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APPLICATION	

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ANGULAR: MACH± BEND±
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INTERPRET GEOMETRIC TOLERANCING PER:
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DO NOT SCALE DRAWING

	NAME	DATE
DRAWN	SR/RSB	12/13/19
CHECKED		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

PVT

Afero, Inc.

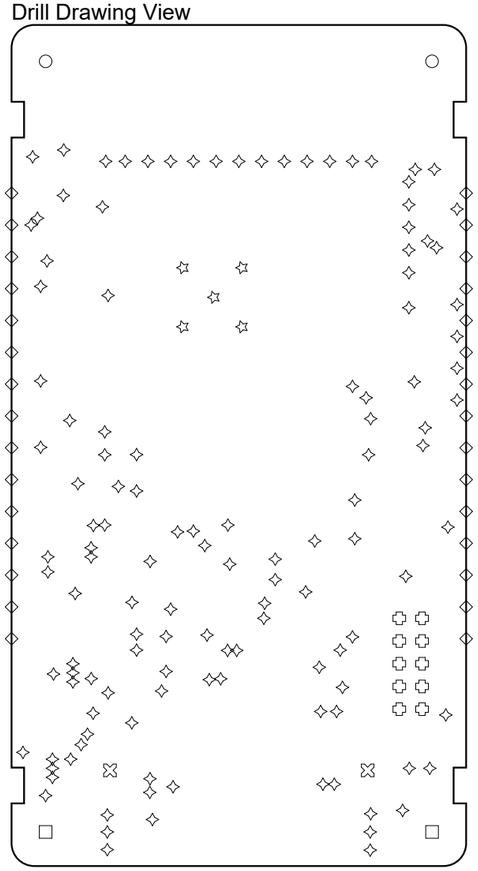
TITLE

ASR-2DF Fabrication Drawing

SIZE	DWG. NO.	

SCALE: 1:1	WEIGHT:	SHEET 1 OF 2

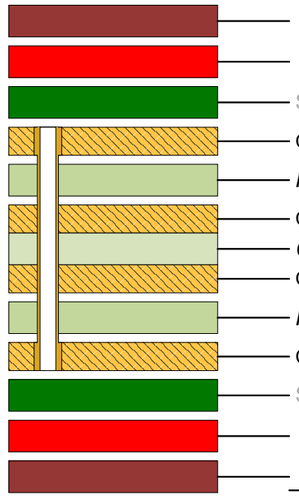
Drill Drawing View



Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
□	2	2.03mm	Plated	None
○	2	2.03mm	Non-Plated	None
◇	30	0.63mm	Plated	None
⊠	2	0.80mm	Non-Plated	None
✣	10	0.70mm	Plated	None
✧	126	0.25mm	Plated	None
☆	5	0.76mm	Plated	None

Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Paste			Paste Mask	GTP
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.010mm	Solder Resist	Solder Mask	GTS
Copper	Top Layer	0.036mm		Signal	GTL
Prepreg		*0.170mm*	*FR408*	*Dielectric*	
Copper	Signal Layer 1	0.018mm		Signal	G1
Core		*0.381mm*	*FR408*	*Dielectric*	
Copper	Signal Layer 2	0.018mm		Signal	G2
Prepreg		*0.170mm*	*FR408*	*Dielectric*	
Copper	Bottom Layer	0.036mm		Signal	GBL
Surface Material	Bottom Solder	0.010mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
	Bottom Paste			Paste Mask	GBP

Total thickness: 0.848mm

1) Fab material: Isola FR408 or 370HR or equivalent lead free process capable material.
2) Lead-free ENIG finish.
3) GREY Solder Mask.
4) WHITE Silk Screen
5) Vias are to be filled with non-conductive material

NEXT ASSY	USED ON
APPLICATION	

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	NAME	DATE
DRAWN	SR/RSB	12/13/19
CHECKED		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

PVT

Afero, Inc.

TITLE

ASR-2DF Fabrication Drawing

SIZE	DWG. NO.	

SCALE: 1:1	WEIGHT:	SHEET 2 OF 2