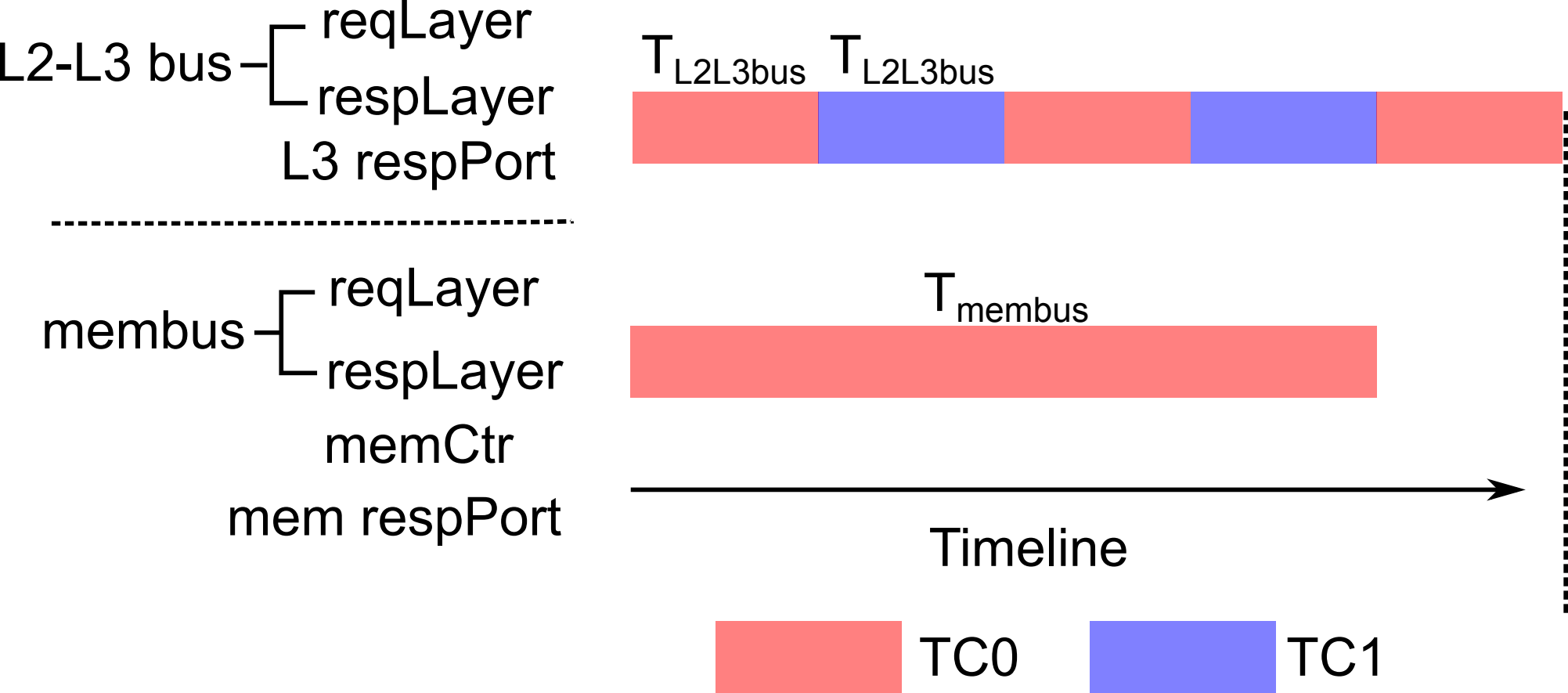
L2-L3 bus
reqLayer
respLayer
L3 respPort
membus
reqLayer
respLayer
memCtr
mem respPort
T L2L3bus
T L2L3bus
T membus
Timeline
TC0
TC1