# High-efficiency Class-D Audio Amplifier using Second Order Delta Sigma Modulation

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# High-efficiency Class-D Audio Amplifier using Second Order Delta Sigma Modulation

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***Abstract***

*This paper presents a high efficiency class-D audio amplifier using a second order delta sigma modulation. The proposed circuit contains a high modulation frequency, two integrators and three resistive feedbacks. The results show that the proposed amplifier has low THD (<0.001), High SNR (>80dB), and high efficiency (>95%).*

***Keywords:*** *Class-D audio amplifier, THD, SNR, Efficiency, Power amplifier.*

## 1. Introduction

Interests to have high-efficiency audio amplifier without any noise or harmonics have been increasing in last decade [1]. Since the efficiency of the linear amplifier such as class–A or class-AB are not even close to class-D, researchers use class-D amplifiers [1, 2].

Class-D amplifiers are divided into two categories: Pulse Width Modulation (PWM) and Pulse Density Modulation (PDM) [3] such as delta sigma modulation [4]. When using PWM, a comparator generates a pulse signal by comparing the input signal and a carrier signal, but the carrier signal with relatively low frequency leads to harmonics issues [5].

The PDM method have relatively a low power efficiency due to its fast clock speed, but instead it doesn't have harmonics issues [6]. If a solution is provided for efficiency of PDM, the result would be outstanding and more useful than PWM. In this paper, we utilized some technics and the result was 97% power efficiency, which can help audio amplifiers with better qualities.

The remaining of this paper is organized as follows: section 2 introduces class-D standard view. Section 3 presents PDM method and simulations. Section 4 presents the proposed model and simulation results. Section 5 compares the proposed circuit with other class-D amplifiers. Finally, section 6 concludes this paper.

## 2. Class-D Standard View

A simple class-D PDM audio amplifier is shown in figure 1 [7, 9].

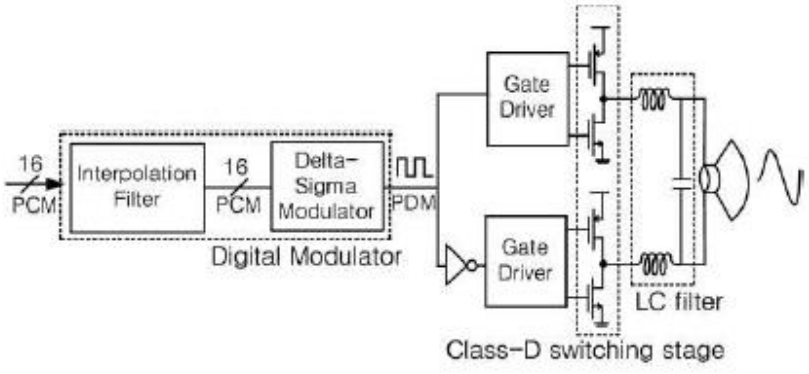


**Figure 1. A simple class-D PDM audio amplifier [9]**

As it is shown in this figure, this type of amplifier has gotten multiple stages to get the best possible output. Note that these stages must be optimized.

The first stage that is considered here is PDM method. To start with PDM method, the basic circuit and simulation was studied in the next section.

## 3. PDM method and simulations

The first order delta sigma modulation with one state feedback is shown in figure 2.

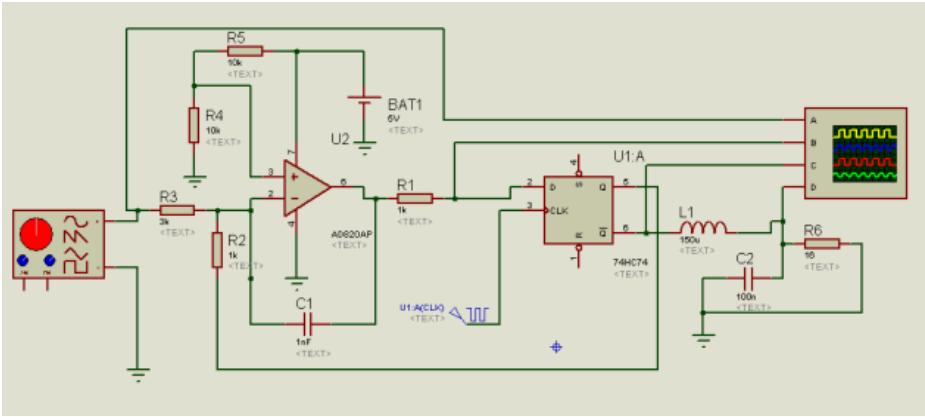


**Figure 2. First order delta sigma modulation with one state feedback**

This circuit was simulated in Proteuse and its outputs are shown in figure 3. The results show that the output is near perfect if we ignore efficiency purposes.

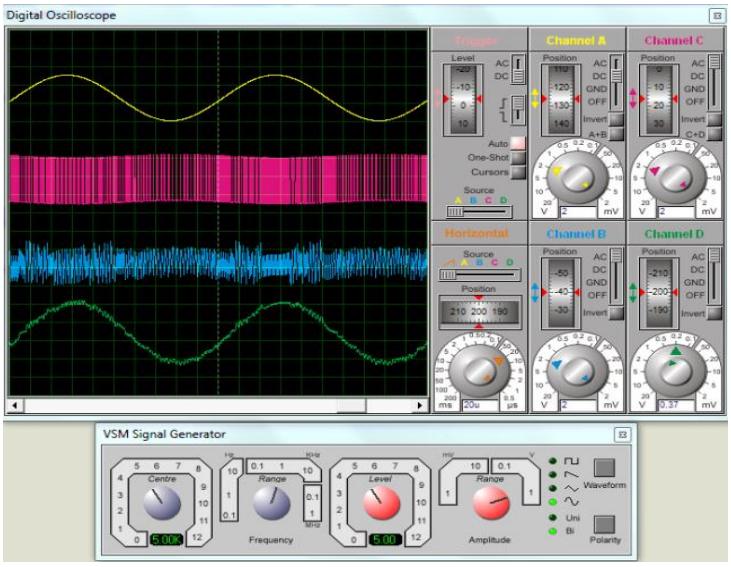


**Figure 3. Result of first order delta sigma modulation with one state feedback**

## 4. The Proposed Model

To have high efficiency, some changes is needed. First a new integrator was added to this circuit. As we know, to have steady results, a resistive feedback must be added, but the results are not as good as expected. Since the noises in the output of another resistor was added to the proposed model at this stage, the results are a little better than before, however by changing the value of this resistor, steady signals are given in the output. The proposed model was simulated as follows.

Figure 4 shows the proposed PDM method.

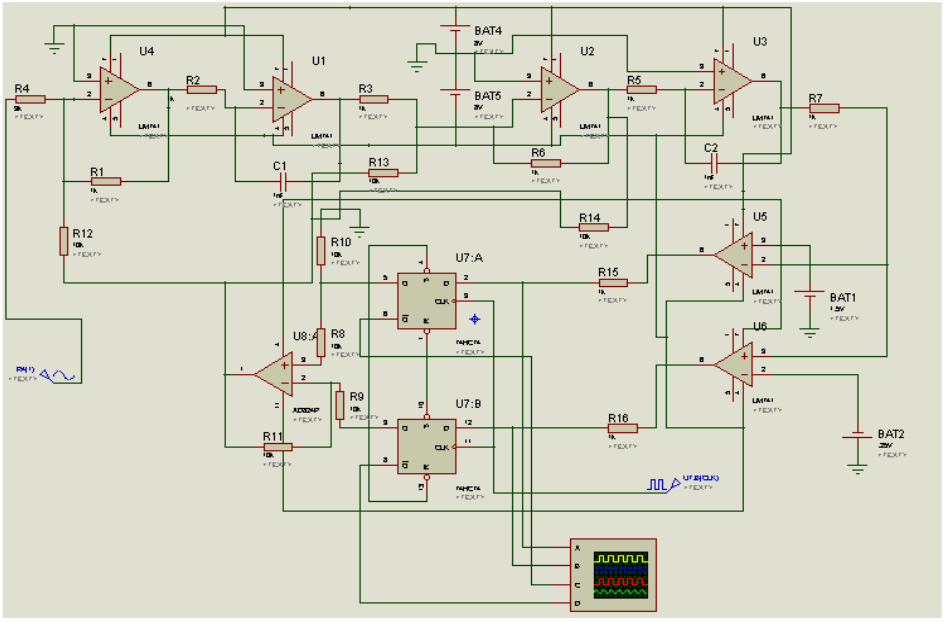


**Figure 4. Second order delta sigma modulation with three state feedback**

Another important role is played by the modulator frequency. By changing modulator frequency between 1MHz to 5MHz, output efficiency was decreased. However, the SNR is increased. As a result, to choose modulator frequency, we had to check efficiency, SNR and output quality. At 1MHz, the proposed model has better power output efficiency, but lower quality (low THD). The best modulator frequency is 5MHz, which has both good power efficiency and low THD. The output of this model is shown in figure 5.

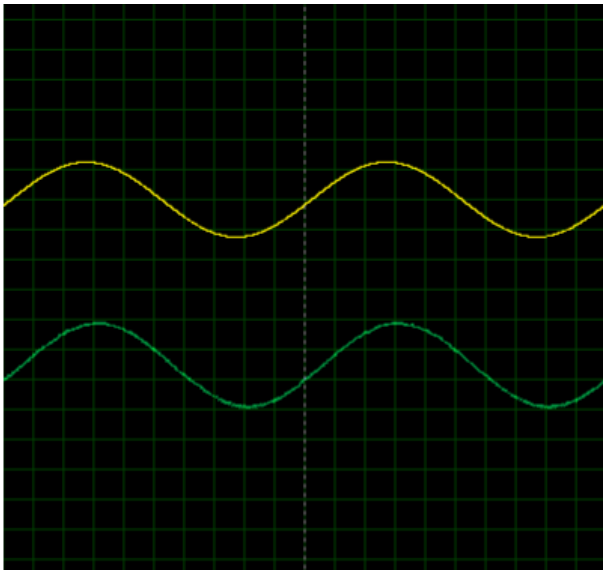

**Figure 5. The simulation results of the proposed method**

PDM was then completed, but we needed to look for a better transistor, which has low resistor ($r_{ds}$). Since in class-D audio amplifier, power consumption during switching time (On state to off state or wise versa) is related to $r_{ds}$, to have high SNR, a transistor with the lowest possible $r_{ds}$ is needed that can work in high frequency and high power. Our investigation shows that IRS20124S(Pbf) transistor can be utilized in this circuit.

Another important part was to drive these MOSFETs. A circuit was design just to drive these MOSFETs. The proposed circuit is shown in figure 6.

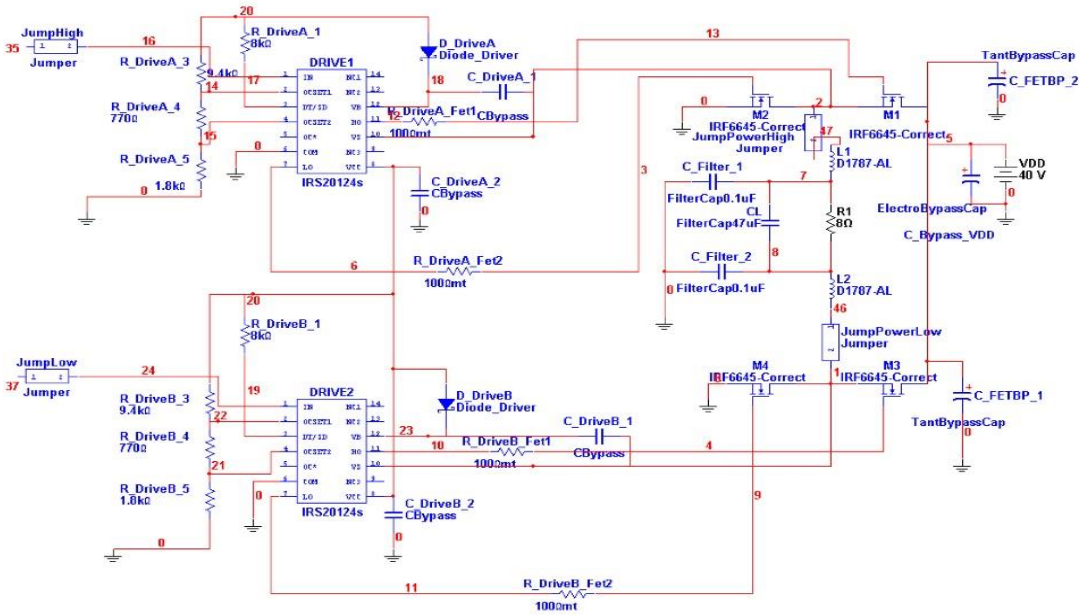


**Figure 6. Driver of MOSFET**

## 5. Comparison

In table 1, the proposed model was compared to the similar works and also PWM modulations.

**Table 1. The comparison table for class-D audio amplifiers**

| Parameters | This Work | [10] | [11] | [12] | [13] | [9] |
|---|---|---|---|---|---|---|
| Modulator architecture | Digital ΣΔ | PWM | PWM | PWM | DSP | Digital ΣΔ |
| $VDD_P$ | 50V | 60V | 20V | 50V | 18V | 80V |
| $P_{Out\ max}$ | 80W | 200W | 20W | 240W | 13W | 45W |
| Peak SNR (dB) | 78 | 82.2 | 91 | 74.1 | 87 | 92.8 |
| THD+N | 0.001 % | 0.017% | 0.01% | 0.1% | 0.07 % | 0.015 % |
| Efficiency (%) | 97 | 90 | 89 | N/A | 88 | 93 |
| Bandwidth (kHz) | 30 | 20 | 20 | 20 | 14 | 20 |

Based on our simulation results, which are shown in table 1, the proposed class-D audio amplifier has an improvement compared to class-D audio amplifier in [9-13] in terms of THD, efficiency, and bandwidth. In addition the proposed class-D audio amplifier provide an improvement compared to class-D audio amplifiers in [9], which utilized digital delta sigma modulator architecture, in terms of output power.

## 6. Conclusion

In this paper, a new PDM class-D audio amplifier was designed and simulated. Our simulation results showed that the proposed class-D audio amplifier has advantages compared to other class-D audio amplifiers in [9 - 13].

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