THIRD ORDER SC CHEBYSHEV LPF USING CMOS TRANSCONDUCTANCE LNA

ABSTRACT

This work presents a Third order SC Cheybshev LPF in a single and short circuit forvital sign processing circuit. The vital sign processing circuit simulates dc elimination and out-of-band interference rejection. This filter (LPF) is used to reduce noise in the circuit. The proposed circuits possess high efficiency in terms of power and current consumption, which is due to the increased area requirement of the chip and noise caused by the use of the OTA in Chebyshev filter design. Moreover, the scheme for generating current output signals using amplifier meets this requirement. However, the noise of the amplifier contributes to the output. Based on the studies, A novel Third order SC Chebyshev LPF implemented in a simple circuit with LNTA. The leap-frog configuration of the LPF is employed to maximize stability and minimize PVT variations.

To investigate the performance of the proposed design, Cadence Virtuoso simulations are used. The simulation results, based on the 45-rim CMOS process technology model, indicate that the proposed design have superior speed and power against other existing design. The proposed design is intended to minimize SNR aswell as power consumption. Therefore, a useful metric used in these cases is the power delay product (PDP) which can be used to characterize the overall performance of a system. The PDP can be improved at different levels at the device level, layout level, circuit level, architecture level. The proposed design is suitable for vital sign processing circuits, especially for radar systems.

BLOCK DIAGRAM

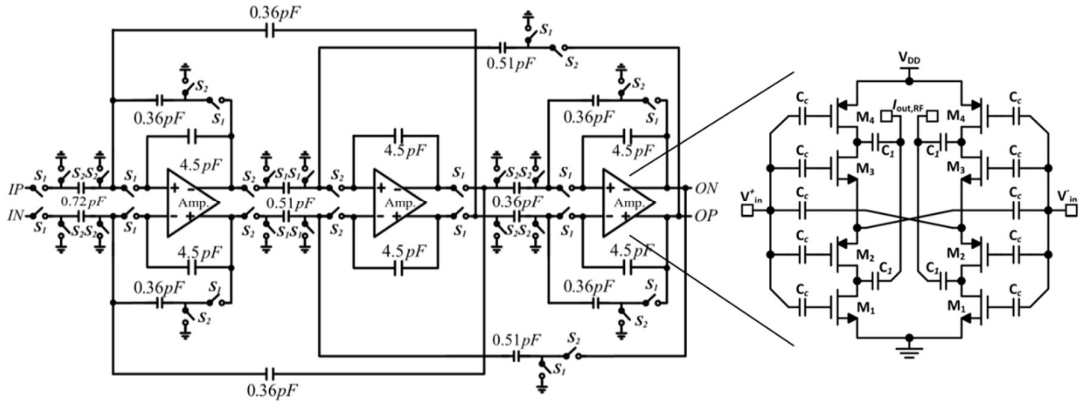

Fig. 2: Diagram of the Third-order SC Chebyshev LPF with LNTA.

SCHEMATIC DIAGRAMS

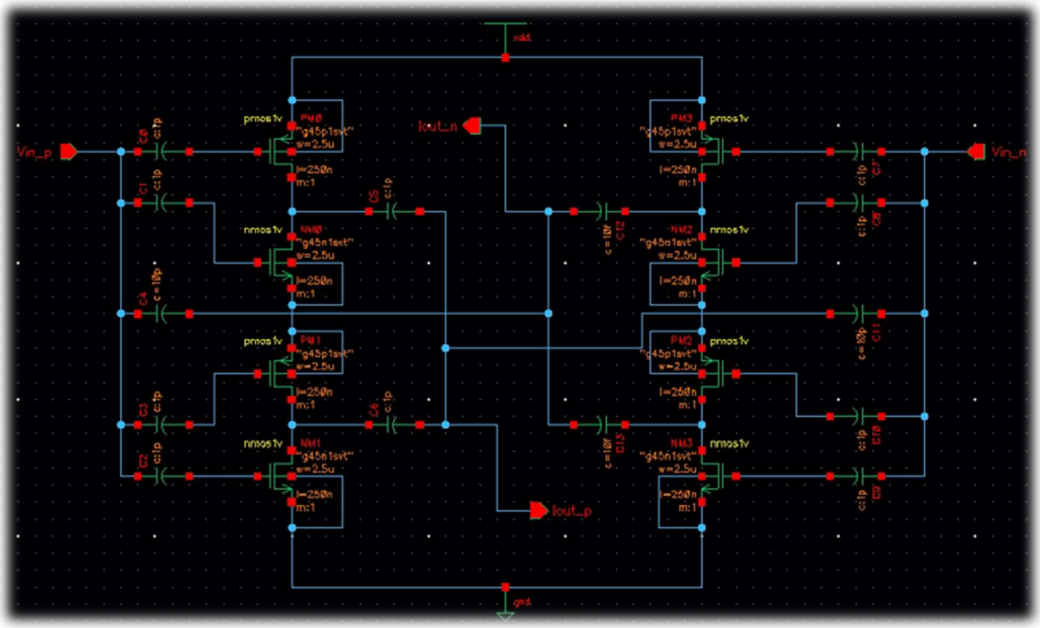

Fig. 2: Schematic Diagram of LNTA.

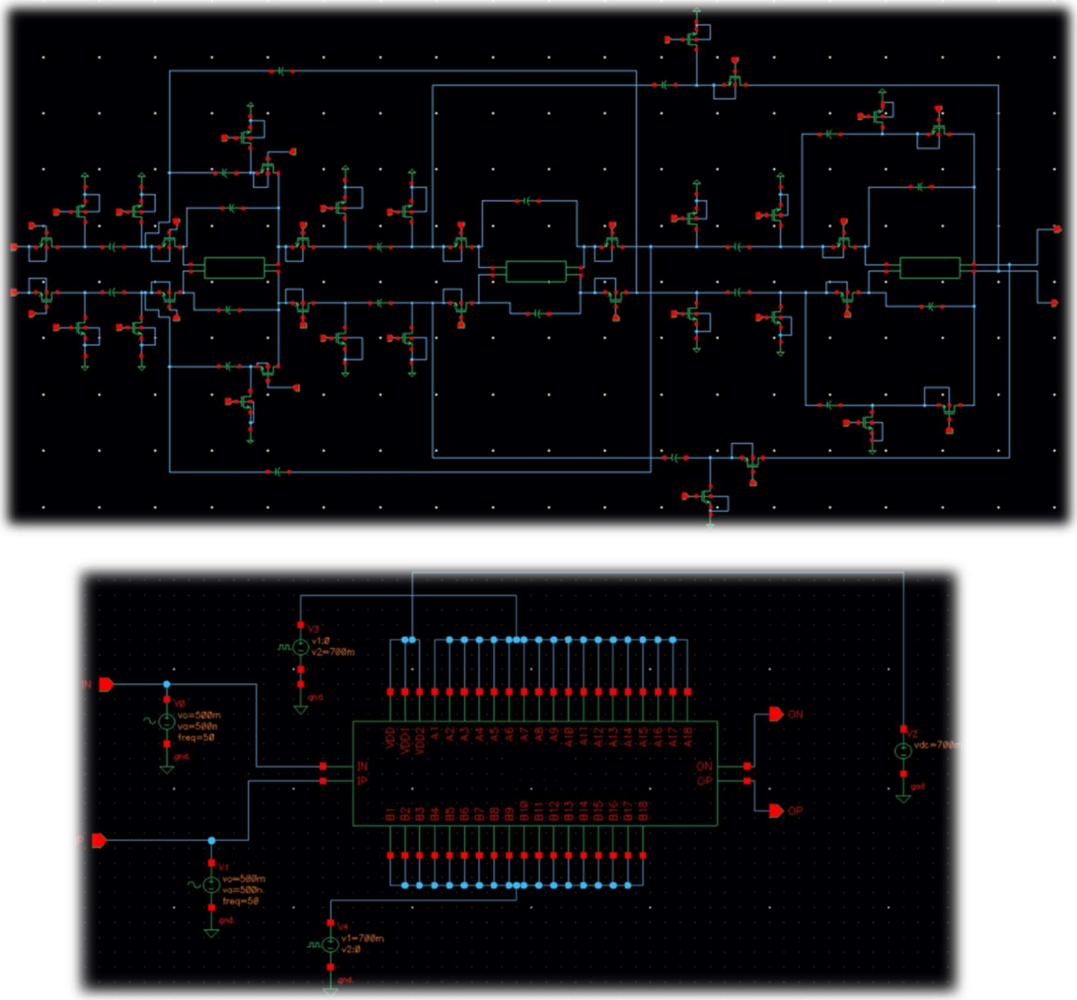

Fig. 3: Schematic Diagram of the Third-order SC Chebyshev LPF with LNTA.

Third-order SC Chebyshev LPF

The Third order SC Chebyshev LPF as shown in Figure 1 helped improve the overall SNR by suppressing noise. Leap-frog configuration of the LPF is adopted to maximize stability and low-impact PVT variations. The bandwidth may be adjusted from 50 Hz to 20 kHz, decided with the aid of using the sampling rate of the SC LPF using interval sample and hold (S/H) clocks

Low Noise Transconductance amplifier

The Third order SC Chebyshev LPF designed with low noise transconductance amplifier as shown in Fig 1. The transconductance LNA has two roles: First, it must convert the input voltage signal to an output current signal with minimal noise introduced. Second, it should provide input adaptation. LNA transconductance topologies. Common source LNA is shown in Figure 4 (a). It provides reasonable transconductance while it does not provide input matching. Common source LNA with inductive degeneration is shown in Figure (b). Its Gm does not depend on the transconductance of the transistor while it provides a narrow band adaptation. Figure (c) shows the asymmetric common gate LNA. Provides broadband matching; however, the gm transistor must be large enough to provide the matching. Figure (d) shows the cross differential common gate LNA.

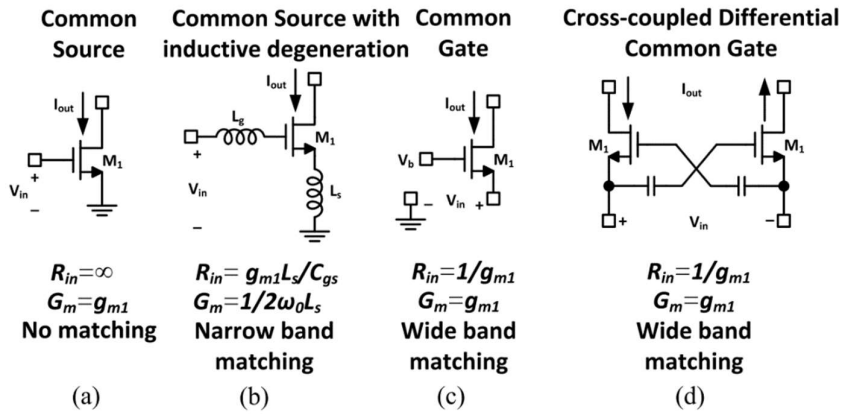

Figure 4: Transconductance LNA topologies. (a) Common source. (b) Common source with inductive degeneration. (c) Single-ended common gate. (d) Cross-coupled differential common gate.

Provides wideband matching and cross coupling increases transistors by gm. The downside of a LNA common gate is that it requires a lot of current to provide an input

match. As a solution, Figure 5.2 shows the basic concept of the proposed transcon ductance LNA. Unlike, complementary CMOS transistors (M2 and M3) are used to provide an input match. Both transistors have an input voltage (negative input voltage) applied to the gate (source) of the transistor to increase the transconductance by a factor of two. In addition, M1 and M4 are added to increase the total transconductance.

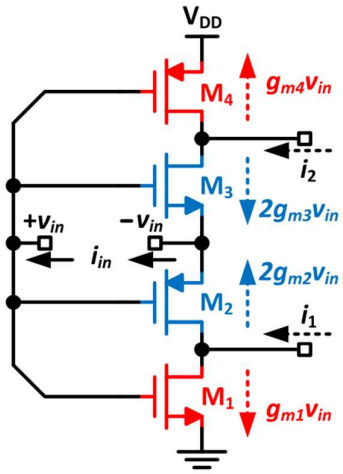

Figure 5: Transconductance LNA concept.

Goals and Future Scope

In this work, first evaluated the existing Third Order SC Chebyshev LPF circuit design based on the 45-nm CMOS process technology in Cadence Virtuoso simulations. The evaluation revealed that using the OTA in the circuit is a drawback. Another disadvantage of a circuit is the amplifiers are adopted additional noise and affected the system stability. Further amplifier won't solely increase the power consumption of the chip; however, its input offset voltage and noise conjointly have an effect on the accuracy of the output. This feedback increases the delay, output capacitance, and, as a result,energy consumption of the circuit.

To overcome these limitations. A Novel Third Order SC Chebyshev LPF circuit is designed with Low noise Transconductance amplifier. It has very good speed, low SNR, accuracy and convergence. After simulating the Proposed circuit, The results of the simulation revealed that the proposed circuit has excellent performance in simulated conditions. The proposed design is suitable for vital sign processing, especially for radar systems, as well as for audio applications, including audio crossover.

This work can be extended to designing of Chebyshev low pass filter with low frequency and low power in the future. However, the basic need in order to design Chebyshev LPF for low power is to minimize the power of LNTA. The proposed

design in thus highly suitable for use in low power, low-voltage sensor interfaces and in portable medical instrumentation. This can further be used for lower cut-off frequency and power. And since it is 3rd order filter so for improved performances higher order filters for few nW power can be designed using this topology.

Third-order SC Chebyshev LPF Characteristics

Parameter	Description	Unit	Condition
Technology	45nm CMOS Process		
IP	Input Positive Signal	mV, nV, Hz	Offset Voltage = 500mV, Amplitude = 500nV, Frequency = 50Hz
IN	Input Negative Signal	mV, nV, Hz	Offset Voltage = 500mV, Amplitude = 500nV, Frequency = 50Hz
A	Switch 1	V	V1 = 0, V2 = 0.7V
B	Switch 2	V	V1 = 0, V2 = 0.7V
VDD	Supply Voltage	V	VDD = 0.7V