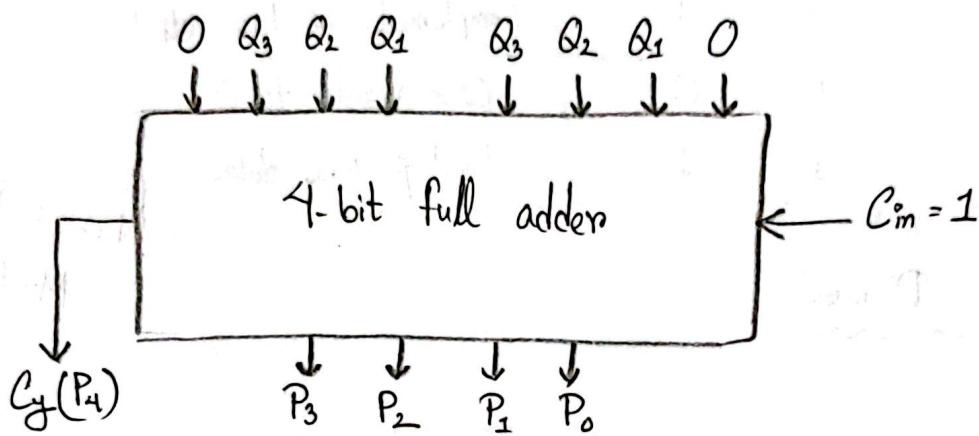


Subject _____

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2.(a) Input : 3-bit input $Q(Q_2, Q_1, Q_0)$ Output : 5-bit output $P(P_4, P_3, P_2, P_1, P_0)$, $P = 3^*Q + 1$ Working Procedure:

- For the first input, we input Q , so output $P = Q$.
- Now if we left shift a binary value once we get the double of that value. So, for the second input we left shift Q once. So, output $P = Q + 2^*Q = 3^*Q$.
- If we set carry input as 1, we will get $P = 3^*Q + 1$.

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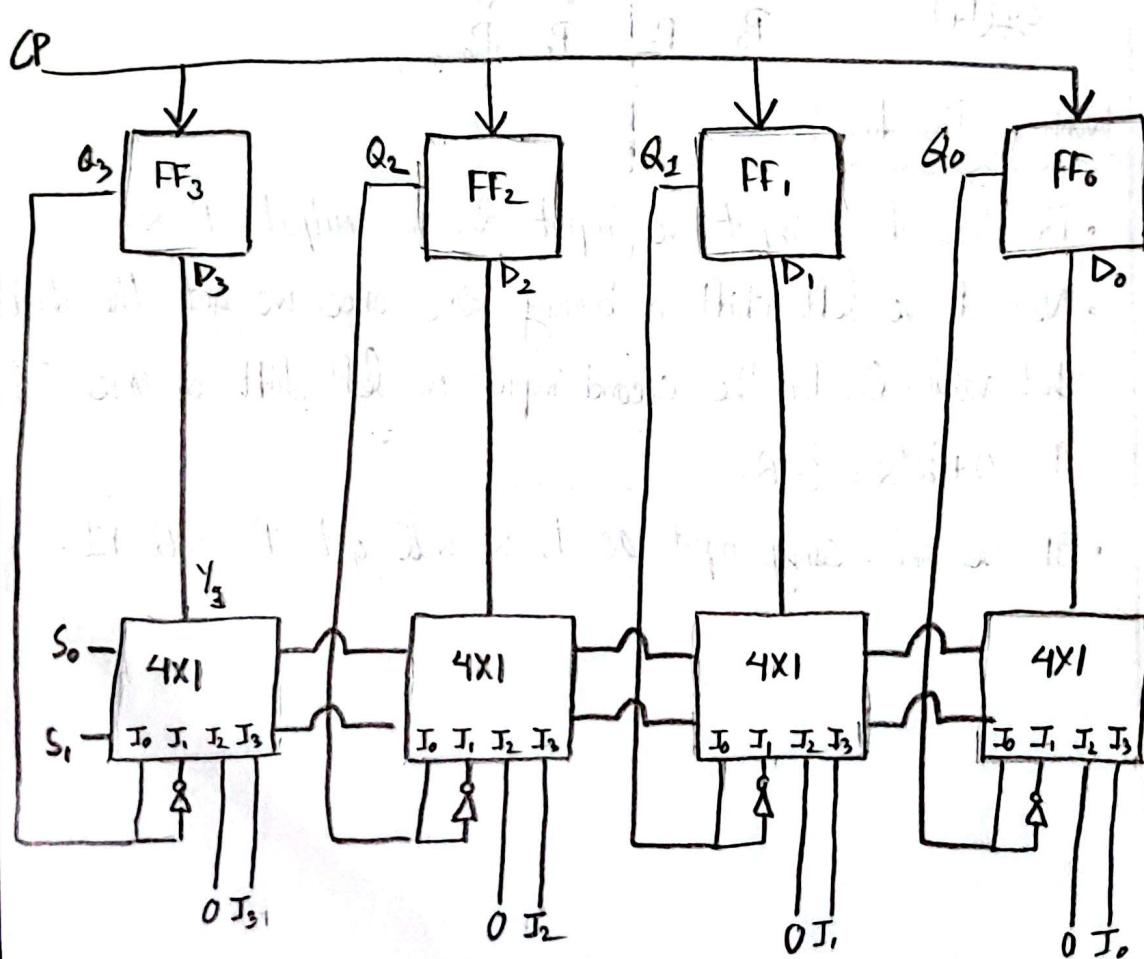
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~~2.0(C)~~Function Table:

Mode Control		Register Operation
S_1	S_0	
0	0	No change
0	1	Complement the four outputs
1	0	Clear register to 0
1	1	Load parallel data

Working Procedure
Must

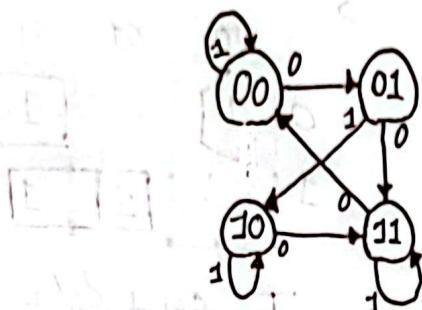
Circuit Diagram:

Subject _____

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0	0	0	0	0	0	0

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2.(d) State diagram:



State table:

Present State			Next State	
S	Q_0	Q_1	Q_0	Q_1
0	0	0	0	1
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	0	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Excitation Map:

Present State			Next State		FF's inputs	
S	Q_0	Q_1	Q_0	Q_1	T_0	T_1
0	0	0	0	1	0	1
0	0	1	1	1	1	0
0	1	0	1	1	0	1
0	1	1	0	0	1	1
1	0	0	0	0	0	0
1	0	1	1	0	1	1
1	1	0	1	0	0	0
1	1	1	1	1	0	0

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For T_0 ,

$S Q_0 Q_1$	00	01	11	10
0	0	1	1	
1	1			

$$T_0 = Q'_0 Q_1 + S' Q, \\ = Q_1 (Q'_0 + S')$$

For T_1 ,

$S Q_0 Q_1$	00	01	11	10
0	1		1	1
1	1	1		

$$T_1 = S' Q'_1 + S' Q_0 + S Q'_0 Q_1 \\ = S' (Q'_1 + Q_0) + S Q'_0 Q_1$$

Circuit Diagram:

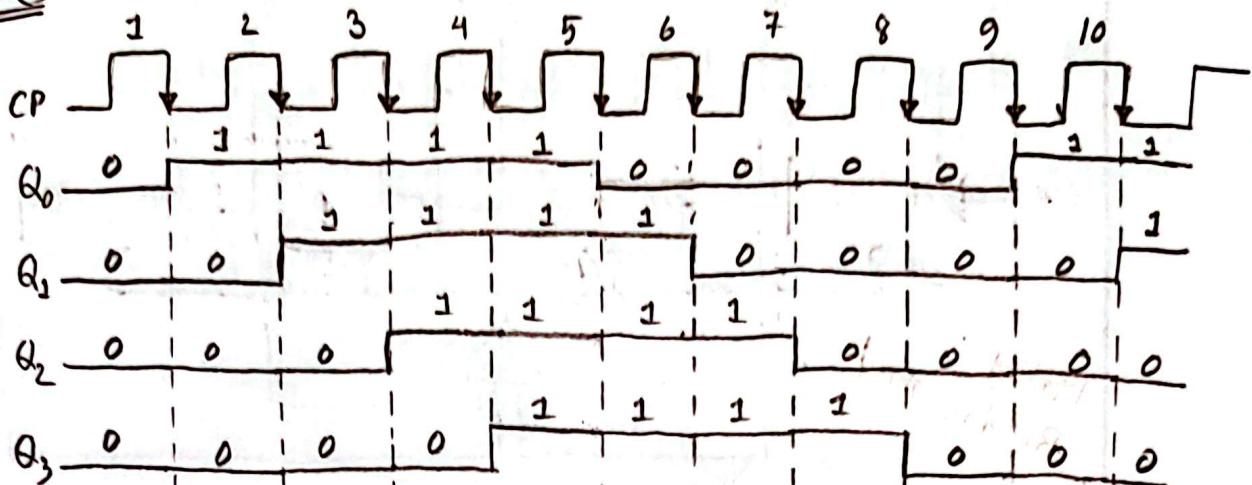


Logic block diagram

Subject _____

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0	0	0	0	0	0	0

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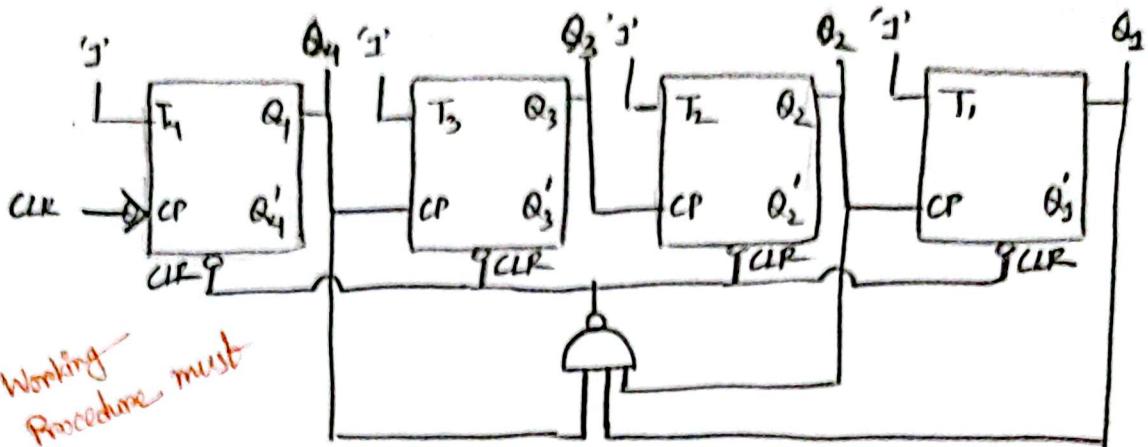
3.(a)3.(b) State table:

Present State	Next State
Q_4 Q_3 Q_2 Q_1	Q_4 Q_3 Q_2 Q_1
0 0 0 0	0 0 0 1
0 0 0 1	0 0 1 0
0 0 1 0	0 0 1 1
0 0 1 1	0 1 0 0
0 1 0 0	0 1 0 1
0 1 0 1	0 1 1 0
0 1 1 0	0 1 1 1
0 1 1 1	1 0 0 0
1 0 0 0	1 0 0 1
1 0 0 1	1 0 1 0
1 0 1 0	0 0 0 0
1 0 1 1	X X X X

Subject _____

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<input type="radio"/>						

Date : / /



3.(c) Given data = "100101010101"

The no. of data bits in the message, $n = 12$

Let, required parity bits = p .

$$\therefore 2^p \geq n+p+1$$

if $p=1$, $2^1 \geq 12+1+1$ (false).

if $p=2$, $2^2 \geq 12+2+1$ (false)

if $p=3$, $2^3 \geq 12+3+1$ (false)

if $p=4$, $2^4 \geq 12+4+1$ (false)

if $p=5$, $2^5 \geq 12+5+1$ (true)

So, $p=5$. We have to send total ~~17~~ $12+5=17$ bits.

Sending End: Original message : "100101010101"
 $m=12$ bits, with parity bits

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0	0	0	0	0	0	0

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Bit position : 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17

values : P₁ P₂ 1 P₃ 0 0 1 P₄ 0 1 0 1 0 1 0 P₅ 1

To find values of P₁, P₂, P₃, P₄, P₅ we have to XOR the binary values of bit position holding 1's.

0 0 0 1 1 (3)

0 0 1 1 1 (7)

0 1 0 1 0 (10)

0 1 1 0 0 (12)

0 1 1 1 0 (14)

1 0 0 0 1 (17)

$$\begin{array}{r}
 (\text{XOR}) \\
 \hline
 1 & 1 & 1 & 0 & 1 \\
 \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\
 P_5 & P_4 & P_3 & P_2 & P_1
 \end{array}$$

So, the sending message will be:

10110011010101011.

Receiving End:
Message

Case 01 → If there is no error in message transmitting, the receiver will get: 10110011010101011

To check receiver will XOR the binary values of the bit positions having 1's in the received message again & XOR results will be all 0s.

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0 0 0 0 1 (1)
 0 0 0 1 1 (3)
 0 0 1 0 0 (4)
 0 0 1 1 1 (4)
 0 1 0 0 0 (8)
 0 1 0 1 0 (10)
 0 1 1 0 0 (12)
 0 1 1 1 0 (14)
 1 0 0 0 0 (16)
 1 0 0 0 1 (17)

(XOR) 0 0 0 0 0

As the result is 0(0000), there
is no errors in the message.

Case #02 → If there is an error in the 6th position while transmitting,
the receiver will get : 10110111010101011

To check:

0 0 0 0 1 (1)
 0 0 0 1 1 (3)
 0 0 1 0 0 (4)
 0 0 1 ~~0~~¹ (6)
 0 0 1 1 1 (7)
 0 1 0 0 0 (8)
 0 1 0 1 0 (10)
 0 1 1 0 0 (12)
 0 1 1 1 0 (14)
 1 0 0 0 0 (16)
 1 0 0 0 1 (17)

(XOR) 0 0 1 1 0 (6)

So, there is an error in the
6th position. The correct message
will be : "1011011010101011".

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1.(c)

$$F(w, x, y, z) = \sum(0, 1, 2, 8, 10, 11, 14, 15)$$

$$= (0000, 0001, 0010, 1000, 1010, 1011, 1110, 1111)$$

Determination of Prime Implicants:

	Column I	Column II	Column III
Group 0	0 0000✓	(0,1) 000-	(0,2,8,10) -0-0
Group 1	1 0001✓	(0,2) 00-0✓	
	2 0010✓	(0,8) -000✓	(10,11,14,15) 11-1-
	8 1000✓	(2,10) -010✓	
Group 2	10 1010✓	(8,10) 10-0✓	
Group 3	11 1011✓	(10,11) 101-✓	
	14 1110✓	(10,14) 1-10✓	
Group 4	15 1111✓	(11,15) 1-11✓	
		(14,15) 111-✓	

\therefore Prime implicants: ~~wxyz + w'x'y' + wy + x'z' + w'x'y'~~ $wy + x'z' + w'x'y'$

Selection of Prime implicants:

PIs	w x y z	0	1	2	8	10	11	14	15
(0,2,8,10)	- 0 - 0	x		(X)	(X)	x			
(10,11,14,15)	1 - 1 -					x	(X)	(X)	(X)
(0;1)	0 0 0 -	x	(X)						

$$\therefore f = wy + x'z' + w'x'y' \text{ (Ans)}$$

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Spring 2022

1.(c) Given message : "101110110"The no. of bits in the message, $n = 9$ Let, required parity bits = p

$$\therefore 2^p \geq n+p+1$$

If $p=1$, $2^1 \geq 9+1+1$ (false)

If $p=2$, $2^2 \geq 9+2+1$ (false)

If $p=3$, $2^3 \geq 9+3+1$ (false)

If $p=4$, $2^4 \geq 9+4+1$ (true)

So, $p=4$. We have to send total $9+4=13$ bits.

Sending End:

Original message : "101110110"

 $n = 9$ bits, with parity bits.

Bit position : 1 2 3 4 5 6 7 8 9 10 11 12 13

values : $P_1 P_2 P_3 P_4$ 1 1 0 1 0 1 1 0To find values of P_1, P_2, P_3 and P_4 we have to ~~not~~ XOR the binary values of bit position holding 1's.

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0	0	0	0	0	0	0

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0011(3)

0110(6)

0111(7)

1001(9)

1011(11)

1100(12)

$$\begin{array}{r} \text{(XOR)} \\ \hline 1100 \\ \downarrow \quad \downarrow \quad \downarrow \\ P_4 \quad P_3 \quad P_2 \quad P_1 \end{array}$$

So, the sending message: 0011011110110.

Receiving End:

Case 1 → If there is no error in message transmitting,

the receiver will get: 0011011110110.

To check, receiver will XOR the binary values of bit positions having 1's in the received message again & XOR results will be 0.

0011(3)

0100(4)

0110(6)

0111(7)

1000(8)

1001(9)

1011(10)(11)

1100(12)

$$\begin{array}{r} \text{(XOR)} \\ \hline 0000 \end{array}$$

As the result is 0(0000), there is no errors in the message.

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Case 2 → If there is an error in the 6th position while transmitting, receiver will get : 0011001110110.

To check,

$$\begin{array}{r}
 0011(3) \\
 0100(4) \\
 0111(7) \\
 1000(8) \\
 1001(9) \\
 1011(11) \\
 \underline{1100(12)} \\
 (\text{xor}) 0110(6)
 \end{array}$$

So, -there is an errors in the 6th position in the received message.
The correct output will be:
"0011011110110".

2.(b)

$$F = (w, x, y, z) = \sum (0, 1, 2, 8, 10, 11, 14, 15)$$

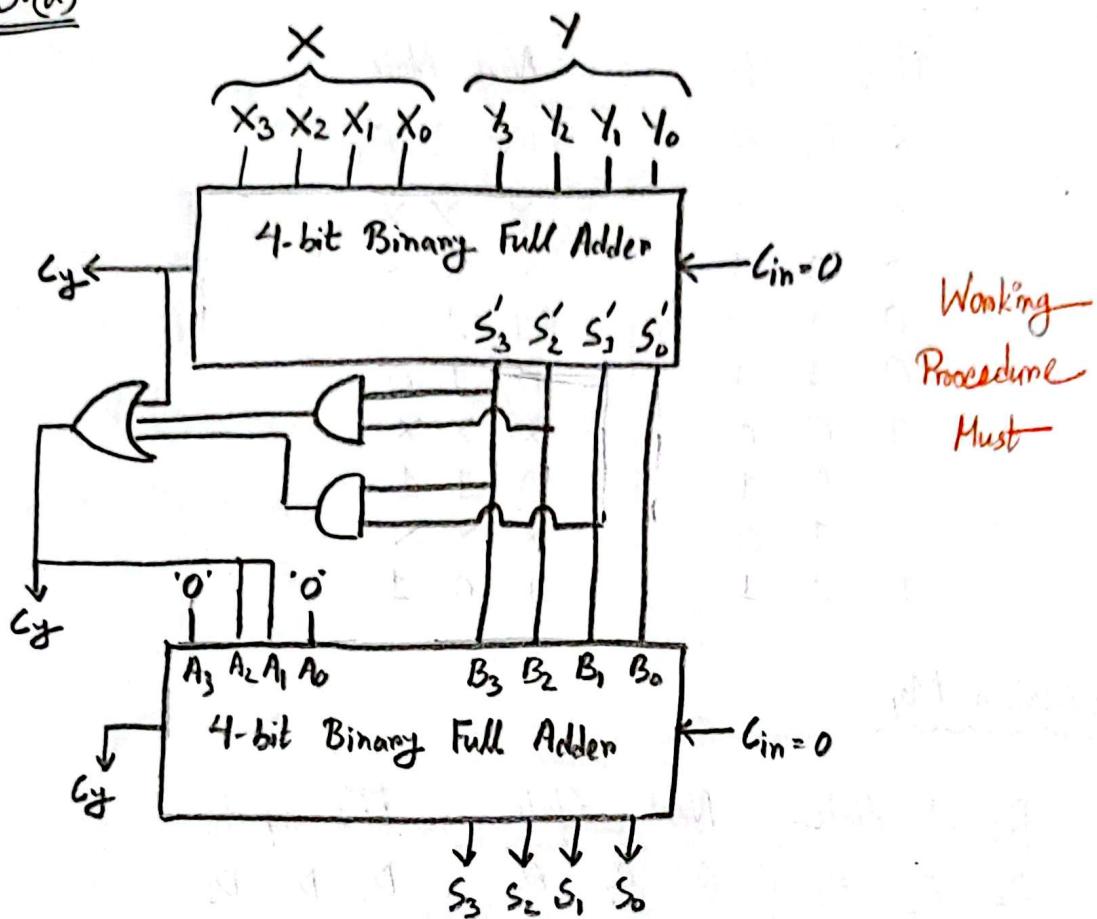
Spring 2023 I(c) — Same

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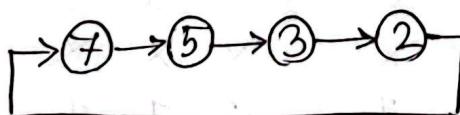
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Q. (a)



Q. (b)

State Diagram:



X Y S C_y

Σ B_3 B_2 B_1 B_0 S_3 S_2 S_1 S_0

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State Table :

Present State			Next State		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1
0	0	0	X	X	X
0	0	1	X	X	X
0	1	0	1	1	1
0	1	1	0	1	0
1	0	0	X	X	X
1	0	1	0	1	1
1	1	0	X	X	X
1	1	1	1	0	1

Excitation Map :

Present State			Next State			FF's Inputs		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	D_3	D_2	D_1
0	0	0	X	X	X	X	X	X
0	0	1	X	X	X	X	X	X
0	1	0	1	1	1	1	1	1
0	1	1	0	1	0	0	1	0
1	0	0	X	X	X	X	X	X
1	0	1	0	1	1	0	1	1
1	1	0	X	X	X	X	X	X
1	1	1	1	0	1	1	0	1

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For D_3 ,

		$Q_2 Q_1$	00	01	11	10
		Q_3	X	X	1	1
$Q_2 Q_1$	00	X	X	1	1	
	01	X	1	X		

$$D_3 = Q_1 + Q_3 Q_2$$

For D_2 ,

		$Q_2 Q_1$	00	01	11	10
		Q_3	X	X	1	1
$Q_2 Q_1$	00	X	X	1	1	
	01	X	1	X		

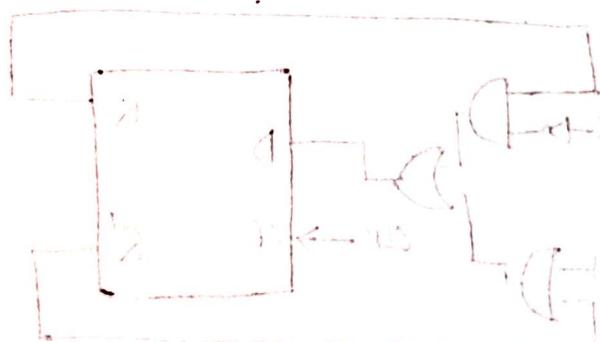
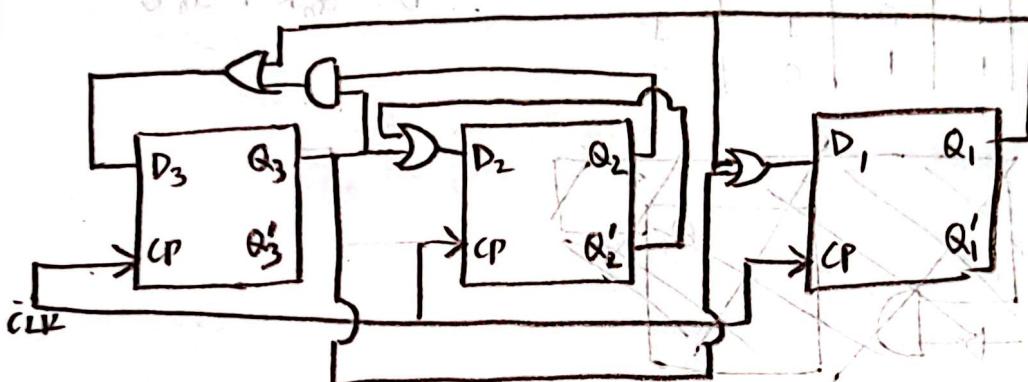
$$D_2 = Q_3 + Q_2'$$

For D_1 ,

		$Q_2 Q_1$	00	01	11	10
		Q_3	X	X	1	1
$Q_2 Q_1$	00	X	X	1	1	
	01	X	1	X		

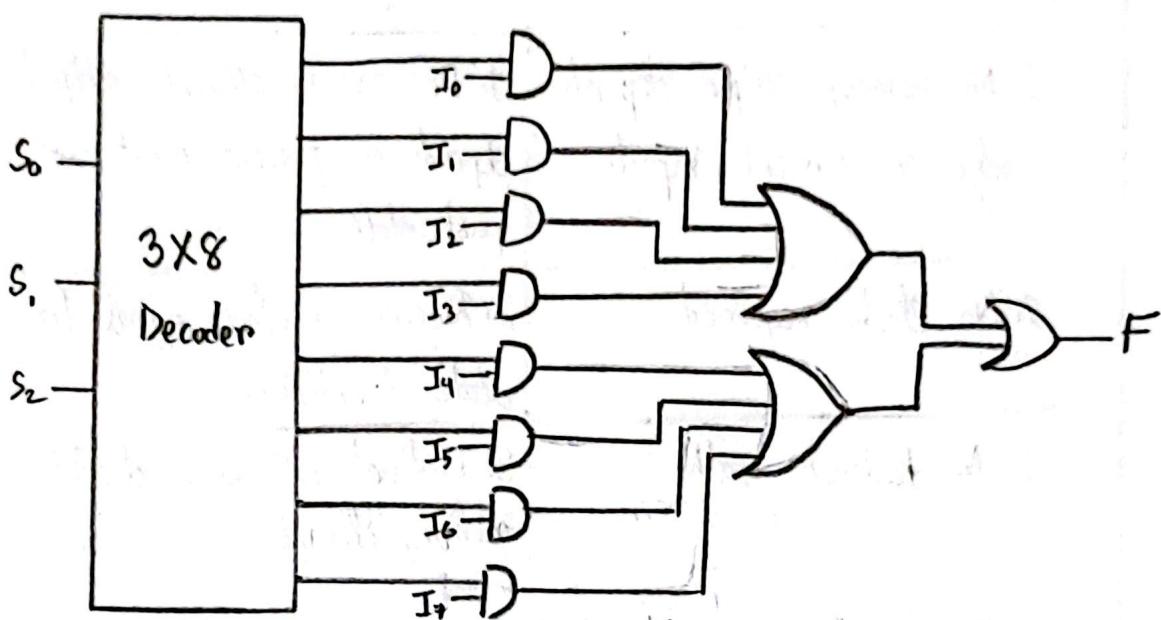
$$D_1 = Q_3 + Q_1'$$

Circuit Diagram:



5.(a)

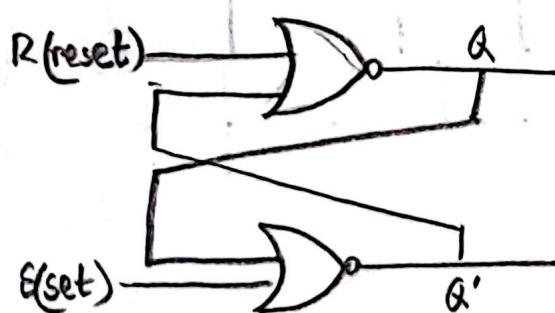
8×1 MUX using a 3×8 Decoder and basic logic gates:



Here, the inputs are $I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7$ and selections are S_0, S_1 and S_2 :

5.(b)

Basic Flip-Flop circuit with NAND gates:

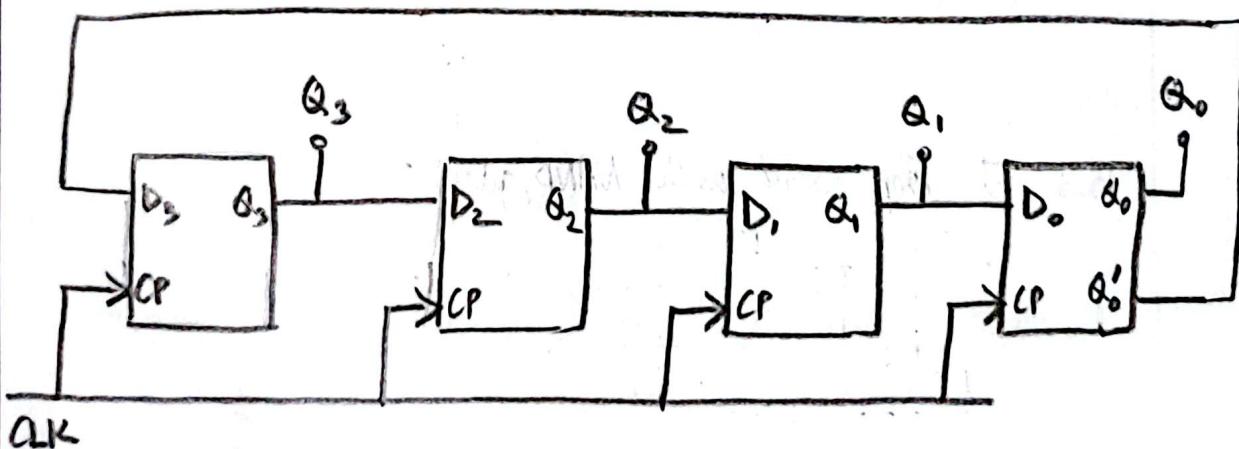


6.(a)

Difference between combinational and sequential circuit:

Combinational Circuit	Sequential Circuit
1. No memory output depends only on current inputs.	1. Has memory elements; output depends on present input & past state.
2. No clock required.	2. Requires a clock signal for state transitions.
3. No feedback path.	3. Feedback path exists due to memory elements.

Logic Diagram of 4-bit Johnson Counter:



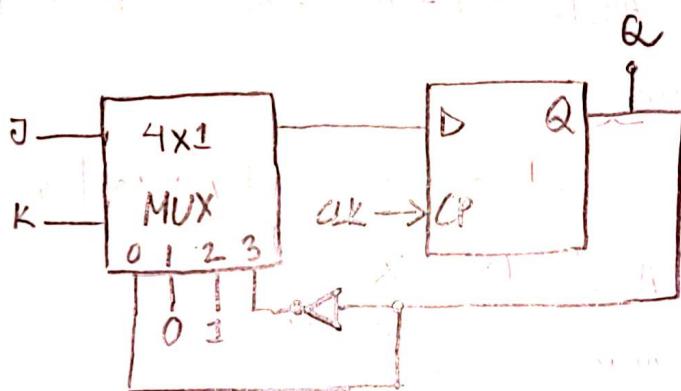
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Counting Sequence:

CP#	Q ₃	Q ₂	Q ₁	Q ₀
CP#0 →	0	0	0	0
CP#1 →	1	0	0	0
CP#2 →	1	1	0	0
CP#3 →	1	1	1	0
CP#4 →	1	1	1	1
CP#5 →	0	1	1	1
CP#6 →	0	0	1	1
CP#7 →	0	0	0	1
CP#8 →	0	0	0	0

7.(a)

Hence, J and K are the selectors.

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Fall 2021

$$\underline{2.(c)} \quad F(A, B, C, D) = \sum(0, 1, 5, 7, 10, 13, 15) \\ = \sum(0000, 0001, 0101, 0111, 1010, 1101, 1111)$$

Determinants of Prime Implicants:

Column I	Column II	Column III
Group 0 ✓ 0-0000	0, 1 - 000-	
Group 1 ✓ 1-0001	1, 5 - 0-01	
Group 2 ✓ 5-0101 10 - 1'010	✓ 5, 7 - 01-1 ✓ 5, 13 - 101	5, 7, 13, 15 - -1-1
Group 3 ✓ 7-0111 ✓ 13 - 1101	✓ 7, 15 - -111	
Group 4 ✓ 15-1111	✓ 13, 15 - 11-1	

∴ Prime Implicants: $AB'CD' + A'B'C' + A'C'D + B'D'$ Selection of Prime Implicants:

PIs	ABCD	0	1	5	7	10	13	15
(5, 7, 13, 15)	- 1 - 1			X	✗		✗	✗
(0, 1)	000 -	✗	X					
(1, 5)	0 - 0 1		X	X				
10	1010					✗		

$$\therefore F = AB'CD' + A'B'C' + B'D' \text{ (Ans)}$$

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3.(a) Draw truth table of Full Adder first

Full Adder using two 4x1 multiplexers.

$$\text{In case of full adder, } \text{Sum} = \sum(1, 2, 4, 7)$$

$$\text{Carry} = \sum(3, 5, 6, 7)$$

For Sum,

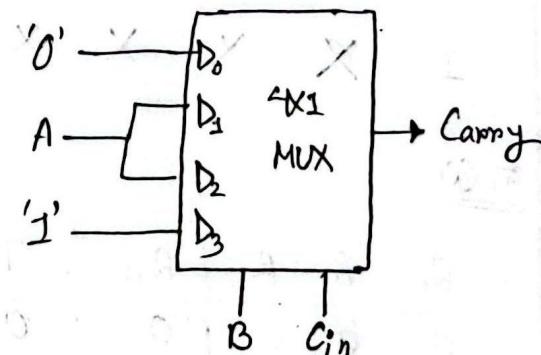
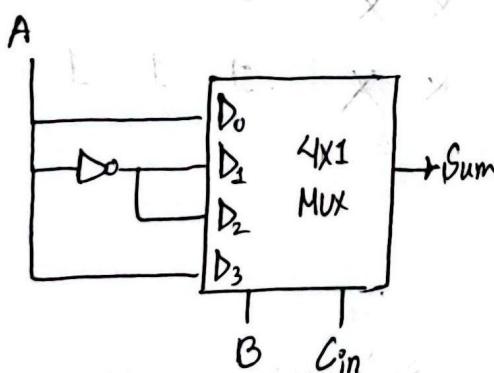
Implementation Table:

MUX input	D ₀	D ₁	D ₂	D ₃
A'	0	(1)	(2)	3
A	(4)	5	6	(7)
Input value	A	A'	A'	A

For Carry,

Implementation Table:

Mux input	D ₀	D ₁	D ₂	D ₃
A'	0	1	2	(3)
A	4	(5)	(6)	(7)
Input value	0	A	A	1



Date out from the test
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0 0 0 0 0 0 0

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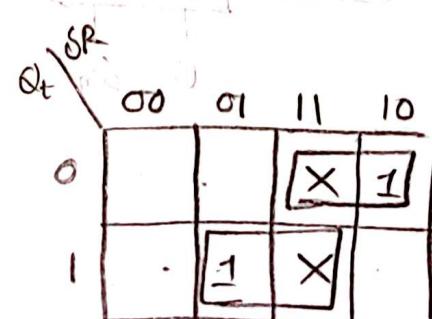
3.(a)

Priority ^{order} : $I_4 > I_3 > I_0 > I_1 > I_2 > I_5 > I_6 > I_7$

I_4	I_3	I_0	I_1	I_2	I_5	I_6	I_7	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	X	X	X
0	0	0	0	0	0	0	1	1	1	1
0	0	0	0	0	0	1	X	1	1	0
0	0	0	0	0	1	X	X	1	0	1
0	0	0	0	1	X	X	X	0	1	0
0	0	0	1	X	X	X	X	0	0	0
0	0	1	X	X	X	X	X	0	1	1
0	1	X	X	X	X	X	X	0	1	1
1	X	X	X	X	X	X	X	1	0	0

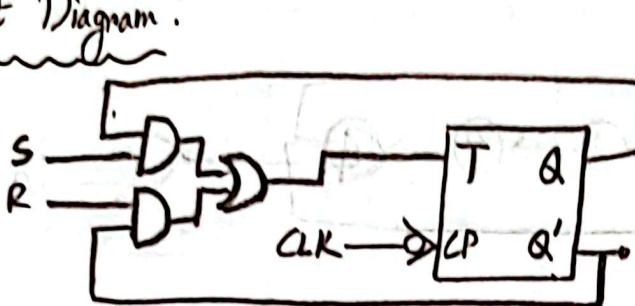
5.(a)

Q_t	S	R	Q_{t+1}	T
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	X	X
1	0	0	01	0
1	0	1	0	1
1	1	0	1	0
1	1	1	X	X



$$\therefore T = Q_t' S + Q_t R$$

~~Ans~~

Circuit Diagram:~~Ans~~
5.(b)

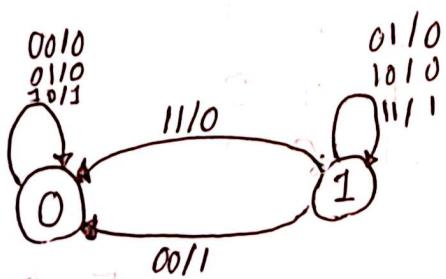
Q_n	x	y	Q_{n+1}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Q_n	xy	00	01	11	10
0			1		1
1		1			1

$$\therefore S = x \oplus y \oplus Q_n$$

Q_n	xy	00	01	11	10
0			1		1
1		1		1	1

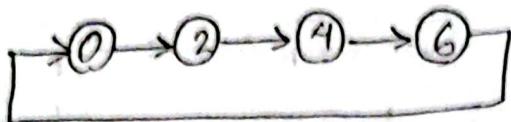
$$\begin{aligned} \therefore Q_{n+1} &= Q_n y + xy + Q_n x \\ &= Q_n(x+y) + xy \end{aligned}$$



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5.(c) State diagram :State table :

Present State			Next State		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1
0	0	0	0	1	0
0	1	0	1	0	0
1	0	0	1	1	0
1	1	0	0	0	0

Excitation Map :

Present State			Next State			FF inputs		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	D_3	D_2	D_1
0	0	0	0	1	0	0	1	0
0	1	0	1	0	0	1	0	0
1	0	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0	0

For D_3 ,

Q_3	00	01	11	10
0	0 X X 1	1 X X 1		
1	1 X X 1	1 X X 1		

$$D_3 = Q_3' Q_2 + Q_3 Q_2'$$

.....

For D_2 ,

Q_3	00	01	11	10
0	1 X X .	1 X X .		
1	1 X X .	1 X X .		

$$D_2 = Q_2'$$

For D_1 ,

Q_3	00	01	11	10
0	X X X .	X X X .		
1	X X X .	X X X .		

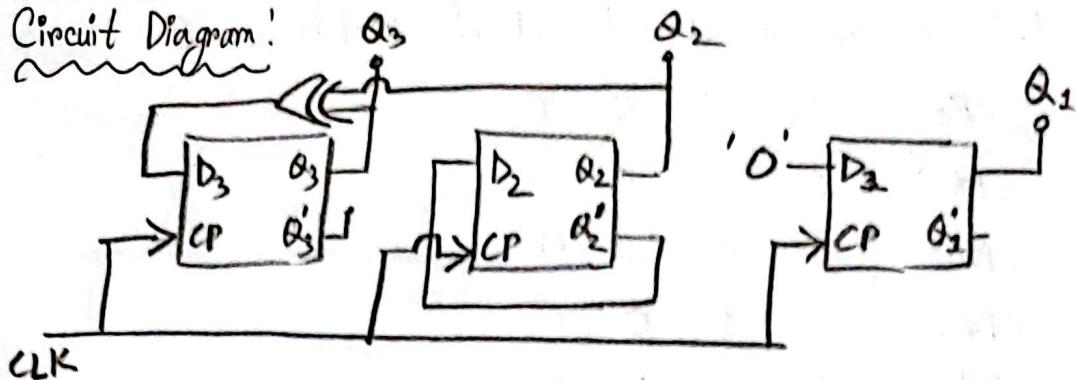
$$D_1 = 0$$

Subject _____

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Circuit Diagram:



6.(a)

Difference between serial and parallel transfer:

In serial transfer bits are sent one after another and in parallel transfer multiple bits are sent simultaneously. Serial transfer is slower and less complex compared to parallel transfer.

Conversion serial data to parallel data:

We need to receive serial data bit by bit and store these bits in a register. After all bits arrive, output them simultaneously as parallel data.

We would need a "Serial-In Parallel-Out (SIPO) Shift Register".

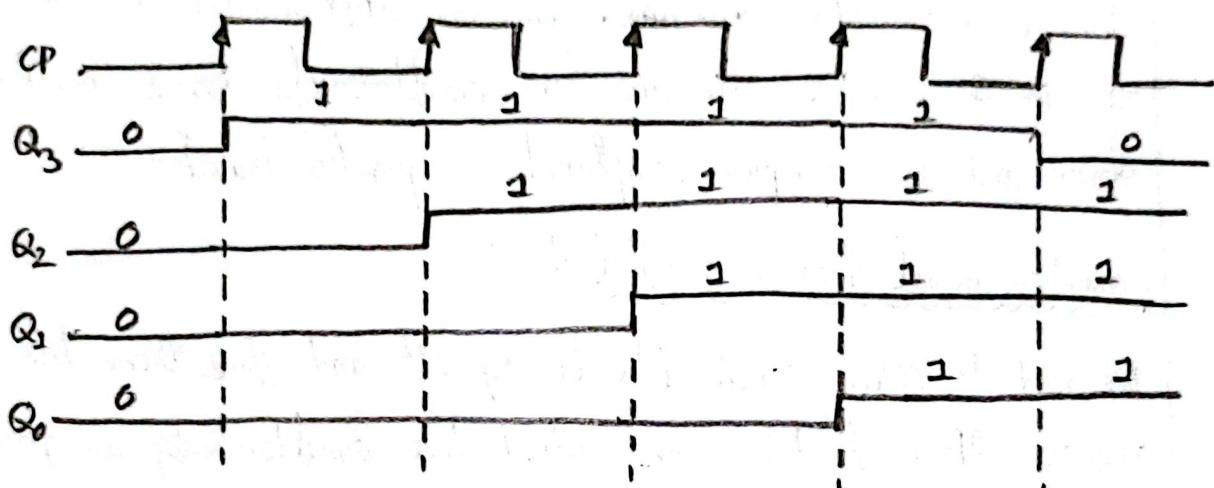
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Q.(b) Let's assume initial value of all 4 bits as 0.

CP#	Q_3	Q_2	Q_1	Q_0
CP#0	0	0	0	0
CP#1	1	0	0	0
CP#2	1	1	0	0
CP#3	1	1	1	0
CP#4	1	1	1	1
CP#5	0	1	1	1

Q.(c)

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7(a)

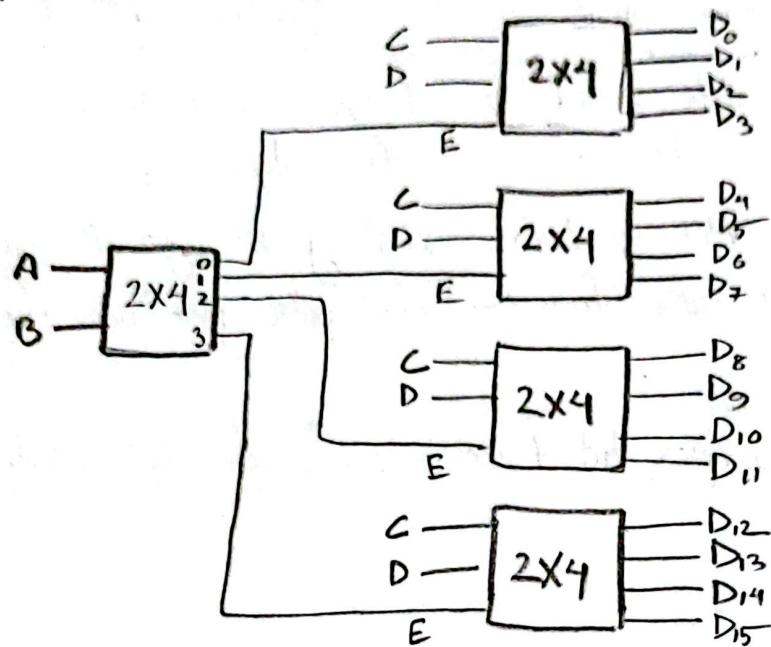
Difference between asynchronous and synchronous circuit:

Asynchronous Circuit	Synchronous Circuit
1. Changes state immediately when inputs change.	1. Changes state only at clock edges.
2. Only the MSB or LSB gets clock pulse from a clock.	2. Every bits get the same clock pulse from same clock.
3. More complex but faster.	3. Less complex but slower.

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Spring 20212.(b) 4x16 Decoder using 2x4 Decoder:5.(a) State Table:

Present State				Next State		
S	Q_3	Q_2	Q_1	Q_3	Q_2	Q_1
0	0	1	0	0	1	1
0	0	1	1	1	0	1
0	1	0	1	1	1	1
0	1	1	1	0	1	0
1	0	1	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	0	1	1
1	1	1	1	1	0	1

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0	0	0	0	0	0	0

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Excitation Map :

Present State	Next State			↓ FF Inputs					
	\bar{Q}_3	Q_2	Q_1	\bar{J}_3	K_3	\bar{J}_2	K_2	\bar{J}_1	K_1
$S \ Q_3 \ Q_2 \ Q_1$	$\bar{Q}_3 \ Q_2 \ Q_1$			0	x	x	0	1	x
0 0 1 0	0 1 1			1	x	x	1	x	0
0 0 1 1	1 0 1			x	0	1	x	x	0
0 1 0 1	1 1 1			x	1	x	0	x	1
0 1 1 1	0 1 0			1	x	x	0	1	x
1 0 1 0	1 1 1			0	x	x	0	x	1
1 0 1 1	0 1 0			1	x	x	0	x	0
1 1 0 1	0 1 1			x	0	1	x	x	0
1 1 1 1	1 0 1			x	0	x	1	x	0

For \bar{J}_3 ,

SQ_3	00	01	11	10
$SQ_2 \bar{Q}_1$	X	X	1	0
00	X	X	X	X
01	X	X	X	X
11	X	1	X	X
10	X	X	0	1

$$\begin{aligned} \therefore \bar{J}_3 &= S'Q_1 + Q_3Q_1 + SQ_2\bar{Q}_1 \\ &= Q_1(S' + Q_3) + SQ_2\bar{Q}_1 \end{aligned}$$

For ~~\bar{J}_2~~ \bar{J}_2

SQ_3	00	01	11	10
$SQ_2 \bar{Q}_1$	X	X	X	X
00	X	X	X	X
01	X	1	X	X
11	X	1	X	X
10	X	X	X	X

~~∴ $\bar{J}_2 = 1$~~ $\therefore \bar{J}_2 = 1$

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For J_1 ,

$SQ_3 Q_2 Q_1$

00	01	11	10
00	X	X	X
01	X	X	X
11	X	X	X
10	X	X	-1

$$J_1 = 1$$

For K_2 ,

$SQ_3 Q_2 Q_1$

00	01	11	10
00	X	-1	-
01	X	X	X
11	X	X	-1
10	X	X	-

$$\therefore K_2 = SQ_3 + S'Q_3'Q_1$$

For K_3 ,

$SQ_3 Q_2 Q_1$

00	01	11	10
00	X	X	X
01	X	-1	X
11	X	-1	X
10	X	X	X

$$\therefore K_3 = S + Q_2$$

For K_1 ,

$SQ_3 Q_2 Q_1$

00	01	11	10
00	X	X	X
01	X	-	X
11	X	-	X
10	X	X	-1

$$\therefore K_1 = S'Q_3 + S'Q_3'Q_2$$

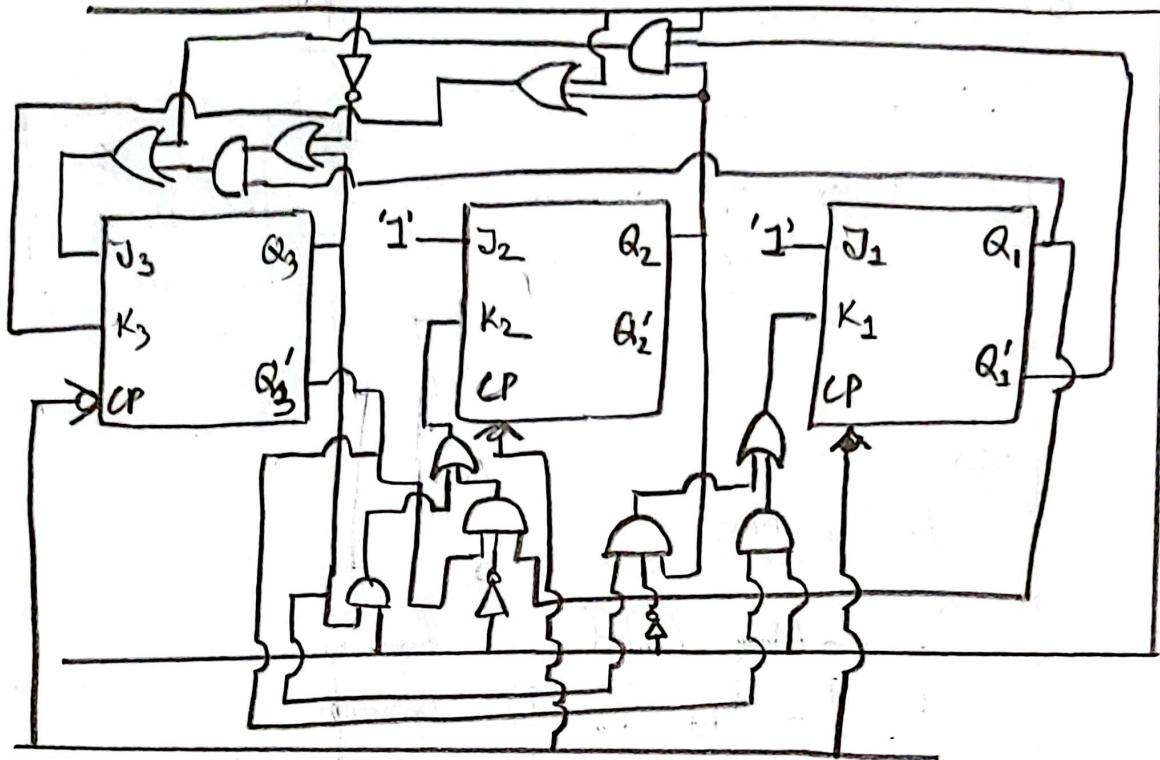
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Circuit Diagram:

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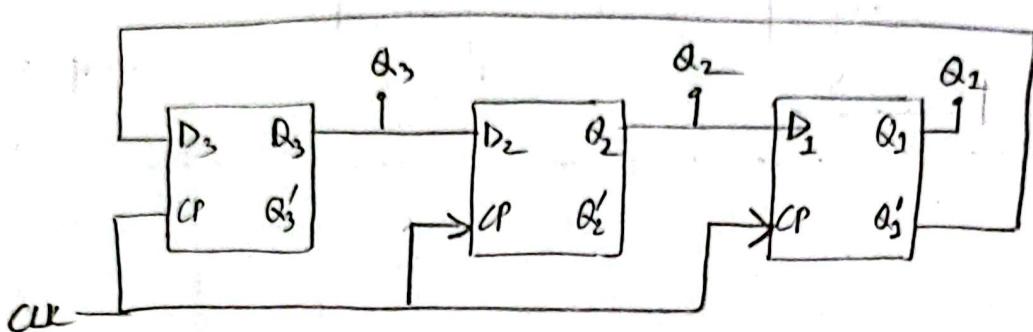
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5.(b)

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6.(a)Circuit Diagram:Working Procedure
Must7.(a)Function Table:

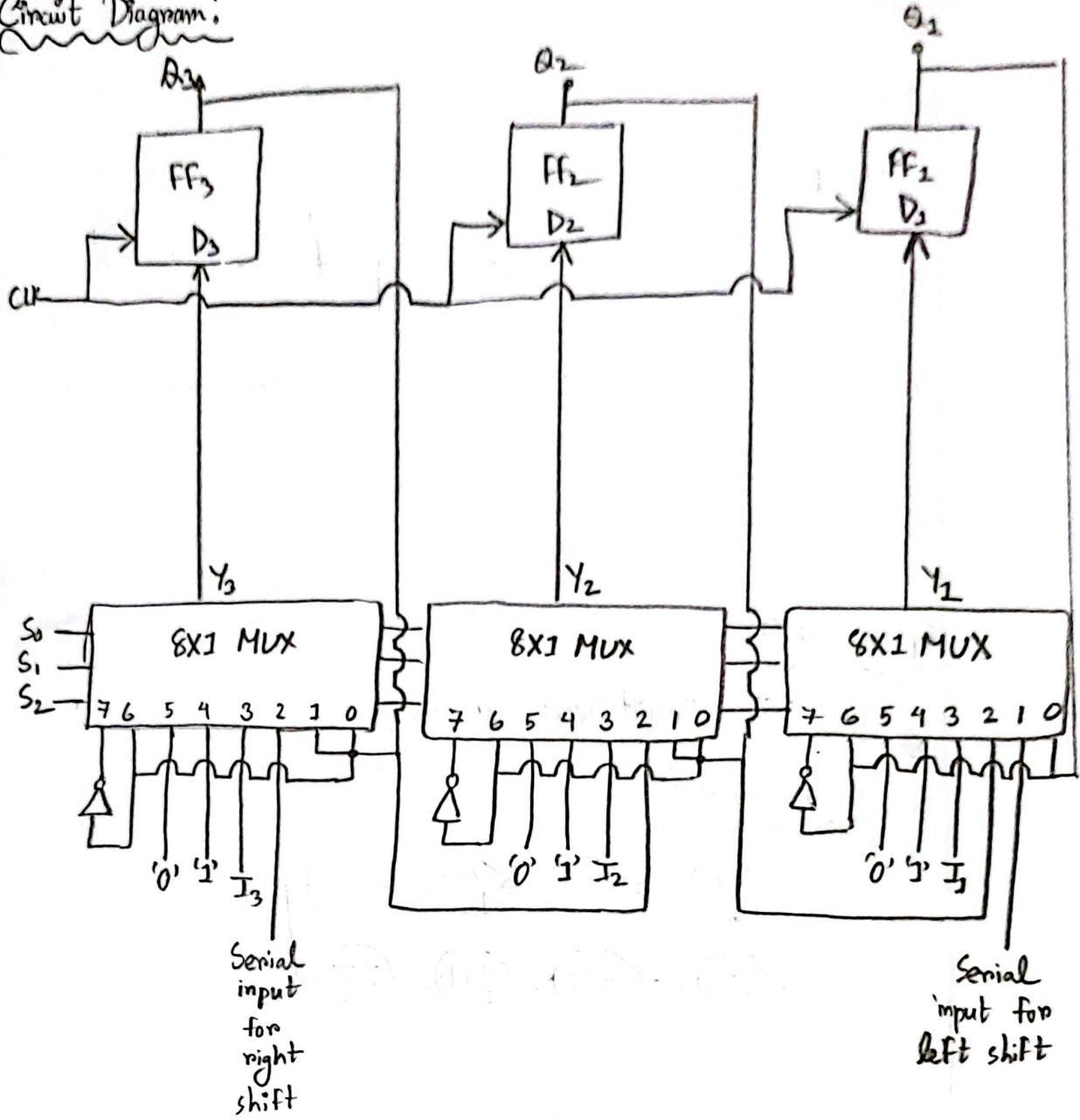
Mode Control			Registers Operation
S_2	S_1	S_0	
0	0	0	No change
0	0	1	Shift left
0	1	0	Shift right
0	1	1	Parallel Load
1	0	0	Set all bits to 1
1	0	1	Set all bits to 0
1	1	0	No change
1	1	1	Invert all bits

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Circuit Diagram:

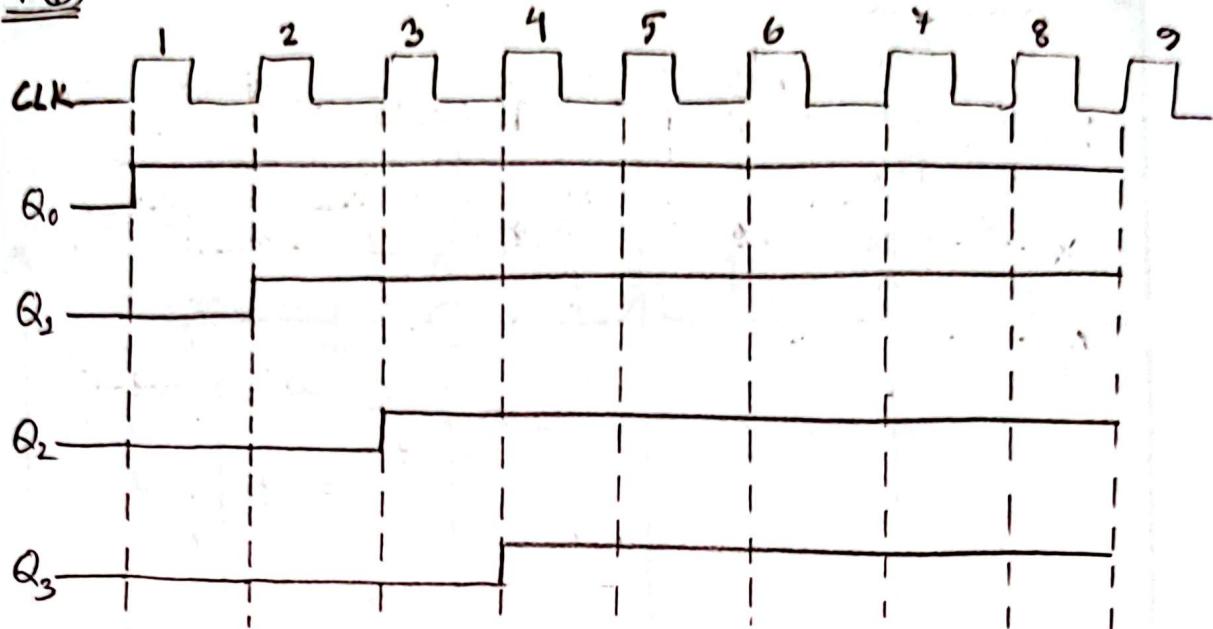


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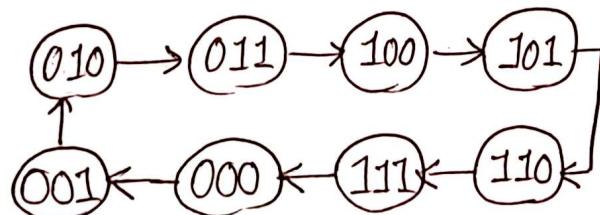
7.(b)



Spring 2019

7.(b) This circuit works as binary up counter

State diagram:



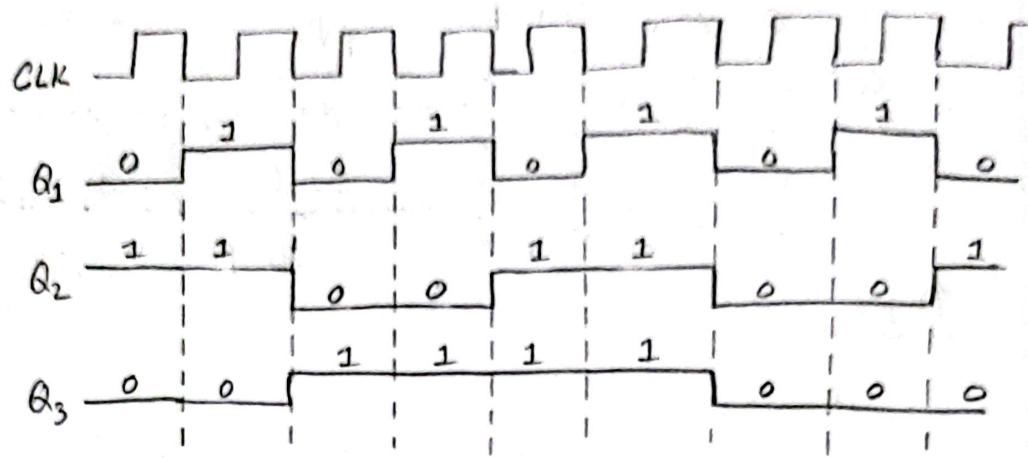
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Timing Diagram:



1.(c)

D FF from JK FF:

D	Q _n	Q _{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

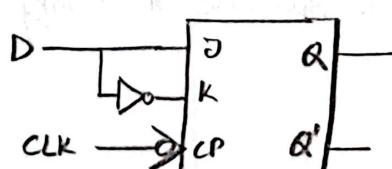
D	Q _n	1	X
0	0	X	1
1	1	1	X

D	Q _n	1	X
0	0	X	1
1	1	1	X

$$\therefore J = D$$

$$\therefore K = D'$$

Diagram:



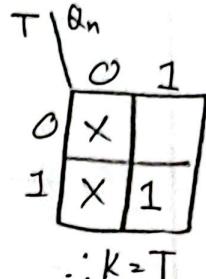
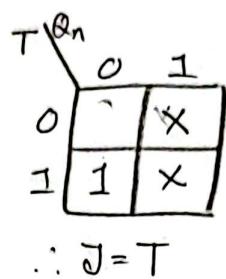
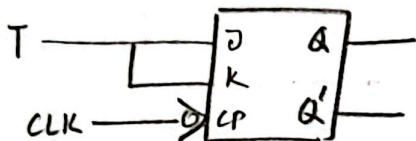
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T FF from JK FF:

T	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

Diagram:2(a)

A ring counter is a type of shift register where the output of the last flip-flop is fed back to the input of the first flip-flop.

In the given circuit, there are three T-flip flops. The output (Q_1) of the first FF is connected to the input of the second FF. The output (Q_2) of the second FF is connected to the input of the third FF. The output (Q_3) of the third FF is fed back to the first FF. This feed back confirms the basic structure of a ring counter.

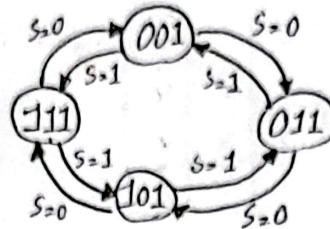
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0	0	0	0	0	0	0

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2.(c) State diagram:



State table:

Present State				Next State		
S	Q ₃	Q ₂	Q ₁	Q ₃	Q ₂	Q ₁
0	0	0	1	0	1	1
0	0	1	1	1	0	1
0	1	0	1	1	1	1
0	1	1	1	0	0	1
1	0	0	1	1	1	1
1	0	1	1	0	0	1
1	1	0	1	0	1	1
1	1	1	1	1	0	1

Excitation Map:

Present State				Next State			FF inputs					
S	Q ₃	Q ₂	Q ₁	Q ₃	Q ₂	Q ₁	J ₃	K ₃	J ₂	K ₂	J ₁	K ₁
0	0	0	1	0	1	1	0	x	1	x	x	0
0	0	1	1	1	0	1	1	x	x	1	x	0
0	1	0	1	1	1	1	x	0	1	x	x	0
0	1	1	1	0	0	1	x	1	x	1	x	0
1	0	0	1	1	1	1	01	x	1	x	x	0
1	0	1	1	0	0	1	0	x	x	1	x	0
1	1	0	1	0	1	1	x	1	1	x	x	0
1	1	1	1	1	0	1	x	0	x	1	x	0

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For J_3 ,

SQ_3	$Q_2 Q_1$	00	01	11	10
00	X	1	X		
01	X	X	X	X	
11	X	X	X	X	
10	X	1			X

$$\begin{aligned} \therefore J_3 &= SQ_2' + S'Q_2 \\ &= S \oplus Q_2 \end{aligned}$$

For J_2 ,

X	1	X	X
X	1	X	X
X	1	X	X
X	1	X	X

$$\therefore J_2 = 1$$

For J_1 ,

X	X	X	X
X	X	X	X
X	X	X	X
X	X	X	X

$$\therefore J_1 = 1$$

For K_3 ,

SQ_3	$Q_2 Q_1$	00	01	11	10
00	X	X	X	X	
01	X	.	1	X	
11	X	1		X	
10	X	X	X	X	

$$\begin{aligned} \therefore K_3 &= SQ_2' + S'Q_2 \\ &= S \oplus Q_2 \end{aligned}$$

For K_2 ,

SQ_3	$Q_2 Q_1$	00	01	11	10
00	X	X	1	X	
01	X	X	1	X	
11	X	X	1	X	
10	X	X	1	X	

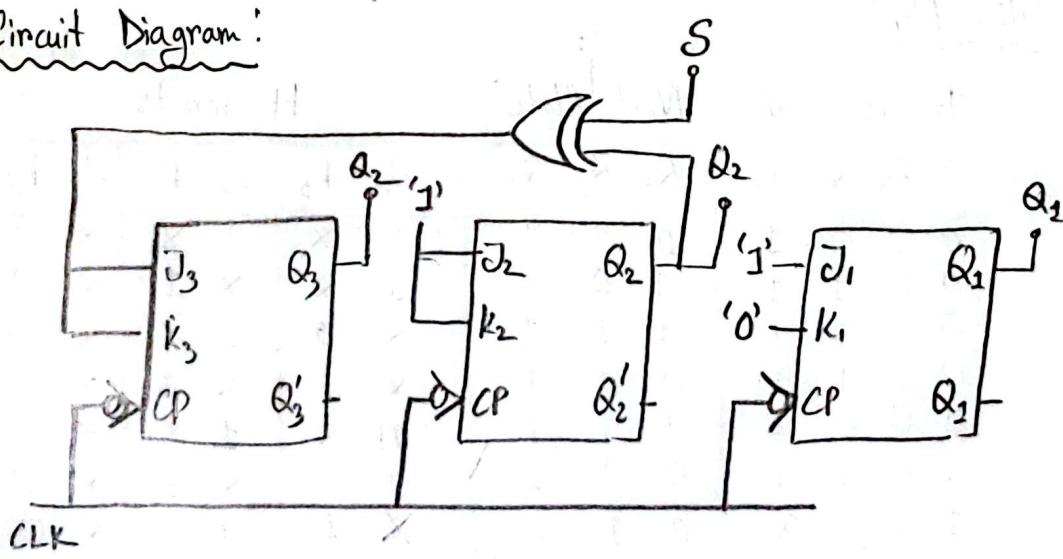
$$\therefore K_2 = 1$$

For K_1 ,

00	01	11	10
X			X
X			X
X			X
X			X

$$\therefore K_1 = 0.$$

Circuit Diagram:



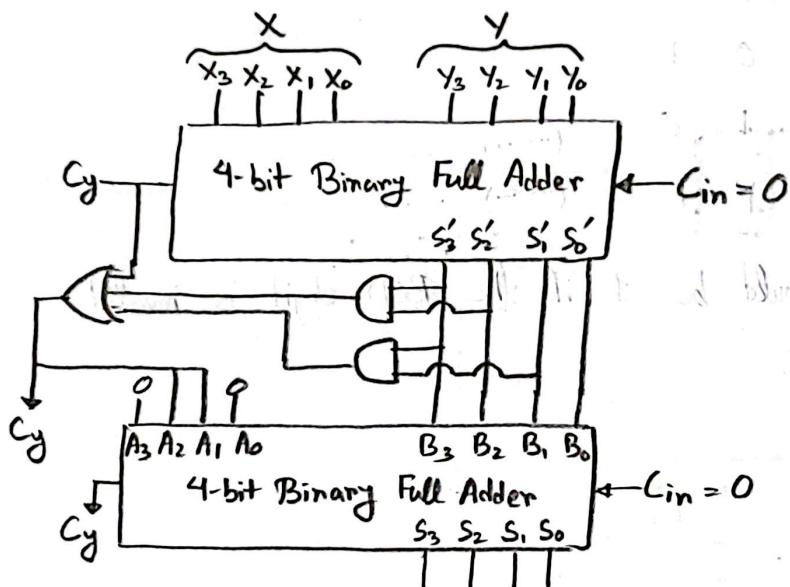
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0	0	0	0	0	0	0

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3.(c)4x16 Decoder using 2x4 Decoders:

Spring 2021 2(b)

5.(a)Circuit Diagram:

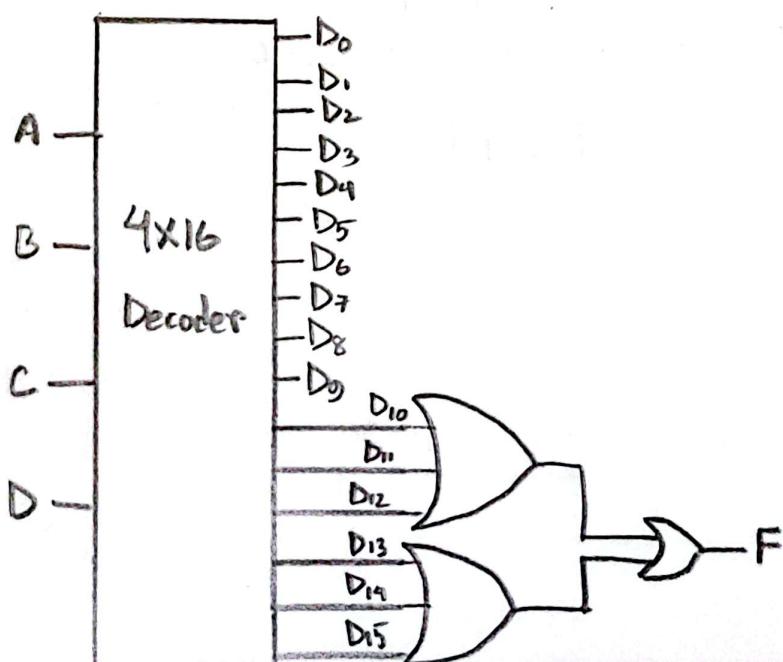
5.(c) BCD (Binary Coded Decimal) represents decimal number (0-9) using 4-bit binary codes. Valid BCD codes range from 0000(0) to 1001(9). Any binary combination 1010(10) to 1111(15) is invalid in BCD.

Invalid BCD conditions:

A	B	C	D
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

The output should be '1' if the BCD digit is invalid.

Circuit Diagram:



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0 0 0 0 0 0 0

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6.(b)

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7.(b)

Priority encoders are encoders with priority function. In this type of encoders, multiple inputs may be true simultaneously but the input with higher priority get precedence.

Given priority order : $I_1 < I_0 < I_3 < I_2$

I_2	I_3	I_0	I_1	Y_1	Y_0
0	0	0	0	X	X
0	0	0	1	0	1
0	0	1	X	0	0
0	1	X	X	1	1
1	X	X	X	1	0

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Fall - 2023

$$\text{Q. Q) } F(p, q, r, s) = \sum(3, 6, 8, 9, 10, 11, 14, 15) \\ = \sum(0011, 0110, 1000, 1001, 1010, 1011, 1110, 1111)$$

Determination of Prime Implicants:

	Column I	Column II	Column III
Group 1	$\checkmark 8 - 1000$	$\checkmark(8,9) - 100 -$	<u>(8,9,10,11) - 10--</u>
Group 2	$\checkmark 3 - 0011$ $\checkmark 6 - 0110$ $\checkmark 9 - 1001$ $\checkmark 10 - 1010$	$\checkmark(8,10) - 10-0$ $(3,11) - -001$ $(6,14) - -110$ $\checkmark(9,11) - 10-1$	<u>(10,11,14,15) - 1-1-</u>
Group 3	$\checkmark 11 - 1011$ $\checkmark 14 - 1110$	$\checkmark(10,11) - 101-$ $\checkmark(10,14) - 1-10$	
Group 4	$\checkmark 15 - 1111$	$\checkmark(11,15) - 1-11$ $\checkmark(14,15) - 111-$	

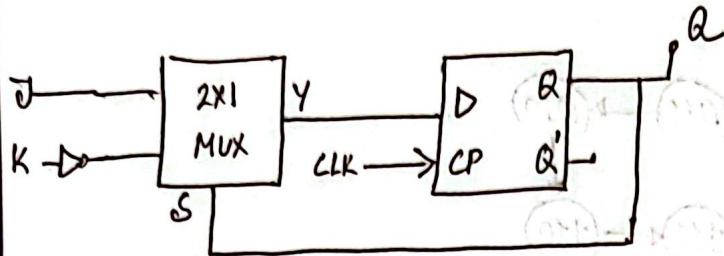
∴ Prime implicants: $pq' + pr + qr's + qr's'$

Selection of Prime Implicants:

PIs	$pqr's$	3	6	8	9	10	11	14	15
$(8,9,10,11)$	10--	pq'		\times	\times	\times			
$(10,11,14,15)$	1-1-	pr				x	x	x	\times
$(3,11)$	-001	$qr's$	\otimes				x		
$(6,14)$	-110	$qr's'$	\otimes					x	

∴ $f = pq' + pr + qr's + qr's'$ (Ans)

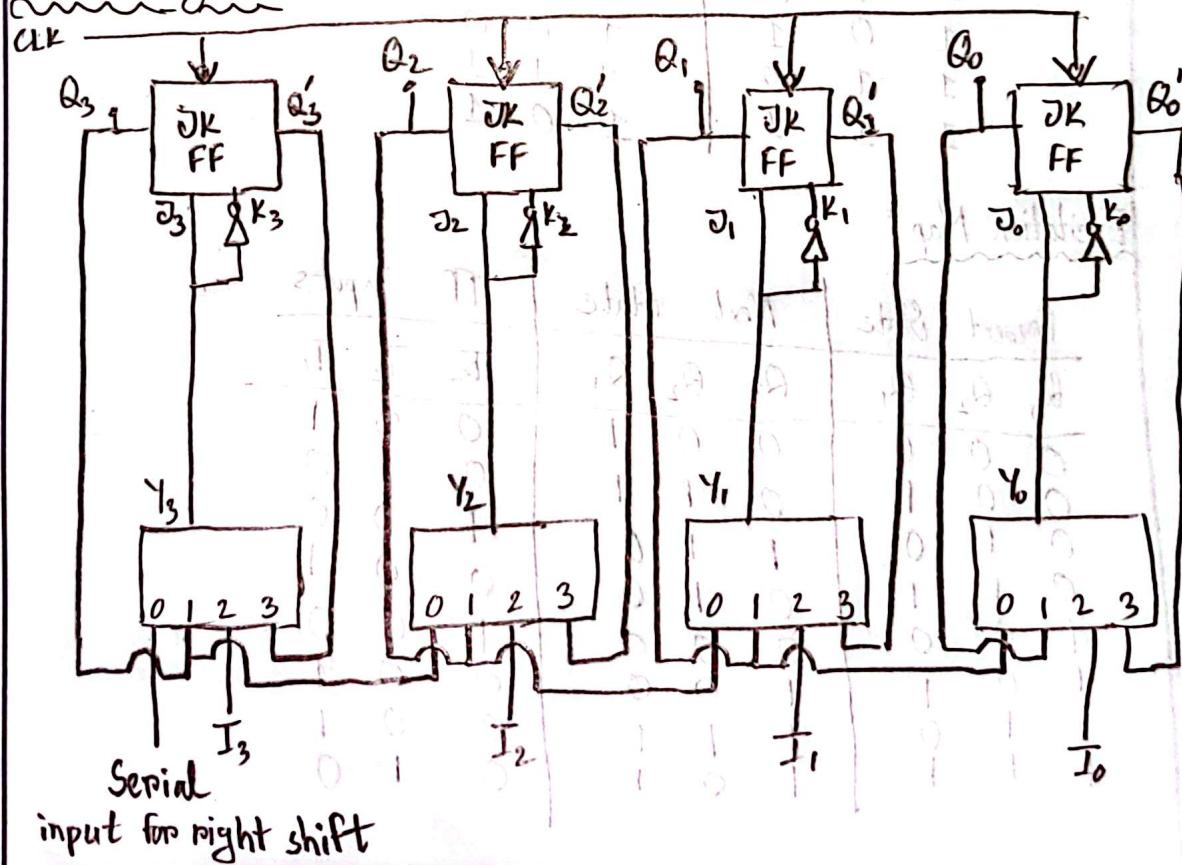
2.(b) JK FF using D FF, 2x1 MUX and Inverter(NOT gate):



2.(c) Function table:

Mode Control		Register Operation
S_1	S_0	
0	0	right shift
0	1	toggle
1	0	parallel load
1	1	unchanged

Circuit Diagram:



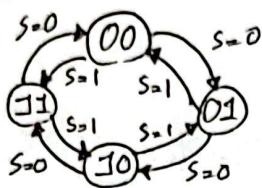
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3(a) State diagram:

Solve of 2(D) at the end of PDF



State Table:

Present State			Next State	
S	Q ₂	Q ₁	Q ₂	Q ₁
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

Excitation Map:

Present State			Next State		FF inputs	
S	Q ₂	Q ₁	Q ₂	Q ₁	T ₂	T ₁
0	0	0	0	1	0	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	0	0	1	1
1	0	0	1	1	1	1
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1

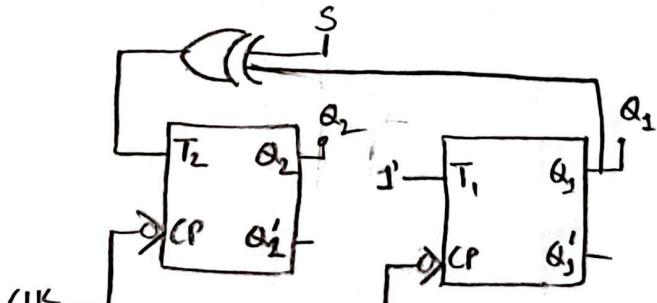
For T₂,

S	Q ₂ Q ₁
0	00 01 11 10
1	11 10 01 00

$$\therefore T_2 = S Q_1' + S' Q_1$$

$$= S \oplus Q_1$$

Circuit Diagram:

For T₁,

S	Q ₂ Q ₁
0	0 1 1 1
1	1 1 1 1

$$\therefore T_1 = 1$$

3.(c) Given message = '10110110001'

The no. of data bits in the message, $n=11$

Required parity bits = p .

$$\therefore 2^p \geq n+p+1$$

If ($p=1$), $2^1 \geq 11+1+1$ (false)

If ($p=2$), $2^2 \geq 11+2+1$ (false)

If ($p=3$), $2^3 \geq 11+3+1$ (false)

If ($p=4$), $2^4 \geq 11+4+1$ (true)

So, $p=4$, we have to send total $11+4=15$ bits.

Ending End:

Original message: 10110110001

$n=11$ bits, with parity bits,

Bit position: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

values : P1 P2 P3 P4 0 1 1 P4 0 1 1 0 0 0 0 1

To find values of P_1, P_2, P_3, P_4 , we have to XOR the binary of bit positions holding 1's,

0011 (3)

0110 (6)

0111 (7)

1010 (10)

1011 (11)

1111 (15)

(XOR) 1100

↓ ↓ ↓ ↓

P4 P3 P2 P1

So, sending message:

'00110110110001'.

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0	0	0	0	0	0	0

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Receiving End:

Case 1 → If there is no error in the message transmitting, the receiver will get : 00.1101110110001

To check if there is any error or not, receiver will XOR the binary values of the bit positions having 1 in the received message again.

$$\begin{array}{r}
 0011 \\
 0100 \\
 0110 \\
 0111 \\
 1000 \\
 1010 \\
 1011 \\
 \hline
 (XOR) 0000
 \end{array}$$

As the result is 0000, there is no errors in the message.

Case 2 → If there is an error in the 6th position while transmitting, the receiver will get: 001100110110001

To check if there is any error or not, receiver will XOR the binary values of the bit positions having 1 in the received message again.

$$\begin{array}{r}
 0011 \\
 0100 \\
 0111 \\
 1000 \\
 1010 \\
 1011 \\
 \hline
 (XOR) 0110 \rightarrow 6
 \end{array}$$

So, there is an error in the 6th position in the received message & the correct message will be :

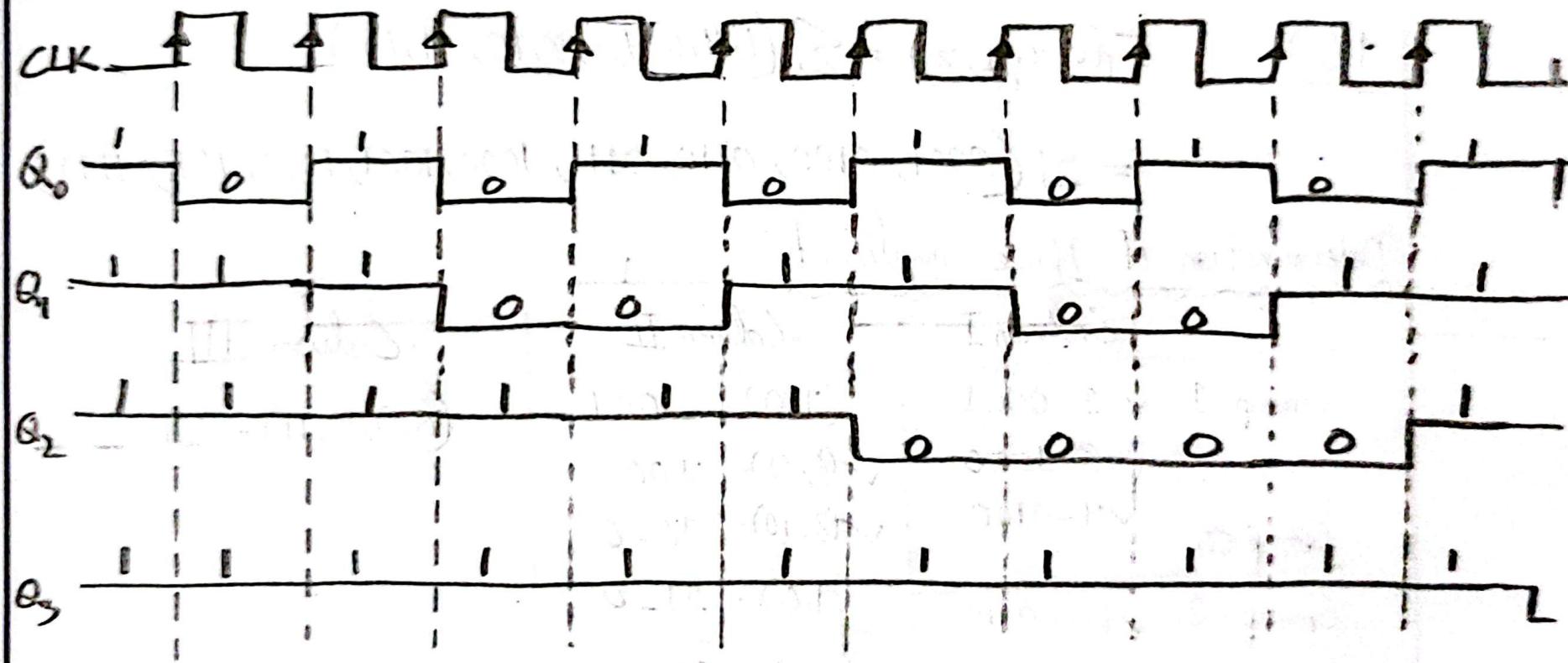
$$001101110110001$$

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3(d)



Full 2022

$$\underline{3.(c)} \quad F(w, x, y, z) = \sum (1, 4, 6, 7, 8, 9, 10, 11, 15)$$

$$= \sum (0001, 0100, 0110, 0111, 1000, 1001, 1010, 1011, 1111)$$

Determination of Prime implicants:

	Column I	Column II	Column III
Group - 1	$\checkmark 1 - 0001$	$(1, 0) - 001$	$(8, 9, 10, 11) - 10 - -$
	$\checkmark 8 - 1000$	$\checkmark (8, 9) - 100 -$	
	$\checkmark 4 - 0100$	$\checkmark (8, 10) - 10 - 0$	
Group - 2	$\checkmark 6 - 0110$	$(4, 6) - 01 - 0$	$(6, 7) - 011 -$
	$\checkmark 9 - 1001$	$\checkmark (9, 11) - 10 - 1$	
	$\checkmark 10 - 1010$	$\checkmark (0, 11) - 101 -$	
Group - 3	$\checkmark 7 - 0111$	$(7, 15) - - 111$	$(1, 15) - 1 - 11$
	$\checkmark 11 - 1011$		
Group - 4	$\checkmark 15 - 1111$		

$$\therefore \text{Prime implicants: } w x' + x'y'z + w'x z' + w'yz + xyz + wyz$$

Selection of Prime implicants:

PIs	wxyz	1	4	6	7	8	9	10	11	15
$\checkmark (8, 9, 10, 11)$	10 - -	wx'				x	x	x	x	
$\checkmark (1, 9)$	- 001	x'y'z	x						x	
$\checkmark (4, 6)$	01 - 0	w'xz'		x						
$(6, 7)$	011 -	w'xy			x	x				
$\times (7, 15)$	- 111	xyz				x				x
$(11, 15)$	1 - 11	wyz						x	x	

$$\therefore f = w x' + x'y'z + w'x z' + xyz$$

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20(a)

Subject _____

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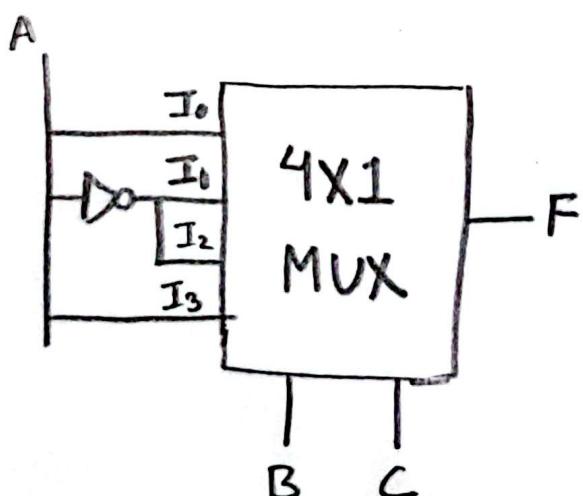
2.(b)

Truth table of 3 input XOR gate:

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Implementation Table:

MUX input lines	I_0	I_1	I_2	I_3
A'	0	①	②	③
A	④	5	6	⑦
Input values	A	A'	A'	A

Circuit Diagram:

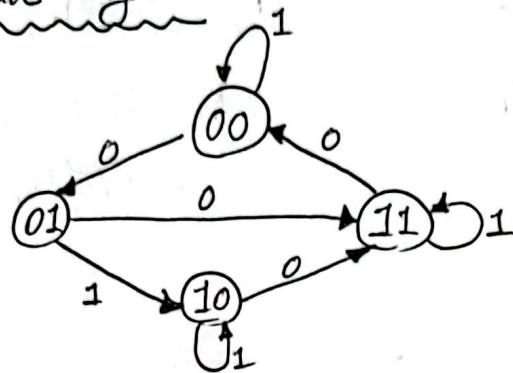
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0	0	0	0	0	0	0

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Q. (c)

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2(d)State diagram:State Table:

Present State	Next State		
	Q_2	Q_1	
0 0 0	0	1	
0 0 1	1	1	
0 1 0	1	1	
0 1 1	0	0	
1 0 0	0	0	
1 0 1	1	0	
1 1 0	1	0	
1 1 1	1	1	

Excitation Map:

Present State

Next State

Excitation Map:

Present State	Next State			FF inputs		
	Q_2	Q_1		Q_2	Q_1	
0 0 0	0	1		0	1	0 1
0 0 1	1	1		1	1	1 1
0 1 0	1	1		1	1	1 1
0 1 1	0	0		0	0	0 0
1 0 0	0	0		0	0	0 0
1 0 1	1	0		1	0	1 0
1 1 0	1	0		1	0	1 0
1 1 1	1	1		1	1	1 1

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For D_2 ,

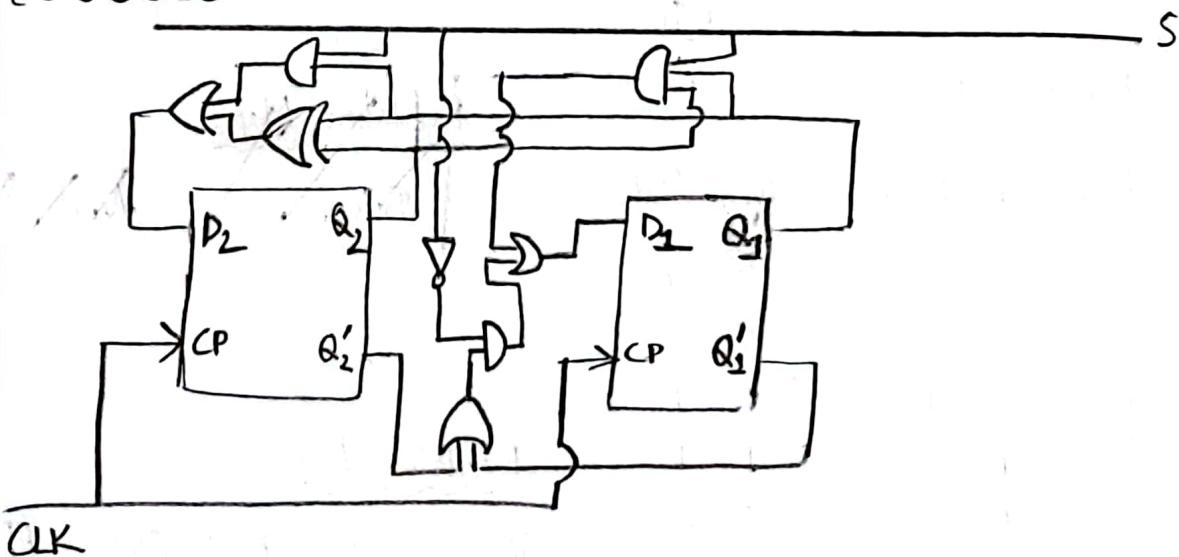
	$Q_2 Q_1$	00	01	11	10
0	$Q_2 Q_1$	0	1	1	1
1	$Q_2 Q_1$	1	1	1	1

$$\therefore D_2 = Q'_2 Q_1 + Q_2 Q'_1 + S Q_1 \\ = (Q_2 \oplus Q_1) + S Q_1$$

For D_1 ,

	$Q_2 Q_1$	00	01	11	10
0	$Q_2 Q_1$	1	1	1	1
1	$Q_2 Q_1$	1	1	1	1

$$\therefore D_1 = S' Q'_2 + S' Q'_1 + S Q_2 Q_1 \\ = S'(Q'_2 + Q'_1) + S Q_2 Q_1$$

Circuit Diagram:

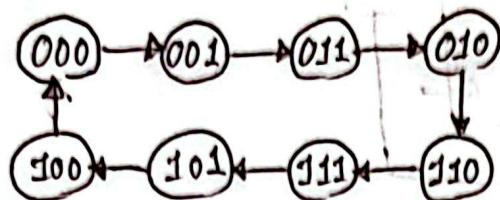
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0 0 0 0 0 0 0

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2.(d)

State diagram:



State table:

Present State			Next State		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	0	1

Excitation Map:

Present State			Next State			FF inputs		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	T_3	T_2	T_1
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	1	1	0	1	0	0
0	1	1	0	1	0	0	0	1
1	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1
1	1	0	1	1	1	0	0	1
1	1	1	1	0	1	0	1	0

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For T_3 ,

$Q_3 \backslash Q_2 Q_1$	00	01	11	10
0	.	.	.	①
1	①			

$$\begin{aligned}
 T_3 &= Q'_3 Q_2 Q'_1 + Q_3 Q'_2 Q_1 \\
 &= Q'_1 (Q'_3 Q_2 + Q_3 Q'_2) \\
 &= Q'_1 (Q_3 \oplus Q_2)
 \end{aligned}$$

For T_2 ,

$Q_3 \backslash Q_2 Q_1$	00	01	11	10
0	.	①	.	.
1	①		①	

$$\begin{aligned}
 T_2 &= Q'_3 Q'_2 Q_1 + Q_3 Q_2 Q_1 \\
 &= Q_1 (Q'_3 Q'_2 + Q_3 Q_2) \\
 &= Q_1 (Q_3 \odot Q_2)
 \end{aligned}$$

For T_1 ,

$Q_3 \backslash Q_2 Q_1$	00	01	11	10
0	①	.	①	.
1	①	①	①	①

$$\begin{aligned}
 T_1 &= Q'_3 Q'_2 Q'_1 + Q_3 Q'_2 Q_1 \\
 &\quad + Q'_3 Q_2 Q_1 + Q_3 Q_2 Q'_1 \\
 &= Q'_2 (Q'_3 Q'_1 + Q_3 Q_1) \\
 &\quad + Q_2 (Q'_3 Q_1 + Q_3 Q'_1) \\
 &= Q'_2 (Q_3 \oplus Q_1)' \\
 &\quad + Q_2 (Q_3 \oplus Q_1) \\
 &= Q_2 \odot (Q_3 \oplus Q_1)
 \end{aligned}$$

Diagram: