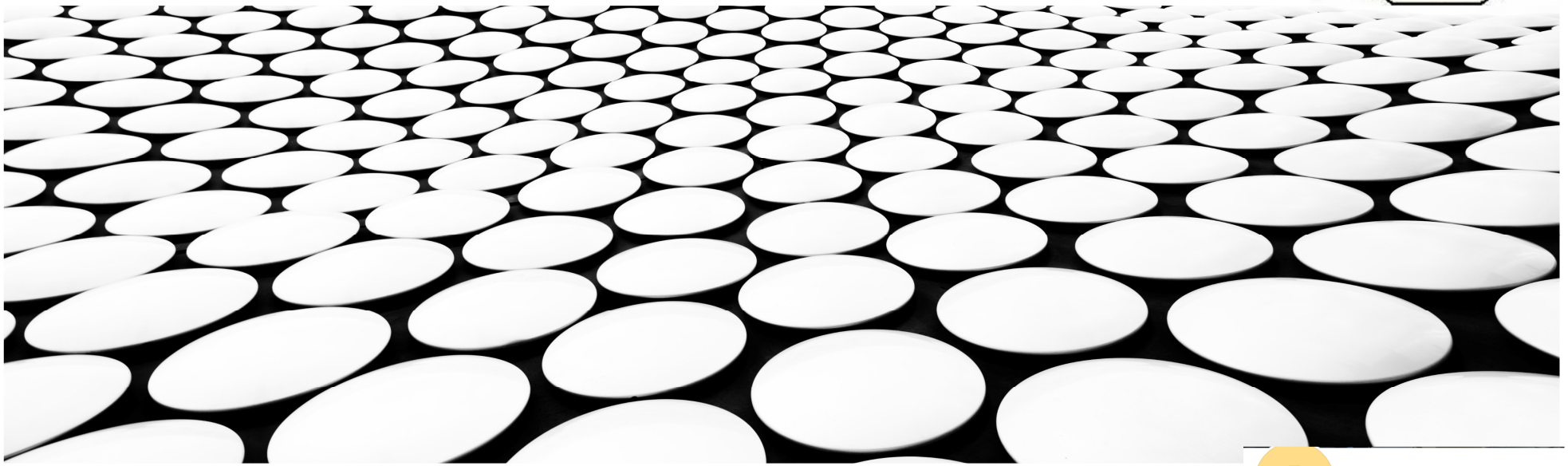
Fall 2022

CSE 2213 - COMPUTER ARCHITECTURE

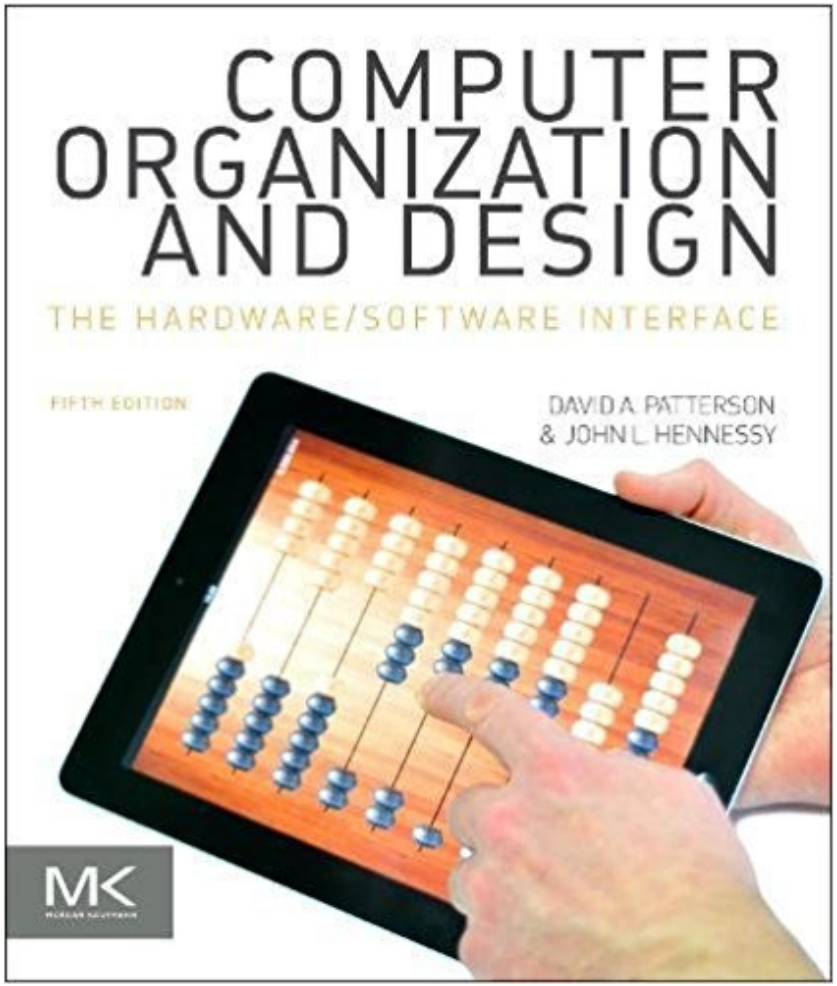
LECTURE I-OVERVIEW OF COMPUTER ARCHITECTURE

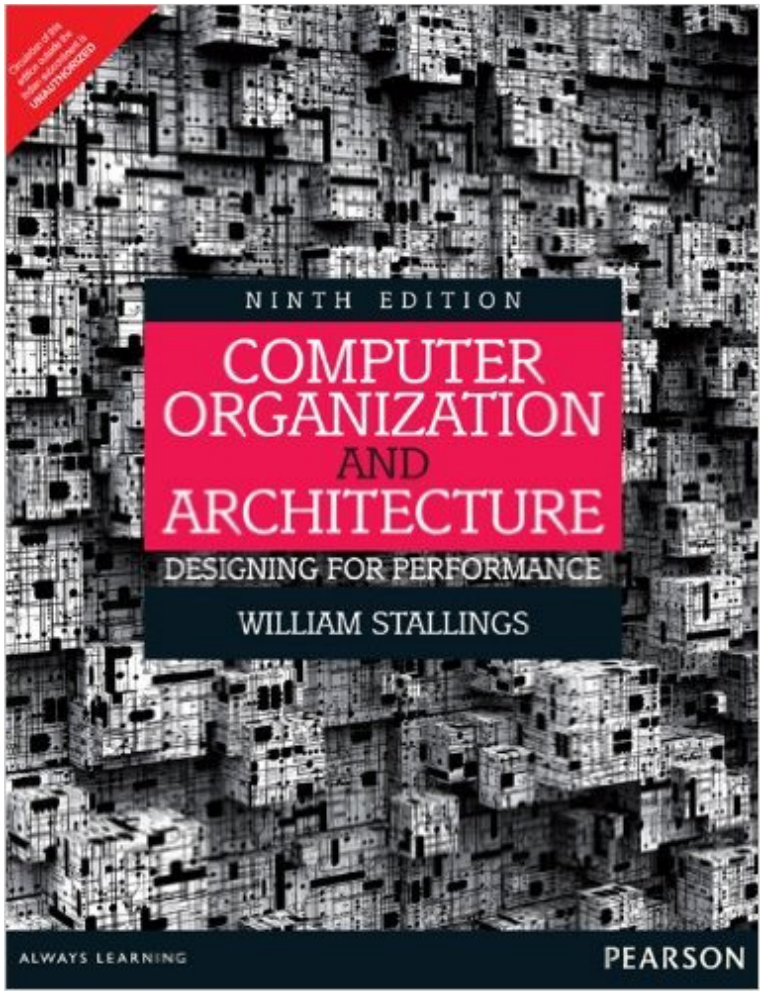
PROF. DR. MD. SHAMIM AKHTER



AISIP-Applied Intelligent System and Information Processing.

TEXTBOOKS


COMPUTER ORGANIZATION AND DESIGN
THE HARDWARE/SOFTWARE INTERFACE
FIFTH EDITION
DAVID A. PATTERSON
& JOHN L. HENNESSY
MK


NINTH EDITION
COMPUTER ORGANIZATION AND ARCHITECTURE
DESIGNING FOR PERFORMANCE
WILLIAM STALLINGS
ALWAYS LEARNING
PEARSON

Text Books have a common name:

a) Computer Organization

b) Design / Architecture

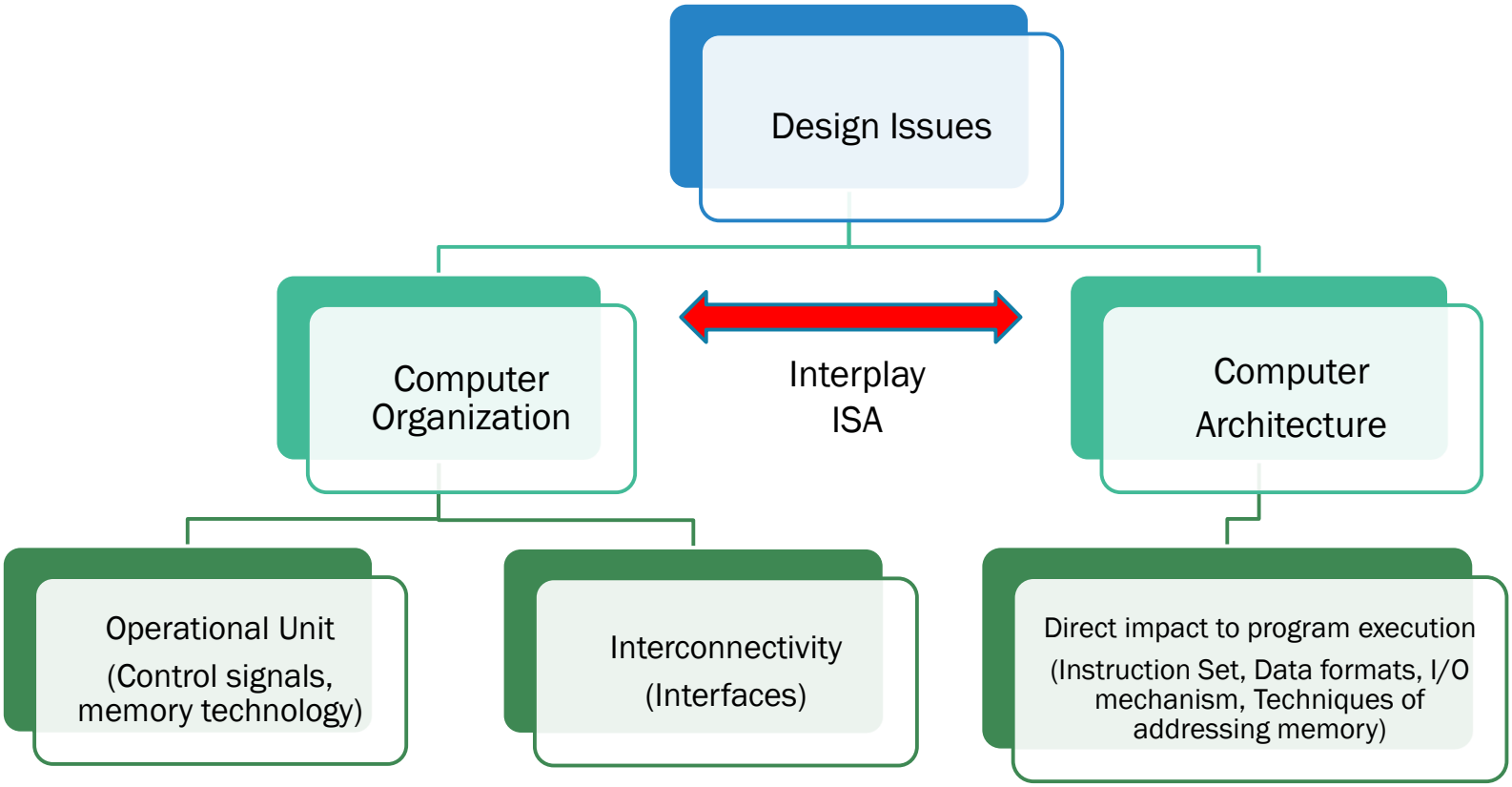
Interesting !!

- Architecture describes what the computer does.
- Organization describes how it does it.

Architectural issue: whether a computer has a multiply instruction

Organizational issue: whether the instruction execute by a special multiply unit or use repeated add unit of the system.

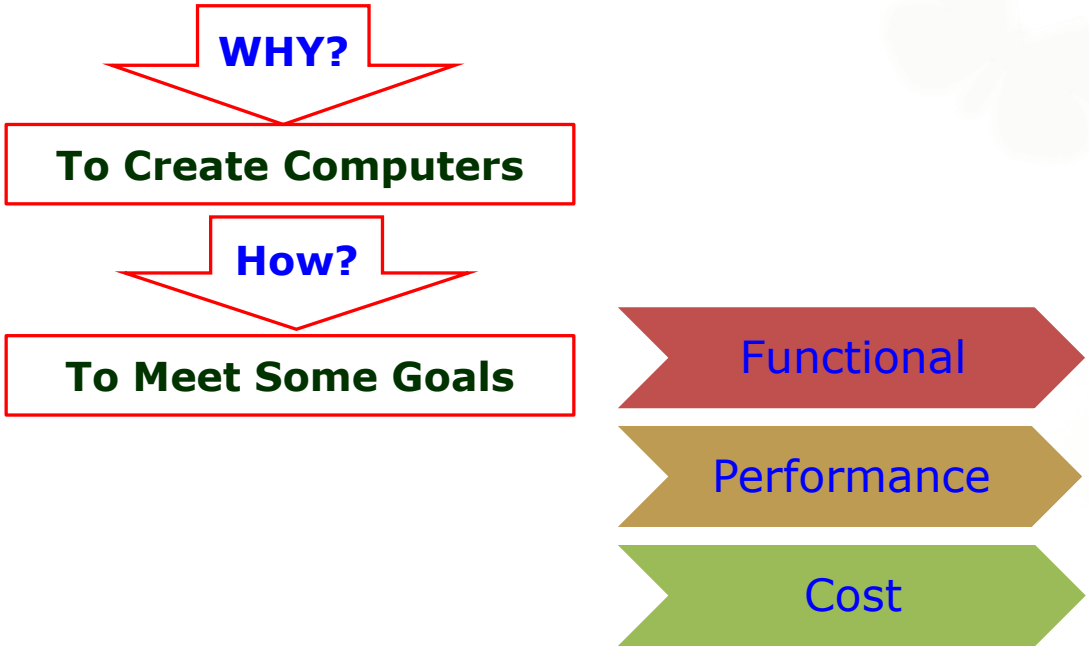
COMPUTER ARCHITECTURE DESIGN



What is Computer Architecture?

Computer Architecture is the science and art of

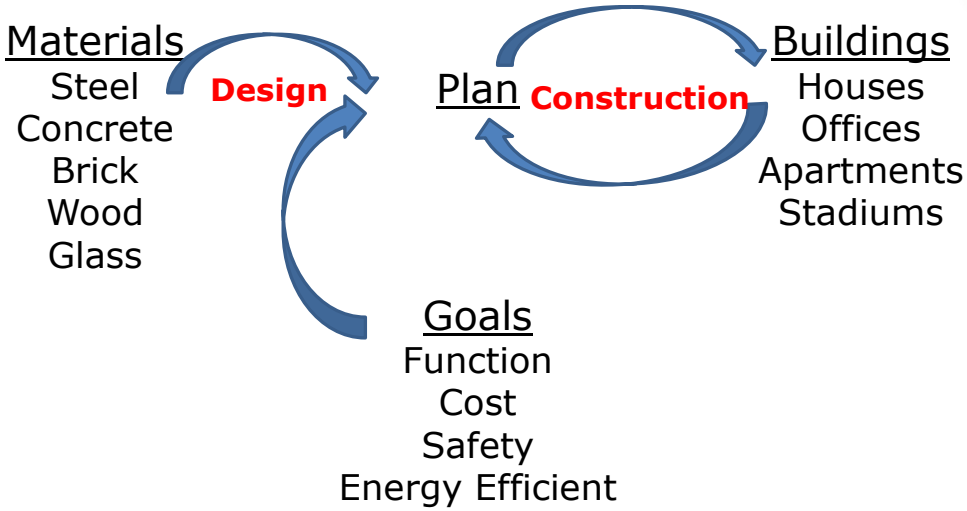
-selecting and interconnecting hardware components



- Analogy to architecture of buildings…

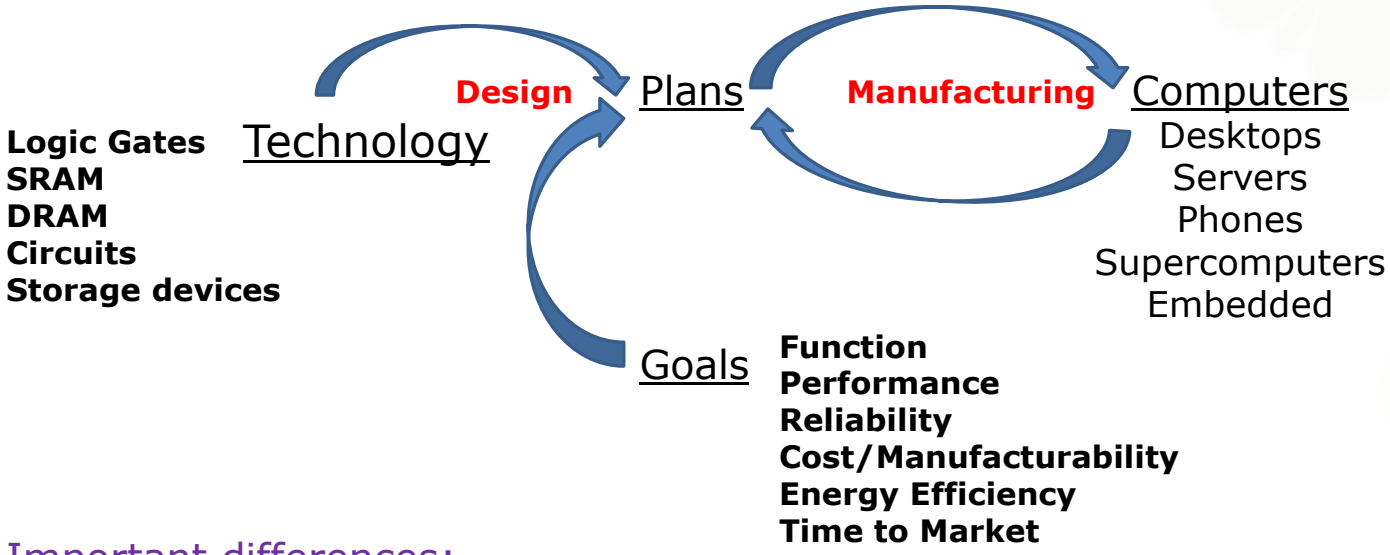
What is ~~Computer~~ Architecture

- The role of a building architect:



What is Computer Architecture?

- The role of a computer architect:

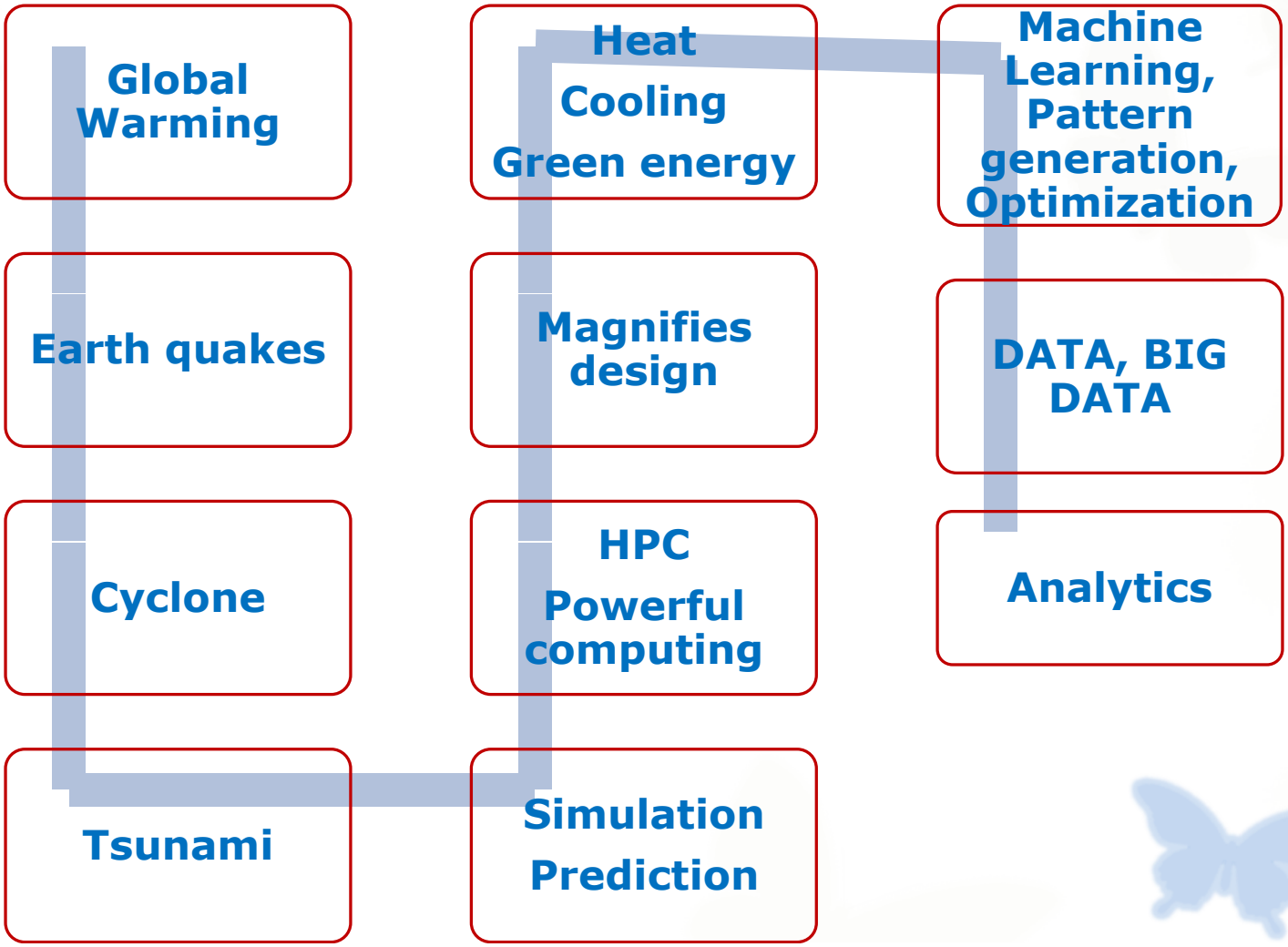


Important differences:

- age (~80 years vs thousands),
- rate of change (technology, applications, goals)

Rate of Changes

Applications



Rate of Changes

Technology

https://www.slideshare.net/BSGAfrica/top-5-considerations-when-choosing-and-managing-a-technology-vendor

"Technology"

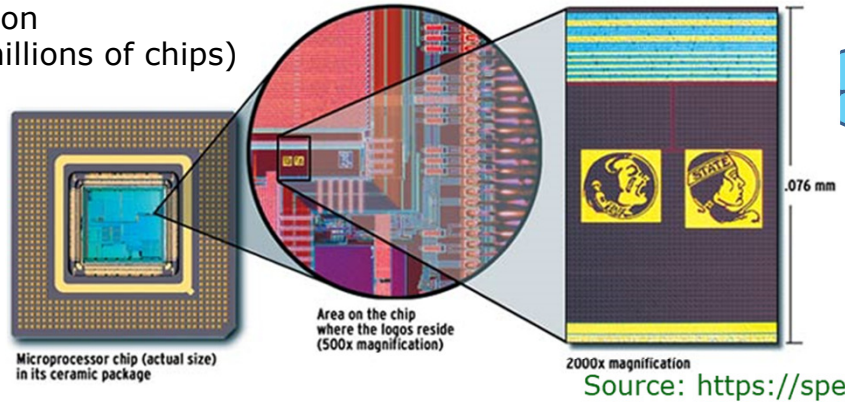
Year	Technology used in computers	Relative performance/unit cost
1951	Vacuum tube	1
1965	Transistor	35
1975	Integrated circuit	900
1995	Very large scale integrated circuit	2,400,000
2005	Ultra large scale integrated circuit	6,200,000,000

ON/OFF switches-control electricity

100 transistors into a single chip

Microprocessor- VLSI device

Automated Mass Production
(magnifies design-over millions of chips)



High Performance, High Reliability

Source: https://spectrum.ieee.org/image/MTQxNTQ3Nw

- Increasing opportunities for integrating multiple technologies
  - Inter-connection technologies
  - Disk, optical storage, ethernet, fiber optics, wireless

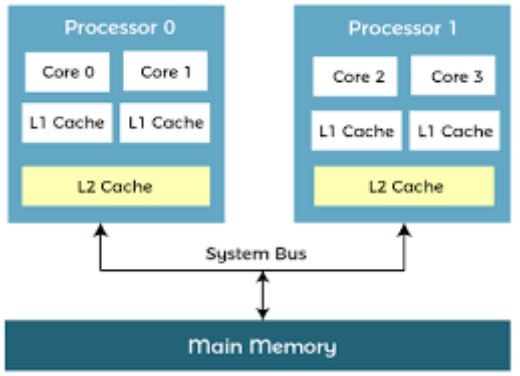
Interconnection technology: Example

μP -> Multi-Processors-> dual-core >Quad-core->multicore

multiple pipelines, and multiple sets of caches.

We want more! 100 cores in a single die !

- Need to make smaller cores but lose the functionality
- Making a bigger die but increases cost



What else???

How about to reduce the cost of **chip-to-chip communication**
- power, bandwidth, latency

Interconnection Technology Exploration

Break a multi-core chip into a many-chip-system
-smaller chips lead to higher yields and lower cost
-different chips lead to system adaptability and reconfigure ability
-aggregate systems of chips effectively

How does the interconnection technology change the word?

Example: Wire Technology

1. Alexander Graham Bell invented the telephone in 1876,messages were traveled as electric currents and transmitted over copper wire.

2. Need better sound quality, cover greater distances, greater capacity
   - integration of metallic two-wire circuits, loading coils, vacuum-tube amplifiers, coaxial cable, and microwave radio relay systems.

3. Then came conversion from Analog Signal to Digital Signal
   - achieved more frequency, greater capacity
   - use in TV and Digital Computer

4. Need to carry information much faster
   - Solution Laser ->Optoelectronics
   - Transmission rate-10kb/S
   - Problem: Clouds, Haze, Rain ---> Block beam.

5. Use laser inside glass fibers
   -achieved 100Mb/S

6. Can data transmit as the speed of light?
   More higher frequency (Gb/S, Tera b/S .....)
   Replace microwave to light wave
   - Light waves ---->
   Noble Prize in Physics-2009, Prof. Charles K. Kao

Glass Fiber

Technology Change Drives Everything

- Computers get **10x faster, smaller, cheaper** every 5-6 years!

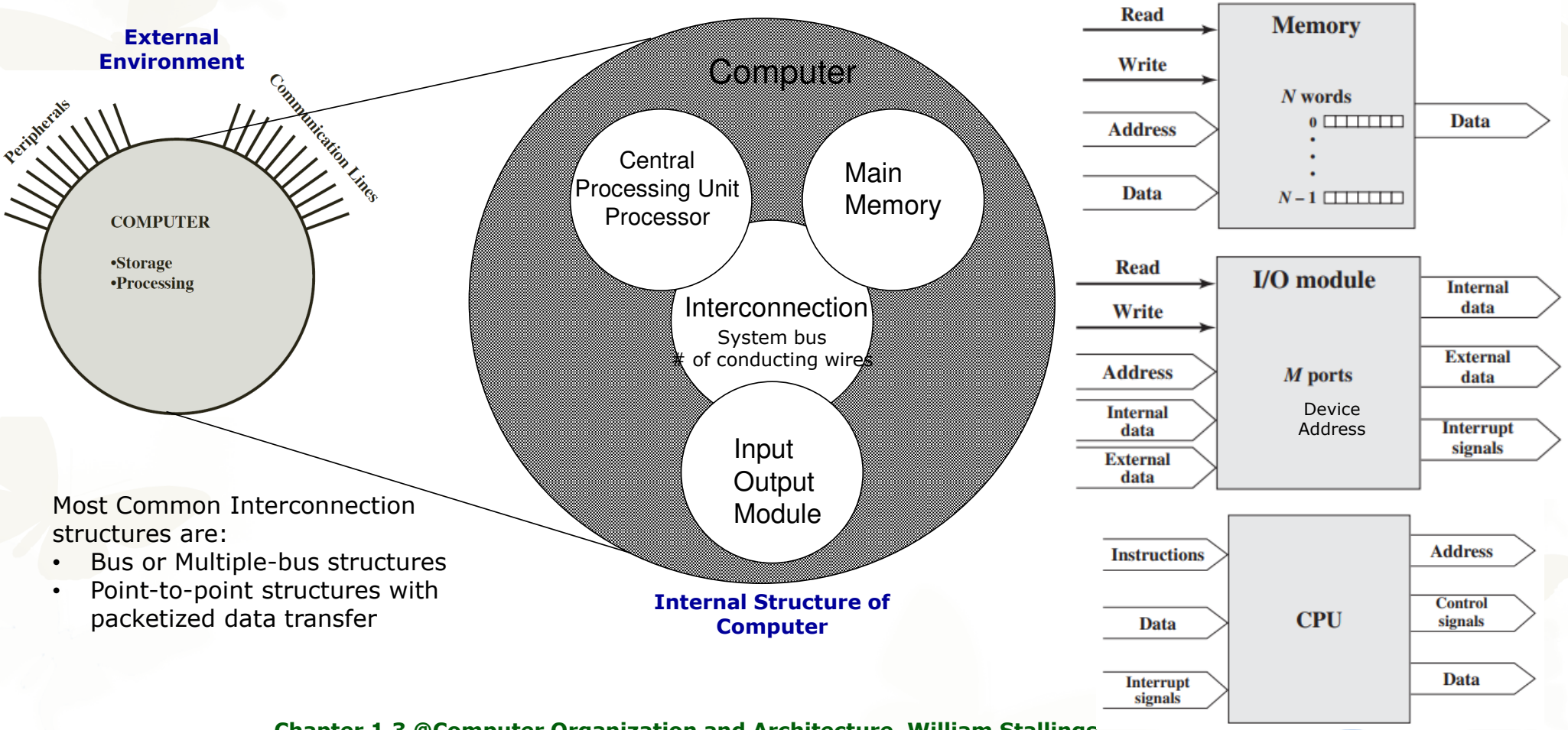
- **Doubling every 1.5 years:**

  -memory capacity

  -processor speed (due to advances in technology and hardware organization)

  - example: if Boeing had kept up with IBM we could *fly from Bangkok to Dhaka in 10 minutes for 500 Taka* !!

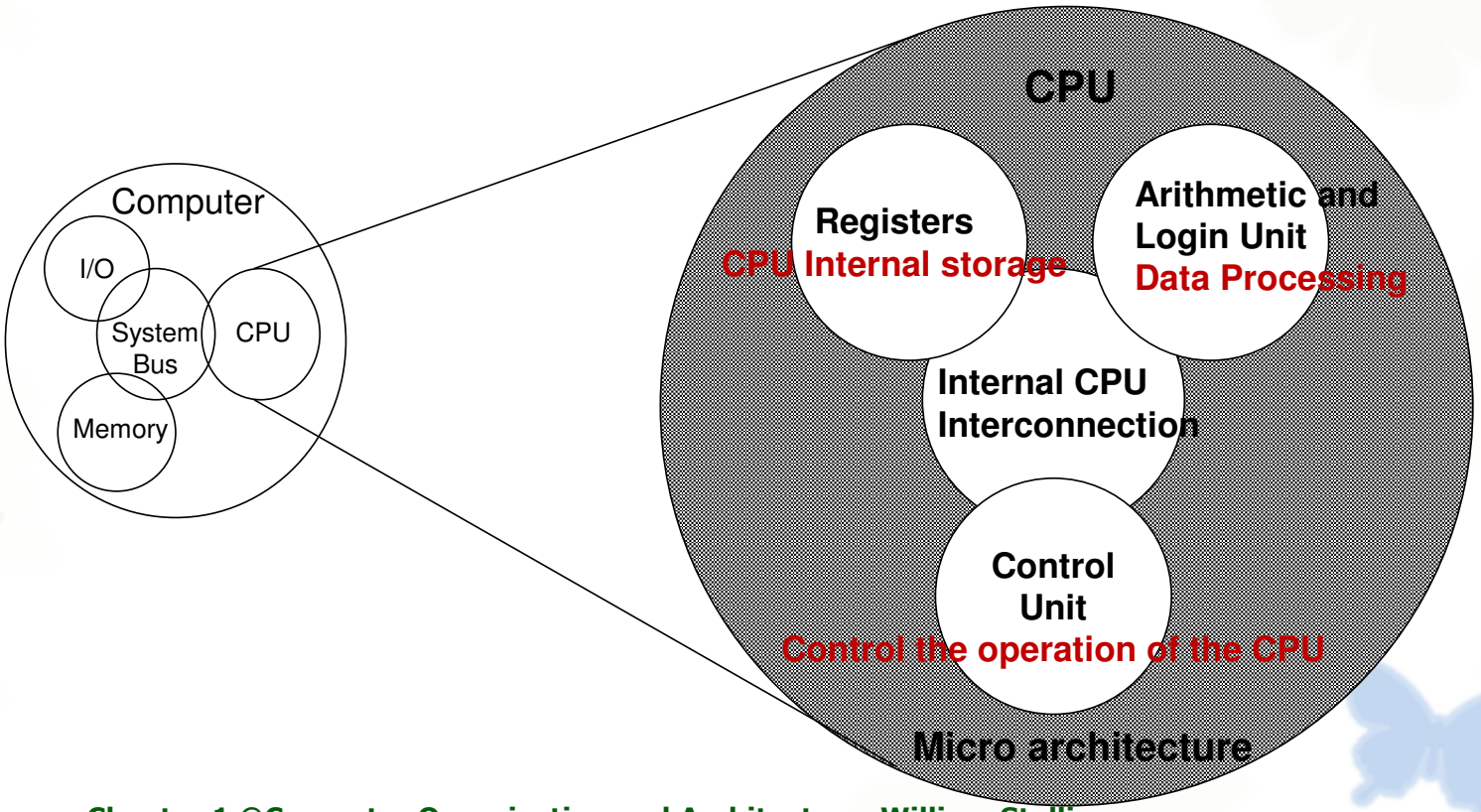
Computer and Top Level Structure Interrelated Components



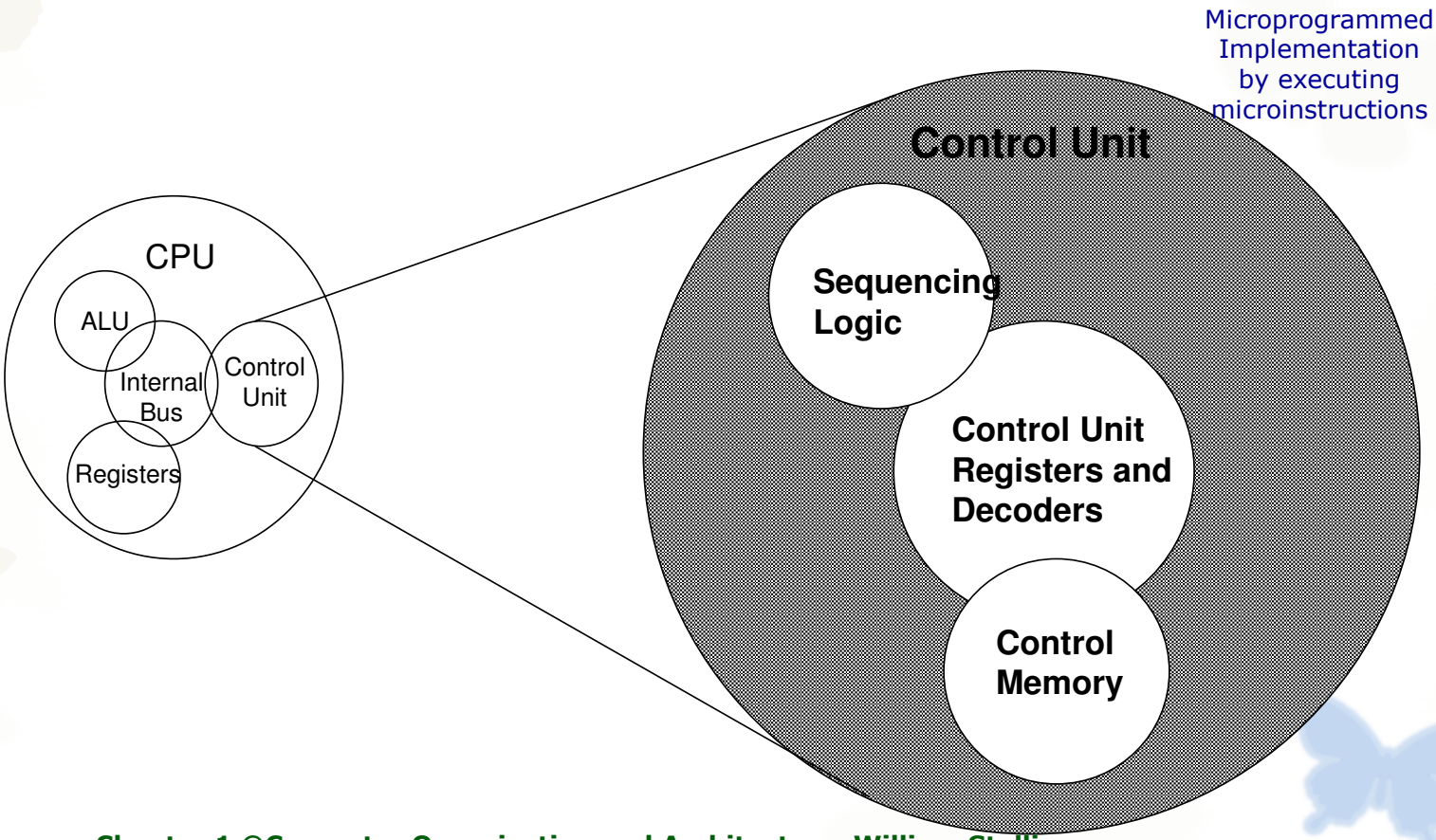
Most Common Interconnection structures are:

- Bus or Multiple-bus structures
- Point-to-point structures with packetized data transfer

CPU Structure



Control Unit Structure



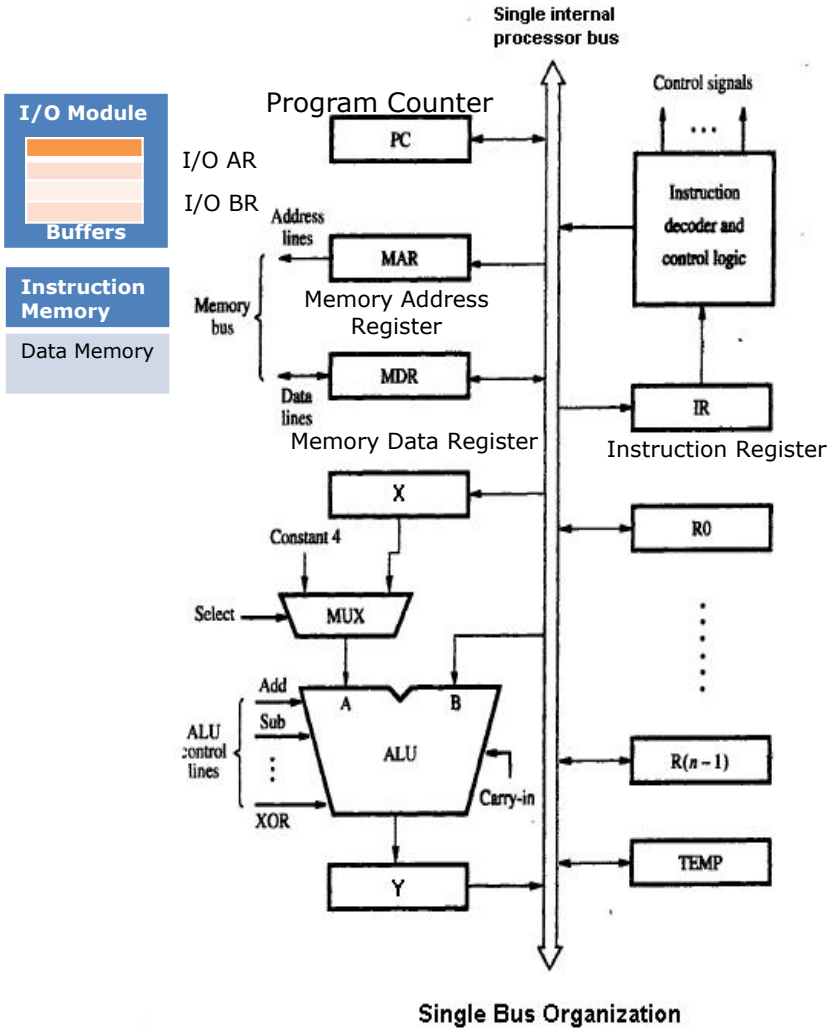
Computer Architecture=Microarchitecture + ISA

The micro architecture includes:
- the parts of the processor and
- how these interconnect and
- interoperate to implement ISA.

Basic function of a micro architecture to execute instructions.

- **The instruction set architecture (ISA) is implemented on a processor**

The ISA includes :
- the execution model,
- processor registers,
- address and data formats.



Single Bus Organization

The Instruction Set Architecture (ISA)

- that part of the architecture that is visible to the programmer
  - operations-how many?, which one?
  - operands –how many?, location
  - number and types of registers
  - instruction formats-size, formats
  - storage access, addressing modes

y=x+b

(add r1, r2, r5)

- advantage: *allows different implementations of the same architecture*
  example: each instruction in MIPS is 32 bits
- disadvantage: *sometimes prevents adding new innovations*

- Modern instruction set architectures:
  - 80x86/Pentium, PowerPC, DEC Alpha, MIPS

RISC VS CISC

RISC	CISC
Reduced Instruction Set Computing	Complex Instruction Set Computing Predecessor of RISC
Designed for Simpler H/W	Designed for Complex H/W
Code length fixed	Small code sizes Variable length code
One clock cycle/instruction	Multiclock complex instruction
Instruction pipeline can be implemented	Instruction pipeline can not be implemented
Can use less RAM as no need to store intermediate results	Can use more RAM to handle intermediate results
Only load/store instruction can access memory	Many instructions can access memory

Example: RISC vs CISC

RISC Approach

```
LOAD  A,  2:3
LOAD  B,  5:2
PROD  A; B
STORE  2:3, A
```

Sun Ultra
SPARC
IBM Power PC

	1	2	3	4
1				
2			3	
3				
4				
5		4		
6				

Resisters

A	D
B	E
C	F

ALU Execution

CISC Approach

```
MULT 2:3, 5:2
```

Intel x86

MIPS Simulator

- Introduced in 1987
- RISC ISA

M Microprocessor

I (Without) Interlock — **Not- I/O Interlock or frame lock**

P Pipeline — Different Stages: Some stages take larger time than others

S Stage — Next Instruction needs to wait

How does system notify to wait for the next instruction from stage to stage?

Solution: Need H/W support.