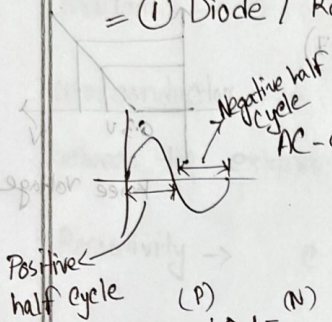
Topic Name : EEE 2141 Day : Thrus Day

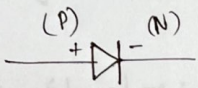
Time : Date : 17 / 11 / 2022

Course Outline :-

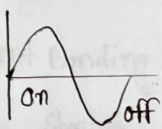
= ① Diode / Rectifier / P-N Junction



AC-current এর চিত্র 2 টাই Positive & Neg



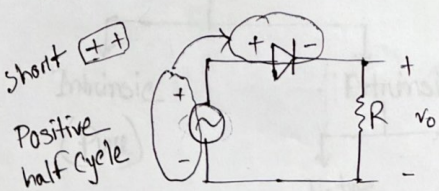
PN Junction



Duty Cycle 50% কাজ করে

$$\frac{on}{on+off} = \frac{1}{2}$$

= ② Clippers & Clampers



++ - Short

+ −

− +

−− — Short

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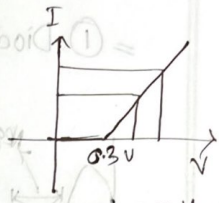
Diode

ideal, Ge, Si

($V_0 = 0$) ($V_0 = 0.3$) ($V_0 = 0.7$)

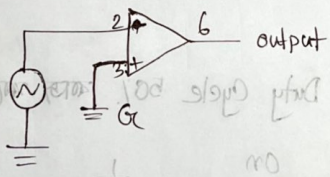


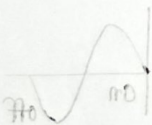
Knee voltage

= (iii) BJT

= (iv) MOSFET

= (v) OP- amp





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Conductor → generous flow of charge.

Insulator → a very low level of conductivity.

semiconductor → has a conductivity level somewhere between the extremes of an insulator and a conductor.

Resistivity → $\sigma \propto \frac{1}{R}$

Atomic Structure :- last orbit electron এর বড়া হয়,

Covalent Bonding :- A bonding of atoms, strengthened by the sharing of electrons, is called covalent bonding.

Intrinsic materials :- Ge & Si

semiconductor
- Intrinsic (Pure)
- Extrinsic (impurity)
  - N-type [Sb, As] (Pentavalent)
  - P-type

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← Hole

→ Electron

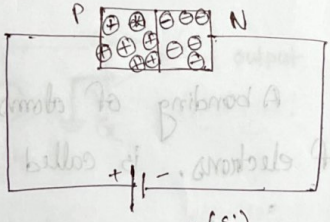
Basic principle of Diode :-

① Zero Bias. → voltage 0 হলে,

② Forward Bias.

③ Backward Bias.

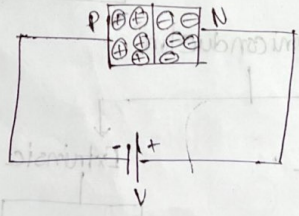
Forward Bias



majority Carrier এর জন্য Current flow

V = 0.7 (Si)

Reverse Bias



Minority Carrier এর জন্য Current flow

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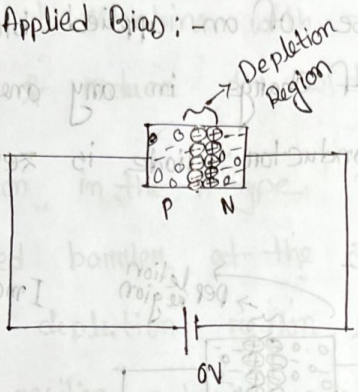
(*) No - Applied Bias : -



Free electrons of N-type diffuse over & fill the free holes in the P-type. So, n-type becomes positively charged due to lost of an electron. On the otherhand, P-type becomes negatively charged due to the gaining of extra electron.

(*) {For every electron that diffuses across the junction & combines with a hole, a positive charge is left in the n region & a negative charge is created in the p-region forming a barrier potential}

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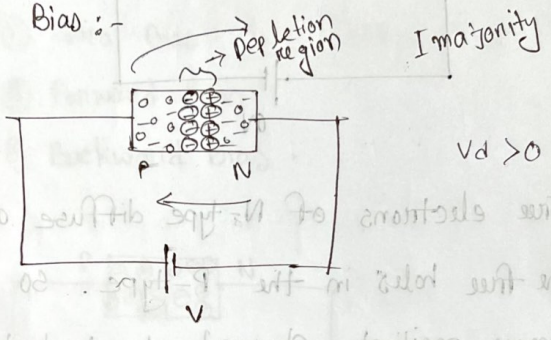
In the absense of an applied bias voltage, the net flows of charge in any one direction for a semi-conductor diode is zero.

(*) Forward Bias :-



A forward Bias or "On" Condition is established by Applying positive potential to the p-type and the negative potential to the n-type material. The application of a forward bias potential vd will "Pressure" electrons in the n-type and holes in p-type

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material to recombine with the ions near the boundary & reduce the width of depletion region.

= An electron in the n-type material now sees a reduced barrier at the Junction due to the reduced depletion region & a strong attraction for the positive potential applied to the p-type material.

verify the statement —

As the applied bias increases in magnitude the depletion region will continue to decrease in width untill a flood of electrons can pass through the Junction, resulting in an exponential rise in currently.

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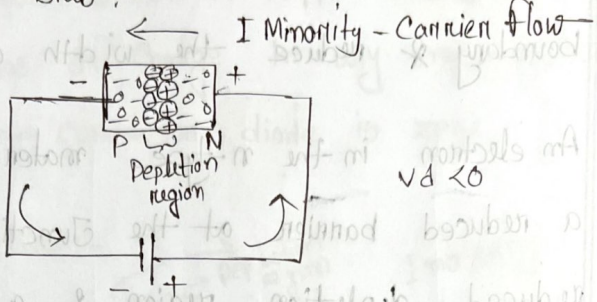
(*) Reverse Bias :-



If an external potential of V volts is applied accross the p-n Junction Such that the positive terminal is connected to the n-type material and the negative terminal is connected to the p-type material. The number of uncovered positive ions in the depletion region of the n-type material will increase. The number of uncovered negative ions will increase in the p-type material. The net effect, therefore, is a widening of the depletion region. This widening of the depletion region will establish too great.

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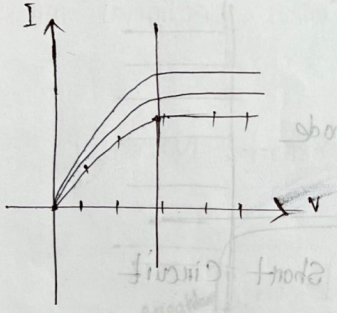
a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero

The current that exists under reverse-bias conditions is called the reverse saturation current and is represented by I_S.



Shockley's Equation → $I_D = I_S\left(e^{V_D/mV_T} - 1\right)$

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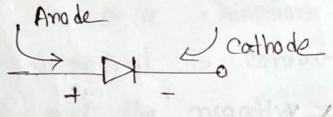
Diode :- ① P-n Junction

② When VD is positive → Diode forward / Conducting

③ VD is negative → Diode reverse / non conducting

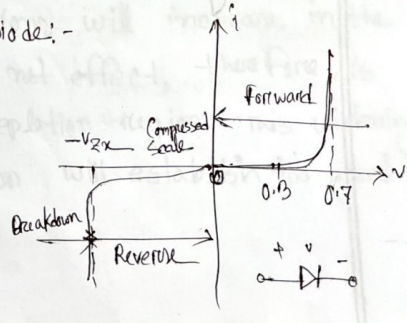
Ideal Diode :-



Forward → Diode Short Circuit

Reverse → Diode Open Circuit

I-V Characteristics of Diode :-



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2 mark Question for Quiz

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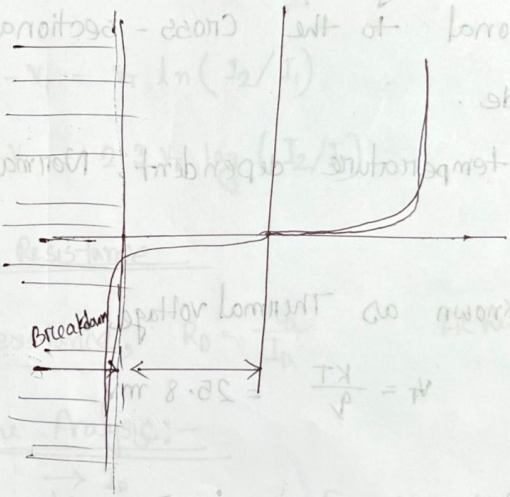
(*) **Breakdown region:** — The breakdown region enters when the magnitude of reverse voltage exceeds a threshold value that is specific for a particular diode, called the breakdown voltage. This voltage is denoted as V_{ZK}, Zener knee voltage.



Same fig as before

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The forward-bias region of Operation is entered when $v > 0$.

The forward bias i-v relation is

$$i = I_S \left(e^{v/V_T} - 1\right) \quad \text{—— (1)}$$

Diode at a given temperature. I_S is directly proportional to the cross-sectional area of the Diode.

I_S is temperature dependent. Normally

V_T is known as Thermal voltage,

$$V_T = \frac{KT}{q} = 25.8 \text{ mV}$$

when forward current $i \gg I_S$

$$i = I_S e^{v/V_T}$$

$$\Rightarrow \ln i = \ln I_S e^{v/V_T}$$

$$\Rightarrow v = V_T \ln\left(\frac{i}{I_S}\right)$$

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$\Rightarrow I_1 = I_s e^{V_1/V_T}$

$\Rightarrow I_2 = I_s e^{V_2/V_T}$

$$\frac{I_2}{I_1} = \frac{I_s e^{V_2/V_T}}{I_s e^{V_1/V_T}}$$

$$\Rightarrow \frac{I_2}{I_1} = e^{(V_2 - V_1)/V_T}$$

$$\Rightarrow V_2 - V_1 = V_T \ln(I_2/I_1)$$

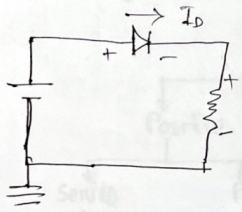
$$\Rightarrow V_2 - V_3 = 2.3\, V_T \log(I_2/I_1)$$

Diode Resistance

DC Resistance, $R_D = \frac{V_D}{I_D}$

AC Resistance $r_d = \frac{\Delta V_d}{\Delta I_d}$

Load Line Analysis:-



$$E - V_D - V_R = 0$$

$$\Rightarrow V_D = E - V_R$$

$$\boxed{= V_D = E - I \cdot R} \quad (E, 0)$$

Topic Name : Day : Time : Date : / /

$$E = V_D + I_D R$$

$$\Rightarrow I_D R = E - V_D$$

$$\boxed{\Rightarrow I_D = \frac{E - V_D}{R}}$$

$$= \frac{E}{R} \qquad \left(0, \frac{E}{R}\right)$$

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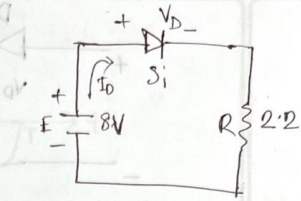
Math on Diode in a Network



$V_D = 0.7V$

$V_R = E - V_D = 8 - 0.7 = 7.3V$

$I_D = I_R = \frac{V_R}{R} = \frac{7.3}{2.2} = 3.32\ mA$

Series

I same থাকে

V change হয়

Parallel

V same থাকে

I change হয়

(*) Clipper :- Clipper is a wave shaping circuit which controls the shape of the output wave-form by removing or clipping a portion of the applied wave.

Clippers
- Positive
  - Series
    - Biased
    - Unbiased
  - Parallel
    - Biased
    - Unbiased
- Negative
  - Series
    - biased
    - unbiased
  - Parallel
    - biased
    - unbiased

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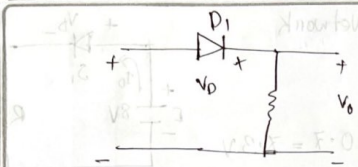


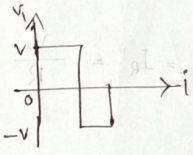
For (+ve) Half Cycle

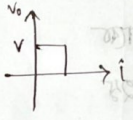
$V_1 - V_{D1} - V_0 = 0$

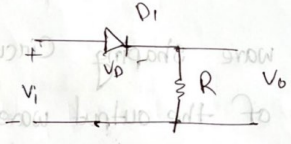
$\Rightarrow V_0 = V_1 - V_{D1}$

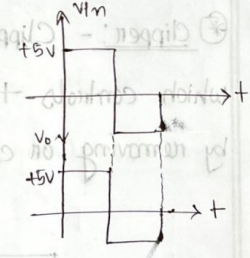
$\Rightarrow V_0 = V_1 - 0$

$\Rightarrow V_0 = V_1$









For (−ve) half Cycle,

D_1 is open Circuit

$V_0 = 0$

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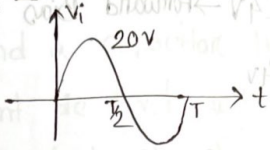
⇒ Biased Series Clipper :-



(i) when $V_i \geq -5V$

↓

Forward Bias

$V_0 = V_i + 5$

(ii) when $V_i \leq -5V$

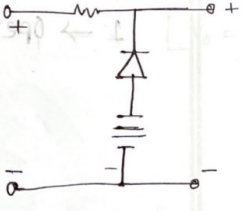
↓

Reverse Bias

$V_0 = 0$

⇒ Unbias Parallel Clippers

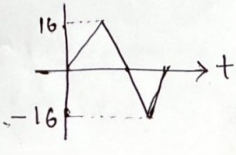
$V_i \rightarrow$ Positive $V_0 = 0$



⇒ Biased Parallel Clippers

$V_i \geq 4V \rightarrow$ Reverse Bias

$V_0 = V_i$



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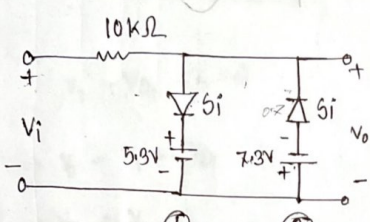
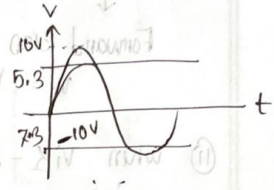
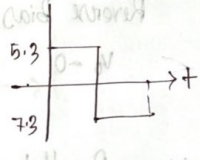
$V_i \leq 4V \rightarrow$ Forward Bias

$V_o = 4V$







Positive Half Cycle

↓

1 → Short

2 → open

Negative half Cycle

2 → Short

1 → open

Quiz-1 (12. . 2022)

Slide - 1, 2, 3

Clipper & (1-2) Slide theory

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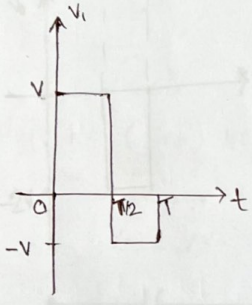
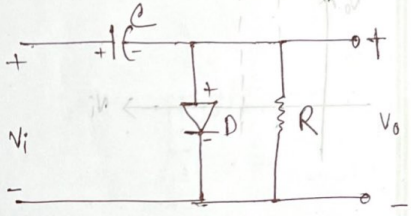
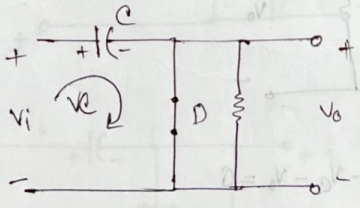
Clampers :- A clamper is a network constructed of a diode, a resistor, and a capacitor that shift a wave-form to a different dc level without changing the apperance of the applied signal.





⇒ For (+ve) Half Cycle,



Applying KVL,

$+V_i - V_c - V_o = 0$

$\Rightarrow V_i = V_c \quad [V_o = 0]$

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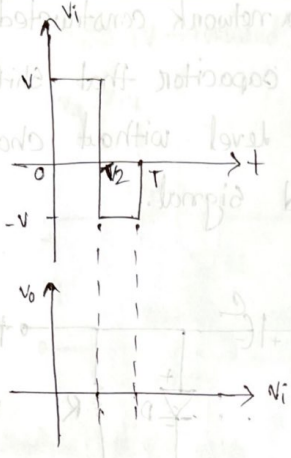
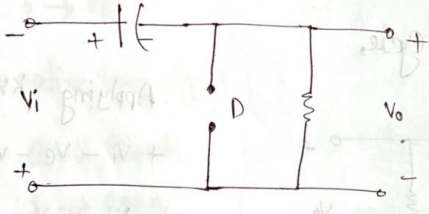


⇒ For (-ve) half cycle,



Applying KVL, $-V_i - V_c - V_o = 0$

$\Rightarrow V_o = -V_i - V_c$

$\Rightarrow V_o = -V - V$

$\Rightarrow V_o = -2V$

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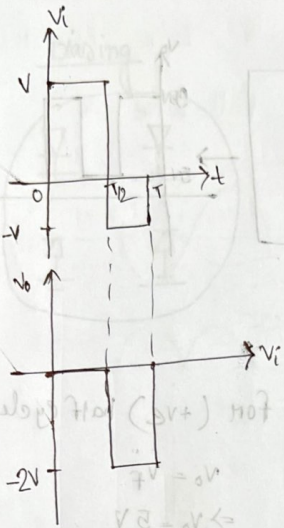
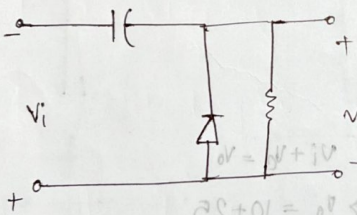
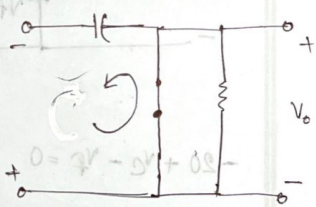
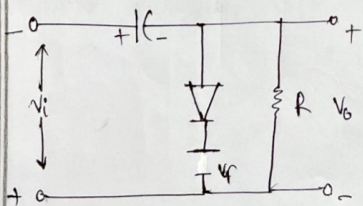


⇒







$V_i - V_c - V_f = 0$

$\Rightarrow V_c = V_i - V_f$

Negative half cycle

$-V_i - V_c - V_o = 0$

$\Rightarrow V_o = V_i - V_c$

$= V_i + V_i + V_f$

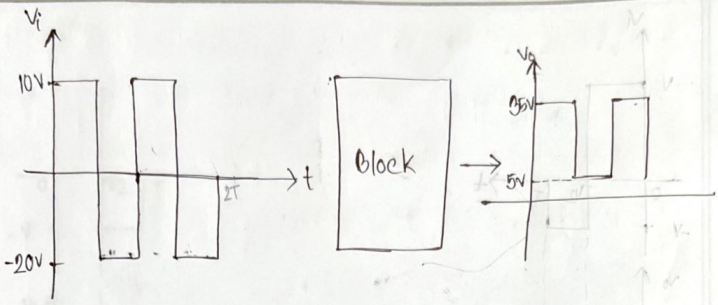
$= -20 + 5$

$= -15$

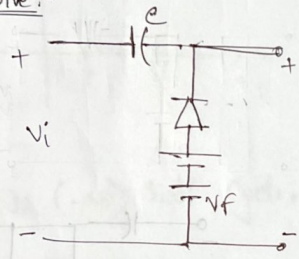
Scanned with CamScanner

Topic Name : Day : Time : Date : / /

(*)



Solve :-



for (+ve) half cycle,

$V_o = V_f$

$\Rightarrow V_o = 5\,V$

$-20 + V_c - V_f = 0$

$\Rightarrow -20 + V_c - 5 = 0$

$\Rightarrow V_c = 25V$

$V_i + V_c = V_o$

$\Rightarrow V_o = 10 + 25$

$\Rightarrow V_o = 35\,V$

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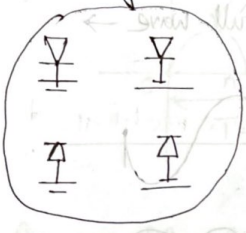
Topic Name :

Day :

Time :

Date : / /

Biasing



Unbiasing

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Topic Name : EEE -2141

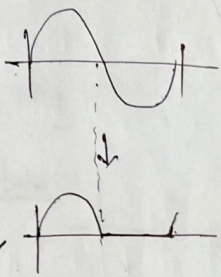
Day : MONDAY

Time :

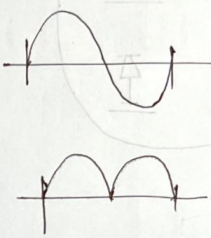
Date : 12 / 12 / 2022

Rectifier :-

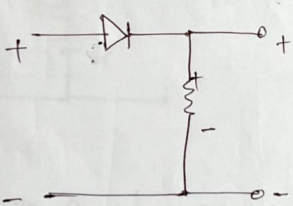
Half-wave →

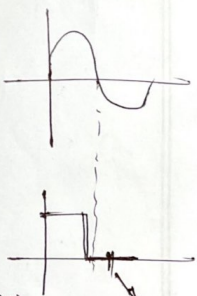


Full-wave →



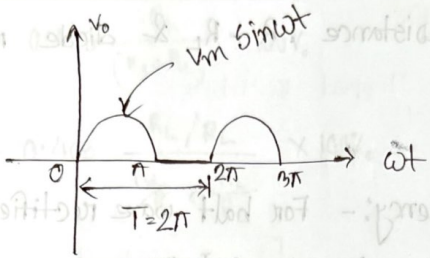
active





series
Half wave negative part
negative clipper

Topic Name : Day : Time : Date : / /



Average DC output voltage of HWR,

$$V_{dc} = \frac{1}{T}\int_0^T V_0 \, d(\omega t)$$

$$= \frac{1}{2\pi}\int_0^{\pi} V_m \sin\omega t + d\omega t + \int_0^{2\pi} 0$$

$$= \frac{1}{2\pi} V_m \left[-\cos\omega t \right]_0^{\pi}$$

$$= \frac{V_m}{2\pi}\left[-\cos\pi + \cos 0 \right]$$

$$= \frac{V_m}{2\pi}\left[1 + 1 \right]$$

$$= \frac{2 V_m}{2\pi}$$

$$= \frac{V_m}{\pi}$$

$$= 0.318 V_m$$

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Topic Name : Day : Time : Date : / /

* For load resistance, $R = R_L$ & diode resistance, r_d.

Rectifier efficiency:- For half wave rectifier, dc power to the load, $P_{dc} = I_{dc}^2 R_L = \left(\frac{I_m}{\pi}\right)^2 R_L$

The total input ac power,

$$P_{ac} = I_{rms}^2 (r_d + R_L) = \left(\frac{I_m}{2}\right)^2 (r_d + R_L)$$

$$\boxed{\begin{array}{l} \eta \propto \frac{1}{\text{input}} \\ \eta \propto \text{output} \end{array}}$$

$$\eta = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{\left(\frac{I_m}{\pi}\right)^2 R_L}{\left(\frac{I_m}{2}\right)^2 (r_d + R_L)} \times 100\%$$

$$= \frac{\frac{I_m^2}{\pi^2} \times R_L}{\frac{I_m^2}{4} \times (r_d + R_L)}$$

$$= \frac{\frac{4}{\pi^2} \times R_L}{r_d + R_L}$$

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Topic Name : Day : Time : Date : / /

$$= 0.405 \frac{R_L}{(r_d + R_L)} \times 100\%$$

$$= 0.405 \frac{R_L / R_L}{\frac{r_d}{R_L} + \frac{R_L}{R_L}} \times 100\%$$

$$= \frac{0.405}{\left(1 + \frac{r_d}{R_L}\right)} \times 100\%$$

$$= \frac{40.6\%}{1 + \frac{r_d}{R_L}}$$ [Prove]

if $r_d << R_L$
$(\eta \rightarrow 40.6\%)$

* Verify the statement :-

The best condition (i.e no diode loss), only 40.6% of the ac input power is converted into dc power. The rest remains as ac power in the load.

PIV / PRV

Peak Inverse voltage

Peake Reverse voltage

PIV (or PRV) $> V_m$

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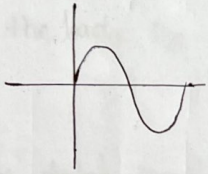
Topic Name : EEE 2141 Day : ThrusDay

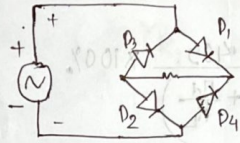
Time : Date : 15 / 12 / 2022

Full wave Rectifier

① Center – Tapped rectifier

② Bridge Rectifier.



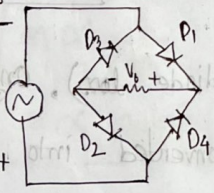


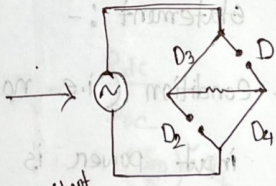
Positive Cycle

D_1, D_2 short

D_3, D_4 Open

Negative Cycle

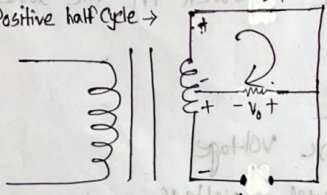


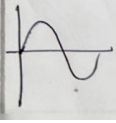


D_1, D_2 Open

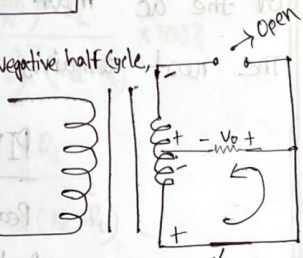
D_3, D_4 Short

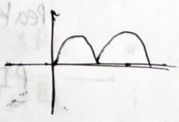
Positive half Cycle →





Negative half Cycle,





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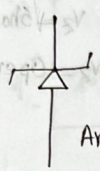
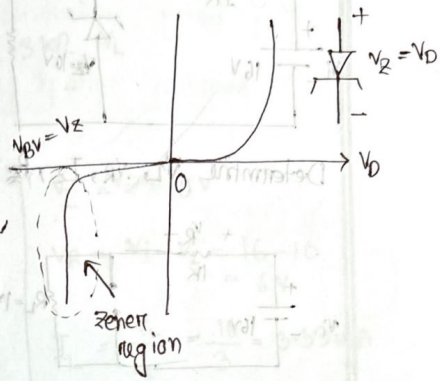
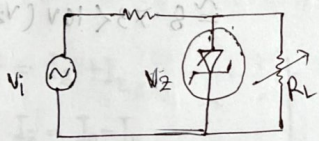
Topic Name : EEE-2141 Day : THRUSDAY Time : Date : 22 / 12 / 2022

Zener Diode :- Special type of Diode





- Heavily doped
- Works in reverse Bias
- work as voltage regulator



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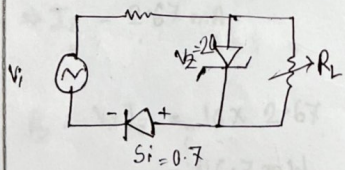

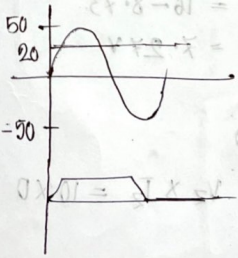

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Topic Name :

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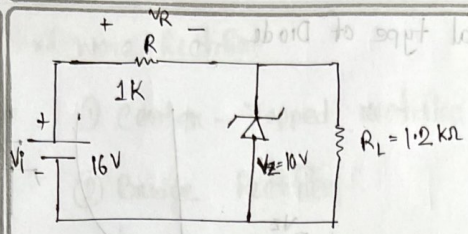
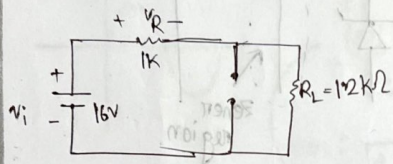


$V_{th} > V_Z$ = Short (ON)

$V_{th} < V_Z$ = Open (OFF)

Determine V_L, V_R, I_Z, P_Z?



$$V_{th} = \frac{R_L V_i}{R + R_L}$$

$$= \frac{1.2\ K\Omega\ (16V)}{(1+1.2)\ K\Omega}$$

$$\cong 8.73 < 10V\ (V_Z)$$

$$V_i - V_R - V_L = 0$$

$$\Rightarrow V_R = V_i - V_L$$

$$= 16 - 8.73$$

$$= 7.27\ V$$

$$I_Z = 0$$

$$P_Z = V_Z \times I_Z = 10 \times 0 = 0$$

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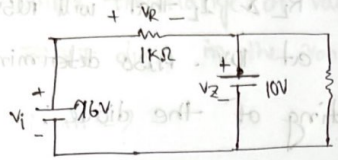
Topic Name : Day : Time : Date : / /



$$V_{th} = \frac{R_L V_i}{R+R_L}$$

$$= \frac{3 \times 16}{(1+3)}$$

$$\simeq 12V > 10V \ (V_Z)$$

$$V_L = V_Z = 10V$$

$$V_R = V_i - V_L = 16 - 10 = 6V$$

$$I_L = \frac{V_L}{R_L} = \frac{10}{3} = 3.33mA$$

$$I = I_Z + I_L$$

$$\Rightarrow I_Z = I_R - I_L$$

$$\Rightarrow I_Z = 6mA - 3.33mA$$

$$\Rightarrow I_Z = 2.67mA$$

$$I_R = \frac{V_R}{R_L} = \frac{6V}{1K\Omega} = 6mA$$

$$P_Z = V_Z I_Z = 10 \times 2.67$$

$$= 26.7mW$$

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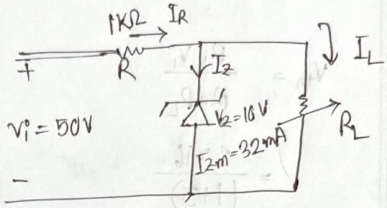
Topic Name : Day : Time : Date : / /

Determine the range of R_L & I_L that will result in V_{RL} being maintained at 10V. Also determine the maximum voltage rating of the diode.



$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

$$R_{Lmin} = \frac{V_Z R}{V_i - V_Z}$$

$$= \frac{10 \times 1}{50 - 10}$$

$$= 250\,\Omega$$

$$R_{Lmax} = \frac{V_Z}{I_{Lmin}}$$

$$= \frac{10}{8} = 1.25\,k\Omega$$

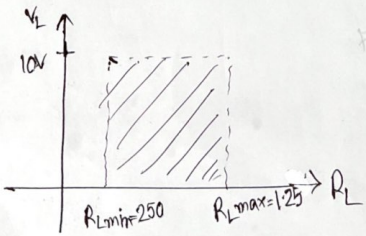
$$V_R = V_i - V_Z = 50 - 10 = 40\,V$$

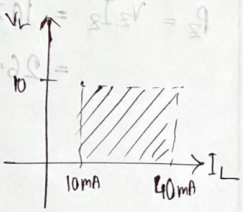
$$I_R = \frac{V_R}{R} = \frac{40V}{1k\Omega} = 40\,mA$$

$$I_{Lmin} = I_R - I_{Zm}$$

$$= 40 - 32$$

$$= 8\,mA$$





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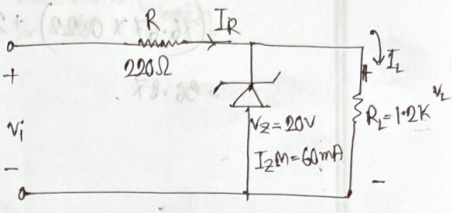
Topic Name : _____ Day : _____ Time : _____ Date : / /

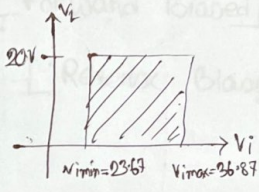
Determine the range of values of v_i that will maintain the zener diode in the on state.

$V_i\,min = ?$

$V_i\,max = ?$



$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$



$$\Rightarrow (R_L + R)V_Z = R_L V_i$$

$$\Rightarrow V_{imin} = \frac{V_Z(R_L + R)}{R_L}$$

$$= \frac{20(1200 + 220)}{1200}$$

$$= 23.63V$$

$$I_L = \frac{20}{1.2} = 16.67$$

$$\cancel{V_{imax} = V_Z} \qquad I_R = I_{ZM} + I_L$$

$$= 60 + \cancel{0.016}\,16.67$$

$$= \cancel{60.016}\ 76.67\ mA$$

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Topic Name : _____ Day : _____ Time : Date : / /

$$V_{1max} = V_R + V_2$$

$$= I_{Rmax} \times 0.22 + 20$$

$$= (76.67 \times 0.22) + 20$$

$$= 36.87$$

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Topic Name : EEE-2141 Day : THRUSDAY Time : Date : 29/ 12/ 2022

BJT (Bipolar Junction transistor)

2 Diodes

Three terminals :-

Electrons & hole } both

input (highly doped) • Emitter (E)

lightly doped • Base (B)

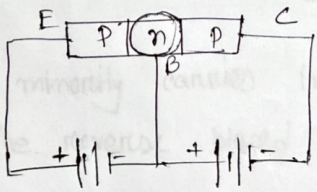
Output • Collector (C)

Two p-n Junctions

- Base - Emitter (BE) [forward Biased]
- Base - Collector (BC) [Reverse Biased]

BJT is a three layer semi-conductor device :-

- Two n- and one p layer (npn)
- Two p- and one n layer (pnp)



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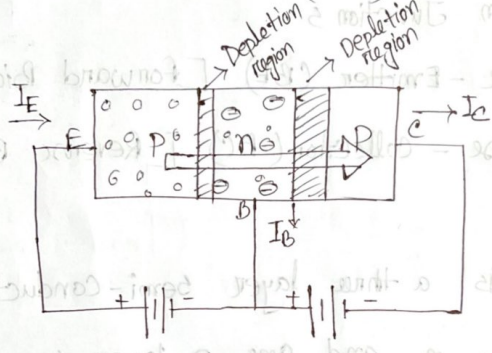
Topic Name : Day : Time : Date : / /

Q_1. BJT working principle

Q_2. 3 types of Configuration

⇒ Working principle of BJT

(PNP)



$$\boxed{I_E = I_B + I_C}$$

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Topic Name :- Day : Time : Date : / /

- Here both Biasing potentials have been applied to a pnp transistor.
- Many majority carries (holes) will diffuse accross the forward Biased p-n junction into the n-type material.
- These carries will contribute to base current (mA)
- The remaining majority carries will diffuse accross the reversed-biased junction into p-type material. connected to the collector terminal.
- The injected majority carries will appear as minority carries in the n-type ~~marat~~ material.
- All the minority carries in the depletion region will cross the reverse biased junction.

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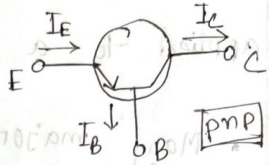
Topic Name : Day : Time : Date : / /

Applying Kirchoff's current law to the transistor,



$$I_E = I_B + I_C$$

$$I_E = I_B + I_{C\,major} + I_{C\,minor}$$

⇒ **Classification of BJT**

- Common Base
- Common Emitter
- Common Collector

input → V_{BE}

I_E (mA)

output → V_{CB}

I_C

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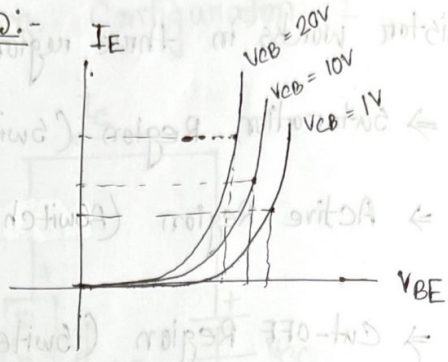
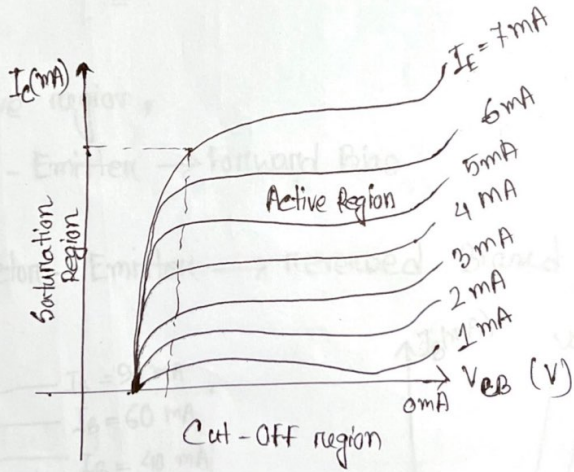
Topic Name : Day : Time : Date : /

Input Characteristics:-



Input

Output Characteristics:-



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Topic Name :

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- Transistor works in three region :-

  ⇒ Saturation Region (Switch-on)

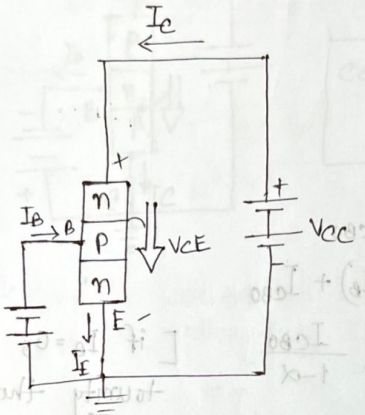
  ⇒ Active Region (Amplifier)

  ⇒ Cut-OFF Region (Switch-OFF)

Topic Name : EEE-2141 Day : MONDAY

Time : Date : 09 / 01 / 2023

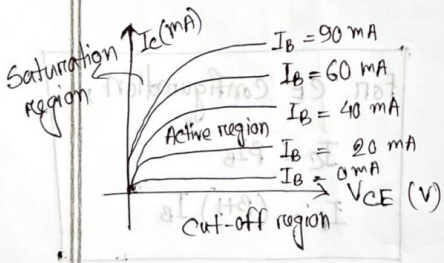
Common Emitter Configuration :-



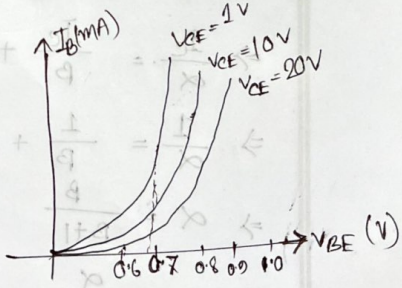
For Active region,

Base - Emitter → Forward Bias

Collector - Emitter → reversed Biased



Output Characteristics



input characteristics

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Topic Name : Day : Time : Date : / /

The following Emitter Configuration :-

$$I_E = I_B + I_C$$

$$\& \ \alpha = \frac{I_C}{I_E}$$

$$I_C = \alpha I_E + I_{CBO}$$

$$\Rightarrow I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$\Rightarrow I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

[if $I_B = 0$; α is close to unity then I_{CBO} is amplified]

Relation between α & β :-

$$I_E = I_B + I_C$$

$$\Rightarrow \frac{I_C}{\alpha} = \frac{I_C}{\beta} + I_C$$

$$\Rightarrow \frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\Rightarrow \alpha = \frac{\beta}{\beta+1}$$

$$\Rightarrow \beta = \frac{\alpha}{\alpha-1}$$

For CE configuration,

$$I_C = \beta I_B$$

$$I_E = (\beta+1) I_B$$

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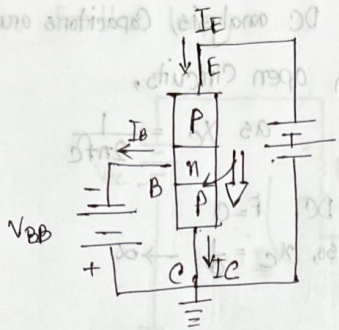
Topic Name : _____ Day : ____ Time : ____ Date : / /



Common collector Configuration

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Topic Name : EE 2142 Day : THRUSDAY Time : Date : 18 / 01 / 2023

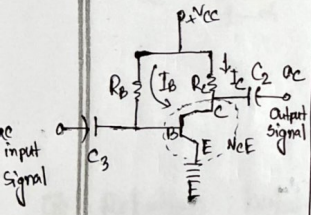
BJT DC Biasing :- For DC analysis, Capacitors are replaced with open circuits,

as $X_C = \frac{1}{2\pi f C}$

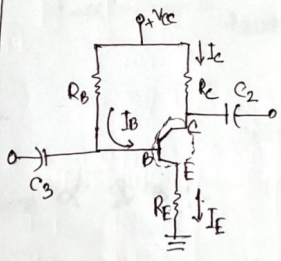
For DC, $F = 0$

so, $X_C = \frac{1}{0} \rightarrow \infty$

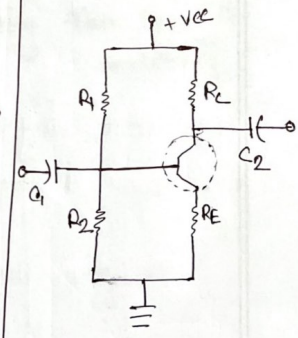
Fixed Bias Configuration



Emitter-Bias Configuration



Voltage Divider Configuration



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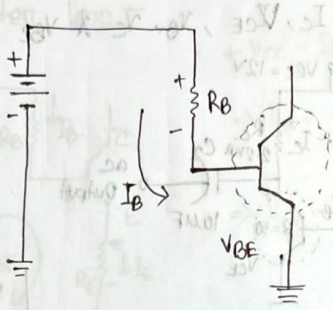
Topic Name : _____ Day : _____ Time : Date : / /

(i) Bias Emitter loop :-



$+V_{CC} - I_B R_B - V_{BE} = 0$

$\Rightarrow I_B = \dfrac{V_{CC} - V_{BE}}{R_B}$

[As V_{CC} & V_{BE} are constant, R_B is used to set I_B]

(ii) Collector - Emitter loop :-

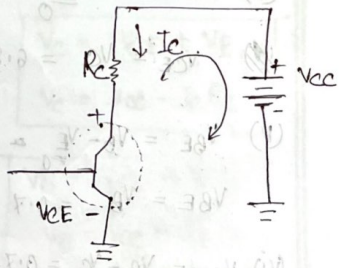
$I_C = \beta I_B$ [I_C is controlled by R_B]

$V_{CE} = V_{CC} - I_C R_C$ [R_C is controlled by V_{CE}]

$V_{CE} = V_C - V_E$

Since, $V_E = 0$

$V_{CE} = V_C$ & $V_{BE} = V_B$



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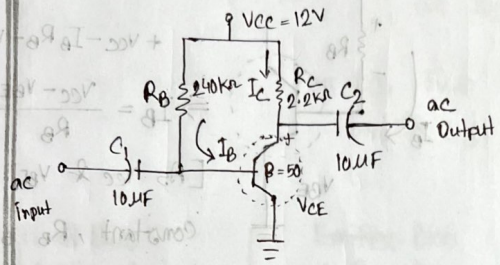
Topic Name : Day : Time : Date : / /

Math related to Fixed Bias –

Determine I_B, I_C, V_{CE}, V_B, V_C & V_{BC}



i) $I_B = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{12 - 0.7}{0.24}$ ($V_{BE} \to 0.7$)

$= 47.08 / 0.047$ mA

ii) $I_C = \beta I_B = 50 \times 0.047 = 2.35$ mA

(iii) $V_{CE} = V_{CC} - I_C R_C = 12 - (2.2 \times 2.35)$

$= 6.83$

(iv) $V_{CE} = V_C - \underset{0}{V_E}$

$V_{CE} = V_C = 6.83$

(v) $V_{BE} = V_B - \underset{0}{V_E}$

$V_{BE} = V_B = 0.7$

(vi) $V_{BC} = V_B - V_C = 0.7 - 6.83$

$= -6.13$

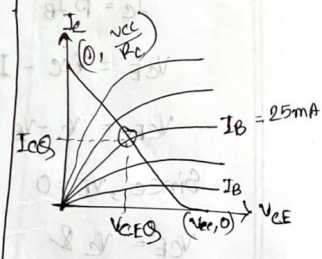
Load line analysis:-

$V_{CE} = V_{CC} - I_C R_C$

$\Rightarrow V_{CE} = V_{CC} \mid I_C = 0$ mA

&

$I_C = \dfrac{V_{CC}}{R_C} \mid V_{CE} = 0V$



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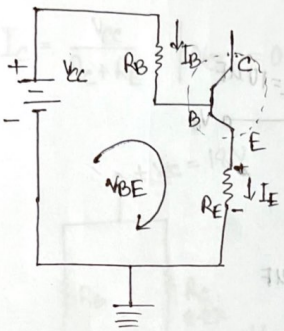
Emitter - Bias

(i) Base - Emitter Loop -



$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_E}$$

$$\Rightarrow V_{CC} - V_{BE} = I_B R_B$$

(ii) Collector - Emitter Loop -

$$+ I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

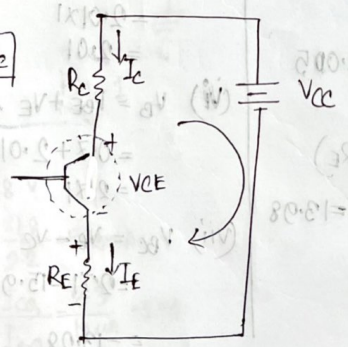
$$\Rightarrow V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$V_E = I_E R_E$$

$$\boxed{\begin{aligned} V_C &= V_{CE} + V_E \\ V_C &= V_{CC} - I_C R_C \end{aligned}}$$

$$\boxed{\begin{aligned} V_B &= V_{BE} + V_E \\ V_B &= V_{CC} - I_B R_B \end{aligned}}$$

$$\boxed{I_E \cong I_C}$$



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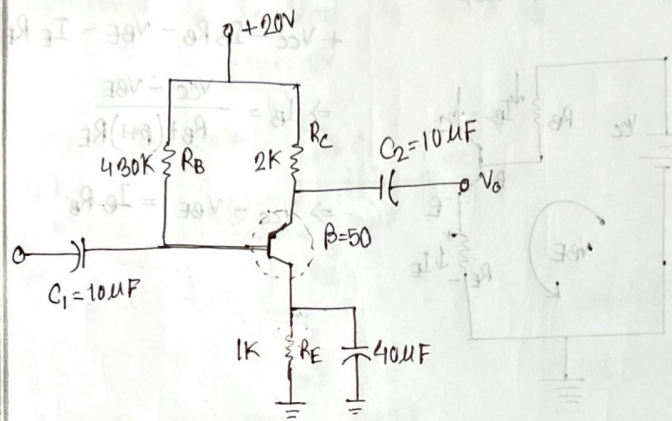
Determine I_B, I_C, V_{CE}, V_B, V_C, V_E, V_{BC}



(i) $I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_E} = 0.040mA$

$= 40.12\mu A$

(ii) $I_C = \beta I_B = 50 \times 0.04 = 2.005$

(iii) $V_{CE} = V_{CC} - I_C (R_C + R_E)$

$= 20 - 2.005(2+1) = 13.98$

(iv) $V_C = V_{CC} - I_C R_C$

$= 20 - 2.005 \times 2$

$= 15.99$

(v) $V_E = V_C - V_{CE}$

$\Rightarrow V_E = I_E R_E$ $\boxed{I_C \cong I_E}$

$= 2.01 \times 1$

$= 2.01$

(vi) $V_B = V_{BE} + V_E$

$= 0.7 + 2.01$

$= 2.71$

(vii) $V_{BC} = V_B - V_C$

$= 2.71 - 15.99$

$= -13.28$

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Load Line :-

$V_{CE} = V_{CC} \quad | \quad I_C = 0\,mA$

$I_C = \dfrac{V_{CC}}{R_C + R_E} \quad | \quad V_{CE} = 0\,V$

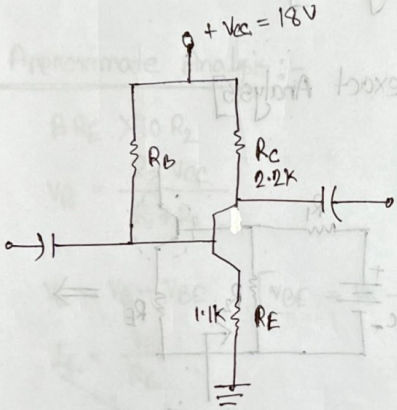

Fig-1

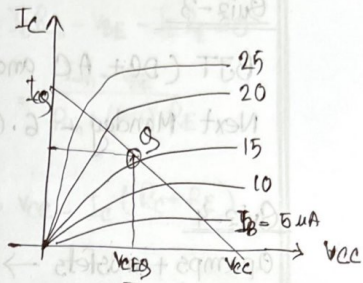

Fig -2

(i) Draw the load line of Fig-1 - on the characteristics for the transistor appearing in Fig-2.

(ii) For a Q point with a base current of 15μA, Find I_{CQ} & V_{CEQ}

(iii) Determine dc beta at Q point

(iv) using the beta, calculated value R_B & suggest a possible value.

$V_{CC} = 18\,V$

$I_C = \dfrac{18}{2.2} = 5.45\,mA$

$\beta = \dfrac{I_{CQ}}{I_{BQ}} = \dfrac{3.3}{15\,\mu A} = 220$

$R_B = 910\,k\Omega$

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Topic Name : EEE2141 Day : MONDAY Time : Date : 30 / 01 / 2023

Quiz-3

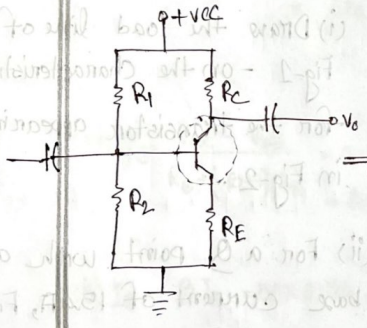
BJT (DC + AC analysis)

Next Monday - 6.02.23

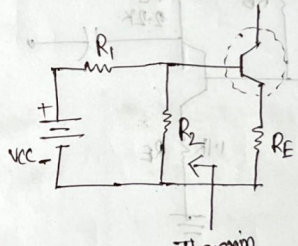
Quiz-4

Opamps + mosfets → [Assignment]

Voltage Divider Bias [exact Analysis]



⟹



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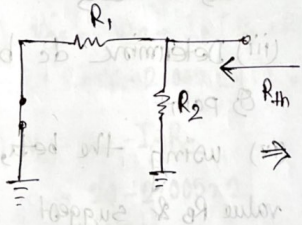

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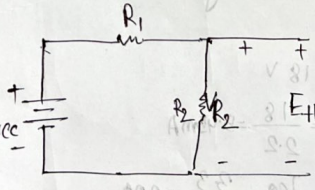

⟹

$$E_{th} = V_{R_2} = \frac{R_2 V_{cc}}{R_1 + R_2}$$

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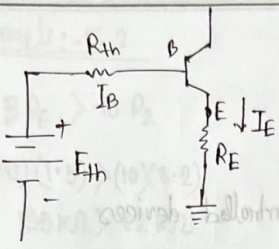

$$E_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

$$\Rightarrow I_B = \frac{E_{th} - V_{BE}}{R_{th} + (\beta+1) R_E}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$I_E = I_B + I_C$$
$$= I_B + \beta I_B$$
$$= I_B (\beta+1)$$

Approximate Analysis :-

$$\beta R_E > 10 R_2$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$V_E = V_B - V_{BE} \qquad [V_{BE} = V_B - V_E]$$

$$I_E = \frac{V_E}{R_E}$$

$$I_{CQ} \cong I_E$$

$$\boxed{V_{CEQ} = V_{CC} - I_C (R_C + R_E)}$$

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Topic Name : EEE 2141 Day : THRUSDAY Time : Date : 02 / 01 / 2023

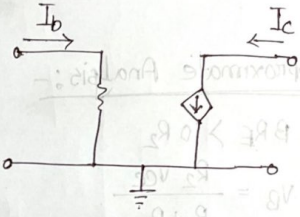
The r_e Transistor Model :-

BJT

Diode + Current Controlled devices

⇒ r_e model

$\beta r_e \parallel \beta I_b$



most important

$$\boxed{Z_i = (\beta+1) r_e \simeq \beta r_e}$$

⇒ Early voltage :-

$$r_o = \frac{\Delta V}{\Delta I} = \frac{V_A + V_{CEQ}}{I_{CQ}}$$

$$\text{Slope} = \frac{\text{Change output}, I_o}{\text{Change input}, \Delta V} = \frac{1}{r_o}$$

⇒ r_e model : voltage Divider bias

$$R' = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$Z_i = R' \parallel \beta r_e$$

$$Z_o = R_C \parallel r_o$$

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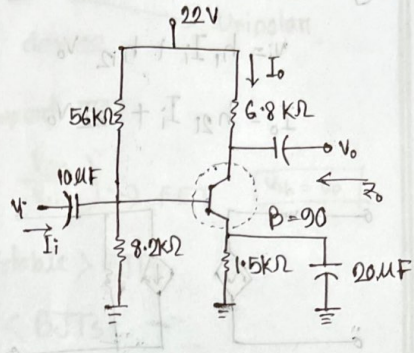
Example: 5.2 Exact / Approximate



(a) $\beta R_E > 10 R_2$

$(90)(1.5) > (10)(8.2)$

$135 K\Omega > 82 K\Omega$

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$= \frac{8.2}{56 + 8.2} \times 22$$

$$= 2.81 V$$

$$V_E = V_B - V_{BE} = 2.81 - 0.7 = 2.11 V$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11}{1.5} = 1.41 mA$$

$$r_e = \frac{26 mA}{I_E} = \frac{26}{1.41} = 18.44 \Omega$$

(b) $R' = R_1 \| R_2 = 56 \| 8.2 = 7.15 K\Omega$

$Z_i = R' \| \beta r_e = 7.15 \| (90)(18.44) = 1.35 K\Omega$

(c) $Z_o = R_C = 6.8 K\Omega$

(d) $A_v = -\frac{R_C}{r_e} = \frac{6.8}{18.44} = -368.76$

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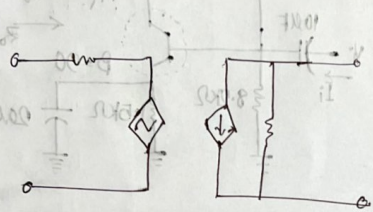
⇒ Hybrid equivalent model—

$$v_i = h_{11} I_i + h_{12} V_o$$

$$I_o = h_{21} I_i + h_{22} V_o$$



Fixed Bias Configuration –

$$Z_i = R_B \parallel h_{ie}$$

$$Z_o = R_C \parallel 1/h_{oe}$$

⇒ Example : 5.20 * Most important

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⇒ Field Effect Transistor (FET) → Unipolar

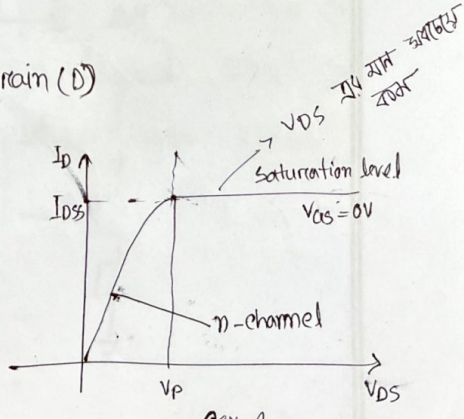
- Voltage Controlled device.
- V_{GS} → I_D depend করে।

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{th}}\right)^2 \rightarrow \text{FET} \quad \boxed{V_{th} = V_P}$$

- FETS more stable > BJTs
- FETS smaller < BJTs.
- higher input impedance (FET > BJT)

⇒ JFET (Junction Field Effect Transistor)

JFET → Source(S), Gate(G), Drain (D)



Gax-1

Topic Name : _____ Day : _____ Time : Date : / /

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

when, $I_D = I_{DSS}$

$$1 = \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\Rightarrow 1 = 1 - \frac{V_{GS}}{V_P}$$

$$\Rightarrow V_{GS} = 0$$

when, $V_{GS} = V_D$

$$I_D = I_{DSS}(1-1)^2$$

$$\Rightarrow I_D = I_{DSS}$$

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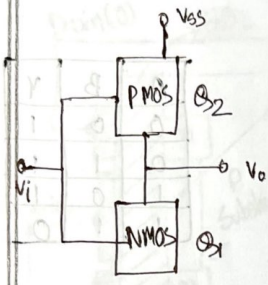
Topic Name : EEE 2141

Day : ~~SUN~~ MONDAY

Time :

Date : 06/ 02 / 2023

CMOS Inverter



(i) when V_i is 1, Q_1 = on,

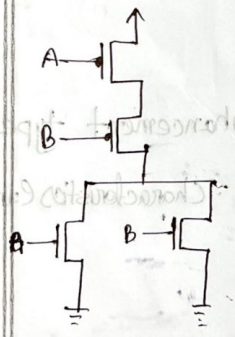
Q_2 = off, so, $V_o = 0$

(ii) when $V_i = 0$, Q_1 = off

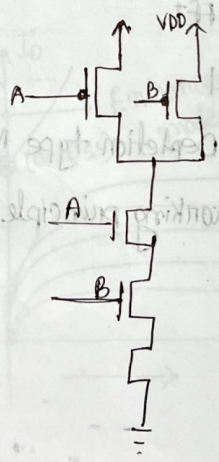
Q_2 = on, so, $V_o = 1$

A+B → PMOS (series)	A.B → PMOS (Parallel)
A+B → NMOS (Parallel)	A.B → NMOS (series)

NOR



NAND



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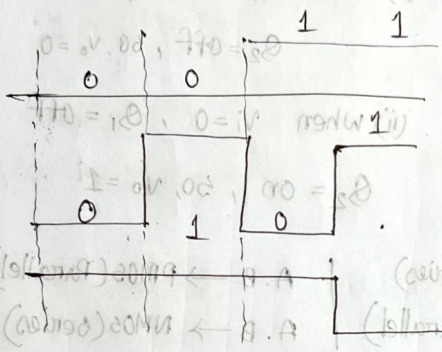
Timing Diagram

$Y = \overline{A.B}$



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

* BJT vs FET
* n channel
* JFET / Depletion type MOSFET / enhancement type MOSFET working principle with fig. Characteristics curve

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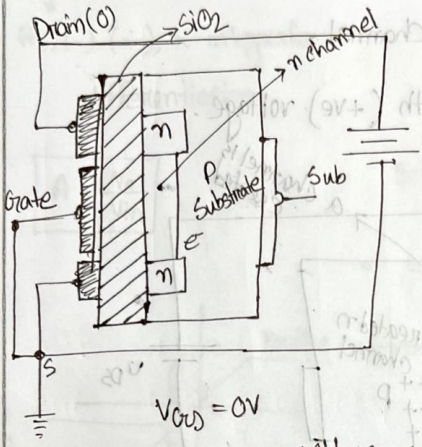
Topic Name : Day : Time : Date : / /

Depletion Type MOSFET (Same working Principle like JFET)

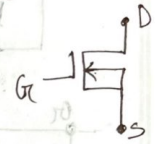


i) $V_{GS} = 0V$, $V_{DD} = +ve$

ii) $V_{GS} = -ve$, $V_{DD} = +ve$

+ve

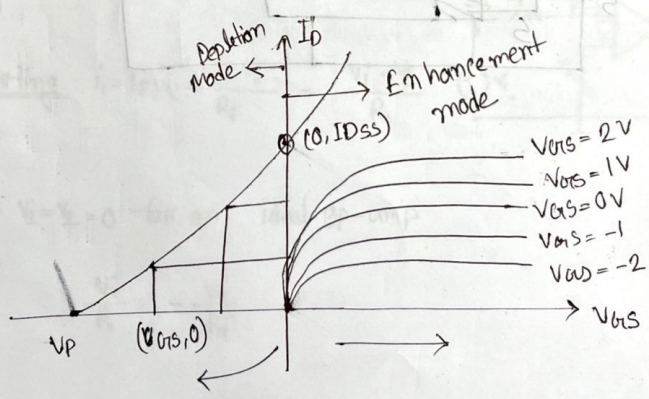
Symbol



$V_{GS} = 0V$

$V_{DD} = +ve$ voltage

n-channel Depletion mode Mosfet



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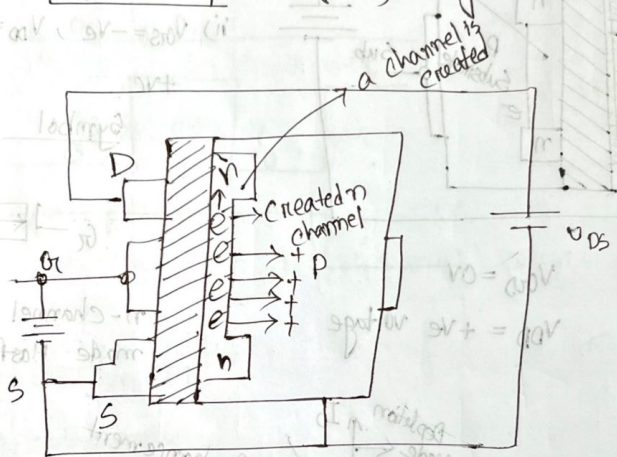
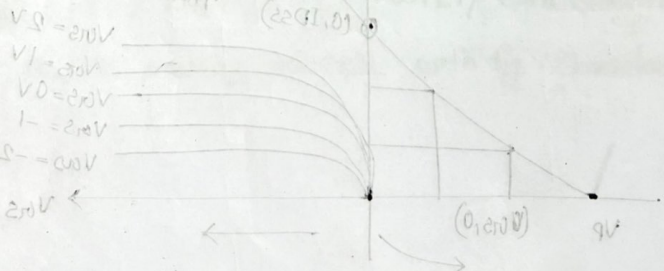
Enhancement type MOSFET

* absense of a- channel.
* V_{GS} & V_{DS} both (+ve) voltage.





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Topic Name : EEE 2141 Day : THRUSDAY

Time : Date : 09 / 02 / 2023

OP-amp

↓

(+), (−), (÷), × integration

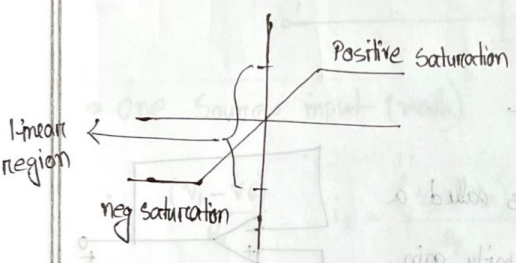
differentiation

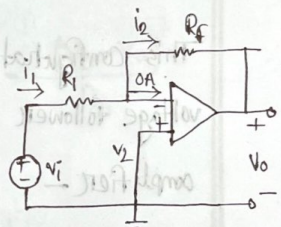
$$\boxed{A = \frac{V_o}{V_{in}}}$$

3-things → 2 → neg input

3 → positive input

6 → Output





Inverting $i_1 = i_2 = \frac{V_i - V_o}{R_f} = \frac{V_i - V_2}{R_1}$

But $V_1 = V_2 = 0$ for an ideal op-amp

$$\frac{V_i}{R_1} = -\frac{V_o}{R_f}$$

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Non - inverting Amp

$$i_1 = i_2 = \frac{0 - v_1}{R_1} = \frac{v_1 - v_0}{R_f}$$

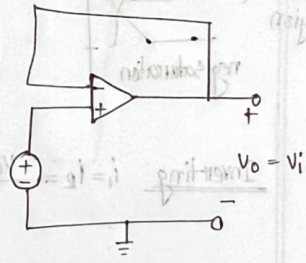
But $v_1 = v_2 = v_i$

$$\frac{-v_i}{R_1} = \frac{v_i - v_0}{R_f}$$

$$\boxed{v_0 = \left(1 + \frac{R_f}{R_1}\right) v_i}$$

This configuration is called a voltage follower or a unity gain amplifier -

$$v_0 = v_i$$



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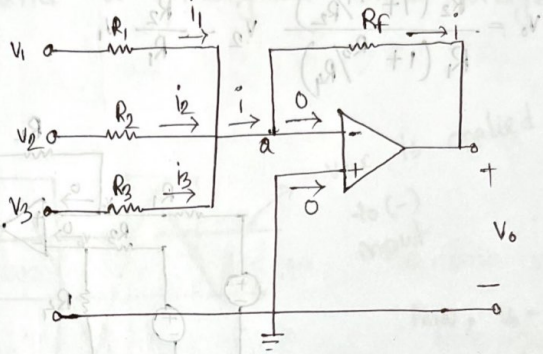
Summing Amplifier / Inverting Adder



* One Source input (math)

$$i_1 = \frac{(V_1 - V_a)}{R_1} \qquad i_2 = \frac{(V_2 - V_a)}{R_2} \qquad i_3 = \frac{(V_3 - V_a)}{R_3}$$

$$i = \frac{(V_a - V_o)}{R_f}$$

putting $V_a = 0$

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right)$$

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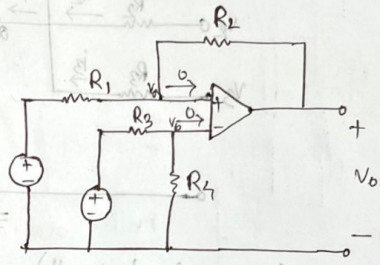
Difference Amplifier

$$V_o = \frac{R_2\left(1+ R_1/R_2\right)}{R_1\left(1+ R_3/R_4\right)} V_2 - \frac{R_2}{R_1} V_1$$



For the given circuit if true :

$$\frac{R_1}{R_2} = \frac{R_3}{R_4}$$

output $\longrightarrow$ $V_o = \frac{R_2}{R_1}\left(V_2 - V_1\right)$

if $R_2 = R_1$ & $R_3 = R_4$ diff amp becomes a subtractor,

$$V_o = V_2 - V_1$$

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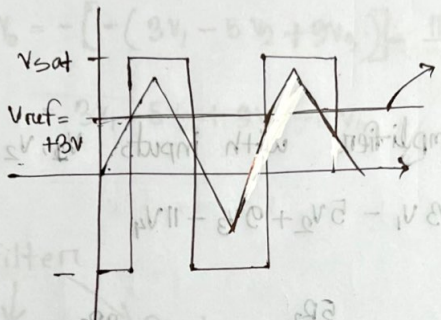
(*) Build a 3V level crossing detector using an op-amp and a triangular input voltage source

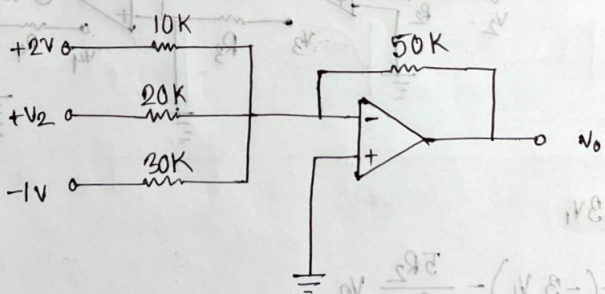


Vref is applied to (−) input

Now, $V_o = +V_{sat}$ when $E_i > V_{ref}$

$V_o = -V_{sat}$ when $E_i < V_{ref}$

(*)



Calculate the value of V_2 to make $V_o = 16.5$

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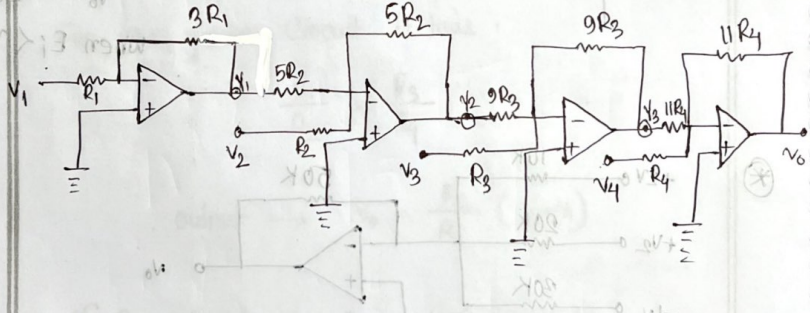
Topic Name : Day : Time : Date : / /

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right)$$

$$16.5 = -\left(\frac{50}{10} \times 2 - \frac{50}{20} V_2 + \frac{50}{30}(-1)\right)$$

$\Rightarrow V_2 = ?$

(*) Use difference amplifier with inputs V_1, V_2, V_3 & V_4 such that $V_o = 3V_1 - 5V_2 + 9V_3 - 11V_4$



$$V_1 = -3V_1$$

$$V_2 = -(-3V_1) - \frac{5R_2}{R_2} V_2$$

$$= 3V_1 - 5V_2$$

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Topic Name : Day : Time : Date : / /

$$V_3 = \left[-(3V_1 - 5V_2) - \frac{9R_3}{R_3} V_3 \right]$$

$$= -(3V_1 - 5V_2 + 9V_3)$$

$$V_o = -\left[-(3V_1 - 5V_2 + 9V_3) \right] - \frac{11R_4}{R_4} V_4$$

$$= 3V_1 - 5V_2 + 9V_3 - 11V_4$$

Filter

↓ active

→ Passive

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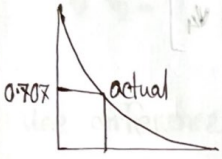
Topic Name : EEE 2141 Day : MONDAY Time : Date : 13 / 02 / 2023

Filter

low pass filter → high frequency cut করে

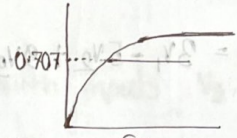
High Pass filter → low frequency cut করে



low pass filter

$H(0) = 0$

$H(\infty) = 1$

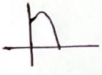


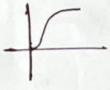
high pass filter

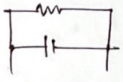
VVI

Band Pass Filter

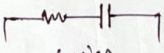
$V_i \rightarrow$ [low Pass] → [high Pass] → [Inverter] → V_o



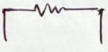




Parallel



Series



Normal

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Topic Name : _____ Day : _____ Time : Date : / /

(*) Construct a first-order active high pass filter with a high-frequency gain of 5 and a corners frequency of 200 Hz. Also derive the transfer function of the filter.

(i) we know,

$$w_c = 2\pi f$$

$$= (2\pi * 200)$$

also, $w_c = \frac{1}{R_i C_i}$

Given, $H(\omega) = -\frac{R_f}{R_i} = -5$

Let, $C_1 = 0.1\mu F = 0.1 \times 10^{-6} F$

$$w_c = \frac{1}{R_i C_i}$$

$$\Rightarrow 2\pi \times 200 = \frac{1}{R_i \times 0.1 \times 10^{-6}}$$

$$\Rightarrow R_i = 7.96 K$$

$$R_f = 5 \times 7.96 K = 39.78 K$$

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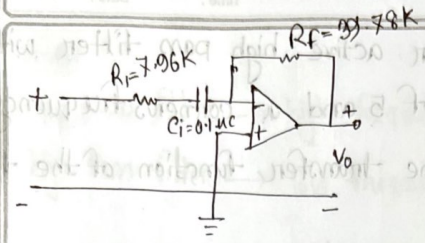
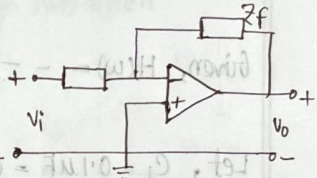


The design / ~~high Pass~~

Circuit of high Pass filter

(ii) $H(\omega) = \frac{V_o}{V_i} = \frac{-Z_f}{Z_i}$



$Z_i = R_i + \frac{1}{j\omega C_i}$

$Z_i = 7.96 + \frac{1}{j\omega(0.1\times10^{-6})}$

$Z_f = R_f$

$H(\omega) = -\frac{j\omega C_i R_f}{1 + j\omega C_i R_i}$

$= -\frac{j\omega \times 0.1 \times 39.78 \times 10^{-6}}{1 + j\omega \times 0.1 \times 10^{-6} \times 7.96}$

Transfer function

$H(\omega) = \frac{-j\omega\ 3.978 \times 10^{-6}}{1 + j\omega\ 7.96 \times 10^{-7}}$

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Topic Name : EEE 214 Day : THRUSDAY

Time : Date : 16 / 02 / 2023

(*) Design a square wave generator, using oscillation frequency = 5 KHz & Duty cycle 33%.

Given,

$f = 5KHz = 5 \times 10^3 Hz$

$D = 33\% = \frac{33}{100} = 0.33$

We know,

$T = \frac{1}{f} = \frac{1}{5 \times 10^3} = 2 \times 10^{-4} s$

Now, $D = \frac{t_{on}}{T}$

$\Rightarrow t_{on} = DT$

$\Rightarrow t_{on} = 6.6 \times 10^{-5} s$

Again, $T = t_{on} + t_{off}$

$\Rightarrow t_{off} = T - t_{on}$

$= 2 \times 10^{-4} - 6.6 \times 10^{-5}$

$t_{off} = 1.34 \times 10^{-4} s$

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Topic Name :

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Case 1 :-

If $R_2 = 0.86\ R_1$ then,

$t_{on} = R'C$

$t_{off} = R'C$

let $C = 0.05\ \mu F$

Now, $t_{on} = R'C$

$\Rightarrow R' = \frac{t_{on}}{C}$

$= \frac{6.6 \times 10^{-5}}{0.05 \times 10^{-6}}$

$= 1.32\ K$

Again, $t_{off} = R''C$

$\Rightarrow R'' = \frac{t_{off}}{C}$

$= \frac{1.34 \times 10^{-4}}{0.05 \times 10^{-6}}$

$= 2.68\ K\Omega$

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Topic Name : Day : Time : Date : / /

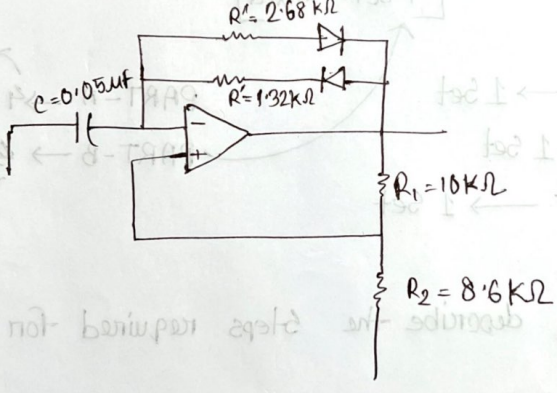
let us consider, $R_1 = 10K\Omega$

So if $\ln\left(\frac{R_1 + 2R_2}{R_1}\right) = 1$ then

$$\frac{R_1 + 2R_2}{R_1} = 2.72$$

$$\Rightarrow 2R_2 = 2.72 \times 10 - 10$$

$$\Rightarrow R_2 = 8.6K$$



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Topic Name : EEE 2141 Day : MONDAY

Time : Date : 20 / 02 / 2023

Diode → half-wave
full-wave
zener diode
clipper - clamper
} 2 set

OP-amp → 3 set → 2 set full op-amp

[OP amp + oscillator]

[1 set - mixed] → opamp + MOSFET

MOSFET → 1 set

BJT → 1 set

BJT + FET → 1 set

PART - A → 4 set → 3 set Ans

PART - B → 4 set → 3 set Ans

(*) Briefly describe the steps required for IC Fabrication.

(*) Discussion different regions of SCR's Characteristics Curve.

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