Topic Name: CSE 2105

Day: TuesDay

Time:

Date: 15 / 11 / 2022

Digital Logic Design

Course Teacher : Syeda Shabnam Hasan

Asst. Professor, CSE, AUST

- Combinational (easy) ***
- Sequencial (tough)

i) Digital ckt → Discrete values

ii) Analog ckt → Continuous values

$\underbrace{0, 1}_{\text{Bit}}$

(0-0.8) 0 → Low

(2-5) 1 → High

IC → Integrate Circuit

- SSI → Small scale integration
- MSI → Medium scale integration
- VLSI → very large scale integration

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Logic /Digital /Switching Circuit → input → 0,1 } → 0,1
Output → 0,1 } → ২ অবস্থা

two State → low & high

Basic logic Circuit → OR , AND , NOT

Gate :- One or more input but output Signal only one

Truth Table :- All output and input possibilities input listed in Binary Progression.

Word :- A string of bits that represent a coded instruction or data..

(*) For n inputs there are 2^n input Combinations.

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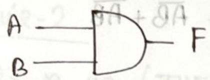
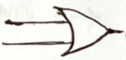
$F = AB$

$= A \cdot B$

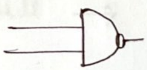


$= AB$

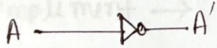
Symbol of AND Gate



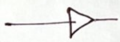
OR



NAND



Not



Buffer

(*) NAND and NOR → Universal Gate

NAND

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

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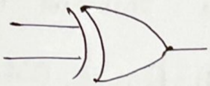
The Exclusive OR (EX-OR / X-OR) :-



$A \oplus B = \overline{A}B + A\overline{B}$

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

total num 1 is odd, output 1.

total num 1 is even, output 0.

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Quiz-1

6-12-2022 (TUESDAY) $\boxed{\text{Chapter - 1\&2}}$ (lec → 1 to 7)

Quiz-2

27-12-22 (TUESDAY)

Boolean Algebra & Logic Simplification:-

Boolean → always either true or false.

variable → represent a logical quantity.

complement → inverse of a variable.

$$A = 1 \;,\; \overline{A} = 0$$

Laws of Boolean Algebra:-

① Commutative Laws:-

$\Rightarrow A + B = B + A$

$\Rightarrow AB = BA$

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(2) Associative Laws :-

$$\Rightarrow A + (B + C) = (A + B) + C$$

$$\Rightarrow A(BC) = (AB)C$$

(3) Distributive Laws :-

AND distributive over OR :- $A(B+C) = AB + AC$

OR distributive over AND :- $A + BC = (A+B)(A+C)$

Rules of Boolean Algebra : 12 rules (must)

(*) Dual :- Operators and fixed values will be changed But variables will not be changed.

$$A + 1 = 1 \rightarrow A \cdot 0 = 0$$

$$A + B + C = 0 \rightarrow ABC = 1$$

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De-morgan's Theorem:-

1. $\overline{AB} = \bar{A} + \bar{B}$

2. $\overline{A+B} = \bar{A}.\bar{B}$

(1) L.H.S $A + \bar{A}C$

$= (A+\bar{A})(A+C)$ [using distributive law]

$= 1 \cdot (A+C)$

$= A+C$

= R.H.S

(2) L.H.S $= X + XY$

$= (X+X)(X+Y)$ $[A+BC = (A+B)(A+C)]$

$= X(X+Y)$ $[A+A = A]$

= R.H.S

(3) L.H.S $= X(\bar{X}+Y)$

$= X\bar{X} + XY$ $[A(B+C) = AB+AC]$

$= 0 + XY$

$= XY$

= R.H.S

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Simplification using Boolean Algebra :-

i. $AB + A(B+C) + B(B+C)$

$= AB + AB + AC + BB + BC$ [Distributive Law]

$= AB + AB + AC + B + BC$ [$BB = B$]

$= AB + AC + B + BC$ [$AB + AB = AB$]

$= AB + AC + B$ [$B + BC = B$]

$= B + AC$ [$AB + B = B$]

(Ans:)

ii. $[A\overline{B}(C+BD) + \overline{A}\,\overline{B}]C$

$= [A\overline{B}C + A\overline{B}BD + \overline{A}\,\overline{B}]C$

$= (A\overline{B}C + A.0.D + \overline{A}\,\overline{B})C$ [$B\overline{B} = 0$]

$= (A\overline{B}C + 0 + \overline{A}\,\overline{B})C$

$= (A\overline{B}C + \overline{A}\,\overline{B})C$

$= A\overline{B}CC + \overline{A}\,\overline{B}C$ [Distributive law]

$= A\overline{B}C + \overline{A}\,\overline{B}C$ [$CC = C$]

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$= \bar{B}C\,(A+\bar{A})$

$= \bar{B}C \cdot 1$

$= \bar{B}C$

$[A+\bar{A} = 1]$

(*) $F_3 = x'y'z + x'yz + xy'$

0 0 1 , 0 1 1 , 1 0

x	y	z	F_3
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Binary Code
└→ weighted
└→ unweighted

Digit (0-9)
Number 10 ≥

BCD (Binary - Coded Decimal) or 8,4,2,1 Code

15 → 0001, 0101

~~000~~(1 0101) → BCD

Excess - 3 Code :-

Decimal + 3 then যে সংখ্যা আসবে তার Binary

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2,4,2,1 Code :- The 2,4,2,1 Code is the same as that in BCD from 0 to 4; it varies from 5 to 9.

Decimal		2 4 2 1 Code	
0	→	0 0 0 0	Binary rule follow
1	→	0 0 0 1	
2	→	0 0 1 0	
3	→	0 0 1 1	
4	→	0 1 0 0	
5	→	1 0 1 1	MSB form
6	→	1 1 0 0	
7	→	1 1 0 1	
8	→	1 1 1 0	
9	→	1 1 1 1	

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Coding Conversion :-

$\boxed{\text{Table Design}} \rightarrow$ full

The Reflected Code / Gray Code :-

MSB →

Binary to Gray

Binary : 1 0 1 1 0

Gray : 1 1 1 0 1

$(10110)_2 = (11101)_{Gray}$

MSB →

Gray to Binary

Gray : 1 1 1 0 1

Binary : 1 0 1 1 0

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Parity Bit :- total number of 1 then extra bit add.

say message :- 10110 __

Odd parity :- P(odd) : 0

even parity :- P(even) : 1

Hamming Code :- * Only one bit change detector.
* Can't detect if more then one bit change.

1. Determine the single error correcting code for '101110110'
└ hamming

Solution :- The number of data bits, in the message, $n = 9$. We can obtain the required no. of parity bits (P) from the following formula :

$2^P >= n + P + 1$

if $P = 1$, $2^1 >= 9+1+1$ (false)

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if $P = 2$, $2^2 >= 9+2+1$ (false)

if $P = 3$, $2^3 >= 9+3+1$ (false)

if $P = 4$, $2^4 >= 9+4+1$ (true)

so, $P = 4$

we have to send total $m+n = 9+4 = 13$ bit message.

2 Power

	2^0	2^1		2^2				2^3					
Bit position	1	2	3	4	5	6	7	8	9	10	11	12	13
values :	P_1	P_2	1	P_3	0	1	1	P_4	1	0	1	1	0

0	0	1	1	3
0	1	1	0	6
0	1	1	1	7
1	0	0	1	9
1	0	1	1	11
1	1	0	0	12
XOR → 1	1	0	0	
P_4	P_3	P_2	P_1 ← LSB	

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⊛ 1010001110

$n = 10$ $2^P >= n+P+1$

if $P=1$, $2^1 >= 10+1+1$ (false)

$P=2$, $2^2 >= 10+2+1$ (false)

$P=3$, $2^3 >= 10+3+1$ (false)

$P=4$, $2^4 >= 10+4+1$ (true)

So, $P=4$

We have to send, $m+n = 10+4$
$= 14$

Bit position:-

1 (2^0)	2 (2^1)	3	4 (2^2)	5	6	7	8 (2^3)	9	10	11	12	13	14
P_1	P_2	1	P_3	0	1	0	P_4	0	0	1	1	1	0

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0	0	1	1	3
0	1	1	0	6
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13

XOR→ 1 1 1 1

P_4 P_3 P_2 P_1 ← LSB

The sending Message Code will be :- 11110101001110

<u>Receiving End:- Case - 1</u>

0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	1	0	6
1	0	0	0	8
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13

XOR→ 0 0 0 0 no error

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Case - 2

If there is an error in the 5th position while transmitting the receiver will get :-

11111101001110

0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
1	0	0	0	8
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13

XOR → 0 1 0 1

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All boolean expression can be converted into either of two standard forms: -

a. The sum- of products (SOP)

b. The product of sum (POS) [ভিতরে sum বাইরে Product]

<u>Canonical Form: -</u>

a sum of minterms.

a product of maxterms.

SOP

$$F = x'y'z + x'yz + xy'z' + xy'z$$

$$F(x,y,z) = \Sigma(\overset{1}{\cancel{001}}, \overset{3}{\cancel{011}}, \overset{4}{\cancel{100}}, \overset{5}{\cancel{101}})$$

$$\rightarrow F = \Sigma(1, 3, 4, 5)$$

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(*) $F = \Sigma(0, 2, 5, 7)$ Practice

$= \Sigma(000, 010, 101, 111)$

$F = x'y'z' + x'yz' + xy'z + xyz$

x	y	z	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

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minterm → যেসব input এর জন্য output 1 Calculate

maxterm → যেসব input এর জন্য Output 0 Calculate

↓

0 থাকলে Prime হবে না & 1 থাকলে Prime.

→ 0 থাকলে Prime & 1 থাকলে not prime.

Boolean to POS →

1. First use Distributive law
2. missing variable P, add PP'
3. All the variable in POS term.

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Minterm Complement Maxterm

$F(x,y,z) = 1$ means

$= \Sigma(0,1,2,3,4,5,6,7)$

$= \Pi(\text{NIL})$

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Chapter - 3

Karnaugh Map (K-Map)

2, 3, 4, 5, 6 ↓ Variable পর্যন্ত use করা যায় K-map

Truth table

A	B	F
0	0	0
0	1	1 ✓
1	0	0
1	1	1 ✓

$F = \Sigma(1,3)$

$F = A'B + AB$

$= B(A' + A)$

$= B$

K-map cell $\longrightarrow 2^n$ Here $\underline{n}$ is input variable.

MSB ⟵ A

A \ B	0	1
0	m_0 0	m_1 1
1	m_2 0	m_3 1

A \ B	0	1
0		1
1		1

→ 0 লেখার দরকার নেই

$2^n = 1, 2, 4, 8, 16, 32 \ldots\ldots$ $\boxed{\text{Group}}$

Ayisha

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$F = \Sigma(1,3)$

A \ B	B′ 0	B 1
A′ 0		1
A 1		1

$F = B$

$F = \Sigma(2,3)$

A \ B	B′ 0	B 1
A′ 0		
A 1	1	1

$F = A$

কর্নারের গুলো মিলে Group করেছে

1			1
1			1

① $F(A,B,C) = \Sigma(1,3,4,6)$

A \ BC	00 ($B'C'$)	01 ($B'C$)	11 (BC)	10 (BC')
A′ 0	m_0	m_1 1	m_3 1	m_2
A 1	m_4 1	m_5	m_7	m_6 1

$F = A'C + AC'$

$= A \oplus C$

(2) $F = \Sigma(0, 1, 2, 4, 6)$

A \ B	B'C' 00	B'C 01	BC 11	BC' 10
A' 0	m_0 1	m_1 1	m_3	m_2 1
A 1	m_4 1	m_5	m_7	m_6 1

~~$F = A'B' + AC' +$~~

$F = C' + A'B'$

(3) $F = \Sigma(1, 2, 3, 5, 7)$

A \ B	B'C' 00	B'C 01	BC 11	BC' 10
A' 0		1	1	1
A 1		1	1	

$F = C + A'B$

(4) $F = \Sigma(3, 4, 6, 7)$

A \ B	B'C' 00	B'C 01	BC 11	BC' 10
A' 0			1	
A 1	1		1	1

$F = BC + AC'$

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- ⊛ No zeros allowed.
- ⊛ No diagonals.
- ⊛ Only power of 2 number of cells in each group
- ⊛ Groups should be as large as possiable.
- ⊛ Everyone must be in at least one group.
- ⊛ Overlapping allowed.
- ⊛ Wrap around allowed.
- ⊛ Fewest number of groups possible.

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4 Variable K-Map

	AB \ CD	00 $C'D'$	01 $C'D$	11 CD	10 CD'
00	$A'B'$	m_0	m_1	m_3	m_2
01	$A'B$	m_4	m_5	m_7	m_6
11	AB	m_{12}	m_{13}	m_{15}	m_{14}
10	AB'	m_8	m_9	m_{11}	m_{10}

(i) $F(w,x,y,z) = \Sigma(0,1,2,4,5,6,8,9,12,13,14)$

(ii) $F(A,B,C,D) = \Sigma(0,1,2,5,8,9,10)$

(iii) $F(A,B,C,D) = \Pi(3,4,6,7,11,12,13,14,15)$

Practice :-

(i)

	wx \ yz	$y'z'$ 00	$y'z$ 01	yz 11	yz' 10
$w'z'$	00	1	1		1
$w'x$	01	1	1		1
wx	11	1	1		1
wx'	10	1	1		

$F = y' + w'z' + xz'$

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(ii)

AB \ CD	C'D' 00	C'D 01	CD 11	CD' 10
A'B' 00	1	1		1
A'B 01		1		
AB 11				
AB' 10	1	1		1

$F = B'D' + B'C + A'C'D$

(iii)

AB \ CD	C+D 00	C+D' 01	C'+D' 11	C'+D 10
A+B 00			0	
A+B' 01	0		0	0
A'+B' 11	0	0	0	0
A'+B 10			0	

$F = (C'+D')(A'+B')(B'+D)$

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⊛ Don't Care Conditions ('d'/'x')

$F = \Sigma(1, 3, 7)$

$F = \Sigma(0, 5)$

input : BCD digit (0–9) 4 bit

Output : Excess-3 Code 4 bit (12)

Minterm → don't care consider 1

Maxterm → don't care consider 0

Solve

A \ BC	B'C' 00	B'C 01	BC 11	BC' 10
A' 0	d	1	1	
A 1		d	1	

$\boxed{F = C}$

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Five - variable K-map :-

AB \ CDE	000	001	011	010	110	111	101	100
00	m_0	m_1	m_3	m_2	m_6	m_7	m_5	m_4
01	m_8	m_9	m_{11}	m_{10}	m_{14}	m_{15}	m_{13}	m_{12}
11	m_{24}	m_{25}	m_{27}	m_{26}	m_{30}	m_{31}	m_{29}	m_{28}
10	m_{16}	m_{17}	m_{19}	m_{18}	m_{22}	m_{23}	m_{21}	m_{20}

$F = \Sigma(0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 29, 31)$

AB \ CDE	$C'D'E'$	$C'D'E$	$C'DE$	$C'DE'$	CDE'	CDE	$CD'E$	$CD'E'$
$A'B'$	1			1	1			1
$A'B$		1	1			1	1	
AB		1	1			1	1	
AB'		1					1	

$F = A'BE' + BE + AD'E$

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6 - variable K-Map :-

ABC \ DEF	000	001	011	010	110	111	101	100
000	m_0	m_1	m_3	m_2	m_6	m_7	m_5	m_4
001	m_8	m_9	m_{11}	m_{10}	m_{14}	m_{15}	m_{13}	m_{12}
011	m_{24}	m_{25}	m_{27}	m_{26}	m_{30}	m_{31}	m_{29}	m_{28}
010	m_{16}	m_{17}	m_{19}	m_{18}	m_{22}	m_{23}	m_{21}	m_{20}
110	m_{48}	m_{49}	m_{51}	m_{50}	m_{54}	m_{55}	m_{53}	m_{52}
111	m_{56}	m_{57}	m_{59}	m_{58}	m_{62}	m_{63}	m_{61}	m_{60}
101	m_{40}	m_{41}	m_{43}	m_{42}	m_{46}	m_{47}	m_{45}	m_{44}
100	m_{32}	m_{33}	m_{35}	m_{34}	m_{38}	m_{39}	m_{37}	m_{36}

$F = \Sigma(6, 9, 13, 18, 19, 25, 27, 29, 41, 45, 57, 61)$

ABC \ DEF	000	001	011	010	110	111	101	100
000					1			
001		1					1	
011		1	1				1	
010			1	1				
110								
111		1					1	
101		1					1	
100								

$F = CE'F + A'B'C'DEF' + A'BD'EF + A'BC'D'E$

Chapter-4 (Combinational Logic)

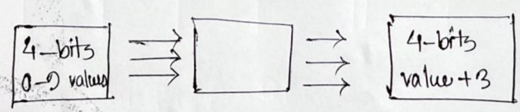
* Present combination of inputs without regard to previous inputs.

Design procedure of Combinational logic circuit :-

1. Determine input variables.
2. Determine output variables.
3. Derive the truth table.
4. Boolean expression / K-map → each output.
5. Produce the required circuit and verify it.

* BCD digit to Excess-3

digit ↓ (0-9) { যেহেতু এক digit & digit (0-9) → 9 (↓ max) লিখতে 4 bit দরকার



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* Design a 2-bit Cube Circuit :-

A	B	F_1 (16)	F_2 (8)	F_3 (4)	F_4 (2)	F_5 (1)
0	0	0	0	0	0	0
0	1	0	0	0	0	1
1	0	0	1	0	0	0
1	1	1	1	0	1	1

→ 3 এর Cube

A	B	C	F
0	0	0	→ 0
0	0	1	→ 0
0	1	0	→ 0
0	1	1	→ 0
1	0	0	→ 1
1	0	1	→ 0
1	1	0	→ 1
1	1	1	→ X

Cricket এ 4 & 6 এর জন্য light জ্বলবে।

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Magnitude Comparator :-

1 bit

input		Output		
X_i	Y_i	$F_1 (x_i > Y_i)$	$F_2 (x_i = y_i)$	$F_3 (x_i < Y_i)$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

$F_1 (x_i > y_i) = X_i Y_i'$

$F_2 (x_i = y_i) = X_i' Y_i' + X_i Y_i$

$= X_i \odot Y_i$

$F_3 (X_i < Y_i) = X_i' Y_i$

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$x = x_2\ x_1$

$y = y_2\ y_1$

$$F_1(x>y) = x_2 > y_2 + (x_2 = y_2)(x_1 > y_1)$$

$$F_1 = x_2 y_2' + (x_2 \odot y_2)\, x_1 y_1'$$

$$F_2(x==y) = (x_2 = y_2)(x_1 = y_1)$$

$$= (x_2 \odot y_2)(x_1 \odot y_1)$$

$$F_3 = (x_2 < y_2) + (x_2 = y_2)(x_1 < y_1)$$

$$= x_2' y_2 + (x_2 \odot y_2)\, x_1' y_1$$

$$\begin{array}{r} 0 \\ +0 \\ \hline 0 \end{array} \qquad \begin{array}{r} 0 \\ +1 \\ \hline 1 \end{array} \qquad \begin{array}{r} 1 \\ +0 \\ \hline 1 \end{array} \qquad \begin{array}{r} 1 \\ +1 \\ \hline 10 \end{array}$$

10: 0 → S, 1 → Cout

Half adder:-

X_i	Y_i	Cout	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

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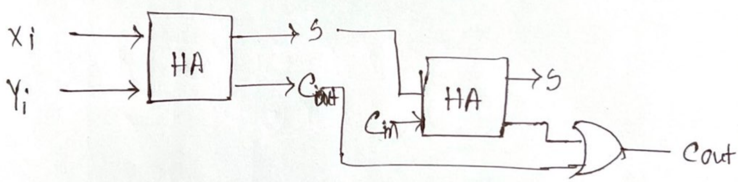
Full adder

A	B	C_{in}	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1



Half substractor

$$\begin{array}{r} 0 \\ -0 \\ \hline 0 \end{array} \qquad \begin{array}{r} 0 \\ -1 \\ \hline 11 \end{array} \qquad \begin{array}{r} 1 \\ -0 \\ \hline 1 \end{array} \qquad \begin{array}{r} 1 \\ -1 \\ \hline 0 \end{array}$$

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Time: Date: 20/12/2022

(*) একটা full adder দিয়ে 3 bit যোগ করা যায়।

Ripple Carry effect → একটা full adder অন্য adder এর উপর depend করে, তাই slow হয়ে যায়।

CLA (Carry Loop Adder)

Carry Propagate ← $P_i = A_i \oplus B_i$

$G_i = A_i B_i$

↓

Carry generate

$A - B$

$\Rightarrow A + 2's$ Complement of B

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BCD Adder :-

দুইটা BCD digit যোগ করবে (in parallel)

A(BCD digit) + B(BCD digit)

= SUM (BCD)

Maximum output $(9+9+1) = 19$

if C_{in} 1

binary output যেটা আসে আর BCD output যা আসে পার্থক্য 6.

binary output + 6 = BCD output

6 যোগ করা যাবে যখন output 9 এর বেশি হবে।

```
if ( sum >= 10)
   sum + = 6
else
   sum + = 0
```

→ যখন আমরা বুঝব output এর আগে 6 যোগ করা লাগবে না 0.

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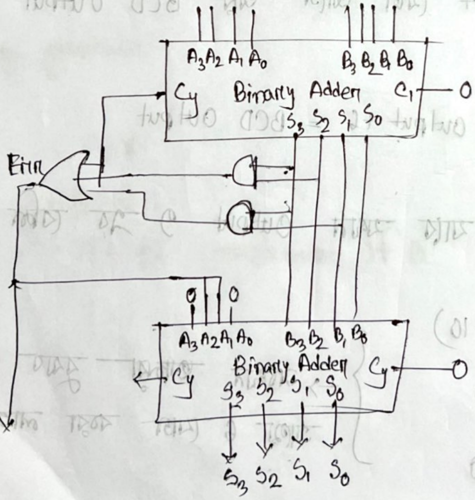
Carry out এর value 1 হলে 6 যোগ করব।

↳ C_{out} value 1 হয় 16, 17, 18 এর ক্ষেত্রে।

	Err
1010	1
1011	1
1100	1
1101	1
1110	1
1111	1

→ K map

$Err = S_3 S_2 + S_3 S_1$



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Switch Controlled adder / Substractor

$S = 0 \longrightarrow A+B$

$S = 1 \longrightarrow A-B$

$6+3 = 9$

$6-3 = 3$

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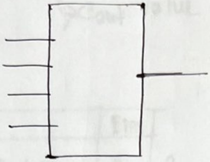
MULTIPLEXERS / MUX / DATA SELECTORS



input অনেক হতে পারে but output একটাই।

- ⇒ input lines $\rightarrow 2^n$
- ⇒ Single output line.
- ⇒ n selection lines.

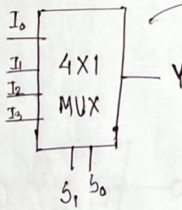
selector

n bit

2^n

S_1	S_0
0	0
0	1
1	0
1	1

2 bit $\rightarrow 2^2 = 4$



4টা input so 4X1 MUX

$\boxed{n \neq 0}$ selector 0 হতে পারবে না।

selector = n

$2^n \times 1 \rightarrow$ output line

↳ total input line

2টা input so 2X1 MUX

$\boxed{2^1 = 2}$

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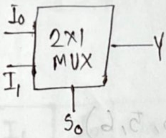
⇒ Function Table :- 4×1 MUX

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Output Equation :-

$$Y = S_1' S_0' I_0 + S_1' S_0 I_1 + S_1 S_0' I_2 + S_1 S_0 I_3$$

⇒ 2×1 MUX



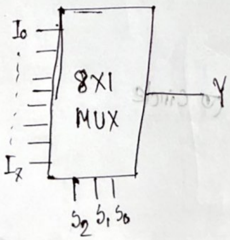
S_0	Y
0	I_0
1	I_1

$$Y = S_0' I_0 + S_0 I_1$$

⇒ 8×1 MUX

$2^3 = 8 \rightarrow$ input 8

$n = 3 \rightarrow$ selector



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Function implementation using MUX

$F(A, B, C)$

$n+1 = 3$

$\Rightarrow n = 2$

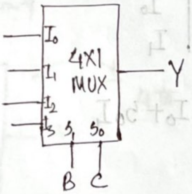
$2^n \times 1 \rightarrow 4\times1$ MUX

Selector $\rightarrow 2$

MSB

$\Rightarrow F(A, B, C) = \Sigma(1, 3, 5, 6)$

selector LSB নিতে হবে



MUX input line	I_0	I_1	I_2	I_3
A'	0	1	2	3
A	4	5	6	7
Input values	0	1	A	A'

কোনো Circle নেই

2টা circle

A তে Circle

A' তে Circle

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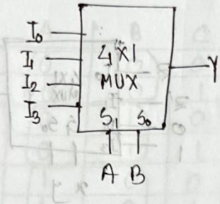
→ If A,B as selector



A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

MUX input line	I_0	I_1	I_2	I_3
C'	0	2	4	6
C	1	3	5	7
Input values	C	C	C	C'

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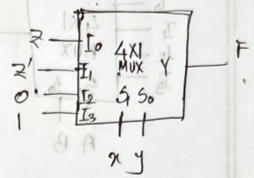
⊞ $F(x, y, z) = \Sigma(1, 2, 6, 7)$ using 4X1 MUX

x	y	z	F	
0	0	0	0	$\to F = z$
0	0	1	1	
0	1	0	1	$\to F = z'$
0	1	1	0	
1	0	0	0	$\to F = 0$
1	0	1	0	
1	1	0	1	$\to F = 1$
1	1	1	1	

Sequence follow করে S0 xy কে selector নিব



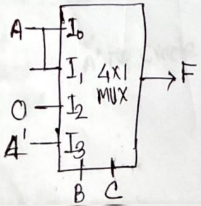
Implementation the following boolean expressions:-

(i) $F(A, B, C) = \Sigma(2, 3, 6, 7)$

(ii) $F(A, B, C) = \Sigma(0, 2, 5, 6)$ using 4X MUX

(iii) $F(A, B, C, D) = \Sigma(0, 1, 5, 6, 8, 10, 12, 15)$ using 8X1 MUX

(iv) For the given multiplexer ckt determine the logic function.



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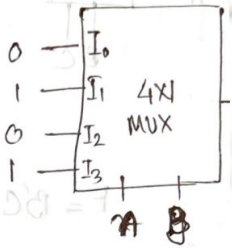
Soln :-

(i) $F(A,B,C) = \sum(2,3,6,7)$

A	B	C	F	
0	0	0	0	$\} \rightarrow F = 0$
0	0	1	0	
0	1	0	1	$\} \rightarrow F = 1$
0	1	1	1	
1	0	0	0	$\} \rightarrow F = 0$
1	0	1	0	
1	1	0	1	$\} \rightarrow F = 1$
1	1	1	1	



(ii) $F(A,B,C) = \sum(0,2,5,6)$

A	B	C	F	
0	0	0	1	$> C'$
0	0	1	0	
0	1	0	1	$> C'$
0	1	1	0	
1	0	0	0	$> C$
1	0	1	1	
1	1	0	1	$> C'$
1	1	1	0	

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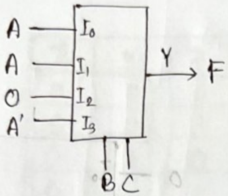
(iv) Solve :-



B	C	F
0	0	A
0	1	A
1	0	0
1	1	A'

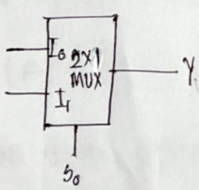
$$F = B'C'A + B'CA + BCA'$$

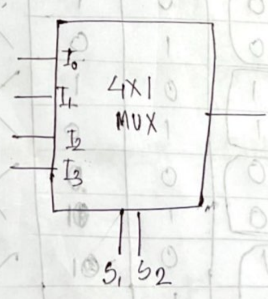
$$= AB'C' + AB'C + A'BC$$

$$= \Sigma(4, 5, 3)$$

$$= \Sigma(3, 4, 5)$$

Construct a 4X1 MUX using 2X1 MUX Only.





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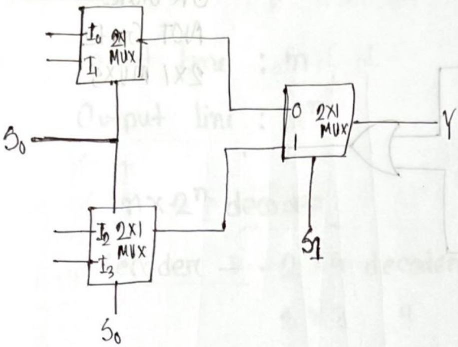

S_1	S_0	F
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Quad 2-to 1 MUX:-

Enable pin

- → Active low → E = 0 (0V)
- → Active high → E = 1 (+5V)

* Construct a 4X1 MUX using two 2X1 MUX, enable pin & basic gate(s).

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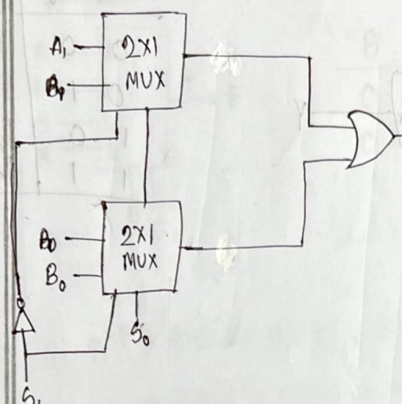
OR Gate
NOT Gate
2X1 MUXS



CSE 2105
Quiz-3
31-01-2023
TUESDAY
Chapter-4

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Topic Name: CSE-2105 Day: TUESDAY
Time: Date: 17 / 01 / 2021

Decoders

input line : n

Output line : 2^n

$n \times 2^n$ decoder

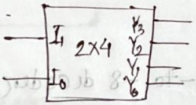
decoder → 2×4 decoder

3×8 4

4×16 4

2 to 4 Line Decoder :- (selector থাকে না)

2টা input 4টা output

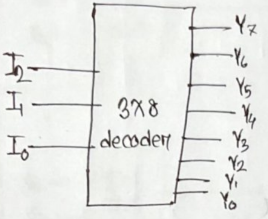


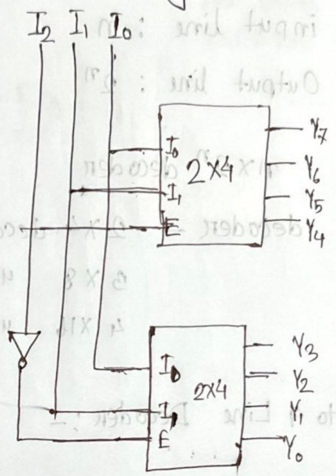
	I_1	I_0	Y_3	Y_2	Y_1	Y_0
0 →	0	0	0	0	0	1
1 →	0	1	0	0	1	0
2 →	1	0	0	1	0	0
3 →	1	1	1	0	0	0

Active High → 1 use হয়

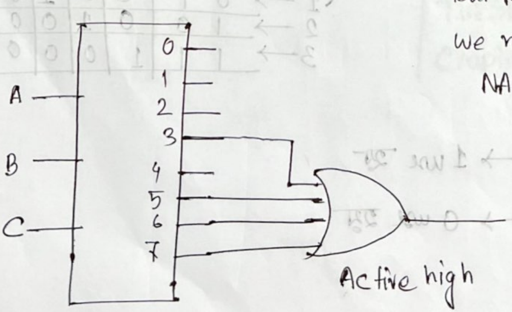
Active low → 0 use হয়

Design a 3x8 Line Decoder using 2x4 Decoders





4. $F = \Sigma(3, 5, 6, 7)$ using 3-to-8 decoder



Active high

But for active low we need to use NAND Gate

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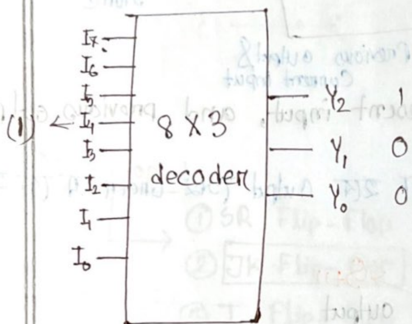
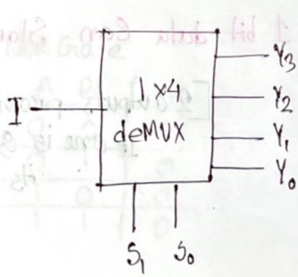
Encoders

Input lines — 2^n

Output lines — n



DeMultiplexers



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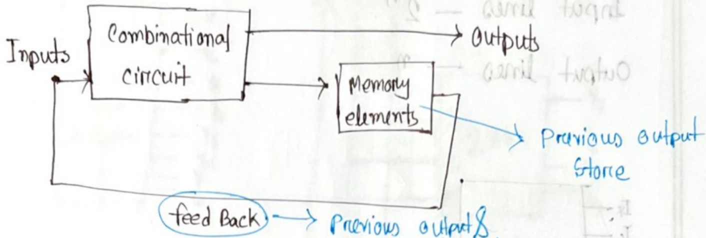
Chapter-5 (Synchronous Sequential Logic)

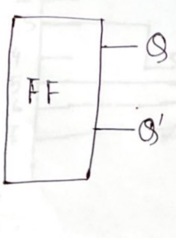


present output = f (Present input, and previous output)

⊛ Input যে Order এ দেয়া হবে, Output সেই Order এ বের হবে।

Present output (Q_t) next output (Q_{t+1})
=
Previous output (Q_t) Current Output (Q_{t+1})

FLIP FLOP (FF) → Only 1 bit data Can Store



[2 outputs provide :- If one is Q & another its not]

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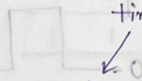
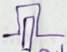
Sequential Circuit
- Asynchronous → Present Output → Current input & previous output
- Synchronous → Present output → Current input & Previous output, time



Clock



Pulse

Flip-Flop
- ① SR Flip-Flop
- ② $\boxed{\text{JK Flip-flop}}$ → LAB available
- ③ T Flip-flop
- ④ D Flip-flop

Basic Flip-flop Circuit → 2 NAND Gate or two NOR Gate can use to construct .

NOR Gate

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

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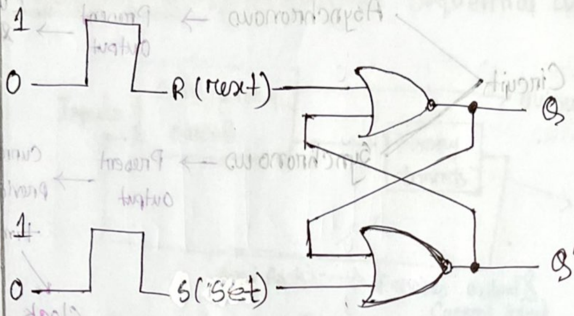

S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

Invalid state

Q & Q' can't be same

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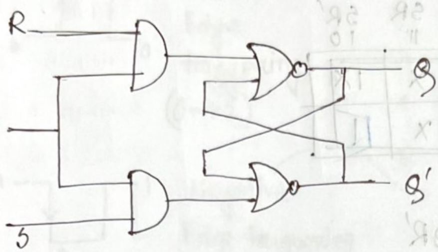
Clocked SR Flip-Flop

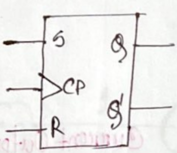


CP ↓ Clockpulse ↓ active-1 inactive-0

logic Diagram dependent

S	R	$Q_{(t+1)}$
0	0	Q
0	1	0
1	0	1
1	1	x

next output → Current input, prev output
$Q_{(t+1)}$ S, R Q_t



Q	S	R	$Q_{(t+1)}$	
0	0	0	0	
0	0	1	0	
0	1	0	1	
* 0	1	1	indeterminate	X
1	0	0	1	
1	0	1	0	
1	1	0	1	
* 1	1	1	indeterminate	X

$Q_{(t+1)}$ Q_t dependent

Q_t always 0

SR both can't be 1

Q এর value যাইহোক always 1 আসছে

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K-map use :-

Q \ SR	S'R' 00	S'R 01	SR 11	SR' 10
Q' 0			X	1
Q 1	1		X	1

$$Q_{(t+1)} = S + QR'$$

Most important ***

SR Flip-Flop (excitation table)

Q_t	$Q_{(t+1)}$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Current Output Q_t

desired Output $Q_{(t+1)}$

R এর value 0/1 যে কোনো টা হতে পারে

S এর value 0/1 যে কোনো টা হতে পারে

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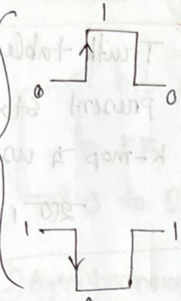
Day: TUESDAY

Time:

Date: 24/01/2023

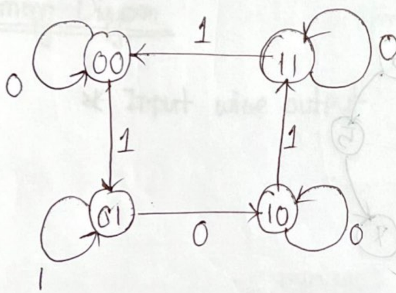
Clock pulse



Positive Edge triggering $(0 \rightarrow 1)$ — JK → Symbol

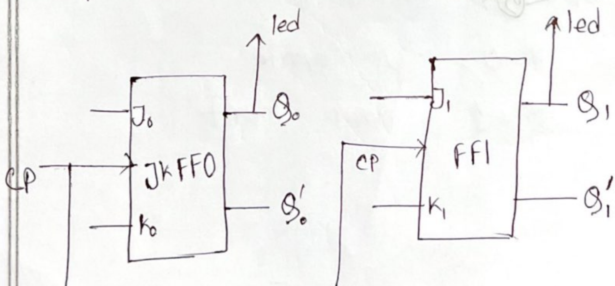
Negative Edge triggering $(1 \rightarrow 0)$ — JK → Symbol

JK-FF Negative Edge triggering



$00 + 0 \rightarrow 00$

$00 + 1 \rightarrow 01$

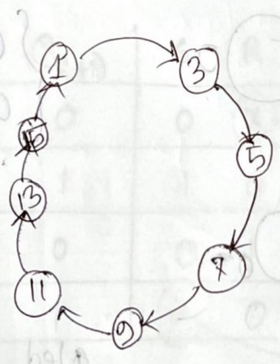


Q_t	Q_{t+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Truth table এর present state K-map এ use করতে হবে।

LAB

4-bit odd counter



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Chapter-6 (Registers & Counters)

n bit counter
↓
n FF
→ 0 to $2^n - 1$

(1) Synchronous Counter ⟶ Clock pulse same

(2) Asynchronous Counter (Ripple) ⟶ Clock pulse different

Timing Diagram

* Input wise output

Binary Up/Down Counter

* Up counter → small to large

2 bit up counter

↓

$\rightarrow 0 \rightarrow 1 \rightarrow 2 \rightarrow 3$

* down Counter → large to Small

2 bit down Counter

↓

$\rightarrow 3 \rightarrow 2 \rightarrow 1 \rightarrow 0$

⇒ 2 bit Up-down Counter:-

M=0 , Up Count

M=1 , down Count

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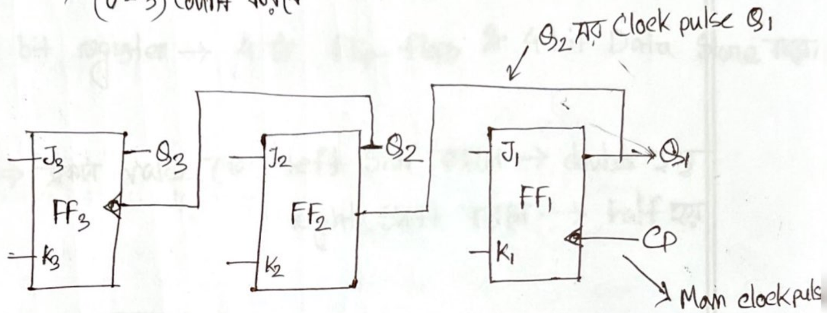
MOD N Counter :-

→ 0 to N-1 Counter

MOD 4 Counter / 2 bit binary Counter

→ (0-3) Count করবে



3 bit ripple counter (0-7)

FF_3 Q_3	FF_2 Q_2	FF_1 Q_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

(1-0) change

Clock Pulse আসে

BCD Ripple Counter
(0-9)
4bit use

$$\left.\begin{array}{l}\text{MOD - 12}\\ \text{MOD - 75}\\ \text{MOD - 100}\\ \text{MOD - 147}\end{array}\right\}\text{using decade Counter}$$

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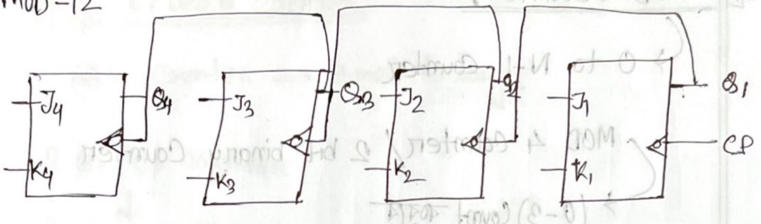
Time : Date : / /

MOD-12



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Topic Name : CSE 2105 Day : SUNDAY
Time : Date : 05/02/2023

REGISTER

↓

A Group of flip-flops.

⇒ flip-flops + Combinational gates.

⇒ 4 bit register → 4 টা flip-flops & 4 bit Data Store করে।

⇒ একটা value কে left shift করলে → double হয়
right shift করলে → half হয়

left shift $\boxed{\text{double}}$

4 → 0 1 0 0
8 → 1 0 0 0 → 8
0 1 0 0 → 4

right shift $\boxed{\text{half}}$

→ Universal Shift Register

S_1 S_0	Operation	
0 0	→ No change	→ A_3 A_2 A_1 A_0
0 1	→ Shift right	→ __ A_3 A_2 A_1
1 0	→ left shift	→ A_2 A_1 A_0 __
1 1	→ parallel load	→ I_3 I_2 I_1 I_0

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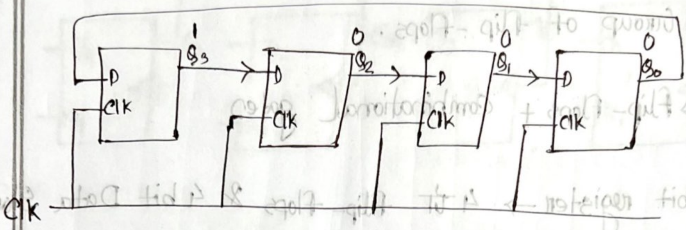
Ring Counter :-



	Q_3	Q_2	Q_1	Q_0
→	1	0	0	0
→	0	1	0	0
→	0	0	1	0
→	0	0	0	1

1 right Shift হলে যায়

Jhonson Counter

$Q_0' \rightarrow$ Inversion of output fed Back

Quiz-4
14-02-2023
Chapter - 5 & 6

Topic Name : CSE 2105 Day : TUESDAY
Time : Date : 07/02/2023

Quine-McCluskey / Tabulation Method

easily Simplify করা যায়।

- Determination of prime implicants
- Selection of prime implicants

Example :-

$$F(a,b,c,d) = \Sigma(0,1,2,5,6,7,8,9,10,14)$$

$$= \Sigma(0000, 0001, 0010, 0101, 0110, 0111, 1000, 1001, 1010, 1110)$$

Implicant Chart

Mismatch bit এ dash বসবে

পাশাপাশি গ্রুপ ধরতে পারবে

	Column 1		
Group 0	0000 ✓	(0,1) 000_ ✓ (0,2) 00_0 ✓ (0,8) _000 ✓	(0,1,8,9) _00_ (0,2,8,10) _0_0
Group 1	1 0001 ✓ 2 0010 ✓ 8 1000 ✓	(1,5) 0_01 (1,9) _001 ✓ (2,6) 0_10 ✓ (2,10) _010 ✓ (8,9) 100_ ✓ (8,10) 10_0 ✓	(2,6,10,14) __10
Group 2	5 0101 ✓ 6 0110 ✓ 9 1001 ✓ 10 1010 ✓	(5,7) 01_1 (6,7) 011_ (6,14) _110 ✓ (10,14) 1_10 ✓	
Group 3	7 0111 ✓ 14 1110 ✓		

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Topic Name: Day: Time: Date:

(*) prime implicant :- (যে গুলোতে টিক পড়ে নি)

$$a'c'd + a'bc + a'bd + b'c' + b'd' + cd'$$

একটা X খুঁজতে হবে।

PIs	abcd		0	1	2	5	6	7	8	9	10	14
(0,1,8,9)	_00_	$b'c'$	X	X					X	X		
(0,2,8,10)	_0_0	$b'd'$	X		X				X		X	
(2,6,10,14)	__10	cd'			X		X				X	X
(1,5)	0_01	$a'c'd$		X		X						
(5,7)	01_1	$a'bd$				X		X				
(6,7)	011_	$a'bc$					X	X				

X থেকে যে eqn আসবে সেগুলোর decimal টিক দিতে হবে then যে ঘর বাকি থাকবে সেটার eqn করবে।

Ans: $b'c' + cd' + a'bd$

Topic Name: CSE2105 Day: THRUSDAY

Time: Date: 09/02/2023

1. It is required to design a ckt to compute the equation $Y = X \bmod 5$, where is, X is a 4 bit unsigned number you can use decoder, Encoder, & additional logic gates if needed.

Solve:-

	X							
	X_3	X_2	X_1	X_0		Y_2	Y_1	Y_0
0 →	0	0	0	0	→	0	0	0
1 →	0	0	0	1	→	0	0	1
2 →	0	0	1	0	→	0	1	0
3 →	0	0	1	1	→	0	1	1
4 →	0	1	0	0	→	1	0	0
5 →	0	1	0	1	→	0	0	0
6 →	0	1	1	0	→	0	0	1
7 →	0	1	1	1	→	0	1	0
8 →	1	0	0	0	→	0	1	1
9 →	1	0	0	1	→	1	0	0
10 →	1	0	1	0	→	0	0	0
11 →	1	0	1	1	→	0	0	1
12 →	1	1	0	0	→	0	1	0
13 →	1	1	0	1	→	0	1	1
14 →	1	1	1	0	→	1	0	0
15 →	1	1	1	1	→	0	0	0

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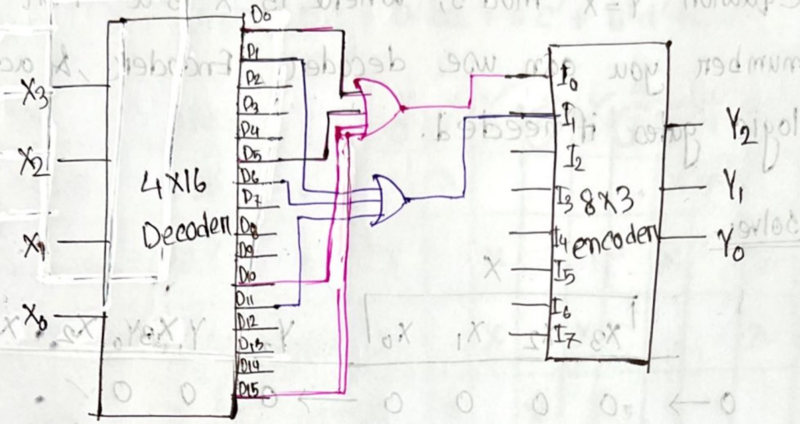
Topic Name : Day : Time : Date : / /



2. Draw a ckt that accepts a 3 bit input A(A_2, A_1, A_0) and Output a 2 bit number B(B_1, B_0) that is equal to the number of 1's that appear in the input A. You can use decoder, encoder & OR Gates.

	A_2 (4)	A_1 (2)	A_0 (1)	B_1 (2)	B_0 (1)
0 →	0	0	0	0	0
1 →	0	0	1	0	1
2 →	0	1	0	0	1
3 →	0	1	1	1	0
4 →	1	0	0	0	1
5 →	1	0	1	1	0
6 →	1	1	0	1	0
7 →	1	1	1	1	1

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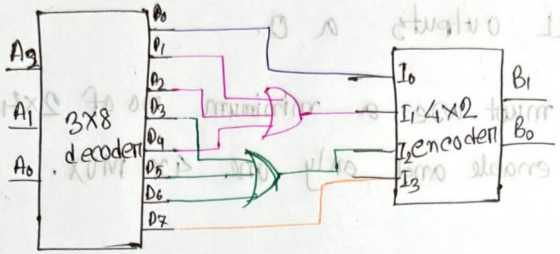

3. Implement a 1X16 demultiplexer using only 2 to 4 decoders with enable inputs & no other logic gates.

4. Using 2X4 decoders & one 4X1 MUX, design a ckt with the following properties. It has two 2 bit binary number inputs X (x_1 x_0), Y (y_1 y_0) and 2 f_1, f_0

- EQ outputs a 1, if X == Y
- GT outputs a 1, if X > Y

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Topic Name : Day : Time : Date : / /

– LTE outputs a 1, if $x <= Y$

– NULL outputs a 0.

You must use a minimum no of 2x4 decoders with enable and only one 4x1 MUX.

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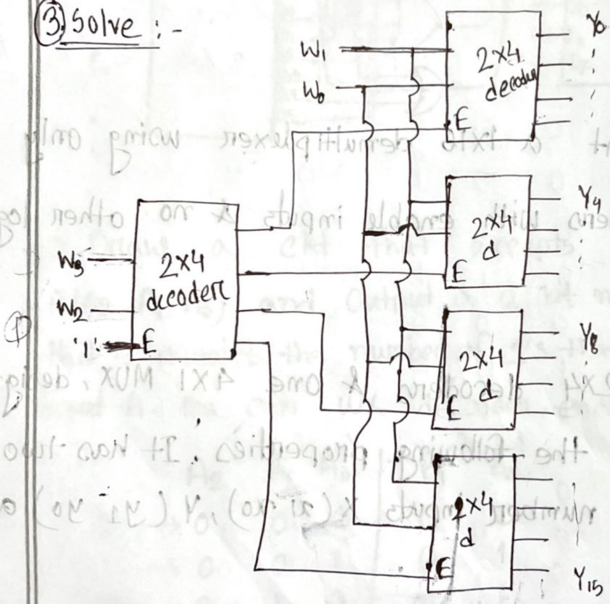
Topic Name : Day : Time : Date : / /

- LTE outputs a 1, if $x <= Y$
- NULL outputs a 0.

You must use a minimum no of 2x4 decoders with enable and only one 4x1 MUX.

③ Solve :-



$0,1,2,3 \rightarrow w_3 w_2 = 00$

$4,5,6,7 \rightarrow w_3 w_2 = 01$

④ Solve:-

X		Y		$X == Y$	$x > y$	$x <= y$	0
X_2	X_1	Y_2	Y_1	EQ	GT	LTE	NULL
0	0	0	0	1	0	1	0
0	0	0	1	0	0	1	
0	0	1	0				
0	0	1	1				
0	1	0	0				
⋮							
1	1	1	1				

$EQ = \Sigma(0, 5, 10, 15)$

$GT = \Sigma(4, 8, 9, 12, 13, 14)$

$LTE = \Sigma(0, 1, 2, 3, 5, 6, 7, 10, 11, 15)$

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