

Date of Examination: 06.03.2024

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department: Computer Science and Engineering

Program: Bachelor of Science in Computer Science and Engineering

Semester Final Examination: Spring 2023

Year: 2nd Semester: 1st

Course Number: CSE 2105

Course Name: Digital Logic Design

Time: 3 (Three) hours

Full Marks: 70

Instruction: There are 3 (Three) questions. Answer all of them.

Marks allotted are indicated in the right margin.

Question 1. Answer any 2 questions.

[Marks: 16]

a) A combinational circuit has four inputs and one output. The output F is equal to 1 when all the inputs are equal to 1 or none of the inputs are equal to 1 or an odd number of inputs are equal to 1. [8]

- (i) Derive the truth table for F .
- (ii) Write the canonical SOP expression for F .
- (iii) Write the canonical POS expression for F .
- (iv) Simplify the function F using Boolean Algebra. Show your work and list which Axiom or Theorem you used in each step.

b) It is necessary to multiply two binary numbers, each two bits long, in order to form their product in binary. Let the two numbers be represented by A_1, A_0 and B_1, B_0 , where subscript 0 denotes the least significant bit. Find the simplified Boolean expressions for each output using K-Maps. [8]

c) Minimize the following Boolean function F by using the Quine–McCluskey method: [8]

$$F(w, x, y, z) = \sum (0, 1, 2, 8, 10, 11, 14, 15)$$

Question 2. Answer any 3 questions.

[Marks: 30]

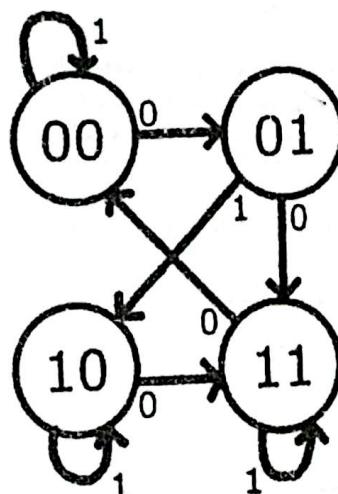
a) Design a circuit that uses the 4-bit adder and any other basic logic gates that you think you might need to compute the equation $P = 3*Q+1$. Assume that you have a 3-bit input Q (Q_2, Q_1, Q_0) and a 5-bit output P (P_4, P_3, P_2, P_1, P_0). Clearly label all inputs and outputs. [10]

- b) Implement a circuit that accepts a 3-bit input number A (A_2, A_1, A_0) and outputs a 2-bit number B (B_1, B_0) that is equal to the number of 1's that appear in the input A. Your circuit should be designed using the minimum number and sizes of decoder, encoder and additional logic gates if needed. Show clearly the size of all used components. [10]
- c) Construct a 4-bit register with four D flip-flops and 4-to-1 multiplexers with mode selection input S_1 and S_0 . The register operates according to the following function table: [10]

Table I: Function table

S_1	S_0	Register Operation
0	0	No Change
0	1	Complement the four Output
1	0	Clear register to 0
1	1	Load parallel data

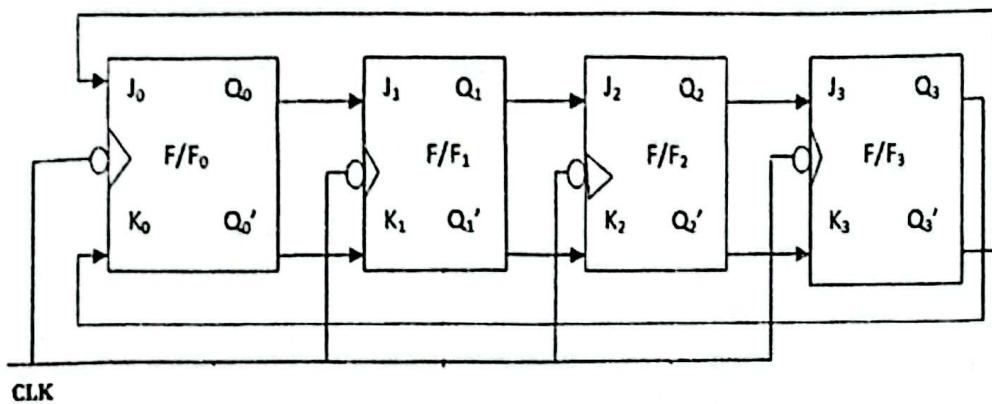
- d) Implement a sequential circuit specified by the following state diagram using T flip-flops: [10]



Question 3. Answer any 3 questions.

[Marks: 24]

- a) For the circuit below, draw a timing diagram for ten clock pulses, showing the Q_3 , Q_2 , Q_1 and Q_0 outputs and counting sequences in relation to the clock. Assume that the initial values of Q_3 , Q_2 , Q_1 and Q_0 are 0,0,0 and 0 respectively. [4+4]



b) Explain the working principle of a MOD 11 asynchronous up counter using negative edge triggered T flip-flops with active clear inputs. [8]

c) Explain the design procedure of a 4-bit comparator circuit. [8]

d) Show the use of Hamming code in detecting and correcting a single bit error for "100101010101" during transmission. [8]

Date of Examination: 03.11.24

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department: Computer Science and Engineering

Program: Bachelor of Science in Computer Science and Engineering

Semester Final Examination: Fall 2023

Year: 2nd Semester: 1st

Course Number: CSE 2105

Course Name: Digital Logic Design

Time: 3 (Three) hours

Full Marks: 70

Instruction: There are 3 (Three) questions. Answer all of them.

Marks allotted are indicated in the right margin.

Question 1. Answer any 2 questions.

[Marks: 16]

a) A museum has three rooms, each with a motion sensor (m_1, m_2 , and m_3). At night, the only person in the museum is one security guard who walks from room to room. The security system sounds an alarm (by setting an output A to 1) if motion is ever detected in more than one room at a time. [8]

- (i) Derive the truth table for A .
- (ii) Write the canonical SOP expression for A .
- (iii) Write the canonical POS expression for A .
- (iv) Simplify the function A using Boolean Algebra. Show your work and list which Axiom or Theorem you used in each step.

b) A combinational circuit computes the equation $Y=X \bmod 16$, where X is a 4-bit unsigned number. [8] Find the simplified Boolean expressions for each output using K-Maps.

c) Minimize the following Boolean function F by using the Quine–McCluskey method: [8]

$$F(p, q, r, s) = \sum(2, 6, 8, 9, 10, 11, 14, 15)$$

Question 2. Answer any 3 questions.

[Marks: 30]

- a) Let $A = A_3A_2A_1$ and $B = B_3B_2B_1$ be two 3-bit binary numbers in 2's complement representation. [10] You are given three full adders, one NOT gate, and six XOR gates. Your task is to design a circuit that can perform two different arithmetic operations: $A-B$ and $B-A$. The operation is selected by

one of the inputs to this circuit that is called S . When $S=0$ the 3-bit result $R = R_3R_2R_1$ is equal to $A-B$. Alternatively, when $S=1$ the result is $B-A$. Design the block diagram for the specified circuit. Clearly label all inputs and outputs.

(b) Implement a JK flip-flop using a D Flip-flop, a 2X1 MUX and an inverter. [10]

(c) Construct a 4-bit Universal Shift Register using JK flip flops and 4X1 MUXs with the following [10] capabilities:

- A shift-right control (associate with serial in/out)
- A toggle control (toggle the output of each flip flop)
- A parallel-load control (to parallel load input bits)
- A control signal to leave register unchanged

(d) Gray codes have a useful property in that consecutive numbers differ in only a single bit position. [10] The Gray code representation for the numbers 0 to 7 is given in Table 1. Design a MOD 8 Gray code counter with no external input and three outputs using T flip-flops. When reset, the output should be 000. On each clock edge, the output should advance to the next gray code. After reaching 100, it should repeat with 000.

Table 1: Gray Codes

Number	Gray Code
0	000
1	001
2	011
3	010
4	110
5	111
6	101
7	100

Question 3. Answer any 3 questions.

[Marks: 24]

(a) Describe the working principle of a switch controlled 2-bit synchronous up- down counter using [8] negative edge triggered T flip-flops.

b) Explain the design procedure of a 4-bit Carry Look Ahead Adder (CLA) circuit. [8]

Show the use of Hamming code in detecting and correcting a single bit error for "10110110001" [8] during transmission.

For the circuit below, draw a timing diagram for ten clock pulses, showing the Q_3 , Q_2 , Q_1 and Q_0 outputs and counting sequences in relation to the clock. Assume that the initial values of Q_3 , Q_2 , Q_1 and Q_0 are 1,1,1 and 1 respectively. [4+4]

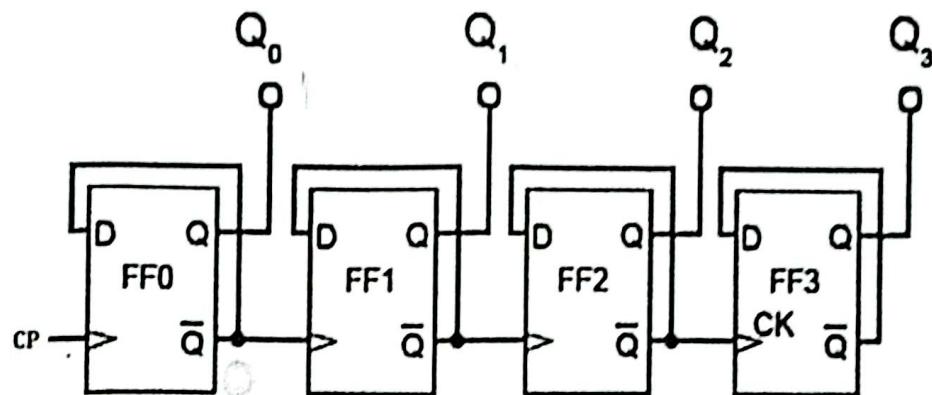


Fig 1: Asynchronous circuit with D flip-flops

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department: Computer Science and Engineering

Program: Bachelor of Science in Computer Science and Engineering

Semester Final Examination: Fall 2022

Year: 2nd Semester: 1st

Course Number: CSE 2105

Course Name: Digital Logic Design

Time: 3 (Three) hours

Full Marks: 70

Instruction: There are 3 (Three) questions, from which you have to answer any 2 (Two) questions in total from Question no. 1,
any 4 (Four) questions in total from Question no. 2
and
any 4 (Four) questions in total from Question no. 3

Marks allotted are indicated in the right margin.

Question 1. Answer any 2 questions.

[Marks: 14]

✓ 2) A function F has four inputs x, y, z, w and one output such that the output is 1 if and only if the [2+1.5+
number of 1s in the inputs is exactly two. 1.5+2]

- Derive the truth table for F .
- Write the canonical SOP expression for F .
- Write the canonical POS expression for F .
- Simplify the function F . Show your work and list which Axiom or Theorem you used in each step.

b) Simplify the following Boolean functions:

[5+2]

- Simplify F using K-Map, together with the don't-care conditions d , and then express the simplified function in sum of minterms:

$$F(A, B, C, D) = \sum (0, 6, 8, 13, 14), \quad d(A, B, C, D) = \sum (2, 4, 10)$$

- Reduce the following expression to a minimum number of literals using the postulates and theorems of Boolean Algebra:

$$F(A, B) = (A+B)'(A'+B)'$$

✓ Minimize the following Boolean function F by using the Quine-McCluskey method:

[7]

$$F(w, x, y, z) = \sum (1, 4, 6, 7, 8, 9, 10, 11, 15)$$

Question 2. Answer any 4 questions.

[Marks: 1]

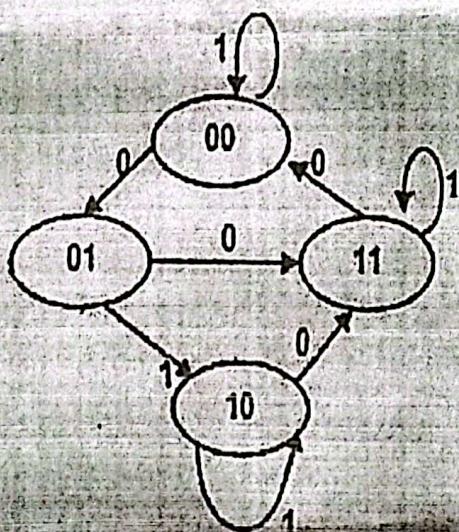
a) Devise a two-bits counter with inputs "up" and "down" (in addition to the common clock) using two JK flip-flops. A third SR flip-flop stores whether or not the counter should currently be counting "up" or "down"; the "up" input makes the clock start counting "up" and the "down" input makes the clock start counting "down". [7]

b) Implement a 3-input XOR gate using only a 4×1 multiplexer and an inverter. Also complete the truth table with the correct labels and function solution. [3+2+2]

c) Construct a 4-bit register with four D flip-flops and 4×1 multiplexers with mode selection input S_1 and S_0 . The register operates according to the following function table: [7]

	S_1	S_0	Register Operation
0	0	0	No Change
1	0	1	Complement the four Output
2	1	0	Clear register to 0
3	1	1	Load parallel data

d) Implement a sequential circuit specified by the following state diagram using D flip-flops: [7]



AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department: Computer Science and Engineering

Program: Bachelor of Science in Computer Science and Engineering

Semester Final Examination: Spring 2022

Year: 2nd Semester: 1st

Course Number: CSE 2105

Course Name: Digital Logic Design

Time: 3 (Three) hours

Full Marks: 70

Instruction: There are 7 (Seven) questions, from which you have to answer any 5 (Five) questions in total, including the Question no. 1 (One) and Question no. 2 (Two), which are mandatory for everyone.

Marks allotted are indicated in the right margin.

Question 1. [Marks: 14]

- (a) Describe duality principle with an example. [2]

- (b) Simplify the following expression using the postulates and theorems of Boolean algebra: [4]

$$\overline{(ABC)}(A+C)(A+\overline{C})$$

$$P(A \oplus A)$$

- (c) Determine the single error correcting code for "101110110". [8]

$$\begin{array}{cccccc} 0 & 0 & 1 & 1 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 & 1 & 1 & 0 \end{array}$$

Question 2. [Marks: 14] ✓

- (a) What is don't care condition? Simplify the following Boolean function F using Karnaugh map, together with the don't-care conditions d: [2+4]

$$F(A, B, C, D) = \sum (1, 3, 5, 7, 9, 15), d(A, B, C, D) = \sum (4, 6, 12, 13) \quad D(A^1 + A^2 + A^3)$$

- (b) Simplify the following Boolean function F by using the Quine-McCluskey method: [8]

$$F(w, x, y, z) = \sum (0, 1, 2, 8, 10, 11, 14, 15)$$

Question 3. [Marks: 14]

- a) Design a 4-bit BCD adder using 4-bit binary adders. [6]

- b) Design a synchronous counter that counts through the 3-bit prime numbers downwards using clocked D flip-flops. [8]

Question 4. [Marks: 14]

- a) Design a four input combinational circuit with one output to determine whether a given 4-bit number is in Fibonacci sequence or not. In your design, the output should "1", if the corresponding input is a Fibonacci number and "0" otherwise. [6]
- b) Draw the circuit diagram of four-bit universal shift register and describe its operation. [8]

Question 5. [Marks: 14]

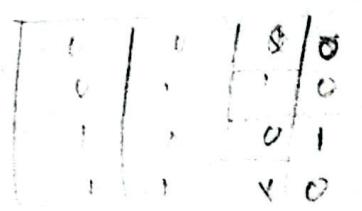
- a) Implement 8X1 multiplexer using a 3X8 decoder and basic logic gates. [6]
Appropriately label the inputs and outputs.
- b) Design a basic flip-flop circuit with NAND gates. [8]

Question 6. [Marks: 14]

- a) What are the differences between a combinational and a sequential circuit? Draw the logic diagram of a 4-bit Johnson counter and show its count sequence for 8 pulses. [2+4]
- b) What is carry look-ahead adder (CLA)? Construct a 4-bit CLA circuit. [1+7]

Question 7. [Marks: 14]

- a) Construct a JK flip-flop using a D flip-flop, a 4-to-1-line multiplexer and an inverter. [6]
- b) Design a 3-bit magnitude comparator. [8]



AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department: Computer Science and Engineering

Program: Bachelor of Science in Computer Science and Engineering

Semester Final Examination: Fall 2021

Year: 2nd Semester: 1st

Course Number: CSE2105

Course Name: Digital Logic Design

Time: 3 (Three) hours

Full Marks: 70

Instruction: There are seven questions carrying a total of 14 marks each. Answer any five questions.
 Marks allotted are indicated in the right margin.

Question 1. [Marks: 14]

- a) Demonstrate by means of truth tables the validity of De Morgan's theorem for three variables. [3]
- b) Simplify the following Boolean function, using Karnaugh Map: [4]
 $F(A,B,C,D) = A'B'D' + A'CD + A'BC$
 $d = A'BC'D + ACD + AB'D'$
- c) Design a three-bit combinational circuit 2's complementer. (The output generates the 2's complement of the input binary number). Show that the circuit can be constructed with exclusive-OR gates. [7]

Question 2. [Marks: 14]

- a) Implement a full-subtractor with two half-subtractor and an OR gate. [3]
- b) Design a BCD-to-excess-3 code converter using a 4-bit full adder. What must be done to change the circuit to an excess-3-to-BCD code converter? [4]
- c) Simplify following Boolean function F using the Quine-McCluskey method: [7]
 $F(A,B,C,D) = \sum(0,1,5,7,10,13,15)$

Question 3. [Marks: 14]

- a) Implement a full adder using two 4×1 multiplexers. [3]
- b) Design a circuit that can check if two 3-bit numbers are equal or not i.e., it produces a 1 only if a 3-bit number $A_2A_1A_0$ is equal to another 3-bit number $B_2B_1B_0$. [4]
- c) Obtain the output expression for a 8 to 3-line priority encoder, where the priorities are as follows: [7]
 $I_4 > I_3 > I_0 > I_1 > I_2 > I_5 > I_6 > I_7$

Question 4. [Marks: 14]

- a) Design a 4-bit ALU that operates based on the function table given below using logic gates, binary adders and multiplexers. [10]

S2	S1	S0	ALU Function
0	0	1	A OR B
0	1	1	A - B
1	0	0	A AND B
1	1	1	A XOR B

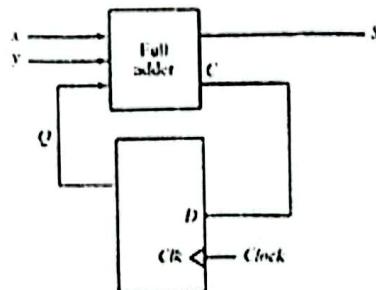
- b) Design a multiplier circuit which can implement 3-bit by 2-bit multiplication. [4]

Question 5. [Marks: 14]

- a) Transform the SR-FF to T-FF and also derive the excitation table.
- b) A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in the figure below. Derive the state table and state diagram of the sequential circuit.

[3]

[4]



- c) Design a binary counter that counts through the 3-bit even numbers upwards using D flip-flops.

[7]

Question 6: [Marks: 14]

- a) What is the difference between serial and parallel transfer? Explain how to convert serial data to parallel. What type of register is needed?
- b) Draw the timing diagram of a 4-bit Johnson counter for five clock pulses.
- c) Draw the logic diagram of a four-bit register with four D flip-flops and four 4×1 multiplexers with mode selection inputs S_1 and S_0 . The register operates according to the following function table:

[3]

[4]

[7]

S_1	S_0	Register Operation
0	0	No change
1	0	Complement the four outputs
0	1	Clear register to 0
1	1	Load Parallel

Question 7. [Marks: 14]

- a) What is the difference between asynchronous circuit and synchronous circuit?
- b) What is race-around condition? Explain how this can be avoided in J-K flip flop.
- c) Explain how, the invalid condition of S-R latch can be eliminated using J-K latch. Use block diagram and truth table for explanation.

[2]

[4]

[8]

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department: Computer Science and Engineering

Program: Bachelor of Science in Computer Science and Engineering

Semester Final Examination: Spring 2021

Year: 2nd Semester: 1st

Course Number: CSE2105

Course Name: Digital Logic Design

Time: 3 (Three) hours

Full Marks: 70

Instruction: There are seven questions carrying a total of 14 marks each. Question number - 1 is mandatory to answer. Then Answer any four from questions- 2 to 7.
 Marks allotted are indicated in the right margin

Question 1. [Marks: 14]

- a) Design a block diagram of the BCD Subtractor for the two BCD input A and B. Explain the operations for the input 9-3 (A=9 and B=3) and 3-9 (A=3 and B=9) with your designed circuit. [7]
- b) Show that, $F(A, B, C, D) = \sum(0, 3, 5, 6, 9, 10, 12, 15) = (A \oplus B \oplus C \oplus D)'$ [4]
- c) What do you mean by Duality Principle? Explain how the dual of the Exclusive-NOR is equal to its complement. [3]

Imp. exp. in

0 0	-0
0 1	-1
1 0	1
1 1	0

Question 2. [Marks: 14]

- a) Using 2 Full Adders and basic gates (if needed) implement the ALU functions for two 2-bit numbers (A_1, A_0 & B_1, B_0) for the following conditions: [10]

[10]

S ₃	S ₂	S ₁	ALU function
0	0	0	$A+B+I$
0	1	0	$-A$
0	1	1	$A \cup B$
1	0	0	$-B$
1	0	1	$A-B-I$
1	1	0	$A-I$
1	1	1	$A \cap B$

[4]

- b) Design a 4X16 decoder using 2X4 decoders only.

[4]

Q, 1, 4, 3, 9,
5, 6

Question 3. [Marks: 14]

- a) Simplify the following Boolean function (POS) by using the tabulation method. $F(W, X, Y, Z) = \sum \pi(0, 1, 3, 5, 7, 8, 10, 11, 14, 15)$. [7]
- b) Design a Combinational Logic Circuit to Convert the code Excess-4 to 2, 4, 2, 1 Code. [7]

Question 4 [Marks: 14]

- a) i. What are the advantages of the CLA (Carry Look Ahead) over normal binary 4-bit adders? Describe briefly with diagram. [4]
- ii. Assume that the exclusive-OR gate has a propagation delay of 10 ns and the AND or OR gate have a propagation delay of 5 ns. What is the total propagation delay time in the 4-bit CLA adder? [4]
- b) Design a 4G X 32 internal memory chip organization. [6]

Question 5 [Marks: 14]

- a) Design a 3-Bit Synchronous Prime Number Counter using JK Flip-Flop that counts Up when $X = 0$ and counts Down when $X = 1$. [10]
- b) Discover how the following circuit (Figure. 5.b) works (up/down counter) when we consider Q_2, Q_1, Q_0 as output. Here, initial values are 100. (You have to follow the clock input to get the correct answer.) [4]

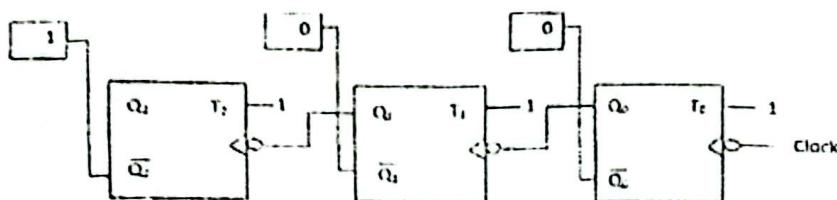


Figure. 5.b

Question 6 [Marks: 14]

- a) Design a 3-bit Synchronous Twisted Counter using D Flip. [8]
- b) Draw the block diagrams of SIPO and SISO Shift Right Registers for 4 bits and briefly describe their operations with an input 1011. [6]

Question 7 [Marks: 14]

- a) Design a 3-bit Universal Shift Register with the following options: [10]

Mode Control			Register Operation
S ₂	S ₁	S ₀	
0	0	0	No Change
0	0	1	Shift Left
0	1	0	Shift Right
0	1	1	Parallel Load
1	0	0	Set all bits to 1
1	0	1	Set all bits to 0
1	1	0	No Change
1	1	1	Invert all bits

w'' = A₃xC
x'' = A₃
y'' = A₂
z = D

$$1+1 = 0 \\ a \cdot a = 0$$

Complete the timing diagram (Figure-7.b.2) for the following circuit (Figure-7.b.1), [4]
assuming all Q outputs begin in the low state:

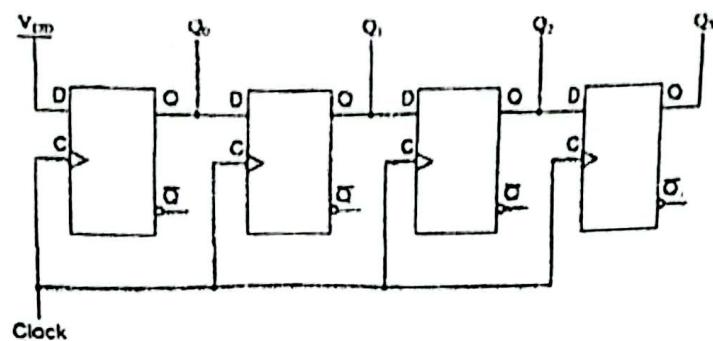


Figure: 7.b.1

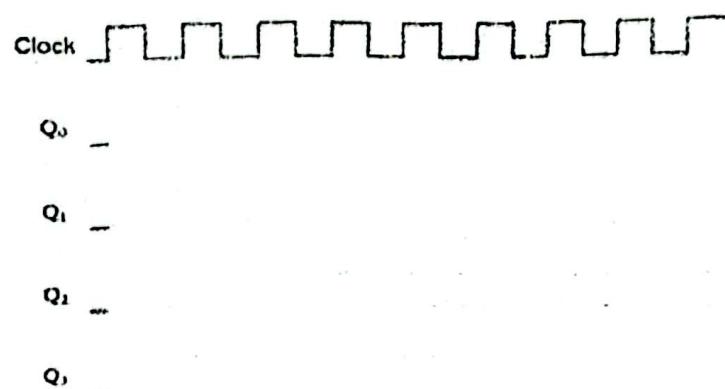


Figure: 7.b.2