

Date of Examination: 24/09/23

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department: Computer Science and Engineering

Program: Bachelor of Science in Computer Science and Engineering

Semester Final Examination: Fall 2022

Year: 2nd Semester: 1st

Course Number: CSE 2105

Course Name: Digital Logic Design

Time: 3 (Three) hours

Full Marks: 70

Instruction: There are 3 (Three) questions, from which you have to answer
any 2 (Two) questions in total from Question no. 1,
any 4 (Four) questions in total from Question no. 2
and
any 4 (Four) questions in total from Question no. 3

Marks allotted are indicated in the right margin.

Question 1. Answer any 2 questions.

[Marks: 14]

✓ A function F has four inputs x, y, z, w and one output such that the output is 1 if and only if the number of 1s in the inputs is exactly two. [2+1.5+1.5+2]

- (i) Derive the truth table for F .
- (ii) Write the canonical SOP expression for F .
- (iii) Write the canonical POS expression for F .
- (iv) Simplify the function F . Show your work and list which Axiom or Theorem you used in each step.

b) Simplify the following Boolean functions: [5+2]

- (i) Simplify F using K-Map, together with the don't-care conditions d , and then express the simplified function in sum of minterms:

$$F(A, B, C, D) = \sum(0, 6, 8, 13, 14), \quad d(A, B, C, D) = \sum(2, 4, 10)$$

- (ii) Reduce the following expression to a minimum number of literals using the postulates and theorems of Boolean Algebra:

$$F(A, B) = (A+B)'(A'+B)'$$

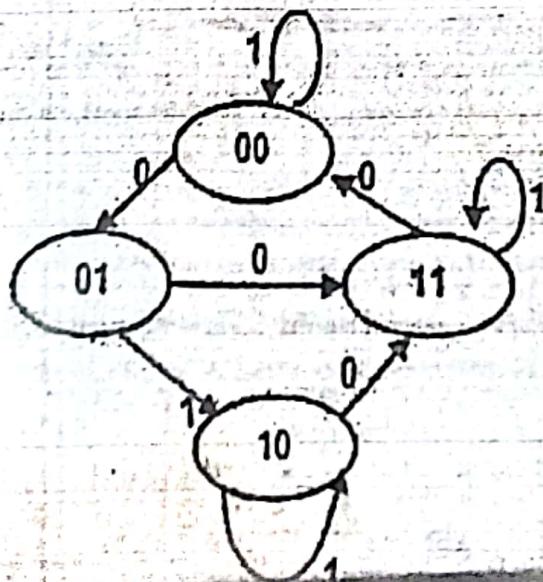
✓ Minimize the following Boolean function F by using the Quine-McCluskey method: [7]

$$F(w, x, y, z) = \sum(1, 4, 6, 7, 8, 9, 10, 11, 15)$$

Question 2. Answer any 4 questions.

[Marks:]

- a) Devise a two-bits counter with inputs "up" and "down" (in addition to the common clock) using two JK flip-flops. A third SR flip-flop stores whether or not the counter should currently be counting "up" or "down"; the "up" input makes the clock start counting "up" and the "down" input makes the clock start counting "down". [7]
- b) Implement a 3-input XOR gate using only a 4×1 multiplexer and an inverter. Also complete the truth table with the correct labels and function solution. [3+2+2]
- c) Construct a 4-bit register with four D flip-flops and 4×1 multiplexers with mode selection input S_1 and S_0 . The register operates according to the following function table: [7]
- | S_1 | S_0 | Register Operation |
|-------|-------|----------------------------|
| 0 | 0 | No Change |
| 1 | 0 | Complement the four Output |
| 2 | 1 | Clear register to 0 |
| 3 | 1 | Load parallel data |
- d) Implement a sequential circuit specified by the following state diagram using D flip-flops: [7]



In a car security system, we usually want to connect the siren in such a way that the siren will be activated when it is triggered by one or more sensors. In addition, there will be a master switch to turn the system on or off. Let us assume that there is a car door switch D, a vibration detector switch V and a master switch M.

[7]

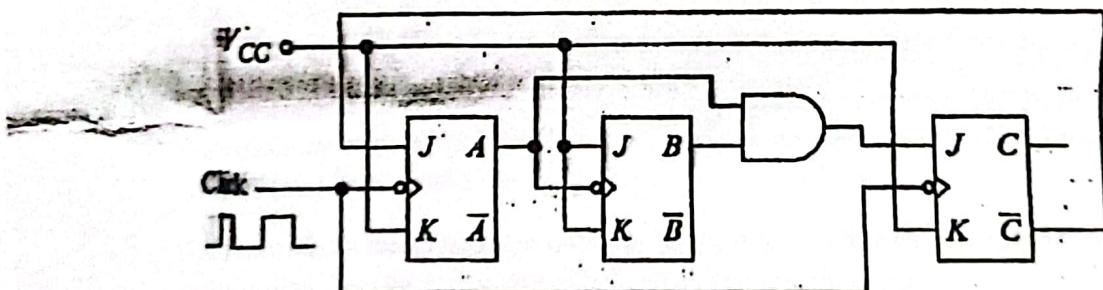
- Assume that when the door is open, $D=1$, otherwise $D=0$.
- Similarly, when the car is being shaken, $V=1$, otherwise, $V=0$.
- We want the siren S to turn on (i.e., set $S=1$) when either the door is open or the car is shaken.
- The siren should turn on only when the system is turned on. However, when we turn off the system, we do not want the siren to turn on regardless of the state of the door switch or the vibration switch.

Given the above description of a car security system, you are required to build a digital circuit that meets the specifications listed above using the minimum number and sizes of Decoder and additional logic gates if needed. Show clearly the size of all used components.

Question 3. Answer any 4 questions.

[Marks: 28]

- a) For the circuit below, draw a timing diagram for ten clock pulses, showing the C, B and A outputs and counting sequences in relation to the clock. Assume that the initial values of C, B and A are 0,0,0 respectively. [5+2]



- b) Explain the working principle of a negative edge triggered asynchronous MOD-10 counter with necessary circuit diagram and timing diagram. [4+1+2]

- c) Describe the basic flip flop circuit using NOR gates only. [7]

- d) Explain the design procedure of a 4-bit BCD adder using 4-bit binary adders. [7]

- e) Determine a single error correcting code for "10110110001". [7]

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department: Computer Science and Engineering

Program: Bachelor of Science in Computer Science and Engineering

Semester Final Examination: Fall 2021

Year: 2nd Semester: 1st

Course Number: CSE2105

Course Name: Digital Logic Design

Time: 3 (Three) hours

Full Marks: 70

Instruction: There are seven questions carrying a total of 14 marks each. Answer any five questions. Marks allotted are indicated in the right margin.

Question 1. [Marks: 14]

- a) Demonstrate by means of truth tables the validity of De Morgan's theorem for three variables. [3]
- b) Simplify the following Boolean function, using Karnaugh Map: [4]
 $F(A,B,C,D) = A'B'D' + A'CD + A'BC$
 $d = A'BC'D + ACD + AB'D'$
- c) Design a three-bit combinational circuit 2's complementer. (The output generates the 2's complement of the input binary number). Show that the circuit can be constructed with exclusive-OR gates. [7]

Question 2. [Marks: 14]

- a) Implement a full-subtractor with two half-subtractor and an OR gate. [3]
- b) Design a BCD-to-excess-3 code converter using a 4-bit full adder. What must be done to change the circuit to an excess-3-to-BCD code converter? [4]
- c) Simplify following Boolean function F using the Quine-McCluskey method: [7]
 $F(A,B,C,D) = \sum(0,1,5,7,10,13,15)$

Question 3. [Marks: 14]

- a) Implement a full adder using two 4×1 multiplexers. [3]
- b) Design a circuit that can check if two 3-bit numbers are equal or not i.e., it produces a 1 only if a 3-bit number $A_2A_1A_0$ is equal to another 3-bit number $B_2B_1B_0$. [4]
- c) Obtain the output expression for a 8 to 3-line priority encoder, where the priorities are as follows: [7]
 $I_4 > I_3 > I_0 > I_1 > I_2 > I_5 > I_6 > I_7$

Question 4. [Marks: 14]

- a) Design a 4-bit ALU that operates based on the function table given below using logic gates, binary adders and multiplexers. [10]

S2	S1	S0	ALU Function
0	0	1	A OR B
0	1	1	A - B
1	0	0	A AND B
1	1	1	A XOR B

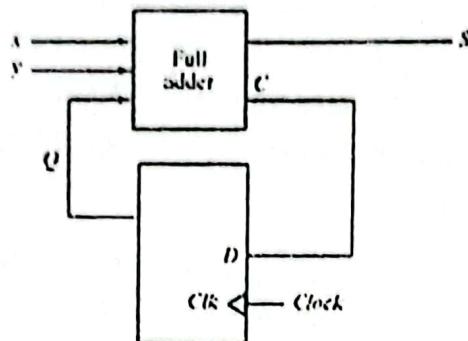
- b) Design a multiplier circuit which can implement 3-bit by 2-bit multiplication. [4]

Question 5. [Marks: 14]

Date: 25/

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- a) Transform the SR-FF to T-FF and also derive the excitation table.
- b) A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in the figure below. Derive the state table and state diagram of the sequential circuit.



- c) Design a binary counter that counts through the 3-bit even numbers upwards using D flip-flops. [7]

Question 6: [Marks: 14]

- a) What is the difference between serial and parallel transfer? Explain how to convert serial data to parallel. What type of register is needed? [3]
- b) Draw the timing diagram of a 4-bit Johnson counter for five clock pulses. [4]
- c) Draw the logic diagram of a four-bit register with four D flip-flops and four 4×1 multiplexers with mode selection inputs S_1 and S_0 . The register operates according to the following function table: [7]

S_1	S_0	Register Operation
0	0	No change
1	0	Complement the four outputs
0	1	Clear register to 0
1	1	Load Parallel

Question 7. [Marks: 14]

- a) What is the difference between asynchronous circuit and synchronous circuit? [2]
- b) What is race-around condition? Explain how this can be avoided in J-K flip flop. [4]
- c) Explain how, the invalid condition of S-R latch can be eliminated using J-K latch. Use block diagram and truth table for explanation. [8]

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department: Computer Science and Engineering

Program: Bachelor of Science in Computer Science and Engineering

Semester Final Examination: Spring 2021

Year: 2nd Semester: 1st

Course Number: CSE2105

Course Name: Digital Logic Design

Time: 3 (Three) hours

Full Marks: 70

Instruction: There are seven questions carrying a total of 14 marks each. Question number - 1 is mandatory to answer. Then Answer any four from questions- 2 to 7.

Marks allotted are indicated in the right margin

Question 1. [Marks: 14]

- a) Design a block diagram of the BCD Subtractor for the two BCD input A and B. Explain the operations for the input 9-3 (A=9 and B=3) and 3-9 (A=3 and B=9) with your designed circuit. [7]
- b) Show that, $F(A, B, C, D) = \Sigma(0, 3, 5, 6, 9, 10, 12, 15) = (A \oplus B \oplus C \oplus D)'$ [4]
- c) What do you mean by Duality Principle? Explain how the dual of the Exclusive-NOR is equal to its complement. [3]

Imp example in

0 0	— 0
0 1	— 1
1 0	— 1
1 1	— 0

Question 2. [Marks: 14]

- a) Using 2 Full Adders and basic gates (if needed) implement the ALU functions for two 2-bit numbers (A_1, A_0 & B_1, B_0) for the following conditions: [10]

S ₃	S ₂	S ₁	ALU function
0	0	0	$A+B+I$
0	1	0	$-A$
0	1	1	$A \oplus B$
1	0	0	$-B$
1	0	1	$A-B-I$
1	1	0	$A \cdot I$
1	1	1	$A \cap B$

- b) Design a 4X16 decoder using 2X4 decoders only. [4]

Question 3. [Marks: 14]

- a) Simplify the following Boolean function (POS) by using the tabulation method
 $F(W, X, Y, Z) = \sum \pi(0, 1, 3, 5, 7, 8, 10, 11, 14, 15)$. [7]
- b) Design a Combinational Logic Circuit to Convert the code Excess-4 to 2, 4, 2, 1 Code. [7]

Question 4 [Marks: 14]

- a) i. What are the advantages of the CLA (Carry Look Ahead) over normal binary 4-bit adders? Describe briefly with diagram. [4]
- ii. Assume that the exclusive-OR gate has a propagation delay of 10 ns and the AND or OR gate have a propagation delay of 5 ns. What is the total propagation delay time in the 4-bit CLA adder? [4]
- b) Design a 4G X 32 internal memory chip organization. [6]

Question 5 [Marks: 14]

- a) Design a 3-Bit Synchronous Prime Number Counter using JK Flip-Flop that counts Up when $X = 0$ and counts Down when $X = 1$. [10]
- b) Discover how the following circuit (Figure. 5.b) works (up/down counter) when we consider Q_2, Q_1, Q_0 as output. Here, initial values are 100. (You have to follow the clock input to get the correct answer.) [4]

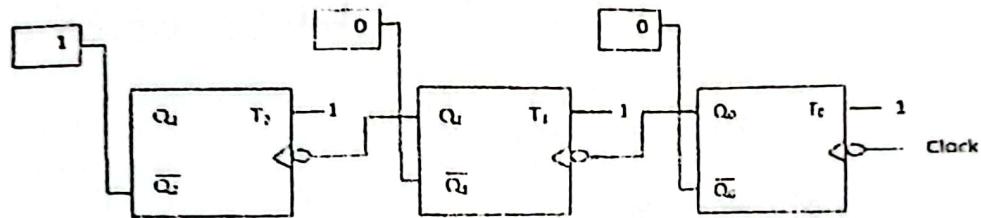


Figure. 5.b

Question 6 [Marks: 14]

- a) Design a 3-bit Synchronous Twisted Counter using D Flip. [8]
- b) Draw the block diagrams of SIPO and SISO Shift Right Registers for 4 bits and briefly describe their operations with an input 1011. [6]

Question 7 [Marks: 14]

- a) Design a 3-bit Universal Shift Register with the following options: [10]

Mode Control			Register Operation
S ₂	S ₁	S ₀	
0	0	0	No Change
0	0	1	Shift Left
0	1	0	Shift Right
0	1	1	Parallel Load
1	0	0	Set all bits to 1
1	0	1	Set all bits to 0
1	1	0	No Change
1	1	1	Invert all bits

$$\begin{array}{l} L \rightarrow L = 0 \\ A \cdot 1 = 1 \end{array}$$

Complete the timing diagram (Figure-7. b.2) for the following circuit (Figure-7. b.1), assuming all Q outputs begin in the low state:

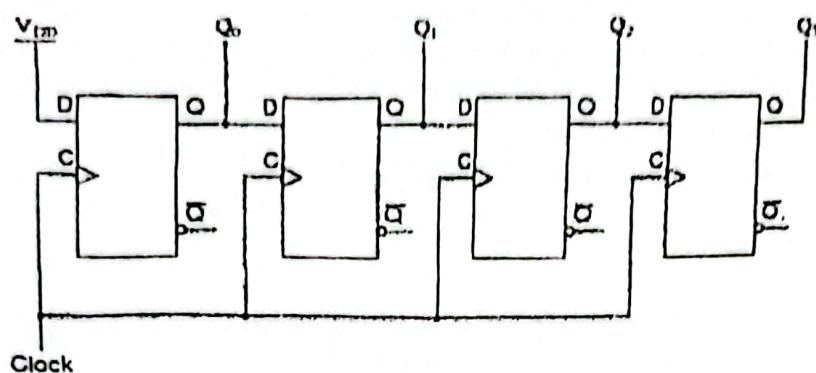


Figure: 7.b.1

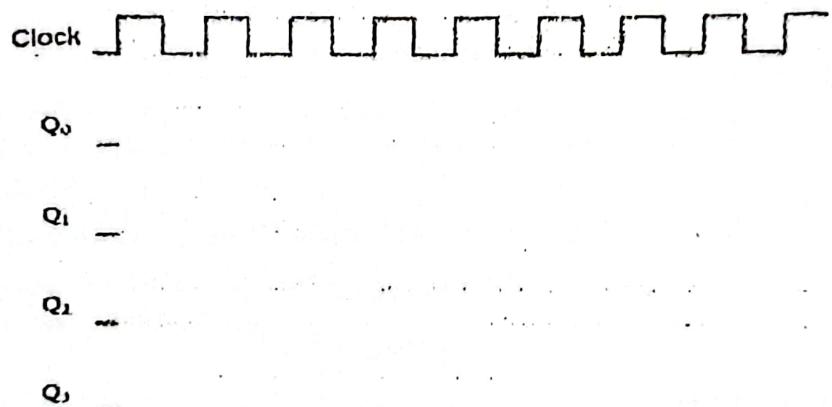


Figure: 7.b.2

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Date of Examination : 15/12/2019

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AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

T.R.
Department: Computer Science and Engineering

Program: Bachelor of Science in Computer Science and Engineering

Semester Final Examination: Spring 2019

Year: 2nd Semester: 1st

Course Number: CSE2105

Course Name: Digital Logic Design

Time: 3 (Three) hours

Full Marks: 70

[There are seven questions carrying a total of 14 marks each. Answer any five questions.
Marks allotted are indicated in the right margin.]

1. a) What do you know about the Race Around Condition in JK flip-flop? How can this problem be solved? Explain with the necessary circuits. [5]
- b) Analyze, whether the following circuit works for binary up or down counter. Write down the sequence table, state diagram and timing diagram for 8 pulses. Assume that, initial state is '010' for $Q_3Q_2Q_1$. [5]

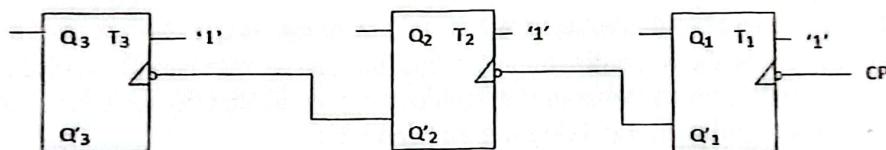


Figure: 1.b

- c) How can you obtain D and T flip-flop from JK flip-flop? Show the necessary connections, characteristic tables and equations. [4]
2. a) Prove that, the following circuit works for the ring counter. Assume, the initial input for $Q_3=1$, $Q_2=0$ and $Q_1=0$. Justify your answer with sequence table and definition of ring counter. [4]

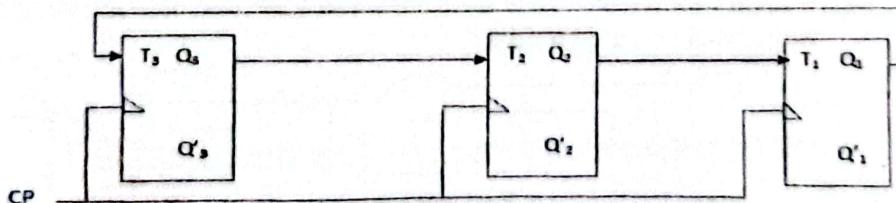


Figure: 2.a

- b) Draw the block diagrams of SIPO and SISO shift left registers for 3 bits and briefly describe their operation with an input 110. [5]
- c) Design a switch controlled 3-bit odd up and down ripple counter using JK flip flops. [5]
3. a) Obtain the expressions for 3-bit Comparator circuit. [6]
- b) There are three components in a course: home work (H), lab (L) and exam (E). You pass the course (P) only if you pass two or more components. Now design a circuit to detect pass (p) in the course. [4]
- c) Design a 4X16 decoder using 2X4 decoders only. [4]

4. a) Using 2 Full Adders and basic gates (if needed), implement the ALU functions for two 2-bit numbers for the following conditions: [10]

S_3	S_2	S_1	ALU function
0	0	0	$-A$
0	0	1	$A \cap B$
0	1	0	$A+B+I$
0	1	1	$B-A-I$
1	0	1	$-B$
1	1	0	$A \text{ XOR } B$
1	1	1	$A \cup B$

- b) Design a 3 X 3 Array Multiplier using Adders and AND gates. [4]

5. a) Explain the circuit diagram of BCD Adder and briefly describe its operation. [6]
 b) What is Carry Look Ahead Adder (CLA)? What is the benefit of using this special circuit instead of a normal adder circuit? [4]
 c) Design a circuit using a decoder and basic gates that can detect an error in the representation of 4 bit binary data in BCD. [4]
6. a) Give a block diagram for 8M X 32 memory using 512K X 8 memory chips. [5]
 b) Draw the logic diagram of a four-bit register with four D flip-flops and four 4 X 1 multiplexers with mode selection inputs S_1 and S_0 so that the register operates according to the following function table. [5]

S_1	S_0	Register Operation
0	0	No Change
0	1	Complement
1	0	Clear Register to 0
1	1	Load Parallel Data

- c) Write a truth table for the latch shown in figure-6.c. Is it similar to any other latch with which you are familiar? [4]

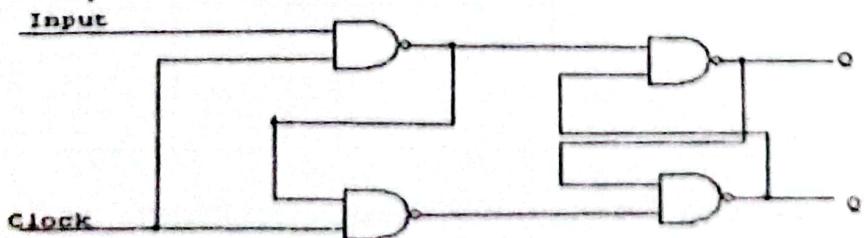


Figure: 6.c

7. a) Design a BCD to Excess-3 Code Converter using an 8 to 1 line Multiplexer and Inverters. [6]
 b) What is Priority Encoder? Design a 4 to 2 line Priority Encoder, where the Priority is $I_1 < I_0 < I_3 < I_2$. [5]
 c) Implement a full-subtractor with two half-subtractors and an OR gate. [3]

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department: Computer Science and Engineering

Program: Bachelor of Science in Computer Science and Engineering

Semester Final Examination: Spring 2018

Year: 2nd Semester: 1st

Course Number: CSE2105

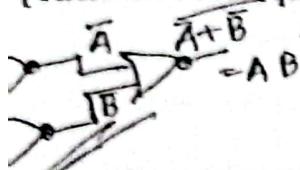
Course Name: Digital Logic Design

Time: 3 (Three) hours

Full Marks: 70

[There are seven questions carrying a total of 14 marks each. Answer any five questions.

Marks allotted are indicated in the right margin.]



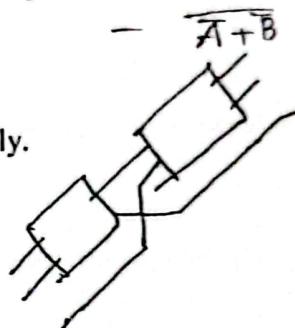
$$\bar{A} + \bar{B} = \bar{A} \cdot \bar{B}$$

1. a) Implement AND, OR and NOT operations using NOR gates only. [3]

- b) Simplify the following expression using Boolean Algebra: [4]

$$A(A + \bar{B}C) + A(\bar{B} + C)$$

- Determine the single error correcting code for "110110110". [7]



2. a) Implement a full adder circuit using a 3-to-8 line Decoder. [3]

- b) Design a four-input combinational circuit with one output to determine whether a given 4-bit number is in Fibonacci sequence or not. In your design, the output should be "1", if the corresponding input is a Fibonacci number and "0" otherwise. [4]

- c) Draw the circuit diagram of MOD-10 asynchronous counter using JK flip-flop and briefly describe its operation. [7]

3. a) Describe duality principle with an example. [3]

- b) Design a 4-input priority encoder. [4]

- c) Simplify the following Boolean function F by using the tabulation method: [7]

$$F(A, B, C, D) = \sum (0, 3, 4, 5, 7, 9, 11, 13)$$

4. a) Design a 16x1 multiplexer with two 8x1 and one 2x1 multiplexers. [3]

- b) Construct a 4-to-16-line decoder with five 2-to-4 line decoders. Use block diagram. [4]

- c) What is a magnitude comparator? Design a four bit magnitude comparator. [7]

5. a) Define different types of shift registers. [3]

- b) Draw the circuit diagram of a 4-bit unidirectional shift register and briefly describe its operation. [4]

- c) Describe a basic flip-flop circuit with NAND gates. [7]

6. a) What are the differences between a combinational and a sequential circuit? [3]

b) Describe master-slave SR flip-flop. [4]

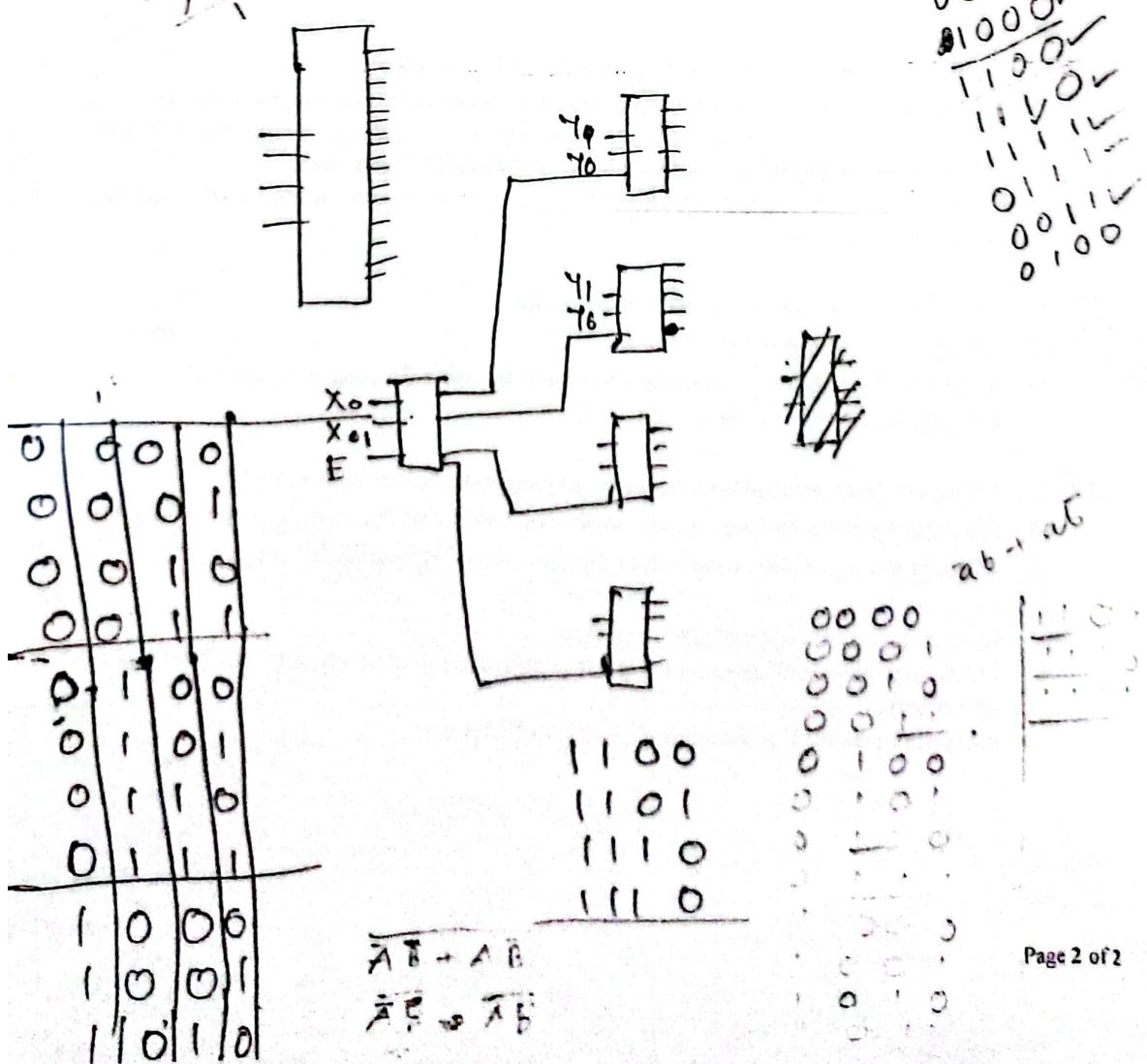
c) Design a 3 bit down counter with clocked T flip-flops. [7]

7. a) Draw the timing diagram of a 4-bit Johnson counter for six clock pulses (negative edge triggered). [3]

b) It is required to design a circuit to compute the equation $Y=X \bmod 5$, where X is a 4-bit unsigned number. Your circuit should be designed using the minimum number and sizes of the following MSI components (Decoder, Encoder) and additional logic gates if needed. Show clearly the size of all used components. [4]

c) Draw the logic diagram of a 4-bit register with four D flip-flops and 4×1 multiplexers with mode selection input S_1 and S_0 . The register operates according to the following function table: [7]

S1	S0	Register Operation
0	0	No Change
0	1	Complement the four Output
1	0	Clear register to 0
1	1	Load parallel data



Date: 20.03.201

Ahsanullah University of Science and Technology

Department of Computer Science and Engineering

2nd Year 1st Semester, Final Examination (Fall 2017)

Course No: CSE 2105

Course Title: Digital Logic Design

Time: 3 Hours

Full Marks: 70

There are 7 (seven) questions carrying 14 marks each. Answer any 5 (five) questions]
[Marks allotted are indicated in the right margin]

- a) Implement AND, OR and NOT operations using NAND gates only. [3]
- b) Convert the following function into Sum of Products (SOP) form: [4]

$$F = (X + \bar{Y} + Z)(\bar{X} + Y)$$
- c) Determine the single error correcting code for "100100110". [7]

- 1. a) Implement the following function using 8X1 MUX only: [3]

$$F(A, B, C) = \sum(2, 3, 6, 7)$$
- b) Design a combinational circuit that receives a 4-bit input number, $X(x_3, x_2, x_1, x_0)$ and computes the number of leading zero's in the input. [4]

For example, if the input $x_3, x_2, x_1, x_0 = 0111$ or $x_3, x_2, x_1, x_0 = 0100$, the output should produce a result indicating that there is a single leading zero.
- c) Draw the circuit diagram of MOD-6 asynchronous counter using JK flip-flop and briefly describe its operation. [7]

- 2. a) What is don't care condition? What is the significance of the don't care condition in a Karnaugh map? [3]
- b) Simplify the following Boolean function F using Karnaugh map, together with the don't-care conditions d: [4]

$$F(W, X, Y, Z) = \sum(1, 3, 5, 7, 9, 15), d(W, X, Y, Z) = \sum(4, 6, 12, 13)$$
- c) Simplify the following Boolean function F by using the tabulation method: [7]

$$F(A, B, C, D) = \sum(0, 3, 4, 5, 7, 9, 11, 13)$$

- 3. a) What is magnitude comparator? Design one bit magnitude comparator. [3]
- b) Design a 4-bit adder/subtractor circuit which uses the least number of Full-Adders (FAs). [4]

The circuit receives two 4-bit signed numbers A and B (2's complement representation) and one control input (M). If the control input M=0, the 4-bit circuit output equals (A+B). If the control input M=1, it equals (A-B). The circuit has another output V which equals 1 only in case of overflow.
- c) Design a combinational logic circuit which receives a 4-bit unsigned number X as input and produces an output Z which equals the result of integer division of X by 3 (e.g., if X=7, then Z=2). Your circuit should be designed using 4X16 Decoders and additional logic gates if needed. [7]

5. a) Define different types of shift registers.
 b) Draw the timing diagram of 4 bit Ring counter for five clock pulses (negative edge 've') triggered.
 c) Describe master-slave SR flip-flop. [7]
6. a) What are the differences between a combinational and a sequential circuit? [3]
 b) Describe basic flip-flop circuit with NOR gates. [4]
 c) Design a counter with a repeated output sequence 0, 1, 2, 4, 5, 6, 3, with clocked D flip-flops. [7]
7. a) Draw a circuit that accepts a 3-bit input number A(A₂,A₁,A₀) and outputs a 2-bit number B(B₁,B₀) that is equal to the number of 1's that appear in the input A. For example, A=101 contains two 1's, so B=10. Also, A=111 contains three 1's, so B=11. You are allowed to use only one 3-8 decoder, two OR gates, and one 4-2 encoder. Label all inputs, pins and outputs. [3]
 b) Implement a 1-16 demultiplexer using only 2-to-4 decoders with enable inputs and no other logic gates. Clearly label all inputs, pins, and outputs of your circuit. [4]
 c) Draw the logic diagram of a 4-bit register with four D flip-flops and 4X1 multiplexers with mode selection input S₁ and S₀. The register operates according to the following function table: [7]

S ₁	S ₀	Register Operation
0	0	No Change
0	1	Complement the four Output
1	0	Clear register to 0
1	1	Load parallel data

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department: Computer Science and Engineering

Program: Bachelor of Science in Computer Science and Engineering

Semester Final Examination: Spring 2022

Year: 2nd Semester: 1st

Course Number: CSE 2105

Course Name: Digital Logic Design

Time: 3 (Three) hours

Full Marks: 70

Instruction: There are 7 (Seven) questions, from which you have to answer any 5 (Five) questions in total, including the Question no. 1 (One) and Question no. 2 (Two), which are mandatory for everyone.

Marks allotted are indicated in the right margin.

Question 1. [Marks: 14]

- a) Describe duality principle with an example. [2]
b) Simplify the following expression using the postulates and theorems of Boolean algebra: [4]

$$\overline{(ABC)}(A + C)(A + \overline{C})$$

$$\wedge \text{ not } \wedge^c$$

- c) Determine the single error correcting code for "101110110". [8]

$$0\ 0\ 1\ 1\ 0\ 1\ 1\ 1\ 1\ 0$$

Question 2. [Marks: 14]

- a) What is don't care condition? Simplify the following Boolean function F using Karnaugh map, together with the don't-care conditions d: [2+4]

$$F(A, B, C, D) = \sum (1, 3, 5, 7, 9, 15), d(A, B, C, D) = \sum (4, 6, 12, 13)$$

$$D(\bar{A} + \bar{B} + \bar{C})$$

- b) Simplify the following Boolean function F by using the Quine-McCluskey method: [8]

$$F(w, x, y, z) = \sum (0, 1, 2, 8, 10, 11, 14, 15)$$

Question 3. [Marks: 14]

- a) Design a 4-bit BCD adder using 4-bit binary adders. [6]

- b) Design a synchronous counter that counts through the 3-bit prime numbers downwards using clocked D flip-flops. [8]

Question 4. [Marks: 14]

- a) Design a four input combinational circuit with one output to determine whether a given 4-bit number is in Fibonacci sequence or not. In your design, the output should "1", if the corresponding input is a Fibonacci number and "0" otherwise. [6]
- b) Draw the circuit diagram of four-bit universal shift register and describe its operation. [8]

Question 5. [Marks: 14]

- a) Implement 8X1 multiplexer using a 3X8 decoder and basic logic gates. Appropriately label the inputs and outputs. [6]
- b) Design a basic flip-flop circuit with NAND gates. [8]

Question 6. [Marks: 14]

- a) What are the differences between a combinational and a sequential circuit? Draw the logic diagram of a 4-bit Johnson counter and show its count sequence for 8 pulses. [2+4]
- b) What is carry look-ahead adder (CLA)? Construct a 4-bit CLA circuit. [1+7]

Question 7. [Marks: 14]

- a) Construct a JK flip-flop using a D flip-flop, a 4-to-1-line multiplexer and an inverter. [6]
- b) Design a 3-bit magnitude comparator. [8]

0	1	0	0
0	.	1	0
1	1	0	1
1	1	x	0