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Chittagong University of Engineering and Technology
Department of Electrical & Electronic Engineering
B.Sc. Engineering, Level 3, Term II, Examination-2020-21

Course No : EEE-367/EEE-359(O)
Course Title : Electronic Communication
Full Marks : 210
Time : 3 Hours

The figures in the right margin indicate full marks. Answer any three questions from each section. Use separate script for each section.

SECTION – A

1(a) Modulation translates lower frequency signal into higher frequency signal. Prove the statement. 10

1(b) What is modulation index of AM signal? Derive an expression of modulation index of AM signal modulated with multi-tone message signal. 10

1(c) The antenna current of an AM transmitter is 10 A when carrier is sent. It increases to 11 A when carrier is modulated by a single sine wave. Find the modulation index. Determine the total power and side band power, and efficiency of the modulator. 15

2(a) Prove that coherent detection is optimum demodulation of full amplitude modulation. 13

2(b) After drawing a block diagram of super heterodyne receiver, explain the working principle of each block. 12

2(c) A modulating signal's voltage $v_m(t) = 25\sin(1000t)$ and a carrier voltage $v_c(t) = 5\sin(4 \times 10^6 t)$ are applied to the input of a non-linear resistance whose input-voltage-output-current characteristics can be represented by $i_0(t) = (10 + 2v_i(t) - 0.2v_i^2(t))$ mA. Calculate the overall modulation index if the output current is passed through a tuned circuit so that only component approximate to AM is produced. 10

3(a) What is primary advantage of FM over AM? List four major applications of FM. 10

3(b) Show that wideband FM produces infinite bandwidth. 10

3(c) A phase modulator produces maximum phase shift of 45^0. The modulating frequency range is 300 to 4000 Hz. What is the maximum frequency deviation possible? 15

4(a) After deriving the SNR equation of FM demodulator, explain the necessity of pre-emphasis and de-emphasis circuit. 13

4(b) How is aliasing prevented? Explain. 10

4(c) Explain pulse modulation. How do you generate PWM signal? Explain with necessary waveform and circuits. 12

SECTION-B

5(a) Explain why multiplexing techniques are necessary in various communication applications. Compare frequency division multiplexing and time division multiplexing. 10

5(b) Describe an FDM telemetry transmitting system. 13

5(c) Describe the operation of a closed loop PAM clock recovery circuit that used to generate the de-multiplexor clock pulses in a TDM system. 12

6(a) Why are synchronizing pulses transmitted along with the picture signal? 05

6(b) What do you understand by compatibility in TV transmission? Enumerate essential requirements that must be met to make a color system fully compatible. 08

6(c) Explain the terms: (i) Additive color mixing, (ii) Hue, (iii) Saturation and (iv) Luminance 12

6(d) Write short notes on HDTV, NTSC, and LCD display. 10

7(a) Develop an equation for mono-static radar and show that the maximum detectable range depends on the energy of the transmitted pulse rather than the transmitted power level. 12

7(b) Explain the operational mechanism of an amplitude comparison mono-pulse radar. 15

7(c) What do you understand by link budget of satellite uplink and downlink system? Explain. 08

8(a) Why sky wave propagation generally better at nigh than during the day. 12

8(b) Draw the general block diagram of a communication satellite and mention the function of all the major sub-systems. 15

8(c) What is VSAT? Write the applications of VSAT. 08

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Chittagong University of Engineering and Technology
Department of Electrical & Electronic Engineering
B.Sc. Engineering, Level 3, Term II, Examination-2020-21

Course No : EEE-365/EEE-495(O)

Course Title : Digital Signal Processing

Full Marks : 210

Time : 3 Hours

The figures in the right margin indicate full marks. Answer any three questions from each section. Use separate script for each section.

SECTION – A

1(a) Show the symmetry property of DFT with typical example. 10

1(b) Determine the circular convolution of following sequences: $x_1(n) = \{1, \underset{\uparrow}{2}, 3, 1\}$ and $x_2(n) = \{\underset{\uparrow}{4}, 3, 2, 2\}$ 15

1(c) Derive the redix-2 decimation in time FFT algorithm. 10

2(a) What are the major factors that influence the choice of a specific realization of discrete time system? Explain briefly. 10

2(b) Sketch the block diagram for direct form realization and the frequency sampling realization of the M=32, α=0, linear phase (symmetric) FIR filter which has frequency samples 15

$$H\left(\frac{2\pi k}{32}\right) = \begin{cases} 1, & k = 0,1,2 \\ \frac{1}{2}, & k = 3,4 \\ 0, & k = 5,6,\dots 15 \end{cases}$$

Compare the computational complexity of these two structures.

2(c) Evaluate the transpose direct form II realization of the system $H(z) = \frac{(1-0.5e^{\left(\frac{j\pi}{4}\right)}z^{-1})(1-0.5e^{-\left(\frac{j\pi}{4}\right)}z^{-1})}{(1-0.8e^{\left(\frac{j\pi}{3}\right)}z^{-1})(1-0.8e^{-\left(\frac{j\pi}{3}\right)}z^{-1})}$ 10

3(a) Convert the analog band pass filter with system function $H_a(s) = \frac{1}{(s+0.1)^2+9}$ into a digital IIR filter by use of the backward difference for the derivative. If we use the mapping $s = \frac{z+z^{-1}}{T}$, how it introduces more poles in the conversion? 15

3(b) Briefly describe the characteristics of practical frequency selective filters. 10

3(c) Write short notes on the following topics: 10

i. MRI, (ii) EEG signal processing

4(a) Design an FIR linear phase digital filter for $H_d(\omega) = \begin{cases} 1, & |\omega| \le \pi/6 \\ 0, & \pi/6 < |\omega| \le \pi \end{cases}$ 15

Determine the coefficients of 25 taps filter based on rectangular window. Also plot magnitude and phase response.

4(b) Define ideal filter. From the ideal filter's frequency response, show that it is not realizable. 10

4(c) How do you design all types of digital filters from low pass filter Kernel? Explain with necessary conditions. 10

SECTION-B

5(a) Explain the concept of energy and power signal. Also determine the power and energy of unit step signal. 08

5(b) How many ways a discrete time signals $x[n]$ can be represented? A discrete time signal is shown in Fig. 5(b). Sketch and level carefully following derived from $x[n]$: 12

i) $x[2n]$, ii. Odd part of $x[n]$, and iii. $x[-n+2]u[n-1]$

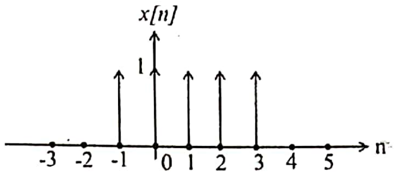

Fig. 5(b)

5(c) Determine the spectra of the signals i. $x[n] = cos\sqrt{2}n\pi$, ii. $x[n] = \cos(n\pi/3)$, and iii. $x[n]$ is periodic with period N=4 and $x[n] = \{\underset{\uparrow}{1}, 1, 0, 0\}$ 15

6(a) Determine the impulse response $h[n]$ for the system described by the second-order difference equation $y[n] = 3y[n-1] + 4y[n-2] + x[n] + 2x[n-1]$ 12

6(b) Sketch the output $y[n]$ of LTI system with impulse response 13

$$h[n] = \begin{cases} 1, & -2 \le n < 2 \\ 0, & elsewhere \end{cases} \text{ when the input is } x[n] = \begin{cases} n/3, & 0 \le n \le 6 \\ 0, & elsewhere \end{cases}$$

6(c) Determine the auto-correlation sequences of the following signal $x[n] = \{\underset{\uparrow}{1}, 2, 1, 1\}$ 10

7(a) Define z transform and ROC. Find the z transformation of the signal in Fig. 7(a) and draw its ROC.

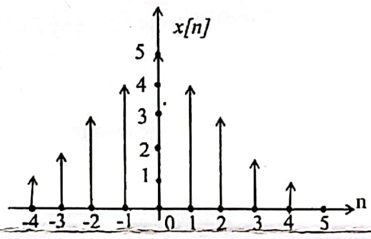

Fig. 7(a)

7(b) Determine the energy density spectrum $S_{XX}(\omega)$ of the signal $x[n] = a^n u[n]$, $-1 < \alpha < 1$ 10

7(c) A discrete time system is realized by the structure shown in Fig. 7(c). Determine the impulse response of the system. 12

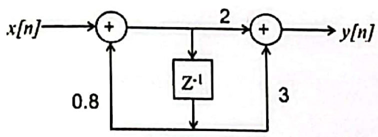

Fig. 7(c)

8(a) An LTI system is described by the following difference equation. 12

$y[n] = ay[n-1] + bx[n]$, $0 < a < 1$

Determine the magnitude and phase of frequency response $H(\omega)$of the system.

8(b) Given that $H[z] = \frac{2-4z^{-1}+6z^{-2}-7z^{-3}}{2+3z^{-1}-5z^{-2}+8z^{-3}}$. Find direct form I and II (both block diagram and signal flow graph representation). 13

8(c) What is aliasing? Consider the analog signal $x_a(t) = 3\cos(100\pi t)$ 10

i. Determine the minimum sampling rate required to avoiding aliasing.

ii. Suppose the signal is sampled as the rate $F_s = 200\text{Hz}$. What is the discrete time signal obtained after sampling?

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Chittagong University of Engineering and Technology
Department of Electrical & Electronic Engineering
B.Sc. Engineering, Level 3 Term II, Examination-2020-21

Course No : EEE-361/EEE-483(O)

Course Title : Power Electronics

Full Marks : 210

Time : 3 Hours

The figures in the right margin indicate full marks. Answer any three questions from each section. Use separate script for each section.

SECTION – A

1(a) Draw the equivalent circuit and *i-v* characteristics curve of SCR. Explain the following terms: 12

i. Forward leakage current

ii. Latching current

iii. Holding current

iv. Reverse leakage current

1(b) Why does *dv/dt* and *di/dt* protection necessary for the semiconductor devices? Explain with proper circuit diagram, the *dv/dt* and *di/dt* protection of SCR. 13

1(c) Draw the two transistor model of SCR. Explain the complementary commutation process to turn off an SCR with necessary circuits and waveforms. 10

2(a) Draw the output voltage, output (L-L) current, phase current and necessary waveforms for a 3-φ full controlled rectifier, using R-L load where $\alpha=60^0$. 17

2(b) For the circuit shown in Fig. 2(b), 18

(i) Find average value of load current for $\alpha=60^0$. 2.67A

(ii) What is the new value of average current, if a large inductor is connected in series with the load? 0.313 A

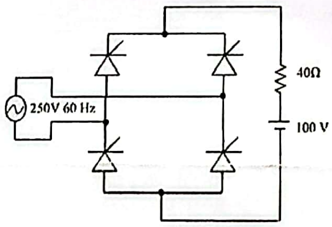

Fig. 2(b)

3(a) Describe with necessary diagrams, how four quadrant operation of DC motor can be obtained using a dual converter. 12

3(b) Distinguish between current source inverter and voltage source inverter. 12

3(c) Discuss the operation of a full bridge resonant inverter (with firing and output current waveforms). 11

4(a) Why is voltage control necessary for the inverter? What are the advantages of unipolar switching over bipolar switching? 10

4(b) Explain the operation of a 3-φ voltage source square wave inverter for 180^0 conduction. 15

4(c) A single phase full bridge inverter has a resistive load of 2.4Ω and $V_s = 48V$. Determine: 10

i. Peak reverse blocking voltage

ii. Output power

iii. RMS output voltage at the fundamental frequency

SECTION-B

5(a) Explain with necessary diagrams about phase control and integral cycle control of AC voltage controllers. 10

5(b) Classify AC voltage controller. Write down their applications. 12

5(c) Draw schematic diagram of TRIAC based voltage regulator and explain its operation. 13

6(a) Draw the circuit diagram of the boost converter and explain its operation with necessary wave shapes. Derive output-input voltage relationship. 11

6(b) Explain continuous and discontinuous conduction modes of operation of DC-DC converter. How the values of inductor and capacitor are chosen? 12

6(c) For a DC-DC boost converter circuit, following paramagnets are given. 12

Input voltage = 150V,

Output voltage = 220V,

Switching frequency = 25kHz.

Determine:

(i) Total switching period,

(ii) Duty cycle and

(iii) Switch turn on period.

7(a) Explain the operation of a single phase full wave ac voltage controller having RL load. Draw the necessary wave shape and find the expressions of output voltage, currents and input power factor. 10

7(b) With necessary diagram explain the operation of a forward converter. Shows its better controllability to regulate the output voltage. 12

7(c) What is cyclo-converter? Draw the schematic diagrams of a three phase half-wave (three pulses) cyclo-converter feeding single phase and three phase load, respectively. 13

8(a) What is dielectric heating? Proof that power in per unit volume of a dielectric is proportional to the operating frequency and square of voltage gradient. 15

8(b) What is induction heating? Write down its applications. 10

8(c) What is MPPT? How does it operate the PV array at its optimum/maximum power point? 10

THE END

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Chittagong University of Engineering and Technology
Department of Electrical & Electronic Engineering
B.Sc. Engineering, Level 3 Term II, Examination-2020-21

Course No : EEE-369/EEE-473(O)

Course Title : Semiconductor Physics and Devices

Full Marks : 210

Time : 3 Hours

The figures in the right margin indicate full marks. Answer any three questions from each section. Use separate script for each section.

SECTION – A

1(a). Why and how semiconductor material is different from conductor? Explain with necessary figures. 08

1(b). Discuss the basic technique for silicon crystal growth from the melt. 12

1(c). Mention the properties of solid materials that determine their applicability. Discuss the different types of defects in crystal. 15

2(a). Calculate the atomic packing factor for the following lattice structures: 10

i. SC lattice

ii. BCC

iii. FCC

2(b). Derive the equation which represents the statement of wave particle duality. 10

2(c). Consider an electron traveling with a velocity of 10^7 cm/sec. Assume the velocity increases by a value of 1 cm/sec. Find out the charge in energy of the electron. (Assume a system with 10^{19} one electron atoms and at equilibrium interatomic distance the allowed energy bond is 1ev. 08

2(d). Write short notes on the followings: 07

i. Compound semiconductor

ii. Thermal stability

3(a). Explain Hall effect phenomena and derive an expression for Hall effect. 12

3(b). Prove that $J = e\mu_n nE + e\mu_p pE + eD_n\frac{dn}{dx} - eD_p\frac{dp}{dx}$; where the symbols have their usual meaning. 10

3(c). Calculate the thermal equilibrium electron and hole concentrations in a compensated n-type semiconductor. Consider a silicon semiconductor at T=300^{0}K in which $N_d=10^{16}cm^{-3}$ and $N_a=0$. Assume $n_i=1.5\times10^{10}cm^{-3}$. 08

3(d). Write short note no carrier generation and recombination. 05

4(a). How does mobility due to ion scattering and lattice scattering vary with change in temperature and doping concentration? Explain. 12

4(b). What does Fermi Level mean in semiconductor? How does it vary with doping concentration and temperature? 11

4(c). Calculate the thermal equilibrium electron and hole concentration in a compensated p-type semiconductor. Consider a Si semiconductor at T=300^{0}K in which $N_a=10^{16}cm^{-3}$ and $N_d=3\times10^{15}cm^{-3}$. Assume $n_i=1.5\times10^{10}cm^{-3}$ 12

SECTION-B

5(a). What happens during a PN junction formation? Explain using band diagram. 10

5(b). Derive an expression for built in potential of a PN junction as a function of doping concentration. Calculate x_n, x_p, V_{bi}, $|E_{max}|$ for a PN junction of Si at T=300⁰K. Given $N_D=10^{16}cm^{-3}$ and $N_a=2\times10^{17}cm^{-3}$. Assume $n_i=1.5\times10^{10}cm^{-3}$, $\epsilon_{r(Si)} = 11.7$ 18

5(c). Draw the E-filed and voltage profile for a metal-n-type Si junction. 07

6(a). Find an expression for the minority carrier distribution in the base region of a NPN transistor. Draw the minority carrier distribution of an NPN BJT in emitter, base and collector under forward-active and reverse-active mode of operation. 20

6(b). Why are two back-to-back PN-diodes not sufficient as a replacement for an NPN transistor? Draw a circuit model that is able to replicate the behavior of an NPN BJT in all four operating modes. Write the equations for your proposed model. 15

7(a). If you form a metal and P-Si junction, where $\varphi_m > \varphi_s$, what characteristics will the junction exhibit? Explain with the aid of band diagram. 15

7(b). Determine the theoretical barrier height, built-in potential and maximum electric field for a metal semiconductor junction under zero bias. Consider N-type Si with T=300⁰K, $\chi = 4.01V$, $\varphi_m(Tungsten) = 4.55V$, $N_d=10^{16}cm^{-3}$ and $N_c=2.8\times10^{19}cm^{-3}$, $\epsilon_{r(Si)} = 11.7$. 15

7(c). Mention one advantage of Schottky diode over PN junction diode. 05

8(a). Why direct band-gap semiconductors are preferred over indirect band-gap semiconductors for optical devices? How III-V semiconductors revolutionized the field of optical devices? 12

8(b). Distinguish between the operation of LASER and LED. 10

8(c). How band-gap dictates the efficiency of a solar cell? Explain with necessary figure. 07

8(d). Draw and explain the I-V characteristics of solar cell. 06

THE END

$\varphi_m > \varphi_s + n$

$\boxed{\varphi_m > + p}$

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Chittagong University of Engineering and Technology
Department of Electrical & Electronic Engineering
B.Sc. Engineering, Level 3,Term II, Examination-2020-21

Course No : EEE-363/EEE-421(O)

Course Title : Microprocessor and Interfacing

Full Marks : 210

Time : 3 Hours

The figures in the right margin indicate full marks. Answer any three questions from each section. Use separate script for each section.

SECTION – A

1(a) Explain the functions of general purpose registers of 8056 microprocessor. 12

1(b) Explain how cache memory speeds up the operation of a microprocessor. 08

1(c) Fin the correct and incorrect functions from the following instructions. Correct the incorrect instructions showing appropriate causes. Also write down the meaning of each corrected instruction. 15

i. MOV JUMP, AX

ii. POP CS CS can't be pop

iii. PUSH A

iv. LODS [AX], [BX] LODS W OR LODS B

v. JMP AX AX cant be a label

Cache memory provides faster data storage and access by storing instances of programs and data routinely accessed by the processor. Thus, when a processor requests data that already has an instance in the cache memory, it does not need to go to the main memory or the hard disk to fetch the data.

2(a) Describe different types of data addressing nodes available in 8086 microprocessor with at least one example for each type. 15

2(b) An assembly language program is given below, where assume that, SS=2000H, SP=2009H and FL=FFCDH 15

MOV AX, 5566H			PUSH DX	04--->2008
MOV BX, 0402H			PUSH AX	02
MOV CX, 0918H			PUSH FL	55
XCHG BX,CX	BX=0918, CX=0402	CX=FFCD	POP CX	66
MOV DX, 0010H			PUSH CX	FF--FF--
MOV BX, AX	BX=5566	DX=FFCD	POP DX	CD--CD--
MOV DX, CX	DX=0402			

5566. ~~0918~~
AX = 5566
BX = ~~0402~~
CX = 0402.
DX = ~~0010~~. 0402

Determine:

i. The physical address. 22009H

ii. The final value of SS and SP after the end of program. 2000H;2005H

iii. The value of AX, BX, CX, DX and FL after end of the program. 5566,5566,FFCD,FFCD,FFCD

iv. Draw the memory map in details.

2(c) Differentiate between JMP and CALL instruction. 05

3(a) A program and memory maps are shown in Fig. 3(a). Determine:- 15

i. All the register value after the final instruction. AX=5514,SI=2005,DI=2007

ii. The final change in DS and ES memory map.

```
MOV AX, 5566H
MOV SI, 2003H
MOV DI, 2004H
DEC BYTE PTR[SI+2]
CLD
LODS B        AX=5514
STOP W
MOVS B
```

DS map		ES map		
11	2000	AA	2000	
12	2001	AB	2001	
13	2002	AC	2002	
~~14~~	2003	AD	2003	
~~15~~	2004	AE	2004	14
15 ~~16~~	2005	~~0A~~	2005	55
17	2006	~~1A~~	2006	15
18	2007	2A	2007	
19	2008	3A	2008	

Fig. 3(a)

200 3+2

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3(b) Program and DS memory map are given in Fig. 3(b). Find out the following:

i. What is the final value of AX after last instruction? 8CA9

ii. What are the changes of flag bits? C=1, A=1, P=1,0=1, S=1, Z=0

iii. Write down the assembly langue to store the final value of AX into 50 extra segment memory locations. Assume DI=2000H.

```
MOV AX,9DBAH
MOV DI,2000H
MOV CX,32H
REP STOS W
```

```
MOV FL, 0F00H
MOV AX, 1101H
MOV BX, 2000H
XLAT                AX=110F
INC WORD PTR[BX]    FL=0704
LAHF                AX=040F
SUB AX, [BX+3]      AX=9DBA
                    FL=0795
```

DS map

~~0F~~ ~~0E~~ OF	2000
0F ~~0F~~	2001
55	2002
66	2003
77	2004
88	2005
99	2006

77 66

Fig. 3(b)

3(c) Explain the function of JNC and JNZ instructions. 05

4(a) Using JUMP instruction, write an assembly language program for the following series: 1+2+3+4+5+ ……….. + 100 13

```
MOV AX,1H
MOV BX,2H
MOV CX,63H
L1: ADC AX,BX
INC BX
DEC CX
JNZ L1
```

4(b) Write an assembly language program to clear right most 2 bits to set bit number 7, 8, and to invert the 14th and 15th bit position of given value FF0EH. 12

```
MOV AX,FF0EH
AND AX,FFFCH
OR AX,00C0H
XOR AX,C000H
```

4(c) Two blank memory structures are shown in Fig. 4(c). Take the value of CS=1000H, SS= A000H, SP_0=FFFEH. Find the following with the execution of CALL 0FFDH. 10

i. The final value of SP FFFC

ii. Fill up the stack memory

iii. Address of procedure. 1002

Stack memory

AFFFF	
AFFFE	
AFFFD	00
AFFFC	05
AFFFB	
AFFFA	

⋮

11005	
11004	
11003	
11002	
11001	
11000	

⋮

CS Memory

10008	
10007	
10006	
10005	
10004	0F
10003	FD
10002	CALL
10001	
10000	

CALL 0FFDH

0005+0FFD=1002

Fig. 4(c).

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SECTION-B

5(a) Differentiate between minimum mode and maximum mode operation of 8086 microprocessor. 05

5(b) For the following instructions, draw the bus timing diagram showing all the control signals. 12

i. MOV [AX], BX

ii. MOV BX, DX

5(c) The circuit shown in Fig. 5(c) using eight 2764 EPROMs for a 64k×8 section of memory in an 8086 microprocessor-based system. 18

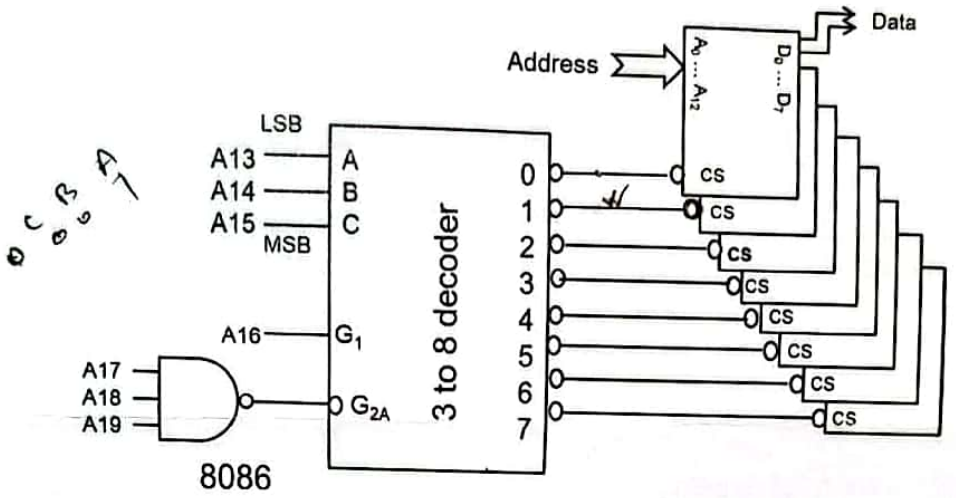

Fig. 5(c)

6(a) Fig. 6(a) represents the interfacing of seven segment LED display with 8086 microprocessor. 15

i. Determine whether it is memory mapped I/O device or isolated I/O device. I/O

ii. Write instruction to display digit 7 at the port.

iii. Why latch is used between decoder and seven segment LEDs?

MOV DL,FDH
MOV AL,F8H
OUT DL,AL

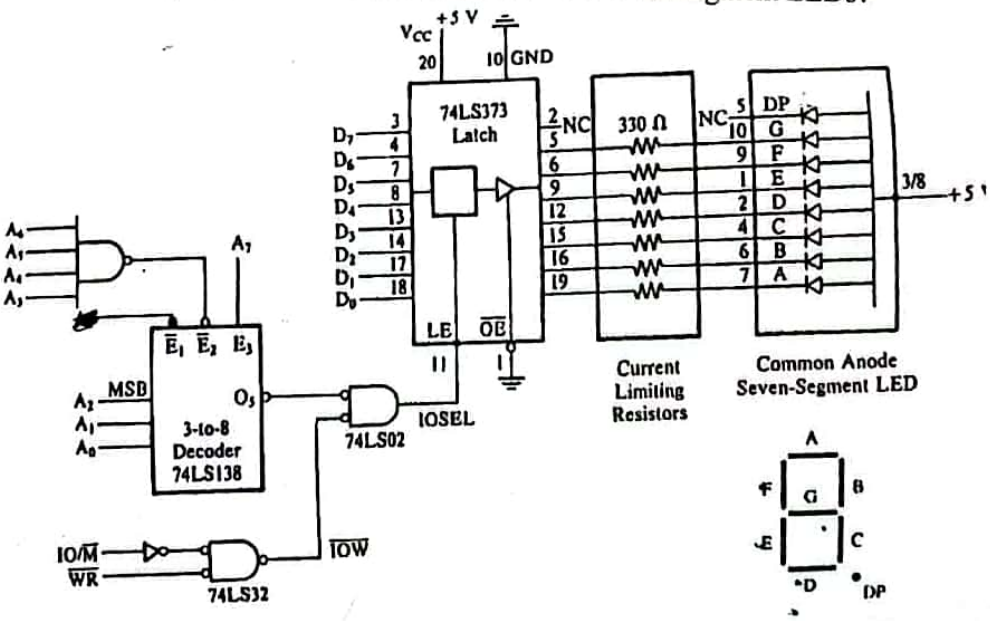

Fig. 6(a)

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6(b) What are the functions of handshaking signals of programmable peripheral interface? Mention two input and output handshaking signals. 10

6(c) Briefly explain the control word format of 8255 PPI in the BSR mode. Also write down one application of BSR mode. 10

7(a) Fig. 7(a) illustrates a 8×8 dual color (Red and Green) dot matrix display. Using EQUATE (EQU) directive, write an assembly language program to illustrate the dots shown in Fig. 7(a) using green LED (solid dots). Assume that the port addresses of PA, PB and PC are 18H, 1AH, and 1CH respectively, where PC is connected to anode. 18

```
PPIC_C EQU 1EH
PPIC   EQU 1CH
PPIB   EQU 1AH
PPIA   EQU 18H
MOV AL,80H
OUT PPIC_C ,AL
MOV AL,00010000B
OUT PPIC,AL
MOV AL,00000000B
OUT PPIB,AL
MOV AL,11111111B
OUT PPIA,AL
```

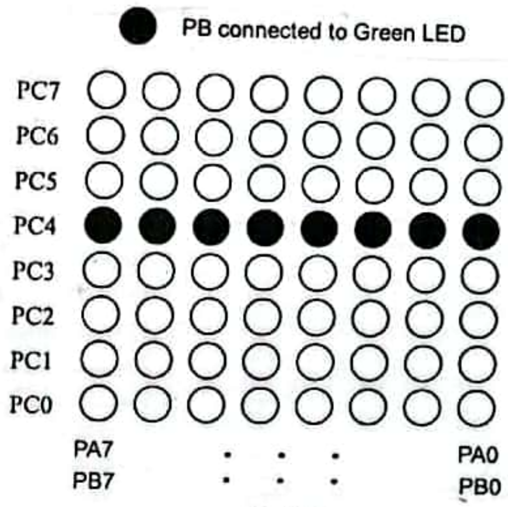

Fig. 7(a)

```
PITC_C EQU 1DH
PITC   EQU 1AH
MOV  AL,10110000B
OUT  PITC_C,AL
MOV  AL,50H
OUT  PITC,AL
MOV  AL,C3H
OUT  PITC,AL
```

7(b) What are the advantages of 8254 PIT over 8253 PIT? 05

7(c) Write a subroutine to initialize counter 2 in mode 0 with a counter of $50{,}000_{10}$ using 8254 PIT. (Set the port address arbitrarily.) 12

8(a) Explain the different modes of 8254 programmable internal timer with neat 13

8(b) How non-mask-able interrupt differs from mask-able interrupt? Explain with relevant examples. 10

8(c) Draw the block diagram of 8259A and define ICWS and OCWS. 12

THE END