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Reg. No._____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, JANUARY 2017

Course Code: **CS203**

Course Name: **SWITCHING THEORY AND LOGIC DESIGN (CS)**

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer All Questions)

1. Convert the following numbers from the given base to the bases indicated
   a) $(250.55)_{10}$ to Hexadecimal (1)
   b) $(357)_8$ to Decimal (1)
   c) $(110101.1011)_2$ to Octal (1)
2. a) Find the 9's and 10's complement of $(13579)_{10}$ (1)
   b) Subtract $(1101)_2$ from $(11010)_2$ using i) 2's complement ii) 1's complement (2)
3. Prove the given Boolean identity using laws of Boolean algebra
   $x+x'y = x+y$ (3)
4. a) Express the given function in sum of minterms form
   $F(x, y, z) = 1$ (1½)
   b) Find the complement of the given Boolean function using De Morgan's theorem
   $F(x,y,z) = x(y'+z)$ (1½)

PART B

(Answer Any Two Questions)

5. a) What is the difference between canonical form and standard form? Which form is preferable while implementing a Boolean function with gates? (2)
   b) Simplify the given Boolean function F (w, x, y, z) =∑(2, 3, 12, 13, 14, 15)
   i) Sum of Products and ii) Product of Sums (use K Map) (7)
6. a) Explain the format of single precision floating point number representation and find the decimal value corresponding to the given floating point number
   $(11000001011110110000000000000000)_2$ (4)
   b) Convert the decimal numbers 596 and 386 into BCD and do the addition and subtraction operations in BCD arithmetic. (3)
   c) What is an alphanumeric code? Why it is useful in digital computers? (2)
7. a) Express the following Boolean function in canonical form
   $F(x, y, z) = x'+yz+xz'+xy'z'+xyz'$ (3)

b) Simplify the Boolean function F (w, x, y, z) = ∑m(0, 5, 7, 8, 9, 10, 11, 14, 15) using Quine-McCluskey method. (6)

PART C

(Answer All Questions)

8. Differentiate between combinational and sequential circuits. (3)
9. Implement the Exclusive OR operation using NAND gates only. (3)
10. Give the excitation table of T Flip Flop. (3)
11. What is *state diagram*? Write down two advantages of state reduction technique. (3)

PART D

(Answer Any Two Questions)

12. a) What is the disadvantage of binary parallel adder? (2)

    b) Draw and explain the logic circuit of 4 bit full adder with look ahead carry. (7)

13. a) Explain the working of JK Flipflop. What is race around condition? How is it overcome? (4)

    b) Implement JK Flip Flop using D Flip Flop. (5)

14. a) Implement a full adder circuit using a 3×8 decoder (additional gates can be used). (5)

    b) Explain clocked sequential circuits with an example. (4)

PART E

(Answer Any Four Questions)

15. a) What is a Universal shift register? (2)

    b) Explain how a shift register is used as a converter from i) serial to parallel data and ii) parallel to serial data (8)

16. a) How does ripple counter differ from synchronous counter? (3)

    b) Design a synchronous counter with the following repeated binary sequence 000, 100, 111, 010, 011 using T Flip Flops. (7)

17. a) Compare RAM and ROM. (3)

    b) Implement the following Boolean functions using a 3×4×2 PLA

    $F1 = \Sigma (0, 1, 3, 4)$

    $F2 = \Sigma (1, 2, 3, 4, 5)$ (7)

18. Draw the block diagram of a 4 -bit ripple counter. Sketch the waveform at the output of each Flip Flop. Explain how this wave form is obtained. By what number N does this system divide? (10)
19. Write an HDL code for a full adder in all three modelling styles. (10)
20. Explain the algorithm for floating point subtraction. (10)