American International University- Bangladesh
Department of Faculty of Engineering
EEE 3102: Digital Logic & Circuits Laboratory

Title: Construction Logic Gates using various MOS transistors

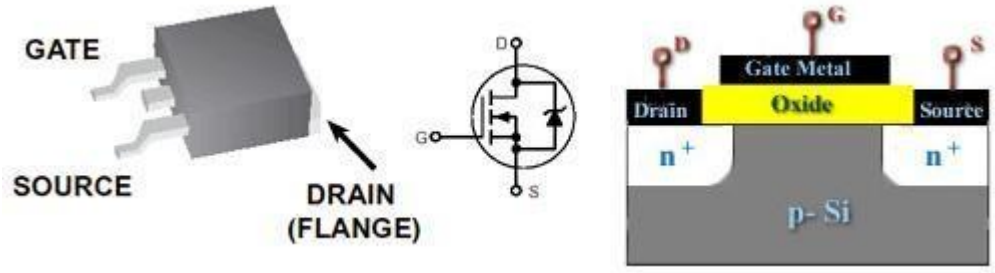
Part I: Construction of MOSFET Logic Gates

Introduction:

MOSFET:
Pronounced MAWS-feht. Acronym for metal-oxide semiconductor field-effect transistor. These are used in many scenarios where you want to convert voltages. On your motherboard for example to generate CPU Voltage, Memory Voltage, AGP Voltage etc. Mosfets are usually used in pairs. If you see six mosfets around your CPU socket you have three-phase power.

Technical Info

MOSFETs come in four different types. They may be enhancement or depletion mode, and they may be n-channel or p-channel. For this application we are only interested in n-channel enhancement mode MOSFETs, and these will be the only ones talked about from now on. There are also logic-level MOSFETs and normal MOSFETs. The only difference between these is the voltage level required on the gate.



Unlike bipolar transistors that are basically current-driven devices, MOSFETs are voltage-controlled power devices. If no positive voltage is applied between gate and source the MOSFET is always non- conducting. If we apply a positive voltage UGS to the gate we'll set up an electrostatic field between it and the rest of the transistor. The positive gate voltage will push away the 'holes' inside the p-type substrate and attracts the moveable electrons in the n-type regions under the source and drain electrodes. This produces a layer just under the gate's insulator through which electrons can get into and move along from source to drain. The positive gate voltage therefore 'creates' a channel in the top layer of material between oxide and p-Si. Increasing the value of the positive gate voltage pushes the p-type holes further away and enlarges the thickness of the created channel. As a result we find that the size of the channel we've made increases with the size of the gate voltage and enhances or increases the amount of current which can go from source to drain- this is why this kind of transistor is called an enhancement mode device. Hence the operation of a p-channel MOSFET is just the opposite of an n-channel MOSFET.

MOSFET testing

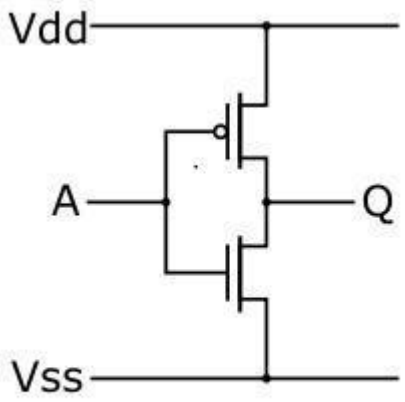
Get a multimeter with a diode test range. Connect the meter negative to the MOSFET's source. Hold the MOSFET by the case or the tab if you wish, it doesn't matter if you touch the metal body but be careful not to touch the leads until you need to. Do NOT allow a MOSFET to come in contact with your clothes,

plastic or plastic products, etc. because of the high static voltages it can generate. First touch the meter positive on to the gate. Now move the positive meter probe to the drain. You should get a low reading. The MOSFET's gate capacitance has been charged up by the meter and the device is turned on. With the meter positive still connected to the drain, touch a finger between source and gate (and drain if you wish, it doesn't matter). The gate will be discharged through your finger and the meter reading should go high, indicating a non-conducting device.

CMOS:

Complementary metal–oxide–semiconductor (**CMOS**) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. Frank Wanlass patented CMOS in 1963 (US patent 3,356,858).

CMOS is also sometimes referred to as **complementary-symmetry metal–oxide–semiconductor** (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.



CMOS inverter (NOT logic gate)

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

Some advantages of CMOS over TTL are:

- CMOS gate inputs draw far less current than TTL inputs, because MOSFETs are voltage-controlled, not current-controlled, devices.

- CMOS gates are able to operate on a much wider range of power supply voltages than TTL: typically 3 to 15 volts versus 4.75 to 5.25 volts for TTL
- CMOS transistors are smaller in size and provide less power dissipation than NMOS transistors.

In this experiment, we will first look at some logic circuit designs using NMOS. Then we will implement the same logic circuits using CMOS and try to identify the potential design advantages of CMOS over NMOS.

Theory and Methodology:

NMOS Inverter with Ohmic/ Resistive Load:

Considering an ideal scenario, when a HIGH (+5V) is applied to the input, the NMOS transistor turns ON and current flows from Vdd to ground; thus output voltage, Vo= 0V.
Similarly, if a LOW (0V) is applied to the input, the NMOS remains in its OFF state. As a result, the current from Vdd has no path to ground. The output voltage is +5V

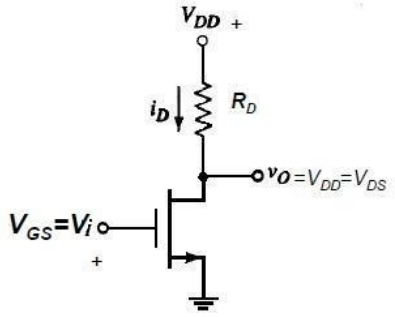


Fig.1: NMOS Inverter with Ohmic/Resistive Load

NMOS Inverter with NMOS Enhancement Transistor load:

One disadvantage of designing NMOS logic circuits with ohmic load is that even when the NMOS is OFF, there is static power dissipation due to the resistor. A better design is to use an enhancement-type NMOS as load. They are "*normally-off*" devices and it takes an applied voltage between gate and drain of the correct polarity to bias them *on*. Thus static power consumption is avoided

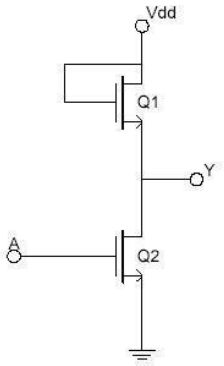


Fig.2 NMOS Inverter with NMOS Load

NMOS NAND Gate:

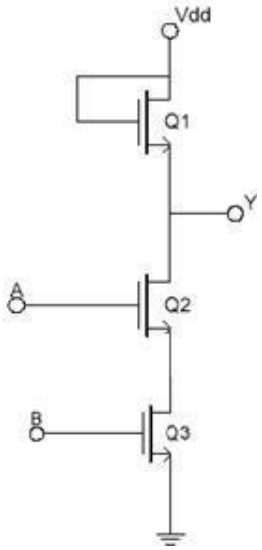


Fig.3 NMOS NAND Gate

NMOS NOR Gate:

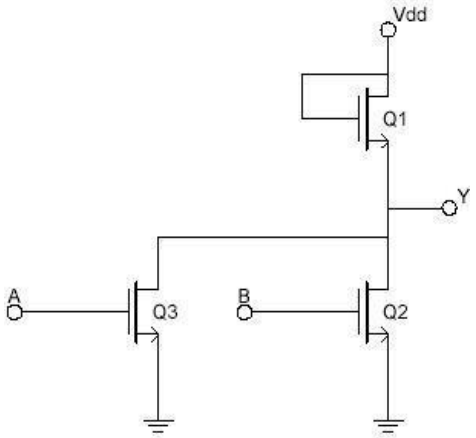


Fig.4 NMOS NOR Gate

CMOS Logic:

CMOS transistors are smaller in size and provide less power dissipation than NMOS transistors. Thus they became the obvious choice of replacing NMOS transistors at the integrating circuit level design in all applications.

CMOS consists of one p-channel MOSFET or PMOS and one NMOS. The two MOSFETs are designed to have matching characteristics. Thus, they are complementary to each other. When OFF, their resistance is effectively infinite; when ON, their channel resistance is quite low (around 200 Ω). Since the gate is essentially an open circuit it draws no current and the output voltage will be equal to either ground or to the power supply voltage, depending on which transistor is conducting.

CMOS Inverter:

When the input is grounded (logic 0), the N-channel MOSFET is unbiased, and therefore has no channel enhanced within itself. It is an open circuit, and therefore leaves the output line disconnected from ground. At the same time, the P-channel MOSFET is forward biased, so it has a channel enhanced within itself. This channel has a resistance of about 200 Ω, connecting the output line to the +V supply. This pulls the output up to +V (logic 1).

When input A is at +V (logic 1), the P-channel MOSFET is off and the N-channel MOSFET is on, thus pulling the output down to ground (logic 0). Thus, this circuit correctly performs logic inversion, and at the same time provides active pull-up and pull-down, according to the output state.

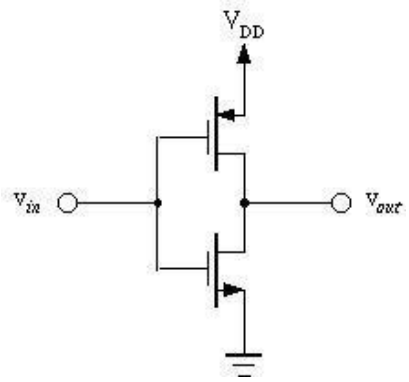


Fig.5 CMOS Inverter

CMOS NAND Gate:

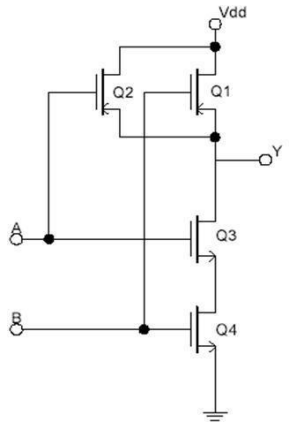


Fig.6 CMOS NAND Gate

CMOS NOR Gate:

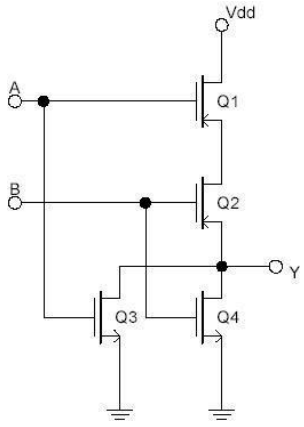
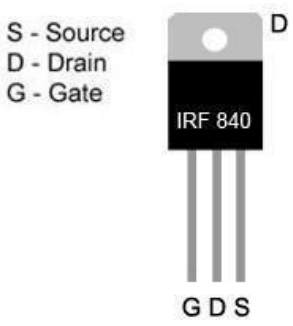


Fig.7 CMOS NOR Gate

MOSFET pin configuration:



Apparatus:

(1) 10KΩ resistor (brown-black-orange).

(2) 1N914 diodes or equivalent.

(3) Connecting wires.

(4)Trainer Board

Precautions:

Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply only enough voltage (within V_{DD}) to turn on the transistors and/or chip, otherwise it may get damaged.

Experimental Procedure:

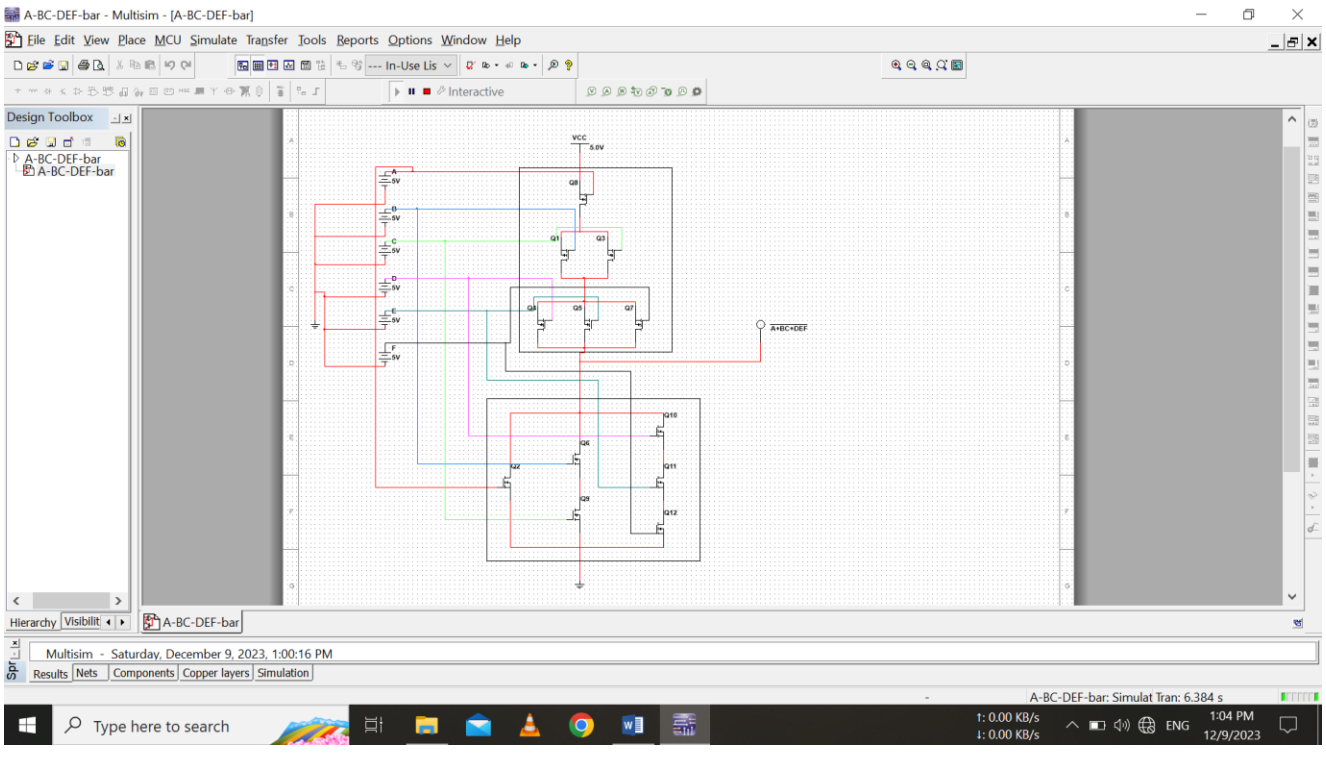
1. Set up the circuit for NMOS inverter as shown in Fig.1.
2. For each input combination, find the output and place them in a Truth Table. The Truth Table should have two sets of outputs- one ideal and one experimental.
3. Repeat steps 1 and 2 for each circuit set-up from Fig.2 to Fig. 7.

Report:

1. For, each of the above set-ups, describe in words what the data means. Did your results match the expected ideal outputs? If not, explain why?

   Ans: For inverter setup, the output truth table interprets that if inputs are HIGH, the output will be below and if input is low, the output will be high.
   The NAND gate has an output that is normally at logic high and only goes to logic low when all of its inputs are at logic high.
   For the NOR Gate, A HIGH output (1) results if both the inputs to the gate are LOW (0); if one or both input is HIGH (1), a LOW output (0) results. NOR is the result of the negation of the OR operator. Yes, the truth table clearly shows us that the results matched the expected ideal outputs.

2. Implement logic function Vout = $\overline{A+ BC+ DEF}$ using: CMOS



Part II: Designing a Half Adder using CMOS

Introduction:
ADDER:

In electronics, an **adder** or **summer** is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations.

Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder– subtractor. Other signed number representations require a more complex adder.

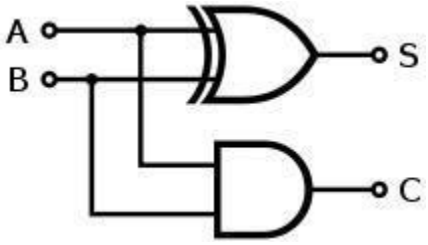


Fig-1 Half adder logic diagram

The **half adder** adds two single binary digits *A* and *B*. It has two outputs, sum (*S*) and carry (*C*). The carry signal represents an overflow into the next digit of a multi-digit addition. The value of the sum is 2*C* □*S*. The simplest half-adder design, pictured above, incorporates an XOR gate for S and an AND gate for C. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder.

The half-adder adds two input bits and generate carry and sum which are the two outputs of half-adder. The input variables of a Half adder are called the Augend and addend bits. The output variables are the Sum and Carry. The

Truth table and equations for the Half adder are :

$$\mathrm{S} = A \oplus B$$

$$\mathrm{C} = AB$$

A	B	A+B	S	C
0	0	0	0	0
0	1	1	1	0
1	0	1	1	0
1	1	2	0	1

This experiment is to help the student in understanding the design at the transistor level.

Theory and Methodology:

To design any logic circuit first the truth table is needed to be established using different combinations of logic '0' and '1' to get the desired output. After that the gate level design is found from which transistor level design is done using desired transistors. Here CMOS is used for the transistor level design of the Half Adder. The whole process is given step wise below:

Half Adder:

Gate Level Design:

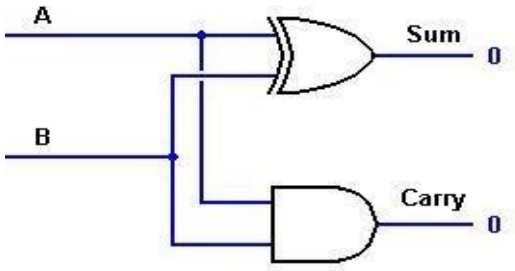


Fig-2 Logic diagram of a Half Adder.

Equation of Sum = A (XOR) B

$$= A\bar{B} + \bar{A}B$$

This equation can be rewritten as $= \overline{\overline{A\bar{B}} + \overline{\bar{A}B}}$

$$= \overline{AB + \bar{A}\bar{B}}$$

Equation of Carry= AB

Apparatus:

(4) PMOS,
(5) NMOS,
(6) IC 7404(Inverter).
(7) Connecting wires.
(8) Trainer Board

Precautions:

Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply only enough voltage (within V_{DD}) to turn on the transistors and/or chip, otherwise it may get damaged.

Experimental Procedure:

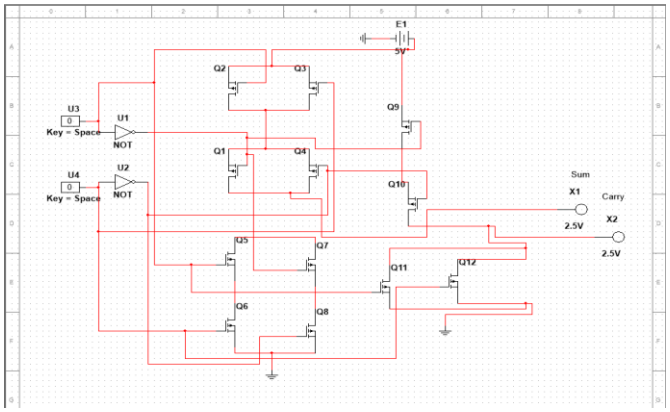
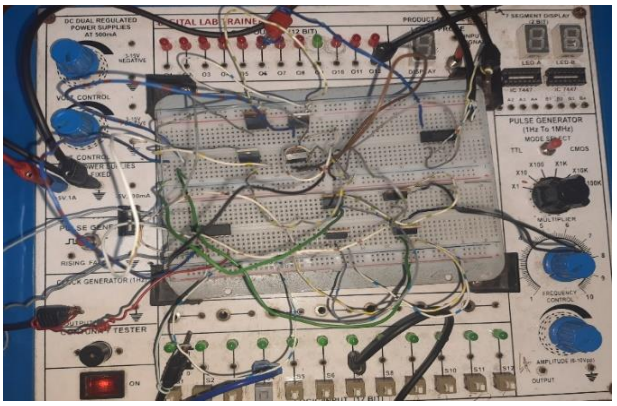
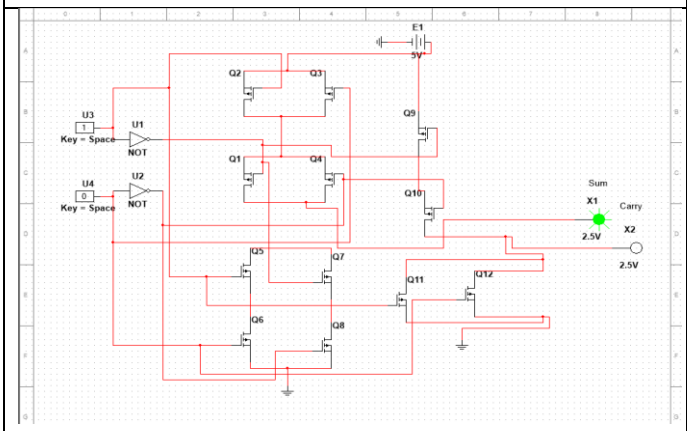
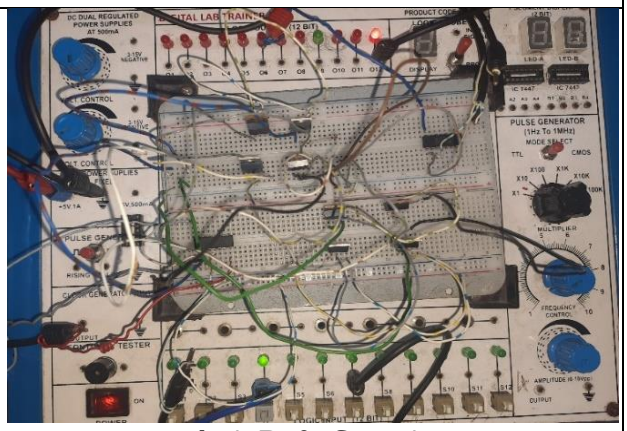
Construct the Half adder circuit using CMOS on your breadboard based on provided expression and truth table. At first draw the schematic circuit diagram for the SUM and CARRY then show to the Instructor. After that record the values in the table below.

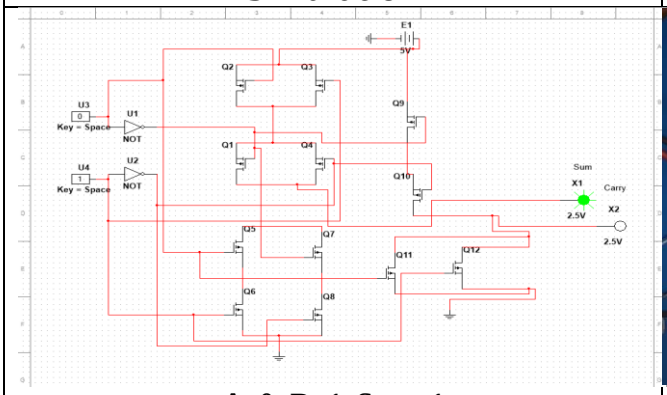
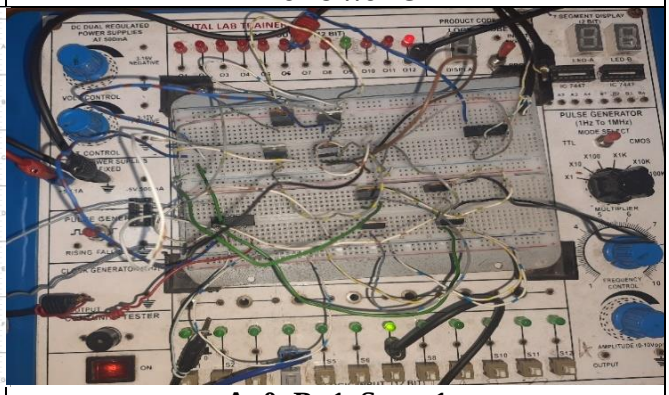
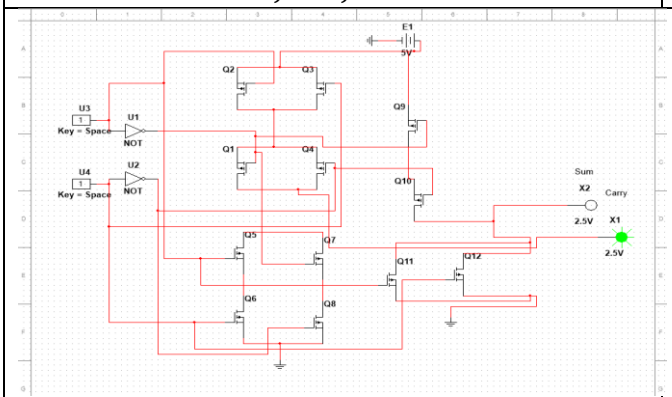
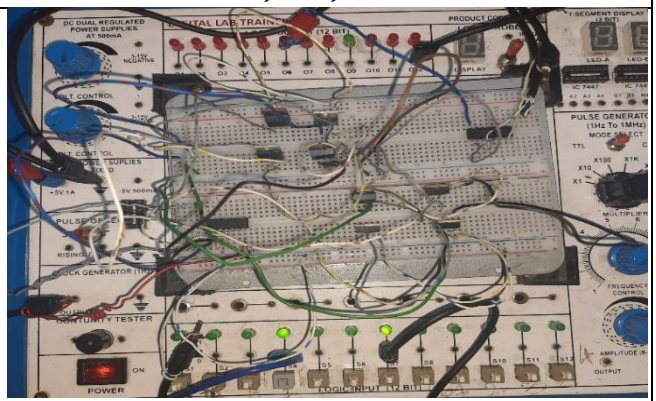
Input A	Input B	Carry Out	Sum
0 V	0 V	0	0
0 V	5 V	0	1
5 V	0 V	0	1
5 V	5 V	1	0

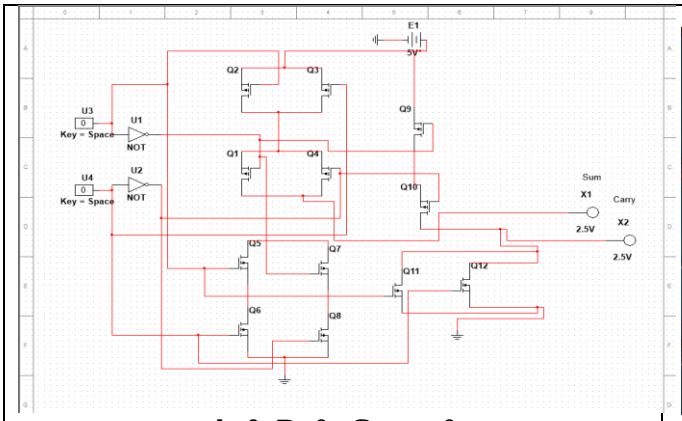
Simulation and Measurement:

Half-Adder Truth Table:

A	B	C_{out}	$\sum$
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Simulation	Hardware
	
A=0, B=0 , Sum=0	A=0, B=0 , Sum=0
	
A=1, B=0 , Sum=1	A=1, B=0 , Sum=1

Simulation	Hardware
	
A=0, B=1, Sum=1	A=0, B=1, Sum=1
	
A=1, B=1 , Sum=0	A=1, B=1 , Sum=0



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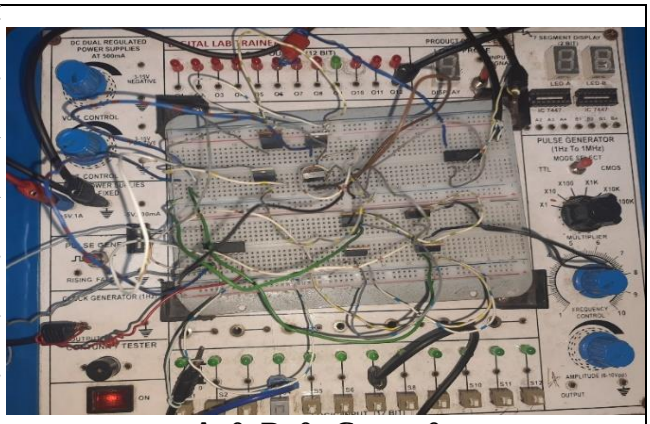

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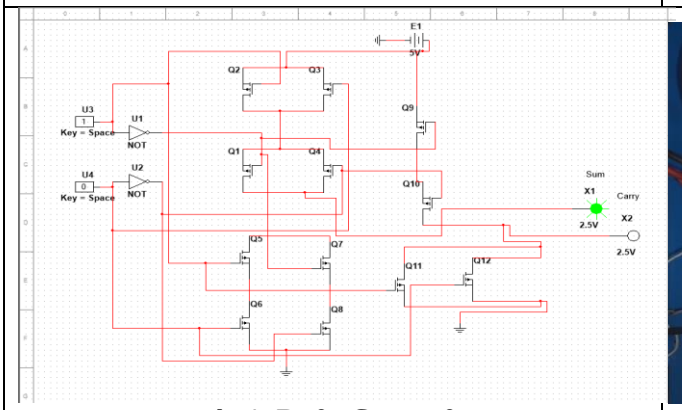

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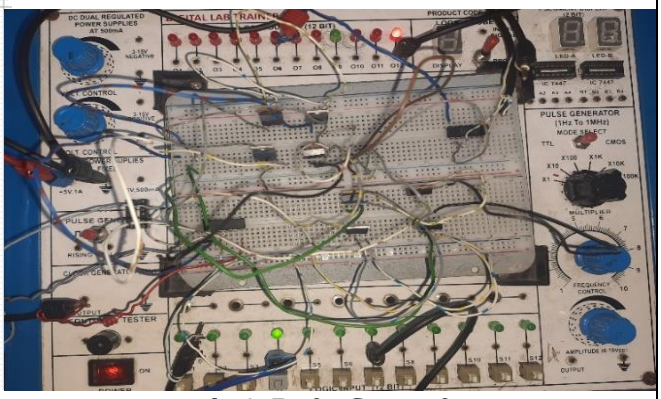
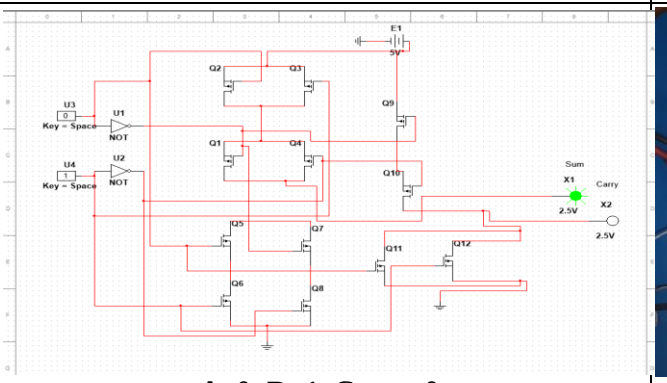


A=1, B=0 , Carry=0

Simulation	Hardware



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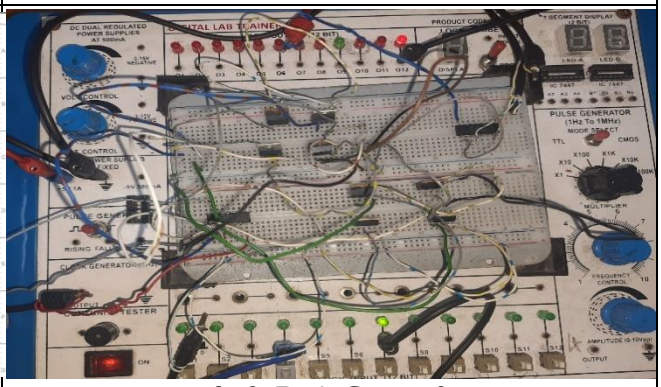

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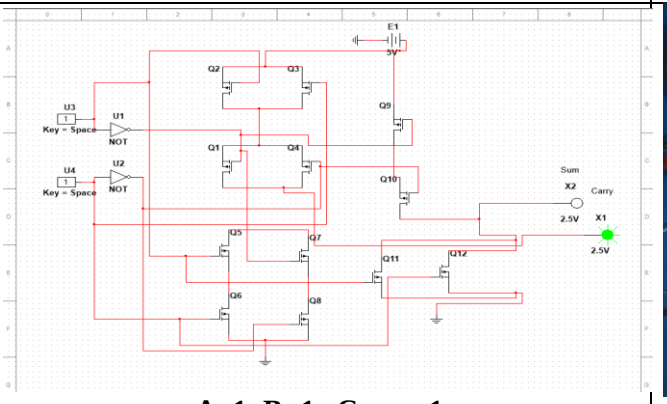
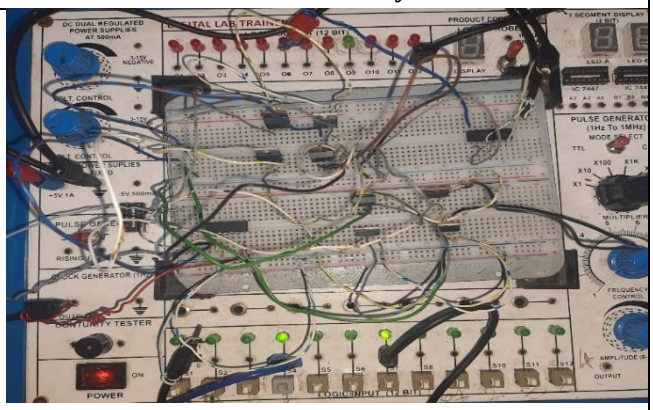


A=1, B=1 , Carry=1



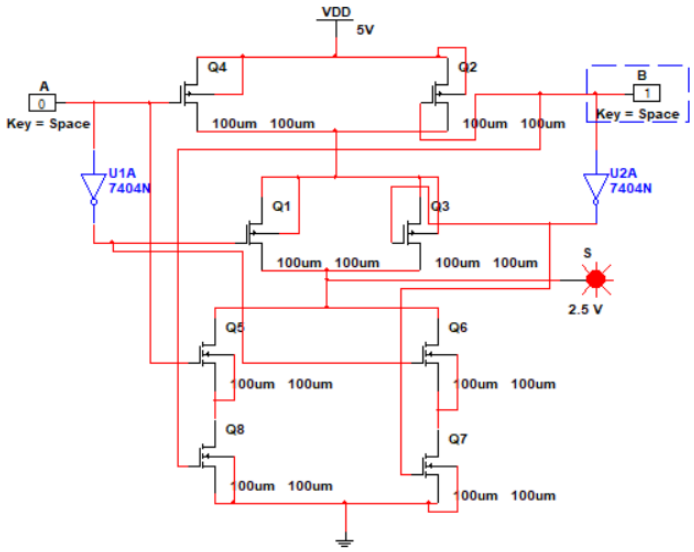
A=1, B=1 , Carry=1

Report:

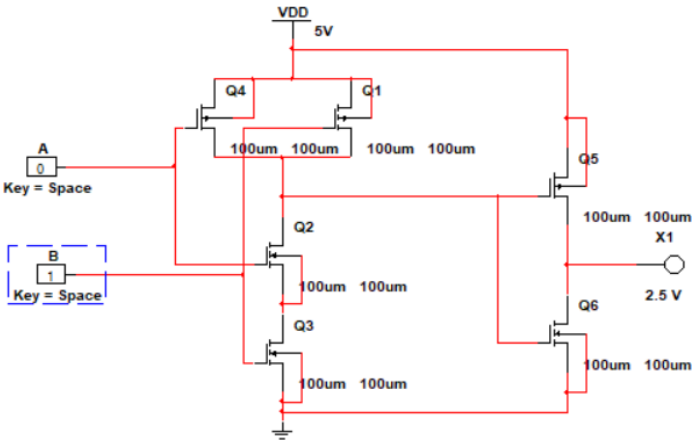
4. Document the data acquired from the hardware, from simulation as well as the expected values for the CarryOut and Sum of the Half Adder.

Half Adder using CMOS:

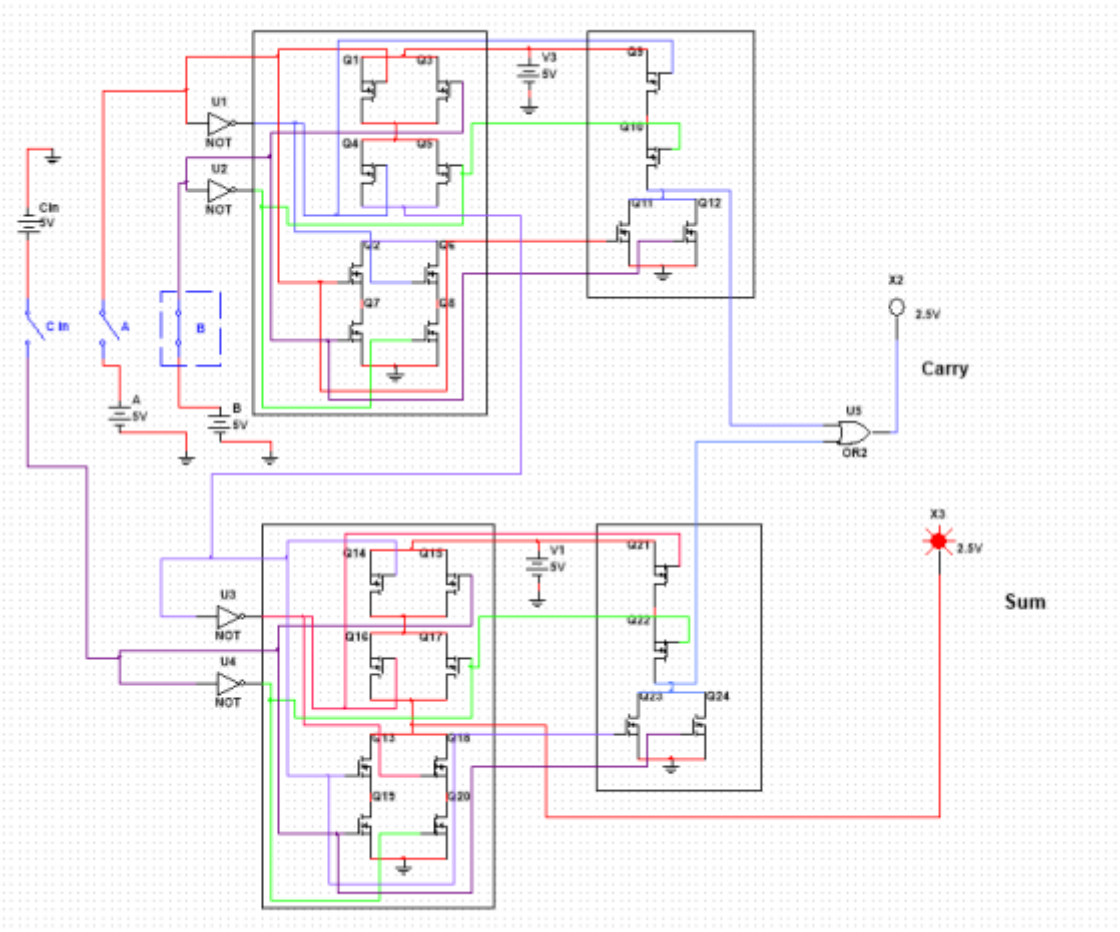
SUM:



Caryy Out:



5. Draw the circuit diagram of a Full Adder using CMOS.



Full Adder Using CMOS

Discussion and Conclusion:

The main goals of this experiment were to gain familiarity with CMOS logic, understand the design process of an inverter, NAND, and NOR gate using CMOS MOSFET. During the hardware implementation phase, we encountered challenges in realizing the CMOS NOR Gate, leading to a significant increase in the time invested. Nevertheless, the overall results were outstanding and aligned with the values in the truth table. Also, NI Multisim version 14.2 was employed. We successfully integrated all components on the Multisim breadboard without encountering any issues. The connection between circuit wires was established seamlessly, and all simulation circuits were executed with outputs consistent with theoretical expectations. No discrepancies or errors were identified in the output values. Consequently, it can be asserted that the hardware implementation was validated by the simulation results and truth table.

We constructed a Half Adder using CMOS logic, achieving success in the experiment. Initially, we designed the sum circuit and then proceeded to construct the carry-out circuit separately. The sum circuit diagram involved the utilization of 4 P-MOS and 4 N-MOS MOSFET.

Reference(s):

1. Thomas L. Floyd, *Digital Fundamentals*, 9th Edition, 2006, Prentice Hall.
2. Link: http://www.techpowerup.com/articles/overclocking/voltmods/21