

2. MODELING OF ELECTRONIC SYSTEMS

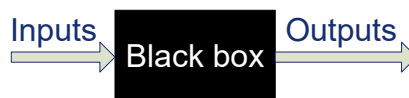
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Projecto, Teste e Fiabilidade de Sistemas Electrónicos – 2019/2020

1

Basic Concepts



The relationship between inputs and outputs defines the behavior of the system

Some examples of models used to describe an electronic system are ...

- Structural models
- Functional models at logic level
- Behavioral models (VHDL, Verilog or even C)



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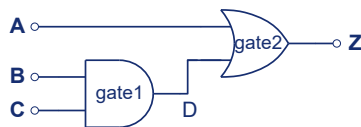
2

2

Structural Models

- The structural models describe the system as a set of sub-systems or components
- The *smallest* components (lowest hierarchical level) are called **primitives**
- Block diagrams and schematics are examples of structural models

Graphical representation



Textual representation

```
module gate (Z, A, B, C);  
input A, B, C;  
output Z;  
wire D;  
and gate1 (D, B, C);  
or gate2 (Z, A, D);  
endmodule
```

Functional Models at Logic Level

Truth tables and primitive cubes

The function $Z(x_1, x_2, \dots, x_n)$ needs a table with 2^n entries to be fully defined

If the number of outputs of Z is m , then we will need m tables to describe the function

When the tables are compressed using the “*don’t care*” symbols, we obtain a representation called **cubic notation**

Functional Models at Logic Level

Truth table

x_1	x_2	x_3	Z
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Primitive cubes

x_1	x_2	x_3	Z
x	1	0	0
1	1	x	0
x	0	x	1
0	x	1	1

Functional Models at Logic Level

Sequential circuits

- A sequential function can be modeled as a **Finite State Machine (FSM)**
- The FSMs ...
 - present a finite number of internal states
 - change from one state to another in response to some external inputs
 - can be described using **state transition tables** or **state diagrams**

Functional Models at Logic Level

State transition table

Present state	Condition		
	X	Y	Z
A
B	...	<next state>, <output>	...
C

The transitions between states are synchronous to a clock signal

The outputs can be associated to the present state (**Moore machines**) or associated to the state transitions (**Mealy machines**)

The example represented in the table corresponds to a Mealy machine

7

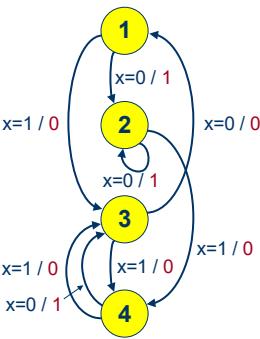
Functional Models at Logic Level

State transition table

Present state	Input (x)	
	0	1
1	2,1	3,0
2	2,1	4,0
3	1,0	4,0
4	3,1	3,0

<next state>, <output>

State diagram

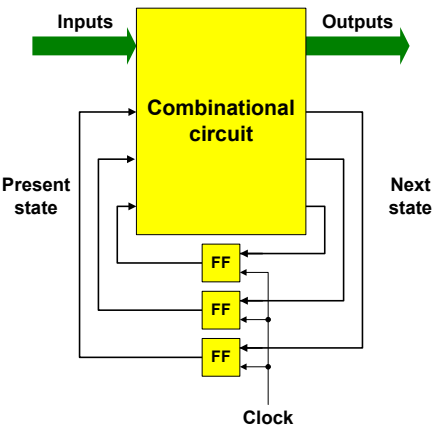


The state is stored in flip-flops

8

Functional Models at Logic Level

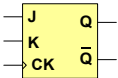
Canonical structure of a synchronous sequential circuit



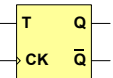
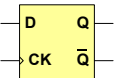
Functional Models at Logic Level

Description of three types of flip-flops

JK				
Q	00	01	11	10
0	0	0	1	1
1	1	0	0	1



D		
Q	0	1
0	0	1
1	0	1

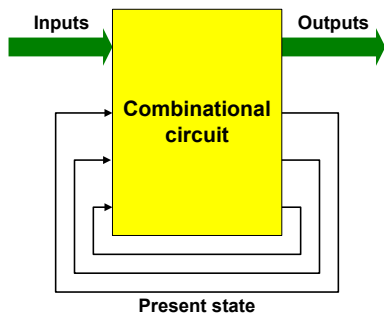


T		
Q	0	1
0	0	1
1	1	0

The flip-flops are finite state machines with 2 states

Functional Models at Logic Level

Canonical structure of an asynchronous sequential circuit



There is no clock signal

11

Functional Models at Logic Level

State transition table (asynchronous circuit)

Present state	Inputs ($x_1 x_2$)			
	00	01	11	10
1	1,0	5,1	2,0	1,0
2	1,0	2,0	2,0	5,1
3	3,1	2,0	4,0	3,0
4	3,1	5,1	4,0	4,0
5	3,1	5,1	4,0	5,1

Stable configurations (marked in red and bold in the table):

<next state> = <present state>

12

Functional Models at Logic Level

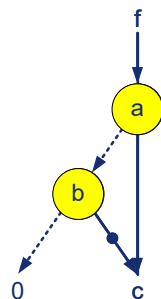
Binary Decision Diagrams (BDD)

- Describes a circuit functionality as a **graph**
- It is a very compact representation of a Boolean function
- The output value is obtained by traversing the graph, analyzing the input values in a given sequence
- The BDDs are extensively used in the CAD tools, namely, in the logic synthesis
- The size of the BDD depends on the ordering of the variables

Functional Models at Logic Level

Binary Decision Diagrams (BDD)

- The procedure starts at the root of the graph
- In each node, we decide to follow the **left edge** or the **right edge** depending on the value of the variable (**0** or **1**), respectively
- A circle in an edge complements the value of the variable associated to that edge



$$f = \bar{a}.b.\bar{c} + a.c$$

Evaluate **f** for ...

1. **abc = 001**
2. **a = 1**

Functional Models at Logic Level

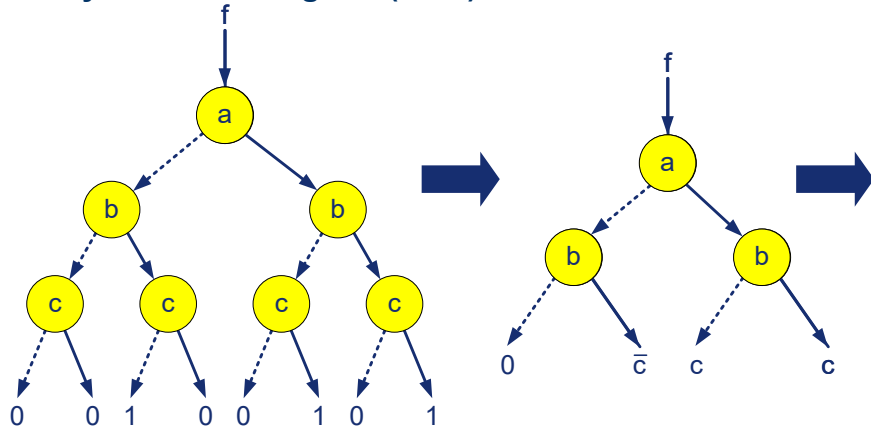
Binary Decision Diagram (BDD)

a	b	c	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

$f = \bar{a}.b.\bar{c} + a.c$

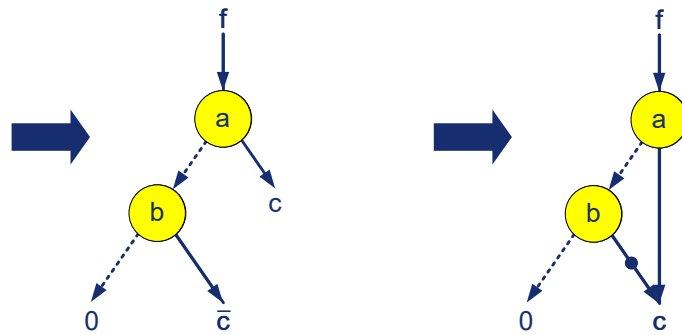
Functional Models at Logic Level

Binary Decision Diagram (BDD)



Functional Models at Logic Level

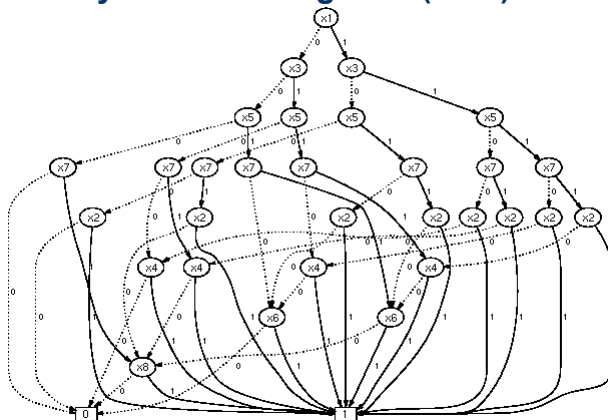
Binary Decision Diagram (BDD)



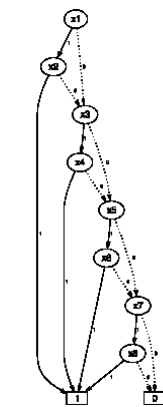
17

Functional Models at Logic Level

Binary Decision Diagrams (BDD)



Bad variable ordering



Good variable ordering

18