4. TEST OF ELECTRONIC SYSTEMS

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Outline

- Introduction to the test of electronic systems
- Reliability
- Test economics
- Quality metrics
- Test phases: planning, preparation, application

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Test Objectives

- to discriminate good from defective devices
  GOOD means without manufacturing defects, operating according to product specifications
- to diagnose and locate faults
  for repair or monitoring process line quality and improvement

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Test and Diagnosis

- **Test**: analysis of the system outputs in order to evaluate its behavior
- **Diagnosis**: locates the cause of the incorrect response. Requires …
  - knowledge of the internal structure of the system (black box model is not enough)
  - run fault simulation to generate a fault dictionary

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Testing

- as an **END** to …
  - identify design errors,
  - identify defective parts,
  - perform failure diagnosis
- as a **MEAN** to …
  - reinforce the product quality,
  - obtain defect statistics,
  - evaluate the reliability at component or system level

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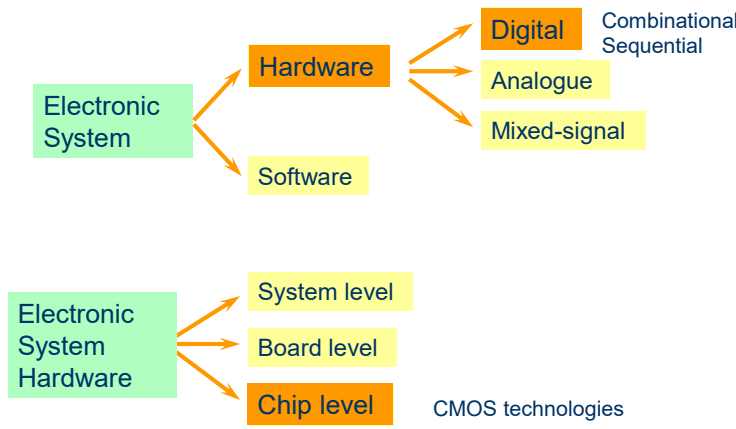
Test Context



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Failures, Defects and Faults

- A **failure** occurs when the system functionality differs from the specified functionality
- A **physical defect** is a modification of the physical structure of a device, compared to the original design (e.g. missing material, extra material, crystal defects)
- The **faults** are the modifications of the circuit topology
- A fault is called a **realistic fault** when the modification of the circuit topology is caused by a **physical defect**

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Test Possibilities

Test phases	Fault manifestation	Test operation modes	Test application
Prototype	Permanent	Off-line	External
Production	Transient	On-line	Internal (BIST)
System	Intermittent		
Field			

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Fault Manifestation

- **Permanent faults**: affects the behavior of a system permanently. Examples:
  - broken lines
  - short circuited lines
  - design errors
- **Transient faults**: are caused by environmental conditions such as cosmic rays, humidity, temperature
- **Intermittent faults**: are caused by non-environmental conditions such as deteriorating or ageing components

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Test Operation Modes

- ***Off-line* testing**: the system stops normal operation, the test vectors are applied and the responses are compared against the correct ones
  - Test vector generation requires high effort: an ATPG (**A**utomatic **T**est **P**attern **G**enerator) is needed
- ***On-line* testing**: the system is continuously checking for any incorrect behavior
  - No test vectors are needed, but extra hardware has to be added to the original circuitry (e.g. checkers).
  - Typically applied to safety critical applications (for instance, avionics)

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Benefits of a Good Quality Test

- Shorter Time-to-Market
- Lower manufacturing cost (reduce test application time)
- Lower investment in ATE (Automatic Test Equipment)
- Increased system up-time
- Increased product reliability
- Lower field/maintenance cost

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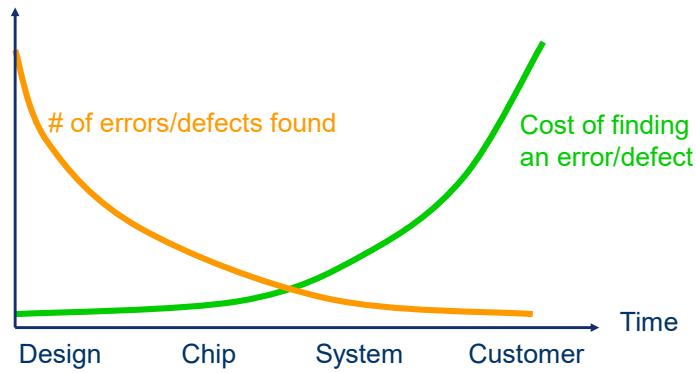
Test



The later you have a problem, the higher price it will cost you

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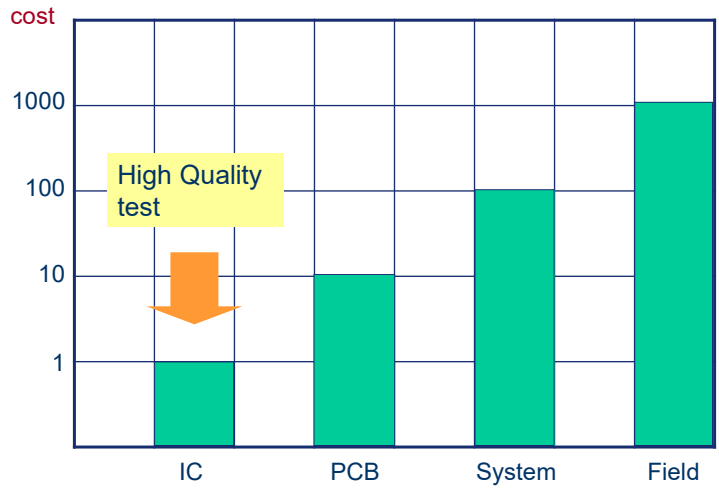
Rule of Ten



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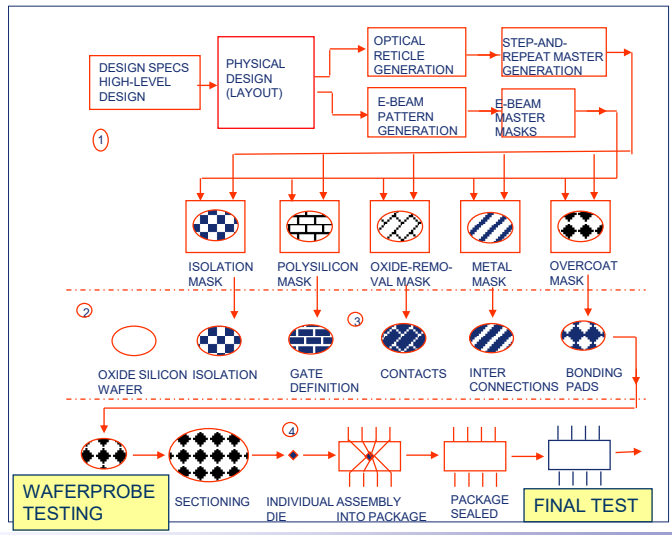
Manufacturing Tests



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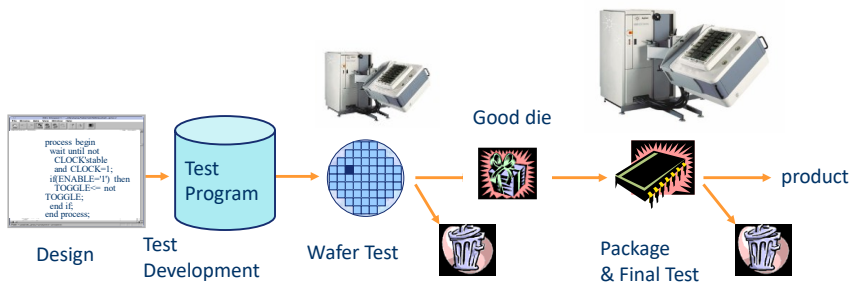
Manufacturing Test

- Verifies correctness of manufactured hardware
- Test application performed on every manufactured device



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Burn-in or Stress Test

- **Procedure**
  - Subject chips to high temperature & over-voltage supply, while running production tests
- **Catches**
  - Weak components that have a high risk of failing during early life under normal operating conditions. These component failures are called freak failures.
  - The failures can be mechanical such as a weak wire bond, or a defective metal line

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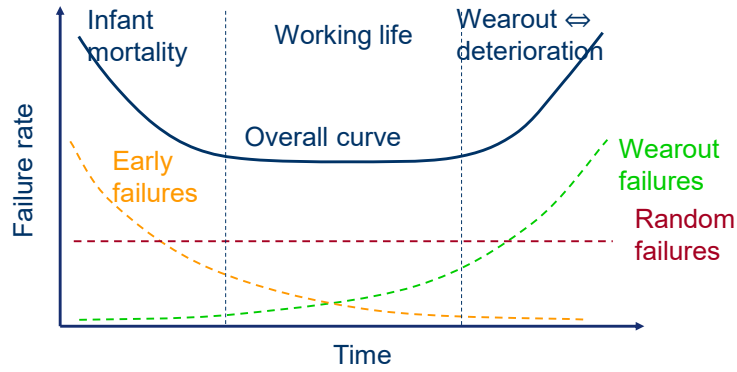
Bathtub Curve



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Reliability

- The time at which a failure occurs can be considered a random variable
- The probability of a failure before time ***t***, **F(t)**, is the **unreliability** of a system
- The **reliability** of a system, **R(t)**, is the probability of a correct functioning system at time ***t***; it can be expressed as

$$R(t) = 1 - F(t)$$

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Reliability

The mean time to failure (MTTF) is expressed as

$$\mathbf{MTTF} = \int_0^\infty \mathbf{R(t)}\ \mathbf{dt}$$

Assuming a system with the following reliability: $\mathbf{R(t)} = e^{-\lambda t}$

and assuming that faults occur randomly, the MTTF is given by

$$\mathbf{MTTF} = \int_0^\infty e^{-\lambda t}\ \mathbf{dt} = \frac{\mathbf{1}}{\boldsymbol{\lambda}}$$

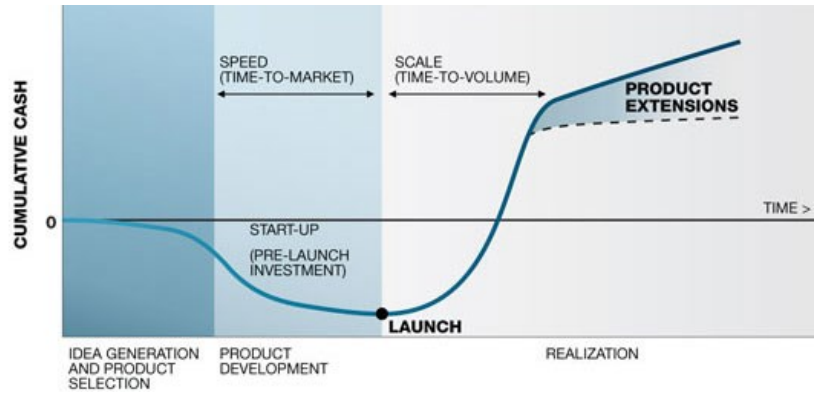
New Product Development

- Innovation
- Performance
- Complexity
- Quality
- Time-to-Market

Test represents a growing percentage of the development costs and a barrier to Time-to-Market reduction

6 months delay ⇒ 30% loss in total profit

Time-to-Market and Time-to-Volume



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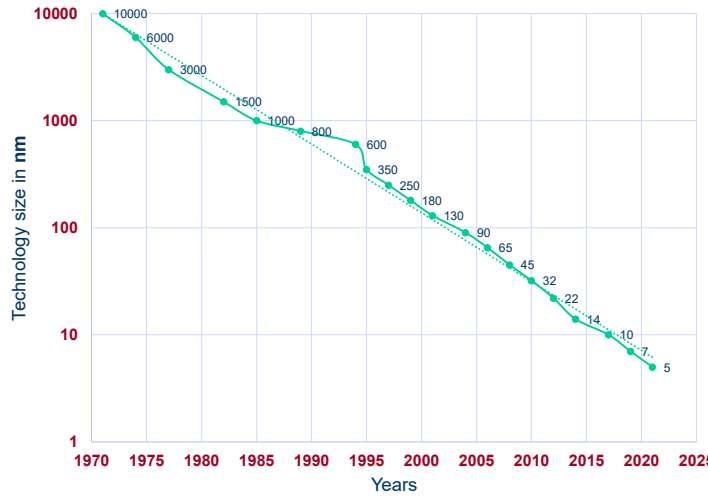
Product Complexity: Technology Size



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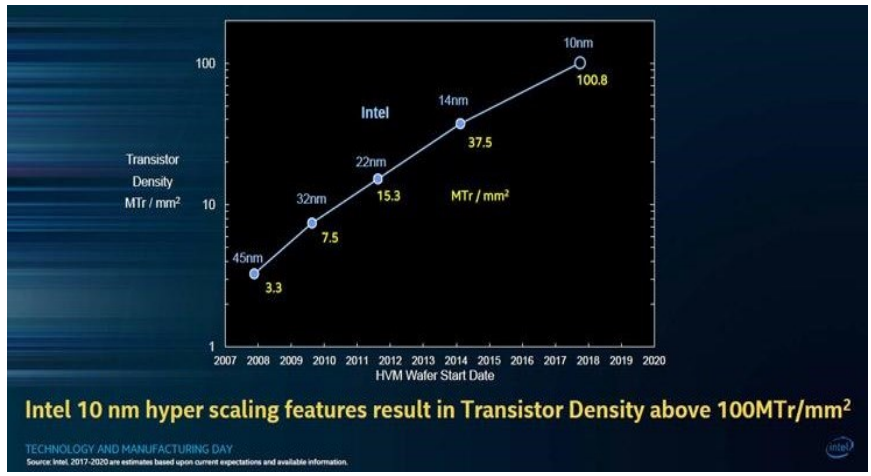
Product Complexity: Transistor Density



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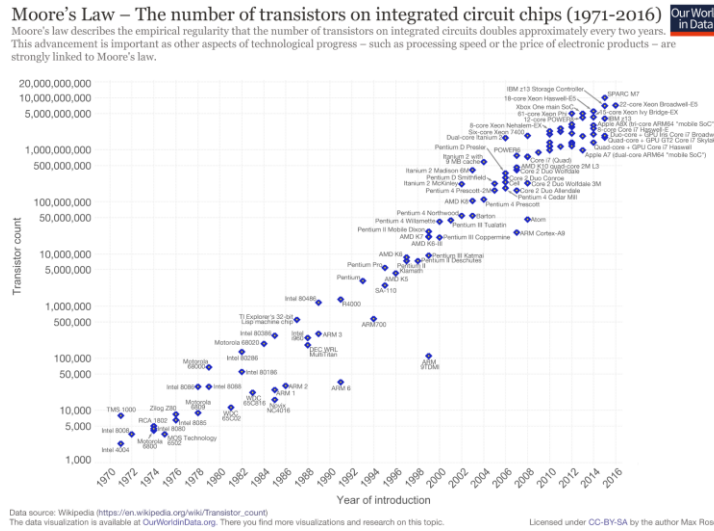
Product Complexity: Transistor Count



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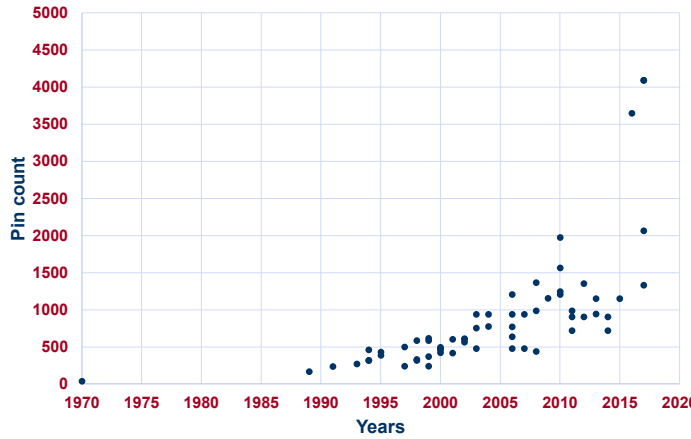
Testing Complexity: Pin Count



Transistor count increases much faster than the number of pins (transistors / pin is increasing) ➡ **higher testing complexity**

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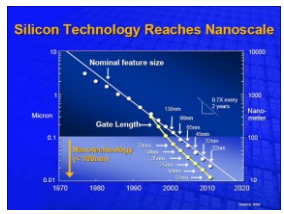
Test Issues



- Controllability
- Observability

- Huge test data volume
- Bandwidth of ATE – DUT communication
- ATE costs

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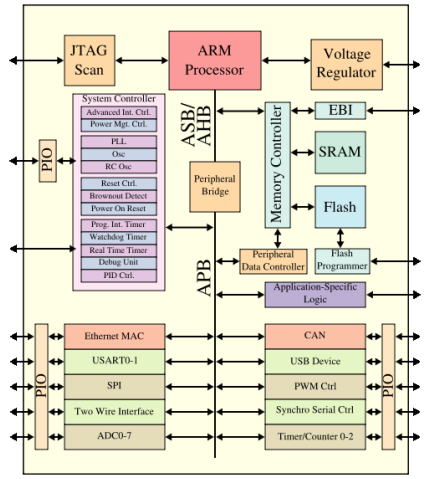
System on a Chip (SoC) Design



Issues

- Functionality
- Timing
- Power
- Testability

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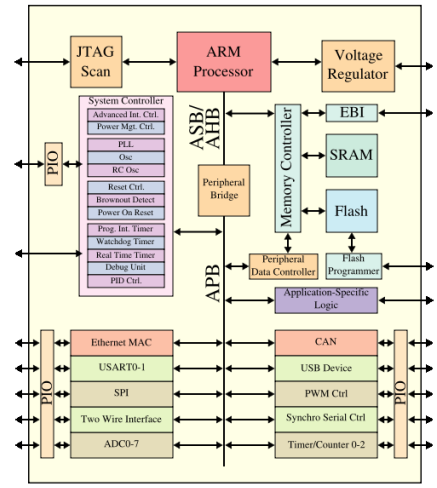
Product Heterogeneity

- Digital, Analog, Mixed-Signal
- Multiple clocks domains
- Different IP vendors
- Different tools
- …

Test requires
• organization
• standards

System on a Chip



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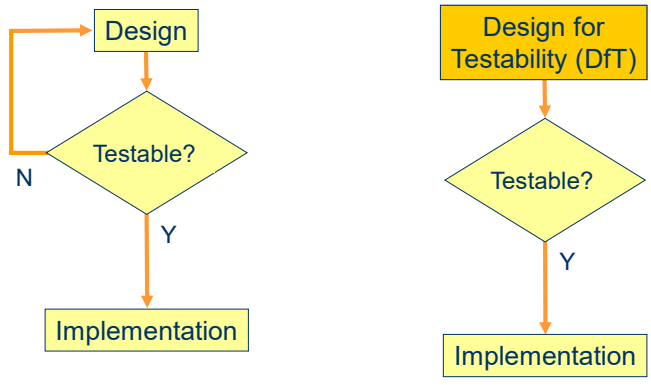
Design for Testability



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Testability

The property of a circuit that makes it easy to test

Design engineer

Complexity of Test Pattern Generation (TPG)

Quality engineer

Fault coverage and escape rates

Test engineer

Compatibility of the design with the test equipment

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Test Costs

- **Test Preparation**
  - Test generation
  - Fault simulation
- **Test Application**
  - Test programming and debug
  - ATE cost
  - ATE operational cost
- **Design for Testability**
  - Design flow overhead
  - Product overhead: silicon area, performance degradation, increased pin count

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Test Application Costs

- ATE purchase price
  0.5 to 1.0 GHz analog instruments and 1,024 digital pins
  = \$1.2M + 1,024 x \$3,000 = \$4.272M
- Running cost (five-year linear depreciation)
  Depreciation + Maintenance + Operation
  = \$0.854M + \$0.085M + \$0.5M = \$1.439M/year
- Test cost (24 hour ATE operation)
  = \$1.439M/(365 x 24 x 3,600)
  = 4.5 cents/second

Test length is critical !

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Defective Products Screening

Ideal

- Yield=1 (zero defects), manufacturing is perfect
- If not, test detects all defects induced during manufacturing

Real

- Yield<1, manufacturing is **not** perfect
- Real test is based on fault models, which cannot accurately describe all likely defects induced during manufacturing

Yield: Percentage of manufactured devices that are defect-free

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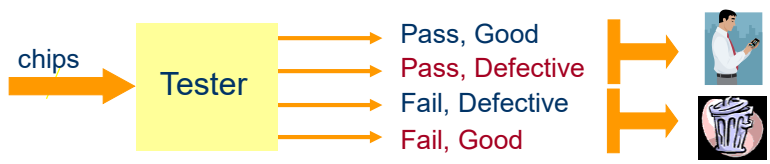
Hardware Test Problem



Pass, Defective: impact on the user side

Field rejections have impact on reputation ⇒ loss of market share

Fail, Good: impact on the manufacturer side

Yield Loss ⇒ higher production cost ⇒ lower profit margin

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Quality Metrics

Product quality → Defect Level

Percentage (or ppm, parts per million) of defective devices which pass the production test (marketed as good)

Test quality → Fault Coverage

Percentage of modeled faults that are uncovered by the production test

Manufacturing quality → Production Yield

Percentage of manufactured devices that are defect-free

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Quality Metrics: Yield (Y)

From the IC designer's point of view, production yield depends mainly on:

- Defect density (**D**)
- Die area (**A**)

$$Y = e^{-\sqrt{A.D}}$$ Seeds model

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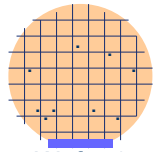
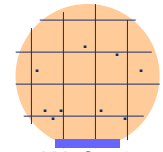
Yield as a Function of the Die Area



Wafer 1

Area circuit 1 < Area circuit 2

$Yield_1 > Yield_2$



Wafer 2

Assuming a random spot defects density …

A larger die area, A, increases the probability of a given die being defective

Yield: Questions

Question 1:

Assume a process line with D = 0.5 defects/cm^2.

What will be the expected yield of a product with a die area of (a) A1 = 0.1 cm^2? (b) A2 = 1 cm^2?

What would be the probability of manufacturing a 4” (inch) wafer without defects? and a 12” wafer?

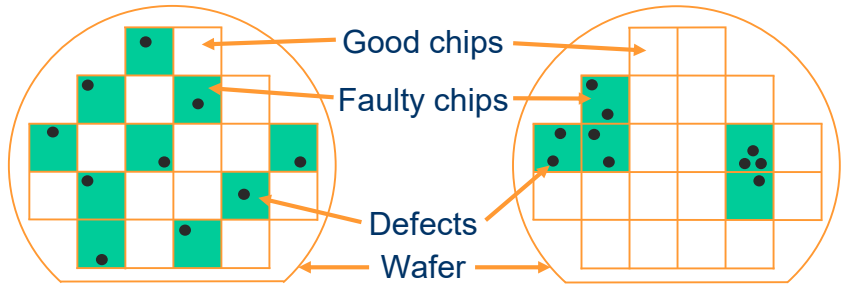
Question 2:

What would be the required defects density for a given process line, to manufacture 1 cm^2 dies with 85% Yield? How many good chips would we get from a 12” wafer?

Yield: Clustered Defects

$Y = e^{-\sqrt{A.D}}$

For a given die area (A), the yield may more accurately depend on two process parameters, defect density (D), and a clustering parameter (α).



Random defects
Yield = 12/22 = 55 %

Clustered defects
Yield = 17/22 = 77 %

Same defect density and same area, but different yields

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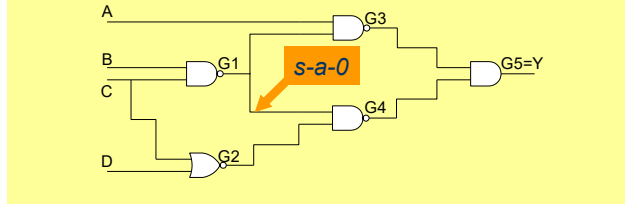
Quality Metrics: Fault Coverage (FC)

Fault coverage depends on

1. the fault model
2. the test patterns

$FC = \#F_{detected} / \#F_{total}$

Typical fault model for digital designs: Stuck-At (SA)



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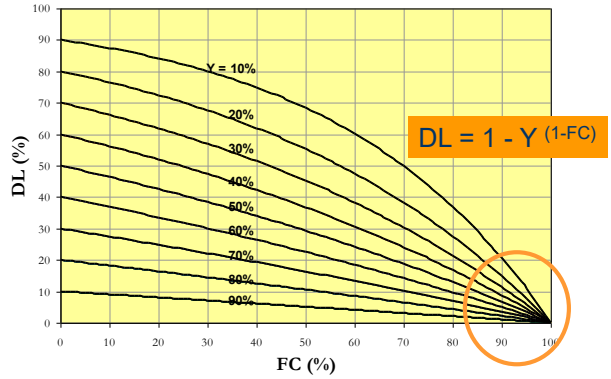
Quality Metrics: Defect Level (DL)

$DL = 1 - Y^{(1-FC)}$ Williams and Brown model



Low DL ⇒ high Y and very high FC

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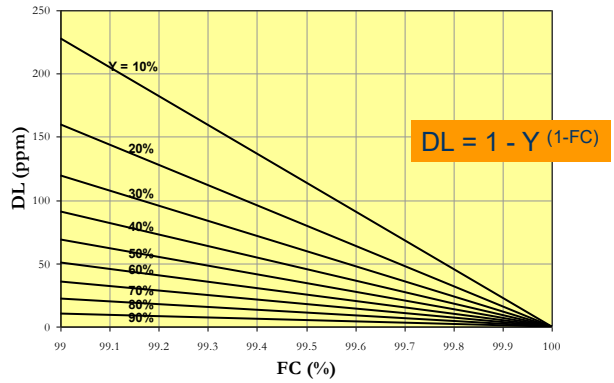
How effective must the test be?



For DL = 50 ppm and Y = 60%, FC must reach 99%

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Test Phases

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Test Planning

- **Test specifications**
  - Physical constraints – package, pin numbers, etc.
  - Environmental characteristics – supply voltage, temperature, humidity, etc.
  - Quality and Reliability – acceptance quality level (DL), failure rate, etc.
  - Functional characteristics per DUT – what DfT technique
- **Test plan generated from specifications**
  - Type(s) of ATE to be used
  - Types of tests
  - Fault coverage requirement

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Test Preparation

- **Test hardware synthesis**
  - Generation of specific test structures
  - Analysis of test overhead (trade-off analysis)
- **Test generation and validation**
  - Automatic Test Pattern Generation
  - Fault simulation
  - Fault coverage evaluation
- **Test program generation**

Test Application

- **Target ATE**
  - Wafer probe
  - Final test
  - Test fixture and pin electronics