

Arash Fouman

CONTACT INFORMATION	Email: arashfouman@gmail.com afouman.github.io Skype ID: Arash.Fouman Phone: (+98) 912 564 41 49																																									
RESEARCH INTERESTS	Embedded Systems, Implantable Systems, Digital Health Care System Design, Approximate Computing, Low-Power Design, Neural Networks																																									
EDUCATION	University of Tehran , Tehran, Iran B.S., Electrical and Computer Engineering, <i>Expected: 2016</i> <ul style="list-style-type: none">• Thesis Topic: <i>FPGA Realization of Better than Worst-Case Design Techniques in Pipeline Processors</i>• Advisor: Z. Navabi, Ph.D Relative Courses: <table><tr><td>Mathematics1:</td><td>18.75/20(4/4)</td><td>Advanced Programming:</td><td>16.5/20(4/4)</td></tr><tr><td>Mathematics2:</td><td>16/20(4/4)</td><td>Signals & Systems:</td><td>16.3/20(4/4)</td></tr><tr><td>Ordinary Differential Equations:</td><td>17/20(4/4)</td><td>Filter & Circuit Synthesis:</td><td>16/20(4/4)</td></tr><tr><td>Digital Logic Design:</td><td>17.1/20(4/4)</td><td>Computer Architecture:</td><td>17.6/20(4/4)</td></tr><tr><td>D.L.D. Lab:</td><td>19.5/20(4/4)</td><td>C.A. Lab:</td><td>18.25/20(4/4)</td></tr><tr><td>Electronics I:</td><td>17/20(4/4)</td><td>Microprocessors:</td><td>17/20(4/4)</td></tr><tr><td>Electronics Lab I:</td><td>18/20(4/4)</td><td>Microprocessors Lab:</td><td>17/20(4/4)</td></tr><tr><td>Electronics Lab II:</td><td>18.25/20(4/4)</td><td>HW/SW Codesign:</td><td>15.5/20(3/4)</td></tr><tr><td>VLSI:</td><td>16/20(4/4)</td><td>Computer Workshop:</td><td>18.75/20(4/4)</td></tr><tr><td>VLSI & Digital Electronics Lab:</td><td>19.5/20(4/4)</td><td></td><td></td></tr></table> <ul style="list-style-type: none">• Overall GPA = 15.12/20(Equivalent to B) [with School Average = 13.82/20]• GPA of Relative Courses = 17.01/20 (Equivalent to A) Danesh High School , Tehran, Iran High school Diploma., Mathematics and Physics, 2012 GPA = 19.27 /20 or 4/4		Mathematics1:	18.75 /20(4/4)	Advanced Programming:	16.5 /20(4/4)	Mathematics2:	16 /20(4/4)	Signals & Systems:	16.3 /20(4/4)	Ordinary Differential Equations:	17 /20(4/4)	Filter & Circuit Synthesis:	16 /20(4/4)	Digital Logic Design:	17.1 /20(4/4)	Computer Architecture:	17.6 /20(4/4)	D.L.D. Lab:	19.5 /20(4/4)	C.A. Lab:	18.25 /20(4/4)	Electronics I:	17 /20(4/4)	Microprocessors:	17 /20(4/4)	Electronics Lab I:	18 /20(4/4)	Microprocessors Lab:	17 /20(4/4)	Electronics Lab II:	18.25 /20(4/4)	HW/SW Codesign:	15.5 /20(3/4)	VLSI:	16 /20(4/4)	Computer Workshop:	18.75 /20(4/4)	VLSI & Digital Electronics Lab:	19.5 /20(4/4)		
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LANGUAGES	<ul style="list-style-type: none">• Persian(Farsi): Native proficiency• English: Professional working proficiency <i>test scores are to be announced</i>• Azerbaijani: Familiar																																									
RESEARCH EXPERIENCE	Research Assistant June 2016 to present ESL Tools & Methodologies Laboratory , University of Tehran Supervisor: Z. Navabi , Ph.D Research Assistant March 2015 to June 2016 Silicon Intelligence Laboratory , University of Tehran Supervisors: Sied M. Fakhraie , Ph.D and M. E. Salehi Nasab , Ph.D																																									
REFEREED PUBLICATIONS	1. Hashemi,H., Fouman, A. , Soltani, M., Navabi, Z., “Early Prediction of Timing Critical Instructions in Pipeline Processor.” <i>Baltic Electronics Conference</i> , 2016.																																									
SUBMITTED PUBLICATIONS	1. <i>Under Construction</i>																																									

PAPERS IN PREPARATION	<ol style="list-style-type: none"> 1. Moghaddas, I., Fouman, A., E. Salehi Nasab, M., Kargahi, M. “Fine-Grained Aging Rate Prediction for Embedded Cores Using Instruction-Level Stress Monitoring.” 2. Fouman, A., Navabi, Z., “A Low-Power and Low-Area Overhead Technique toward On-line Timing Error Resilience.” 	
AWARDS	<ul style="list-style-type: none"> • Nomination for membership of National Elites Foundation 2016 {<i>Still Under Study</i> } • Semi-Finalist in National Olympiad in <i>Mathematics</i> at Young Scholars Club. Mar. 2011 • Graduated in high school Summa Cum Laude Sep. 2012 	
TEACHING EXPERIENCE	<p>Teaching Assistant Falls 2014–15 & Spring 2015 & Fall 2016 Electronics I Instructor: Z. Sanaee, Ph.D</p> <p>Teaching Assistant Springs 2015–16 & Fall 2016 Electronics Lab I Instructor: H. Khodkari, M.S.</p> <p>Teaching Assistant Fall 2016 Digital Logic Design Lab Instructor: Z. Navabi, Ph.D</p> <p>Teaching Assistant Fall 2016 Electronics II Instructor: A. Afzali-Kusha, Ph.D</p> <p>Teaching Assistant Fall 2016 Hardware/Software Co-design Instructor: M. E. Salehi Nasab, Ph.D</p> <p>Teaching Assistant Fall 2016 Computer Architecture & Computer Architecture Lab Instructor: S. Safari, Ph.D</p> <p>Teaching Assistant Fall 2016 Digital Electronic Circuits Instructor: M. Kamal, Ph.D</p> <p>Teaching Assistant Spring 2016 Electronics Lab II Instructor: M. Kolahdouz, Ph.D</p> <p>Teaching Assistant Spring 2016 Electronics I Instructor: M. Kolahdouz, Ph.D</p> <p>Teaching Assistant Spring 2015 Ordinary Differential Equations Instructor: P. Nasehpour, Ph.D</p> <p>Teaching Assistant Fall 2014 Mathematics I Instructor: Committee of Mathematics, Faculty of Engineering</p> <p>Grading TA Fall 2014 Digital Logic Design Instructor: Z. Navabi, Ph.D</p>	
INTERNSHIP	Design & Revision of the experiments of Digital Logic Laboratory Supervisor: Z. Navabi, Ph.D Division of Digital Systems, University of Tehran	Summer 2015

HARDWARE AND SOFTWARE SKILLS	Computer Programming:
	<ul style="list-style-type: none"> • <i>Expert</i> in: Verilog, Hspice, C, C++, UNIX shell scripting, MATLAB • <i>Familiar</i> with: GNU make, L^AT_EX, VHDL
	Tools & OS:
	<ul style="list-style-type: none"> • <i>Expert</i> in: Altera Quartus II, Altera Modelsim, Pspice • <i>Familiar</i> with: OS X, Linux, Design Compiler, LabView
	Skills:
	<ul style="list-style-type: none"> • <i>Expert</i> in: Debugging, Electronics, Digital Logic Design, FPGA, AVR • <i>Familiar</i> with: Nios II, ARM
NOTABLE PROJECTS	Set-up of a fully functional SDRAM Controller
	<ul style="list-style-type: none"> • using <i>verilog HDL</i> and implemented on Altera DE-2 <i>Cyclone IV</i> FPGA board
	Implementation of a fully synthesizable pipelined MIPS processor
	<ul style="list-style-type: none"> • using <i>verilog HDL</i> and implemented on Altera DE-2 <i>Cyclone II</i> FPGA board
	Digital Oscilloscope
	<ul style="list-style-type: none"> • using <i>verilog HDL</i> and implemented on FPGA board
	Digital Electrocardiography Device
	<ul style="list-style-type: none"> • using <i>verilog HDL</i> and implemented on FPGA board
	Digital Plants Word System
	<ul style="list-style-type: none"> • using <i>verilog HDL</i> and implemented on FPGA board
CERTIFICATES	Digital Voltmeter
	<ul style="list-style-type: none"> • using <i>verilog HDL</i> and implemented on FPGA board
	Smart Plants irrigation System
	<ul style="list-style-type: none"> • using <i>AVR Micro-Controller</i> and <i>Android</i> platform
	Line Follower Robot
	<ul style="list-style-type: none"> • using <i>AVR Micro-Controller</i> , <i>C programming language</i>, and designing a <i>Printed Circuit Board (PCB)</i>
	<ul style="list-style-type: none"> • Application of Mathematical Models in Biology and Cancer, Cancer Modelling Research Center(CMRC), Tehran University of Medical Sciences Dec. 2014
	<ul style="list-style-type: none"> • Industrial Automation System –PLC Controllers training course, Negar Sanat Co, Iran Aug. 2014
	<ul style="list-style-type: none"> • AVR Micro Controllers training course, IEEE Student Branch of University of Tehran Oct. 2013
SERVICES	Alumni Association of Faculty of Engineering, University of Tehran
	<ul style="list-style-type: none"> • Assist with holding the annual “50th graduation anniversary” of former alumni • Assist with holding the 80th anniversary of the enactment of constitution of University of Tehran
	How to Apply, IEEE Student Branch, University of Tehran
	<ul style="list-style-type: none"> • Assist with holding of annual How To Apply talks
	University of Tehran Open Day
	<ul style="list-style-type: none"> • Assist with holding of annual Open Day and Admitted Student Visit Days • Meet with prospective and admitted students
SPORTS AND HOBBIES	Soccer, Swimming, Biking, Basketball, TV Series, Cooking
ACTIVITIES AND SOCIETIES	<ul style="list-style-type: none"> • IEEE Student Member, IEEE International Mar. 2015 – Present • Iranian National Student-Scientific Organization of Electrical Engineering 2014 – 2015
REFERENCES	<i>Available upon Request</i>