CSCE311 Spring, 2017 Home Work Due: 4/04/17

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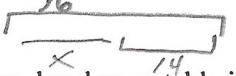
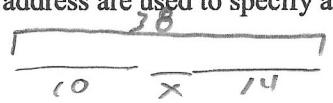
1. Consider a 64-bit architecture machine where physical memory is 32GB. 1 2 4 6 8 16 32 64 128
   a. If we would like to run processes as big as 128GB how many bits would be required for the logical address? $1\,GB = 2^{30}$ $128\,GB = 2^{38}$ 38 bits
   b. If we are using pages of size 16KB, how many bits are needed for displacement into a page? $16\,KB = 2^{14}\,B$ 14 bits
   c. If a single level page table is used, what is the maximum number of entries in this table? total 38 bits − page size 14 bits = 24 2^{24} entries
   d. What is the size of this single level page table in terms of 16KB pages? 2B 4B or 8B? 4B will hold
      

      $(2^{26} \times 2^2) / 2^{14} =$ 2^{14} pages
   e. If a two-level page-table is used and the outer page table is an 16KB page, how many entries does it contain, maximally?
      $16\,KB = 2^{14} / 2^4 =$ 2^{10} entries
   f. How many bits of the logical address are used to specify an index into the inner page (page of page table)?
      

      38 − 10 − 14 = 14 bits

2. Consider a paging system where the page table is stored in the translation look aside buffer (TLB). The hit ratio is 95% meaning the page table entry will be found in TLB 95% of the time. The normal memory access time is t = 2.0 microseconds whereas TLB access is 0.4 microseconds.
   $EAT = (1+\epsilon)\,\alpha + (2+\epsilon)(1-\alpha)$
   a. When calculating the effective paged memory access time, why is the cost of a TLB miss the sum of TLB access time plus normal memory access time?
      the cost of a miss is access time plus normal memory access time because a miss will require both to provide correct info
   b. If we consider only swap-in/swap-out time and if swap-in-time 20 milliseconds and swap-out-time = 18 milliseconds, and, on the average, 80% of the pages are dirty, what is the effective page fault service time?
      $0.8\,(20 + 18) = 30.4\,ms$