

The Mediatek logo, consisting of the word "MEDIATEK" in a bold, sans-serif font, is contained within a white, parallelogram-shaped box with a slight 3D effect.

MEDIATEK

MT7986 Smart Carrier Sensing

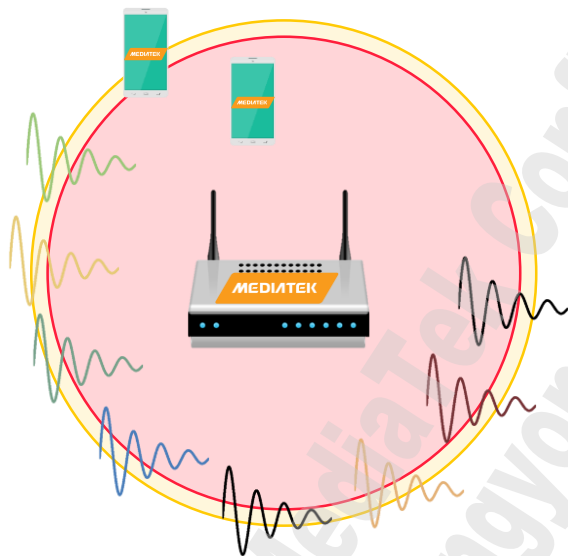
2021/09/24

Outline

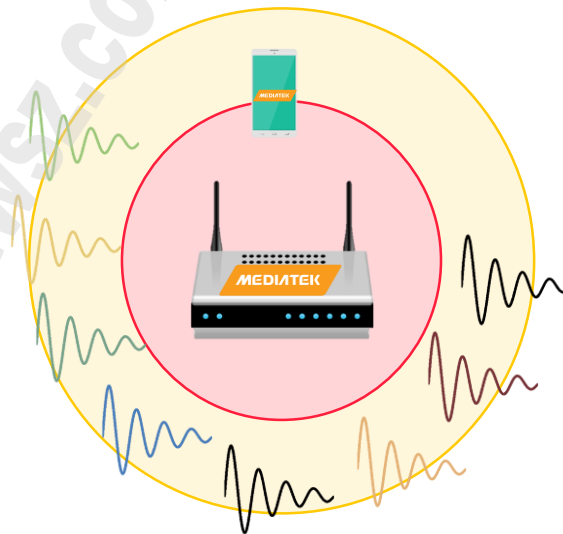
- **Introduction**
- **Motivation**
- **Smart Carrier Sense Concept**
- **Limitation**
- **Command**

Introduction

- Improve **2.4G/5G** OTA/Noisy Throughput Performance



If there are long range/short range STA → keep good Rx sensitivity



If there are only short range STA → adjust Rx range to ignore legal wifi packet and ACI/CCI → Increase Tx opportunities

IEEE CSCCA Spec

- IEEE802.11a: OFDM CSCCA spec is **-82dBm**, EDCCA spec is -62dBm

17.3.10.5 CCA sensitivity

The start of a valid OFDM transmission at a receive level equal to or greater than the minimum 6 Mbit/s sensitivity **(-82 dBm)** shall cause CCA to indicate busy with a probability >90% within 4 μ s. If the preamble portion was missed, the receiver shall hold the carrier sense (CS) signal busy for any signal 20 dB above the minimum 6 Mbit/s sensitivity (-62 dBm).

- IEEE802.11: define CS function and CCK 2M sensitivity = **-80dBm**

15.4.8.1 Receiver minimum input level sensitivity

The frame error ratio (FER) shall be less than 8×10^{-2} at an MPDU length of 1024 bytes for an input level of **-80 dBm** measured at the antenna connector. This FER shall be specified for 2 Mbit/s DQPSK modulation. The test for the minimum input level sensitivity shall be conducted with the energy detection threshold set ≤ -80 dBm.

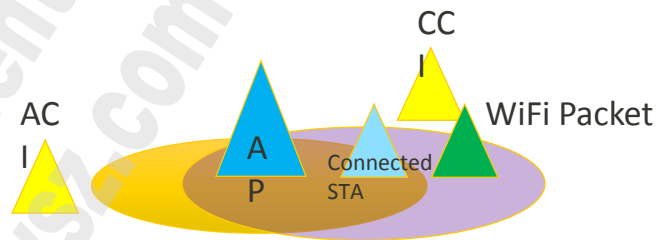
Table 91—Receiver performance requirements

Data rate (Mbits/s)	Minimum sensitivity (dBm)	Adjacent channel rejection (dB)	Alternate channel rejection (dB)
6	-82	16	
9	-81	15	
12	-79	13	
18	-77	11	
24	-74	8	
36	-70	4	

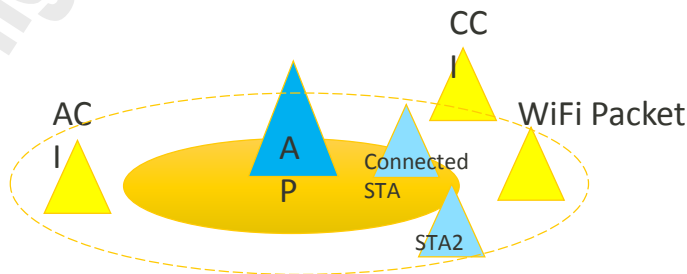
- Thus IEEE defined CCK/OFDM CS sensitivity
 - CCK 2M: **-80dBm**
 - OFDM 6M: **-82dBm**

Limitation

- **Hidden node close to STA.**

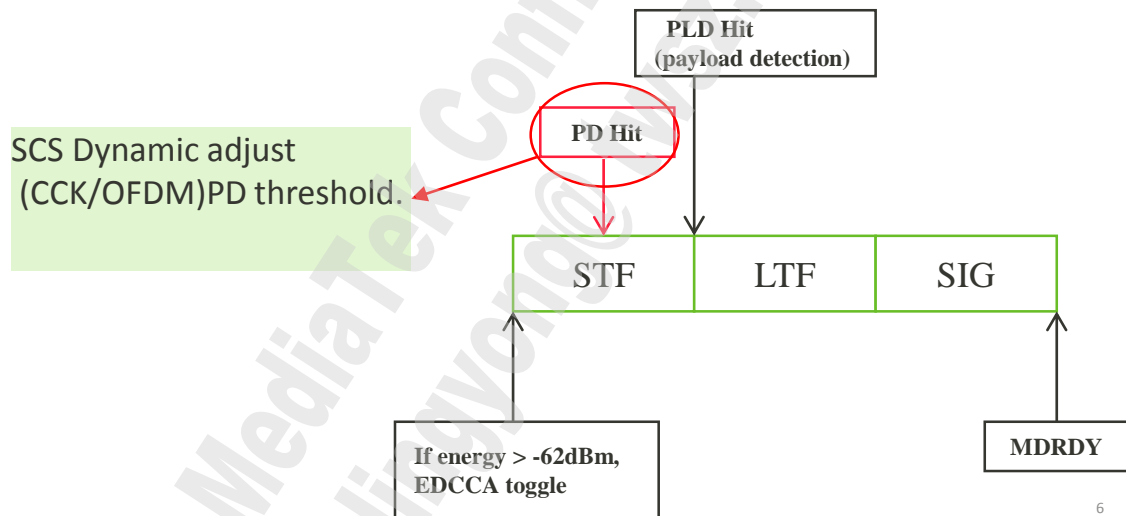


- **Far STA can't connect to AP during PD blocking enabled.**



Smart Carrier Sense Mechanism

- Mechanism
 - PD blocking threshold.



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MT7986 Smart Carrier Sense

- **Alpha Branch MP version only supports SCS on Band0**
- **MT7986 SCS Characteristics**
 - **Entry Condition: Channel congestion, Low TX airtime and traffic Busy**
 - Only Activated when there's only 1 active station (with throughput)
 - **Measurement Indicators: Effective throughput**
 - **Activated in Channel busy condition (both ACI and CCI Scenario)**
 - **Adjust Pd by monitoring effective throughput**

Driver Config

- **Must Enable Configuration in driver:**

COFIG	Note	Path
SMART_CARRIER_SENSE_SUPPORT	Kconfig	Eg. Jedi/os/linux/Kconfig.mt_wifi_4_4 Jedi/os/linux/Kconfig.mt_wifi_3_18 Jedi/os/linux/Kconfig.mt_wifi
CONFIG_MTK_SCS_FW_OFFLOAD	SDK menuconfig	Eg: lede/autobuild/mt7621-mt7986-AX6000/.config

MT7986 CR for PD Threshold

- PD_BLK_TH Band0:

CR address	LSB MSB	Description		
830A611C	1 8	CCK	CR_CCK_PD_SEN_LIMITED	Formula : Value + 256
830A6120	24 31	CCK 1R	CR_CCK_PD_SEN_LIMITED_1R	ex: -70 + 256 = 186 (0xBA)
830884f0	20 28	OFDM	CR_BAND0_MIN_PRI_PWR_DBM	Formula : Value*2 + 512
830884f0	19 19	OFDM enable	CR_BAND0_MIN_PRI_PWR_EN	ex: -70*2 + 512 = 374 (0x174)

- PD_BLK_TH Band1:

CR address	LSB MSB	Description		
831A611C	1 8	CCK	CR_CCK_PD_SEN_LIMITED	Formula : Value + 256
831A6120	24 31	CCK 1R	CR_CCK_PD_SEN_LIMITED_1R	ex: -70 + 256 = 186 (0xBA)
831884f0	20 28	OFDM	CR_BAND0_MIN_PRI_PWR_DBM	Formula : Value*2 + 512
831884f0	19 19	OFDM enable	CR_BAND0_MIN_PRI_PWR_EN	ex: -70*2 + 512 = 374 (0x174)

- Default Pd Threshold

- Default_PD_Upper_Bound = -72dBm
- Default_PD_Lower_Bound = -110dBm

SCS Command

- **SCS enable for Band0 :**
 - **iwpriv ra0 set SCSEnable=0/1 (Disable/Enable Default Enable)**
- **SCS enable for Band1 :**
 - **iwpriv rax0 set SCSEnable=0/1 (Disable/Enable)**
- **SCS log enable**
 - **iwpriv ra0 set SCSEnable=2 | iwpriv ra0 set fwlog=0:3**

SCS Command (for Debug) – 1/2

- Dump SCS status every 0.5 sec

- iwpriv ra0 set fwlog=0:2

```

Band0: Busy/OBSS/MyT/MyR 638113/789457/89010/10845, Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 316/146, IniT 0, CurT 0, LstT 0, D
175, flush one!
12ba, flush one!
Band0: Busy/OBSS/MyT/MyR 607977/750250/104413/18067 Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 316/146, IniT 0, CurT 0, LstT 0, D
Band0: Busy/OBSS/MyT/MyR 612506/728153/139159/15267 Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 316/146, IniT 0, CurT 0, LstT 0, D
Band0: TputDiff is too large !
Band0: Busy/OBSS/MyT/MyR 604787/714662/154140/18392 Rst/ChBusy/ActSta 1/0/1, OFDM/CCK 316/146, IniT 0, CurT 0, LstT 59,
Jca0, flush one!
Band0: Busy/OBSS/MyT/MyR 558169/552572/275809/51012 Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 316/146, IniT 0, CurT 0, LstT 0, D
Band0: Busy/OBSS/MyT/MyR 524100/478933/342894/74819 Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 316/146, IniT 0, CurT 0, LstT 0, D
Jc31, flush one!
Band0: Busy/OBSS/MyT/MyR 455568/386720/419835/69828 Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 316/146, IniT 0, CurT 0, LstT 0, D
Band0: Busy/OBSS/MyT/MyR 383322/296998/558962/93560 Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 322/161, IniT 189, CurT 0, LstT 18
Band0: Busy/OBSS/MyT/MyR 344481/261366/617376/82323 Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 322/161, IniT 189, CurT 0, LstT 0,
Band0: Busy/OBSS/MyT/MyR 423256/362316/522038/70414 Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 322/161, IniT 189, CurT 0, LstT 0,
Band0: CurAvgTput >= IniAvgTput*1.1, Keep PD, Reset e tput monitor period!!
Band0: Busy/OBSS/MyT/MyR 388314/336500/545572/66005 Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 322/161, IniT 189, CurT 605, LstT
Band0: Busy/OBSS/MyT/MyR 375488/320187/576271/65952 Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 322/161, IniT 189, CurT 0, LstT 0,
0]Band0: Busy/OBSS/MyT/MyR 373307/335501/563182/562 9, Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 322/161, IniT 189, CurT 0, LstT
Band0: TputDiff is too large !
Band0: Busy/OBSS/MyT/MyR 328679/280290/617455/60271 Rst/ChBusy/ActSta 1/0/1, OFDM/CCK 316/146, IniT 0, CurT 0, LstT 682,
Band0: Busy/OBSS/MyT/MyR 372550/311869/579135/61213 Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 316/146, IniT 0, CurT 0, LstT 0, D
0]Band0: Busy/OBSS/MyT/MyR 359794/320443/575352/604 2, Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 316/146, IniT 0, CurT 0, LstT 0,
Band0: Busy/OBSS/MyT/MyR 387359/345920/534177/67024 Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 316/146, IniT 0, CurT 0, LstT 0, D
Band0: Busy/OBSS/MyT/MyR 599876/746760/129480/7671 Rst/ChBusy/ActSta 0/1/1, OFDM/CCK 368/184, IniT 766, CurT 0, LstT 766
Band0: ActiveSTA is 0 which is not equal to 1

```

PDRreset Flag
 ChanBusyFlag
 ActiveSTA number

OFDM Pd Threshold
 CCK Pd Threshold

SCS Command (for Debug) – 2/2

• Dump all SCS Related Variables in Firmware:

- Step1 : Fetch address of FW global data structure
 - iwpriv ra0 show get_scs_glo_addr

```

root@PLEDE:/# Get address of global data structure
root@PLEDE:/# iwpriv ra0 show get_scs_glo_addr
[ 368.869881] ShowScsGloAddr:
[ 368.872688] scsEventDispatcher: u4EventId = 6, len = 24
[ 368.878828] scsEventDispatcher: SCS_EVENT_GET_GLO_ADDR
[ 368.883161] scs_get_glo_addr_handler:SCS_EVENT_GET_GLO_ADDR
[ 368.888728] eventId 6
[ 368.891064] ShowScsGloAddr:(Ret = 1)

```

- Step 2: Dump data via address (both for Band0 and Band1)
 - iwpriv ra0 show SCSInfo_2

```

root@PLEDE:/# iwpriv ra0 show SCSInfo_2
[ 443.584417] ===== Band 0 Information =====
[ 443.590166] scsBand0 (0x16003D80)
[ 443.592783] 1-(0xEM003D80) u1SCSwaRssi = 0
[ 443.598183] 1-(0xEM003D8C) u4OneSecRxByteCount = 0
[ 443.603168] 1-(0xEM003D90) u4OneSecRxByteCount = 0
[ 443.608146] 1-(0xEM003D94) u2CnAPB1k1kth = 146
[ 443.612677] 1-(0xEM003D96) u2OfdmPdB1k1kth = 316
[ 443.617211] 1-(0xEM003D98) u2SCSMinRssiTolerance = 5
[ 443.622457] 1-(0xEM003D9D) u2CnAPFixedRssiThresh = 194
[ 443.627232] 1-(0xEM003D9E) u2OfdmFixedRssiThresh = 368
[ 443.632648] 1-(0xEM003D9E) u2IntrusgInput
[ 443.636617] 1-(0xEM003D9E) u2IntrusgInput[0] = 0
[ 443.641452] 1-(0xEM003D9C) u2IntrusgInput[1] = 0
[ 443.646253] 1-(0xEM003D9C) u2IntrusgInput[2] = 0
[ 443.651051] 1-(0xEM003D94) u2IntrusgInput[3] = 0
[ 443.655844] 1-(0xEM003D95) u2LastInputDiff
[ 443.660143] 1-(0xEM003D9C) u2LastInputDiff[0] = 0
[ 443.665115] 1-(0xEM003D9C) u2LastInputDiff[1] = 0
[ 443.670085] 1-(0xEM003D9C) u2LastInputDiff[2] = 0
[ 443.675054] 1-(0xEM003D9C) u2LastInputDiff[3] = 0
[ 443.680040] 1-(0xEM003D9C) u2LastAvgInput
[ 443.684176] 1-(0xEM003D9C) u2LastAvgInput[0] = 0
[ 443.689088] 1-(0xEM003D9D) u2LastAvgInput[1] = 0
[ 443.693974] 1-(0xEM003D9D) u2LastAvgInput[2] = 0
[ 443.698857] 1-(0xEM003D9D) u2LastAvgInput[3] = 0
[ 443.703732] 1-(0xEM003D95) u2LastMaxInput
[ 443.707423] 1-(0xEM003D96) u2LastMaxInput[0] = 0
[ 443.712161] 1-(0xEM003D96) u2LastMaxInput[1] = 0
[ 443.717597] 1-(0xEM003D96) u2LastMaxInput[2] = 0
[ 443.722314] 1-(0xEM003D96) u2LastMaxInput[3] = 0
[ 443.727291] 1-(0xEM003D9E) u2LastMinInput
[ 443.731492] 1-(0xEM003D9D) u2LastMinInput[0] = 255
[ 443.736438] 1-(0xEM003D9D) u2LastMinInput[1] = 255
[ 443.741684] 1-(0xEM003D9D) u2LastMinInput[2] = 255
[ 443.746668] 1-(0xEM003D94) u2LastMinInput[3] = 255
[ 443.751708] 1-(0xEM003D96) u1LastInputIdx
[ 443.755888] 1-(0xEM003D96) u1LastInputIdx[0] = 0
[ 443.760748] 1-(0xEM003D97) u1LastInputIdx[1] = 0
[ 443.765623] 1-(0xEM003D98) u1LastInputIdx[2] = 0
[ 443.770507] 1-(0xEM003D98) u1LastInputIdx[3] = 0
[ 443.775382] 1-(0xEM003D9A) fgLastInputDone
[ 443.779569] 1-(0xEM003D9A) fgLastInputDone[0] = 0
[ 443.784538] 1-(0xEM003D9B) fgLastInputDone[1] = 0
[ 443.789507] 1-(0xEM003D9C) fgLastInputDone[2] = 0
[ 443.794476] 1-(0xEM003D9D) fgLastInputDone[3] = 0
[ 443.799463] 1-(0xEM003D9E) u2CurAvgInput
[ 443.803478] 1-(0xEM003D9E) u2CurAvgInput[0] = 0
[ 443.808274] 1-(0xEM003D9E) u2CurAvgInput[1] = 0
[ 443.813071] 1-(0xEM003D9E) u2CurAvgInput[2] = 0
[ 443.817857] 1-(0xEM003D9E) u2CurAvgInput[3] = 0
[ 443.822659] 1-(0xEM003D96) u1CurInputIdx
[ 443.826673] 1-(0xEM003D96) u1CurInputIdx[0] = 0
[ 443.831494] 1-(0xEM003D97) u1CurInputIdx[1] = 0
[ 443.836298] 1-(0xEM003D98) u1CurInputIdx[2] = 0
[ 443.841088] 1-(0xEM003D99) u1CurInputIdx[3] = 0
[ 443.845874] 1-(0xEM003D9A) u1InputPeriodScaleBit
[ 443.850684] 1-(0xEM003D9B) u1InputPeriodScaleBit[0] = 1
[ 443.855473] 1-(0xEM003D9B) u1InputPeriodScaleBit[1] = 1
[ 443.861581] 1-(0xEM003D9C) u1InputPeriodScaleBit[2] = 1
[ 443.867071] 1-(0xEM003D9D) u1InputPeriodScaleBit[3] = 1
[ 443.872561] 1-(0xEM003D9E) u1ChannelBusy = 80
[ 443.877278] 1-(0xEM003D9F) fgChBusy = 0
[ 443.881311] 1-(0xEM003E00) u1MxTxRt = 70
[ 443.885624] 1-(0xEM003E01) fgPreset = 0
[ 443.889727] 1-(0xEM003E02) u4ChannelBusyTime = 0
[ 443.894521] 1-(0xEM003E03) u4MxTxRtTime = 0
[ 443.898988] 1-(0xEM003E0C) u4MxTxRtTime = 0
[ 443.903472] 1-(0xEM003E10) u4SCSMinRssi = 0
[ 443.908434] ===== Band 1 Information =====
[ 443.914086] scsBand1 (0x16003D14)
[ 443.917597] 1-(0xEM003E15) u1SCSMinRssi = 0

```

```

[ 443.751708] 1-(0xEM003D96) u1LastInputIdx
[ 443.755888] 1-(0xEM003D96) u1LastInputIdx[0] = 0
[ 443.760748] 1-(0xEM003D97) u1LastInputIdx[1] = 0
[ 443.765623] 1-(0xEM003D98) u1LastInputIdx[2] = 0
[ 443.770507] 1-(0xEM003D98) u1LastInputIdx[3] = 0
[ 443.775382] 1-(0xEM003D9A) fgLastInputDone
[ 443.779569] 1-(0xEM003D9A) fgLastInputDone[0] = 0
[ 443.784538] 1-(0xEM003D9B) fgLastInputDone[1] = 0
[ 443.789507] 1-(0xEM003D9C) fgLastInputDone[2] = 0
[ 443.794476] 1-(0xEM003D9D) fgLastInputDone[3] = 0
[ 443.799463] 1-(0xEM003D9E) u2CurAvgInput
[ 443.803478] 1-(0xEM003D9E) u2CurAvgInput[0] = 0
[ 443.808274] 1-(0xEM003D9E) u2CurAvgInput[1] = 0
[ 443.813071] 1-(0xEM003D9E) u2CurAvgInput[2] = 0
[ 443.817857] 1-(0xEM003D9E) u2CurAvgInput[3] = 0
[ 443.822659] 1-(0xEM003D96) u1CurInputIdx
[ 443.826673] 1-(0xEM003D96) u1CurInputIdx[0] = 0
[ 443.831494] 1-(0xEM003D97) u1CurInputIdx[1] = 0
[ 443.836298] 1-(0xEM003D98) u1CurInputIdx[2] = 0
[ 443.841088] 1-(0xEM003D99) u1CurInputIdx[3] = 0
[ 443.845874] 1-(0xEM003D9A) u1InputPeriodScaleBit
[ 443.850684] 1-(0xEM003D9B) u1InputPeriodScaleBit[0] = 1
[ 443.855473] 1-(0xEM003D9B) u1InputPeriodScaleBit[1] = 1
[ 443.861581] 1-(0xEM003D9C) u1InputPeriodScaleBit[2] = 1
[ 443.867071] 1-(0xEM003D9D) u1InputPeriodScaleBit[3] = 1
[ 443.872561] 1-(0xEM003D9E) u1ChannelBusy = 80
[ 443.877278] 1-(0xEM003D9F) fgChBusy = 0
[ 443.881311] 1-(0xEM003E00) u1MxTxRt = 70
[ 443.885624] 1-(0xEM003E01) fgPreset = 0
[ 443.889727] 1-(0xEM003E02) u4ChannelBusyTime = 0
[ 443.894521] 1-(0xEM003E03) u4MxTxRtTime = 0
[ 443.898988] 1-(0xEM003E0C) u4MxTxRtTime = 0
[ 443.903472] 1-(0xEM003E10) u4SCSMinRssi = 0
[ 443.908434] ===== Band 1 Information =====
[ 443.914086] scsBand1 (0x16003D14)
[ 443.917597] 1-(0xEM003E15) u1SCSMinRssi = 0

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