

## CS 6354: Graduate Computer Architecture

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### Cache design space exploration

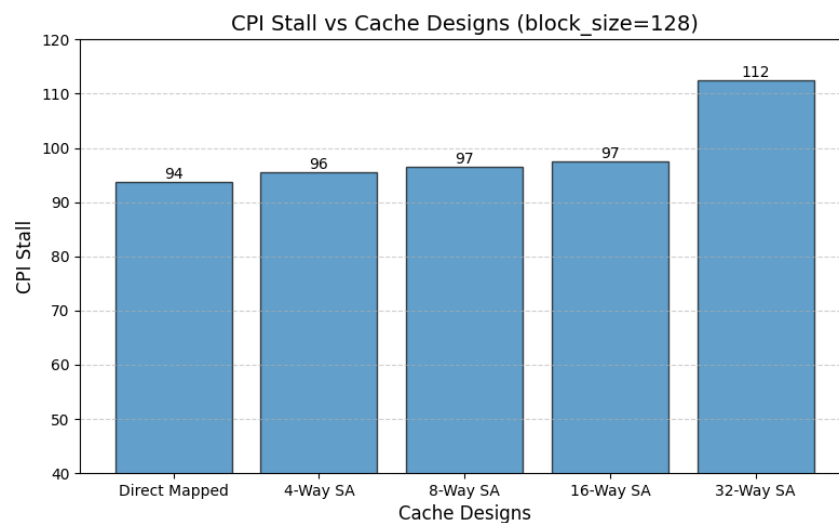
Keeping the cache size constant (16KB), In terms of associativity, we explore 1-way (direct-mapped), 4-way, 8-way, 16-way, and 32-way. In terms of block size, we explore 128B, 256B, 512B.

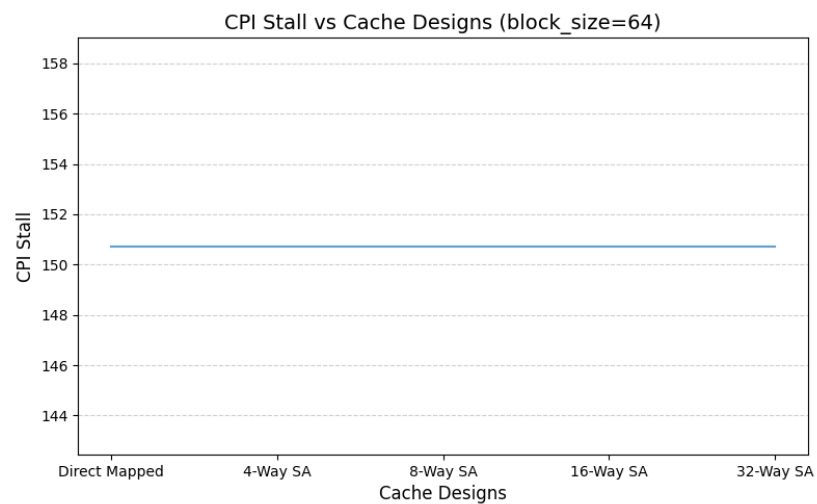
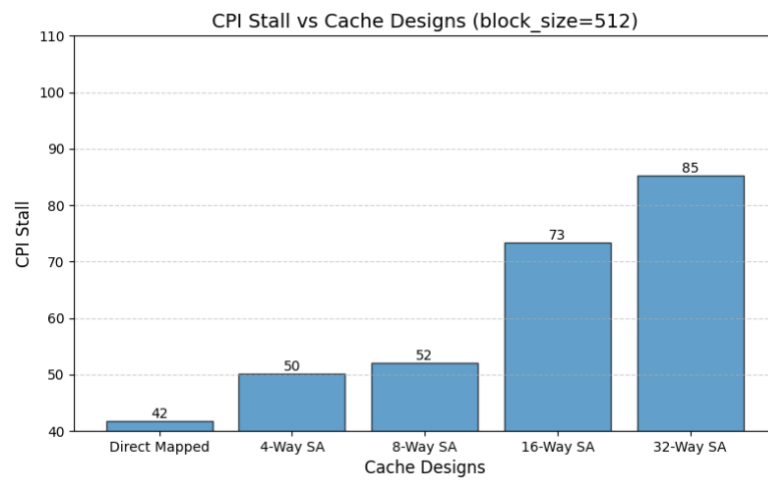
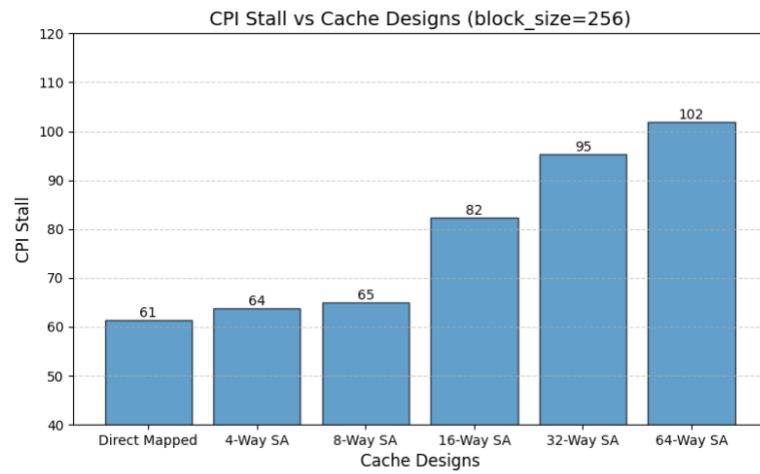
The CPI stall for a cache design X (i.e., combination of cache size, associativity, and block size), is the geometric mean of CPI stall numbers on the 4 trace files provided.

The results are show in graphs below. We notice that CPI\_stall increases with increase in # ways. As the block size increases, CPI\_stall decreases.

The rate of variance in CPI\_stall is more prominent as the block size increases: in block size 64, CPI\_stall is constant across any associativity, whereas in block\_size 512, the CPI\_stall varies from 42 to 85.

Multiple good choices of cache design can exist – among them (1,4 8) way and block size 512 cache design seems to be an optimal choice, considering CPI\_stall as the sole deciding metric.





Exceptions:

With a block size of 2048, the CPI\_stall varies from 62-125 in (1,4,8) way associativity.