CS 6354: Graduate Computer Architecture

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The output of the code is similar to the folders provided in output_files. This is the link to the generated output: https://github.com/afsara-ben/Computer-Architecture/tree/main/HW5/resources-hw5/output_files

(Link is given because of shortage of space.)

Cache design space exploration

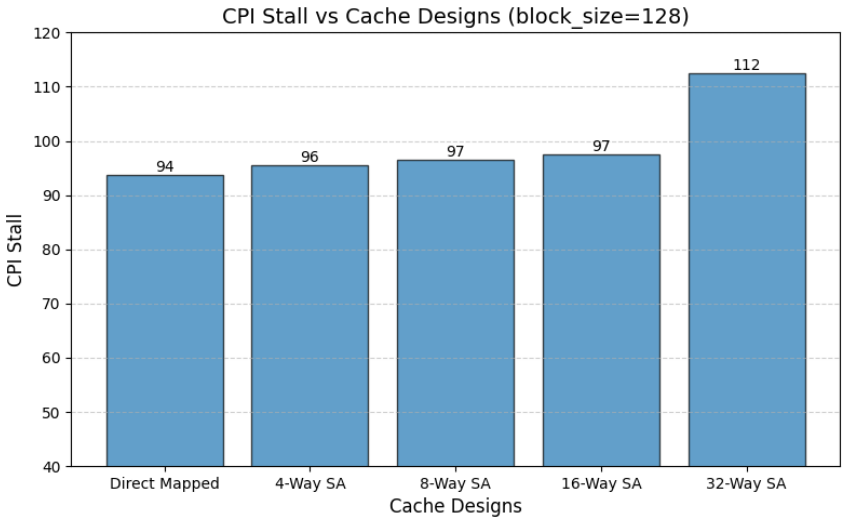
Keeping the cache size constant (16KB), In terms of associativity, we explore 1-way (direct-mapped), 4-way, 8-way, 16-way, and 32-way. In terms of block size, we explore 128B, 256B, 512B.

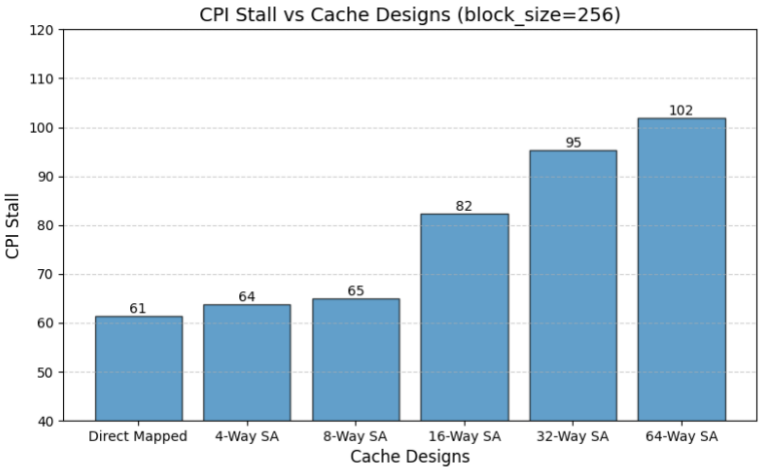
The CPI stall for a cache design X (i.e., combination of cache size, associativity, and block size), is the geometric mean of CPI stall numbers on the 4 trace files provided.

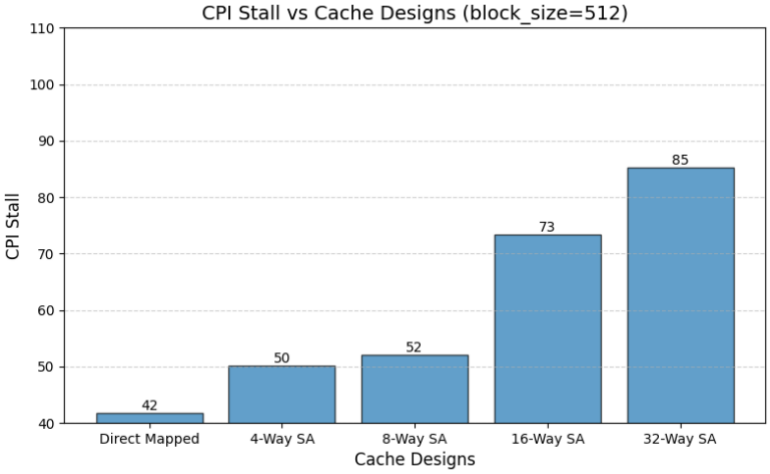
The results are show in graphs below. We notice that CPI_stall increases with increase in # ways. As the block size increases, CPI_stall decreases.

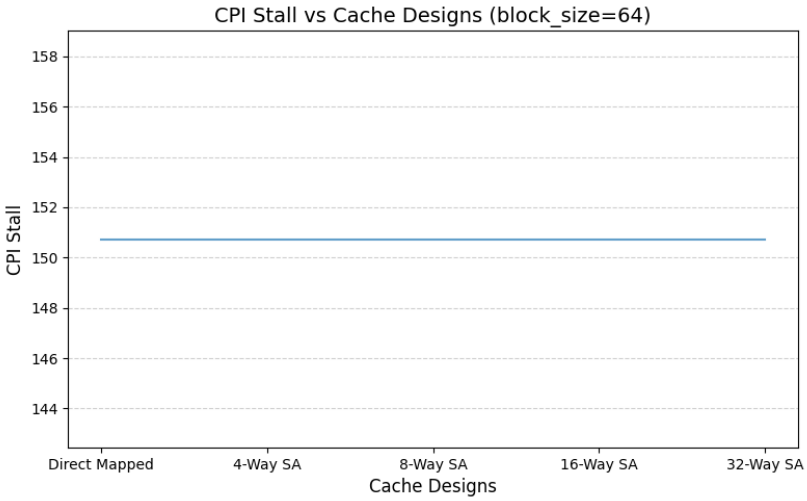
The rate of variance in CPI_stall is more prominent as the block size increases: in block size 64, CPI_stall is constant across any associativity, whereas in block_size 512, the CPI_stall varies from 42 to 85.

Multiple good choices of cache design can exist – among them (1,4 8) way and block size 512 cache design seems to be an optimal choice, considering CPI_stall as the sole deciding metric.


CPI Stall vs Cache Designs (block_size=128)
CPI Stall
Cache Designs
Direct Mapped
4-Way SA
8-Way SA
16-Way SA
32-Way SA
94
96
97
97
112


CPI Stall vs Cache Designs (block_size=256)
CPI Stall
Cache Designs
Direct Mapped
4-Way SA
8-Way SA
16-Way SA
32-Way SA
64-Way SA
61
64
65
82
95
102


CPI Stall vs Cache Designs (block_size=512)
CPI Stall
Cache Designs
Direct Mapped
4-Way SA
8-Way SA
16-Way SA
32-Way SA
42
50
52
73
85



Exceptions:
With a block size of 2048, the CPI_stall varies from 62-125 in (1,4,8) way associativity.