## About Us

Atrenta's SpyGlass® Predictive Analysis software platform significantly improves design efficiency for the world's leading semiconductor and consumer electronics companies. Patented solutions provide early design insight into the demanding performance, power and area requirements of the complex system-on-chip (SoC) devices fueling today's consumer electronics revolution.

More than two hundred companies and thousands of design engineers worldwide rely on SpyGlass to reduce risk and cost before traditional electronic design automation (EDA) tools are deployed. SpyGlass functions like an interactive guidance system for design engineers and managers, finding the fastest and least expensive path to implementation for complex SoCs.

Headquartered in San Jose, CA, USA, Atrenta Inc. has its biggest R&D center in India. Atrenta India was formed in May 2001 and operates from its development centers in Noida (near Delhi) and Bangalore. It is led by an experienced and technically skilled management team and currently employs approximately 200 professionals from premier technical institutes in India.

Atrenta Lanka operations started in 2011. This facility is one of the fastest growing product development centers for Atrenta. The location provides excellent opportunities to learn and work on complex SoC designs as part of the EDA industry. With a hot startup culture, there is immense opportunity for professional growth. Atrenta is the largest privately held EDA company in the industry.

## Our Technology

Atrenta's SpyGlass and GenSys® product lines form a complete, proven solution for SoC design. With the recent addition of the BugScope™ product from NextOp Software, Atrenta now addresses functional verification as well as design. Atrenta's products all work at the architectural or register transfer level (RTL) of abstraction, making it easier to create an optimized design very early in the development process.

These product families address challenges in architecture definition, IP import, chip assembly, synthesizability, clock synchronization (CDC), power management, constraints management, testability, routing congestion and function verification completeness. Atrenta's GuideWare reference methodology allows our solutions to easily fit into a user's existing design flow.

Our products use advanced EDA technologies, such as:

- Logic synthesis and optimization
- Logic simulation
- Design for test (DFT) and testability analysis
- Formal techniques such as SAT solvers, BDD and bounded model checking
- Low power design and power estimation
- Floor planning and place & route
- Static timing analysis and timing optimization
- Interconnect synthesis

## Our Customers

Atrenta's customers are leading semiconductor and system companies including: Altera, Cisco, Qualcomm, TSMC, Fujitsu, LG, NVIDIA, STMicroelectronics, Texas Instruments and AMD. The list goes on. Many advanced processors and some of the hottest consumer electronics products are designed using Atrenta's software.

## Our Executive Team

- **Ajoy Bose, PhD, Chairman, President and CEO**
  Dr. Bose has over 30 years experience in engineering and management. Prior to establishing Atrenta, Dr. Bose was founder and president of Interra, Inc. and Software & Technologies. He has also held senior management positions at AT&T Bell Laboratories and Cadence Design Systems.
- **Bert Clement, Chief Financial Officer**
  Mr. Clement's experience in financial management spans more than 25 years with companies such as VeriSign, MCI Telecommunications, Broad Point Communications, Advanced Water Technologies and Network Solutions.
- **Mike Fazeli, Vice President of Strategic Development**
  Mike Fazeli is a 27 year veteran of the semiconductor industry. He has held a variety of senior management positions at Texas Instruments, including the development of worldwide EDA strategies for TI business units.
- **Mike Gianfagna, Vice President of Corporate Marketing**
  Mike Gianfagna's career spans both semiconductor and EDA. He has held senior management positions at General Electric, Harris Semiconductor and Cadence Design Systems. He was an early employee at eSilicon and a CEO at a venture-funded DFM startup.
- **Sushil Gupta, VP and Managing Director, India**
  Mr. Gupta has held senior positions with Texas Instruments, Cadence Design Systems and Duet Technologies. Most recently, Mr. Gupta was head of Motorola's Design Center at Noida, India.
- **Mo Movahed, Vice President of Engineering**
  Mr. Movahed previously held key positions at Lattice Semiconductor as vice president of software engineering, and senior management and research positions at Cadence Design Systems and Xerox.
- **Bernard Murphy, PhD, Chief Technology Officer**
  Dr. Murphy previously held senior positions with Cadence Design Systems, National Semiconductor and Fairchild.
- **Piyush Sancheti, Vice President of Product Marketing**
  Mr. Sancheti has over 18 years of experience in marketing, sales, business development and engineering. He has previously held senior positions at Cadence Design Systems, Senté and Sequence Design.
- **Ravi Varadarajan, Atrenta Fellow**
  Mr. Varadarajan has previously worked as a senior architect at Cadence Design Systems. He was one of the early employees of Tera Systems and at AT&T Bell Laboratories.
- **Yunshan Zhu, PhD, Vice President of New Technologies**
  Before its acquisition by Atrenta, Dr. Yunshan Zhu co-founded NextOp Software and led the company through the development, delivery and production implementation of its flagship assertion synthesis product for multiple semiconductor companies.

**For more information contact your Placement Office or visit our corporate website at [www.atrenta.com](http://www.atrenta.com)**