

# DESIGN OF COMMON SOURCE AMPLIFIER (REDESIGNED)

AS W/L RATIO WAS VERY HIGH IN PREVIOUS  
DESIGN APPROACH AND SIMULATIONS RESULT  
WERE NOT EXACTLY MATCHING THE  
SPECIFICATION

# COMMON SOURCE AMPLIFIER

USING NMOS AND PASSIVE LOAD

MODEL FILE : 180n

SPECIFICATIONS

GBW=800MHz , VDD=1.8V , L=0.36u

## CALCULATIONS

GBW=800MHz , L=0.36u , Vdd=1.8V, Model file = 180n

Let GAIN (A) = 10

$$f(-3\text{db}) = \frac{GBW}{Gain} = 80\text{MHz} \quad \text{LET } Gm=2\text{mS} \text{ (Practical value range 1-3 S)}$$

given by Javed Sir)

$$\text{USING } C_L = \frac{Gm}{2\pi GBW} \quad C_L = 0.397\text{pF} \text{ (assume 0.3pF)}$$

Now by Back calculation ,

$$Gm = 2\pi GBW C_L = 1.5\text{mS}$$

Assume  $V_{ov}=0.2\text{V}$

$V_{gs}=0.65\text{V}$

$$I_d = \frac{Gm V_{ov}}{2} = 150\mu\text{A}$$

Then ,  $Gm/I_d = 10$

$$R = (1.8 - 0.9)/150\mu\text{A} = 6\text{Kohm}$$

W is calculated by sweeping for 150uA current

# SCHEMATIC IN LT SPICE

## COMMON SOURCE AMPLIFIER DESIGNED USING GM OVER ID new approach METHOD USING NMOS AND RESISTOR for GBW = 800MHz

(SPECIFICATIONS)

GBW=800MHz

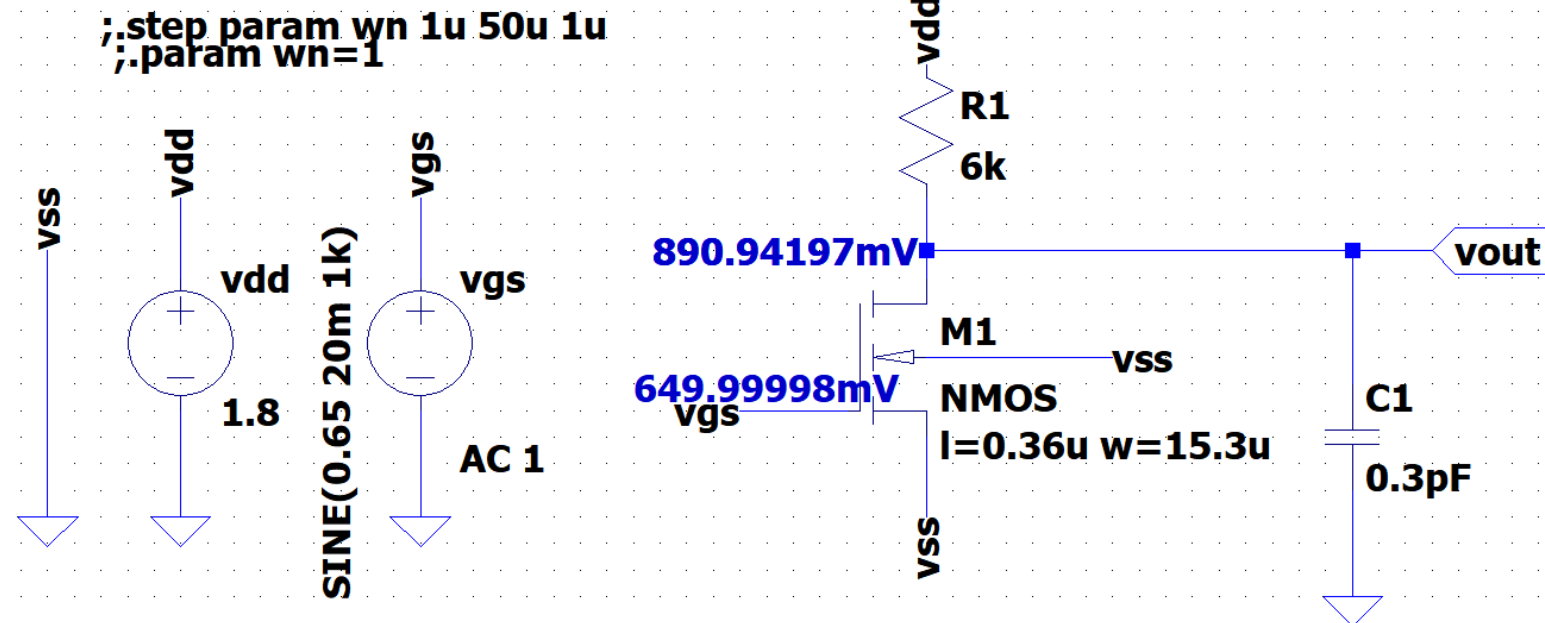
vdd=1.8V

```
.include tsmc180.txt  
.op
```

```
;.tf V(vout) vgs
```

```
;.ac dec 100 1Meg 100G
```

```
.tran 5m
```



--- Transfer Function ---

Transfer_function:	-10.0208	transfer
vgs#Input_impedance:	1e+020	impedance
output_impedance_at_V(vout):	5453.14	impedance

--- Operating Point ---

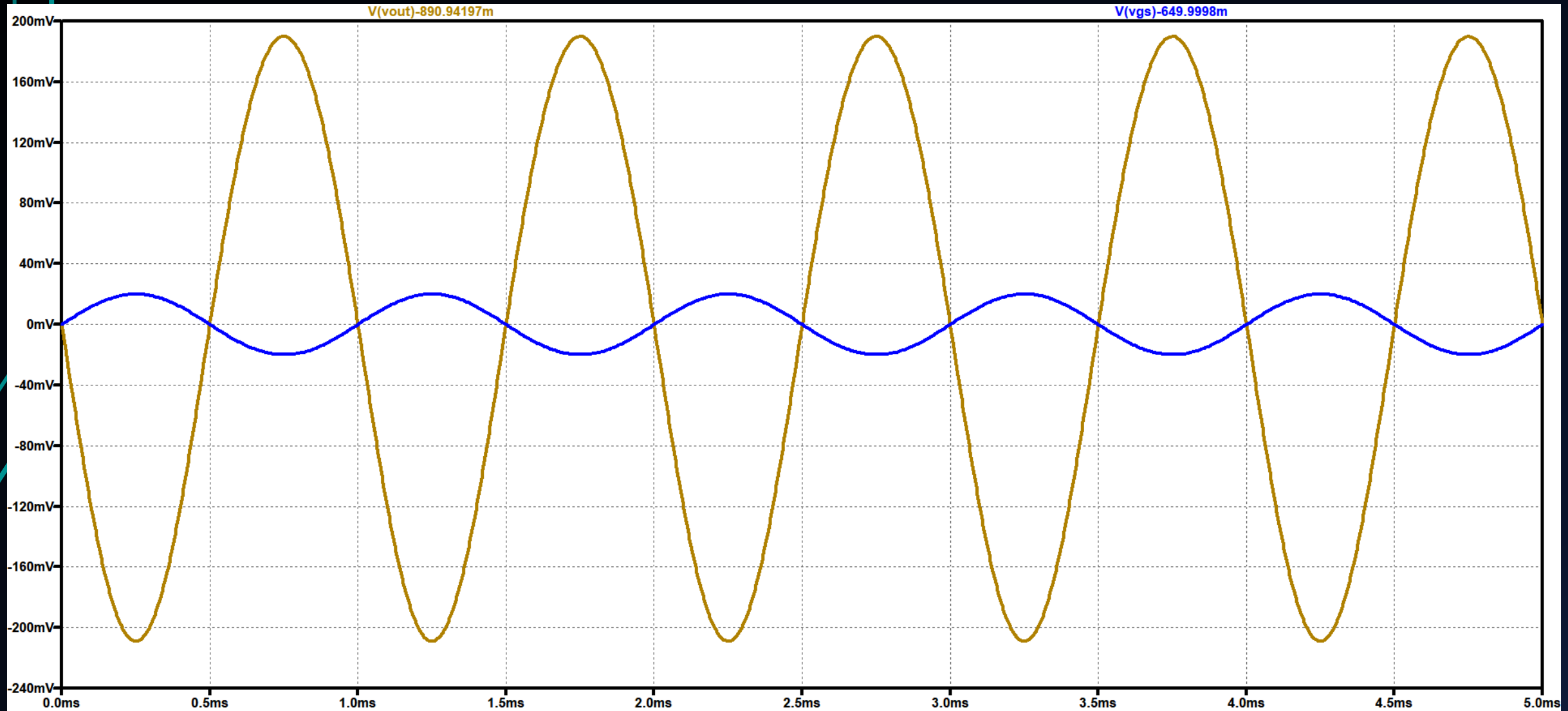
V(vout):	0.890942	voltage
V(vgs):	0.65	voltage
V(vdd):	1.8	voltage
Id(M1):	0.00015151	device_current
Ig(M1):	0	device_current
Ib(M1):	-9.00942e-013	device_current
Is(M1):	-0.00015151	device_current
I(C1):	2.67283e-025	device_current
I(R1):	0.00015151	device_current
I(Vgs):	0	device_current
I(Vdd):	-0.00015151	device_current

Semiconductor Device Operating Points:

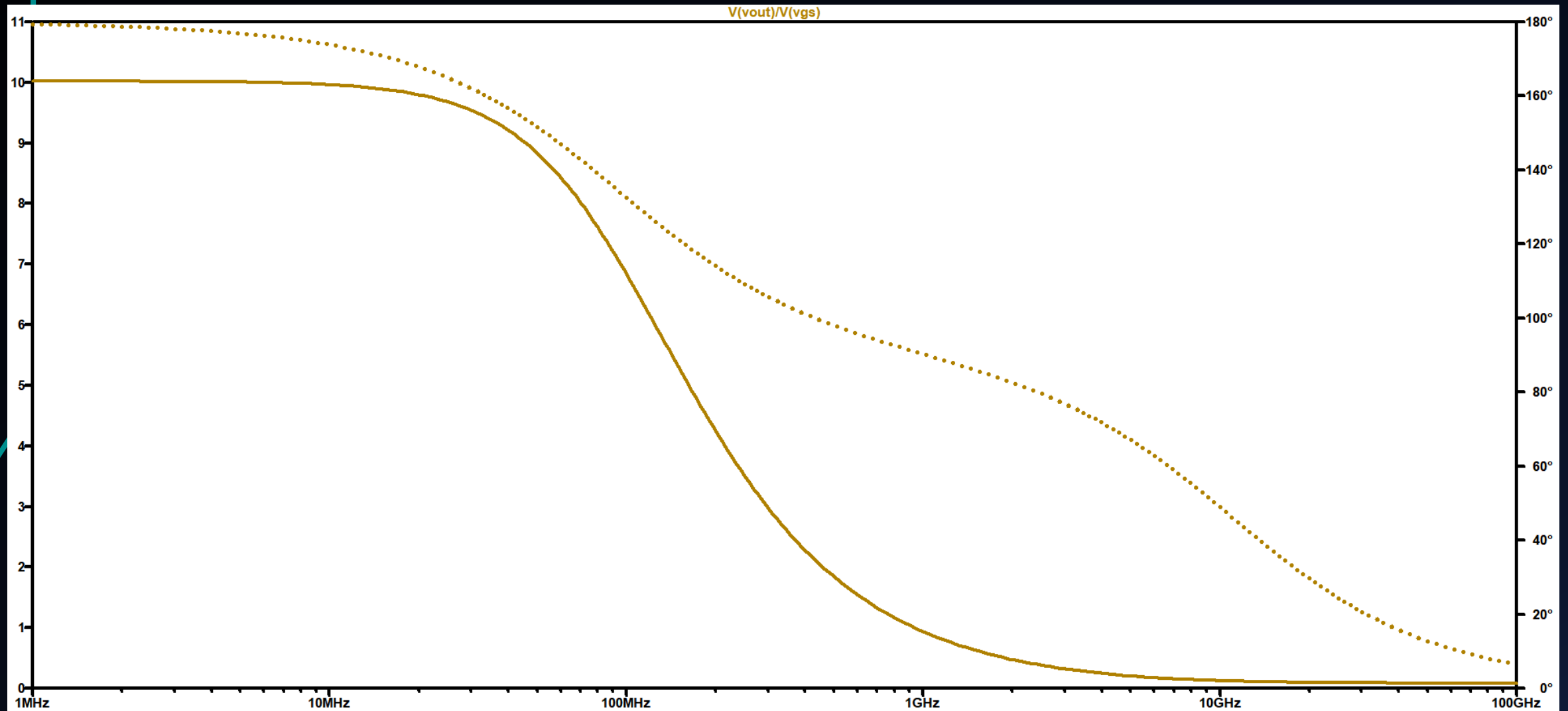
--- BSIM3 MOSFETS ---

Name:	m1
Model:	nmos
Id:	1.52e-04
Vgs:	6.50e-01
Vds:	8.91e-01
Vbs:	0.00e+00
Vth:	4.66e-01
Vdsat:	1.41e-01
Gm:	1.84e-03
Gds:	1.67e-05
Gmb:	4.81e-04
Cbd:	0.00e+00
Cbs:	0.00e+00

# TRANSIENT ANALYSIS IN LT SPICE



# FREQUENCY RESPONSE IN LT SPICE



# COMMON SOURCE AMPLIFIER

USING PMOS AND PASSIVE LOAD

MODEL FILE : 180n

SPECIFICATIONS

GBW=800MHz , VDD=1.8V , L=0.36u



## CALCULATIONS

GBW=800MHz , L=0.36u , Vdd=1.8V, Model file = 180n

LET  $G_m=3\text{mS}$  (Practical value range 1-3 S given by Javed Sir)

USING  $C_L = \frac{G_m}{2\pi GBW}$        $C_L = 0.49\text{pF}$  (assume 0.5pF)

Now by Back calculation ,

$$G_m = 2\pi GBW C_L = 2.5\text{mS}$$

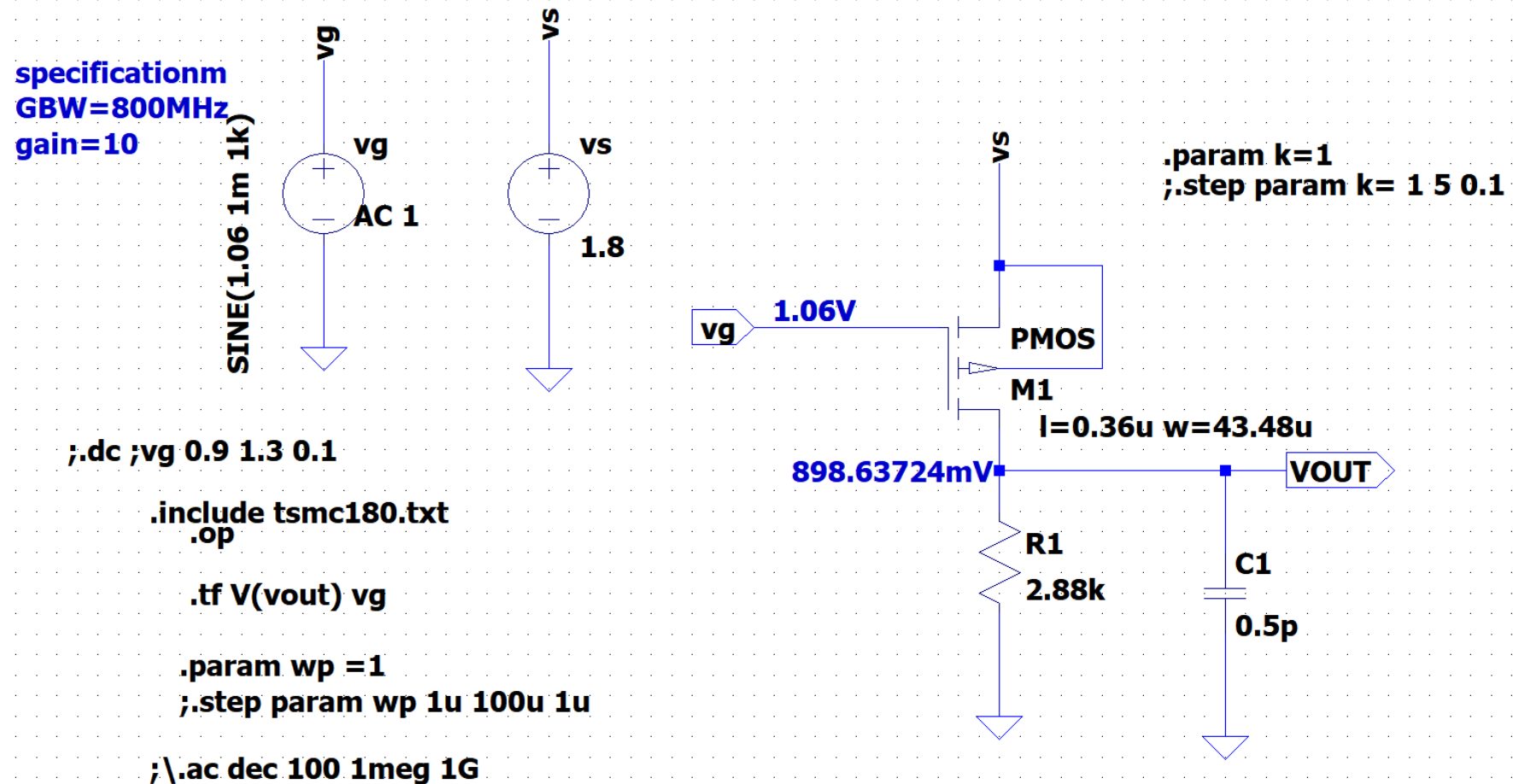
Assume  $V_{ov}=0.2\text{V}$        $V_g=1.1\text{V}$        $I_d = \frac{G_m V_{ov}}{2} = 312\mu\text{A}$

Then ,  $G_m/I_d = 8.01$

$$R = (1.8 - 0.9)/312\mu\text{A} = 2.88\text{ Kohm}$$

W is calculated by sweeping for 312uA current

# SCHEMATIC IN LT SPICE



--- Transfer Function ---

Transfer_function:	-5.74605	transfer
vg#Input_impedance:	1e+020	impedance
output_impedance_at_V(vout):	2676.28	impedance

--- Operating Point ---

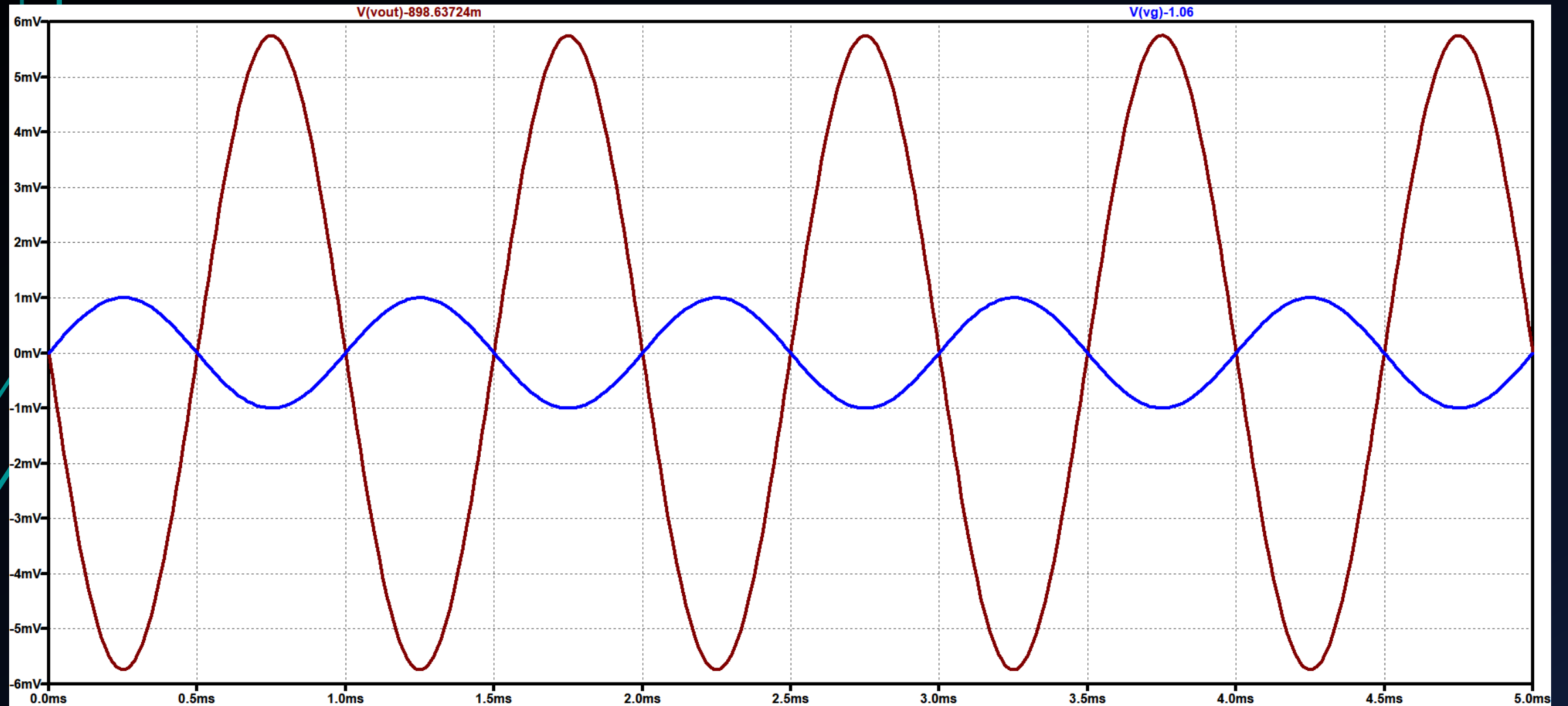
V(vg) :	1.06	voltage
V(vs) :	1.8	voltage
V(vout) :	0.898637	voltage
Id(M1) :	-0.000312027	device_current
Ig(M1) :	-0	device_current
Ib(M1) :	9.11363e-013	device_current
Is(M1) :	0.000312027	device_current
I(C1) :	4.49319e-025	device_current
I(R1) :	0.000312027	device_current
I(Vs) :	-0.000312027	device_current
I(Vg) :	0	device_current

Semiconductor Device Operating Points:

--- BSIM3 MOSFETS ---

Name:	m1
Model:	pmos
Id:	-3.12e-04
Vgs:	-7.40e-01
Vds:	-9.01e-01
Vbs:	0.00e+00
Vth:	-4.73e-01
Vdsat:	-2.33e-01
Gm:	2.15e-03
Gds:	2.64e-05
Gmb:	6.96e-04
Cbd:	0.00e+00
Cbs:	0.00e+00
Cgsov:	3.09e-14
Cgdov:	3.09e-14

# TRANSIENT ANALYSIS IN LT SPICE



# COMMON SOURCE AMPLIFIER

USING NMOS AND CURRENT SOURCE LOAD

MODEL FILE : 180n

SPECIFICATIONS

GBW=1GHz , Gain = 10 at 100MHz

## CALCULATIONS

GBW=1GHz , Gain = 10 at 100MHz

LET  $G_m=2\text{mS}$  (Practical value range 1-3 S given by Javed Sir)

USING  $C_L = \frac{G_m}{2\pi GBW}$   $C_L = 0.318\text{pF}$  (assume 0.3pF)

Now by Back calculation ,

$G_m = 2\pi GBW C_L = 1.884\text{mS}$

(For nmos)  $V_{ov}=0.2\text{V}$   $V_{gs}=0.65\text{V}$   $I_d = \frac{G_m V_{ov}}{2} = 188\mu\text{A}$

Then ,  $G_m/I_d = 10.021$   $I_d/W = 13.6$

$W=14\mu$

(For pmos)  $V_g=1.1\text{V}$

Width of PMOS is taken twice as that of nmos

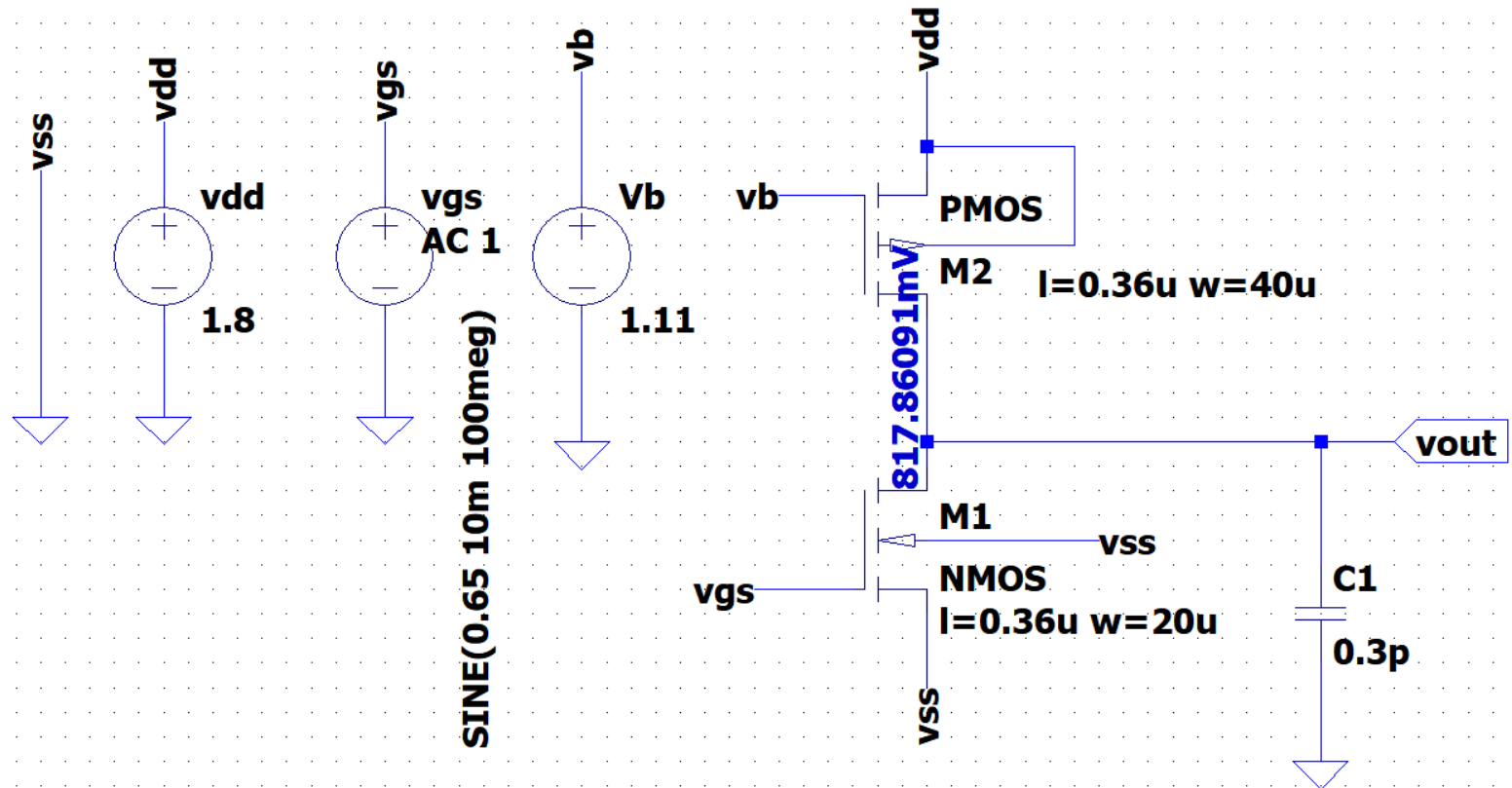
$W=28\mu$

NOTE : Now some manipulations are done in calculations to meet the specifications

# SCHEMATIC IN LT SPICE

## COMMON SOURCE AMPLIFIER DESIGNED USING GM OVER ID METHOD USING NMOS AND CURRENT SOURCE LOAD

```
.op  
;tf V(vout) vgs  
.include tsmc180.txt  
;.tran 400n  
;.dc vb 0 1.8 1m
```



```
.ac dec 10 1MEG 400G
```

--- Operating Point ---

V(vout):	0.817861	voltage
V(vgs):	0.65	voltage
V(vdd):	1.8	voltage
V(vb):	1.11	voltage
Id(M2):	-0.000197001	device_current
Ig(M2):	-0	device_current
Ib(M2):	9.92139e-013	device_current
Is(M2):	0.000197001	device_current
Id(M1):	0.000197001	device_current
Ig(M1):	0	device_current
Ib(M1):	-8.27861e-013	device_current
Is(M1):	-0.000197001	device_current
I(C1):	2.45358e-025	device_current
I(Vb):	0	device_current
I(Vdd):	-0.000197001	device_current
I(Vgs):	0	device_current

Semiconductor Device Operating Points:

--- BSIM3 MOSFETS ---

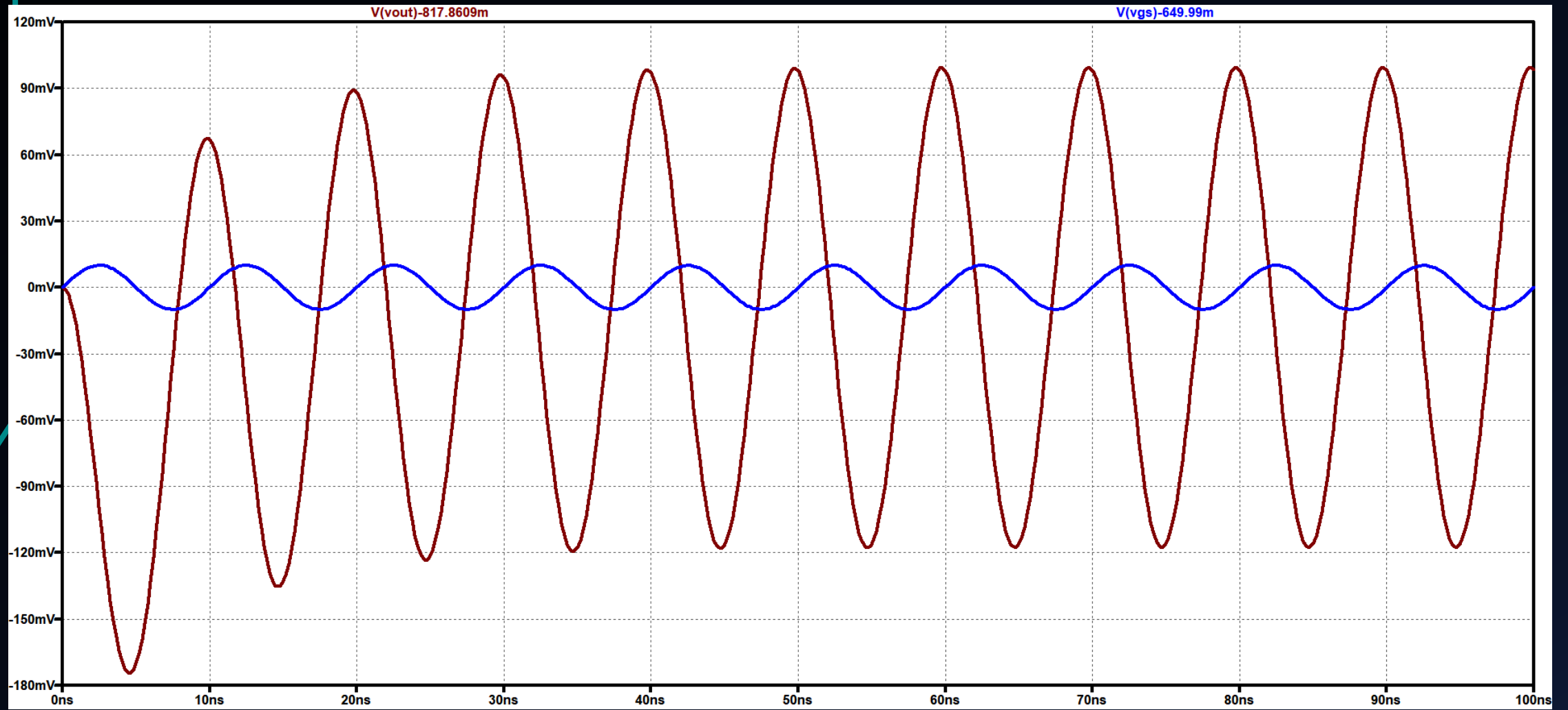
Name:	m2	m1
Model:	pmos	nmos
Id:	-1.97e-04	1.97e-04
Vgs:	-6.90e-01	6.50e-01
Vds:	-9.82e-01	8.18e-01
Vbs:	0.00e+00	0.00e+00
Vth:	-4.73e-01	4.65e-01
Vdsat:	-1.94e-01	1.41e-01
Gm:	1.68e-03	2.39e-03
Gds:	1.69e-05	2.22e-05
Gmb:	5.39e-04	6.26e-04
Cbd:	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00
Cgsov:	2.84e-14	1.54e-14
Cgdov:	2.84e-14	1.54e-14
Cgbov:	2.11e-10	2.22e-10

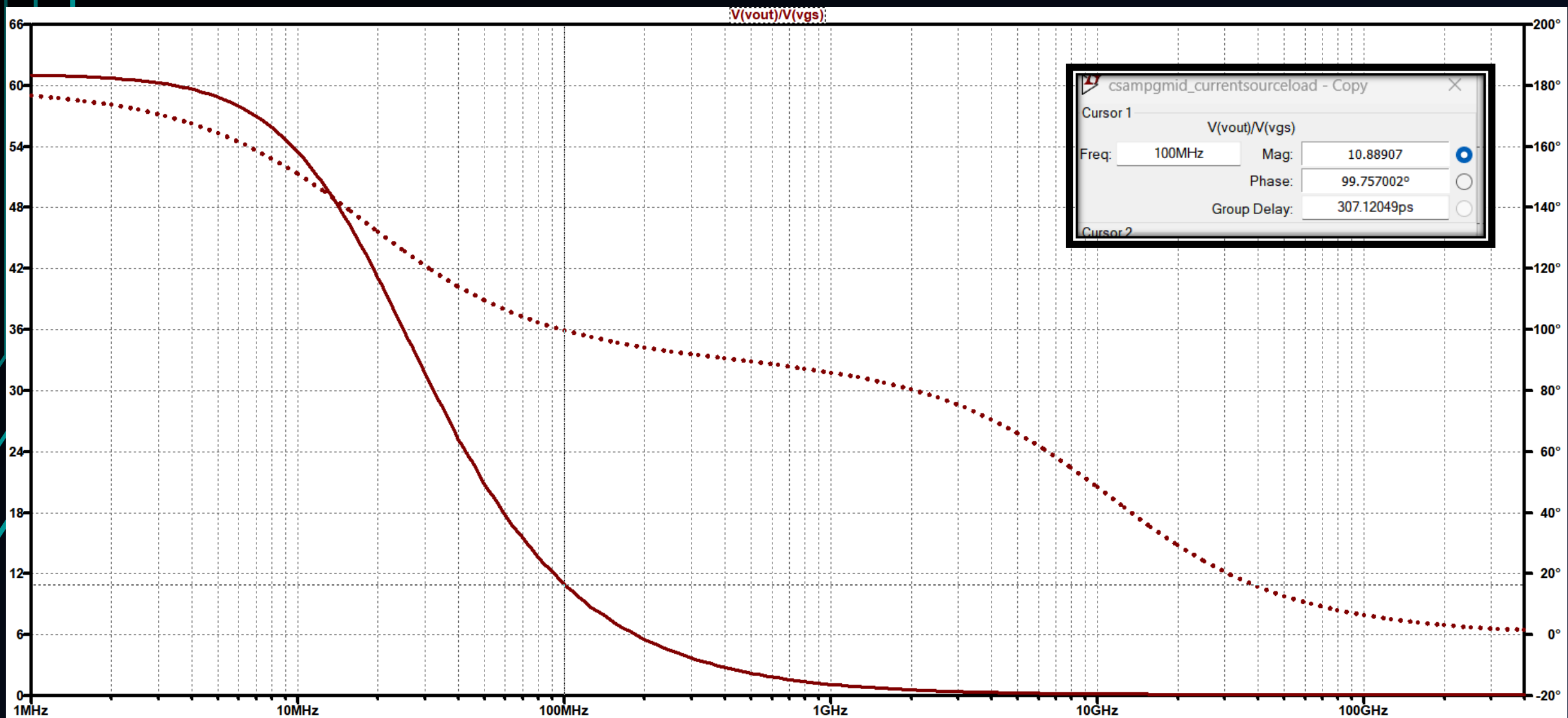
--- Transfer Function ---

Transfer_function:	-61.0818	transfer
vgs#Input_impedance:	1e+020	impedance
output_impedance_at_V(vout):	25549.1	impedance



# TRANSIENT ANALYSIS IN LT SPICE





csampgmid\_currentsourceload - Copy

Cursor 1

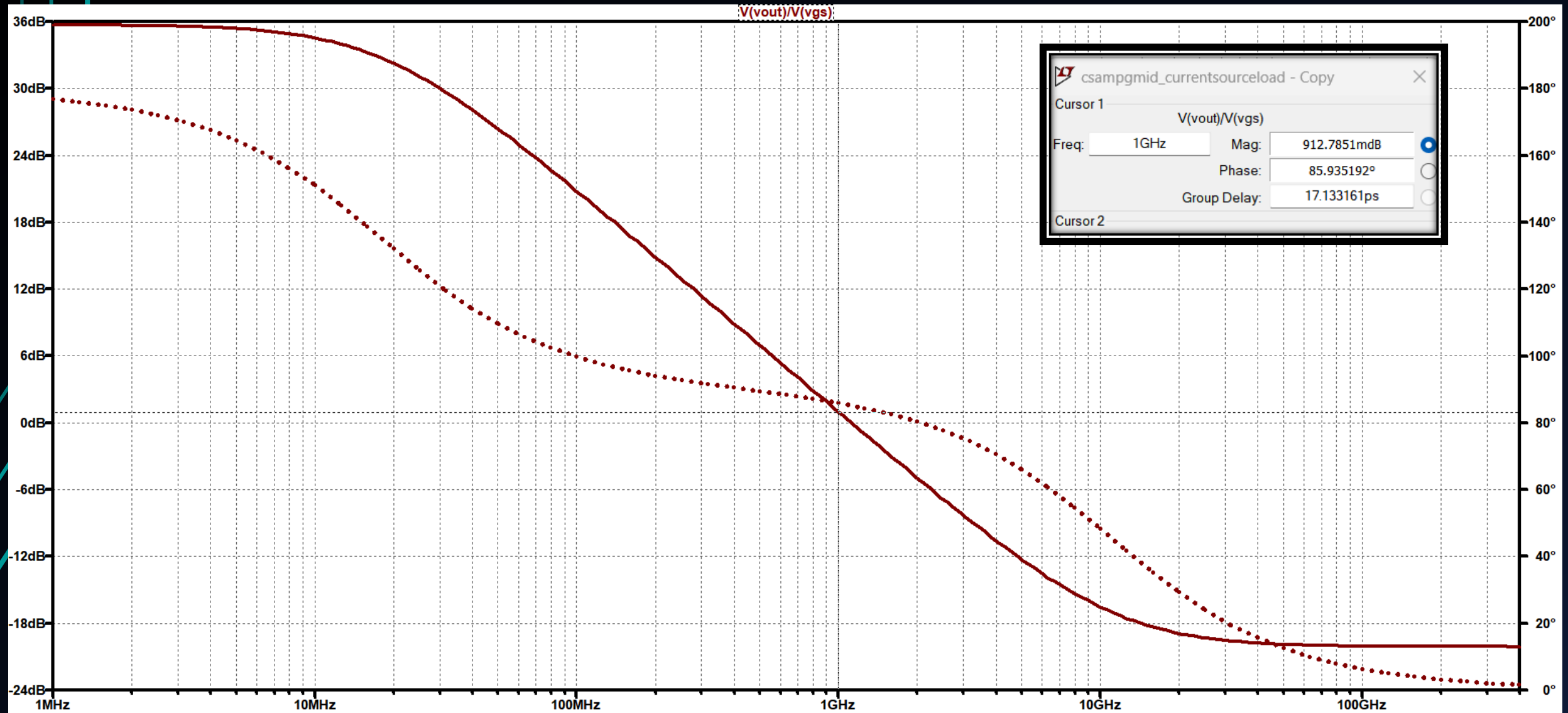
$V(vout)/V(vgs)$

Freq: 100MHz Mag: 10.88907

Phase: 99.757002°

Group Delay: 307.12049ps

Cursor 2





*THANK YOU*