

# INTERNSHIP REPORT

*A report submitted in partial fulfilment of the requirements for the*

## SUMMER INTERNSHIP PROGRAM

in

### ANALOG CIRCUIT DESIGN

By

**AFZAL MALIK**

**Under Mentorship of**

**Dr. GS Javed**

**Technical Lead @Intel**

**Prof. Naushad Alam & Prof. Atiqur Rahman**

**(Department of Electronics Engineering, ZHCET, AMU)**



**DEPARTMENT OF ELECTRONICS ENGINEERING  
ZAKIR HUSAIN COLLEGE OF ENGINEERING  
AND TECHNOLOGY  
ALIGARH MUSLIM UNIVERSITY**



## STUDENTS' DECLARATION

I hereby certify that this internship work entitled "**ANALOG DESIGN INTERNSHIP**" was completed under the guidance of Dr. G S Javed, Technical Lead at Intel, and Prof. Naushad Alam, Department of Electronics Engineering, Zakir Husain College of Engineering & Technology, Aligarh Muslim University, Aligarh.

**AFZAL MALIK**



## CERTIFICATE

This is to certify that the internship report titled '**ANALOG DESIGN INTERNSHIP**' is being submitted to Dr. G S Javed, Technical Lead at Intel, and Dr. Naushad Alam, Professor in the Department of Electronics Engineering, Zakir Husain College of Engineering & Technology, Aligarh Muslim University, Aligarh.

The undersigned confirm that the contents of this report are the result of the intern's original work and have been duly reviewed and found to be in accordance with the prescribed guidelines and standards.

Date: 16 July 2023

Place: Bengaluru

**Dr. G S Javed**

Technical Lead, Intel

**Dr. Naushad Alam**

Professor, Department of Electronics Engineering  
Zakir Husain College of Engineering & Technology  
Aligarh Muslim University, Aligarh"

## ACKNOWLEDGEMENT

I take this opportunity to express my sincere gratitude to all those who have contributed to the successful completion of my internship.

First and foremost, I would like to extend my deepest appreciation to our esteemed mentors, Dr. GS Javed, Professor Syed Atiqur Rahman, Professor Naushad Alam, for their invaluable guidance, encouragement, and expertise throughout the internship. Their mentorship has been instrumental in shaping my understanding of Analog Circuit Design and has inspired me to pursue excellence in this field.

I am immensely thankful to the Engineering Design and Implementation Club, AMU (EDIC), and the Department of Electronics Engineering at Aligarh Muslim University for providing me with the opportunity to participate in this internship program. The well-structured and insightful program has been a transformative experience in my professional journey.

I would like to express my deep gratitude to Saif Abrar Sahab, Mudassir Sir, and Shamsul Haq Sir for their exceptional support and hospitality during my internship. Their guidance, logistical support, and welcoming atmosphere have contributed significantly to the overall success of the internship.

I would also like to acknowledge the contributions of all the faculty members and staff members who have shared their knowledge and provided valuable insights during the course of this internship. Their dedication to teaching and willingness to address our queries have been immensely beneficial.

Furthermore, I would like to extend my thanks to my fellow interns, whose camaraderie and collaborative spirit have made this internship experience enjoyable and enriching.

Last but not least, I am deeply grateful to my family and friends for their unwavering support, understanding, and encouragement throughout this journey. Their belief in my abilities has been a constant source of motivation.

In conclusion, this internship and the preparation of this report have been a rewarding experience, and I am humbled by the invaluable support and encouragement I have received from everyone involved. I am confident that the knowledge and skills gained during this internship will serve as a strong foundation for my future endeavours in the field of Analog Circuit Design.

Thank you all for being an integral part of my professional growth.

With sincerest regards,

[AFZAL MALIK]

## ABSTRACT

This internship report provides an overview of a fulfilling Summer Internship in Analog Circuit Design. The internship was organized by the Engineering Design and Implementation Club (Edic) in collaboration with the Department of Electronics Engineering at Aligarh Muslim University. Throughout six weeks, we had a fantastic chance to learn Analog Circuit Design with the help of experienced professionals like Dr. GS Javed, Professor Syed Atiqur Rahman, and Professor Naushad Alam.

During the internship, we worked on designing and simulating various Analog circuits using LTspice, a popular circuit simulation software. We designed circuits like the Common Source Amplifier, Common Drain Amplifier, Simple Current Mirror, Differential Pair, Single Stage Operational Amplifier, and a Two Stage Operational Amplifier.

A key technique we learned was the Gm over Id Methodology, which helped us optimize the circuit performance. We used simulation techniques like DC sweep, transient analysis, and AC analysis to understand how the circuits behaved.

For our designs, we used software tools like LTspice and ADT (Analog Designer Toolbox). ADT was especially helpful as it provided Lookup Tables for NMOS and PMOS devices, making plotting parameter charts easier.

Throughout the internship, we documented our progress and key learnings each week. We tackled challenges and optimized circuit parameters. We also had access to valuable lectures by experts like Professor H. Omran, Bahzad Razavi, and NPTEL IIT Madras Op-Amp Course, which deepened our understanding.

In conclusion, we are proud of completing various Analog circuit design tasks successfully. The Gm over Id Methodology, combined with LTspice and ADT, helped us design intricate circuits with excellent performance. We are grateful for this opportunity and are excited to apply our new knowledge in the world of Analog circuit design.

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## WEEK 1: ANALOG DESIGN INTERNSHIP

### GM OVER ID METHOD: DESIGN METHODOLOGY

In order to design an amplifier using gm over id methodology we require primary parameter charts:

There are two types of parameter charts for NMOS and PMOS:

- 1) Primary Charts
  - i) Gm/Gds vs Gm/Id
  - ii) Id/W vs Gm/Id
  - iii) Ft vs Gm/Id
- 2) Secondary Charts
  - i) Cgd/Cgg vs Gm/Id
  - ii) Cdd/Cgg vs Gm/Id

### PLOTTING PARAMETER CHARTS FOR NMOS

The Parameter Charts for NMOS are plotted using LT Spice and MS Excel for the Technology node 180 nm. The model file used is tsmc180.txt

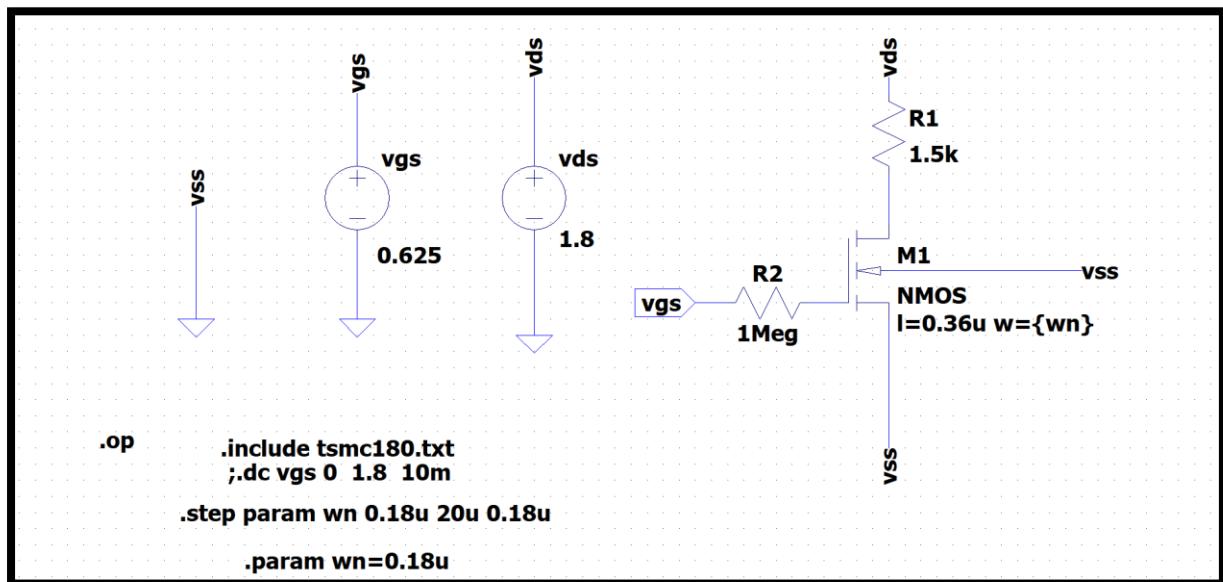


Figure 1 : LT SPICE SETUP TO PLOT CHARTS FOR NMOS

After making the setup in LT spice,

Id vs Vgs is plotted by sweeping vgs from 0 to 1.8 V

Gm [ d(Id(M1)) ] vs Vgs is plotted by sweeping vgs from 0 to 1.8 V

Id vs Vds is plotted by sweeping Vds from 0 to 1.8 V

Gds [ d(Id(M1)) ] vs Vds is plotted by sweeping vgs from 0 to 1.8 V

All this data is transferred in MS Excel and then

Gm/Gds vs Gm/Id is plotted

Id/W vs Gm/Id is plotted

Hence, we got two of the parameter charts that are required to design basic Analog Circuits using Gm over Id Method.

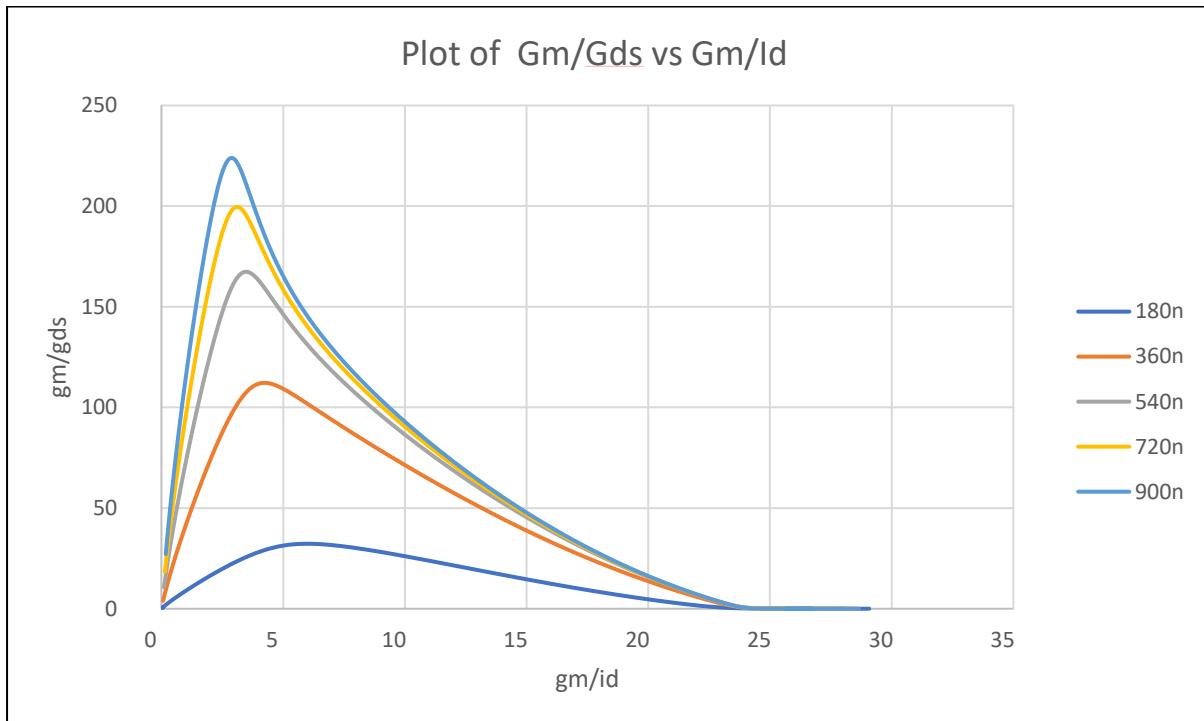


Figure 2

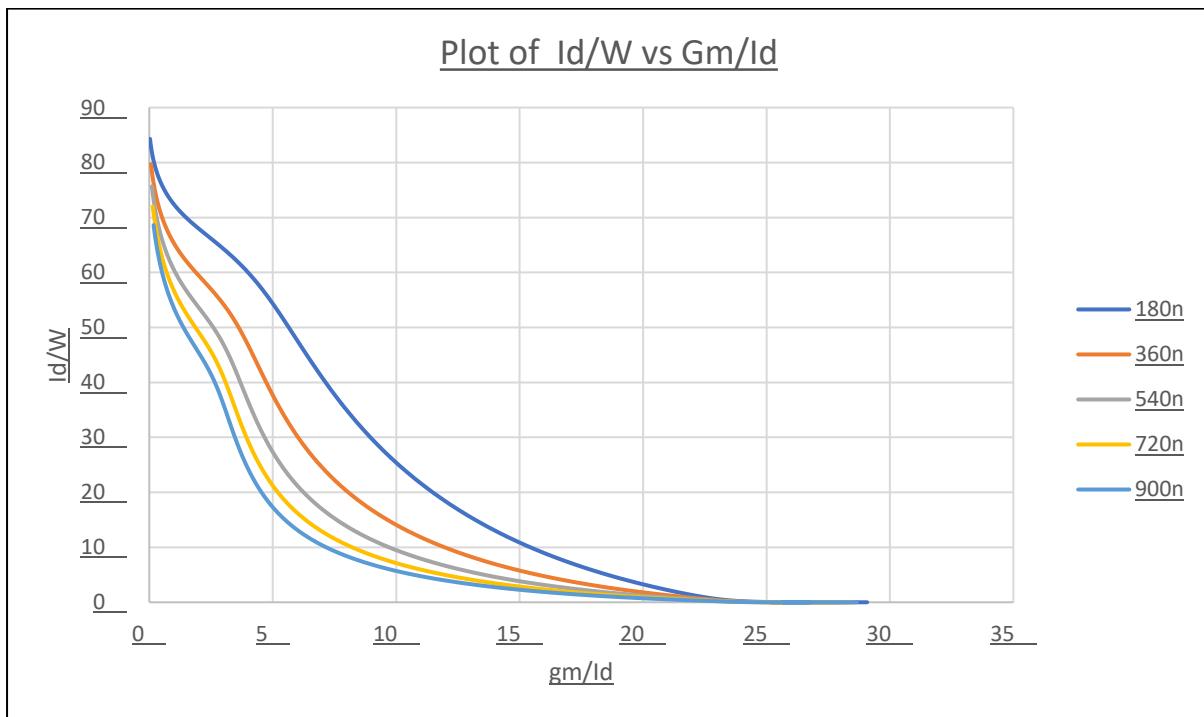


Figure 3

Then, similar to NMOS, schematic for PMOS is made in LT spice and following the similar steps PMOS parameter charts are plotted.

## PLOTTING PARAMETER CHARTS FOR PMOS

The Parameter Charts for PMOS are plotted using LT Spice and MS Excel for the Technology node 180 nm. The model file used is tsmc180.txt

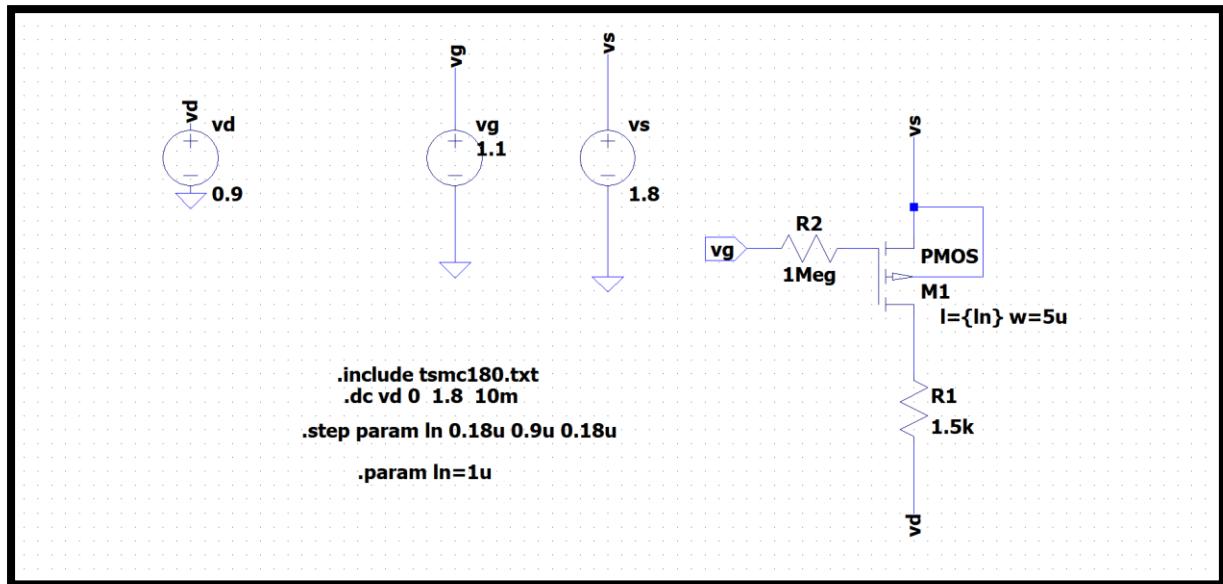


Figure 4 : LT SPICE SETUP TO PLOT CHARTS FOR PMOS

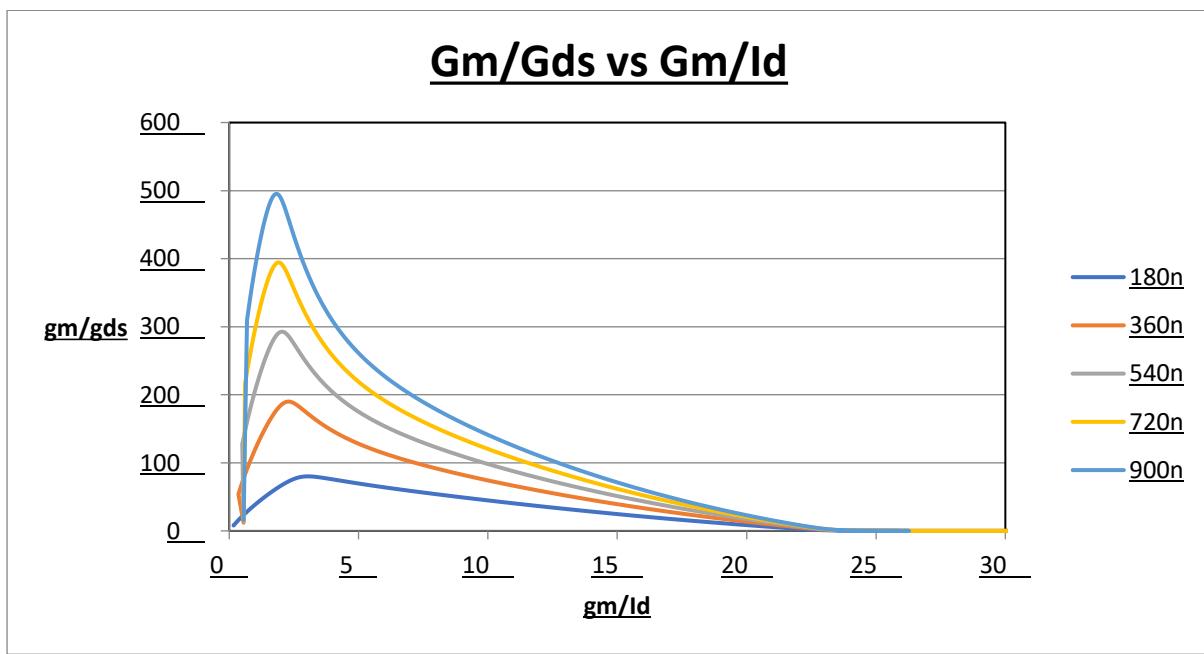


Figure 5

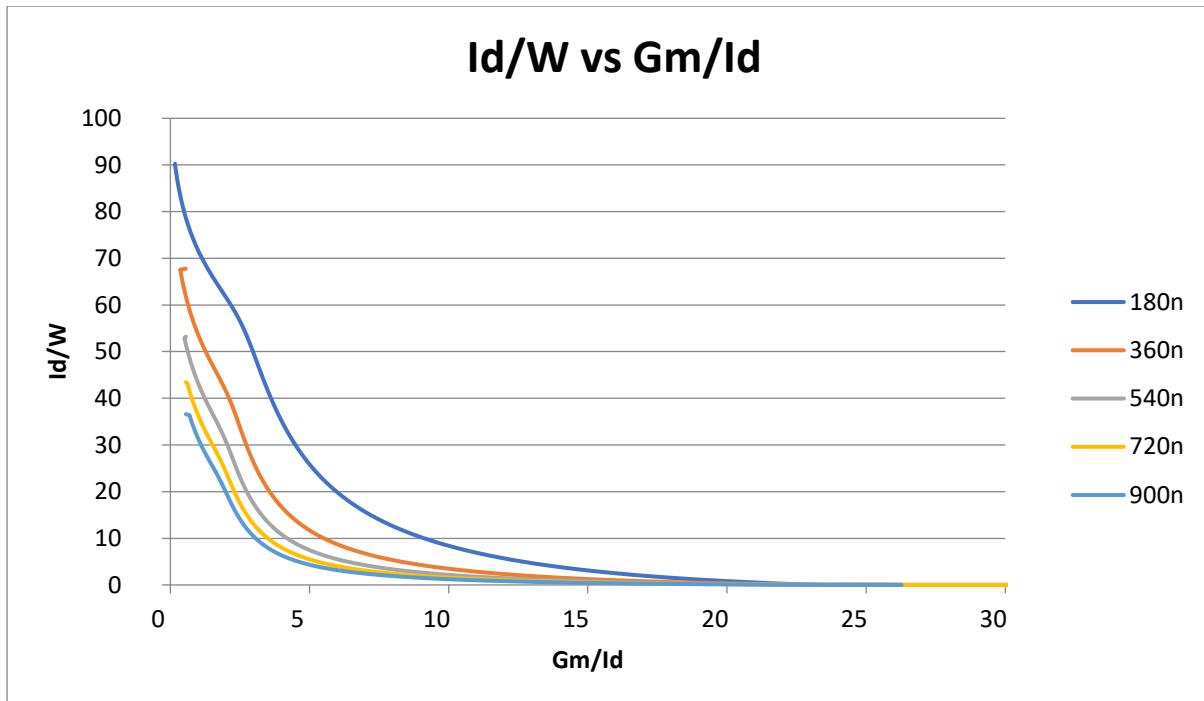


Figure 6

### DESIGN OF COMMON SOURCE AMPLIFIER USING NMOS AND RESISTIVE LOAD

The Model file used is tsmc180.txt

SPECIFICATIONS
GBW=800MHz
CL=5pF
Gain = 10

### CALCULATIONS

GBW=800MHz, L=0.36u, Vdd=1.8V, Model file = 180n

Let GAIN (A) = 10

$$f(-3\text{db}) = \frac{GBW}{Gain} = 80\text{MHz} \quad \text{let } C_L = 5\text{pF}$$

$$\text{USING } f(-3\text{db}) = \frac{1}{2\pi R_{out} C_L} \quad R_{out} = 397.88 \text{ ohm}$$

$$\text{Now, Gain (A)} = G_m R_{out} \quad G_m = 25.1 \text{ mS}$$

$$\text{Now, Let } G_m/Id = 10.2 \quad Id = 2.46 \text{ mA}$$

(From NMOS Parameter Charts)

Gm/Gds = 69.9

Gds=359 uS

AS Ro=1/Gds,

Ro=2785ohm

(From NMOS Parameter Charts)

Id/W= 13.6

W=180u

Now Rout = Ro || RL

$$R_L = \frac{Ro * Rout}{(Ro - Rout)}$$

$$R_L = 464.197 \text{ ohms}$$

Now, Vgs is calculated from Gm/Id vs Vgs Curve in LT Spice

For, Gm/Id = 10.2 Vgs = 702mV = 0.702V

## SCHEMATIC

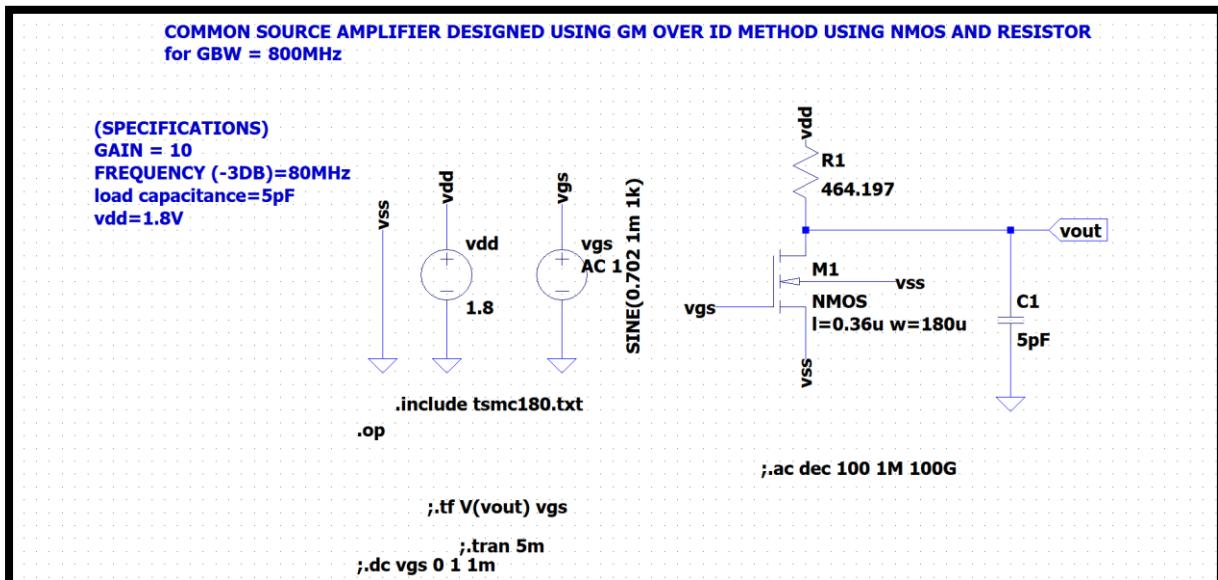


Figure 7

## SIMULATIONS

--- Operating Point ---		
V(vout) :	0.421546	voltage
V(vgs) :	0.702	voltage
V(vdd) :	1.8	voltage
Id(M1) :	0.00296954	device_current
Ig(M1) :	0	device_current
Ib(M1) :	-4.31546e-013	device_current
Is(M1) :	-0.00296954	device_current
I(C1) :	2.10773e-024	device_current
I(R1) :	0.00296954	device_current
I(Vgs) :	0	device_current
I(Vdd) :	-0.00296954	device_current

```

--- Transfer Function ---

Transfer_function:          -10.2737      transfer
vgs#Input_impedance:        1e+020       impedance
output_impedance_at_V(vout): 382.623     impedance

```

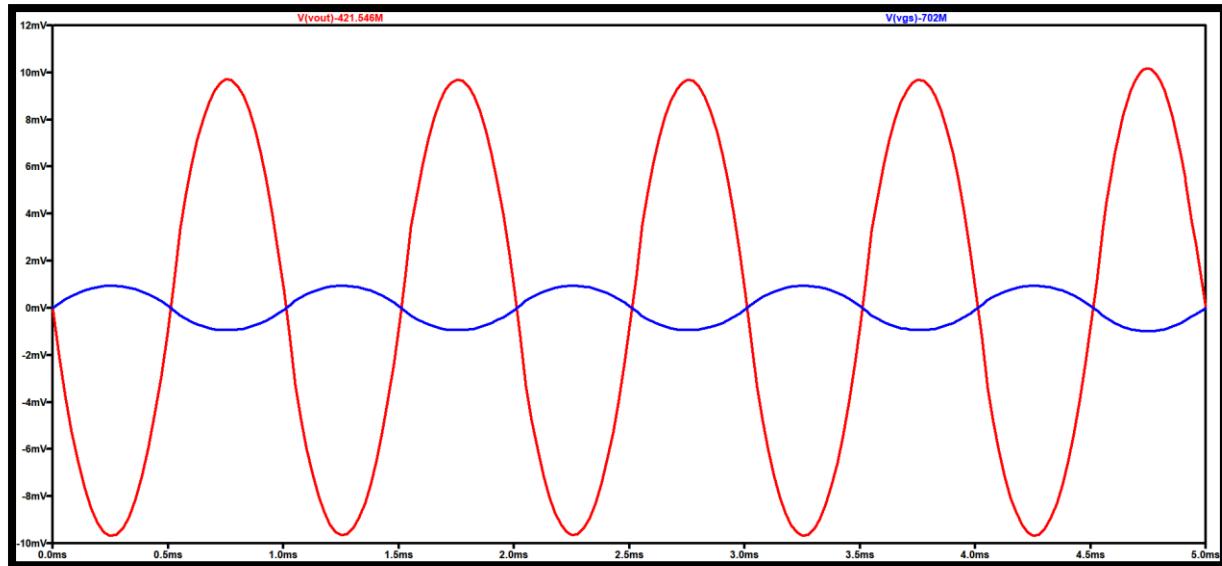


Figure 8: TRANSIENT ANALYSIS IN LT SPICE

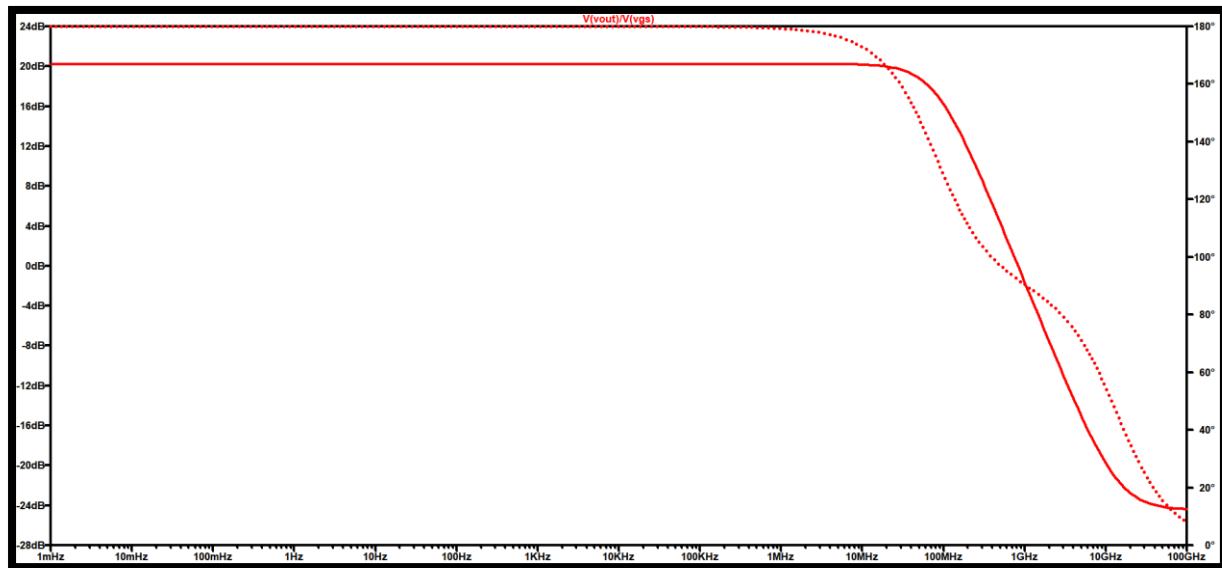


Figure 9: FREQUENCY RESPONSE IN LT SPICE

SIMULATION RESULTS
GBW=837MHz
CL=5pF
Gain=10.2

## DESIGN OF COMMON SOURCE AMPLIFIER USING PMOS AND RESISTIVE LOAD

The Model file used is tsmc180.txt

SPECIFICATIONS
GBW=800MHz
CL=5pF
Gain = 10

### CALCULATIONS

#### CALCULATIONS

GBW=800MHz, L=0.36u, Vs=1.8V, Model file = 180n

Let GAIN (A) = 10

$$f(-3\text{db}) = \frac{GBW}{Gain} = 80\text{MHz} \quad \text{let } C_L = 5\text{pF}$$

$$\text{USING } f(-3\text{db}) = \frac{1}{2\pi R_{out} C_L} \quad R_{out} = 397.88 \text{ ohm}$$

Now, GAIN (A) = Gm Rout    Gm=25.1 mS

Now, Let Gm/Id = 10.2                  Id = 2.46 mA

(From NMOS Parameter Charts)

Gm/Gds = 72.2                  Gds=347.64 uS

AS      Ro=1/Gds,                  Ro=2876.5 ohm

(From NMOS Parameter Charts)

Id/W= 3.3                  W=745u

$$\text{Now } R_{out} = R_o \parallel R_L \quad R_L = \frac{R_o * R_{out}}{(R_o - R_{out})} \quad R_L = 461.75 \text{ ohms}$$

Now, Vgs is calculated from Gm/Id vs Vgs Curve in LT Spice

For, Gm/Id = 10.2

Vg = 1.1V

## SCHEMATIC

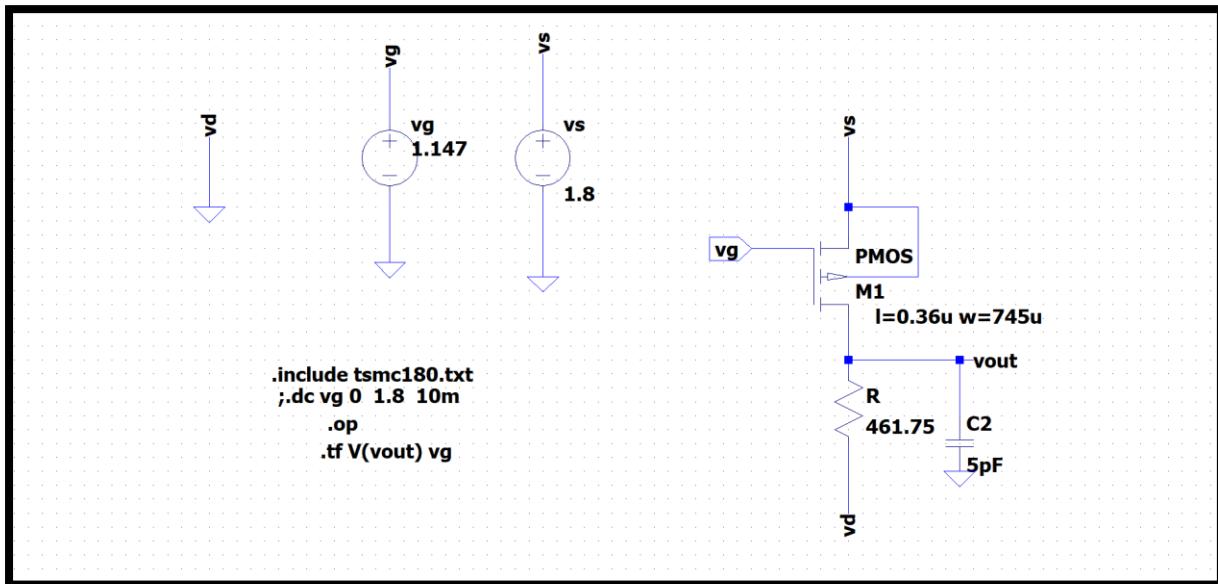


Figure 10

## SIMULATIONS

```

--- Operating Point ---

V(vg) : 1.147      voltage
V(vs) : 1.8      voltage
V(vout) : 1.16995      voltage
Id(M1) : -0.00253372      device_current
Ig(M1) : -0      device_current
Ib(M1) : 6.40054e-013      device_current
Is(M1) : 0.00253372      device_current
I(C2) : 5.84973e-024      device_current
I(R) : 0.00253372      device_current
I(Vs) : -0.00253372      device_current
I(Vg) : 0      device_current

```

```

--- Transfer Function ---

Transfer_function: -10.7566      transfer
vg#Input_impedance: 1e+020      impedance
output_impedance_at_V(vout): 416.704      impedance

```

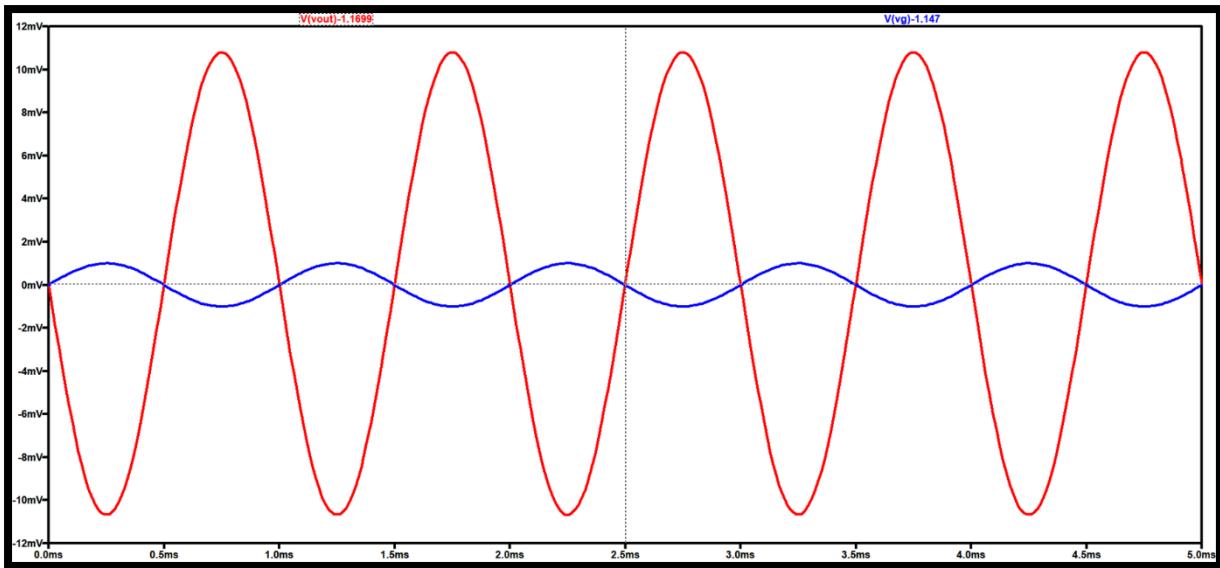


Figure 11: TRANSIENT ANALYSIS IN LT SPICE

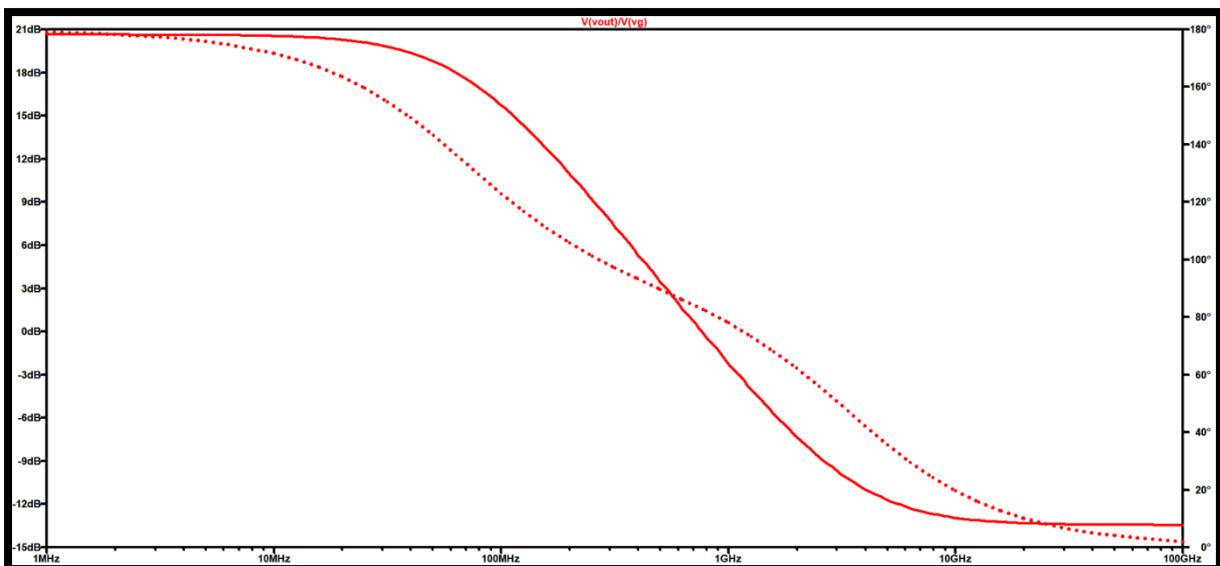


Figure 12: FREQUENCY RESPONSE IN LT SPICE

<b>SIMULATION RESULTS</b>	
GBW=763MHz	
CL=5pF	
Gain=10.756	

## **FEEDBACK AFTER WEEK 1 DESIGN PRESENTATION**

The Specifications are not exactly matching with simulations, W/L ratio is very high, so now a Design Constraint is Introduced: Optimizing W/L ratio

## **WEEK 2: ANALOG DESIGN INTERNSHIP**

### **REDESIGN OF COMMON SOURCE AMPLIFIER USING NMOS AND RESISTIVE LOAD**

The Model file used is tsmc180.txt

SPECIFICATIONS
GBW=800MHz
CL=5pF
Gain = 10

## **CALCULATIONS**

GBW=800MHz, L=0.36u, Vdd=1.8V, Model file = 180n

Let GAIN (A) = 10

$$f(-3\text{db}) = \frac{GBW}{Gain} = 80\text{MHz} \quad \text{LET } Gm=2\text{mS} \text{ (Practical value range 1-3 S given by Javed Sir)}$$

$$\text{USING } C_L = \frac{Gm}{2\pi GBW} \quad C_L = 0.397\text{pF} \text{ (assume 0.3pF)}$$

Now by Back calculation,

$$Gm = 2\pi GBW C_L = 1.5\text{mS}$$

$$\text{Assume } V_{ov}=0.2\text{V} \quad V_{gs}=0.65\text{V} \quad I_d = \frac{Gm V_{ov}}{2} = 150\text{uA}$$

Then,  $Gm/I_d = 10$

$$R = (1.8 - 0.9)/150\text{uA} = 6 \text{Khom}$$

W is calculated by sweeping for 150uA current

## SCHEMATIC

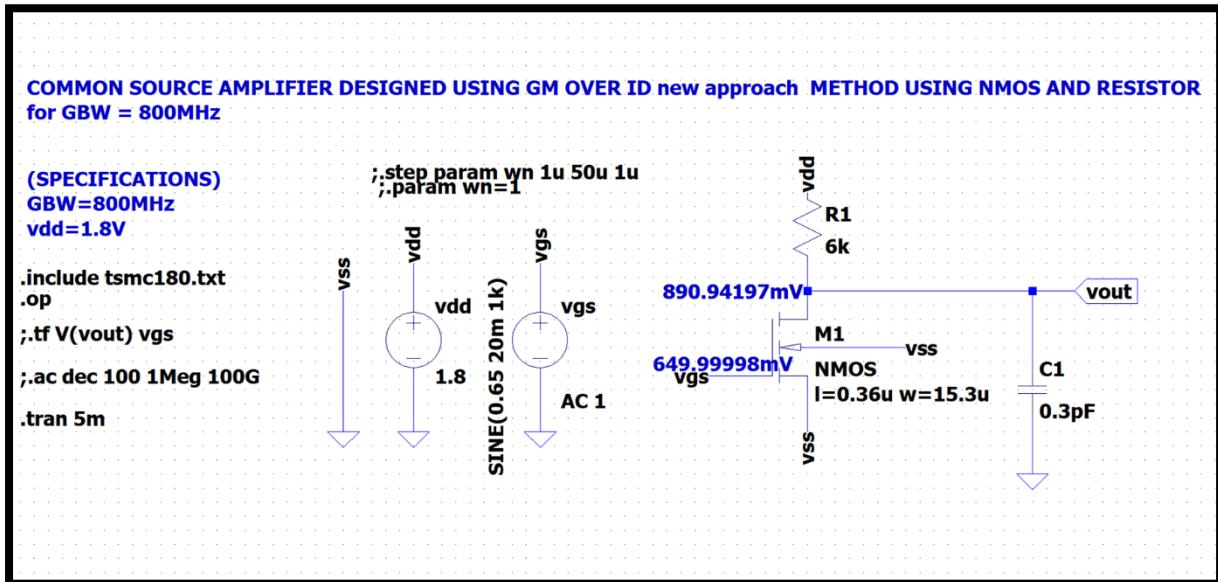


Figure 13

## SIMULATIONS

```
--- Operating Point ---

vout) : 0.890942      voltage
vgs) : 0.65           voltage
vdd) : 1.8            voltage
(M1) : 0.00015151    device_current
(M1) : 0              device_current
(M1) : -9.00942e-013 device_current
(M1) : -0.00015151   device_current
C1) : 2.67283e-025   device_current
R1) : 0.00015151     device_current
Vgs) : 0              device_current
Vdd) : -0.00015151   device_current
```

```
--- Transfer Function ---

Transfer_function:      -10.0208      transfer
vgs#Input_impedance:    1e+020       impedance
output_impedance_at_V(vout): 5453.14  impedance
```

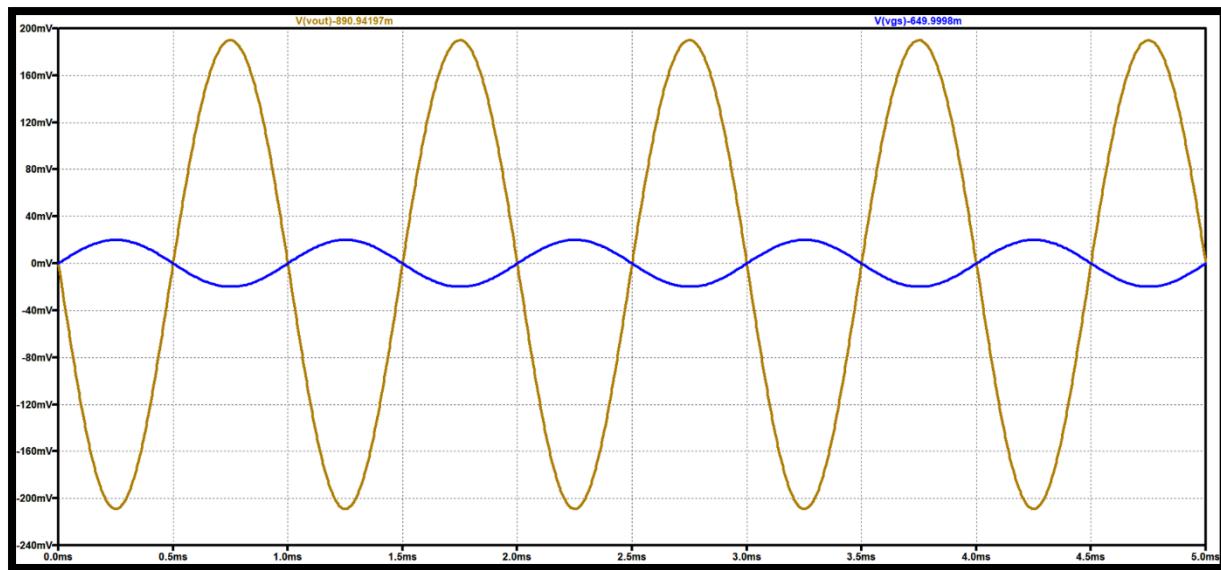


Figure 14 : TRANSIENT ANALYSIS IN LT SPICE

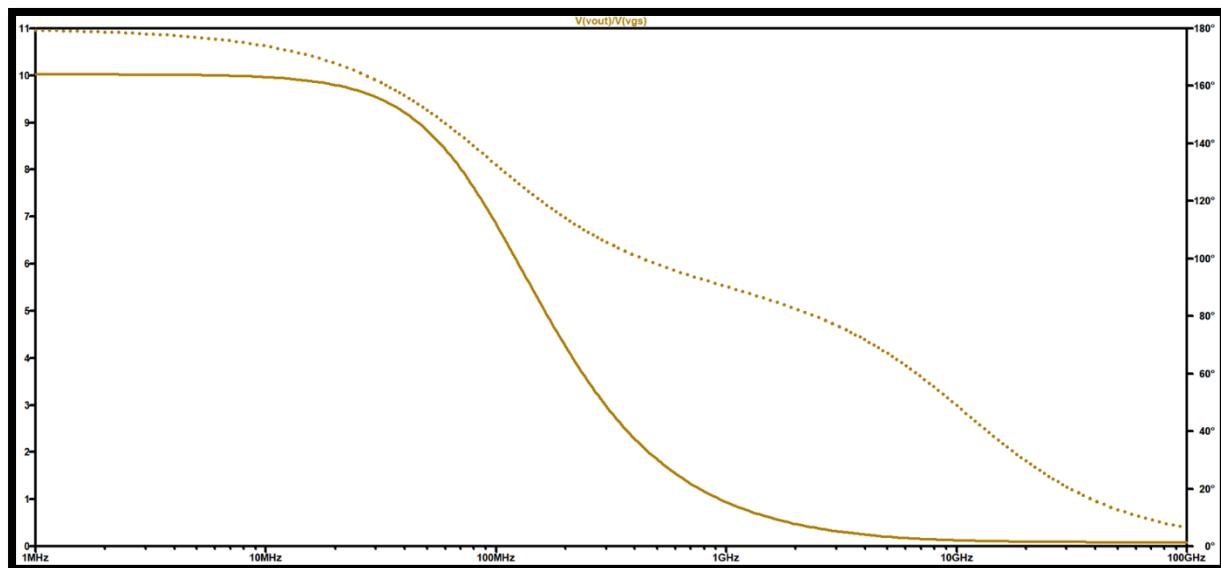


Figure 15: FREQUENCY RESPONSE IN LT SPICE

SIMULATION RESULTS
CL=5pF
Gain=10.02

## COMMON SOURCE AMPLIFIER USING NMOS AND CURRENT SOURCE LOAD

The Model file used is tsmc180.txt

**DESIGN CONSTRAINT:** Design should have optimized W/L ratio

SPECIFICATIONS
GBW=1GHz
Gain = 10 At 100MHz

### **CALCULATIONS**

GBW=1GHz, Gain = 10 at 100MHz

LET  $Gm=2mS$  (Practical value range 1-3 S given by Javed Sir)

$$\text{USING } C_L = \frac{Gm}{2\pi GBW} \quad C_L = 0.318\text{pF} \text{ (assume } 0.3\text{pF)}$$

Now by Back calculation,

$$Gm = 2\pi GBW C_L = 1.884\text{mS}$$

$$(\text{For nmos}) V_{ov}=0.2V \quad V_{gs}=0.65V \quad I_d = \frac{Gm V_{ov}}{2} = 188\mu A$$

$$\text{Then, } Gm/I_d = 10.021 \quad I_d/W = 13.6$$

$$W=14\mu$$

$$(\text{For pmos}) V_g=1.1V$$

Width of PMOS is taken twice as that of nmos

$$W=28\mu$$

**NOTE:** Now some manipulations are done in calculations to meet the specifications

## SCHEMATIC

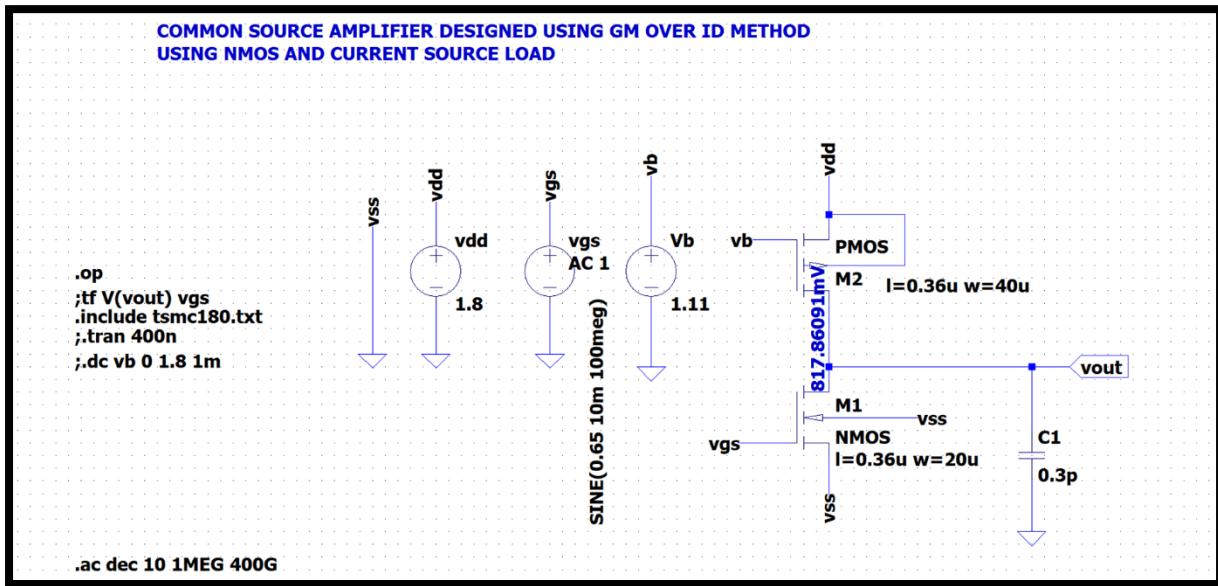


Figure 16

## SIMULATIONS

```

--- Operating Point ---

V(vout) : 0.817861      voltage
V(vgs) : 0.65            voltage
V(vdd) : 1.8              voltage
V(vb) : 1.11             voltage
Id(M2) : -0.000197001   device_current
Ig(M2) : -0                device_current
Ib(M2) : 9.92139e-013    device_current
Is(M2) : 0.000197001    device_current
Id(M1) : 0.000197001    device_current
Ig(M1) : 0                device_current
Ib(M1) : -8.27861e-013   device_current
Is(M1) : -0.000197001   device_current
I(C1) : 2.45358e-025    device_current
I(Vb) : 0                device_current
I(Vdd) : -0.000197001   device_current

```

```

--- Transfer Function ---

Transfer_function: -61.0818      transfer
vgs#Input_impedance: 1e+020       impedance
output_impedance_at_V(vout): 25549.1 impedance

```

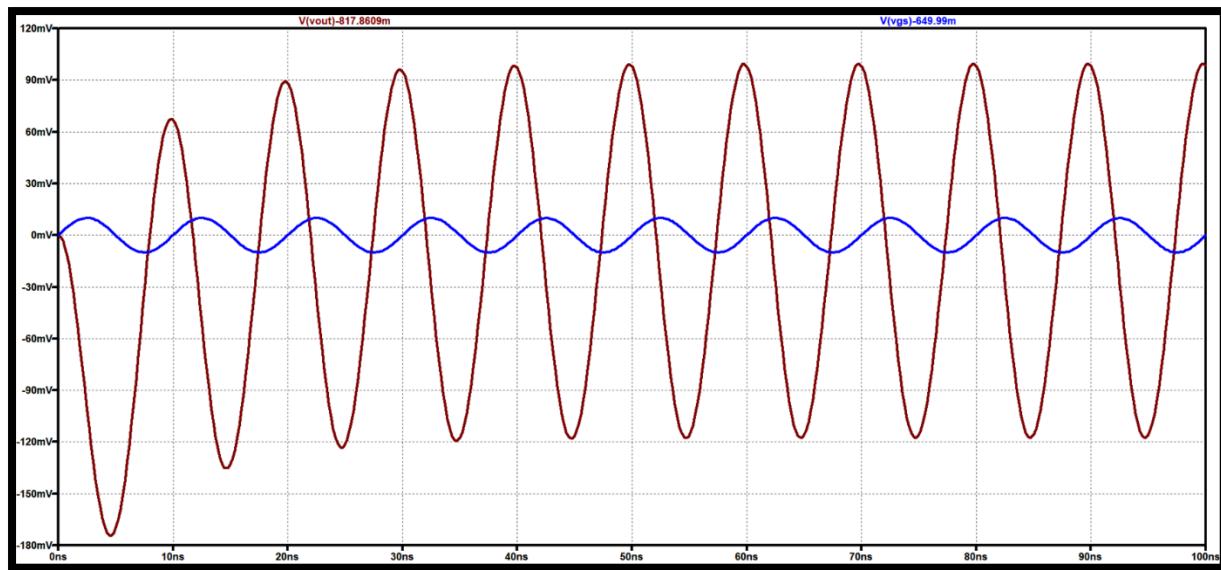


Figure 17: TRANSIENT ANALYSIS IN LT SPICE

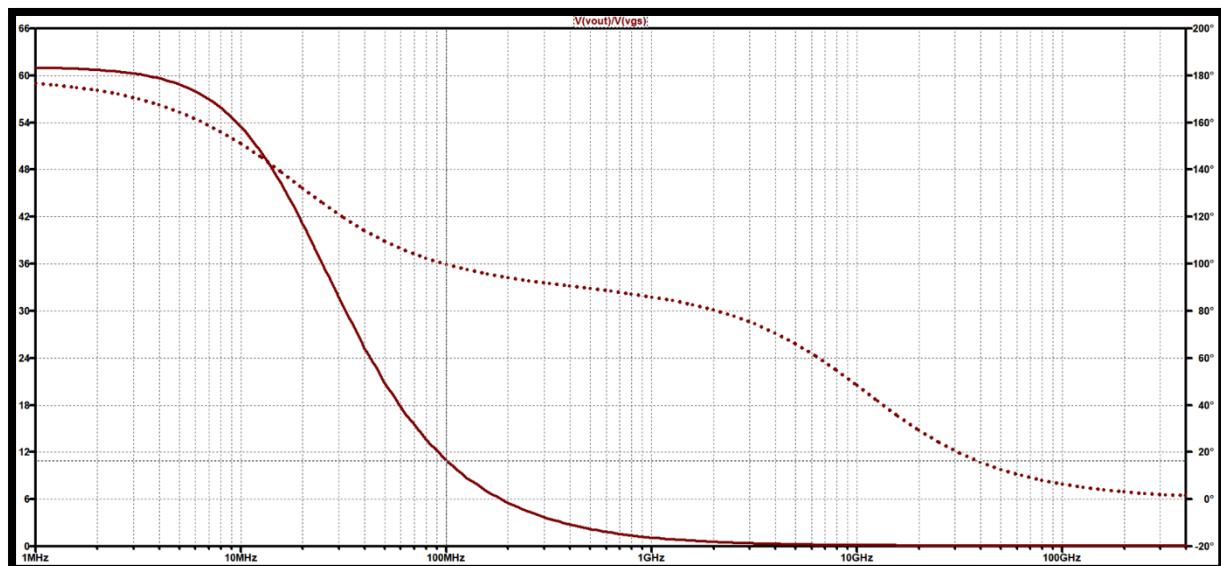


Figure 18: FREQUENCY RESPONSE IN LT SPICE

SIMULATION RESULTS
GBW=1GHz
Gain=10.88 at 100MHz

## DESIGN OF SIMPLE CURRENT MIRROR

The Model file used is tsmc180.txt

**DESIGN CONSTRAINT:** Design should have optimized W/L ratio

SPECIFICATIONS
Iref=52.4u
Iout=524u

## SCHEMATIC

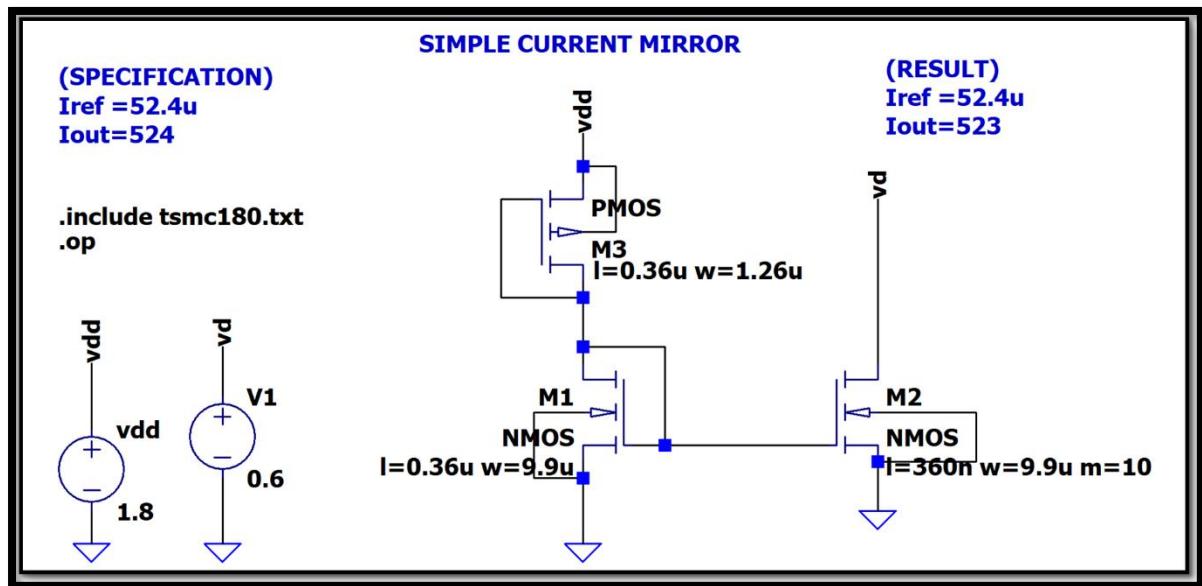


Figure 19

## SIMULATIONS

Semiconductor Device Operating Points:			
--- BSIM3 MOSFETS ---			
Name:	m3	m2	m1
Model:	pmos	nmos	nmos
<b>Id:</b>	<b>-5.24e-05</b>	<b>5.23e-04</b>	<b>5.24e-05</b>
Vgs:	-1.19e+00	6.07e-01	6.07e-01
Vds:	-1.19e+00	6.00e-01	6.07e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00
Vth:	-4.68e-01	4.66e-01	4.66e-01
Vdsat:	-5.47e-01	1.10e-01	1.10e-01
Gm:	1.24e-04	8.10e-03	8.11e-04
Gds:	3.75e-06	7.59e-05	7.57e-06
Gmb:	4.07e-05	2.14e-03	2.14e-04
Cbd:	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00

SIMULATION RESULTS
Iref=52.4u
Iout=523u

## DESIGN OF DIFFERENTIAL PAIR

The Model file used is tsmc180.txt

**DESIGN CONSTRAINT:** Design should have optimized W/L ratio

SPECIFICATIONS
GBW=1GHz
Gain = 10 At 100MHz

## **SCHEMATIC**

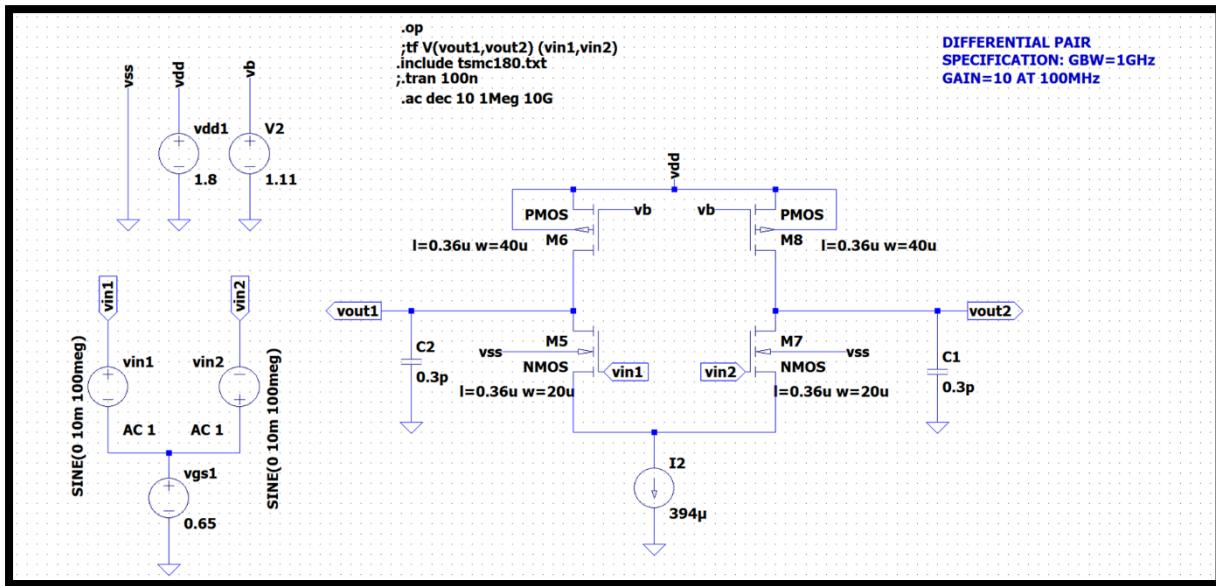


Figure 20

## **SIMULATIONS**

```

    Device Operating Points:
    --- BSIM3 MOSFETS ---
      m8       m6       m7       m5
      pmos     pmos     nmos     nmos
-1.97e-04 -1.97e-04 1.97e-04 1.97e-04
-6.90e-01 -6.90e-01 6.50e-01 6.50e-01
-9.82e-01 -9.82e-01 8.18e-01 8.18e-01
 0.00e+00  0.00e+00 -8.44e-07 -8.44e-07
-4.73e-01 -4.73e-01 4.65e-01 4.65e-01
-1.94e-01 -1.94e-01 1.41e-01 1.41e-01
 1.68e-03  1.68e-03 2.39e-03 2.39e-03
 1.69e-05  1.69e-05 2.22e-05 2.22e-05
 5.39e-04  5.39e-04 6.26e-04 6.26e-04
 0.00e+00  0.00e+00 0.00e+00 0.00e+00
 0.00e+00  0.00e+00 0.00e+00 0.00e+00
 2.84e-14  2.84e-14 1.54e-14 1.54e-14
 2.84e-14  2.84e-14 1.54e-14 1.54e-14
 3.11e-19  3.11e-19 3.33e-19 3.33e-19

```

### --- Transfer Function ---

```
Transfer_function: -61.0825 transfer
vin1#Input_impedance: 1e+020 impedance
output impedance at V(vout1,vout2): 51098.9 impedance
```

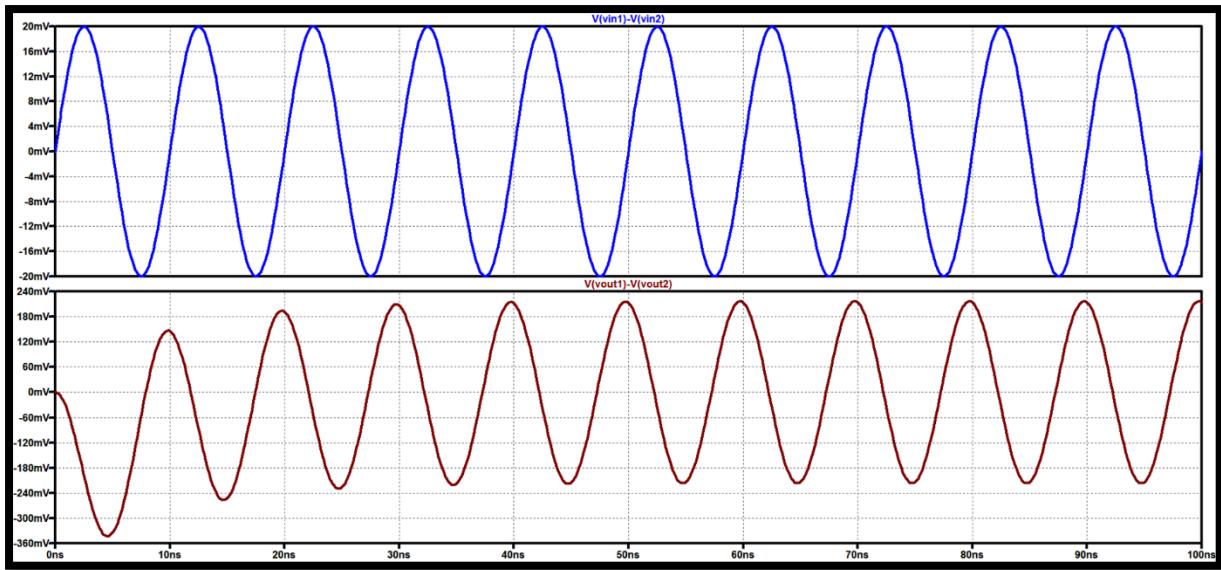
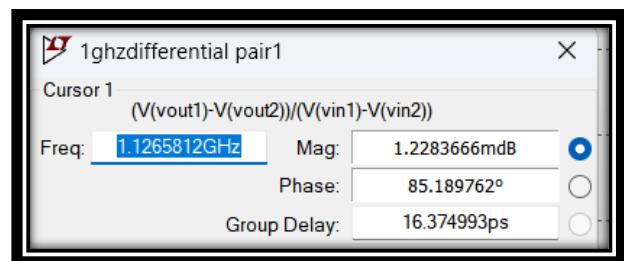
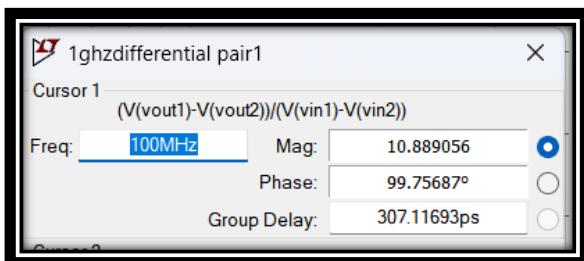


Figure 21: TRANSIENT ANALYSIS IN LT SPICE

If 10mV signal is given at 100MHz then we can observe from here Gain is nearly 10



Figure 22: FREQUENCY RESPONSE IN LT SPICE



SIMULATION RESULTS
GBW=1.12GHz
Gain=10.88 at 100MHz

### SCHEMATIC (IDEAL CURRENT SOURCE REPLACED WITH TRANSISTOR)

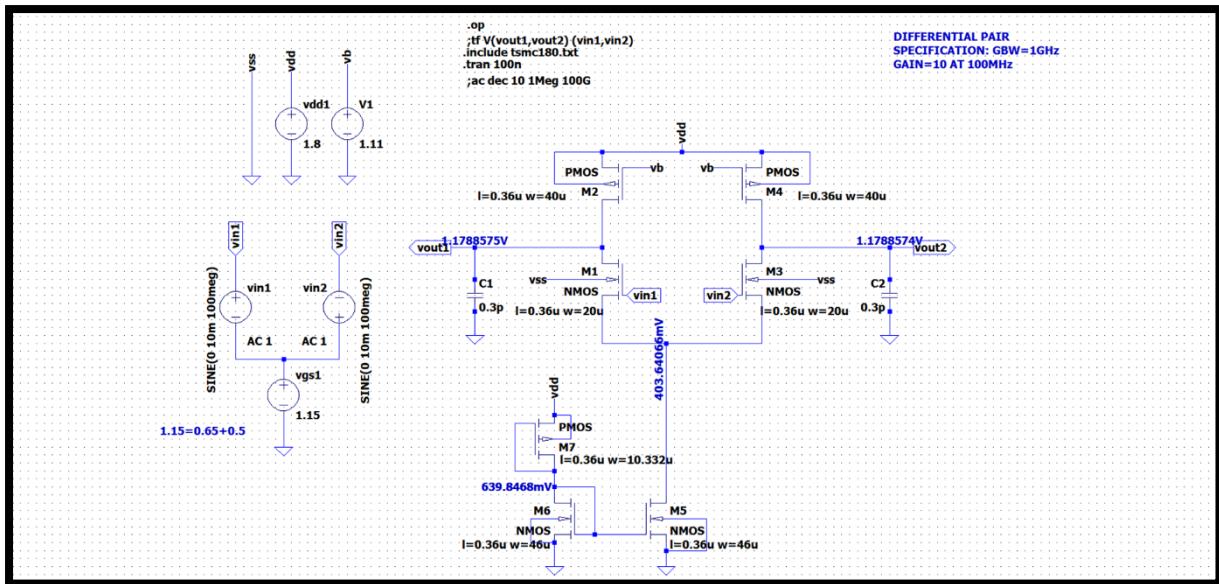


Figure 23

### SIMULATIONS

```

Transfer_function:          -58.179      transfer
vin1#Input_impedance:     1e+020      impedance
output_impedance_at_V(vout1,vout2): 49365      impedance

```

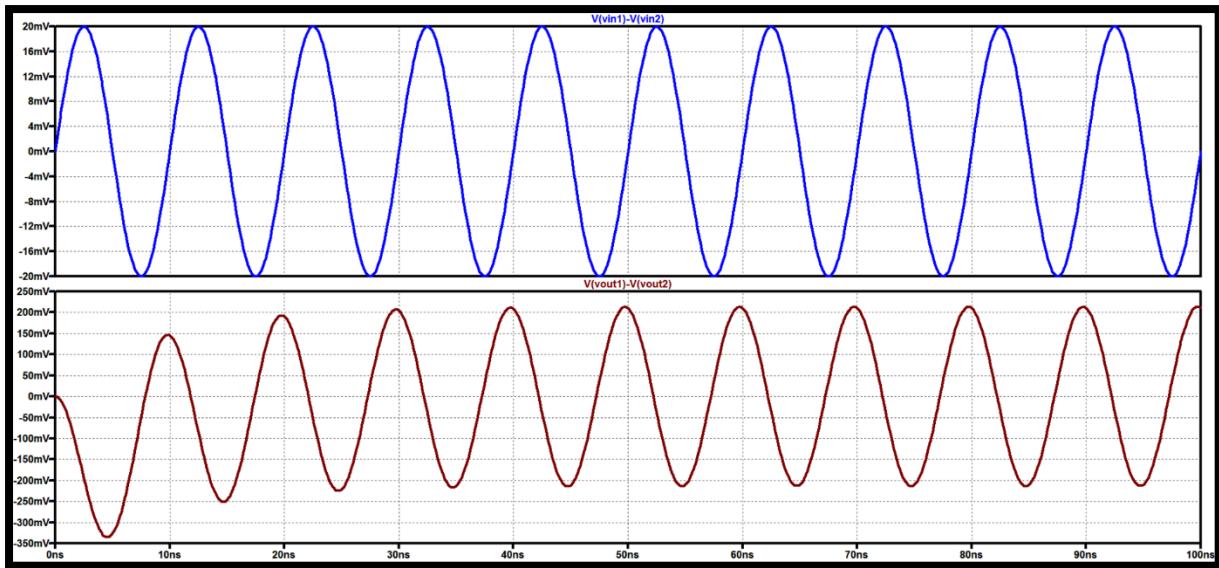


Figure 24: TRANSIENT ANALYSIS IN LT SPICE

If 10mV signal is given at 100MHz then we can observe from here Gain is nearly 10

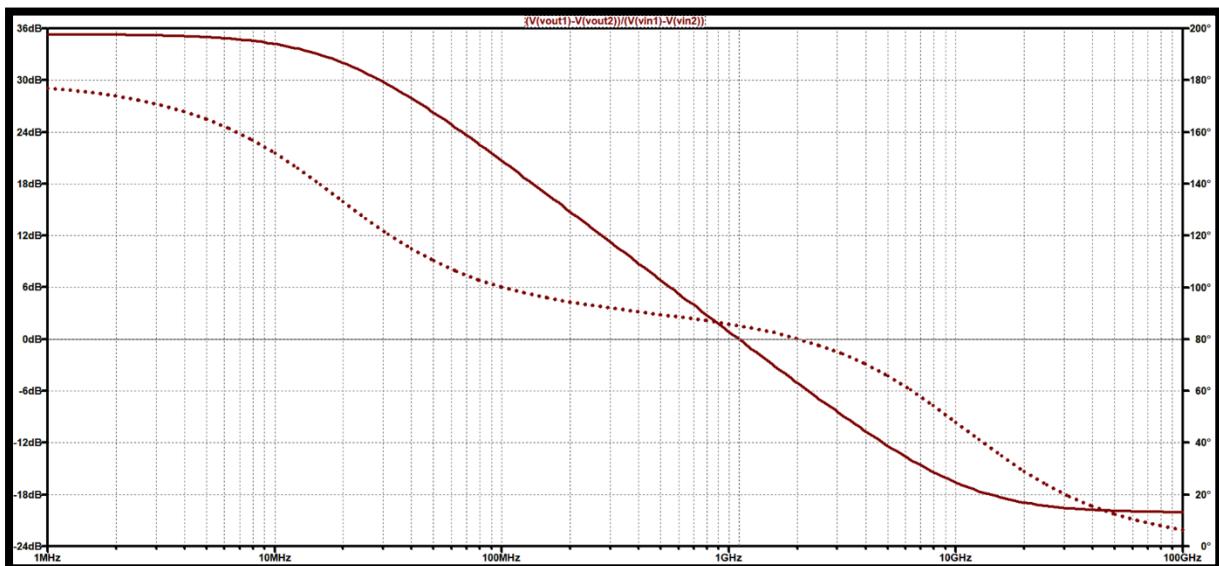
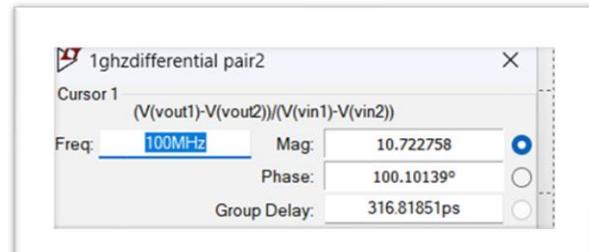
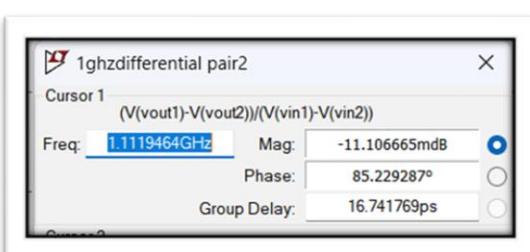


Figure 25: FREQUENCY RESPONSE IN LT SPICE



SIMULATION RESULTS
GBW=1.119GHz
Gain=10.722 at 100MHz

### **AFTER WEEK 2 NEW DESIGN CONSTRAINT INTRODUCED**

Now, The Design Constraints are Optimizing W/L ratio and using Unit Devices

## WEEK 3: ANALOG DESIGN INTERNSHIP

### DESIGN OF SIMPLE CURRENT MIRROR

The Model file used is tsmc180.txt

**DESIGN CONSTRAINT:** Design should have optimized W/L ratio , and use Unit Devices

SPECIFICATIONS
Iref=50u
Iout=500u

### SCHEMATIC

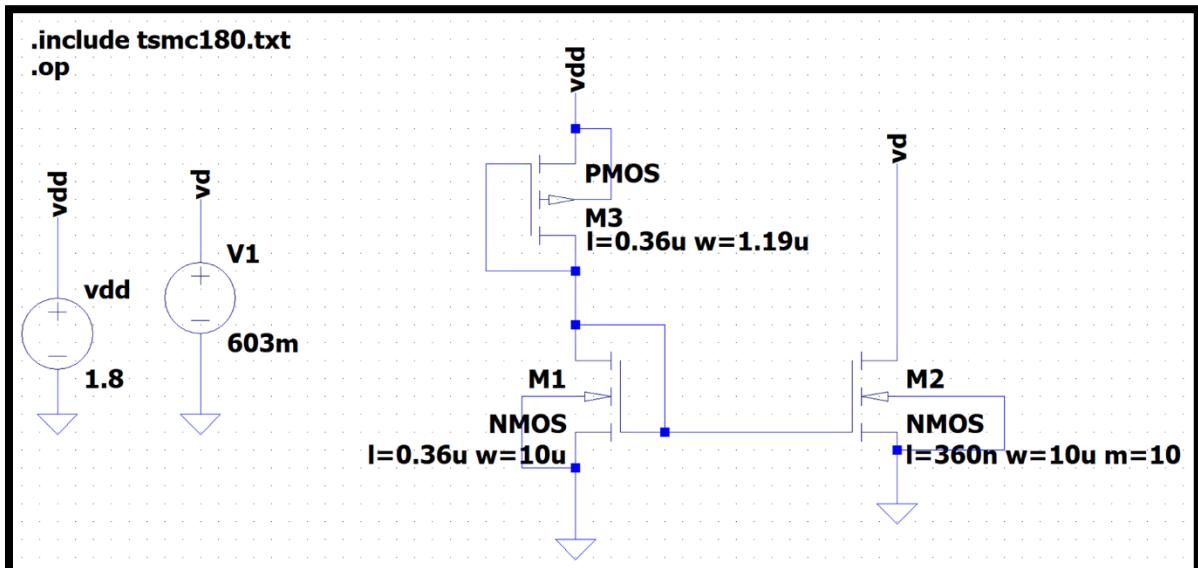


Figure 26

### SIMULATIONS

--- BSIM3 MOSFETS ---		
Name:	m3	m2
Model:	pmos	nmos
<b>Id:</b>	<b>-5.00e-05</b>	<b>5.00e-04</b>
Vgs:	-1.20e+00	6.04e-01
Vds:	-1.20e+00	6.03e-01
Vbs:	0.00e+00	0.00e+00
Vth:	-4.67e-01	4.66e-01
Vdsat:	-5.49e-01	1.08e-01
Gm:	1.18e-04	7.89e-03

<b>SIMULATION RESULTS</b>
Iref=50u
Iout=500u

## **DESIGN OF DIFFERENTIAL PAIR**

The Model file used is tsmc180.txt

**DESIGN CONSTRAINT:** Design should have optimized W/L ratio & using Unit Devices

<b>SPECIFICATIONS</b>
GBW=1GHz
Gain = 10 At 100MHz

## **SCHEMATIC**

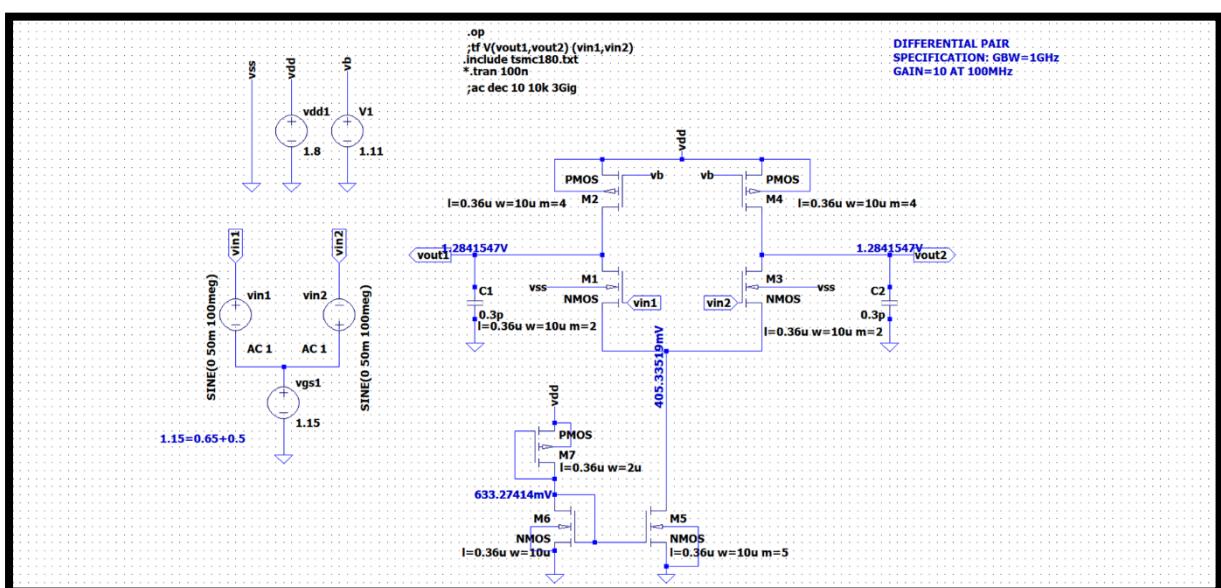


Figure 27

## SIMULATIONS

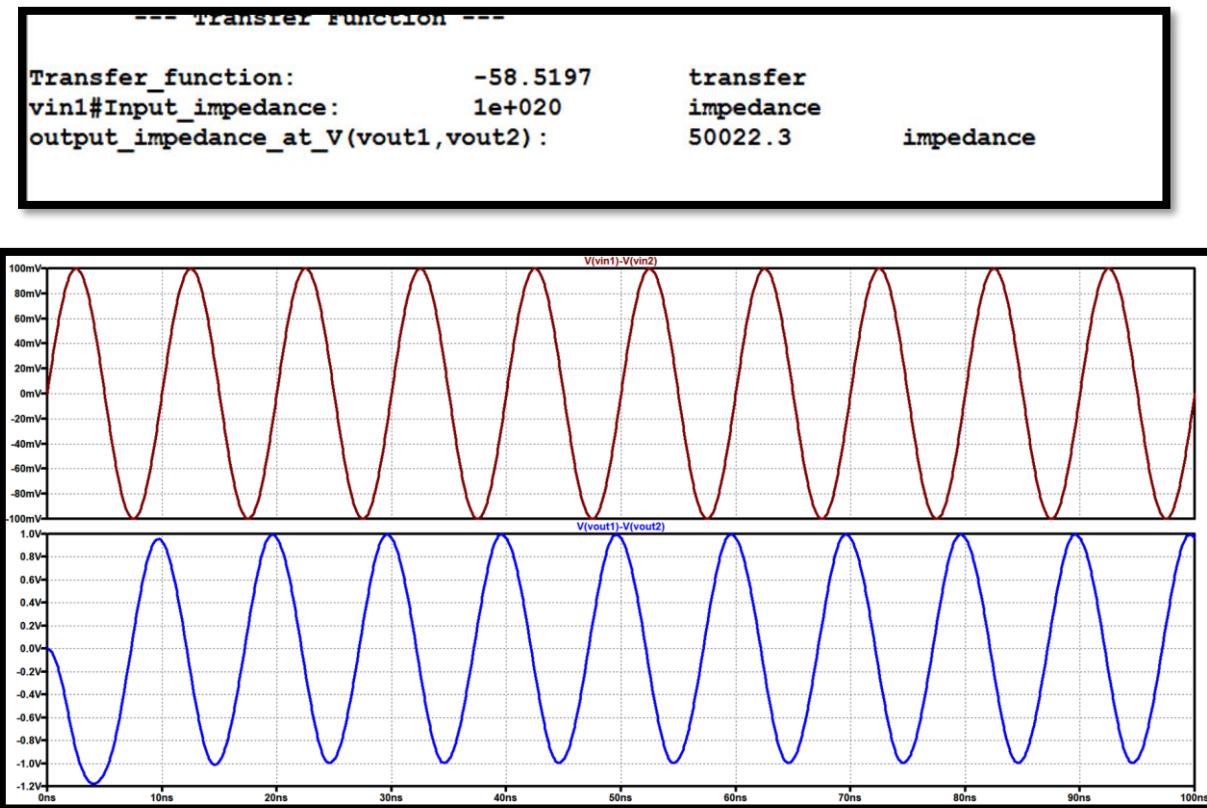


Figure 28: TRANSIENT ANALYSIS IN LT SPICE

If 10mV signal is given at 100MHz then we can observe from here Gain is nearly 10

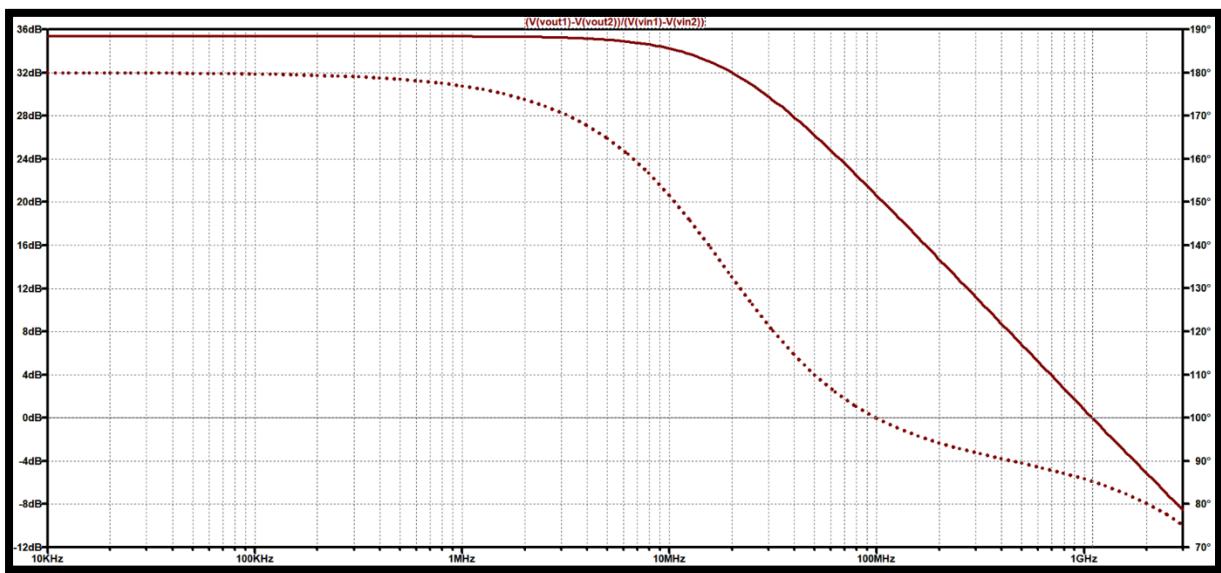
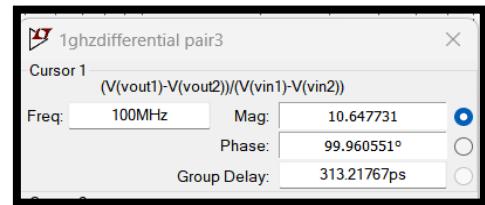
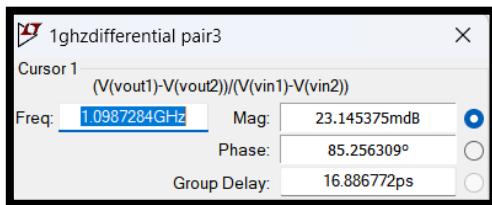


Figure 29: FREQUENCY RESPONSE IN LT SPICE



### SIMULATION RESULTS

GBW=1.098GHz

Gain=10.647 at 100MHz

## **WEEK 4: ANALOG DESIGN INTERNSHIP**

## **DESIGN OF SINGLE STAGE OPAMP**

The Model file used is tsmc180.txt

**DESIGN CONSTRAINT:** Design should have optimized W/L ratio, and use Unit Devices

# SPECIFICATIONS

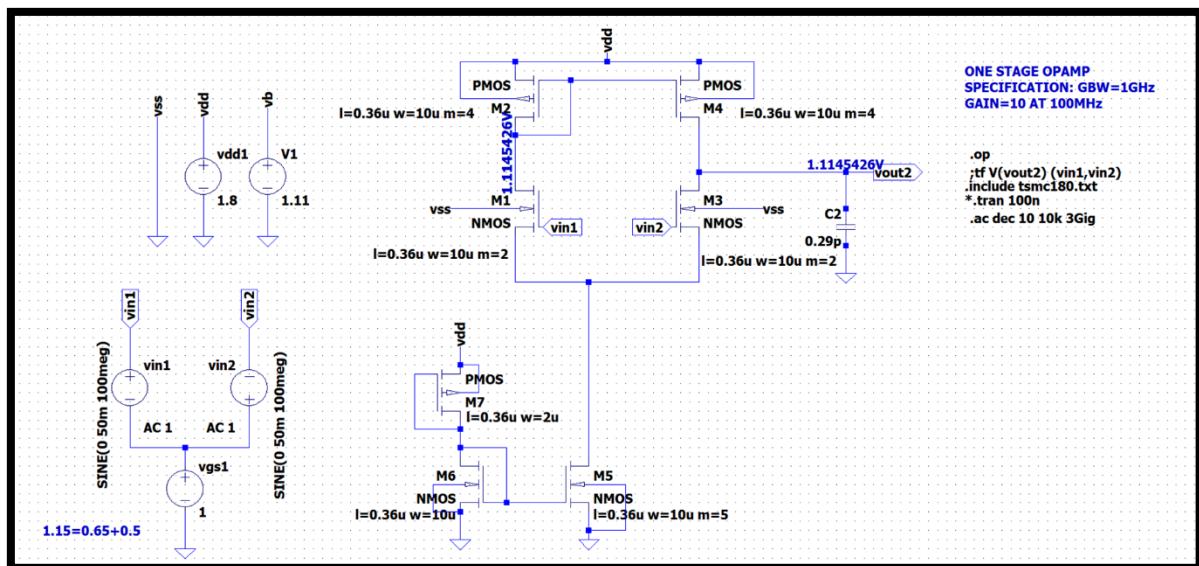
---

GBW=1GHz

---

Gain = 10 At 100MHz

## **SCHEMATIC**



*Figure 30*

## **SIMULATIONS**

```
Transfer_function:          60.0541      transfer
vin1#Input_impedance:     1e+020       impedance
output impedance at V(vout2): 26348.2      impedance
```

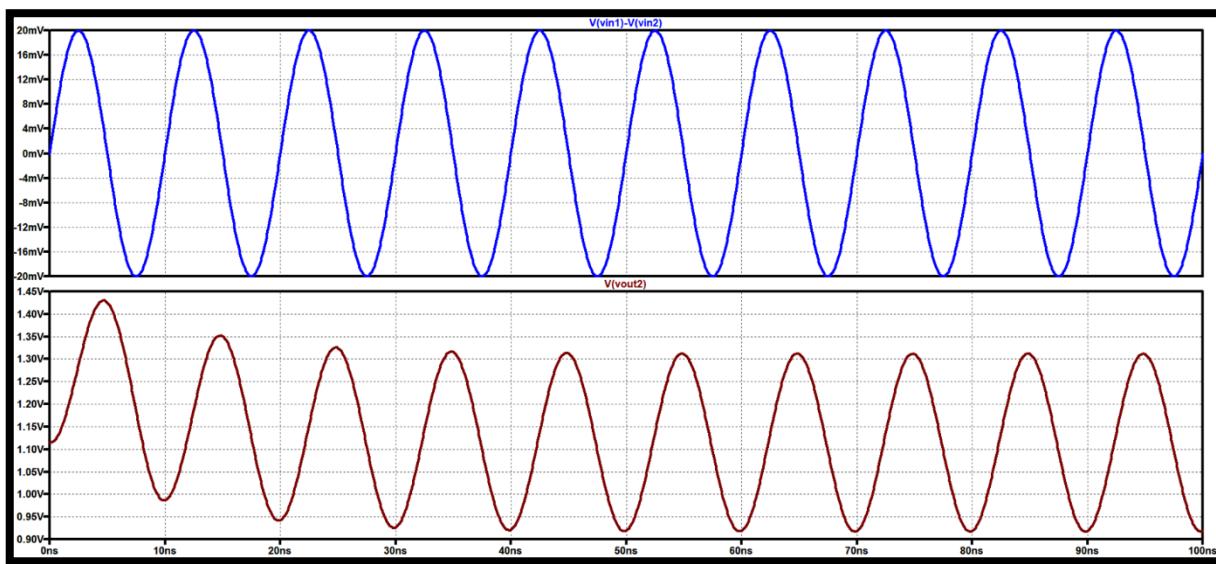


Figure 31: TRANSIENT ANALYSIS IN LT SPICE

If 10mV signal is given at 100MHz then by measuring peak to peak voltages we can observe from here Gain is nearly 9.9

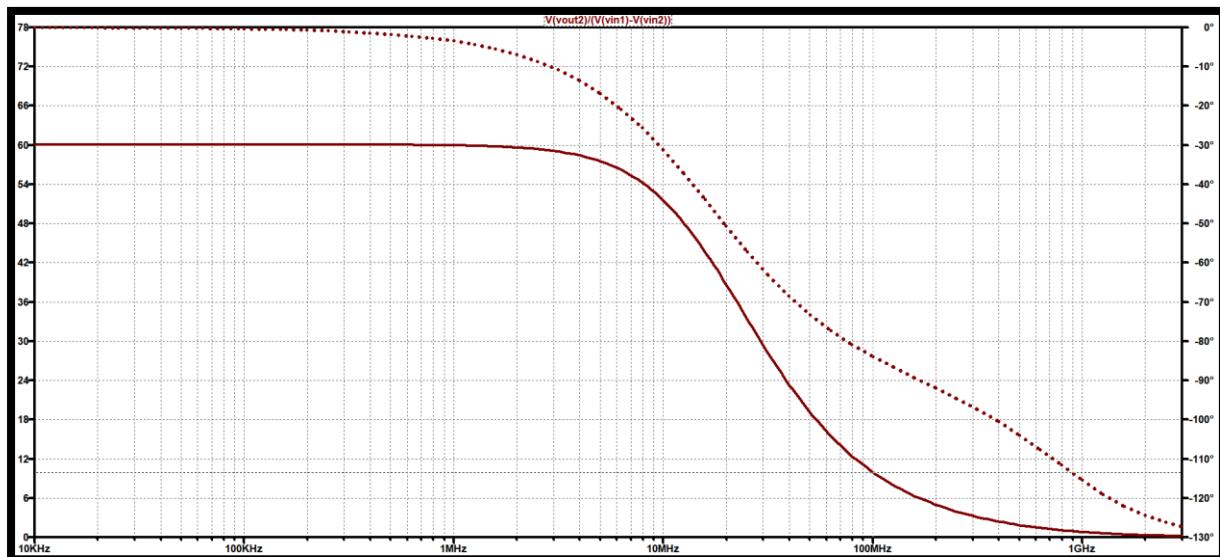
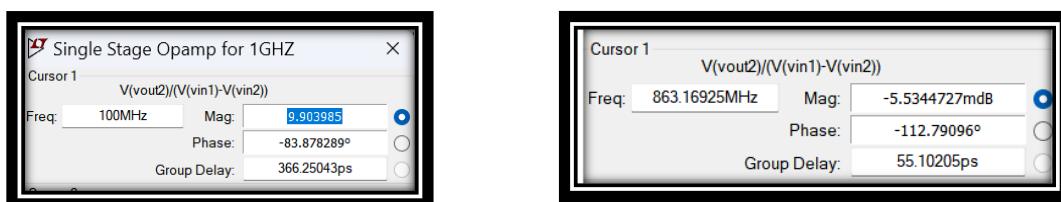


Figure 10



SIMULATIONS RESULT
GBW=863MHz
Gain = 9.9 At 100MHz

## COMMON SOURCE AMPLIFIER USING PMOS AND CURRENT SOURCE LOAD

The Model file used is tsmc180.txt

**DESIGN CONSTRAINT:** Design should have optimized W/L ratio & use Unit Devices Method

SPECIFICATIONS
GBW=1GHz
Gain = 10 At 100MHz

## CALCULATIONS

GBW=1GHz, Gain = 10 at 100MHz

LET  $Gm=2mS$  (Practical value range 1-3 S given by Javed Sir)

$$\text{USING } C_L = \frac{Gm}{2\pi GBW} \quad C_L = 0.318\text{pF} \text{ (assume } 0.3\text{pF)}$$

Now by Back calculation,

$$Gm = 2\pi GBW C_L = 1.884\text{mS}$$

(For PMOS)

$$V_{ov} = V_{sg} - |V_t| = 1.8 - 1.1145 - 0.44 \quad V_{ov} = 0.2355\text{V} \quad I_d = \frac{Gm V_{ov}}{2} = 221.8\mu\text{A}$$

$$\text{Then, } Gm/I_d = 8.49 \quad I_d/W = 4.71 \quad W = 47\mu\text{m}$$

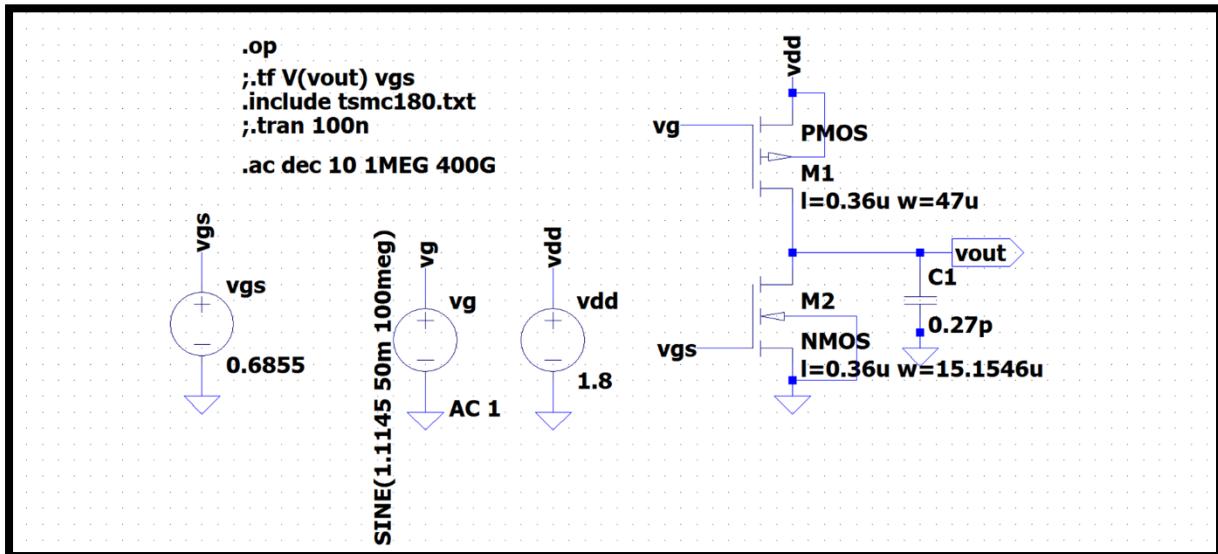
(For NMOS)

$$V_{gs} = 0.2355 + 0.45\text{V} = 0.6855$$

Width of NMOS is taken by sweeping method

$$W = 15.1546\mu\text{m}$$

## **SCHEMATIC**



*Figure 33*

## **SIMULATIONS**

V(vout) :	0.885755	voltage
V(vg) :	1.1145	voltage
V(vdd) :	1.8	voltage
V(vgs) :	0.6855	voltage
Id(M2) :	0.000221557	device_current
Ig(M2) :	0	device_current
Ib(M2) :	-8.95755e-013	device_current
Is(M2) :	-0.000221557	device_current
Id(M1) :	-0.000221557	device_current
Ig(M1) :	-0	device_current
Ib(M1) :	9.24245e-013	device_current
Is(M1) :	0.000221557	device_current
I(C1) :	2.65727e-025	device_current
I(Vgs) :	0	device_current
I(Vg) :	0	device_current
I(Vdd) :	-0.000221557	device_current

```
--- Transfer Function ---  
  
Transfer_function:      -53.6958      transfer  
vgs#Input_impedance:    1e+020       impedance  
output_impedance_at_V(vout): 24403.3   impedance
```

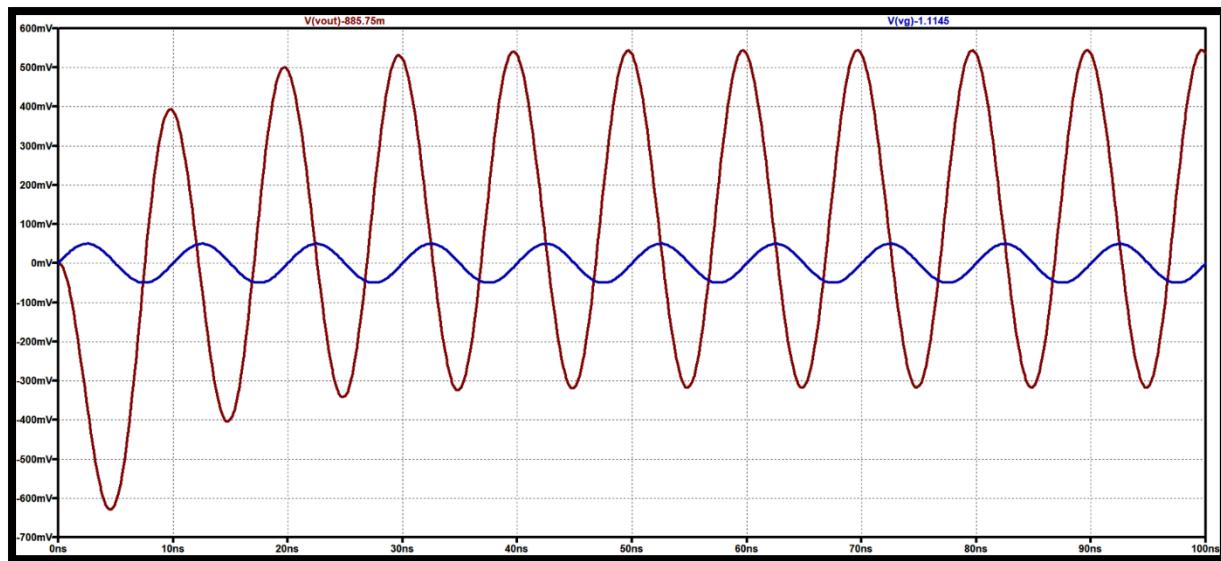


Figure 34: TRANSIENT ANALYSIS IN LT SPICE



Figure 35: FREQUENCY RESPONSE IN LT SPICE

SIMULATION RESULTS
GBW=1GHz
Gain=9.54 at 100MHz

## DESIGN OF TWO STAGE OPAMP

The Model file used is tsmc180.txt

**DESIGN CONSTRAINT:** Design should have optimized W/L ratio, and use Unit Devices

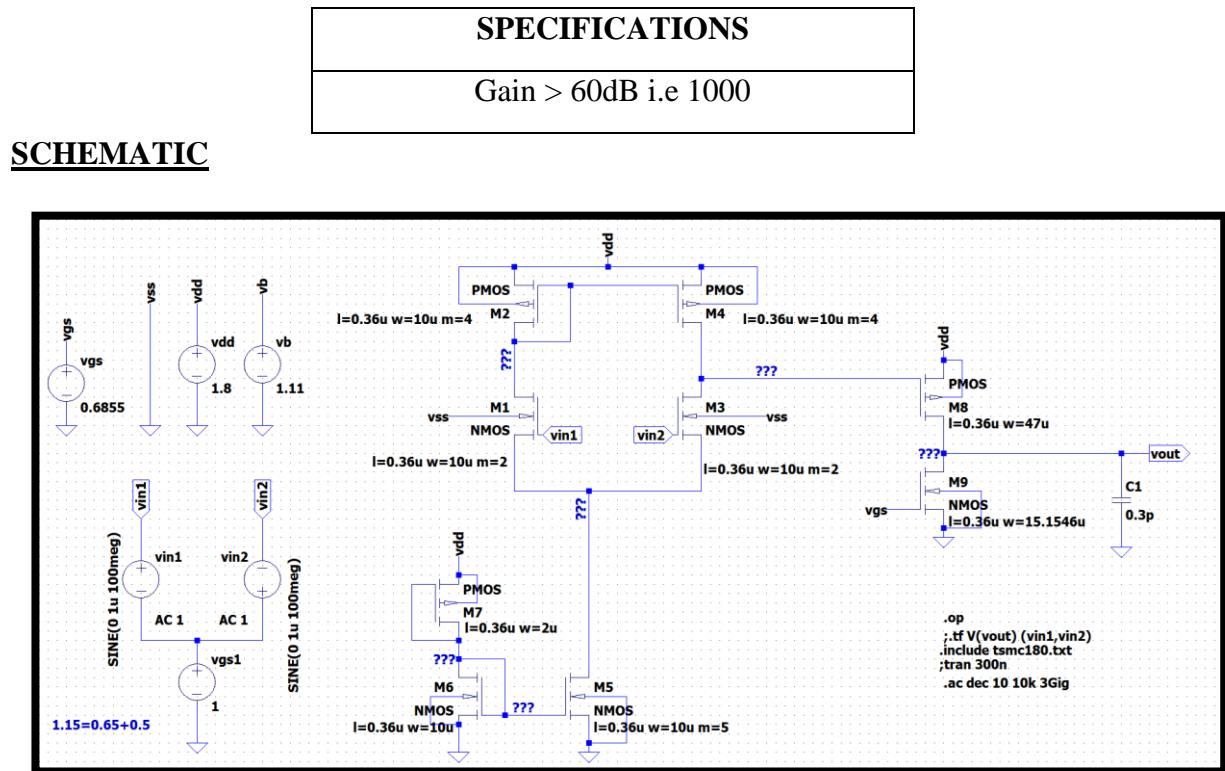


Figure 36

## SIMULATIONS

Transfer_function:	-2828.25	transfer
vin1#Input_impedance:	1e+020	impedance
output_impedance_at_V(vout):	24401.6	impedance

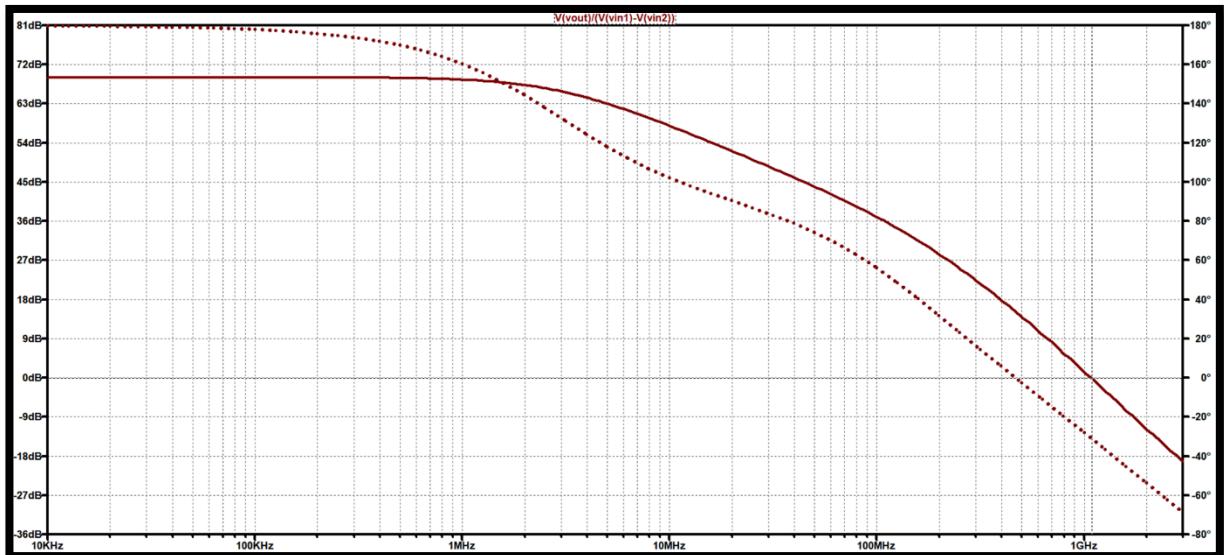


Figure 37: Frequency Response

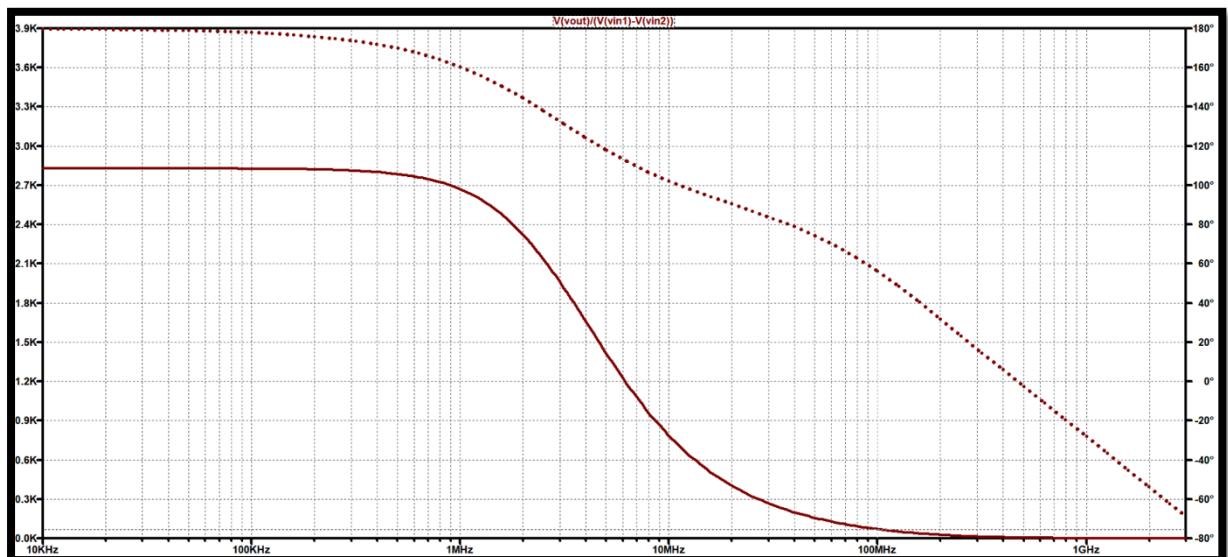
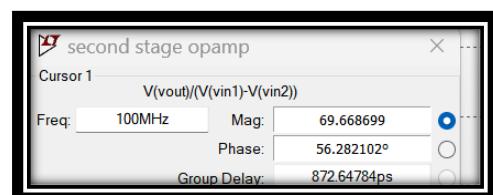
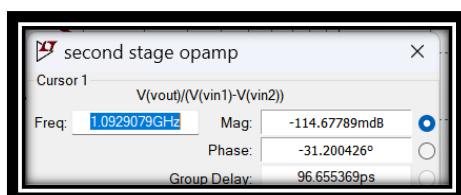


Figure 38 : Frequency Response



## SIMULATIONS RESULT

Gain > 60dB As Gain= 2828

## WEEK 5: ANALOG DESIGN INTERNSHIP

### **Previous Method: LT SPICE and Gm over Id Method**

In the earlier weeks of the internship, we utilized LT SPICE, a popular circuit simulation tool, to extract the NMOS and PMOS parameter charts required for circuit design. The Gm over Id Method was employed to analyse and characterize these devices.

### **Introduction of ADT (Analog Designer Toolbox)**

In Week 5, we introduced a new tool called ADT (Analog Designer Toolbox). ADT is a powerful software that comes with pregenerated lookup tables specifically tailored for the 180nm technology. By using the provided CMOS180.txt model file, ADT allows us to plot various parameter charts for NMOS and PMOS devices, considering different specifications such as length, VDS, VSB, and more.

## COMMON SOURCE AMPLIFIER USING NMOS AND CURRENT SOURCE LOAD

The Model file used is CMOS180.txt

**DESIGN CONSTRAINT:** Design should have optimized W/L ratio and Width and Length should be multiple of 0.18nm

SPECIFICATIONS
GBW=1GHz
Gain = 10 At 100MHz

### **CALCULATIONS**

GBW=1GHz, Gain =10 at 100MHz

$$\text{Let } Gm = 2mS \text{ (Assumed)} \quad CL = \frac{Gm}{2\pi 1\text{GHz}} = 0.27\text{pF}$$

$$\text{Taking } \frac{Gm}{Id} = 12 \quad Id = \frac{2mS}{12} = 166.67\mu\text{A} = 167\mu\text{A}$$

For NMOS: (From Look Up Tables in ADT)

$$\text{For } \frac{Gm}{Id} = 12, \quad \frac{Gm}{Gds} = 83.71, \quad \frac{Id}{W} = 9.356, \quad Vgs = 0.6238$$

$$\text{Hence, } Gds = \frac{2mS}{83.71} = 23.892\mu\text{s} \quad W = \frac{167\mu}{9.356} = 17.84\text{. u} \quad (\text{Taken } 17.82\text{u})$$

For PMOS: (From Look Up Tables in ADT)

From Id vs Gm/Id graph, AT Id=167uA, Gm/Id=8.989 Hence, Gm=1.5mS

$$\text{For } \frac{G_m}{I_d} = 8.989, \frac{G_m}{G_{ds}} = 62.51, \frac{I_d}{W} = 4.801, V_{sg} = 0.6798$$

$$\text{Hence, } G_{ds} = \frac{1.5mS}{62.51} = 23.9\mu\text{S} \quad W = \frac{167u}{4.801} = 34.784\mu \quad (\text{Taken } 34.74\mu)$$

$$\text{And, } V_b = 1.8 - 0.6798 = 1.1202 \quad R_{out} = 20.924\text{K}$$

## SCHEMATIC

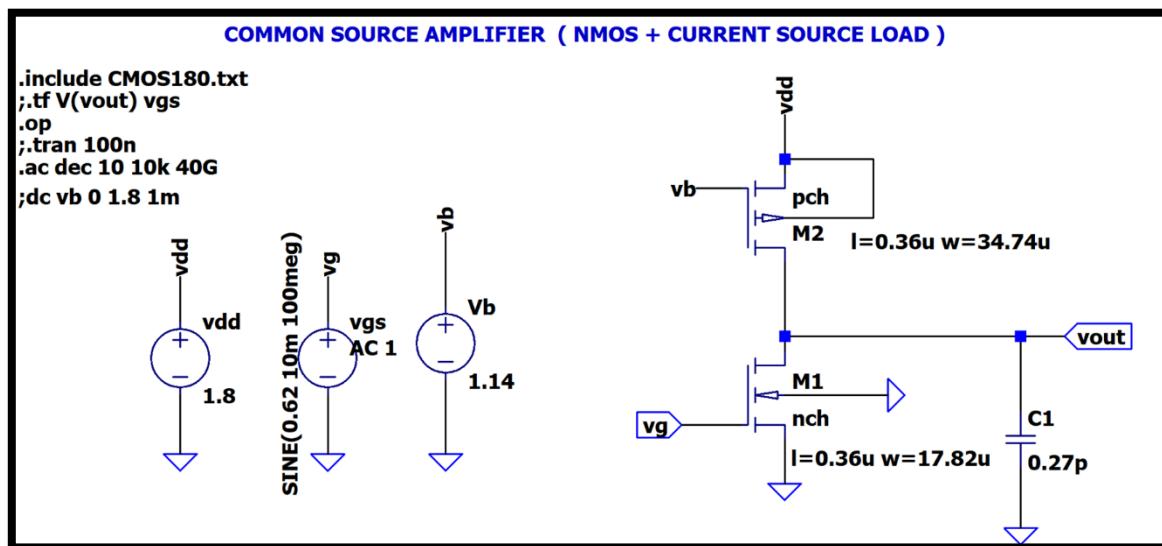


Figure 39

## SIMULATIONS

Name:	m2	m1
Model:	pch	nch
Id:	-1.62e-04	1.62e-04
Vgs:	-6.60e-01	6.20e-01
Vds:	-7.31e-01	1.07e+00
Vbs:	0.00e+00	0.00e+00
Vth:	-4.50e-01	4.58e-01
Vdsat:	-1.82e-01	1.30e-01
Gm:	1.47e-03	1.97e-03
Gds:	2.58e-05	2.28e-05
Gmb:	4.65e-04	5.23e-04
Cbd:	0.00e+00	0.00e+00

--- Transfer Function ---

Transfer_function:	-40.5869	transfer
vgs#Input_impedance:	1e+020	impedance
output_impedance_at_V(vout):	20583.6	impedance

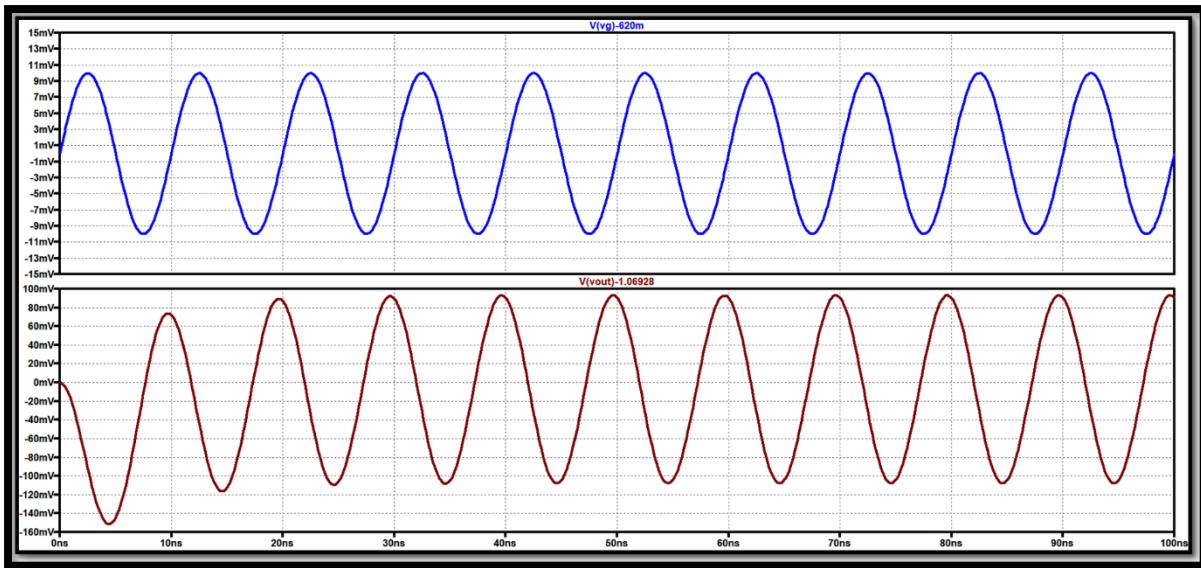


Figure 40: TRANSIENT ANALYSIS IN LT SPICE

**Gain =10 at 100MHz, Input given is 10mV**

### AC ANALYSIS

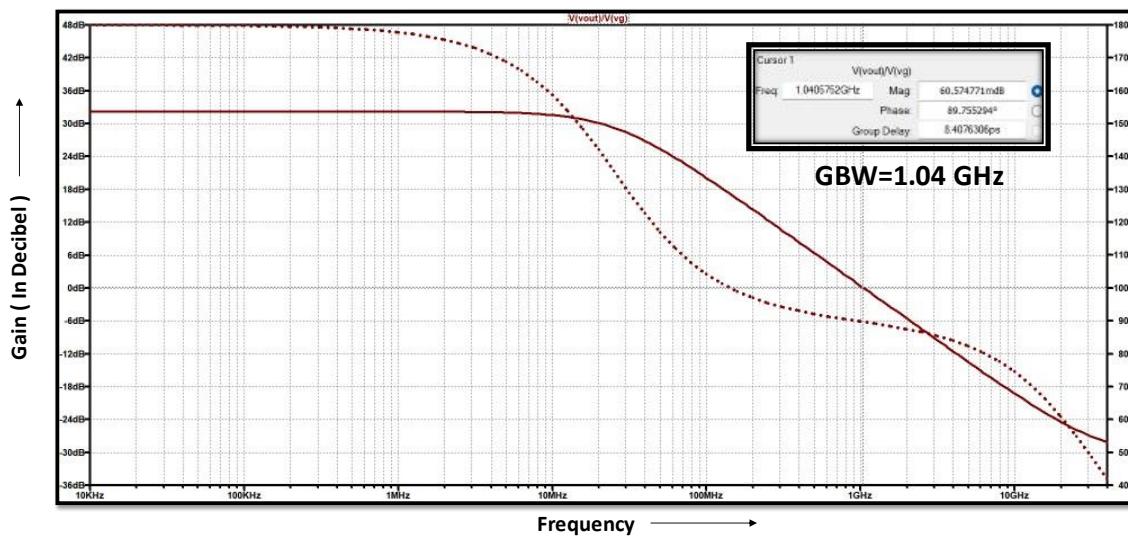


Figure 41: FREQUENCY RESPONSE IN LT SPICE

### AC ANALYSIS

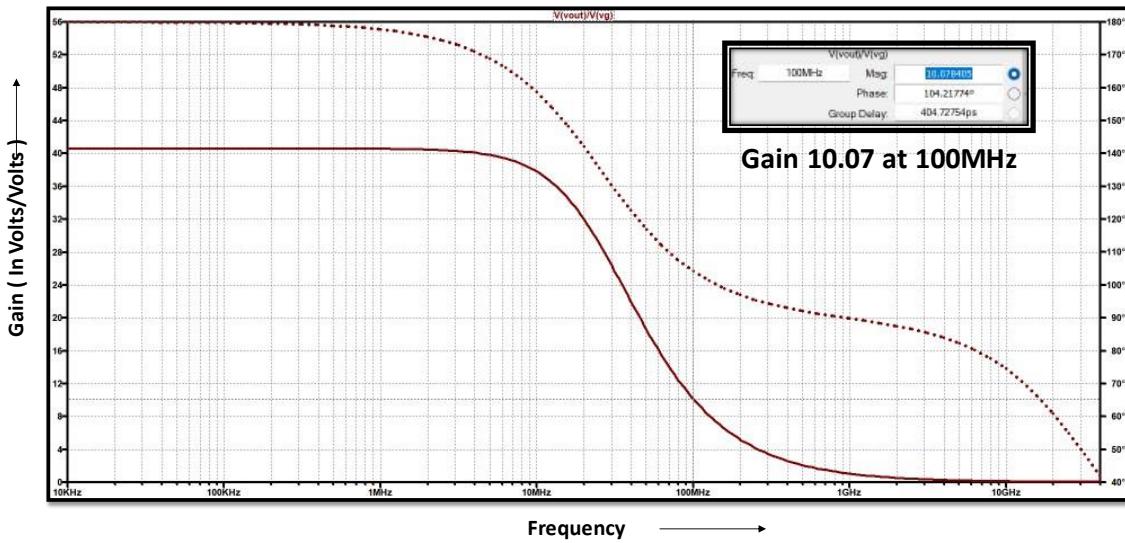


Figure 42: FREQUENCY RESPONSE IN LT SPICE

### **SIMULATION RESULTS**

GBW=1.04GHz

Gain=10.07 at 100MHz

### COMMON SOURCE AMPLIFIER FOR DESIGNING DIFFERENTIAL PAIR

The Model file used is CMOS180.txt

**DESIGN CONSTRAINT:** Design should have optimized W/L ratio and Width and Length should be multiple of 0.18nm

### **SPECIFICATIONS**

GBW=1GHz

Gain = 10 At 100MHz

## CALCULATIONS

GBW=1GHz, Gain =10 at 100MHz

Let  $Gm = 2\text{mS}$  (Assumed)       $\text{CL} = \frac{Gm}{2\pi 1\text{GHz}} = 0.29\text{pF}$

Taking  $\frac{Gm}{Id} = 12$        $Id = \frac{2\text{mS}}{12} = 166.67\text{uA} = 167\text{uA}$

For NMOS: (From Look Up Tables in ADT)

For       $\frac{Gm}{Id} = 12$       ,  $\frac{Id}{W} = 9.913$  ,     $Vgs = 0.7417$  hence  $Vg = 1.1917$

Hence,  $W = \frac{167\text{u}}{9.913} = 16.84\text{u}$       (Taken 16.92u)

For PMOS: (From Look Up Tables in ADT)

From Id vs Gm/Id graph, AT  $Id = 167\text{uA}$ ,  $Gm/Id = 4.144$  Hence,  $Gm = 0.69\text{mS}$

For       $\frac{Gm}{Id} = 4.144$  ,     $\frac{Id}{W} = 16.7$  ,     $Vsg = 0.8743$

Hence,  $W = \frac{167\text{u}}{16.7} = 10\text{u}$  (Taken 9.9u)

And,  $Vb = 1.8 - 0.8743 = 0.9257$

## SCHEMATIC

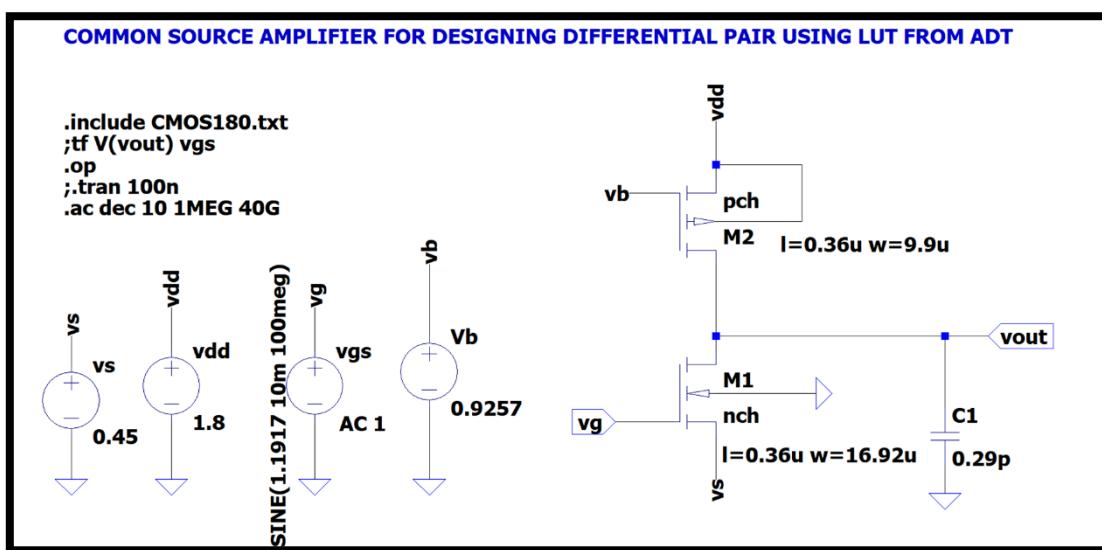


Figure 43

## SIMULATIONS

```
--- BSIM4
Name:      m2          m1
Model:     pch         nch
Id:       -1.66e-04   1.66e-04
Vgs:      -8.74e-01   7.42e-01
Vds:      -6.97e-01   6.53e-01
Vbs:       0.00e+00  -4.50e-01
Vth:      -4.49e-01   5.83e-01
Vdsat:    -3.43e-01   1.40e-01
Gm:       6.84e-04   1.97e-03
Gds:      2.14e-05   2.59e-05
Gmb:      2.24e-04   4.51e-04
Cbd:      0.00e+00   0.00e+00
```

### --- Transfer Function ---

Transfer_function:	-41.7108	transfer
vgs#Input_impedance:	1e+020	impedance
output_impedance_at_V(vout):	21127	impedance

## TRANSIENT ANALYSIS

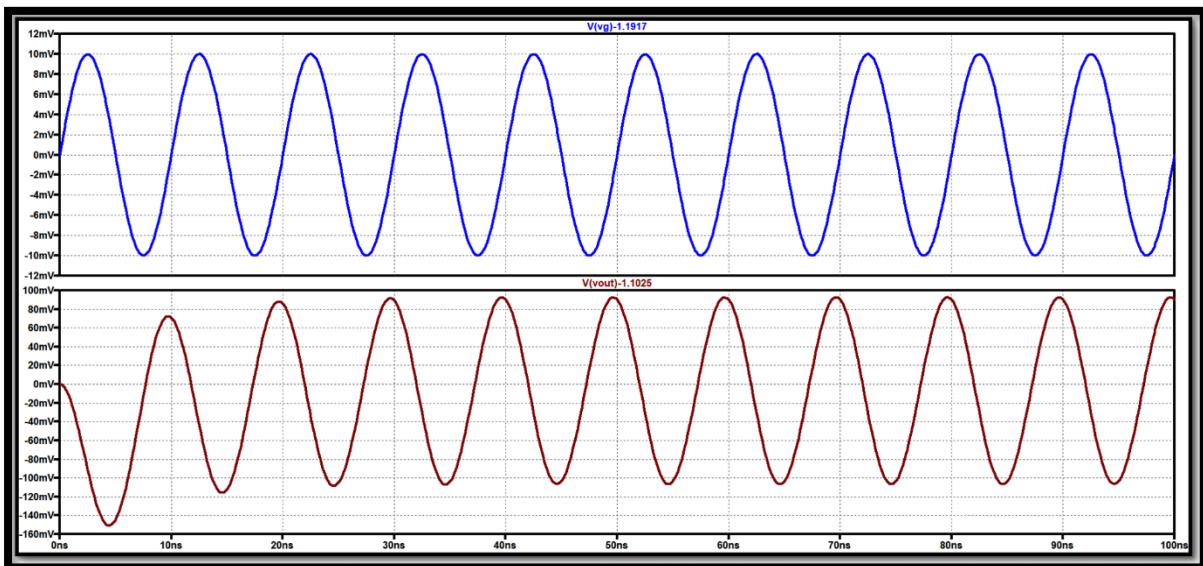


Figure 44: TRANSIENT ANALYSIS IN LT SPICE

Gain =10 at 100MHz, Input given is 10mV

## AC ANALYSIS

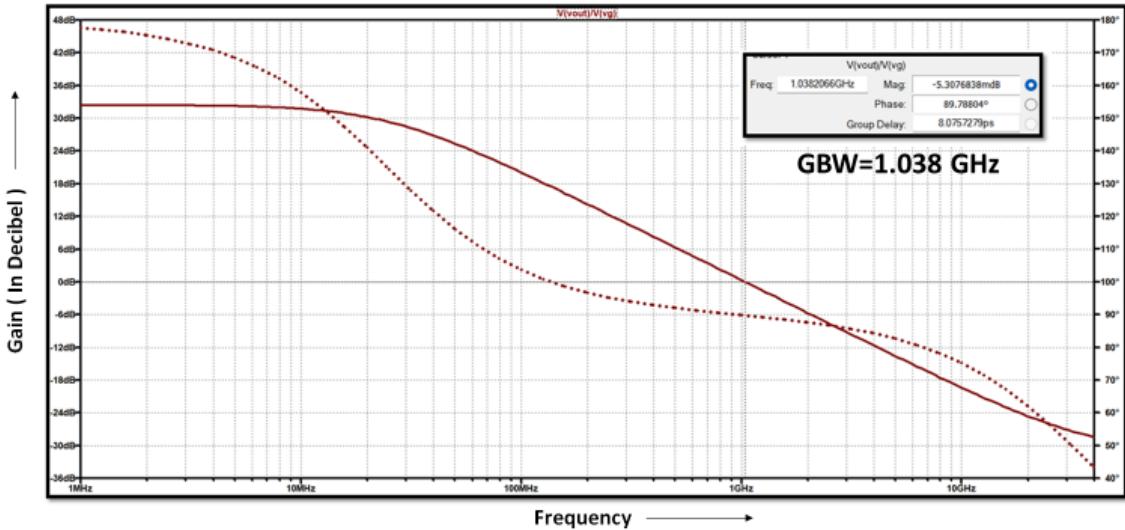


Figure 45: FREQUENCY RESPONSE IN LT SPICE

## AC ANALYSIS

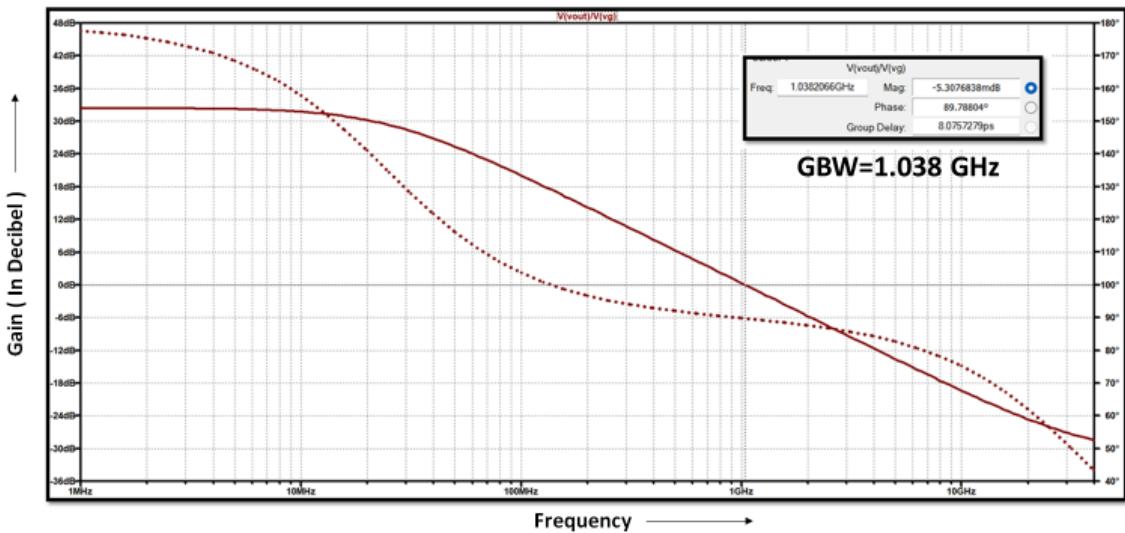


Figure 46: FREQUENCY RESPONSE IN LT SPICE

## SIMULATION RESULTS

GBW=1.038GHz

Gain=10.004 at 100MHz

## DESIGN AND SIMULATION OF DIFFERENTIAL PAIR

The Model file used is CMOS180.txt

**DESIGN CONSTRAINT:** Design should have optimized W/L ratio and Width and Length should be multiple of 0.18nm

SPECIFICATIONS
GBW=1GHz
Gain = 10 At 100MHz

## SCHEMATIC

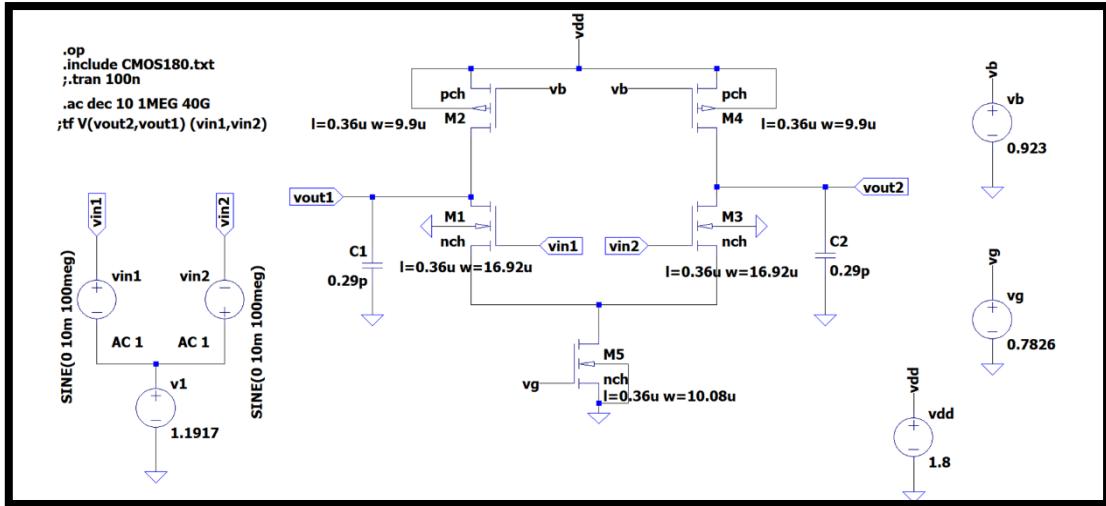


Figure 47

## SIMULATIONS

--- BSIM3 MOSFETS ---					
Name:	m4	m2	m5	m3	m1
Model:	pch	pch	nch	nch	nch
<i>Id</i> :	-1.68e-04	-1.68e-04	3.35e-04	1.68e-04	1.68e-04
<i>Vgs</i> :	-8.77e-01	-8.77e-01	7.83e-01	7.42e-01	7.42e-01
<i>Vds</i> :	-6.76e-01	-6.76e-01	4.50e-01	6.75e-01	6.75e-01
<i>Vbs</i> :	0.00e+00	0.00e+00	0.00e+00	-4.50e-01	-4.50e-01
<i>Vth</i> :	-4.49e-01	-4.49e-01	4.62e-01	5.83e-01	5.83e-01
<i>Vdsat</i> :	-3.44e-01	-3.44e-01	2.28e-01	1.40e-01	1.40e-01
<i>Gm</i> :	6.85e-04	6.85e-04	1.95e-03	1.98e-03	1.98e-03
<i>Gds</i> :	2.22e-05	2.22e-05	5.21e-05	2.58e-05	2.58e-05
<i>Gmb</i> :	2.24e-04	2.24e-04	5.05e-04	4.53e-04	4.53e-04
<i>Cbd</i> :	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
<i>Cbs</i> :	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
<i>Cgsov</i> :	6.50e-15	6.50e-15	4.95e-15	8.31e-15	8.31e-15
<i>Cgdov</i> :	6.50e-15	6.50e-15	4.95e-15	8.31e-15	8.31e-15
<i>Cgbov</i> :	2.98e-19	2.98e-19	3.28e-19	3.28e-19	3.28e-19
<i>dQgdVgb</i> :	3.39e-14	3.39e-14	3.35e-14	5.53e-14	5.53e-14
<i>dQgdVdb</i> :	-6.52e-15	-6.52e-15	-4.87e-15	-8.09e-15	-8.09e-15
<i>dQgdVsb</i> :	-2.65e-14	-2.65e-14	-2.72e-14	-4.48e-14	-4.48e-14

```

--- Transfer Function ---

Transfer_function:          41.3049      transfer
vin1#Input_impedance:        1e+020       impedance
output_impedance_at_V(vout2,vout1): 41644.3      impedance

```

## TRANSIENT ANALYSIS

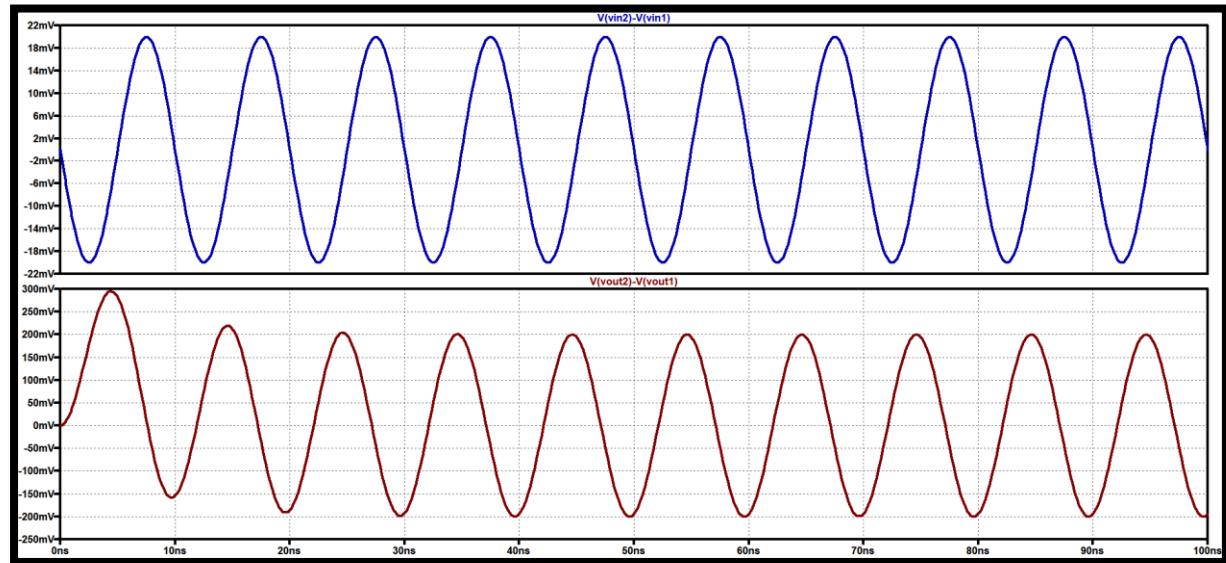


Figure 48: TRANSIENT ANALYSIS IN LT SPICE

Gain =10 at 100MHz, Input given is 10mV

## AC ANALYSIS

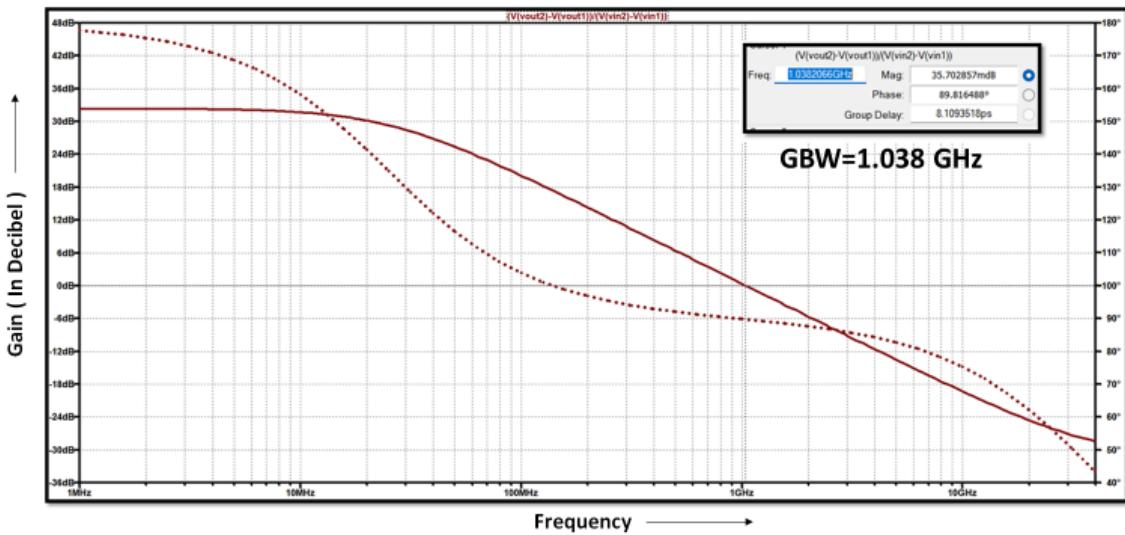


Figure 49: FREQUENCY RESPONSE IN LT SPICE

### AC ANALYSIS

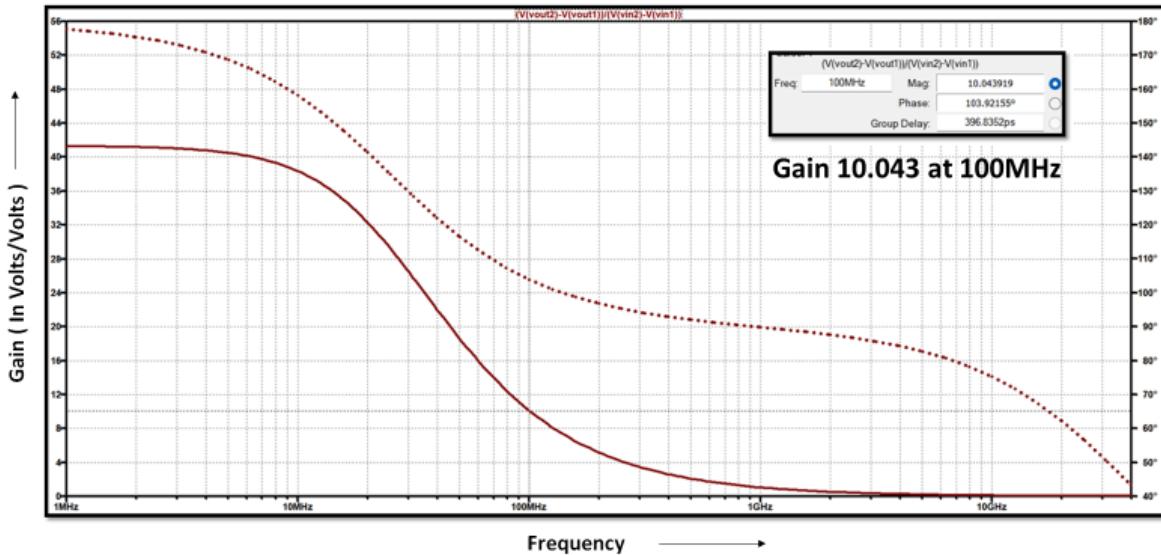


Figure 50: FREQUENCY RESPONSE IN LT SPICE

### SIMULATION RESULTS

GBW=1.038GHz

Gain=10.043 at 100MHz

### DESIGN AND SIMULATION OF SINGLE STAGE OPAMP

The Model file used is CMOS180.txt

**DESIGN CONSTRAINT:** Design should have optimized W/L ratio and Width and Length should be multiple of 0.18nm

### SPECIFICATIONS

GBW=1GHz

Gain = 10 At 100MHz

## SCHEMATIC

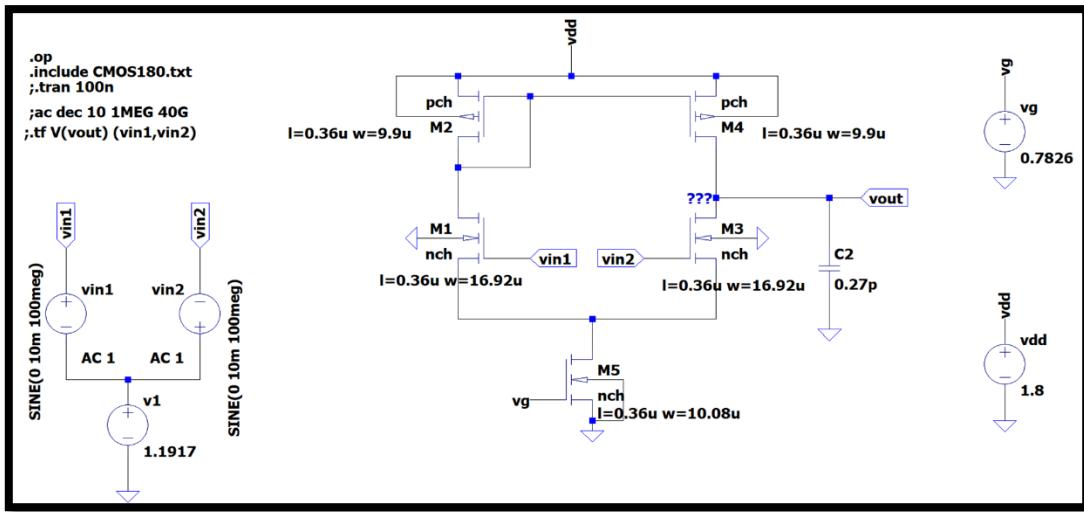


Figure 51

## SIMULATIONS

Semiconductor Device Operating Points:					
--- BSIM3 MOSFETS ---					
Name:	m4	m2	m5	m3	m1
Model:	pch	pch	nch	nch	nch
Id:	-1.68e-04	-1.68e-04	3.35e-04	1.68e-04	1.68e-04
Vgs:	-8.71e-01	-8.71e-01	7.83e-01	7.44e-01	7.44e-01
Vds:	-8.71e-01	-8.71e-01	4.48e-01	4.81e-01	4.81e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	-4.48e-01	-4.48e-01
Vth:	-4.49e-01	-4.49e-01	4.62e-01	5.84e-01	5.84e-01
Vdsat:	-3.40e-01	-3.40e-01	2.28e-01	1.41e-01	1.41e-01
Gm:	6.93e-04	6.93e-04	1.95e-03	1.97e-03	1.97e-03
Gds:	1.80e-05	1.80e-05	5.25e-05	2.95e-05	2.95e-05
Gmb:	2.26e-04	2.26e-04	5.05e-04	4.51e-04	4.51e-04
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	6.50e-15	6.50e-15	4.95e-15	8.31e-15	8.31e-15
Cgdov:	6.50e-15	6.50e-15	4.95e-15	8.31e-15	8.31e-15
Cgbov:	2.98e-19	2.98e-19	3.28e-19	3.28e-19	3.28e-19
dQgdVgb:	3.39e-14	3.39e-14	3.35e-14	5.53e-14	5.53e-14

--- Transfer Function ---		
Transfer_function:	41.0444	transfer
vin1#Input_impedance:	1e+020	impedance
output_impedance_at_V(vout):	21508.6	impedance

## TRANSIENT ANALYSIS

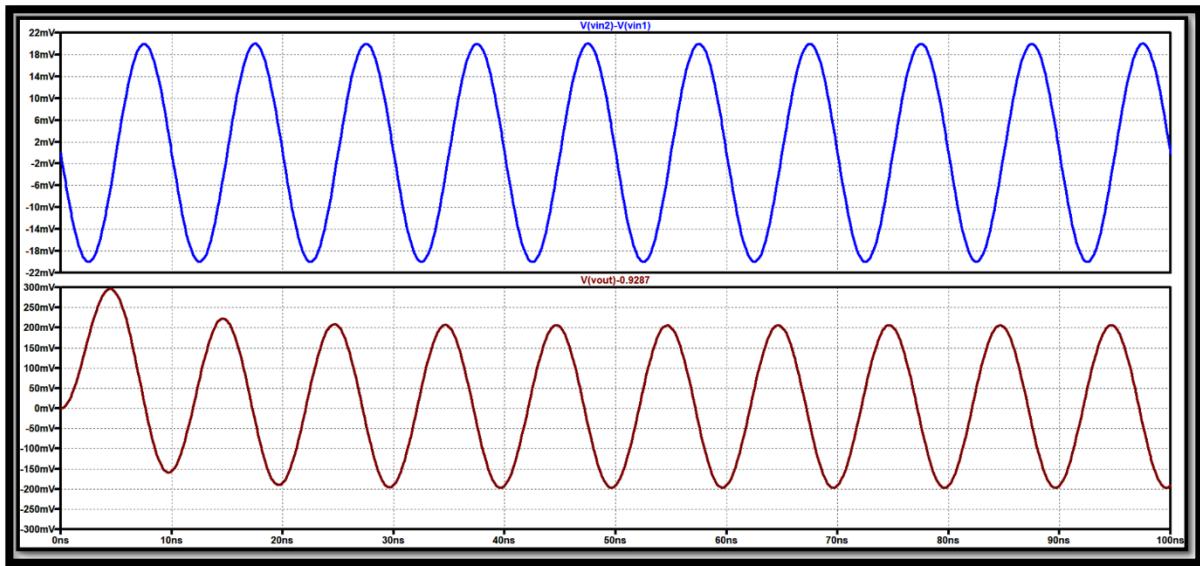


Figure 52: TRANSIENT ANALYSIS IN LT SPICE

**Gain =10 at 100MHz, Input given is 10Mv**

### AC ANALYSIS

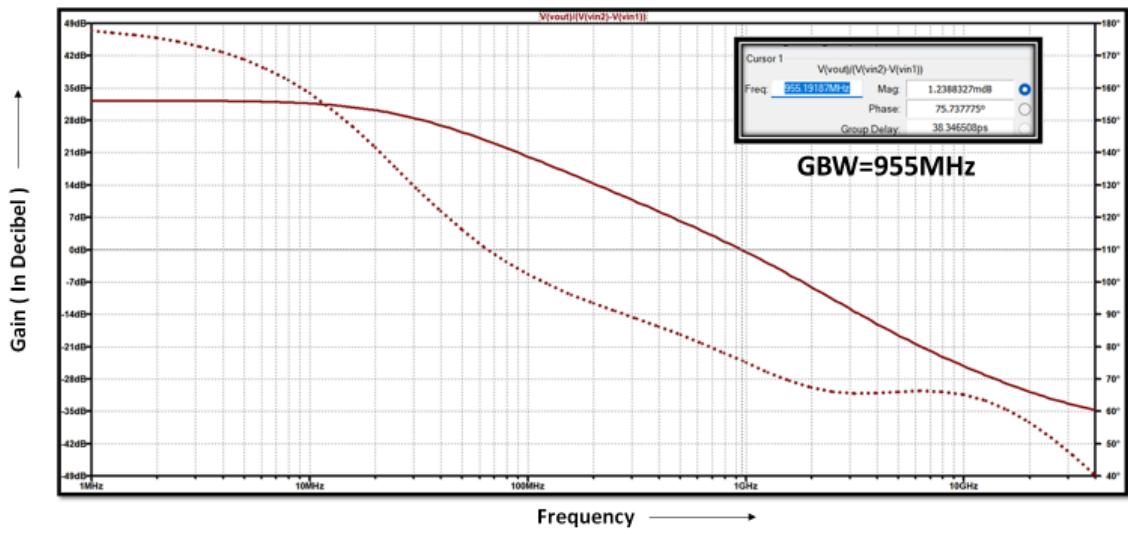


Figure 53: FREQUENCY RESPONSE IN LT SPICE

## AC ANALYSIS

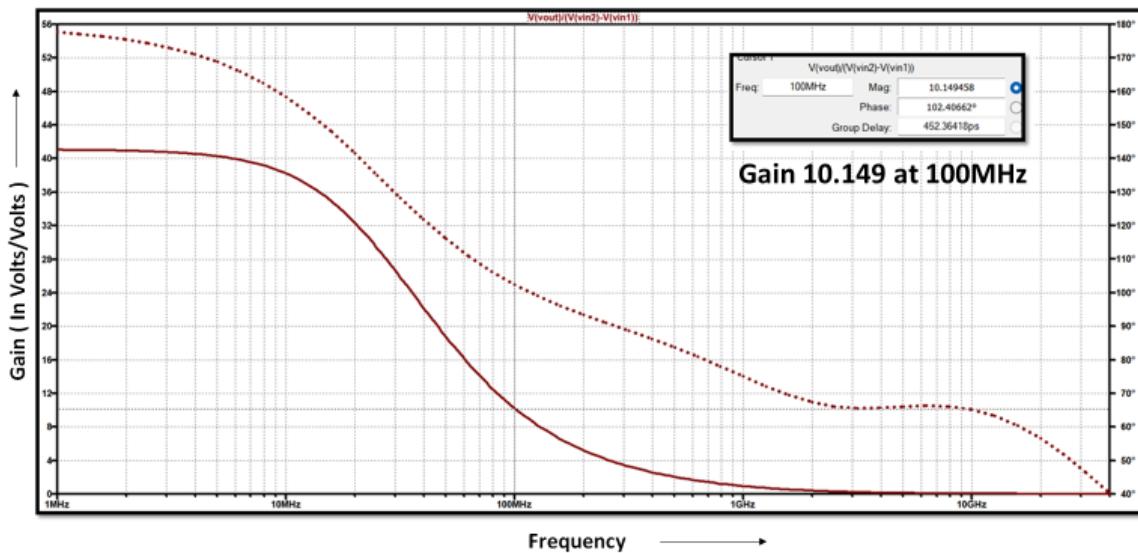


Figure 54: FREQUENCY RESPONSE IN LT SPICE

SIMULATION RESULTS
GBW=955 MHz
Gain=10.14 at 100MHz

## DESIGN AND SIMULATION OF TWO STAGE OPAMP

The Model file used is CMOS180.txt

**DESIGN CONSTRAINT:** Design should have optimized W/L ratio and Width and Length should be multiple of 0.18nm

SPECIFICATIONS
Gain > 60dB i.e. 100
CL=20fF and Phase Margin > 50

### CALCULATIONS FOR FIRST STAGE

Gain = 40, C<sub>L</sub> = 20fF, R<sub>out</sub> = 93 KΩ (Assumed after Back Calculations)

$$\text{Let } Gm = \frac{\text{Gain}}{R_{\text{out}}} = 0.43\text{mS}$$

$$\text{Taking } \frac{Gm}{Id} = 12 \quad Id = \frac{0.43\text{mS}}{12} = 35.83\text{uA}$$

For NMOS: (From Look Up Tables in ADT)

$$\text{For } \frac{Gm}{Id} = 12, \frac{Gm}{Gds} = 77.05, \frac{Id}{W} = 9.913, V_{gs} = 0.7316$$

$$\text{Hence, } Gds = \frac{0.43\text{mS}}{77.05} = 5.58\text{uS} \quad W = \frac{35.83\text{u}}{9.913} = 3.6\text{u} \quad \text{and } V_g = 0.7316 + 0.45$$

$$V_g = 1.18$$

For PMOS:

$$\text{As, } R_{\text{out}} = R_o(\text{NMOS}) \parallel R_o(\text{PMOS}) \quad Gds(\text{PMOS}) = \frac{1}{R_{\text{out}}} - Gds(\text{NMOS})$$

$$\text{Hence, } Gds(\text{PMOS}) = 5.172\text{uS}$$

Now, as current will remain same i.e., 35.83uA

$$\frac{Id}{Gds(\text{PMOS})} = \frac{35.83\text{u}}{5.172\text{u}} = 6.93 \quad \text{using this From LUT in ADT, } Gm/Id \text{ is calculated for PMOS}$$

$$\text{Hence, } \frac{Gm}{Id} = 5.487 \quad Gm(\text{PMOS}) = 5.487 * 35.83\text{uA} = 0.196\text{mS}$$

$$\text{For } \frac{Gm}{Id} = 5.487 \quad \frac{Id}{W} = 10.8 \quad V_{sg} = 0.781$$

$$\text{Hence, } W = \frac{35.83\text{u}}{10.8} = 3.317 \quad (\text{Taken } 3.24\text{u})$$

$$\text{And } V_b = 1.8 - 0.781 = 1.019 \quad \text{As, } CL = 20\text{f} \quad \text{BW (-3dB)} = \frac{Gm}{2\pi R_{\text{out}} CL} = 85.56\text{MHz}$$

## SCHMATIC (FIRST STAGE)

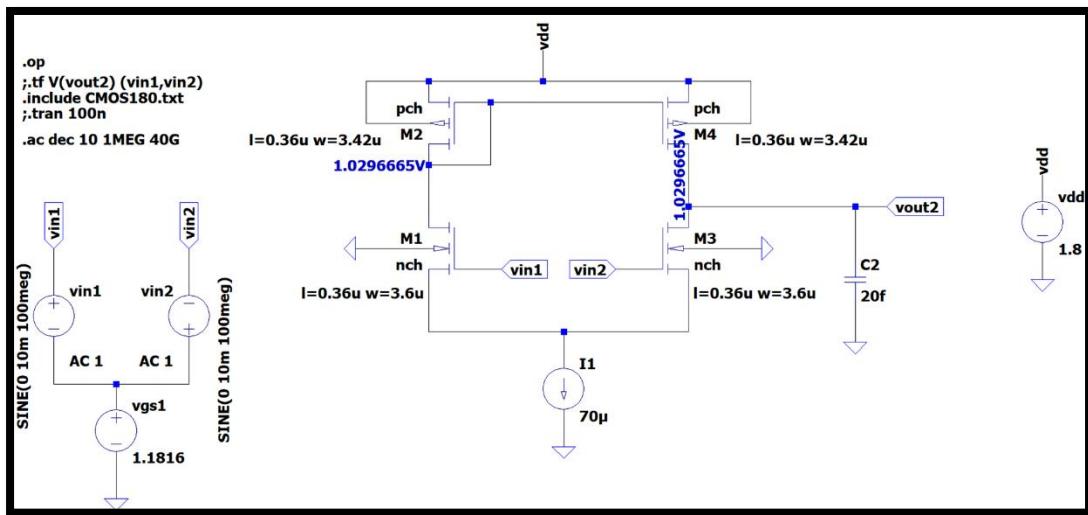


Figure 55

## CALCULATIONS FOR SECOND STAGE

### (COMMON SOURCE USING PMOS AND CURRENT SOURCE LOAD)

Gain = 28 ,  $C_L = 20f$

For PMOS :

Taking  $Gm = 8 * 0.43mS = 3.44 mS$

$$\text{As } Av = Gm * Rout \quad Rout = Av/Gm = 8.139K$$

$$Vb(\text{PMOS}) = 1.0296 \text{ V} \quad Vsg = 0.7704$$

From ADT, For  $Vsg = 0.7704$   $Gm/Id$  is Calculated  $\frac{Gm}{Id} = 5.658$   $Id = 607.8U$

$$\text{Now, for above } Gm/Id \quad \frac{Gm}{Gds} = 47.92 \quad , \quad \frac{Id}{W} = 10.51$$

$$\text{Hence, } Gds = 71.7uS \quad W = 57.84u$$

For NMOS:

$$\text{As, } Rout = Ro (\text{NMOS}) \parallel Ro (\text{PMOS}) \quad Gds (\text{NMOS}) = \frac{1}{R_{OUT}} - Gds (\text{PMOS})$$

$$\text{Hence, } Gds (\text{NMOS}) = 48.5uS$$

Now, as current will remain same i.e.,  $607.98uA$

$$\frac{Id}{Gds(\text{NMOS})} = 12.534 \quad \text{using this From LUT in ADT,}$$

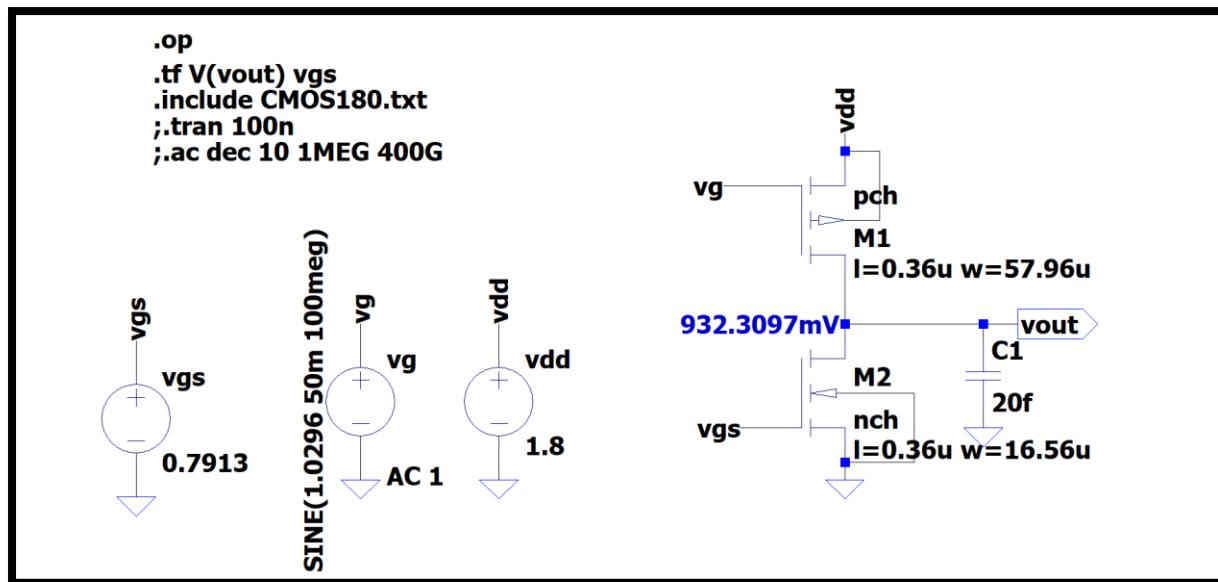
$Gm/Id$  is calculated for NMOS

$$\text{Hence, } \frac{Gm}{Id} = 5.61 \quad Gm (\text{PMOS}) = 5.61 * 607.98\mu\text{A} = 3.41\text{mS}$$

$$\text{For } \frac{Gm}{Id} = 5.61 \quad \frac{Id}{W} = 36.7 \quad V_{GS} = 0.7913$$

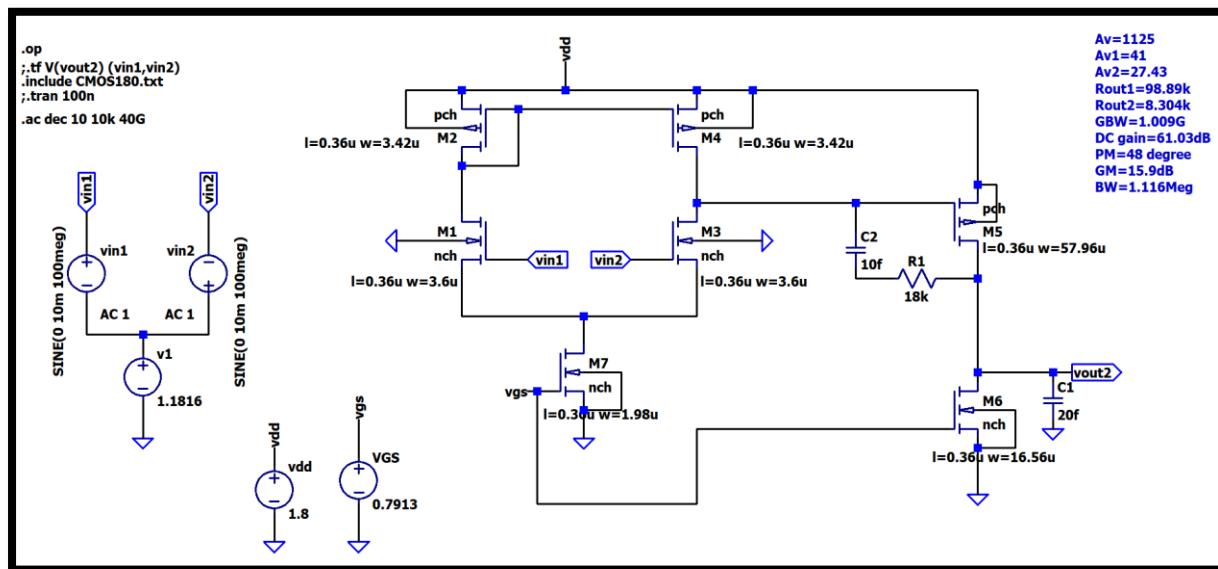
Hence,  $W = 16.56\text{u}$

## **SCHEMATIC (SECOND STAGE)**



*Figure 56*

## **TWO STAGE OPAMP SCHEMATIC IN LTSPICE**



*Figure 57*

## SIMULATIONS

Semiconductor Device Operating Points:					
--- BSIM3 MOSFETS ---					
Name:	m5	m4	m2	m7	m6
Model:	pch	pch	pch	nch	nch
Id:	-6.09e-04	-3.53e-05	-3.53e-05	7.06e-05	6.09e-04
Vgs:	-7.72e-01	-7.72e-01	-7.72e-01	7.91e-01	7.91e-01
Vds:	-8.24e-01	-7.72e-01	-7.72e-01	4.42e-01	9.76e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	-4.50e-01	-4.48e-01	-4.48e-01	4.61e-01	4.58e-01
Vdsat:	-2.69e-01	-2.63e-01	-2.63e-01	2.32e-01	2.36e-01
Gm:	3.42e-03	1.98e-04	1.98e-04	3.97e-04	3.39e-03
Gds:	7.53e-05	4.54e-06	4.54e-06	1.14e-05	4.69e-05
Gmb:	1.11e-03	6.28e-05	6.28e-05	1.02e-04	8.77e-04
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	3.81e-14	2.25e-15	2.25e-15	9.72e-16	8.13e-15
Cgdov:	3.81e-14	2.25e-15	2.25e-15	9.72e-16	8.13e-15
Cgbov:	2.98e-19	2.98e-19	2.98e-19	3.28e-19	3.28e-19
dQggdVgb:	1.98e-13	1.17e-14	1.17e-14	6.60e-15	5.50e-14
dQgdtVdb:	-3.81e-14	-2.25e-15	-2.25e-15	-9.58e-16	-7.92e-15
dQgdtVsb:	-1.54e-13	-9.13e-15	-9.13e-15	-5.36e-15	-4.47e-14
dQddtVgb:	-3.83e-14	-2.26e-15	-2.26e-15	-1.01e-15	-8.17e-15
dQddtVdb:	3.82e-14	2.25e-15	2.25e-15	1.01e-15	8.15e-15
dQddtVsb:	1.16e-16	7.48e-18	7.48e-18	8.16e-18	2.45e-17
dQbdVgb:	-2.50e-14	-1.51e-15	-1.51e-15	-9.86e-16	-8.27e-15
dQbdVdb:	-3.15e-17	-2.48e-18	-2.48e-18	-1.12e-17	1.62e-17
dQbdVsb:	-1.22e-14	-6.67e-16	-6.67e-16	-3.88e-16	-3.36e-15

Transfer_function:	-1125.91	transfer
vin1#Input_impedance:	1e+020	impedance
output_impedance_at_V(vout2) :	8185.31	impedance

## TRANSIENT ANALYSIS

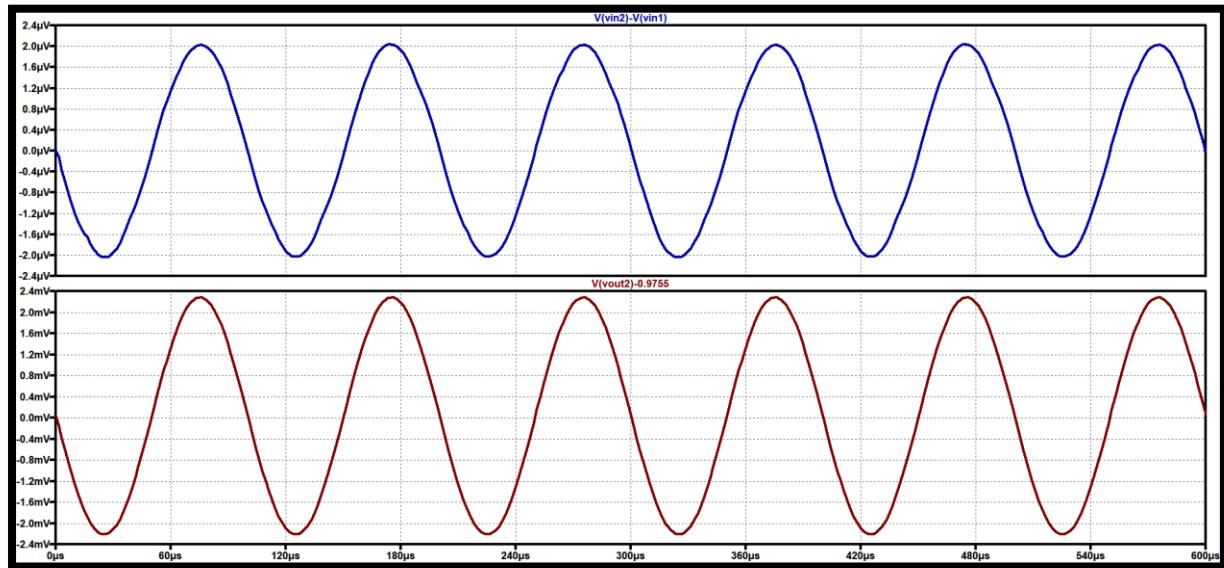


Figure 58: TRANSIENT ANALYSIS IN LT SPICE

Gain > 1000 at 10k, Input given is 1uV

### AC ANALYSIS

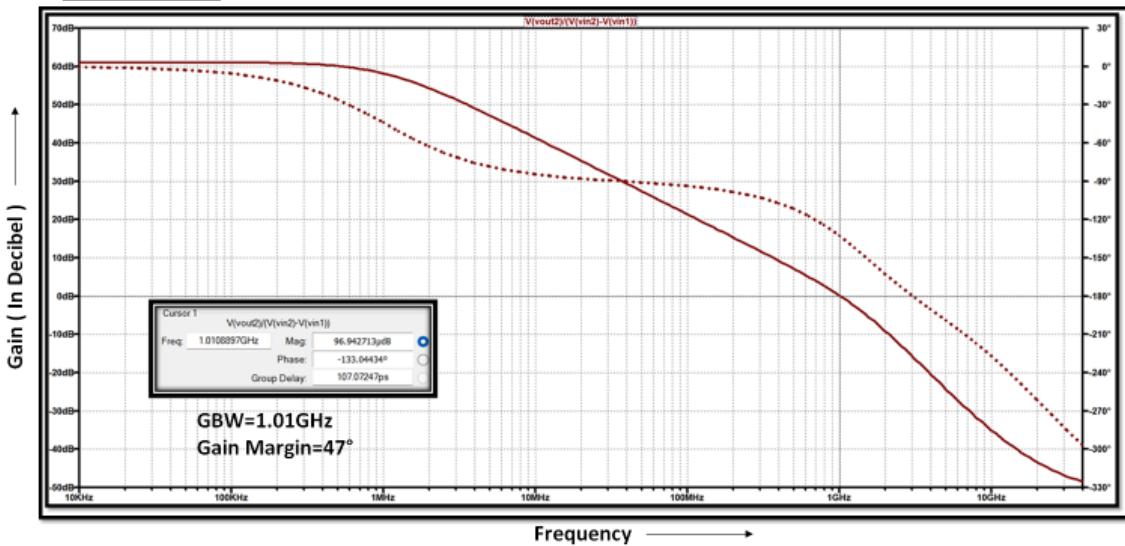


Figure 59: FREQUENCY RESPONSE IN LT SPICE

### SIMULATION RESULTS

GBW=1.01 GHz

Gain= 1125 i.e., 61.03dB

Phase Margin = 47°

## REFERENCES

- [The Gm/Id Design Methodology Demystified](#)  
By DR. Hesham Omran
- [CMOS Analog IC Design Lectures](#)  
By Dr. GS Javed
- [The Design of TWO STAGE Miller OpAmp: Final Verdict](#)  
By DR. Hesham Omran
- NPTEL IIT Madras Course on OpAmp  
[Lecture1](#)    [Lecture 2](#)    [Lecture 3](#)
- **GitHub Repository:** [Analog Design Internship](#)  
This Repository contains all the work done under this Internship Program

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