WEEK 3

INTERNSHIP UNDER DR GS JAVED SIR

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YEAR – SECOND

WEEK 3 INTERNSHIP TASK

- Differential Pair simulation
- Current Mirror simulation

NOTE : DESIGN CONSTRAINT IS TO USE UNIT DEVICES

SOFTWARE USED : LT Spice

SIMPLE CURRENT MIRROR

DESIGN AND SIMULATION USING LT SPICE

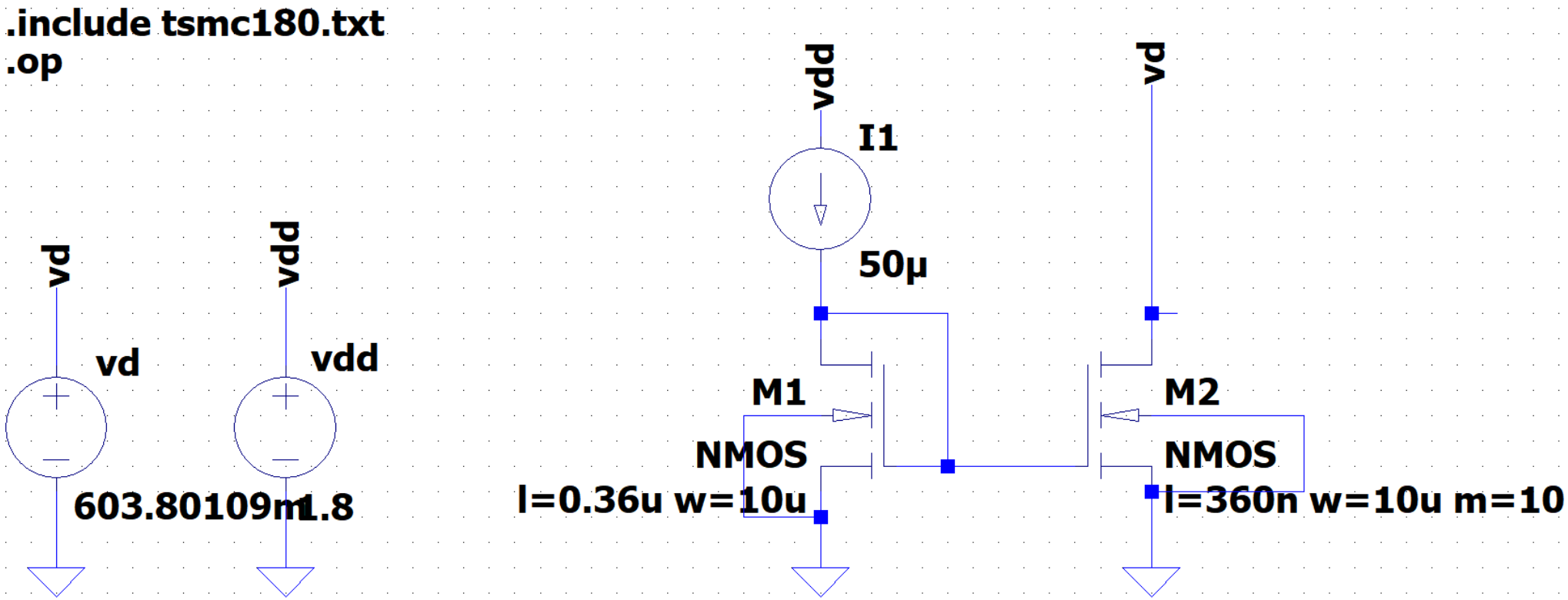
MODEL FILE : 180n

SPECIFICATIONS

Iref=50uA is used for Id(M2) =500uA

SCHEMATIC

SIMPLE CURRENT MIRROR (IDEAL CURRENT SOURCE AS REFERENCE)
SPECIFICATION: Iref=50uA



SPICE ERROR LOG

```
Semiconductor Device Operating Point
                              --- BSIM3 MO
Name:          m2             m1
Model:         nmos           nmos
Id:         5.00e-04       5.00e-05
Vgs:        6.04e-01       6.04e-01
Vds:        6.04e-01       6.04e-01
Vbs:        0.00e+00       0.00e+00
Vth:        4.66e-01       4.66e-01
Vdsat:      1.08e-01       1.08e-01
Gm:         7.88e-03       7.88e-04
Gds:        7.33e-05       7.33e-06
Gmb         2.08e-03       2.08e-04
Cbd:        0.00e+00       0.00e+00
Cbs:        0.00e+00       0.00e+00
Cgsov:      7.70e-14       7.70e-15
Cgdov:      7.70e-14       7.70e-15
```

SUMMARY

SPECIFICATION	SIMULATION RESULTS
Iref= Id(M1) = 50uA	Iref= Id(M1) = 50uA
Id(M2) = 500uA	Id(M2) = 500uA

SIMPLE CURRENT MIRROR

DESIGN AND SIMULATION USING LT SPICE

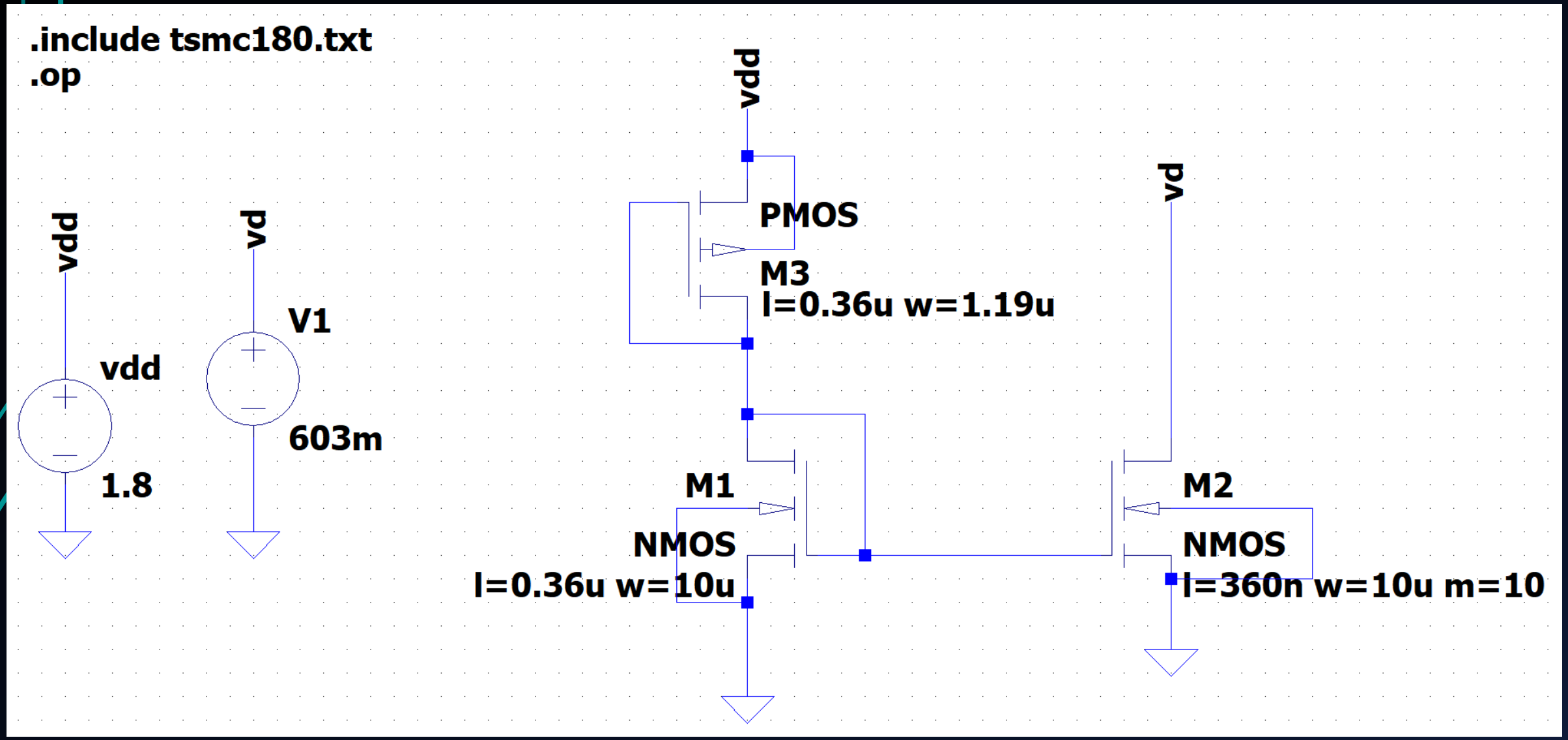
MODEL FILE : 180n

SPECIFICATIONS

Iref=50uA is used for Id(M2) =500uA

Note: Ideal Current Source is replaced by Diode connected PMOS

SCHEMATIC


.include tsmc180.txt
.op
vdd
vdd
vd
V1
603m
1.8
vdd
PMOS
M3
l=0.36u w=1.19u
vd
M1
NMOS
l=0.36u w=10u
M2
NMOS
l=360n w=10u m=10

SPICE ERROR LOG

```
Semiconductor Device Operating Points:
                                --- BSIM3 MOSFETS ---
Name:          m3              m2              m1
Model:         pmos            nmos            nmos
Id:         -5.00e-05       5.00e-04        5.00e-05
Vgs:        -1.20e+00       6.04e-01        6.04e-01
Vds:        -1.20e+00       6.03e-01        6.04e-01
Vbs:         0.00e+00       0.00e+00        0.00e+00
Vth:        -4.67e-01       4.66e-01        4.66e-01
Vdsat:      -5.49e-01       1.08e-01        1.08e-01
Gm:          1.18e-04       7.89e-03        7.89e-04
Gds:         3.58e-06       7.34e-05        7.33e-06
Gmb          3.87e-05       2.08e-03        2.08e-04
Cbd:         0.00e+00       0.00e+00        0.00e+00
Cbs:         0.00e+00       0.00e+00        0.00e+00
Cgsov:       8.45e-16       7.70e-14        7.70e-15
Cgdov:       8.45e-16       7.70e-14        7.70e-15
```

SUMMARY

SPECIFICATION	SIMULATION RESULTS
Iref= Id(M1) = 50uA Id(M3) = 50uA	Iref= Id(M1) = 50uA Id(M3) = 50uA
Id(M2) = 500uA	Id(M2) = 500uA

CASCODE CURRENT MIRROR

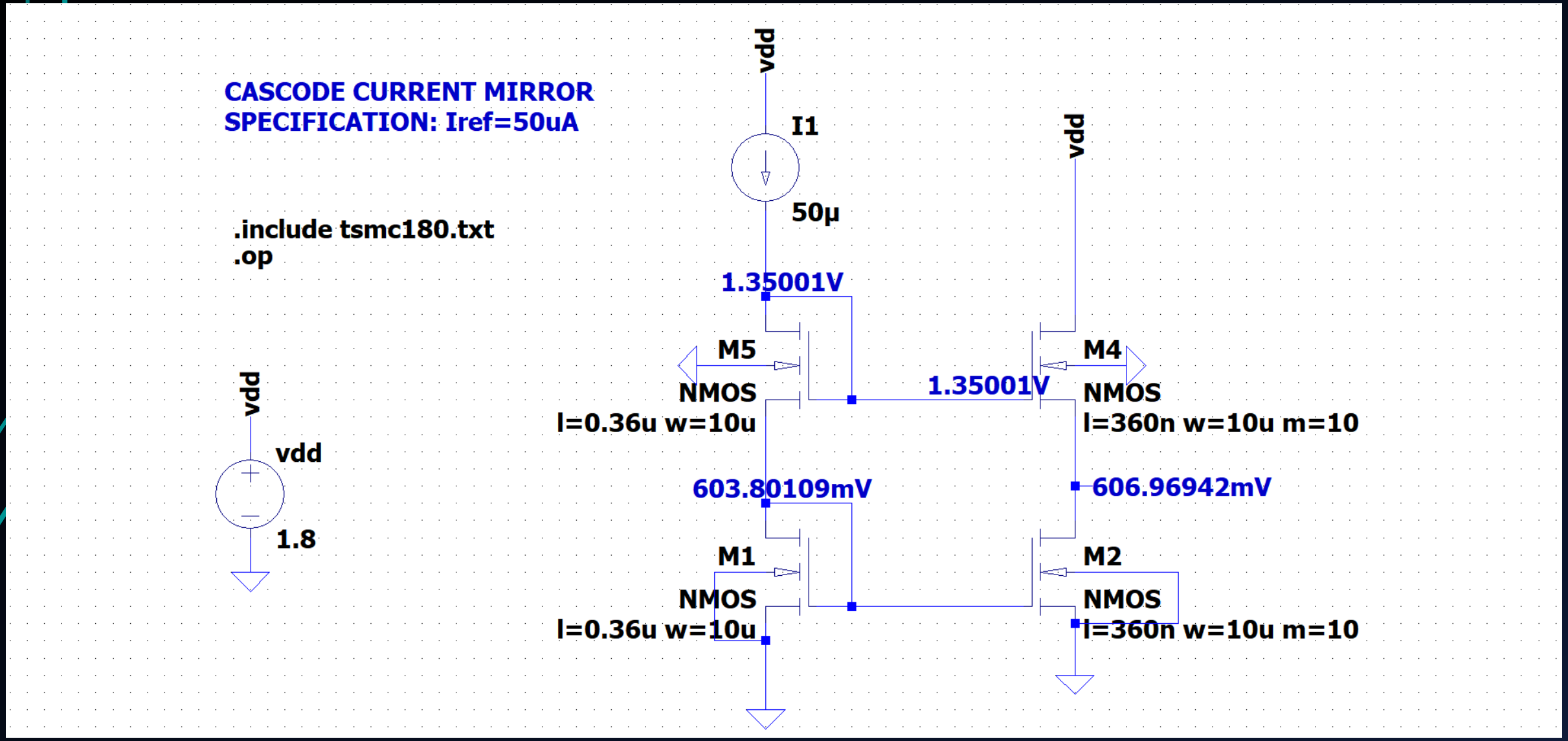
DESIGN AND SIMULATION USING LT SPICE

MODEL FILE : 180n

SPECIFICATIONS

Iref=50uA is used for Id(M2) =500uA

SCHEMATIC


CASCODE CURRENT MIRROR
SPECIFICATION: Iref=50uA
.include tsmc180.txt
.op
vdd
vdd
1.8
vdd
I1
50µ
1.35001V
M5
NMOS
l=0.36u w=10u
603.80109mV
M1
NMOS
l=0.36u w=10u
vdd
M4
1.35001V
NMOS
l=360n w=10u m=10
606.96942mV
M2
NMOS
l=360n w=10u m=10

SPICE ERROR LOG

Semiconductor Device Operating Points:

	--- BSIM3 MOSFETS ---			
Name:	m5	m4	m2	m1
Model:	nmos	nmos	nmos	nmos
Id:	5.00e-05	5.00e-04	5.00e-04	5.00e-05
Vgs:	7.46e-01	7.43e-01	6.04e-01	6.04e-01
Vds:	7.46e-01	1.19e+00	6.07e-01	6.04e-01
Vbs:	-6.04e-01	-6.07e-01	0.00e+00	0.00e+00
Vth:	6.21e-01	6.22e-01	4.66e-01	4.66e-01
Vdsat:	1.13e-01	1.10e-01	1.08e-01	1.08e-01
Gm:	8.05e-04	8.09e-03	7.89e-03	7.88e-04
Gds:	7.36e-06	6.76e-05	7.32e-05	7.33e-06
Gmb	1.75e-04	1.75e-03	2.08e-03	2.08e-04
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	7.70e-15	7.70e-14	7.70e-14	7.70e-15
Cgdov:	7.70e-15	7.70e-14	7.70e-14	7.70e-15

SUMMARY

SPECIFICATION	SIMULATION RESULTS
Iref= 50uA	Iref= 50uA
Id(M4) = 500uA Id(M3) = 500uA	Id(M4) = 500uA Id(M3) = 500uA

DIFFERENTIAL PAIR

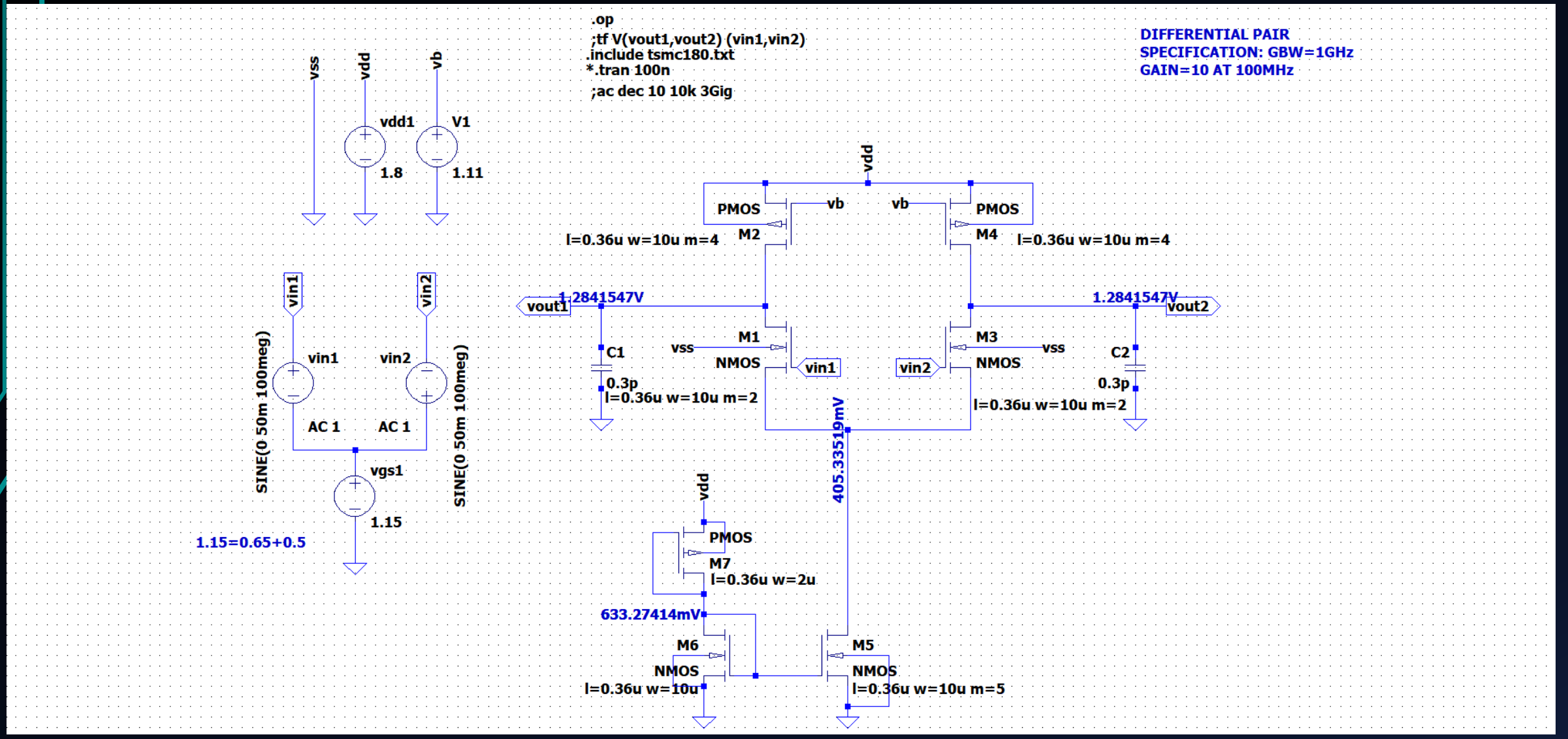
DESIGN AND SIMULATION USING LT SPICE
MODEL FILE : 180n

SPECIFICATIONS

GBW= 1GHz

Gain = 10 at 100 MHz frequency

SCHEMATIC


.op
;tf V(vout1,vout2) (vin1,vin2)
.include tsmc180.txt
*.tran 100n
;ac dec 10 10k 3Gig
DIFFERENTIAL PAIR
SPECIFICATION: GBW=1GHz
GAIN=10 AT 100MHz
vss
vdd
vb
vdd1
1.8
V1
1.11
vin1
vin2
AC 1
AC 1
SINE(0 50m 100meg)
SINE(0 50m 100meg)
vgs1
1.15
1.15=0.65+0.5
vdd
PMOS
M2
l=0.36u w=10u m=4
vb
vb
PMOS
M4
l=0.36u w=10u m=4
1.2841547V
vout1
1.2841547V
vout2
C1
0.3p
l=0.36u w=10u m=2
M1
vss
NMOS
vin1
vin2
M3
vss
NMOS
C2
0.3p
l=0.36u w=10u m=2
405.33519mV
vdd
PMOS
M7
l=0.36u w=2u
633.27414mV
M6
NMOS
l=0.36u w=10u
M5
NMOS
l=0.36u w=10u m=5

SPICE ERROR LOG

Semiconductor Device Operating Points:

--- BSIM3 MOSFETS ---

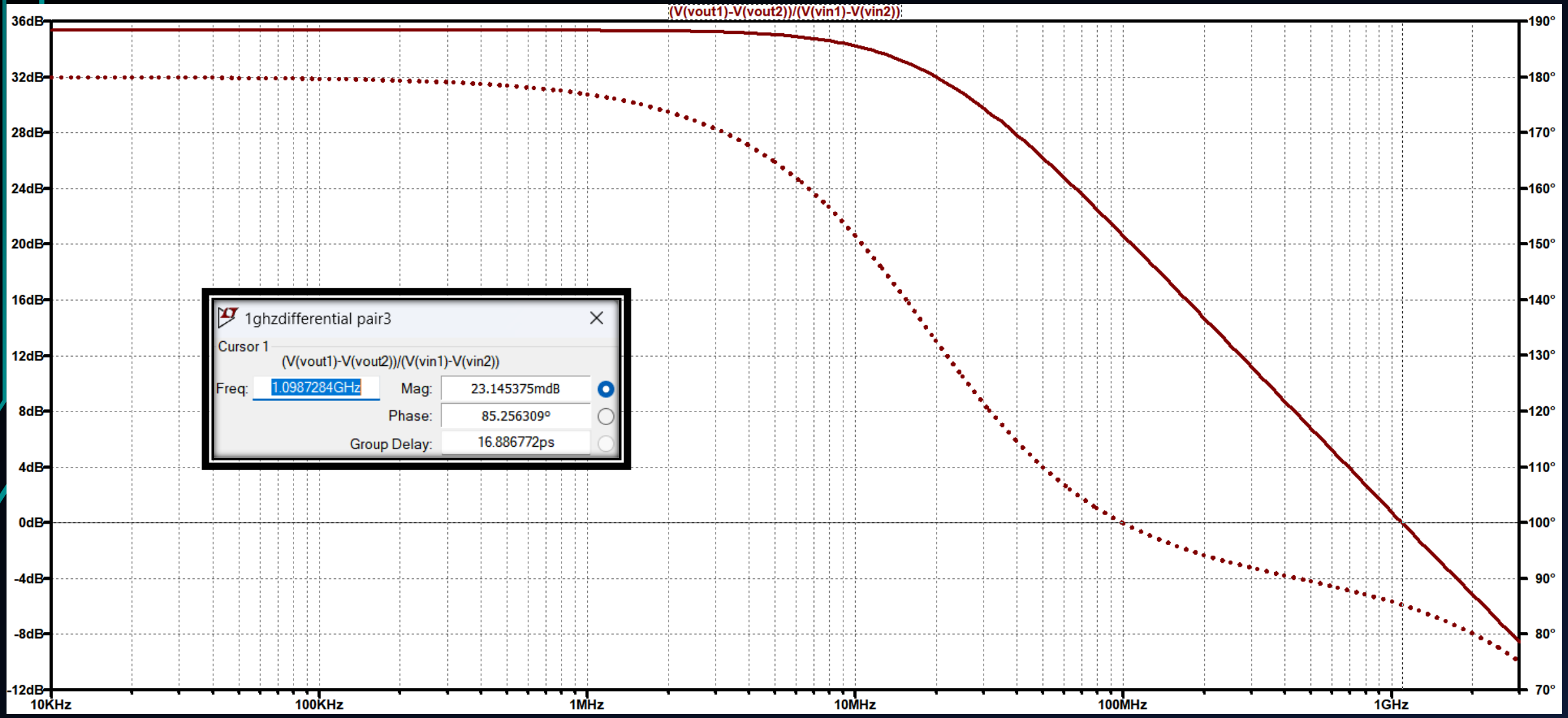
Name:	m7	m4	m2	m5	m6
Model:	pmos	pmos	pmos	nmos	nmos
Id:	-7.72e-05	-1.87e-04	-1.87e-04	3.74e-04	7.72e-05
Vgs:	-1.17e+00	-6.90e-01	-6.90e-01	6.33e-01	6.33e-01
Vds:	-1.17e+00	-5.16e-01	-5.16e-01	4.05e-01	6.33e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	-4.70e-01	-4.73e-01	-4.73e-01	4.66e-01	4.66e-01
Vdsat:	-5.31e-01	-1.91e-01	-1.91e-01	1.29e-01	1.29e-01
Gm:	1.90e-04	1.59e-03	1.59e-03	5.06e-03	1.04e-03
Gds:	5.53e-06	1.80e-05	1.80e-05	6.17e-05	1.01e-05
Gmb	6.23e-05	5.06e-04	5.06e-04	1.33e-03	2.73e-04
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	1.42e-15	2.84e-14	2.84e-14	3.85e-14	7.70e-15
Cgdov:	1.42e-15	2.84e-14	2.84e-14	3.85e-14	7.70e-15
Cgbov:	3.11e-19	1.24e-18	1.24e-18	1.66e-18	3.33e-19
dQgdVgb:	7.26e-15	1.45e-13	1.45e-13	1.94e-13	3.88e-14
dQgdVdb:	-1.42e-15	-2.85e-14	-2.85e-14	-3.86e-14	-7.70e-15
dQgdVsb:	-5.77e-15	-1.13e-13	-1.13e-13	-1.47e-13	-2.93e-14
dQddVgb:	-3.17e-15	-6.33e-14	-6.33e-14	-8.49e-14	-1.70e-14

Name:	m3	m1
Model:	nmos	nmos
Id:	1.87e-04	1.87e-04
Vgs:	7.45e-01	7.45e-01
Vds:	8.79e-01	8.79e-01
Vbs:	-4.05e-01	-4.05e-01
Vth:	5.74e-01	5.74e-01
Vdsat:	1.43e-01	1.43e-01
Gm:	2.34e-03	2.34e-03
Gds:	2.20e-05	2.20e-05
Gmb	5.35e-04	5.35e-04
Cbd:	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00
Cgsov:	1.54e-14	1.54e-14
Cgdov:	1.54e-14	1.54e-14
Cgbov:	6.66e-19	6.66e-19
dQgdVgb:	7.69e-14	7.69e-14

--- Transfer Function ---

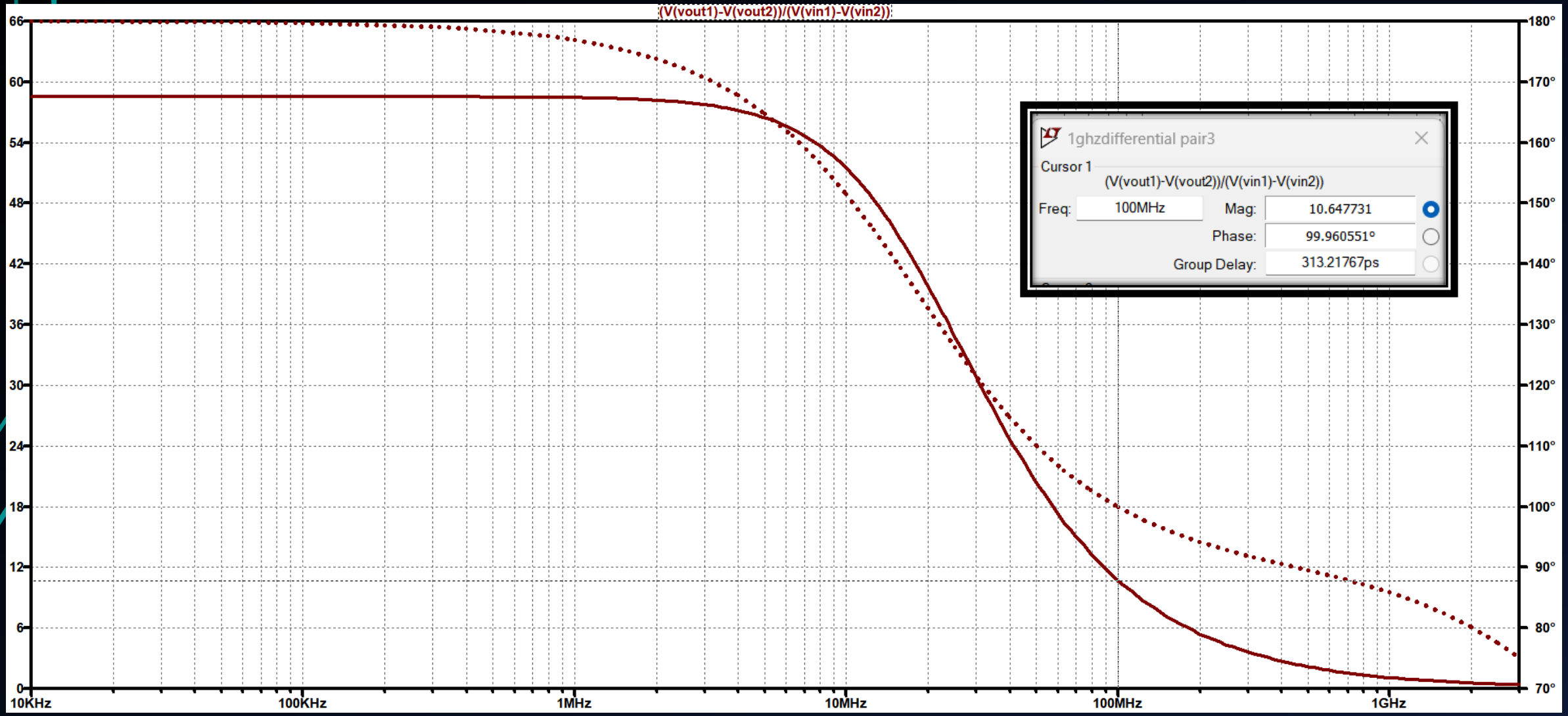
Transfer_function:	-58.5197	transfer
vin1#Input_impedance:	1e+020	impedance
output_impedance_at_V(vout1,vout2):	50022.3	impedance

FREQUENCY RESPONSE



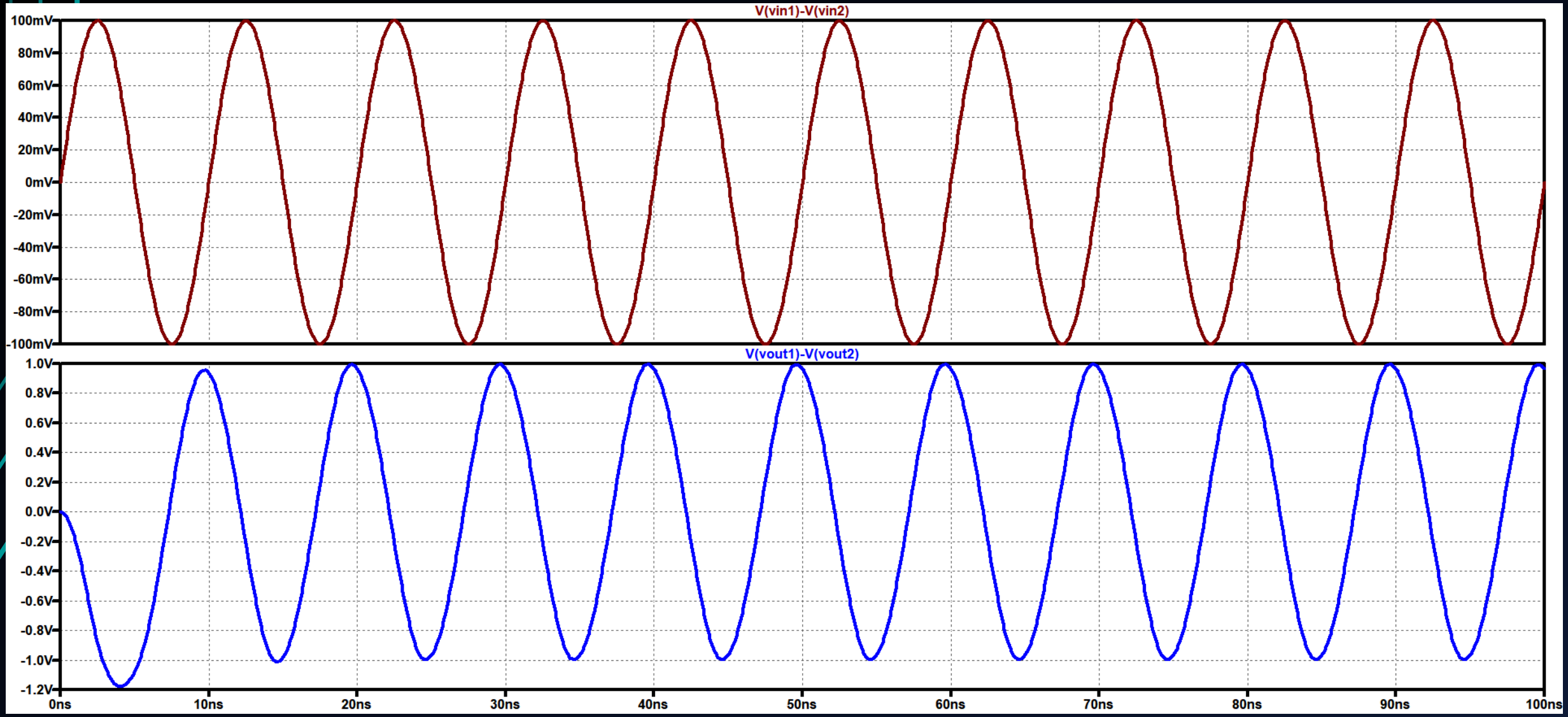
GBW=1.0987GHz

FREQUENCY RESPONSE



AT 100MHz Gain = 10.647

TRANSIENT ANALYSIS



If 10mV signal is given at 100MHz then we can observe from here Gain is nearly 10

SUMMARY

SPECIFICATION	SIMULATION RESULTS
GBW=1GHz	GBW=1.09GHz
Gain 10 at 100MHz	Gain 10.647 at 100MHz

THANK YOU