WEEK 2

INTERNSHIP UNDER DR GS JAVED SIR

INTERN NAME - AFZAL MALIK

COLLEGE/UNIVERSITY – ZAKIR HUSAIN COLLEGE OF ENGG. & TECH.
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COURSE- BACHELOR OF TECHNOLOGY (ELECTRONICS ENGG.)

YEAR – SECOND

WEEK 2 INTERNSHIP PLAN

- Differential Pair simulation
- Current Mirror simulation
- Delay Cell simulation
- Comparator simulation

SOFTWARE USED : LT Spice

SIMPLE CURRENT MIRROR

DESIGN AND SIMULATION USING LT SPICE

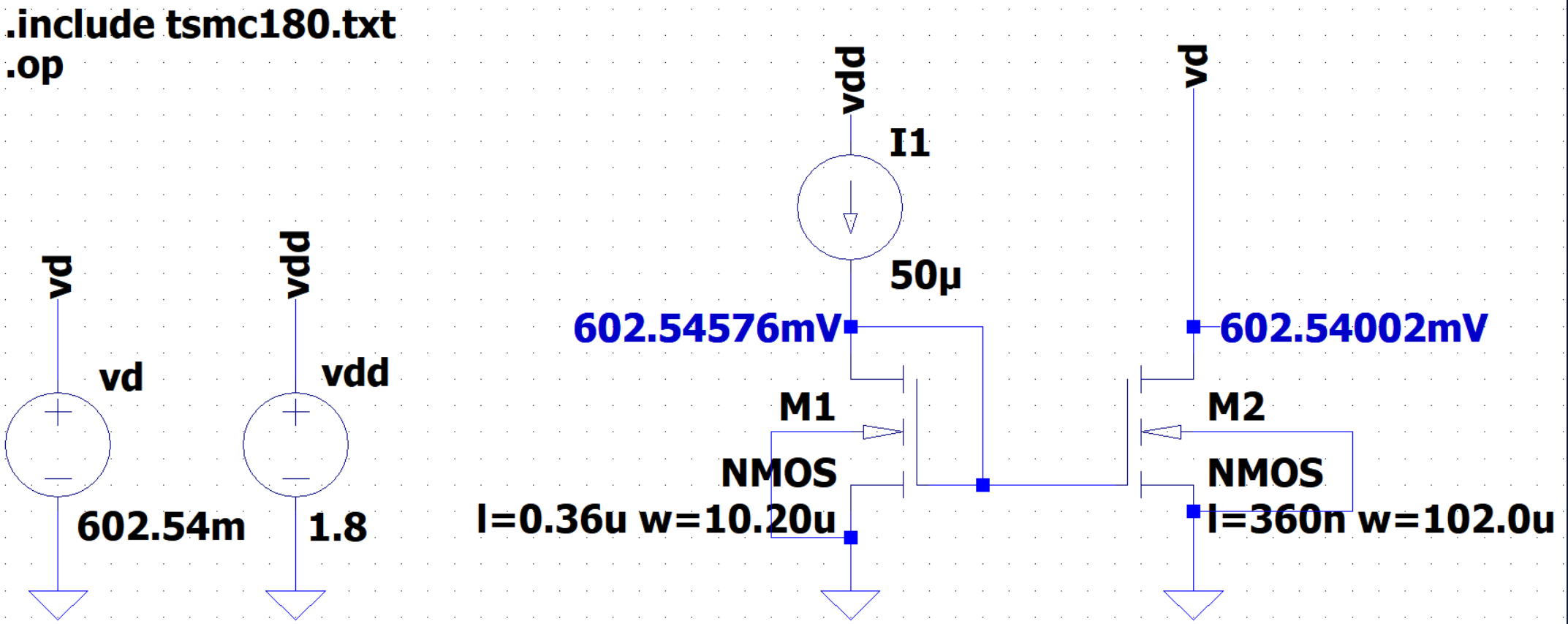
MODEL FILE : 180n

SPECIFICATIONS

Iref=50uA is used for Id(M2) =500uA

SCHEMATIC

SIMPLE CURRENT MIRROR (IDEAL CURRENT SOURCE AS REFERENCE)
SPECIFICATION: Iref=50uA



SPICE ERROR LOG

```
Semiconductor Device Operating Points:
                              --- BSIM3 MOSFETS ---
Name:            m2             m1
Model:          nmos           nmos
Id:          5.16e-04       5.00e-05
Vgs:         6.03e-01       6.03e-01
Vds:         6.00e-01       6.03e-01
Vbs:         0.00e+00       0.00e+00
Vth:         4.64e-01       4.66e-01
Vdsat:       1.09e-01       1.07e-01
Gm:          8.09e-03       7.93e-04
Gds:         7.55e-05       7.37e-06
Gmb          2.13e-03       2.09e-04
Cbd:         0.00e+00       0.00e+00
Cbs:         0.00e+00       0.00e+00
```

Iref= Id(M1) = 50uA AND Id(M2) = 516uA

SIMPLE CURRENT MIRROR

DESIGN AND SIMULATION USING LT SPICE

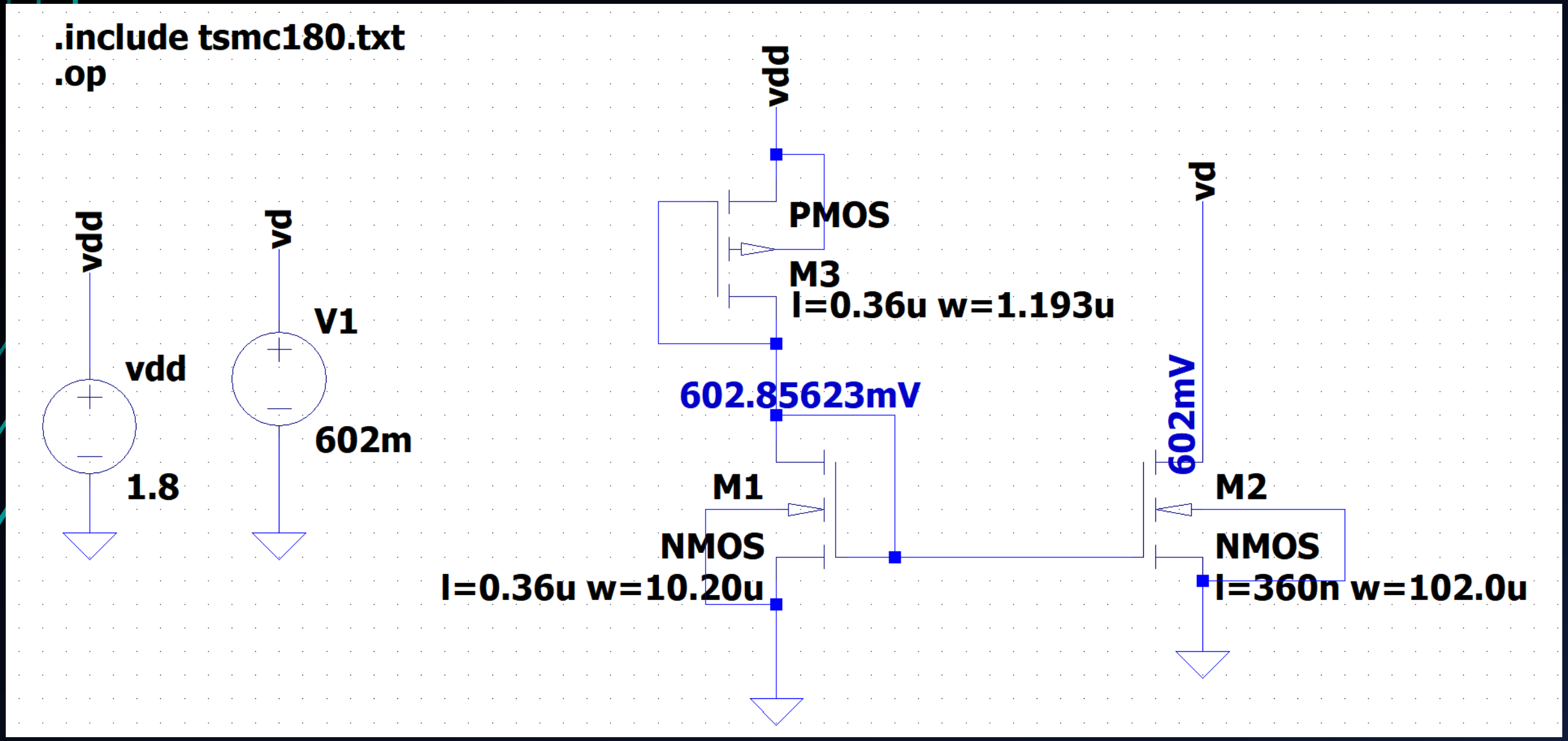
MODEL FILE : 180n

SPECIFICATIONS

Iref=50uA is used for Id(M2) =500uA

Note: Ideal Current Source is replaced by Diode connected PMOS

SCHEMATIC


.include tsmc180.txt
.op
vdd
vdd
1.8
vd
V1
602m
vdd
PMOS
M3
l=0.36u w=1.193u
602.85623mV
M1
NMOS
l=0.36u w=10.20u
vd
602mV
M2
NMOS
l=360n w=102.0u

SPICE ERROR LOG

```
Semiconductor Device Operating Points:
                                --- BSIM3 MOSFETS ---
Name:          m3              m2              m1
Model:         pmos            nmos            nmos
Id:         -5.02e-05       5.19e-04        5.02e-05
Vgs:        -1.20e+00       6.03e-01        6.03e-01
Vds:        -1.20e+00       6.02e-01        6.03e-01
Vbs:         0.00e+00       0.00e+00        0.00e+00
Vth:        -4.67e-01       4.64e-01        4.66e-01
Vdsat:      -5.50e-01       1.09e-01        1.07e-01
Gm:          1.18e-04       8.12e-03        7.96e-04
Gds:         3.59e-06       7.57e-05        7.40e-06
Gmb          3.88e-05       2.14e-03        2.10e-04
```

Iref= Id(M1) = 50uA AND Id(M2) = 519uA

CASCODE CURRENT MIRROR

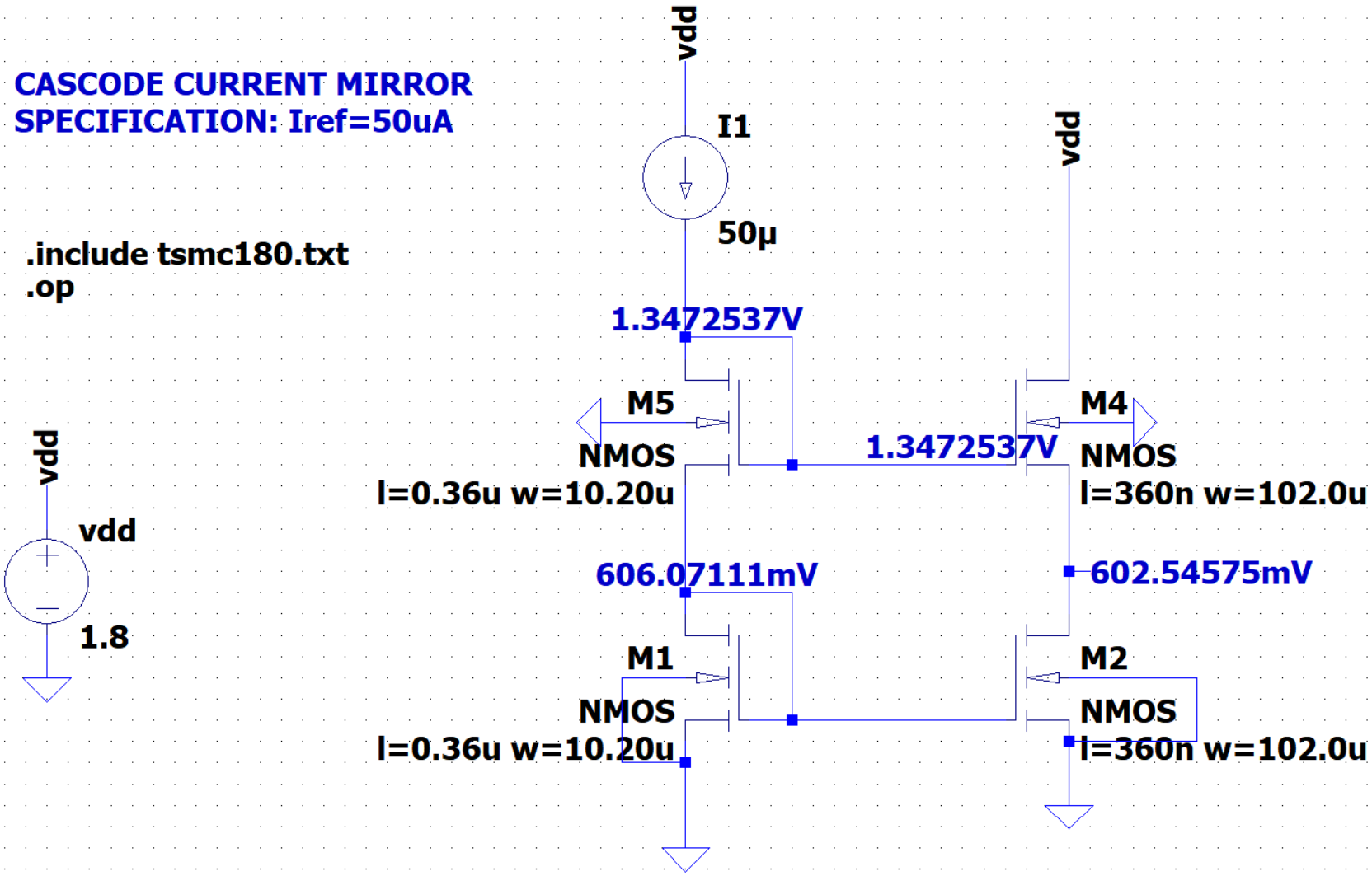
DESIGN AND SIMULATION USING LT SPICE

MODEL FILE : 180n

SPECIFICATIONS

Iref=50uA is used for Id(M2) =500uA

SCHEMATIC


CASCODE CURRENT MIRROR
SPECIFICATION: Iref=50uA
.include tsmc180.txt
.op
vdd
vdd
1.8
vdd
I1
50µ
1.3472537V
M5
NMOS
l=0.36u w=10.20u
1.3472537V
vdd
M4
NMOS
l=360n w=102.0u
606.07111mV
602.54575mV
M1
NMOS
l=0.36u w=10.20u
M2
NMOS
l=360n w=102.0u

SPICE ERROR LOG

Semiconductor Device Operating Points:

	--- BSIM3 MOSFETS ---			
Name:	m5	m4	m2	m1
Model:	nmos	nmos	nmos	nmos
Id:	5.00e-05	5.16e-04	5.16e-04	5.00e-05
Vgs:	7.45e-01	7.41e-01	6.03e-01	6.03e-01
Vds:	7.45e-01	1.19e+00	6.06e-01	6.03e-01
Vbs:	-6.03e-01	-6.06e-01	0.00e+00	0.00e+00
Vth:	6.21e-01	6.19e-01	4.64e-01	4.66e-01
Vdsat:	1.12e-01	1.11e-01	1.09e-01	1.07e-01
Gm:	8.10e-04	8.31e-03	8.09e-03	7.93e-04
Gds:	7.39e-06	6.94e-05	7.53e-05	7.37e-06
Gmb	1.76e-04	1.79e-03	2.13e-03	2.09e-04
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	7.85e-15	7.85e-14	7.85e-14	7.85e-15

Iref= Id(M1) = 50uA AND Id(M2) = 516uA

DIFFERENTIAL PAIR

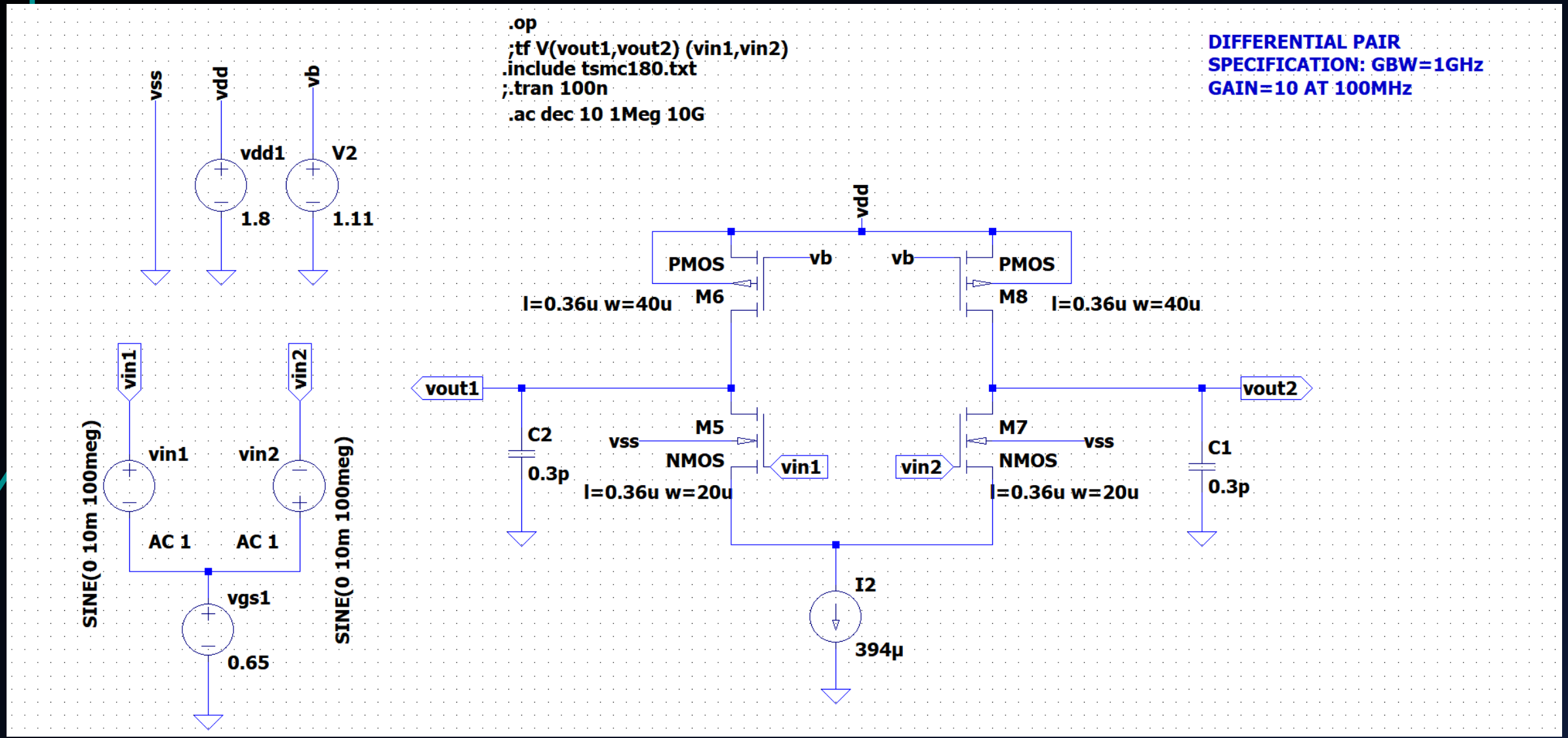
DESIGN AND SIMULATION USING LT SPICE
MODEL FILE : 180n

SPECIFICATIONS

GBW= 1GHz

Gain = 10 at 100 MHz frequency

SCHEMATIC

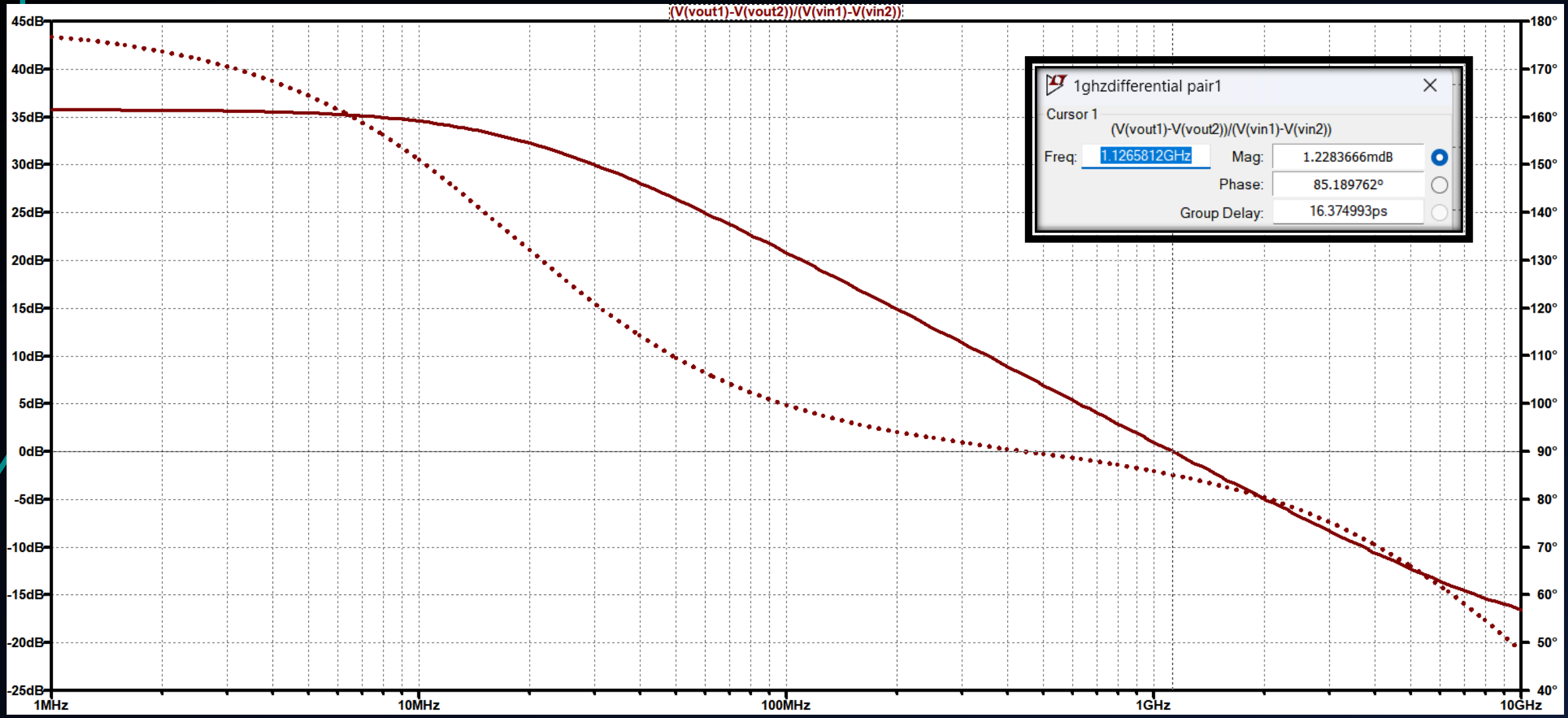

.op
;tf V(vout1,vout2) (vin1,vin2)
.include tsmc180.txt
;.tran 100n
.ac dec 10 1Meg 10G
DIFFERENTIAL PAIR
SPECIFICATION: GBW=1GHz
GAIN=10 AT 100MHz
vss
vdd
vb
vdd1
1.8
V2
1.11
vin1
vin2
SINE(0 10m 100meg)
AC 1
vgs1
0.65
PMOS
M6
l=0.36u w=40u
M8
M5
NMOS
M7
C2
0.3p
C1
vout1
vout2
I2
394µ

SPICE ERROR LOG

```
Semiconductor Device Operating Points:
                          --- BSIM3 MOSFETS ---
Name:          m8           m6           m7           m5
Model:       pmos         pmos         nmos         nmos
Id:       -1.97e-04    -1.97e-04     1.97e-04     1.97e-04
Vgs:      -6.90e-01    -6.90e-01     6.50e-01     6.50e-01
Vds:      -9.82e-01    -9.82e-01     8.18e-01     8.18e-01
Vbs:       0.00e+00     0.00e+00    -8.44e-07    -8.44e-07
Vth:      -4.73e-01    -4.73e-01     4.65e-01     4.65e-01
Vdsat:    -1.94e-01    -1.94e-01     1.41e-01     1.41e-01
Gm:        1.68e-03     1.68e-03     2.39e-03     2.39e-03
Gds:       1.69e-05     1.69e-05     2.22e-05     2.22e-05
Gmb        5.39e-04     5.39e-04     6.26e-04     6.26e-04
Cbd:       0.00e+00     0.00e+00     0.00e+00     0.00e+00
Cbs:       0.00e+00     0.00e+00     0.00e+00     0.00e+00
Cgsov:     2.84e-14     2.84e-14     1.54e-14     1.54e-14
Cgdov:     2.84e-14     2.84e-14     1.54e-14     1.54e-14
Cgbov:     3.11e-19     3.11e-19     3.33e-19     3.33e-19
```

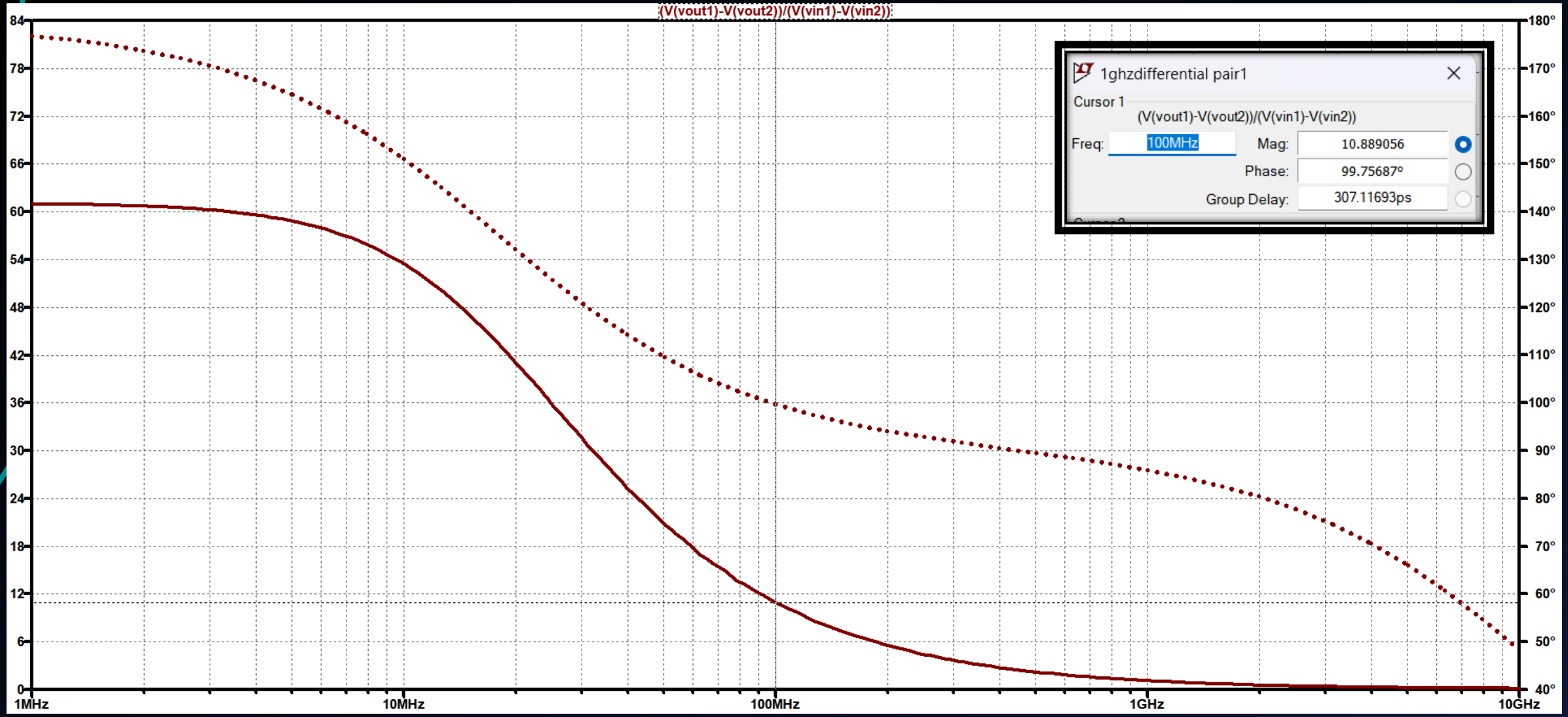
```
        --- Transfer Function ---

Transfer_function:                -61.0825        transfer
vin1#Input_impedance:             1e+020          impedance
output_impedance_at_V(vout1,vout2):               51098.9         impedance
```

FREQUENCY RESPONSE



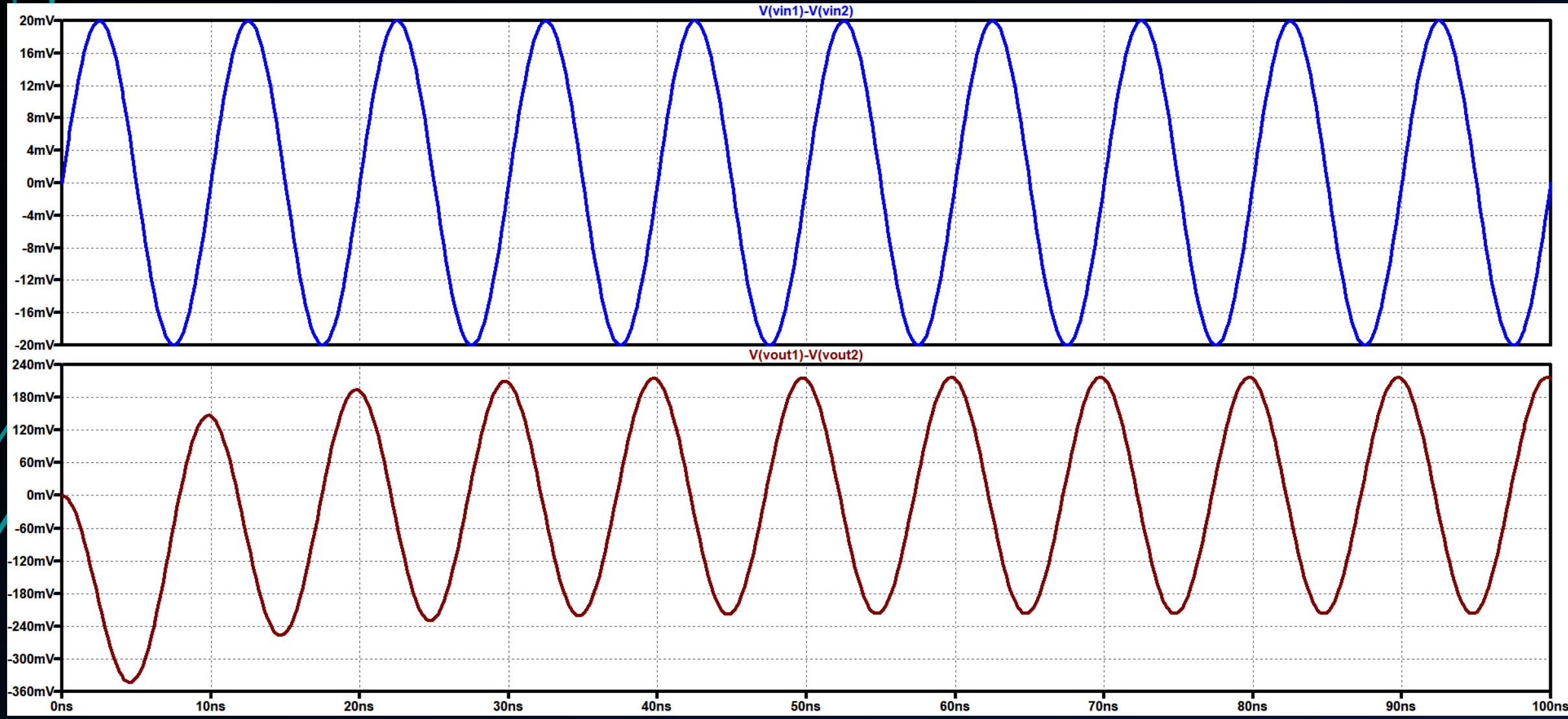
GBW=1.12GHz

FREQUENCY RESPONSE



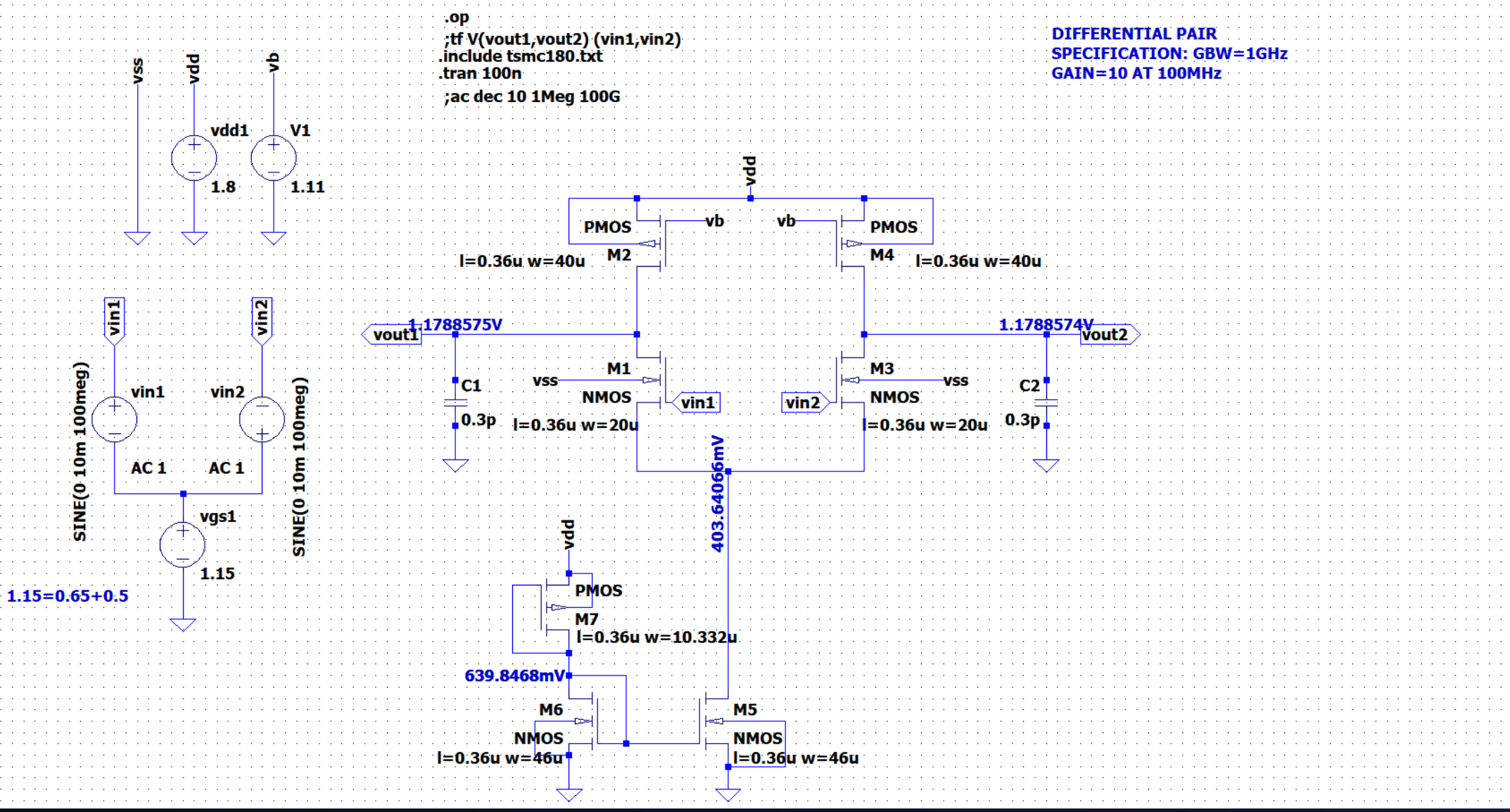
AT 100MHz Gain =10.88

TRANSIENT ANALYSIS



If 10mV signal is given at 100MHz then we can observe from here Gain is nearly 10

SCHEMATIC


.op
;tf V(vout1,vout2) (vin1,vin2)
.include tsmc180.txt
.tran 100n
;ac dec 10 1Meg 100G
DIFFERENTIAL PAIR
SPECIFICATION: GBW=1GHz
GAIN=10 AT 100MHz
vss
vdd
vb
vdd1
1.8
V1
1.11
vin1
vin2
SINE(0 10m 100meg)
AC 1
vgs1
1.15
1.15=0.65+0.5
PMOS
M2
l=0.36u w=40u
M4
1.1788575V
1.1788574V
vout1
vout2
C1
0.3p
C2
M1
M3
NMOS
l=0.36u w=20u
403.64066mV
M7
l=0.36u w=10.332u
639.8468mV
M6
M5
l=0.36u w=46u

SPICE ERROR LOG

Semiconductor Device Operating Points:

--- BSIM3 MOSFETS ---

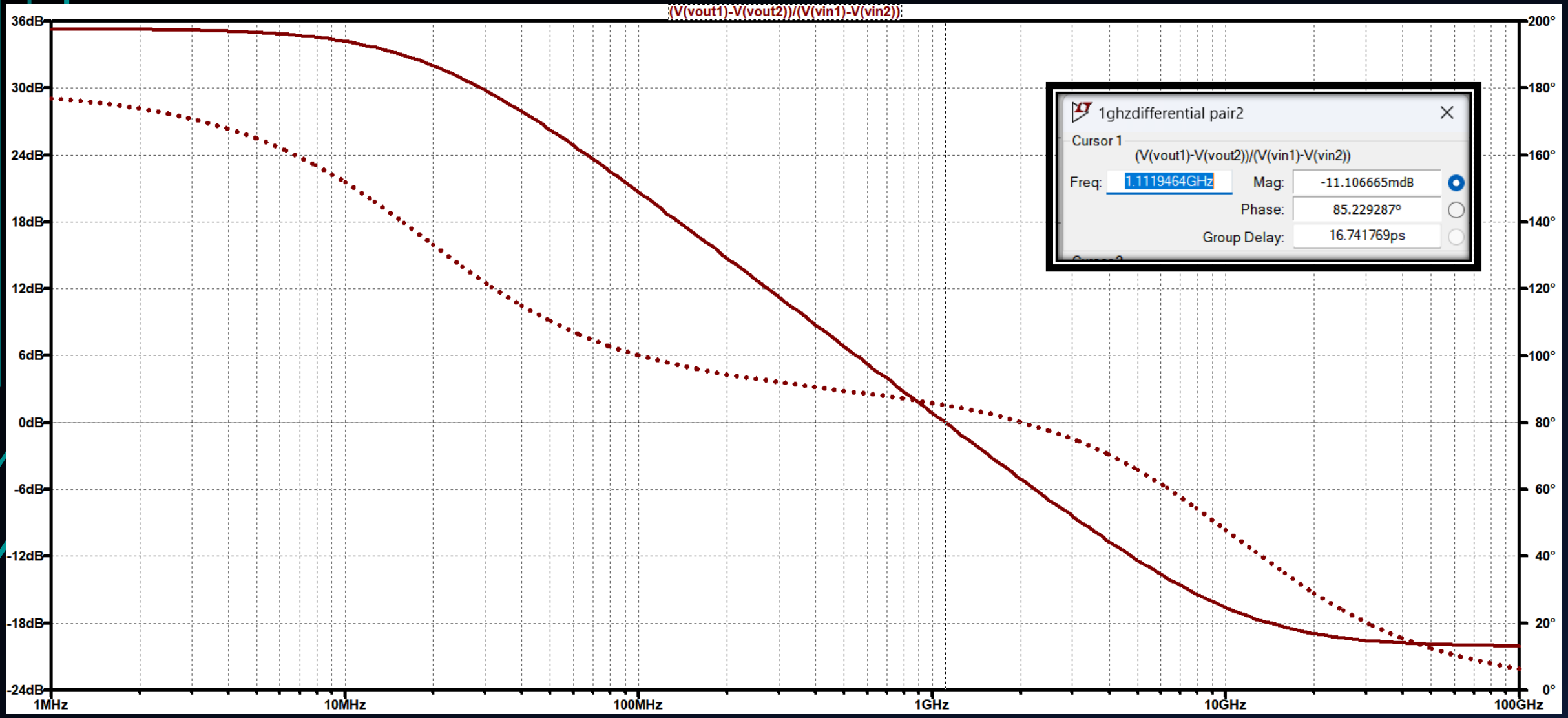
Name:	m7	m4	m2	m6	m5
Model:	pmos	pmos	pmos	nmos	nmos
Id:	-3.95e-04	-1.91e-04	-1.91e-04	3.95e-04	3.82e-04
Vgs:	-1.16e+00	-6.90e-01	-6.90e-01	6.40e-01	6.40e-01
Vds:	-1.16e+00	-6.21e-01	-6.21e-01	6.40e-01	4.04e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	-4.73e-01	-4.73e-01	-4.73e-01	4.64e-01	4.64e-01
Vdsat:	-5.39e-01	-1.94e-01	-1.94e-01	1.35e-01	1.35e-01
Gm:	9.73e-04	1.63e-03	1.63e-03	5.07e-03	4.94e-03
Gds:	2.79e-05	1.75e-05	1.75e-05	4.99e-05	6.26e-05
Gmb	3.28e-04	5.21e-04	5.21e-04	1.33e-03	1.29e-03
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	7.35e-15	2.84e-14	2.84e-14	3.54e-14	3.54e-14
Cgdov:	7.35e-15	2.84e-14	2.84e-14	3.54e-14	3.54e-14
Cgbov:	3.11e-19	3.11e-19	3.11e-19	3.33e-19	3.33e-19
dQgdVgb:	3.74e-14	1.45e-13	1.45e-13	1.78e-13	1.79e-13
dQgdVdb:	-7.35e-15	-2.85e-14	-2.85e-14	-3.54e-14	-3.55e-14
dQgdVsb:	-2.97e-14	-1.13e-13	-1.13e-13	-1.35e-13	-1.35e-13

Name:	m3	m1
Model:	nmos	nmos
Id:	1.91e-04	1.91e-04
Vgs:	7.46e-01	7.46e-01
Vds:	7.75e-01	7.75e-01
Vbs:	-4.04e-01	-4.04e-01
Vth:	5.73e-01	5.73e-01
Vdsat:	1.45e-01	1.45e-01
Gm:	2.36e-03	2.36e-03
Gds:	2.30e-05	2.30e-05
Gmb	5.39e-04	5.39e-04
Cbd:	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00
Cgsov:	1.54e-14	1.54e-14
Cgdov:	1.54e-14	1.54e-14
Cgbov:	3.33e-19	3.33e-19

--- Transfer Function ---

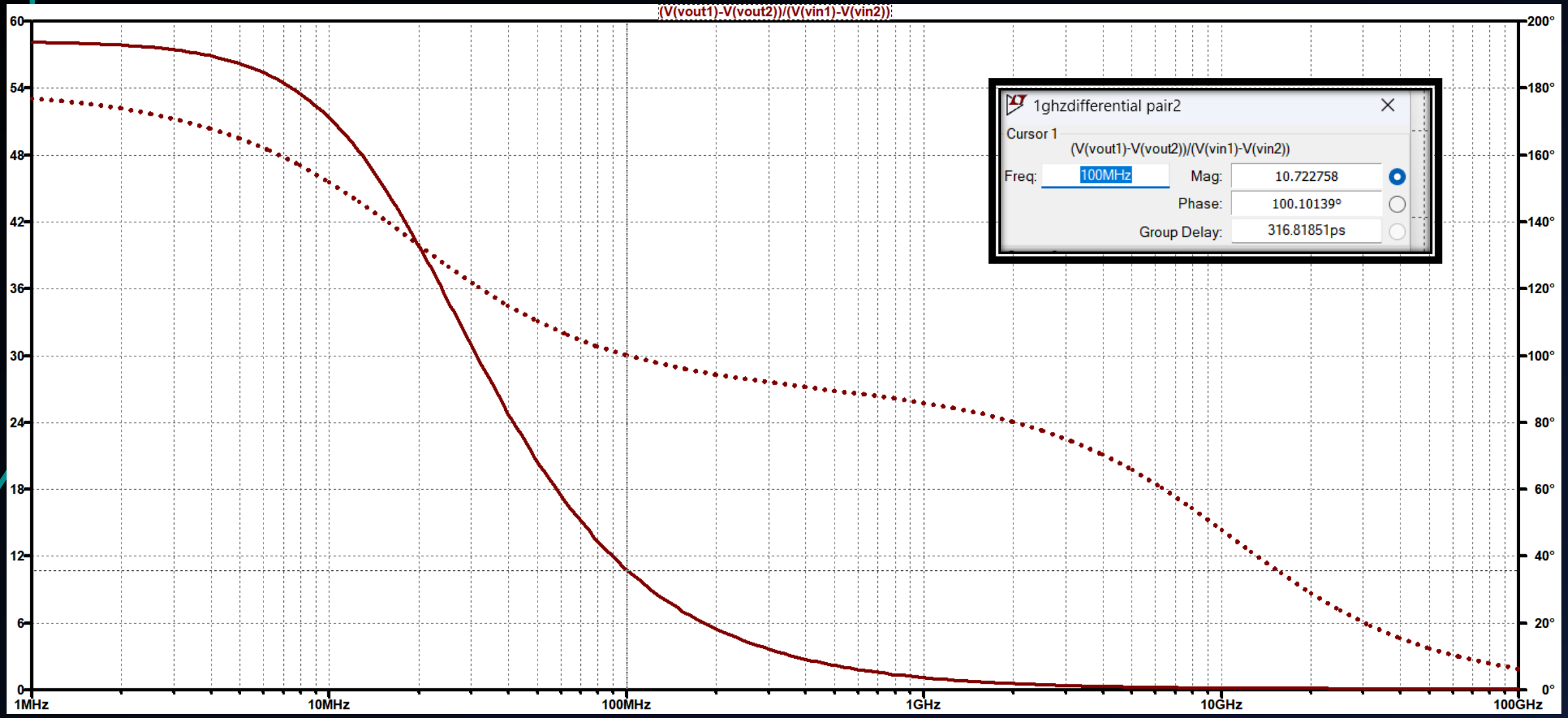
Transfer_function:	-58.179	transfer
vin1#Input_impedance:	1e+020	impedance
output_impedance_at_V(vout1,vout2):	49365	impedance

FREQUENCY RESPONSE



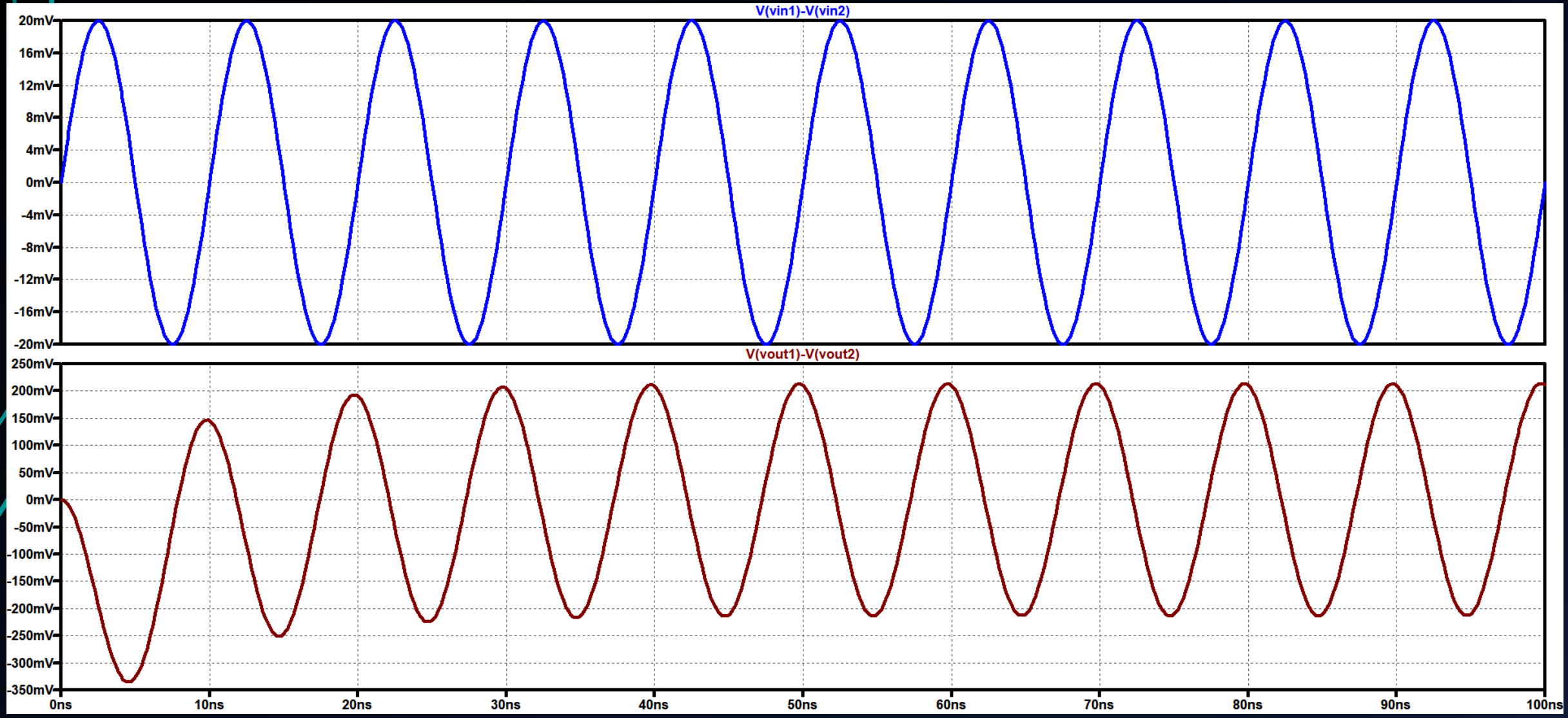
GBW=1.119GHz

FREQUENCY RESPONSE



AT 100MHz Gain = 10.722

TRANSIENT ANALYSIS



If 10mV signal is given at 100MHz then we can observe from here Gain is nearly 10

THANK YOU