CMOS Inverter Design and GDSII Generation using Cadence Virtuoso (GPDK90)

Contents

1 Introduction

This report documents the complete design and analysis process of a CMOS inverter using **Cadence Virtuoso** and the **GPDK90** technology library. The design workflow spans from schematic creation to GDSII file generation, encompassing pre-layout and post-layout simulations, delay analysis, RC parasitics extraction, and validation through DRC and LVS checks.

The primary goal was to implement the CMOS inverter and perform a detailed comparison of pre-layout and post-layout simulation results.

2 Tools and Technologies

- **Cadence Virtuoso**
- **GPDK90 technology**

3 Project Workflow

3.1 Schematic Design

The CMOS inverter schematic was created in Cadence Virtuoso, followed by symbol generation for reuse in simulations and testbenches.

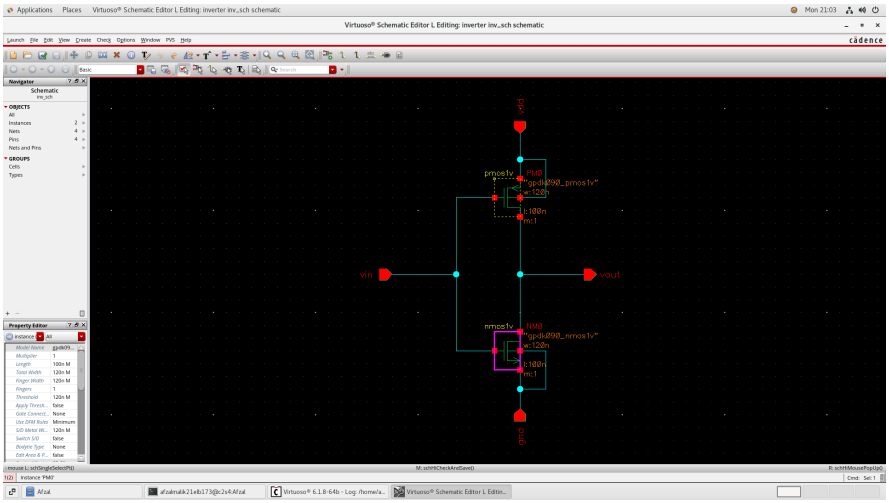

Figure 1: CMOS Inverter Schematic

3.2 Testbench Setup

A testbench was designed to simulate the behavior of the CMOS inverter and validate its output characteristics.

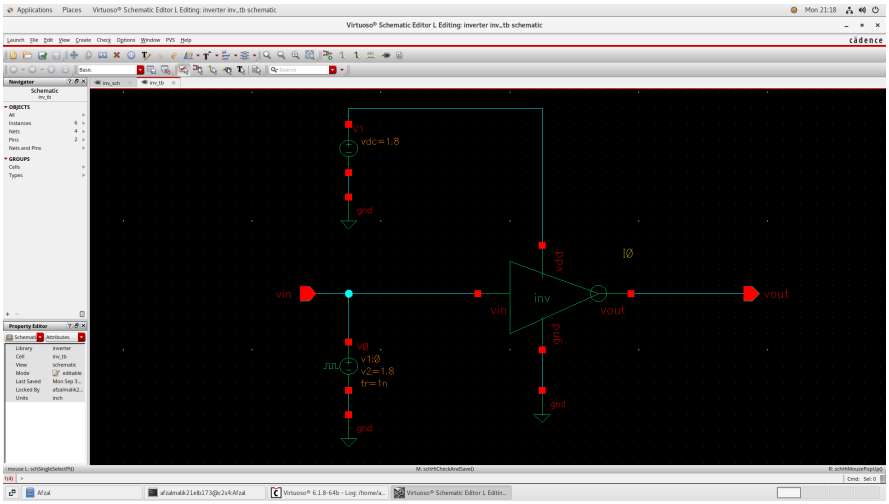

Figure 2: Testbench Setup

3.3 Analysis Setup

The Analog Design Environment (ADE) was configured for transient and DC sweep analyses, focusing on obtaining the Voltage Transfer Characteristics (VTC) and threshold voltage.

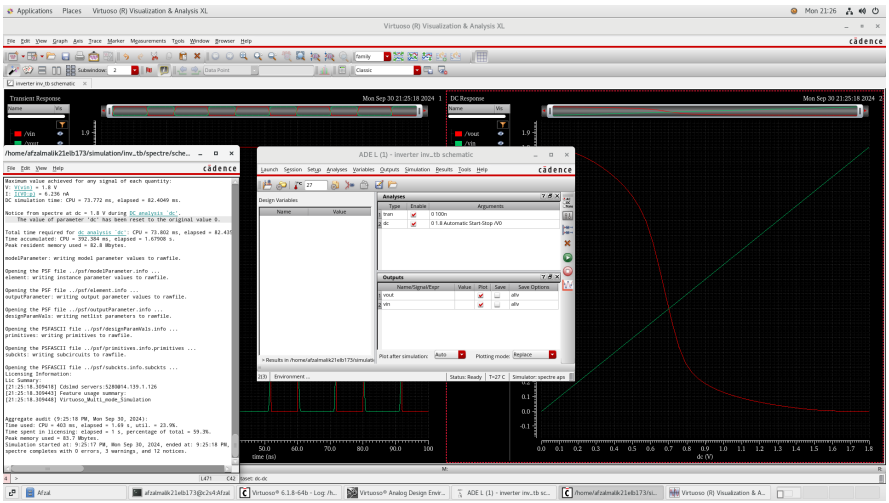

Figure 3: Analysis Setup in ADE

3.4 Simulation Results

The inverter's Voltage Transfer Characteristics (VTC) and threshold voltage were measured through transient and DC sweep analyses.

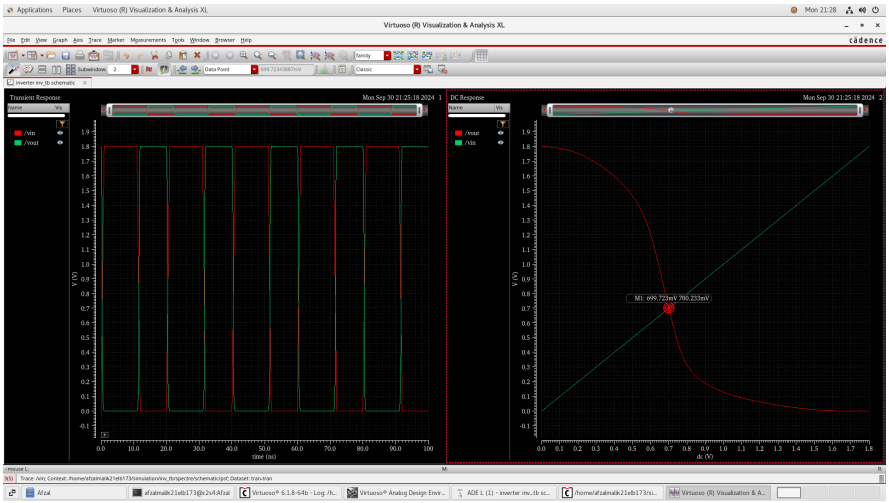

Figure 4: Voltage Transfer Characteristics (VTC) and Threshold Voltage

3.5 Layout Design

The layout of the CMOS inverter was designed, following the specifications of GPDK90 technology. This layout forms the foundation for DRC and LVS checks.

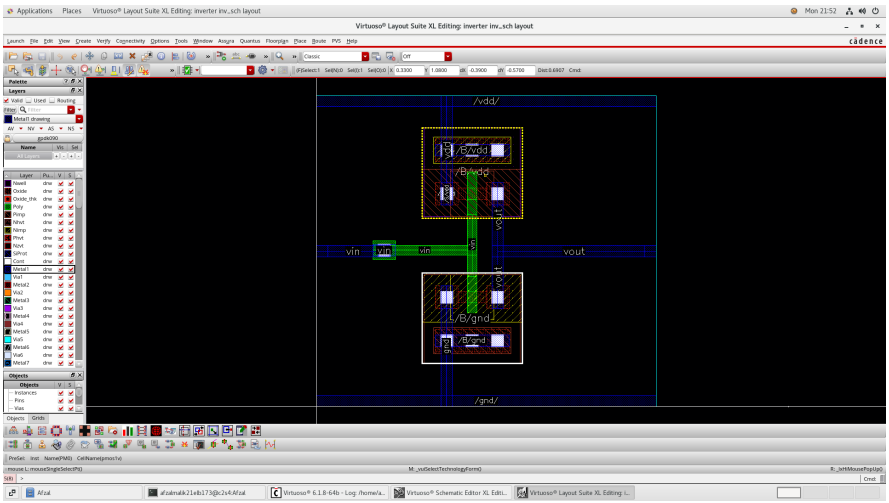

Figure 5: CMOS Inverter Layout

3.6 DRC and LVS Checks

Design Rule Check (DRC) and Layout Versus Schematic (LVS) checks were performed to verify that the layout complies with fabrication rules and matches the schematic.

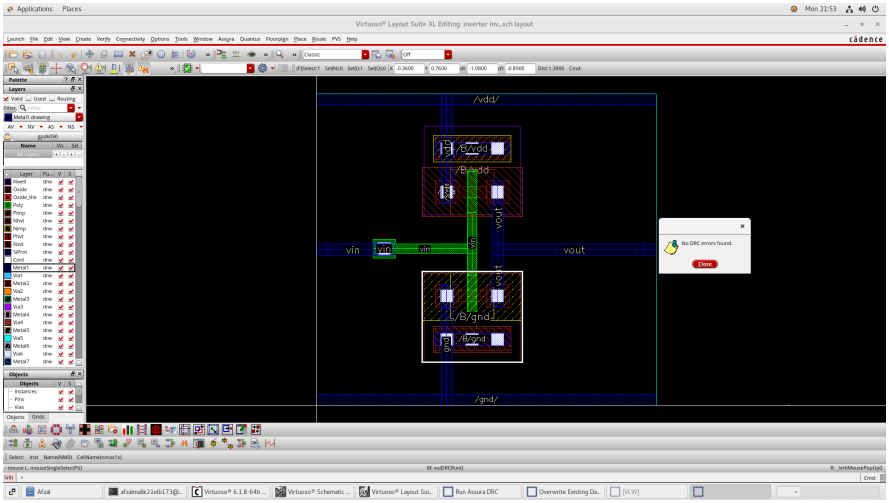

Figure 6: Design Rule Check (DRC) Passed

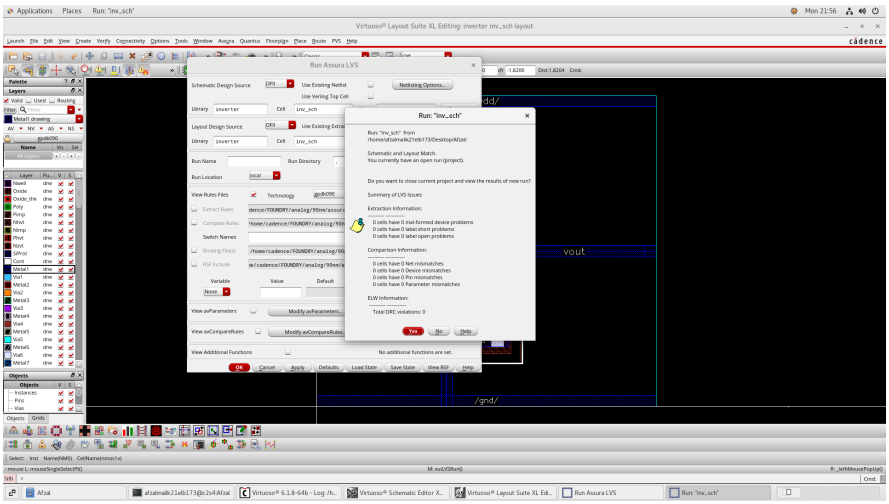

Figure 7: LVS Check Passed

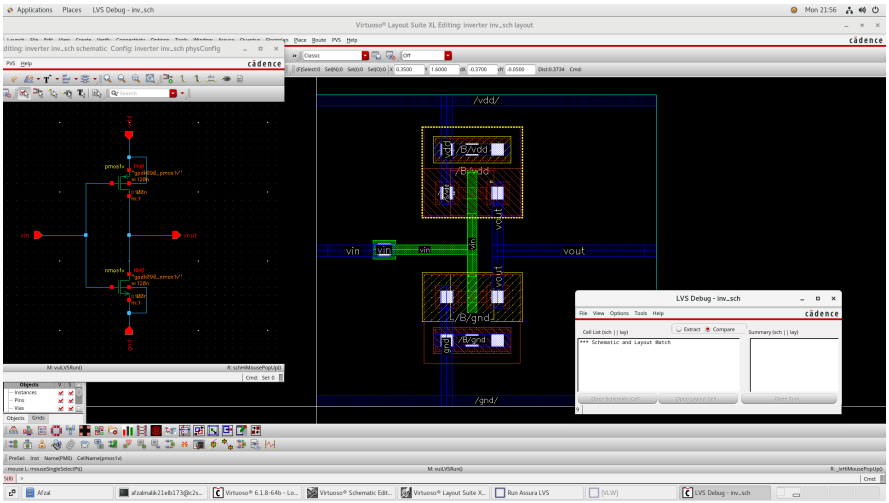

Figure 8: LVS Results

3.7 RC Parasitics Extraction

RC parasitics were extracted from the layout to account for resistive and capacitive elements, which affect the circuit's performance in post-layout simulations.

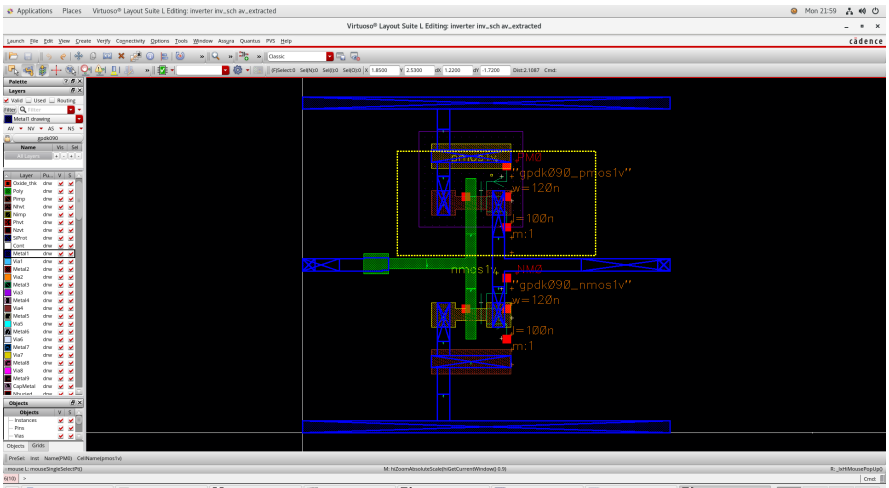

Figure 9: RC Extraction Results

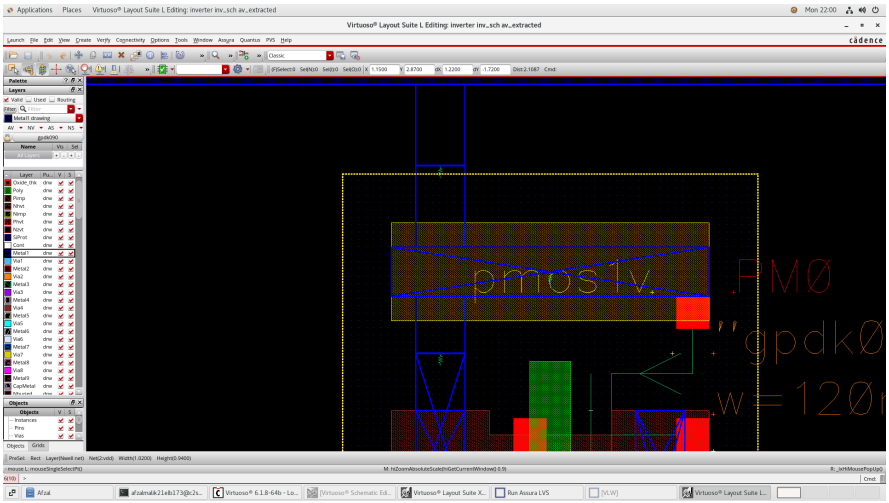

Figure 10: Zoomed RC Extraction Layout

3.8 Pre-Layout and Post-Layout Simulations

Simulations were performed on both pre-layout and post-layout designs to compare performance metrics such as delay.

3.8.1 Pre-Layout Results

The delay measured in pre-layout simulations was found to be 115.1 ps.

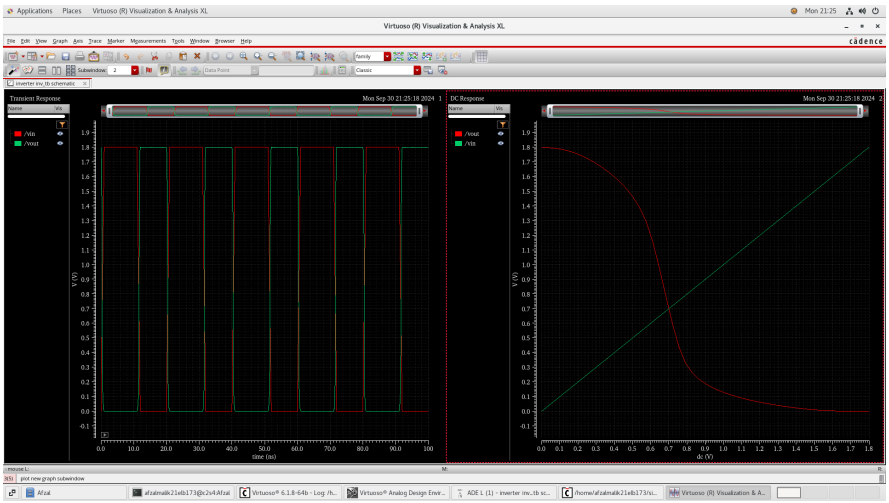

Figure 11: Pre-Layout Simulation

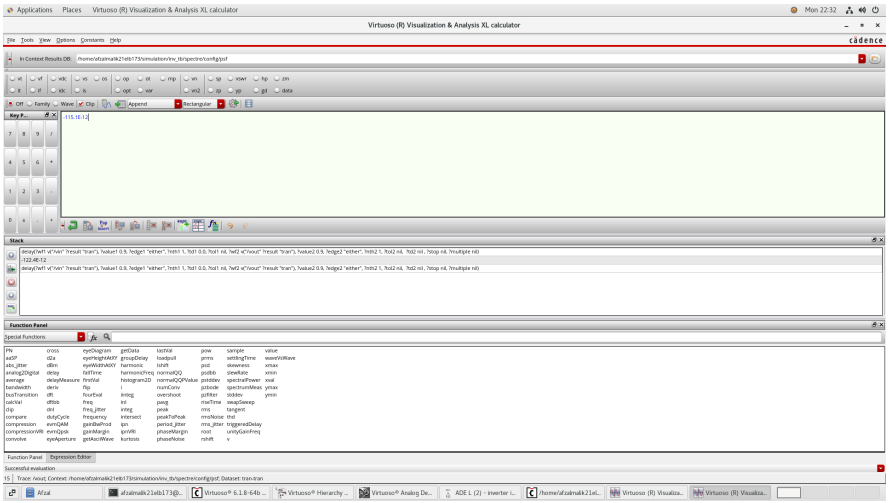

Figure 12: Delay from Input to Output (Pre-Layout)

3.8.2 Post-Layout Results

Post-layout simulations showed an increase in delay to 122.4 ps due to parasitic effects.

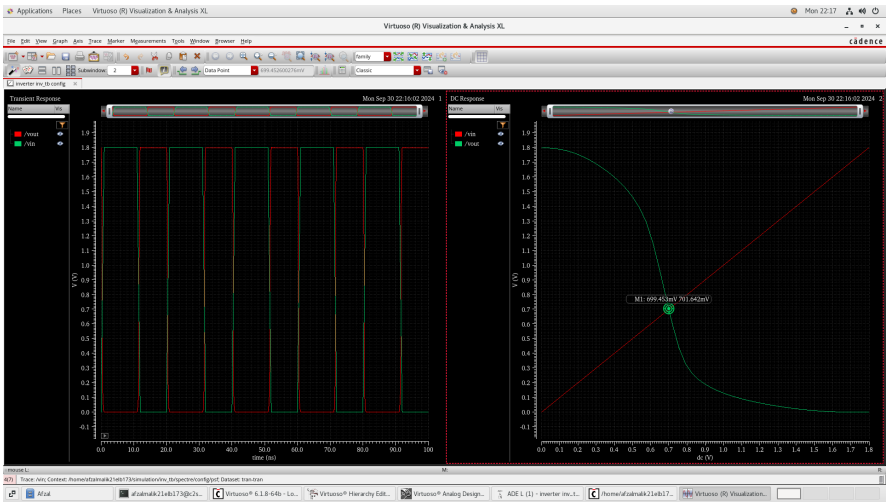

Figure 13: Post-Layout Simulation

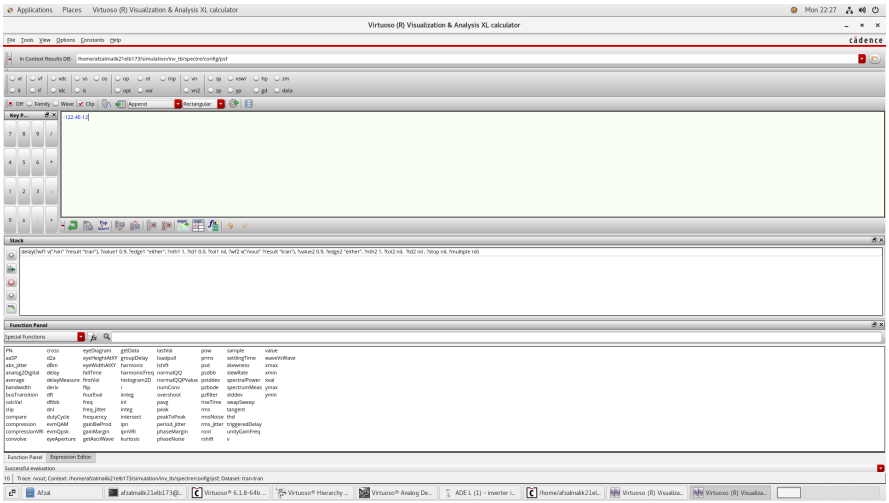

Figure 14: Delay from Input to Output (Post-Layout)

3.9 GDSII File Generation

The final layout was exported in GDSII format, ready for tape-out and further fabrication steps.

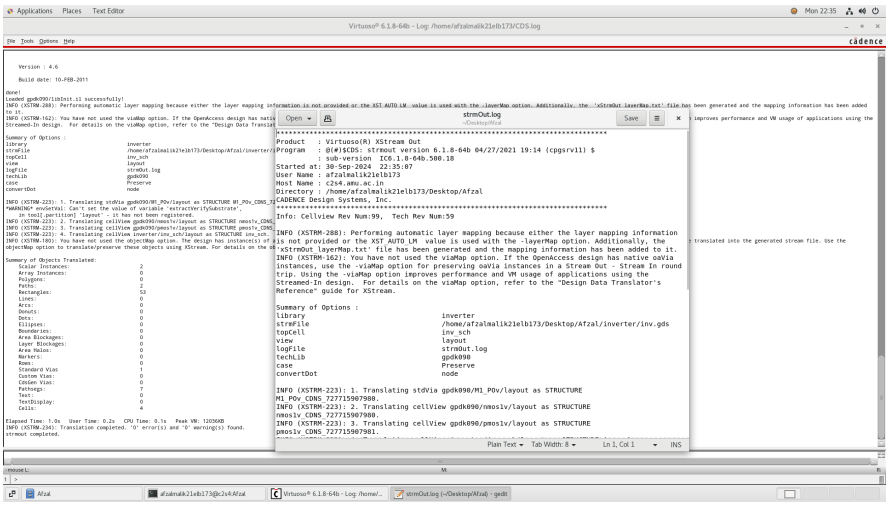

Figure 15: GDSII Export of CMOS Inverter

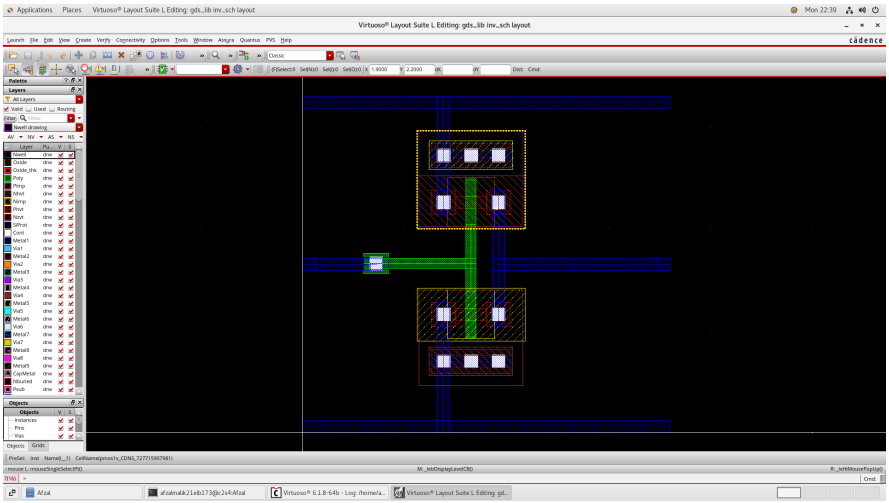

Figure 16: GDSII Layout Visualization

4 Conclusion

The project successfully covered the design, simulation, and layout of a CMOS inverter using Cadence Virtuoso. A comparison between pre-layout and post-layout simulation results indicated a slight increase in delay due to parasitics. The final GDSII file is prepared and validated for fabrication.

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