Department of Electronics Engineering, AMU

Presentation of UG Project (Phase II)

Design of Phase-Locked Loop (PLL)

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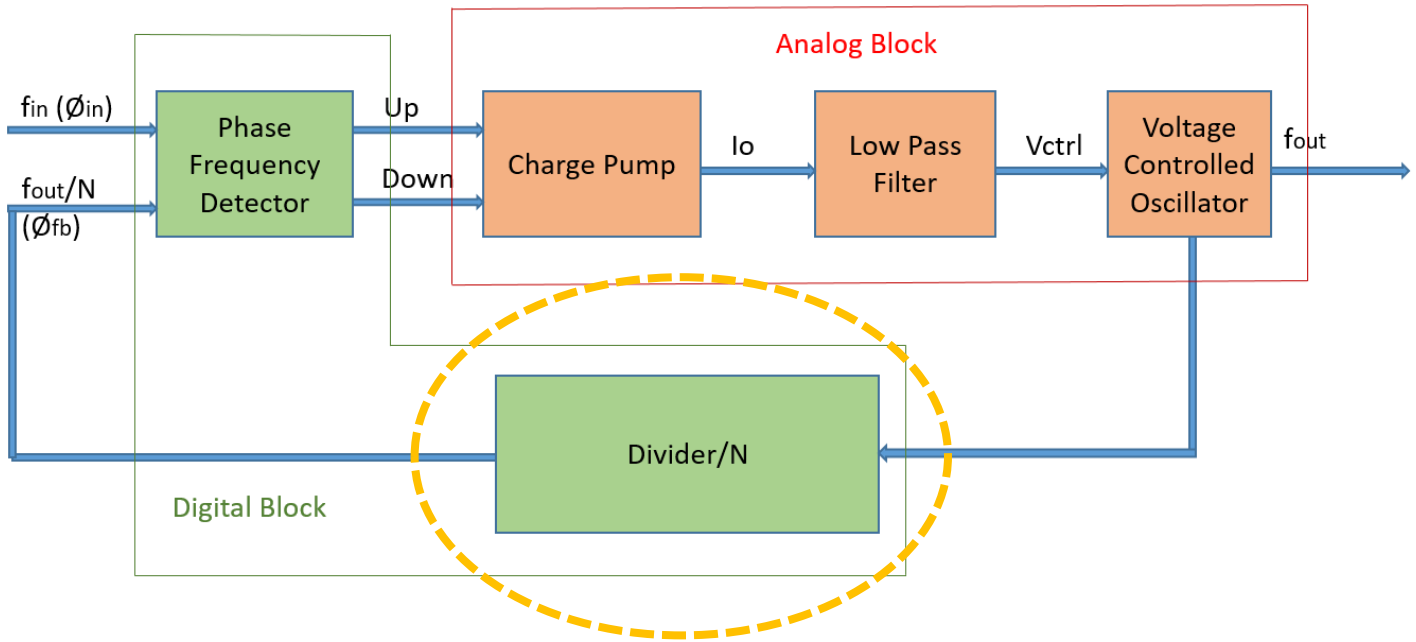
Design of PLL

- **Technology Node :** 180nm | **Tools Used :** LT Spice
- The Phase-Locked Loop (PLL) is a feedback system that creates a frequency from a Voltage Controlled Oscillator (VCO) that is synchronous to the input signal.
- It is a Mixed block which uses a Phase Frequency Detector (PFD) and Divide by N network as Digital Block and Charge Pump (CP), Low Pass Filter and Voltage Control Oscillator as Analog Block.

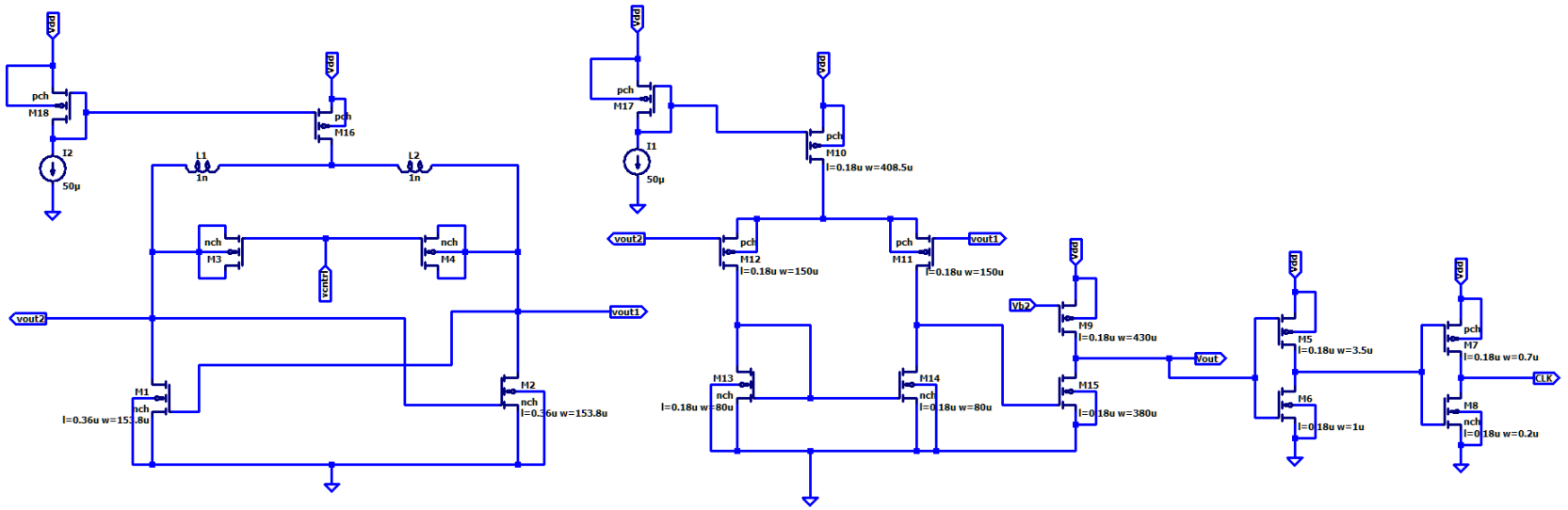


Block Diagram of Phase-Locked Loop

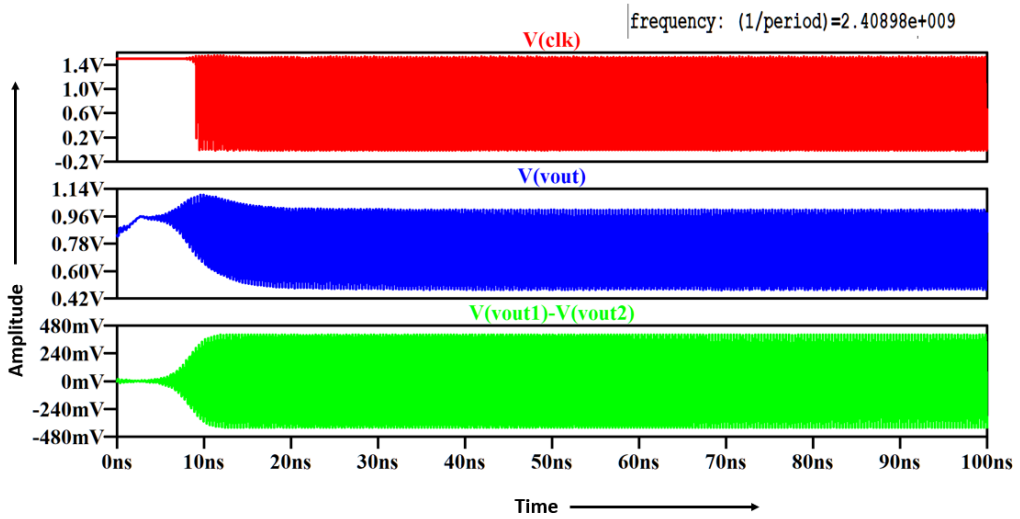
Design of Voltage Controlled Oscillator (VCO)

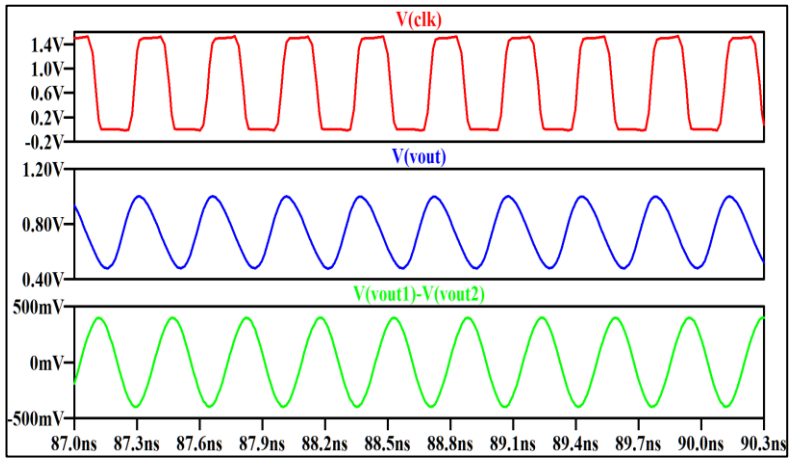
Design of LC VCO for 2.4 GHz frequency at Vcntrl = 0.6 V

Schematic:



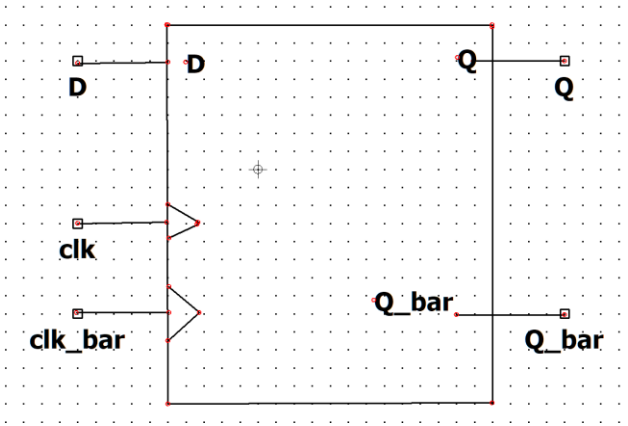
TRANSIENT ANALYSIS

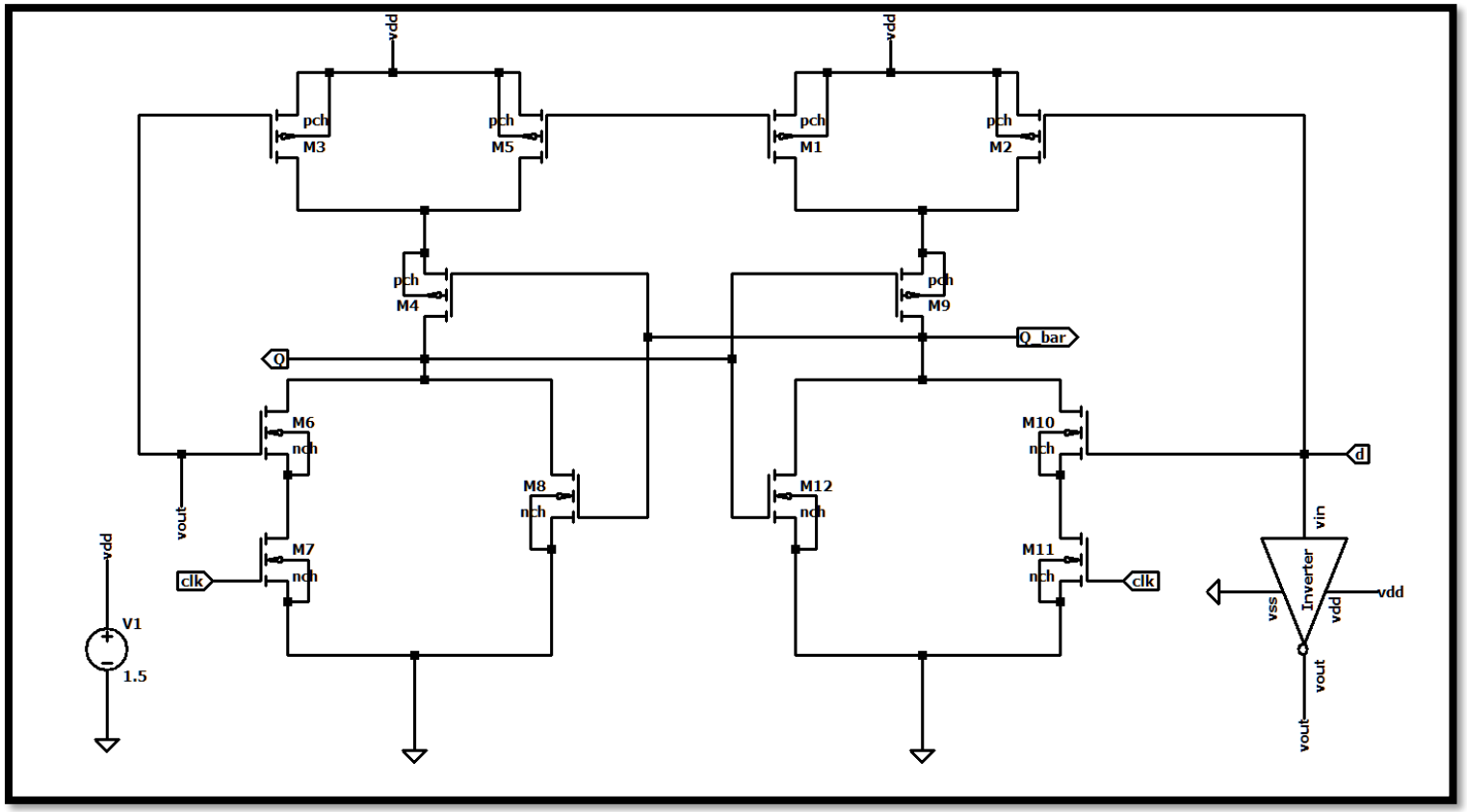




DESIGN OF DIVIDER CIRCUIT

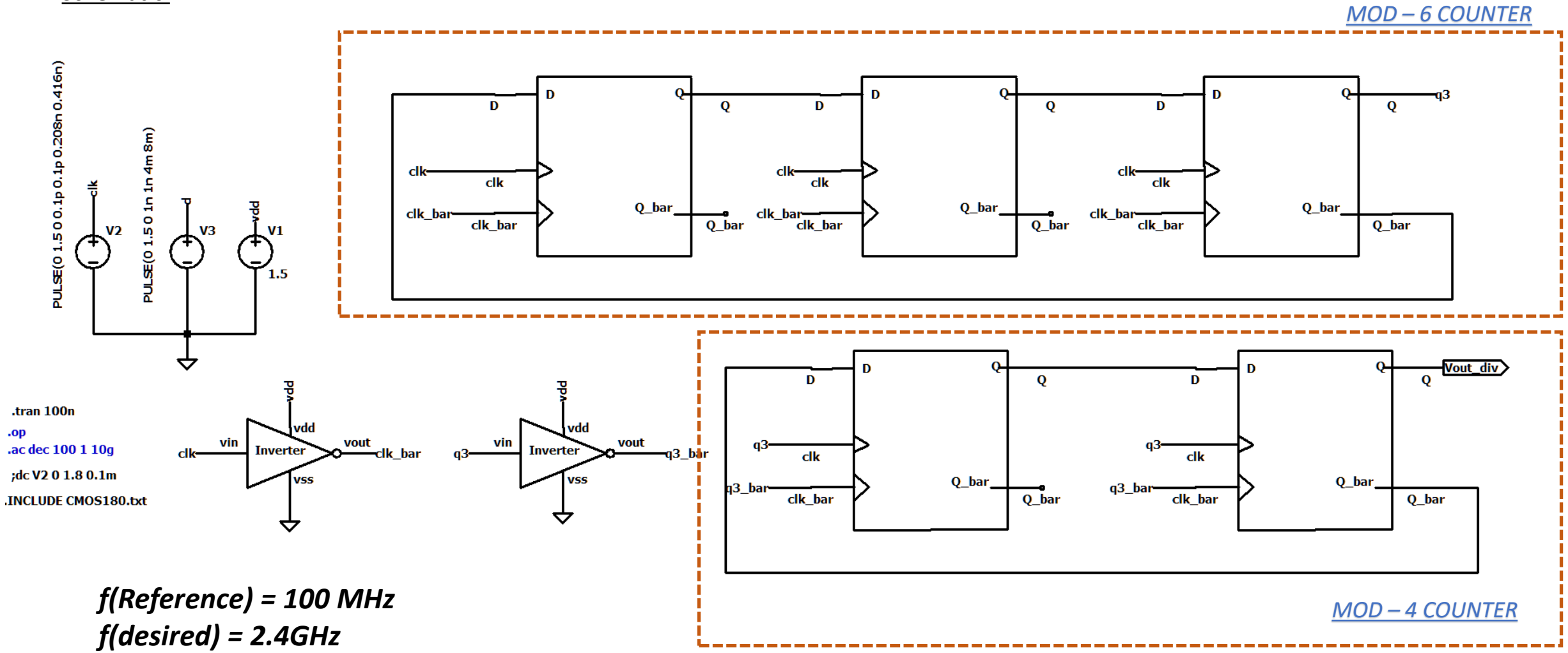
CMOS IMPLEMENTATION OF D FLIP FLOP





DESIGN OF DIVIDER CIRCUIT

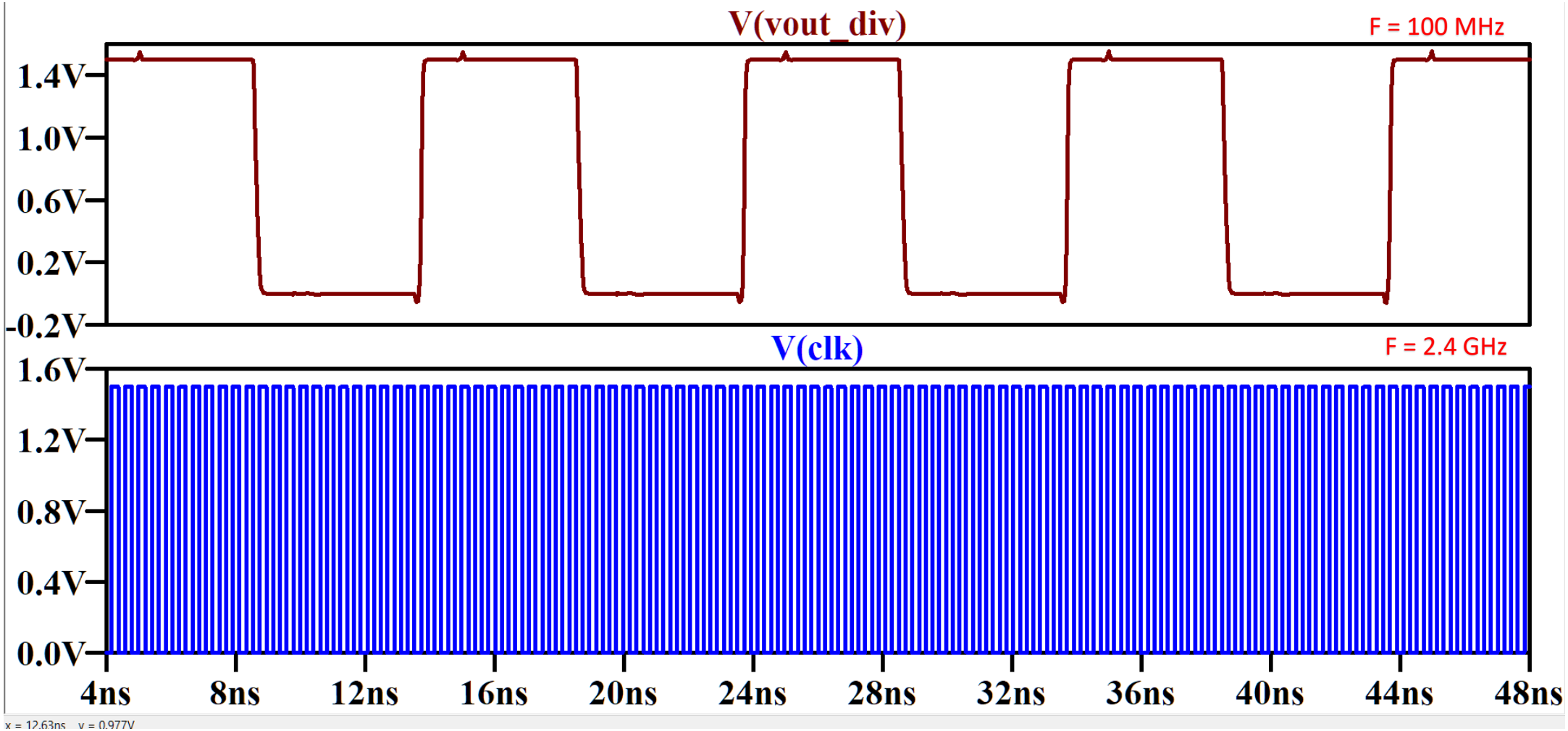
Schematic:



f(Reference) = 100 MHz
f(desired) = 2.4GHz
MOD No. = f(desired) / f(Reference)

Simulation Results:

Transient Analysis:



References

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[2]. LC Tank Voltage Controlled Oscillator tutorial. UW ASIC Analog Group, Waterloo, Ontario, Canada, 2005. https://www.academia.edu/26763368/LC_Tank_Voltage_Controlled_Oscillator_Tutorial

[3]. C. -H. Yen, M. Nasrollahpour and S. Hamedi-Hagh, "Low-power and high-frequency ring oscillator design in 65nm CMOS technology," 2017 IEEE 12th International Conference on ASIC (ASICON), Guiyang, China, 2017, pp. 533-536, doi: 10.1109/ASICON.2017.8252530.

[4]. Razavi, B. (2020). Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level. Cambridge: Cambridge University Press.