PHASE LOCKED LOOP DESIGN USING COTS IC's

MINI PROJECT REPORT

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STUDENTS' DECLARATION

I hereby certify that the work which is being presented in this project report entitled **"PHASE LOCKED LOOP DESIGN USING COTS IC's"** in partial fulfilment of the requirements for the award of the Degree of Bachelor of Technology and submitted in the Department of Electronics Engineering of the Zakir Husain College of Engineering & Technology, Aligarh Muslim University, Aligarh is an authentic record of my own work carried out during third year of B. Tech. under the guidance of **Prof. Naushad Alam**, Professor, Department of Electronics Engineering, Aligarh Muslim University, Aligarh.

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This is to certify that the above statement made by students is correct to the best of my knowledge.

(Prof. Naushad Alam)
Project Supervisor

Date:

ABSTRACT

Phase-locked loops (PLLs) are integral components of modern electronic systems, facilitating the generation of high-quality, stable clock signals crucial for telecommunications, computing, and various electronic devices. Their programmable frequency adjustment capability enhances versatility across a broad range of applications. However, traditional PLL designs, amalgamating analog and digital circuitry, demand specialized expertise for development. As chip technology advances, the need for higher frequency clocks intensifies, presenting challenges in signal stability and quality. This project examines the evolution of on-chip clock generators, focusing on PLLs as preferred solutions for producing stable, low-jitter clock signals. Despite their complexity, PLLs demonstrate proficiency in generating on-chip clocks with low jitter levels comparable to stable reference sources. The emergence of digital PLL designs offers more compact and energy-efficient alternatives, although achieving equivalent output signal quality remains a challenge. This project delves into the development and challenges of PLLs, underscoring their critical role in contemporary electronic systems.

ACKNOWLEDGEMENTS

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF ABBREVIATIONS

COTS	Commercially Off the Shelf
PLL	Phase Locked Loop
PFD	Phase Frequency Detector
LPF	Low Pass Filter
VCO	Voltage Controlled Oscillator
K_{VCO}	Sensitivity of VCO

PHASE-LOCKED LOOPS

1.1 Overview:

The Phase-locked loops (PLL) have a variety of applications in the areas of telecommunication, computers and other electronic devices. PLL circuits have outstanding capability of generating very high-quality stable clock signals. They are also very useful as they can be programmed to change their output frequency over a wide range of frequencies and thus are very flexible [ref]. Having the capability of operating at very higher frequencies leads to a key factor for their continued use and development. They are excellent for the operations in which clock frequency is not required to change very often as their stability can be achieved using a very stable reference clock source. Various chip designs typically possess distinct clocking needs, and no sole PLL circuit proves ideal for all purposes. Moreover, the amalgamation of analog and digital circuitry in traditional PLL configurations has led to the evolution of a highly specialized skill set for their circuit development. The emergence of entirely digital PLL designs offers more compact and energy-efficient alternatives in numerous applications. However, they have not yet attained the equivalent standard of output clock signal quality as traditional PLL circuits [ref].

1.2 Introduction:

As chip technology progressed and circuit speeds increased, the demand for higher frequency clocks escalated. However, providing a high-frequency, high-quality clock directly onto a chip proved challenging, especially for operational frequencies exceeding a few hundred MHz Generating a stable high-frequency clock was not only daunting, but transmitting it to chips via

traces on a printed circuit board posed a significant obstacle. At these elevated frequencies, the dimensions of wire traces and their proximity to neighboring wires caused degradation in the clock signal waveform. Additionally, signal coupling from the clock wire to adjacent data wires introduced noise onto the data lines. Moreover, the clock wires functioned as antennas, emitting radiation that interfered with other circuits. These challenges spurred the development of various techniques for generating on-chip high-frequency clocks. These on-chip clock generators range from small ring oscillator designs, characterized by poor stability and high sensitivity to environmental factors such as supply voltage and temperature, to larger circuits capable of producing high-quality, stable clocks.

Phase-Locked Loop (PLL) clock generator circuits, although bulky, emerged as the preferred choice for clocking chips due to their ability to produce highly stable, low jitter, on-chip clock signals. Another benefit lies in their ability to program the output frequency, although adjusting it may require many tens to hundreds of clock cycles. PLLs employ a high-quality, stable, and low-frequency reference clock source, typically located off-chip. Their output clock signal typically multiplies the reference frequency, ensuring low jitter levels comparable to those of the reference source. Typically, stable reference clock sources utilize a quartz crystal to regulate their oscillation frequency.

1.3 Design of PLL:

The fundamental concept of PLL is depicted in the figure 1.1:

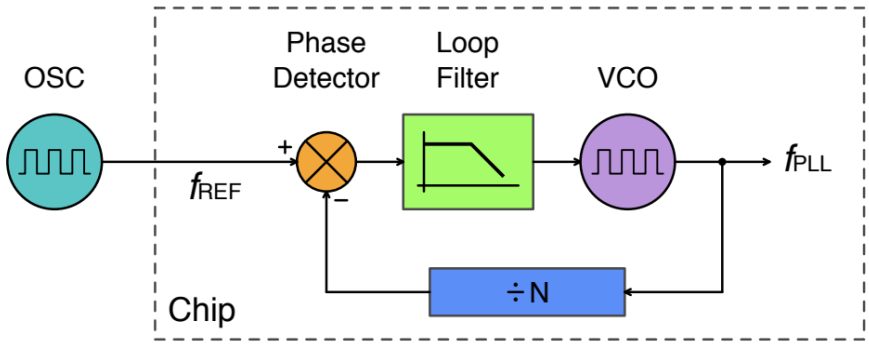


Fig. 1.1. Basic PLL design utilizing off-chip frequency source and generating on-chip clock signal

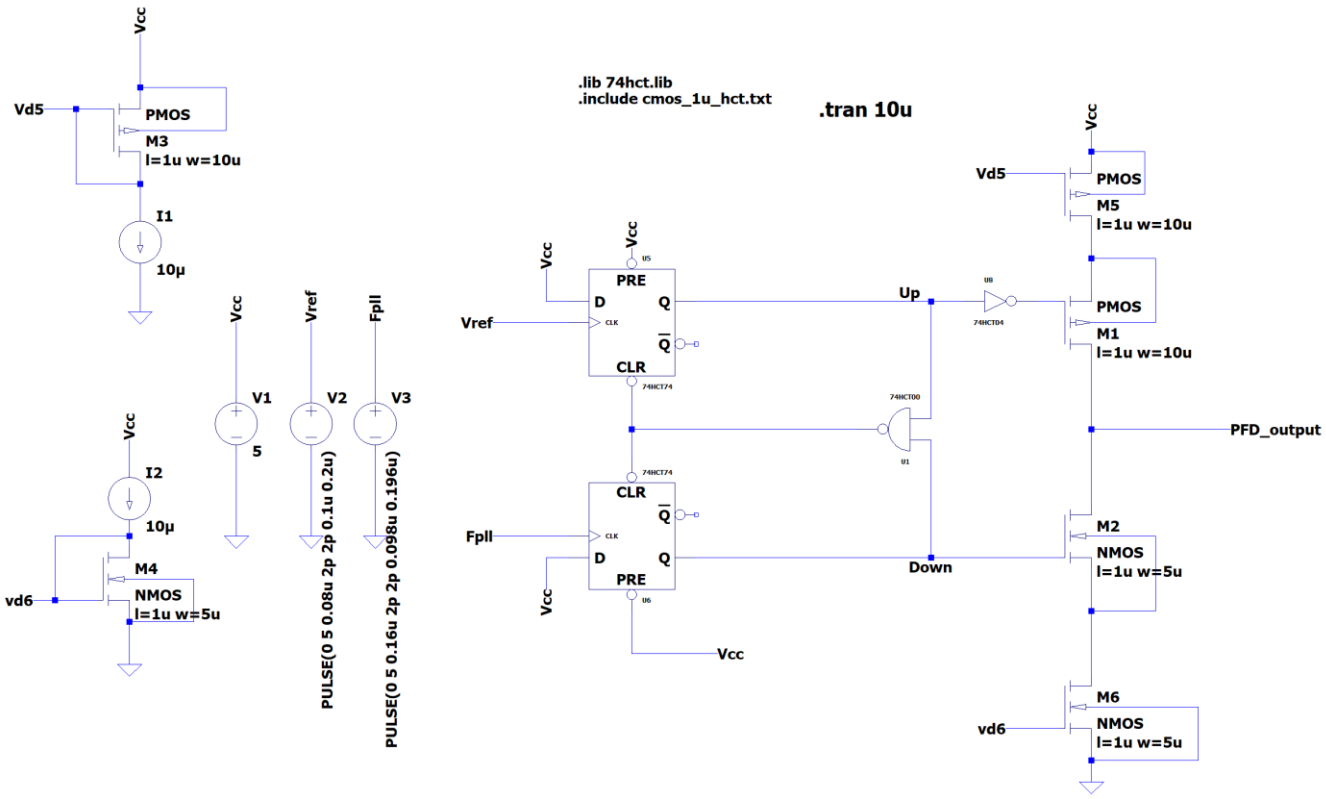
The PLL circuit utilizes an off-chip oscillator, often a high-quality stable quartz crystal reference frequency oscillator, having frequency f_{REF} denoted as OSC. All other components of the PLL are integrated on-chip. A Voltage Controlled Oscillator (VCO) serves as the second oscillator, responsible for generating the output clock signal from the PLL, having frequency f_{PLL}. Both oscillators produce square wave signals. A negative feedback loop channels the VCO output signal to the Phase Detector, where it undergoes subtraction from the incoming reference signal. Subsequently, the Phase Detector generates a sequence of pulses whose widths correspond to the phase difference between the two input signals. These pulses then pass through the Loop Filter, which produces the analog control voltage for the VCO. When the phase of f_{REF}, precedes that of f_{PLL}, a sequence of positive pulses is triggered, resulting in an increment in the rising positive VCO control voltage, thus elevating the frequency of the VCO. Conversely, if the phase of f_{PLL} precedes that of f_{PLL}, negative pulses diminish the frequency of the VCO. In this manner, the control loop of the PLL ensures that f_{PLL} matches the frequency of f_{REF} while also preserving a consistent phase offset between them. The feedback loop of a PLL facilitates the convergence of the output signal to its intended frequency and synchronizes it with the phase of the reference clock.

1.4 Components of PLL:

1. Phase Frequency Detector:

The Phase Frequency Detector (PFD) circuit is selected due to its advanced capabilities surpassing those of a conventional phase detector. Its design enables simultaneous response to both phase variance and input frequency, ensuring efficient operation across a broad frequency spectrum.

Fig. 1.2. Design Of Phase Frequency Detector Circuit



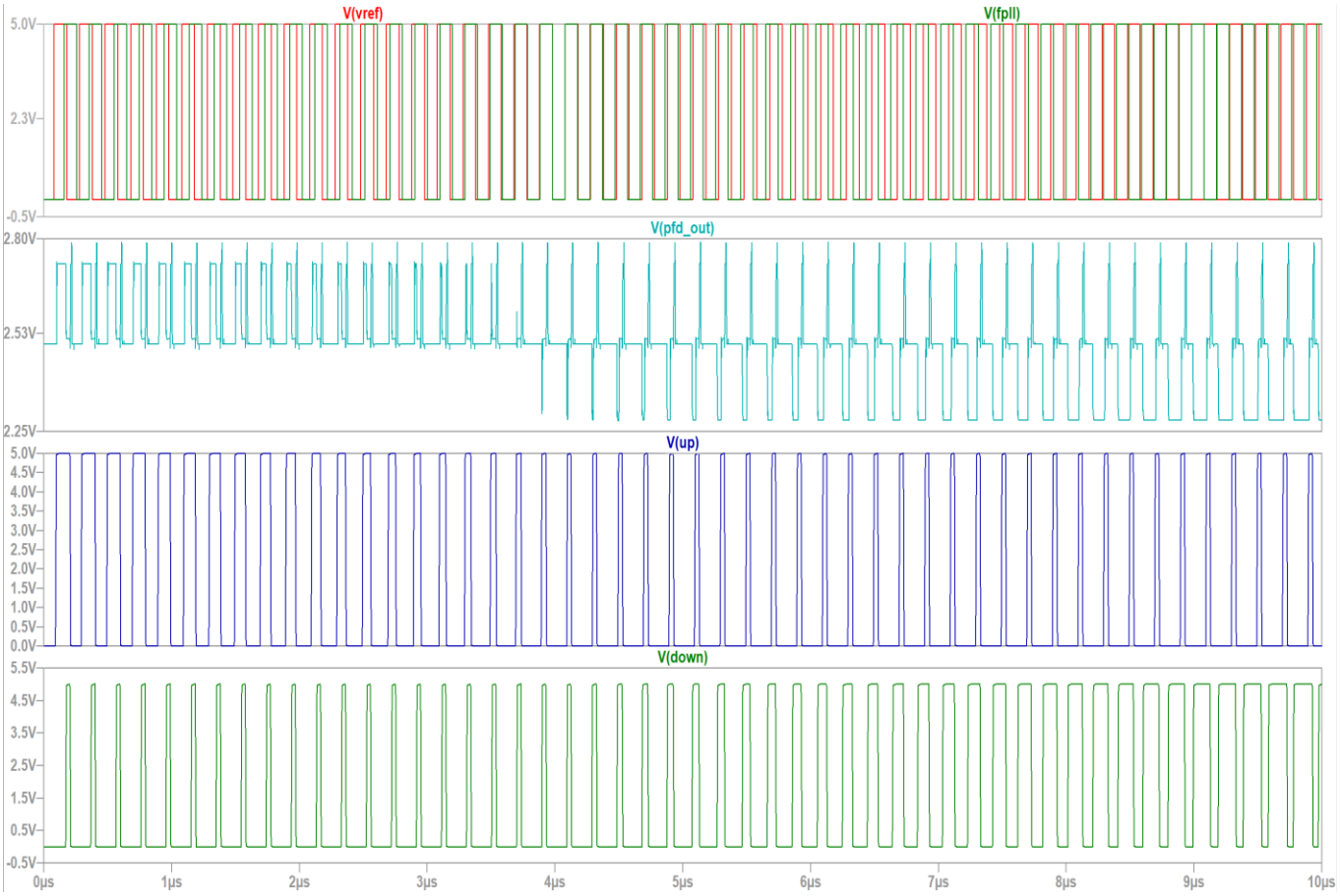


Fig. 1.3. Simulation Output of Phase Frequency Detector Circuit

These flip-flops are arranged to generate a logical high output following each rising clock edge. Subsequent to this, an AND gate, along with a delay element, resets both flip-flops once their outputs reach a logical high state. Consequently, pulses are generated on the Q output signals q_P and q_N respectively. The duration of these pulses corresponds to the phase differential between f_{REF} and f_{PLL}, with q_P exhibiting a longer duration than q_N in scenarios where f_{REF} precedes f_{PLL}, and vice versa. The q_P signal is employed to raise the PFD_{OUT} output, while q_N is utilized to lower the PFD_{OUT} output. An exemplar representation of timing waveforms for the PFD circuit is provided in Figure 1.4, depicting instances where f_{REF} and f_{PLL} possess similar frequencies but differing phase offsets. The upper portion of the figure demonstrates a scenario where the phase

of f_{REF} precedes that of f_{PLL}, resulting in brief high-polarity pulses on PFD_{OUT}, which marginally elevates the frequency of f_{PLL}, thereby diminishing the phase disparity between the signals. Conversely, the lower portion of the figure showcases a scenario where the phase of f_{REF} trails that of f_{PLL}, generating brief low-polarity pulses on PFD_{OUT}, consequently slightly reducing the frequency of f_{PLL} and once again reducing the phase difference between the signals.

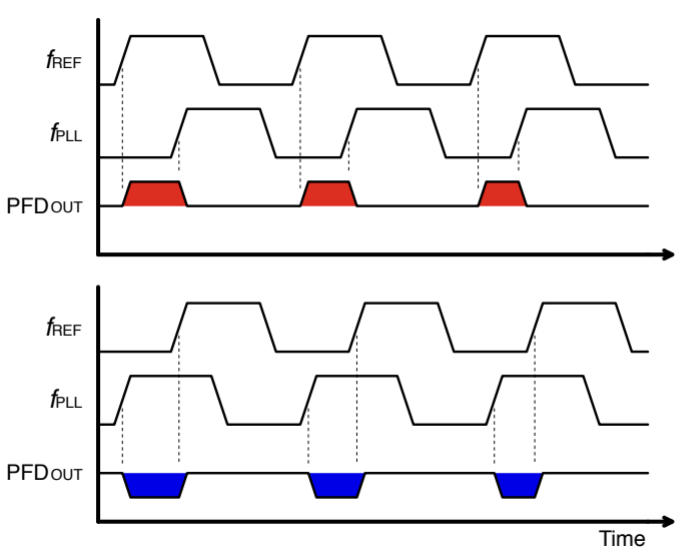


Fig. 1.4. Phase Frequency Detector Circuit Timing Waveform

The flip-flops generate pulses on q_P and q_N outputs, their durations correlating with the phase disparity between f_{REF} and f_{PLL}. Incorporating a delay element guarantees the presence of these pulses, maintaining a minimum width. The output circuit combines the pulse signals from q_P and q_N into PFD_{OUT}. This integration ensures the production of positive-going pulses when f_{PLL} leads f_{REF} in phase, and negative-going pulses when f_{PLL} lags f_{REF}.

2. Low Pass Filter:

Moving forward, our attention shifts to the Loop Filter, a pivotal component essential for stabilizing the PLL control loop. This LPF filter, commonly referred to as a Loop Filter (LF), plays a crucial role in integrating the pulses generated by the Phase Detector. Its primary function is to generate a refined and stabilized control voltage for the Voltage Controlled Oscillator (VCO), thereby ensuring the desired performance of the PLL system. For clarity, a basic schematic of a low pass filter circuit, employing an R-C combination, is provided in Figure 1.5.

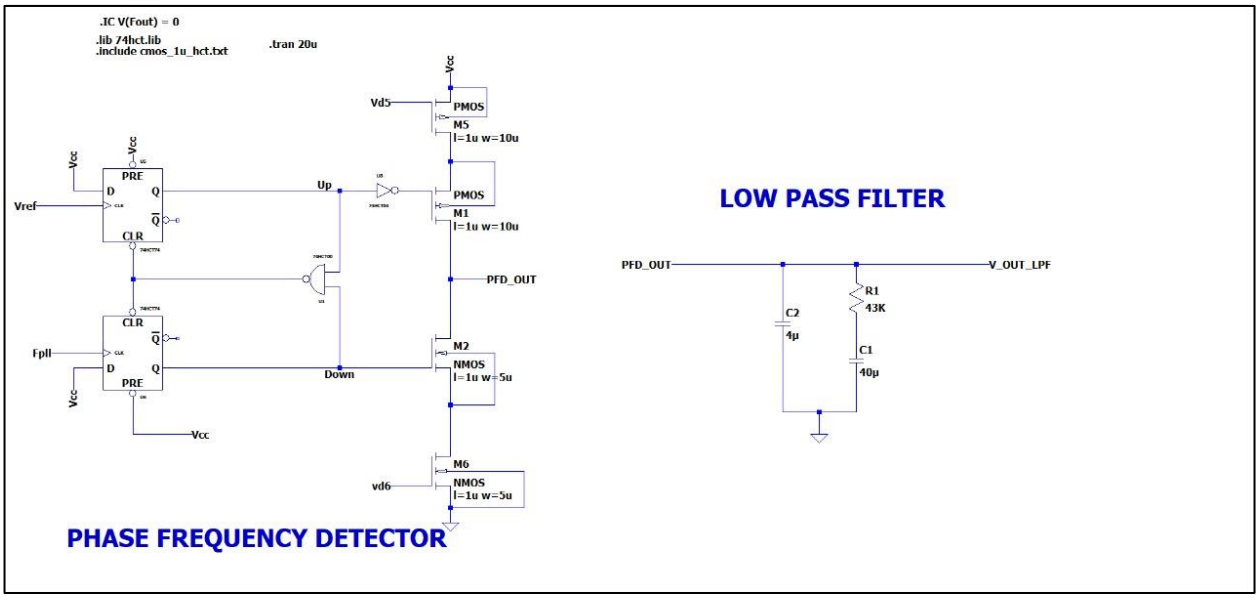


Fig. 1.5. Low Pass Filter Design

It is worth noting the criticality of the capacitor within this filter structure. When considering implementation using parallel plate capacitors utilizing metal layers within the chip, it becomes evident that such an approach would result in a significant occupation of chip area, rendering it impractical. In light of this challenge, an alternative solution is sought. As an efficient alternative, CMOS transistor gate capacitors are utilized due to their capability of offering approximately

tenfold greater capacitance per unit area. This strategic choice not only addresses the space constraint issue but also enhances the overall performance and efficiency of the system.

Nevertheless, it is essential to acknowledge that the capacitance of gate capacitors exhibits voltage dependency. To mitigate this issue and ensure a more stable performance, a configuration employing both P-transistor and N-transistor pairs is adopted. This arrangement not only reduces the circuit's sensitivity to voltage fluctuations but also enhances its overall robustness.

Design Steps:

In the design of a phase-locked loop (PLL), the low pass filter (LPF) plays a crucial role in filtering noise and unwanted high-frequency components from the control voltage input to the voltage-controlled oscillator (VCO). Leveraging the sensitivity parameter (K_{VCO}) of the VCO, we can devise an efficient LPF using one resistor and two capacitors.

Key Steps:

Determine VCO Sensitivity (K_{VCO}): Establish the sensitivity parameter (K_{VCO}) of the VCO, representing the change in VCO frequency per unit change in control voltage. Typically denoted in MHz/V or rad/s/V, K_{VCO} is essential for filter design.

Select Cutoff Frequency (Fc) or Loop Bandwidth as given by

$$F_C = F_{ref}/20$$

Estimating the desired cutoff frequency (F_C) for the LPF, defining the point where signal attenuation begins. This selection hinges on PLL bandwidth requirements and noise characteristics.

Select Resistor Value (R): Choose an appropriate resistor value (R_s) to achieve the desired cutoff frequency. Rs influences the filter's impedance and overall performance.

$$F_C = \frac{R_S I_C K_{VCO}}{2\pi N}$$

Calculate Capacitor Values (C_s and C_p): Using the formula of zero and pole frequencies F_z & F_p for finding the value of C_s & C_p using relationships given below

$$F_Z = \frac{1}{2\pi R_S C_S} \leq \frac{F_C}{3}$$

$$F_P = \frac{1}{2\pi R_S C_P} \geq 3F_C$$

Determine C_S and C_P, ensuring their equality or adjusting for specific filter response requirements. For which we use the stability relationship

$$C_s = 10 * C_p$$

Construct the LPF using one resistor and two capacitors. Connect one resistor end to the input signal and the other to the junction of the capacitors, with their other terminals grounded. This configuration forms a second-order RC low pass filter.

Verify Performance: Simulate the LPF circuit to confirm its performance using circuit simulation software. Analyze the frequency response to ensure the cutoff frequency meets specifications and provides effective filtering.

By following these steps, we can design a robust LPF for PLL applications using VCO sensitivity (K_{VCO}), ensuring stable and reliable PLL operation with effective noise filtering.

Design Parameters:

F_{ref} = 35 MHz
F_C = 250 KHz
R_S = 3.7 KΩ
$F_Z \leq$ 83.3KHz
$F_P \geq$ 750KHz
C_s = 516 pF
C_p = 57.3 pF

3. Voltage Controlled Oscillator:

A multitude of circuit designs have showcased remarkable efficacy as Voltage Controlled Oscillators (VCOs) in various applications. In this study, we present a novel approach to VCO design, introducing a simplified yet robust circuit architecture centered around current-starved inverters arranged meticulously within a ring oscillator configuration. The distinctive feature of this circuit lies in its utilization of analog control voltages, specifically V_{CNTL} and $V_{DD} - V_{CNTL}$, to finely regulate the delay characteristics inherent in the inverter stages comprising the ring. Furthermore, our investigation extends to a comprehensive exploration of VCO performance, particularly focusing on a meticulously implemented 93-stage current-starved inverter ring oscillator circuit. By meticulously analyzing the resulting frequency output range stemming from the modulation of the VCO control voltage, V_{CNTL}, we aim to provide a thorough understanding of the operational dynamics and performance nuances exhibited by the VCO under varying control conditions. This in-depth examination offers valuable insights into the intricacies of VCO behavior, facilitating a deeper comprehension of its functionality and potential applications in diverse engineering contexts.

Design Specifications:

Target Output Frequency: 35MHz

Technology: 1µ CMOS Process

Number of Stages: 93

Stabilizing Drivers: CMOS-based

Design Steps:

Inverter-Based Architecture Selection: Start by selecting an appropriate architecture based on CMOS inverters to realize the VCO. This choice is pivotal in achieving the desired frequency range and stability characteristics while leveraging the advantages offered by CMOS technology.

Frequency Determination and Stage Count: Determine the necessary number of stages and their configuration to achieve the target frequency of 35MHz. Each stage, comprising CMOS inverters, contributes to the frequency generation process, and the total count of 93 stages is chosen to meet the design requirements.

Component Sizing and Parameter Optimization: Size the CMOS inverters and passive components in each stage to meet the frequency and performance specifications while adhering to the constraints of 1µm CMOS technology. Optimization techniques are employed to balance speed, power consumption, and noise performance.

Biasing Scheme Design: Develop a biasing scheme tailored to the CMOS inverters to ensure stable operation across process and temperature variations. Proper biasing is essential for maintaining the desired operating point and optimizing the VCO's performance.

Voltage Control Implementation: Implement voltage control mechanisms to enable frequency tuning, which is crucial for PLL applications. These mechanisms allow for precise adjustment of the VCO's output frequency to lock onto the reference signal in the PLL system.

Stabilizing Driver Integration: Integrate stabilizing drivers using CMOS technology to enhance the VCO's stability and mitigate noise and process variations. These drivers provide additional buffering and control to ensure reliable performance under varying operating conditions.

Simulation and Validation: Utilize circuit simulation tools to validate the design and assess its compliance with the specified requirements. Perform extensive analysis, including frequency response, transient behavior, and noise performance, to verify the VCO's suitability for its intended application.

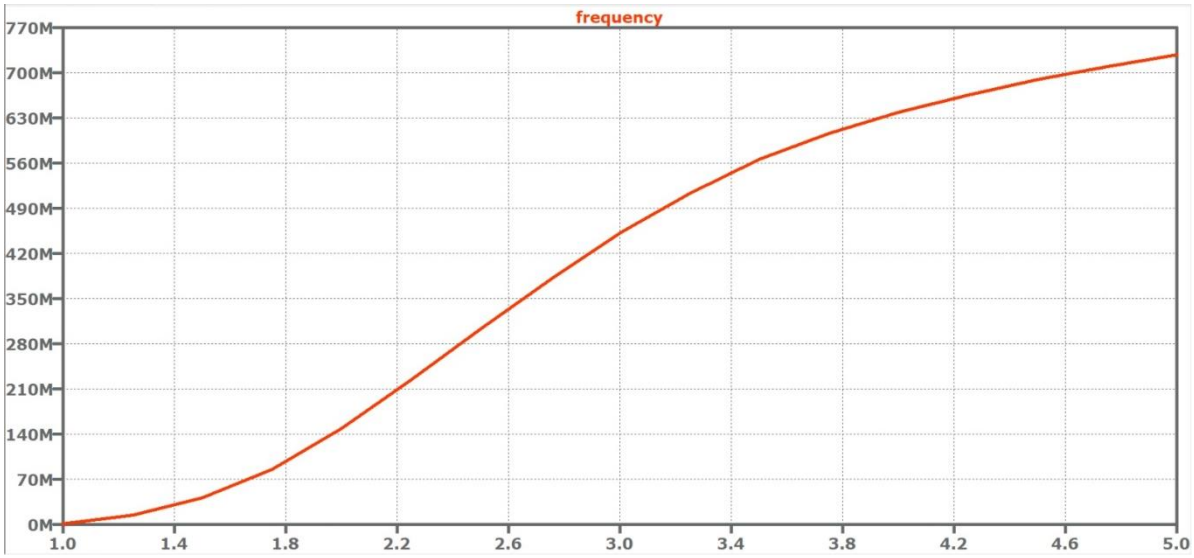
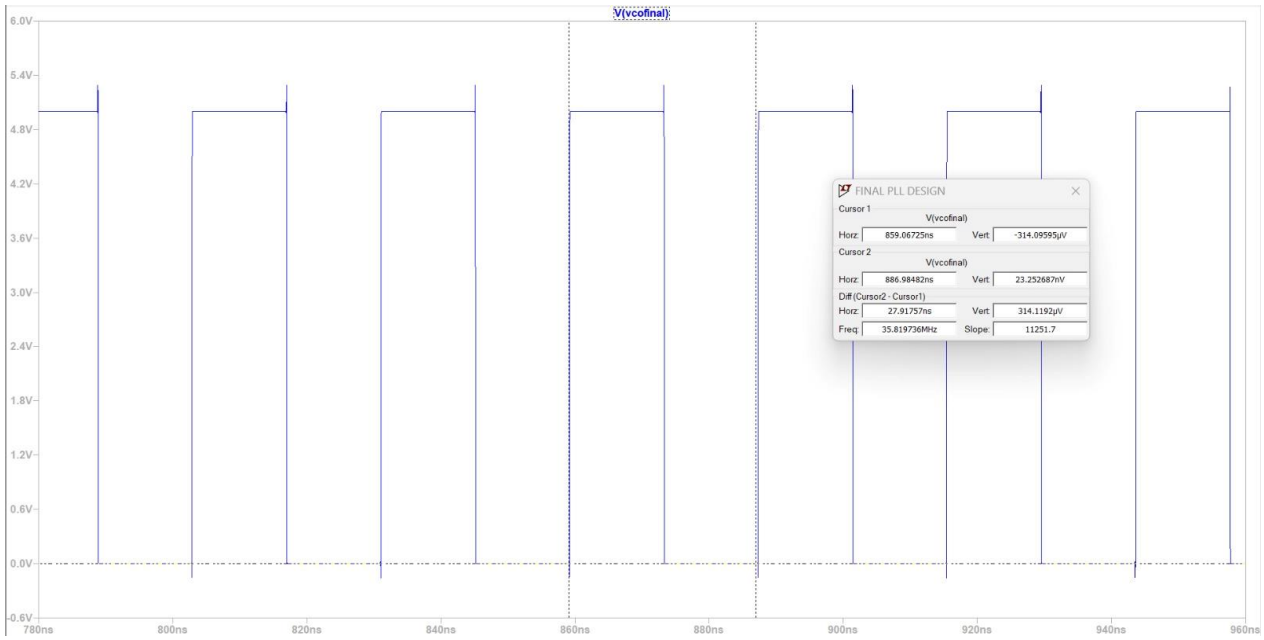


Fig. 1.6. Simulation Result for Frequency vs Voltage Control of 11-Stage VCO Circuit



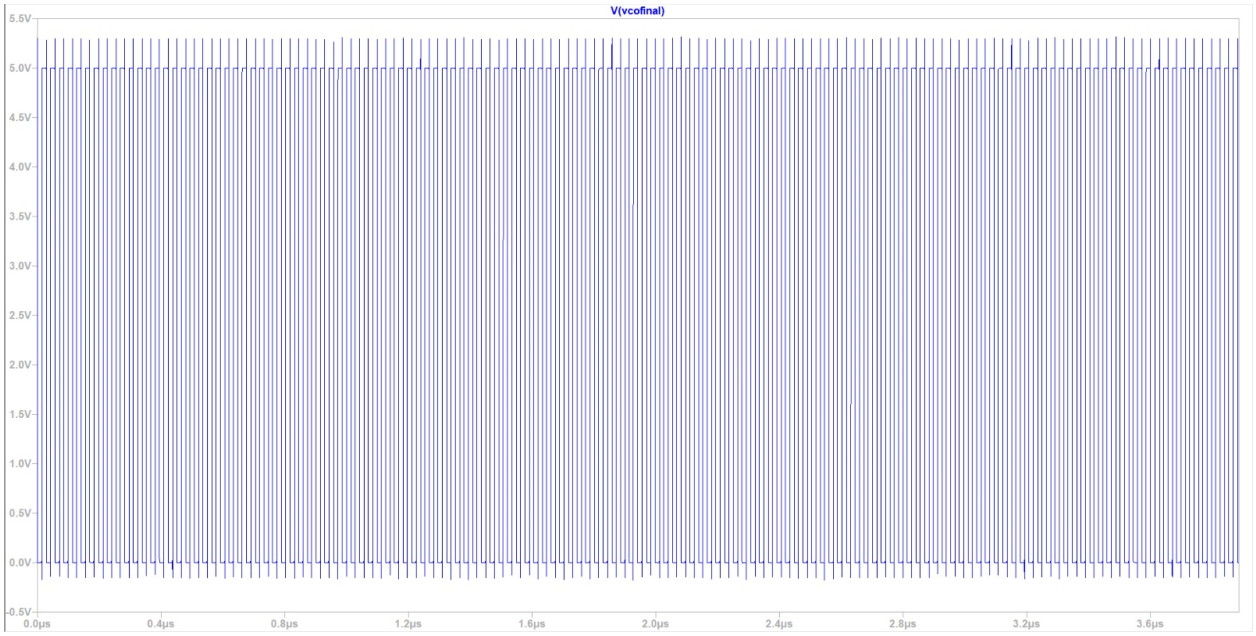


Fig. 1.7. Simulation Result of 93-Stage VCO Circuit

Within this context, the behavior of this VCO circuit exhibits a predominantly linear response in its intermediate range. However, it is anticipated that frequency adjustments reach a saturation point as the input control voltage approaches the supply rails. Remarkably, oscillation halts entirely when the control voltage descends below 0.3V. Fortunately, this occurrence is inconsequential due to the inherent self-starting nature of this oscillator type once the control voltage exceeds 0.3V. Notably, a crucial attribute of the VCO lies in its capacity for monotonic frequency variations across the entire span of the input control voltage. This is vital as a non-monotonic response can potentially destabilize the Phase-Locked Loop (PLL) or lead to frequency misalignment.

4. Divide By 7 Counter:

In Phase-Locked Loop (PLL) circuits, accurate frequency division is crucial for synchronizing different signals. A common requirement is dividing the PLL output frequency by a specific factor to match it with the reference frequency from the Phase Frequency Detector (PFD). One efficient way to achieve this is by designing a Divide-by-n counter using D flip-flops and logic gates.

In this design, the PLL output frequency is 35 MHz, and the input frequency from the Phase Frequency Detector (PFD) is 5 MHz Thus, the goal is to design a Divide-by-7 counter to divide the PLL output frequency by 7, matching it with the reference frequency from the PFD.

Design Overview:

The Divide-by-7 counter will take the PLL output frequency as its input and produce a divided output signal with a frequency seven times lower. The design will employ D flip-flops and combinational logic gates to achieve the desired division.

Design Steps:

1. Firstly, the state variables are defined required for the counter. Since we need to count up to 7, four flip-flops are necessary to store the states corresponding to the numbers 0 to 6 and to divide frequency at end of counter.
2. Implement the logic to transition between states. For each state, determine the next state based on the current state and input conditions. This logic will involve appropriate combinations of gates to achieve the desired counting sequence.
3. Ensure that the counter resets to the initial state after reaching the count of 6 (or 011 in binary). This step is crucial for maintaining the divide-by-7 functionality.
4. Connect the output of the counter to the input of the next stage or utilize it as required in the overall system design.

Figure 6 given below provides a visual representation of the schematic diagram illustrating the divide-by-7 counter architecture. This counter is constructed using D flip-flops interconnected in a precise arrangement, complemented by strategically integrated logic gates responsible for facilitating state transition and reset functionalities. The intricate interconnections between the flip-flops and logic gates are meticulously determined based on logical expressions derived from the systematic design process. These expressions serve as guiding principles in configuring the circuit layout, ensuring optimal functionality and efficiency in achieving the desired divide-by-7 counting operation.

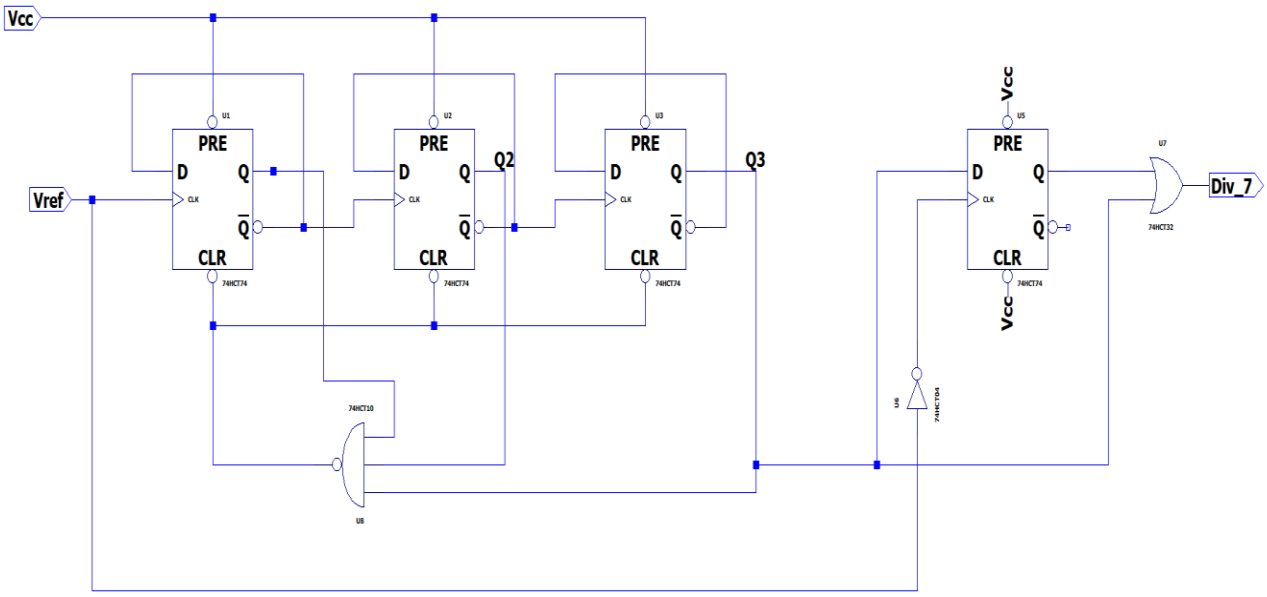


Fig. 1.8. Basic Design of Divide By 7 Counter

Fig. 1.9. Simulation Result of Divide By 7 Counter

Thus, a divide-by-7 counter using D flip-flops and gates is implemented shown above. This counter serves as a crucial component in digital systems where frequency division or timing control is necessary.

1.5 Conclusion:

The culmination of the Phase Lock Loop (PLL) design project utilizing **commercial off-the-shelf (COTS) ICs** from the 74HC series represents a significant achievement in the realm of circuit design and signal processing. Throughout this endeavor, the integration of crucial components such as the phase frequency detector, loop filter, voltage-controlled oscillator (VCO), and frequency divider has been meticulously orchestrated to realize a robust and functional PLL system.

The cornerstone of this project lies in its utilization of LT

spice for simulation purposes. This powerful tool has enabled thorough exploration and analysis of the PLL circuit's behavior and performance across a spectrum of operating conditions. By subjecting the design to rigorous simulation, critical parameters including lock range, phase noise, and jitter have been scrutinized and optimized to align with project specifications and industry standards.

The success of this project underscores the efficacy and adaptability of PLL designs employing readily available COTS ICs. By leveraging existing components from the 74HCT series, the project has demonstrated a cost-effective approach to implementing complex signal processing systems. Moreover, the scalability of this design framework opens avenues for customization and adaptation to suit diverse application requirements.

Beyond its immediate implications, the knowledge gleaned from this project holds broader significance in the realm of electronics and telecommunications. PLLs serve as fundamental building blocks in a myriad of systems, ranging from frequency synthesis in wireless communication to clock recovery in digital circuits. As such, the insights gained from this endeavor not only contribute to the advancement of PLL technology but also lay a foundation for innovation in related fields.

Looking ahead, the outcomes of this project serve as a springboard for further exploration and refinement. Future endeavors could involve the integration of advanced features such as fractional-N synthesis or digital signal processing techniques to enhance the performance and versatility of PLL systems. Additionally, real-world validation through hardware implementation and testing would provide invaluable insights into the practical considerations and challenges associated with deploying PLL designs in operational environments.

In conclusion, the successful completion of the Phase Lock Loop design project represents not only a technical achievement but also a testament to the ingenuity and collaborative effort of the team involved. As we reflect on the journey from conception to realization, it is evident that the insights gained and lessons learned will continue to resonate in our pursuit of innovation and excellence in the field of electronic engineering.

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