DESIGN AND ANALYSIS OF A 1.28GHZ CHARGE PUMP PHASE-LOCKED LOOP IN 180NM TECHNOLOGY NODE

BY

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THESIS

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ABSTRACT

This thesis presents readers, especially undergraduate electrical engineering students in their junior or senior years who have solid background knowledge in Integrated Circuits (IC) design and strong passion in the semiconductor industry, with some flavors of the fundamentals of the mixed-signal IC design of a phase-locked loop (PLL) implemented in 180nm technology node and operated at a center frequency of 1.28GHz. It begins by introducing the applications and motivations of PLLs. The thesis then moves on by diving deep into the discussion of each of the PLL component's intuition, schematic, characteristic, and linear model. Afterwards, a complete analysis of PLL is conducted, including its block diagram, linear model, stability, and characteristics, etc. The thesis finishes with the conclusion and discussion of future work to improve the PLL design.

To my family and friends, for their love and support

ACKNOWLEDGEMENTS

Trite though the saying goes: Time flies. As I recall the wonderful experiences since my matriculation as an undergraduate student six years ago, the memories of the exciting first day I arrived on campus as a freshman, the joyful days I hung out with friends, the gratifying moments I learned that I was admitted to the ECE Illinois graduate program, and the ecstatic news that a major US semiconductor company offered me a full-time position just several weeks ago remain crystal clear to me. In retrospect, my journey as an electrical engineering student at UIUC is by no means without challenges as I reflect upon the countless all-nighters I pulled up before exams, homework, and project deadlines, the cornucopia of internship and full-time position rejection emails, and most importantly, the over four years of not being able to go back to my hometown, Shanghai, to visit my family and friends due to Covid and visa reasons. Throughout my journey, I felt the essential need to look back and express my sincere gratitude for my family, advisor, friends, and myself.

My answer to whom I thank the most is always my family, since it is my family that has provided me with the most support, not only financially, but also offered me advice and guidance in life. It is also through the many conversations and overseas calls I had with my parents and grandmother that helped me not to be too homesick amid the difficult Covid times.

I'd like to also thank my graduate thesis advisor Professor Jose E Schutt-Aine for welcoming me to his excellent research group, providing me with precious advice with my thesis both during weekly group meetings and personally in his office, and being my instructor for two very useful and interesting classes: *Wireless Communication Systems* and *Advanced Signal Integrity*. Professor Jose's unwavering commitment to both research and academia motivates me further to actively engage in class and research.

My appreciation also goes to my friends, and two of the best friends during my two years of graduate studies are Ram Krishna and Michael Molter. Ram and Michael are two very talented and hard-working PhD students in Professor Elyse Rosenbaum's research group, and I'm fortunate to work with them on several course projects. I learned so much while working with them, as they are my role models for an electrical engineering graduate student interested in semiconductors and Integrated Circuits (IC) design. Academics aside, we are good friends and brothers, and I always enjoyed our casual conversations and extracurricular

activities like eating out together, going to supermarkets, visiting movie theaters, etc.

I know it might be a bit unusual and awkward, but I think I am the final person to acknowledge. Spending six years out of my hometown Shanghai, China, with more than four years unable to go back, adapting to a completely new and diverse culture, immersing myself into the challenging discipline of electrical engineering with an emphasis in IC design at a prestigious university, and landing a job in the US, I would like to devote my MS thesis to myself as a source of accomplishment of the past and an encouragement to strive in the future. As the classical Chinese saying goes: “The way ahead is long and has no ending, yet high and low I will search with my will unbending.”

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION AND MOTIVATION OF PLL

1.1 What is PLL?

A phase-locked loop, in the most straightforward sense and as its name indicates, is a circuit whose topology utilizes feedback and therefore forms a loop. We can also infer from its name that a PLL has some kind of mechanism that, utilizing feedback, locks the phase of a signal over time. In literature, PLL has many other names: multiplying delay-locked loop (MDLL), multiplying injection-locked oscillator (MILO), etc. that all refer to the PLL architecture.

1.2 PLL Applications

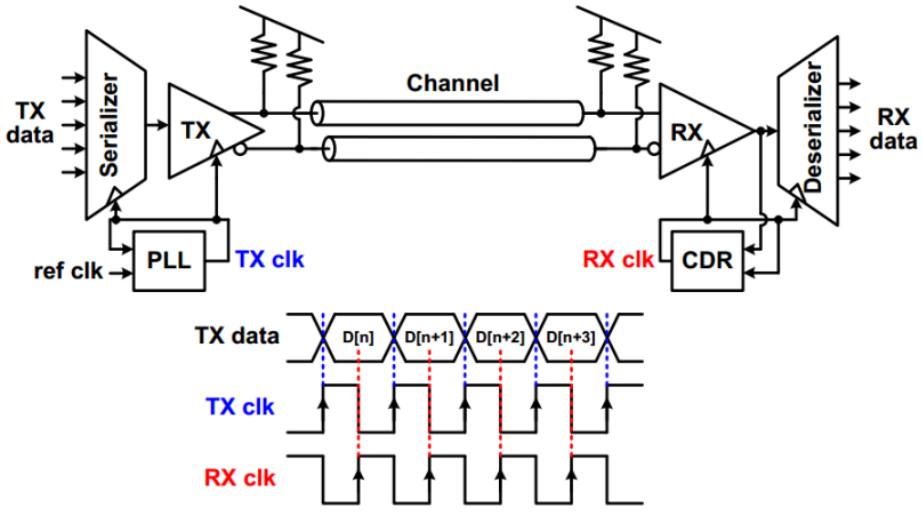

Figure 1.1 High-Speed Link System

Figure 1.1 displays the simplified model of a modern high-speed link system [1]. Parallel data stream goes through a serializer which, in turn, converts it into serial data stream. Serial data stream is then propagated through a line driver (ex. a transmitter (TX)), whose main responsibilities include impedance matching, equalization, and signal amplification to compensate for any data loss through the channel. At the receiver (RX) side, serial data stream is sampled and then converted back to parallel data stream through the deserializer. As is also shown in the graph, the transmitter is driven by a high-speed clock (TX clk) that is generated through the phase-locked loop circuitry with an input of a reference clock (ref clk). The receiver, on the other hand, is driven by a receiver clock (RX clk) generated by the clock and data recovery (CDR) circuit whose architecture bears much resemblance to that of a PLL. Figure 1.1 also shows that the transmitted data (TX data) is transmitted at each rising edge of the TX clk and is received by the receiver at each falling edge of the RX clk after some propagation delay through the channel.

In fact, PLL's application extends way beyond that of high-speed link systems. Radios, TVs, mobile phones, and other wireless and RF devices all depend on PLL. Three of the most important functionalities of a PLL are clock generation, frequency synthesis, and data recovery. We are going to pay close attention to its first function of generating a steady, low-noise, and high-speed clock, since generating a clock of varying frequencies is rather simple, and the CDR circuit is not the focus of this thesis.

1.3 PLL Motivation

From Figure 1.1, one might wonder why it is even necessary to make a hassle and dedicate an entire MS thesis into devising a PLL that takes in a reference clock in the high-speed link system for clock generation. Why not just implement the clock using a crystal oscillator and change the oscillation clock frequency by altering the varactor? Indeed, crystal oscillators are known for their generation of stable and low-noise clocks, yet the highest clock frequency a typical crystal oscillator can generate is in the order of hundreds of megahertz [2], well below the gigahertz range as is required in modern high-speed links. In fact, a crystal oscillator is often used as the reference clock for the PLL circuitry.

When it comes to the topic of generating a high frequency clock for high-speed links, thoughtful readers may also ponder the possibility of simply using an LC or ring oscillator. Figure 1.2 shows a simple 3-stage ring oscillator consisting of three series inverters that form a loop. Granted, such a ring oscillator can generate clock signals with frequencies as high as 6.345GHz as is shown in Figure 1.3, but a closer look at the simulated graph draws one's

attention to the presence of significant noise in the generated clock of a ring oscillator. Although one might argue that several megahertz of noise is merely around 1% of the generated clock frequency, it is totally unacceptable in an industrial setting to have a high-speed link clock with that much noise. In addition, the simple ring oscillator circuitry is very susceptible to PVT changes, meaning that any slight variation in process corner, voltage, or temperature of the transistors will result in significant noise and jitter of the generated clock. Finally, the simple ring oscillator in Figure 1.2 has only one fixed frequency, whereas we would like to have our clock generator's frequency to be easily tuned. Thus, more complicated topology needs to be analyzed for a high-speed and robust clock generator, which will be discussed and analyzed in Chapter 2.

Finally, it is the author's hope that students interested in IC design can gain more insights not only into the transistor-level implementation of a charge pump PLL, but, more importantly, into the intuitions and characteristics of the PLL topology which is a major topic of the thesis.

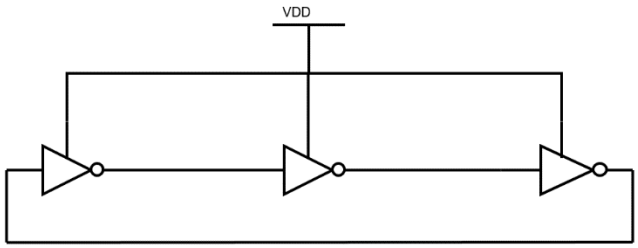

Figure 1.2 A Simple 3-Stage Ring Oscillator

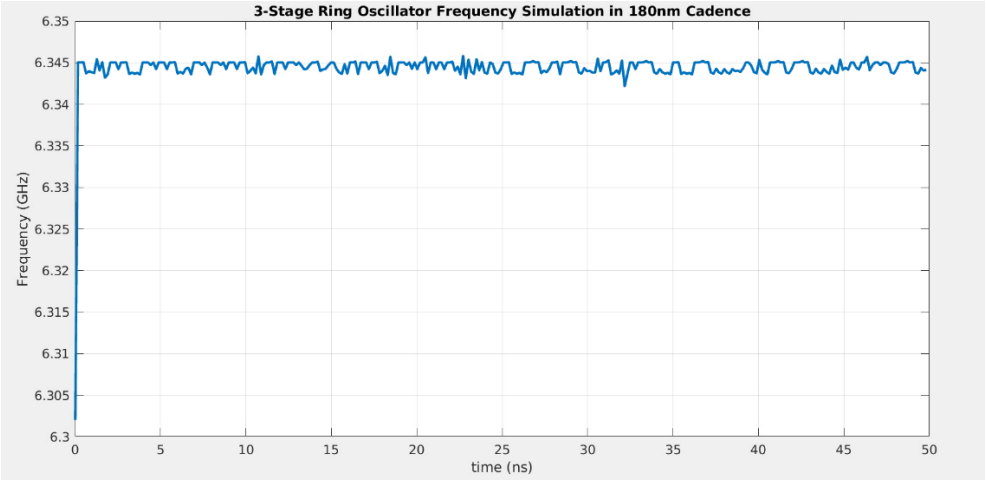

Figure 1.3 Simulated 3-Stage Ring Oscillator Using 180nm TN in Cadence

CHAPTER 2

A PROGRESSIVE DISCUSSION AND DETAILED ANALYSIS OF PLL COMPONENTS INTUITION, TOPOLOGY, CHARACTERISTICS, AND LINEAR MODEL

2.1 Voltage-Controlled Oscillator (VCO)

2.1.1 Ring Oscillator Frequency Knobs

We learned the basic properties of a ring oscillator (shown in Figure 1.2) from our digital IC design course that its oscillation frequency satisfies the following:

$$f = \frac{1}{2 \cdot t_p \cdot N} \tag{2.1}$$

Here, t_p is the propagation delay of one inverter, and N is the number of stages (ex. how many inverters) in the ring oscillator. We also know that the propagation delay of a CMOS inverter is related to:

$$t_p \propto \frac{C_L}{(\frac{W}{L})} \tag{2.2}$$

where C_L is the load capacitance, W and L are the width and length of the MOSFET. Thus, taking both formulas 2.1 and 2.2 into account, to achieve a higher oscillation frequency (ex. higher f), we should have fewer inverter stages by setting N=3, ensure smaller load capacitance, and use large effective channel width and small effective channel length. Higher supply voltage also leads to higher oscillation frequency, as the charging and discharging process of the parasitic capacitances speeds up for large V_{DD}, resulting in smaller delay t_p. While we can take all these knobs into account when designing the ring oscillator, one of the main problems discussed in Chapter 1.3 is that it is still hard to tune the ring oscillator frequency, as the above strategies are all static tuning. If we can have a dynamic tuning knob

while keeping the static tuning strategies in mind, our ring oscillator will have a lot more flexibility in its generation of a high-speed clock.

2.1.2 Transistor-Level Implementation of VCO

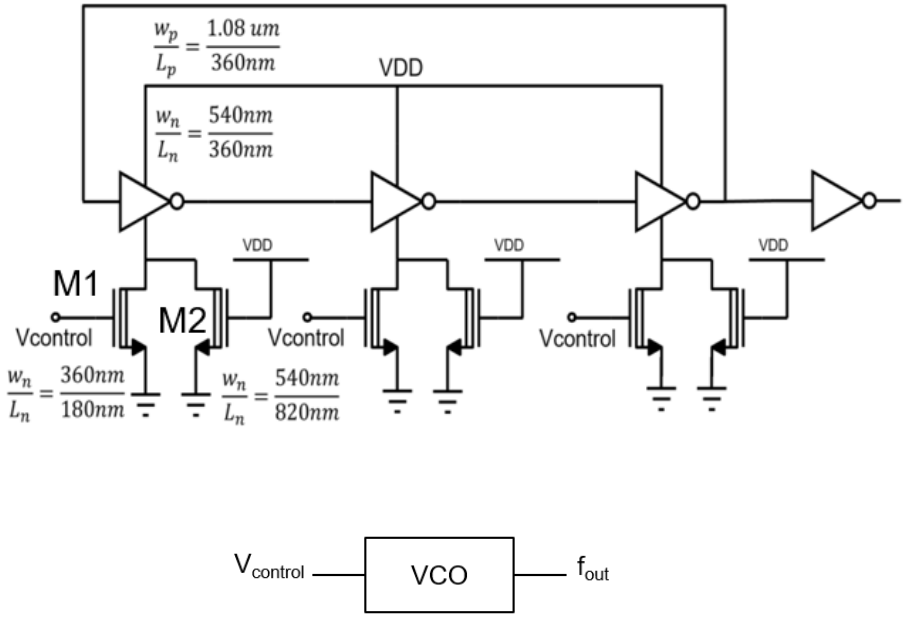

Figure 2.1 VCO Schematic and Symbol

Figure 2.1 shows the transistor-level schematic of a voltage-controlled ring oscillator. It is very similar to the ring oscillator in Figure 1.2 except that the oscillation frequency can be tuned directly by the control voltage $V_{control}$. Let us analyze this topology closely.

Of the three inverters that form the ring oscillator (the fourth inverter is applied so as not to reverse the logic), each inverter's NMOS has two additional transistors (ex. M1 and M2 for the first inverter) connecting to its source. By changing the control voltage that serves as the gate voltage for M1, we are effectively varying the driving strength of the first inverter by tuning the resistance in its pull-down network, thereby changing its propagation delay and the VCO oscillation frequency. M2, a pseudo-NMOS transistor, is needed, since when $V_{control}$ is smaller than the threshold voltage of M1 (ex. $V_{control} < V_{th1}$), M1 is cut-off and oscillation will stop due to an open-circuit in M1. The parallel pair of M1 and M2 thus act as a variable resistance that is always turned on. Since we know a MOSFET's effective resistance R_{eff} is inversely proportional to the absolute value of the gate-source voltage (ex. $R_{eff} \propto 1/|V_{GS}|$),

as the control voltage increases from V_{thn} to V_{DD} for M1, its effective resistance decreases. The drop in M1 resistance reduces the overall resistance in the inverter's pull-down network, thus decreasing the propagation delay and increasing the oscillation frequency as we know delay t_p is directly proportional to R_{eff} (ex. $t_p \propto R_{eff}$).

As for the sizing of the transistors, the PMOS widths are twice as that of the NMOS widths inside each inverter since we assume electrons have twice the mobility of holes, and we'd like to ensure equal rise and fall times of the inverters. Since the thesis targets to have a PLL output frequency of 1.28GHz, parametric sweeps are conducted to optimize the VCO transistor sizes such that we can have a wide frequency tuning range and that the 1.28GHz target frequency is at the center of the VCO frequency range, as is shown in Figure 2.2.

2.1.3 Simulated VCO Characteristics

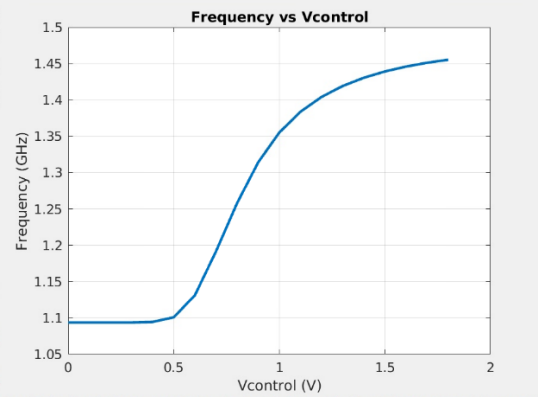

Figure 2.2 VCO Frequency vs $V_{control}$ Curve

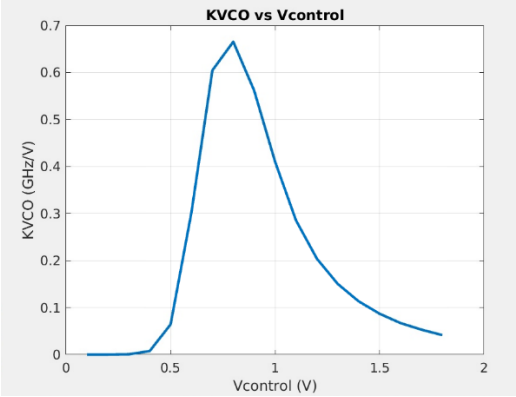

Figure 2.3 VCO K_{VCO} vs $V_{control}$ Curve

Two important metrics of a VCO are its available frequency range and its gain, as the VCO frequency range determines the PLL output frequency, and the VCO gain, denoted as K_{VCO} whose unit is expressed in Hz/V, is related to the PLL loop gain, as will be discussed in Chapter 3.

Figure 2.2 shows the relationship between VCO frequency and control voltage regarding the topology in Figure 2.1 in 180nm Cadence Virtuoso. As is shown in the graph, the VCO frequency ranges from 1.09GHz to 1.46GHz, where our goal frequency of 1.28GHz is centered where $V_{control}$ is 0.9V.

To plot the frequency vs $V_{control}$ graph in Cadence Spectre, we can do a parametric sweep of the control voltage from 0 to 1.8V with a linear step of 0.1V. Using the calculator under the Tools menu, we can plot this characteristic by taking the average of the swept

frequency curve with a threshold of 0.9V as shown in Figure 2.4.

```
average(freq(VT("/output") "rising" ?xName "time" ?mode "auto" ?threshold 0.9) )
```

Figure 2.4 VCO frequency vs $V_{control}$ Plot Setup in Spectre

Figure 2.3 shows the K_{VCO} vs $V_{control}$ curve. We can see that at 1.28GHz frequency, the VCO has a frequency/voltage gain of 551MHz/V.

To plot the K_{VCO} vs $V_{control}$ graph in Spectre, we just need to take the derivative of the previous function in the calculator as is shown in Figure 2.5, since the VCO gain is the slope of the frequency vs $V_{control}$ curve.

```
deriv(average(freq(VT("/output") "rising" ?xName "time" ?mode "auto" ?threshold 0.9) ))
```

Figure 2.5 VCO K_{VCO} vs $V_{control}$ Plot Setup in Spectre

2.1.4 VCO Linear Model

The linear model of each PLL component is useful because it gives us insights into the Laplace Transform of the loop gain of the PLL, which is critical when drawing the loop gain Bode plot and determining the stability of our PLL topology. Thus, at the end of discussion of each component, we will analyze each linear model.

A VCO is essentially an integrator circuit in that it takes in control voltage and outputs frequency as is shown in Figure 2.1. Thus, the linear model of VCO is K_{VCO}/s, where $s = j\omega$ and s is the frequency-dependent complex variable in the Laplace Transform.

2.2 Phase Frequency Detector (PFD)

2.2.1 Frequency vs Phase

Before we even delve into the discussion of a phase frequency detector, it is paramount to first get a grasp of the relationship between two seemingly similar concepts: frequency and phase.

$$\omega(t) = \frac{d\emptyset(t)}{dt} \tag{2.3}$$

$$\emptyset(t) = \int_0^t \omega(\tau)\, d\tau \tag{2.4}$$

As we can see from Equation 2.3 and 2.4, frequency is the instantaneous time derivative of phase, while phase can be calculated from the time integral of frequency. Frequency tells us how often a signal repeats itself, while phase tracks the position of the signal with respect to time. It can easily be observed that in Figure 2.6, while all three signals A, B, and C have the same frequency, signal C has a different phase than signals A and B. Thus, we can also arrive at the conclusion that two signals having the same phase is a sufficient and necessary condition for the two signals to have the same frequency, whereas two signals having the same frequency may not necessarily have the same phase.

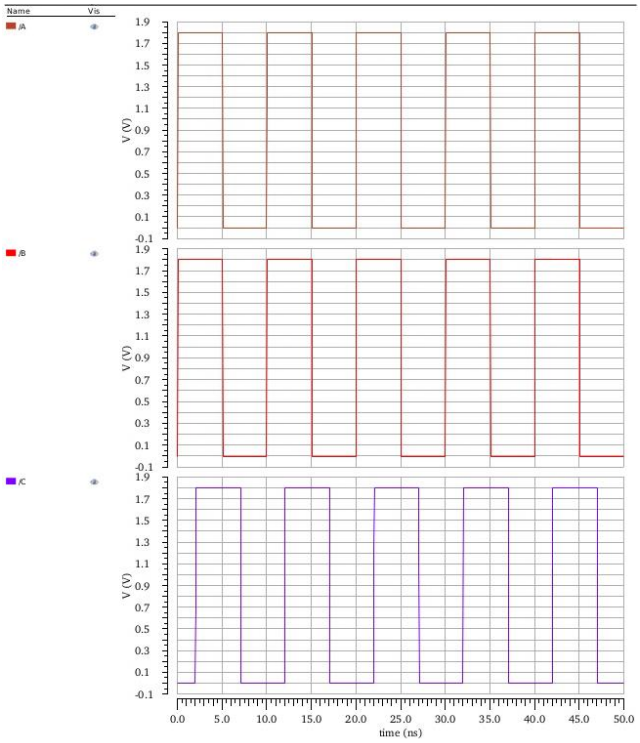

Figure 2.6 Frequency vs Phase Example

2.2.2 PFD Intuition

Recall that in Chapter 2.2.1, we distinguished the differences between frequency and phase, and in Chapter 2.1, we discussed the necessity of a control voltage within the VCO. But where does $V_{control}$ come from?

The most common way to generate the control voltage is through a phase frequency detector (PFD). A phase frequency detector is essentially a mixer that compares both the

phase and frequency difference between the reference clock from a crystal oscillator and the feedback clock from the VCO and sends out an error signal whose phase error ($\emptyset_e$) is proportional to the magnitude of the control voltage. It is through the negative feedback configuration between the reference and feedback clock as is shown in Figure 2.7 that helps generate $V_{control}$, which, in turn, helps to adjust any phase or frequency difference between the two signals and achieve locking condition within the PLL. When the PLL is in lock, meaning that there is zero phase error in theory and very small phase error in practice, the control voltage will stay constant, and thus the frequency generated by the VCO will remain the same as that of the reference clock.

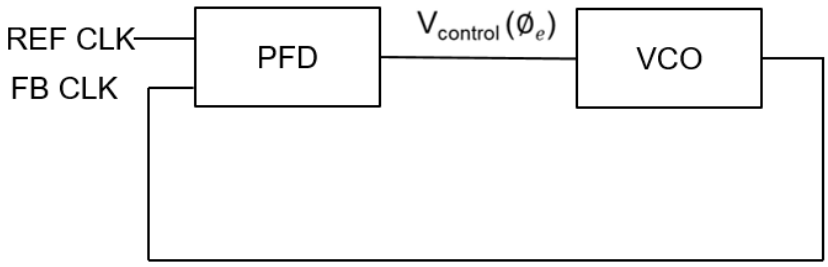

Figure 2.7 Phase Frequency Detector (PFD) + VCO Configuration

2.2.3 PFD Phase Detection

The outputs of the PFD are two signals, conventionally denoted as “UP” and “DN”. When there is no phase error between the reference clock and the feedback clock, both UP and DN signals are low. When the reference clock leads the feedback clock, the UP signal will be high for a duration equal to the phase difference between the nearest positive edges of the two clocks, and the DN signal will remain low as is shown in Figure 2.8. In contrast, when the feedback clock leads the reference clock, the DN signal will be high, and the UP signal will be low, as is illustrated in Figure 2.9. It is, therefore, the UP and DN pulses that interact with the control voltage that is also the input to the VCO.

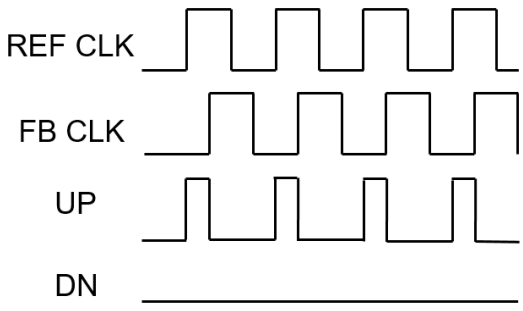

Figure 2.8 PFD REF CLK Leads FB CLK

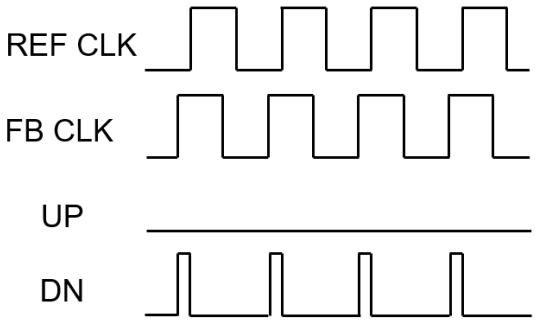

Figure 2.9 PFD FB CLK Leads REF CLK

2.2.4 PFD Frequency Detection

A PLL would work fine by using a phase detector for a fixed reference clock frequency, but when the reference clock undergoes some drastic frequency changes, the PLL will often fail to lock. A phase frequency detector, on the other hand, not only tracks any phase difference between the two clocks, but it also gives commands to any frequency adjustment to the VCO in case the reference clock frequency changes significantly.

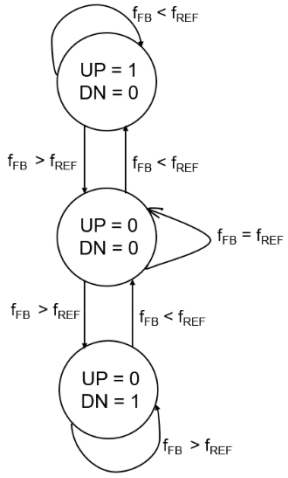

Figure 2.10 PFD FSM

Not only is the PFD a mixer that performs the task of phase comparison, but it is also a three-state finite state machine (FSM). Figure 2.10 displays the FSM block diagram. When the reference clock and the feedback clock have the same frequency, the PFD is in the state where both UP and DN signals are 0. When the reference clock's frequency suddenly increases, the PFD will go to the state where UP=1 and DN=0. This sudden change in state

results in a gradual increase in the control voltage, and we know from our simulated Figure 2.2 that an increase in $V_{control}$ will lead to an increase in the feedback clock frequency $f_{FB.}$ Similarly, in the presence of a sudden decrease in the reference clock frequency, the PFD will enter the state where UP=0 and DN=1, leading to a gradual decrease in $V_{control}$ that, in turn, lowers f_{FB} over time. Finally, we will learn from our PFD topology in the next subchapter that when both UP and down signals are logic high, it automatically sets the reset signal of the NOR latches to be high so that the PFD immediately settles in the UP=DN=0 state.

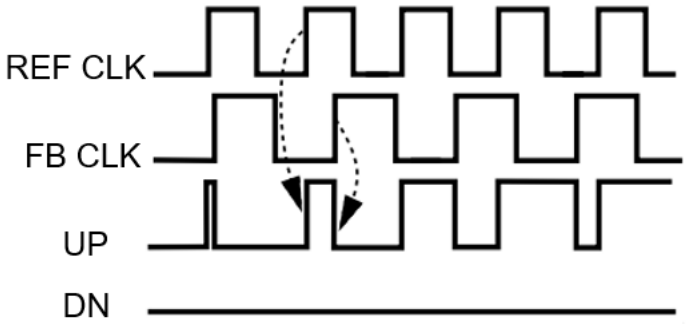

Figure 2.11 PFD $f_{REF\ CLK} > f_{FB\ CLK}$ Waveform

Figure 2.11 showcases the waveform where the PFD tracks the reference and feedback clock with different frequencies [3]. When the reference clock has a higher frequency than that of the feedback clock, only the UP signal will be high and the DN signal will always remain low. The only difference in this case is that the output pulse width of the UP signal is constantly changing, and it will not remain constant until the feedback clock is adjusted to have the same frequency as that of the reference clock.

2.2.5 Logic Gate-Level Implementation of PFD

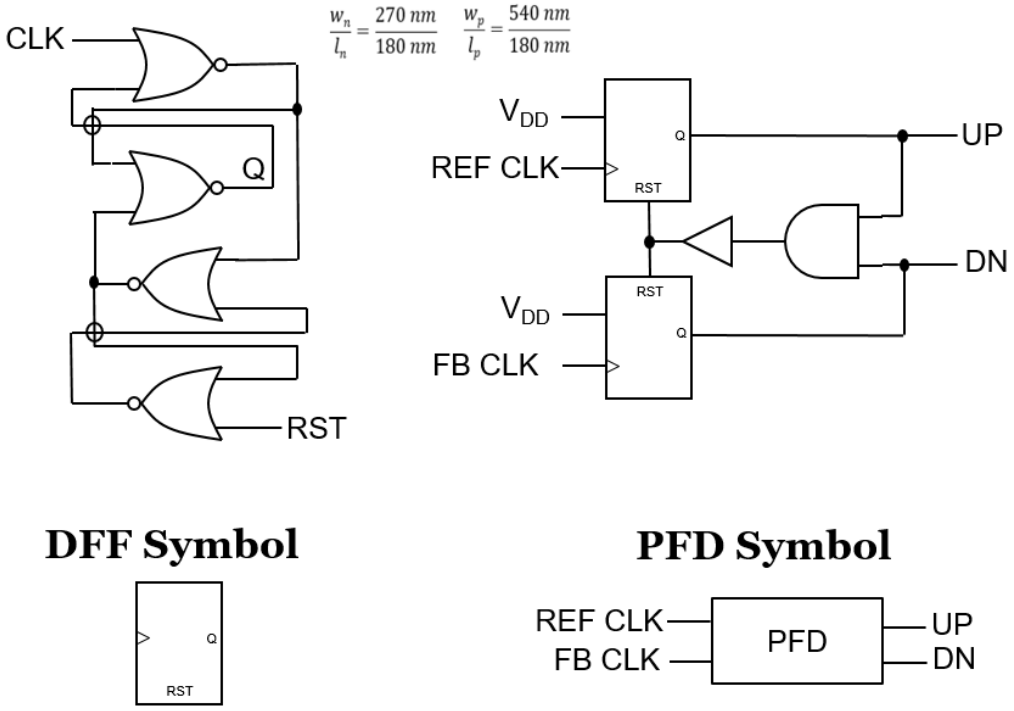

Figure 2.12 NOR-Based Resettable DFF and PFD Schematics and Symbols

Figure 2.12 demonstrates the gate-level design of a classical PFD, where it is a purely digital circuit primarily consisting of two NOR-based resettable D Flip-Flops (DFF) and an AND gate. For the DFF, its output Q remains low when the reset signal RST is high and is independent of the clock CLK, and Q will be held always high once CLK is high, and RST is low. For the PFD, when the reference clock leads the feedback clock, the UP signal will be held high first, and when the bottom DFF outputs a high signal after some time making DN high, the joint high inputs will immediately result in a high output from the AND gate and thus reset both DFFs, making both UP and DN signals low concurrently. The other condition where the feedback clock leads the reference clock works in similar fashion. These explain the waveforms in Figures 2.8, 2.9, and 2.11.

Notice in Figure 2.12 that a buffer is inserted between the output of the AND gate and the input of the RST port of the DFF. This is to avoid dead zones in PFD. A dead zone in PFD refers to the scenario where the phase difference between the reference and feedback clock is very small that will lead to a very narrow UP or DN pulse, which, in turn, will fail to send

any meaningful information to the VCO. Consequently, delay-increasing techniques like adding a buffer consisting of an even number of inverters are necessary to widen the UP and DN pulses to minimize dead zones.

2.2.6 Simulated PFD Characteristics

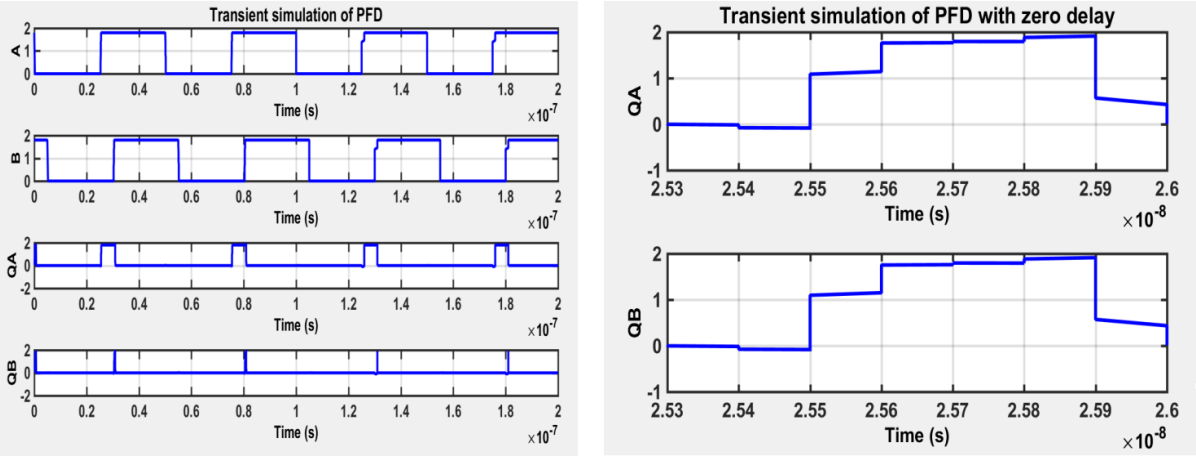

Figure 2.13 Simulated PFD Waveform

Figure 2.13 shows the simulated PFD waveform, with the left graph being the case of the reference clock leading the feedback clock. We can see that the simulated result matches the expected UP and DN waveforms (denoted as QA and QB in the graph). When there is no phase difference between the two clocks, as is seen in the right graph, both clocks will be concurrently high for an extremely short period of time.

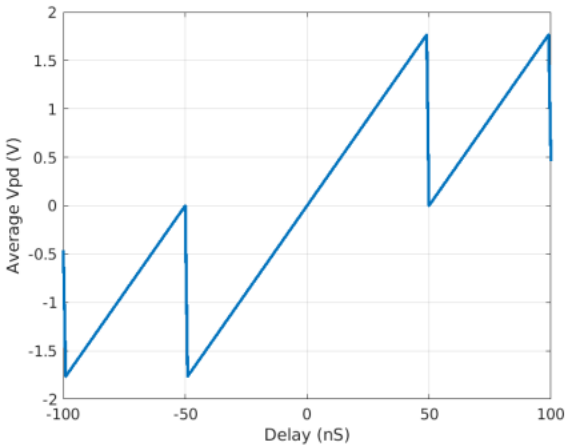

Figure 2.14 Simulated $\overline{V_{PD}}$ vs Delay Curve

Another important PFD characteristic is its $\overline{V_{PD}}$ vs delay curve. Here, $\overline{V_{PD}}$ is the difference between the average voltage of the UP and DN pulse (ex. $\overline{V_{PD}} = \overline{UP} - \overline{DN}$), and delay is the phase error in the time domain between the reference and the feedback clock (ex. delay is positive when REF CLK leads FB CLK, and it is negative otherwise). Figure 2.14 is the simulated PFD characteristic, where we can see a direct correlation between the phase error and the $\overline{V_{PD}}$ magnitude. It is also worth noting from the $\overline{V_{PD}}$ vs delay curve that when either one of the clocks leads the other by exactly an integer number of time periods, $\overline{V_{PD}}$ becomes 0, as there is essentially no phase difference under these circumstances. Finally, we observe no dead zone in figure 2.14, thanks to the buffer in the PFD circuitry.

2.2.7 PFD Linear Model

The linear model of a PFD can be simply regarded as the unitless voltage gain between its input and output voltages and is denoted as K_{PD}. Although we would generally like to increase the PLL loop gain, it is usually very challenging to design a PFD with a very large K_{PD}.

2.3 Charge Pump (CP)

2.3.1 CP Intuition

We equivocally mentioned in Chapter 2.2.4 that when either of the UP or DN signal of

the PFD is high, frequency steering of the PLL is achieved through the gradual increase or decrease of the control voltage magnitude. Exactly how the UP and DN pulses interact with $V_{control}$ is still unknown, and Chapter 2.3 is dedicated to the discussion of such a solution.

The most common way PLLs nowadays tackle the issue is by utilizing a charge pump (CP), and, thus, a phase-locked loop that incorporates the charge pump circuitry is also called a "charge pump PLL" or "CP-PLL".

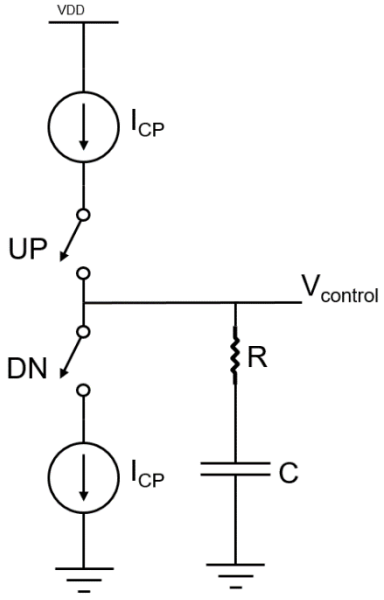

Figure 2.15 CP Schematic Diagram

Figure 2.15 shows a basic charge pump schematic. The charge pump consists of a current source that connects to V_{DD}, a current sink that connects to ground, and two switches constantly being turned on and off by the UP and DN pulses from the PFD. The output of the charge pump is linked to a resistor R and capacitor C connected in series. When UP=1 and DN=0, the top switch is closed and the bottom switch is left open, resulting in the gradual charging of the capacitor C. The charging of the capacitor increases the current going through resistor R, and it is through the resistor that converts increasing current into increasing control voltage, that, in turn, increases the VCO or the feedback clock frequency. Likewise, when UP=0 and DN=1, the top switch acts as an open circuit while the bottom switch acts as a wire, leaving the capacitor to gradually discharge. It is also with the help of the resistor that, as the current through it decreases during the capacitor discharging process, gradually decreases control voltage magnitude which, in turn, decreases the feedback clock frequency. It turns out that the resistor and capacitor are two key components of the loop filter which will be discussed in the next chapter, and by the end of the thesis, we will learn that the

seemingly simple R and C serve a lot more purposes and play multiple indispensable roles in the entire PLL circuit.

2.3.2 Transistor-Level Implementation of CP

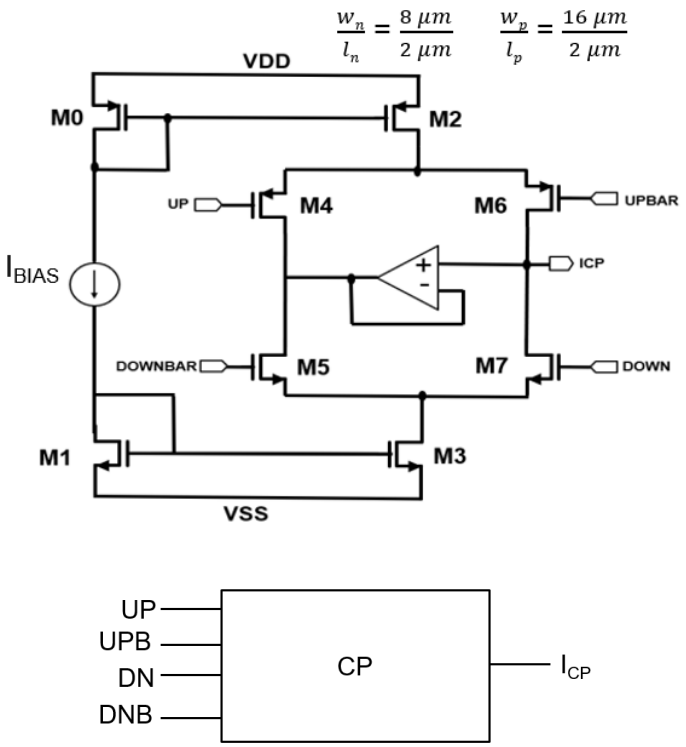

Figure 2.16 CP Schematic and Symbol

Figure 2.16 illustrates the transistor-level design of the charge pump. The two switches in Figure 2.15 are represented by the M4 and M7 MOSFETs, and the current source and the current sink are implemented using a current mirror in both the pull-up and pull-down network of the charge pump. We learned from analog IC design course that the common-mode output voltage of such active load topology with current mirrors is extremely sensitive to any current mismatches due to channel length modulation (CLM). Thus, to ensure the charge pump output currents I_{CP} generated by both the pull-up and pull-down network are as close in magnitude as possible, longer channel lengths of MOSFETs are applied to mitigate the CLM effect (ex. the channel length implemented here is 2μm under 180nm TN). In addition, we also know that to minimize CLM, V_{DS} across the current-mirrored transistors should be set the same. This is achieved by using an operational transconductance amplifier

(OTA) connected in a voltage follower (also known as a unity-gain buffer) fashion. For this thesis, the classical 5T OTA is used for the differential-input, single-ended output amplifier, though readers are encouraged to use OTAs that enjoy a larger voltage gain such as a telescopic cascode or a folded cascode OTA topology with proper biasing to further suppress CLM. Finally, we arrive at the desired MOSFETs' channel widths that minimize I_{CP} through parametric analysis to lower power consumption.

2.3.3 PFD and CP Interface

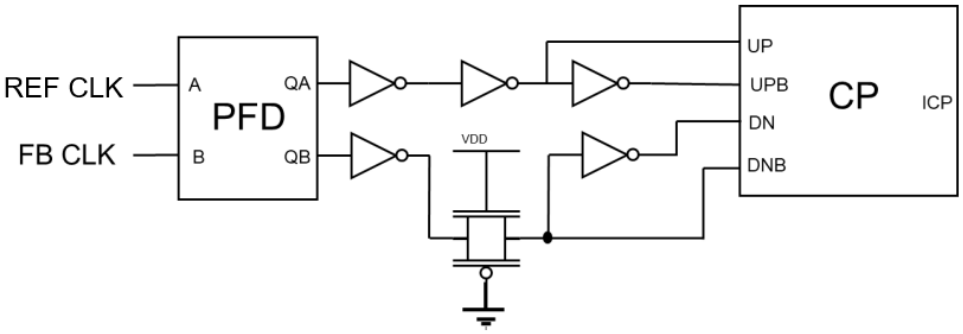

Figure 2.17 PFD+CP Interface

Notice that our charge pump circuit in Figure 2.16 utilizes UP and DN as well as their complementary signal inputs. The complementary signals, UP_{BAR} and DN_{BAR}, are achieved by passing UP and DN pulses through inverters. However, this runs into the problem of unequal inputs arriving times for the charge pump as inverters introduce extra gate delays. To resolve the issue, we resort to the interface between the PFD and the CP as is shown in Figure 2.17 by strategically adding buffers and a transmission gate so that all four inputs to the CP have equal propagation delay.

2.3.4 Simulated CP Characteristic

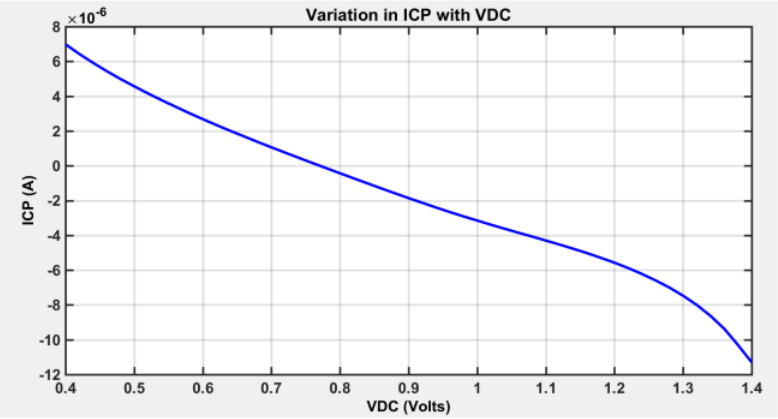

Figure 2.18 Simulated CP I_{CP} vs $V_{control}$ Curve

As we have learned in Chapter 2.3.2, the charge pump output current I_{CP} is easily affected by transistor mismatches. This phenomenon is often manifested in the I_{CP} vs $V_{control}$ curve, where I_{CP} magnitude varies asymmetrically as $V_{control}$ changes. Note that the charge pump output current is positive when the capacitor C in the loop filter is charging and is negative when C is discharging. Figure 2.18 displays the simulated CP I_{CP} vs $V_{control}$ curve, where we can see that I_{CP} reaches 0 when $V_{control}$ is about 0.8V. When $V_{control}$ is 0.4V, I_{CP} is about $7\mu A$, and when $V_{control}$ is 1.2V, I_{CP} is about $-6\mu A$. The key takeaway is that although I_{CP} has slightly different magnitude of current in the two cases, the difference is not large and thus slight asymmetry in our I_{CP} vs $V_{control}$ caused by mismatches in our CP topology is acceptable.

2.3.5 CP Linear Model

When it comes to the topic of the linear model of the charge pump, we usually incorporate it together with the phase frequency detector, since the CP serves as the interface between the PFD and the VCO. Since a 2π radians of phase error between the reference and the feedback clock in the phase frequency detector will generate a charge pump output current of I_{CP}, a $\emptyset_e$ radians of phase error will lead to a $(I_{CP} \cdot \emptyset_e)/2\pi$ charge pump output current. Consequently, we denote the incremental gain of the entirety of PFD+CP as $I_{CP}/2\pi$. Finally, it is essential to note that the charge pump, together with the capacitor in the loop filter, works as an integrator, since it is constantly converting current into the control voltage.

2.4 Loop Filter (LF)

2.4.1 LF Intuition and Schematic

We already learned in Chapter 2.3.2 that the loop filter consists of a resistor R in series with a capacitor C interfacing the output of the charge pump and the input of the VCO. We know that the capacitor is responsible for current steering through the charging and discharging process operated by the UP and DN pulses, and the resistor performs I_{CP} to $V_{control}$ conversion for VCO frequency adjustment.

Satisfying as our current design is, there is another issue to consider. The control voltage pulses generated through the charge pump and the loop filter contain some high frequency components, and those will be deemed as noise that perturb the normal performance of the VCO. Consequently, we need some extra filtering techniques within the loop filter to filter out those high frequency pulses.

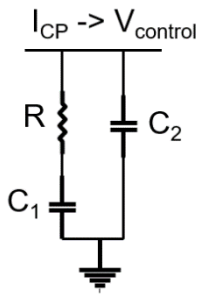

Figure 2.19 Updated LF Schematic

A simple solution is to add another shunt capacitor C_2 in the loop filter as shown in Figure 2.19. Usually, the value of C_2 is much smaller than that of C_1 so that $V_{control}$ pulses with higher frequencies can be effectively filtered out.

2.4.2 LF Linear Model

The linear model of the PLL's loop filter is just its transfer function F(s), where F(s) satisfies:

$$F(s) = \frac{1+RC_1s}{C_1s} \cdot \frac{1}{1+\frac{s}{\omega_p}} \tag{2.5}$$

$$\omega_p = \frac{C_1 + C_2}{RC_1C_2} \tag{2.6}$$

Here, the key takeaways from Equation 2.5 and 2.6 are that the loop filter contributes one zero and two poles to the PLL loop gain transfer function, with the zero contributed by the resistor R, one pole contributed by C_1, and another pole contributed by both C_1 and C_2 in series. Note that R and C_1 form a proportional and integral filter (PI filter), with the resistor R being the proportional path and the capacitor C_1 being the integral path. Finally, we will also see in Chapter 3 that a good design in choosing the values of R, C_1, and C_2 plays a crucial role in stabilizing the PLL circuit.

2.5 Frequency Divider

2.5.1 Frequency Divider Intuition and Schematic

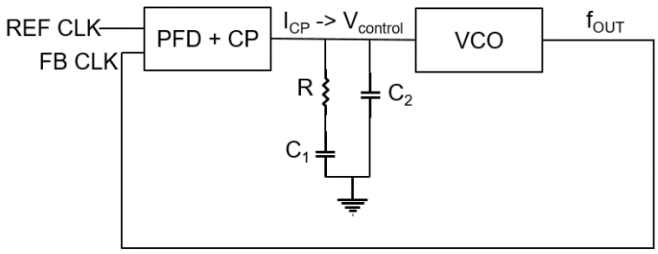

Figure 2.20 Updated PLL Block Diagram

An updated PLL block diagram, as we have discussed thus far, is shown in Figure 2.20. The above PLL will work fine even if there is a step change in the reference clock's frequency, as the feedback clock will be ultimately in phase with the reference clock in steady state. However, there is one component missing. Recall in Chapter 1.3 where we mentioned that one of the key functionalities of a PLL is frequency synthesis. Right now, our PLL is only able to generate an output clock whose frequency is equal to that of the reference clock.

The method to achieve frequency synthesis is in fact quite easy. Due to the PLL negative feedback configuration, our PLL will force the VCO output frequency to be exactly N times that of the reference clock frequency if we connect a divide-by-N frequency divider between the output of the VCO and the input of the PFD.

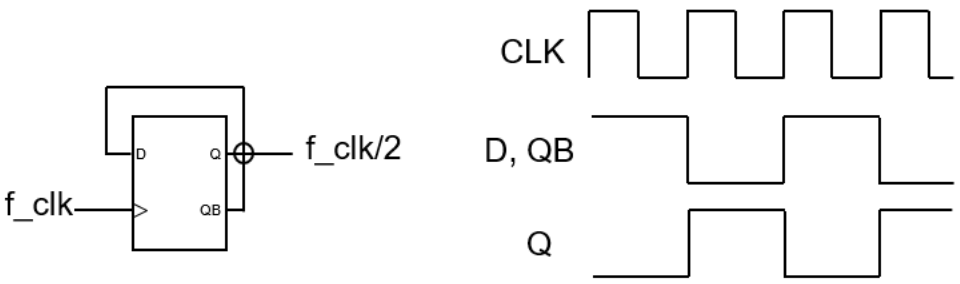

Figure 2.21 Schematic and Waveform of a 50% Duty Cycle Divide-By-2 Frequency Divider

Figure 2.21 shows the schematic and waveform of a divide-by-2 frequency divider with a 50% duty cycle. The frequency divider configuration is quite simple: It's just a DFF with the data port D connecting to its inverse output QB, the original clock feeding into the DFF clock and the divide-by-half clock coming out from the output Q. As we can see in the waveform, Q follows QB at every rising edge of the clock, thereby bearing half the frequency of the input clock and a 50% duty cycle.

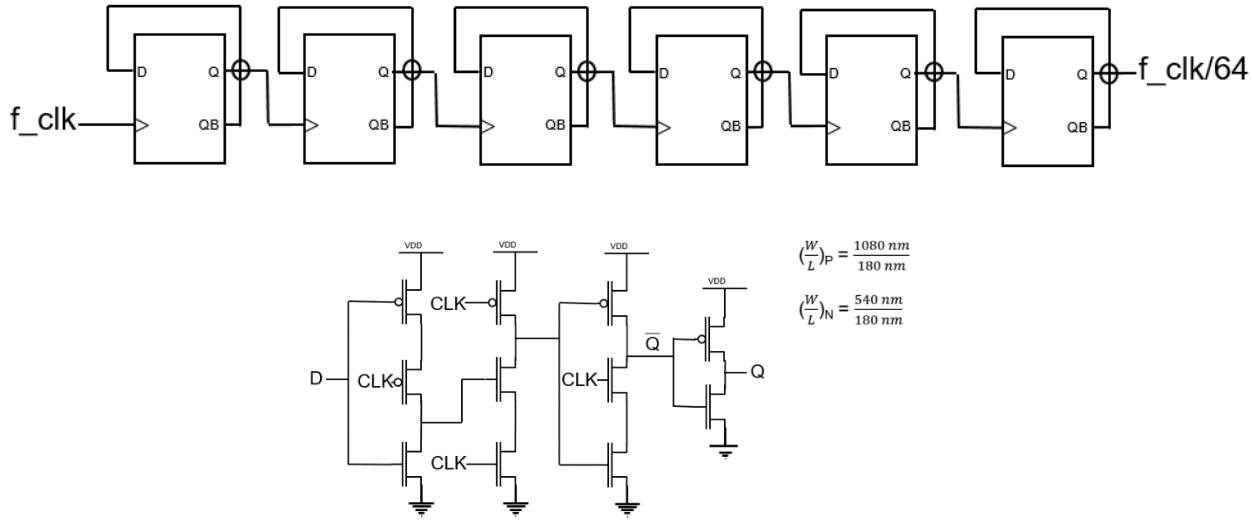

Figure 2.22 Gate and Transistor-Level Design of a ÷64 Frequency Divider

This thesis employs a divide-by-64 frequency divider whose gate and transistor-level designs are shown in Figure 2.22, as our target PLL output frequency is 1.28GHz and our reference clock frequency is 200MHz. Six cascaded D-Flip Flops are connected such that the Q_{BAR} output feeds into the D input, resulting in an output clock frequency to be $1/2^6 = 1/64$ of the input clock frequency with 50% duty cycle. Specifically, true single-phase clock (TSPC)

logic is used to implement the D-Flip Flop, since we know the TSPC D-Flip Flop utilizes relatively few transistors and does not suffer from any clock skews as there is only one single clock in such design. Readers are encouraged to test out other D-Flip Flop logic like clocked-CMOS (C2MOS) logic, etc.

2.5.2 Frequency Divider Linear Model

Since both input and output of the frequency divider are frequencies, the linear model for a divide-by-N frequency divider is simply just $1/N$.

CHAPTER 3

CP-PLL Analysis and Simulation

3.1 PLL Block Diagram and Linear Model

So far, we have discussed and analyzed all components of the CP-PLL, including motivations, working mechanisms, circuit-level schematics, simulated characteristics, as well as their linear models. We are now equipped with the essential knowledge to analyze the entire PLL circuitry and explore its characteristics.

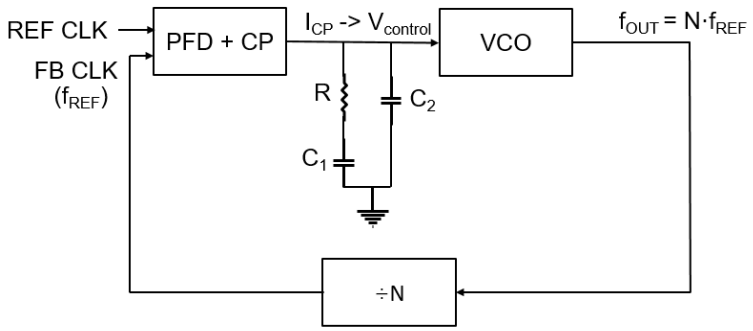

Figure 3.1 Final PLL Block Diagram

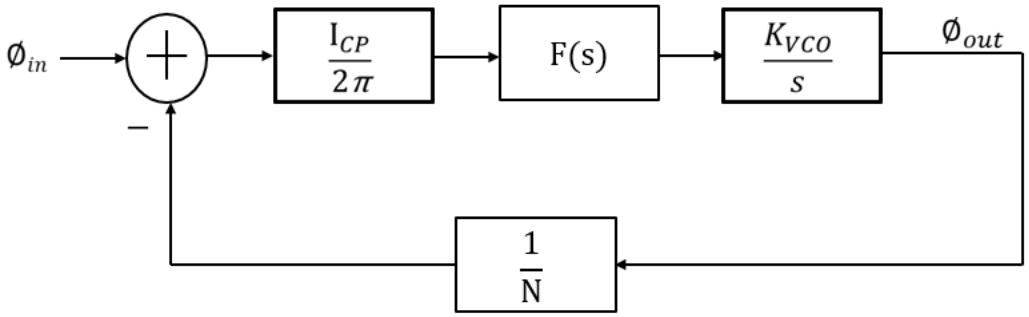

Figure 3.2 PLL Linear Model

Figure 3.1 is our final PLL block diagram that includes the PFD, CP, LF, VCO, and the frequency divider, and Figure 3.2 displays our PLL's linear model. Readers are advised to revisit Chapter 2 where each of PLL components' linear model is discussed.

3.2 PLL Loop Gain

Let us now focus on our CP-PLL stability analysis. From the PLL linear model, we can easily write down the PLL open-loop gain transfer function LG(s):

$$LG(s) = \frac{I_{CP}}{2\pi} \cdot F(s) \cdot \frac{\mathrm{K_{VCO}}}{\mathrm{s}} \tag{3.1a}$$

where the transfer function of the loop filter F(s), as is discussed in Chapter 2.4.2, satisfies:

$$F(s) = \frac{1+RC_1 s}{C_1 s} \cdot \frac{1}{1+\frac{s}{\omega_p}} \tag{3.1b}$$

$$\omega_p = \frac{C_1 + C_2}{RC_1C_2} \tag{3.1c}$$

Here, we can see from Equation 3.1a, 3.1b, and 3.1c that there is one zero and three poles in our PLL loop gain transfer function, with the zero contributed by the resistor in the loop filter. For the three poles, two are from the loop filter, and the remaining one is from the VCO.

3.3 PLL Type and Order

Two important metrics of a PLL are its type and order. The type of a PLL is the number of integrators within the PLL topology, and the order of a PLL is the number of poles within its loop gain transfer function. From our previous discussion in Chapter 2, we know that there are two integrators in our CP-PLL, one integrator being the charge pump and the C_1 in the loop filter, and the other being the VCO. We also just discussed in Chapter 3.2 that our PLL has three poles. Consequently, the CP-PLL in this thesis is a Type-II, 3rd-Order PLL.

3.4 PLL Bode Plot and Stability Analysis

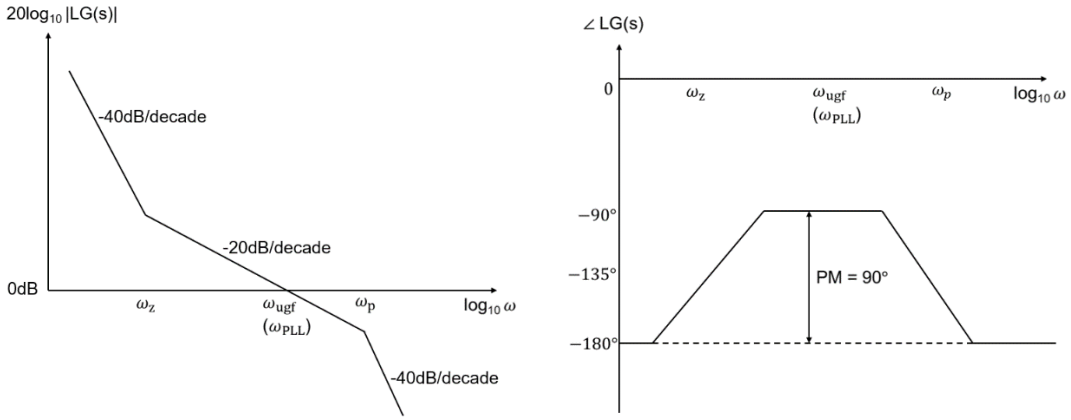

Figure 3.3 Magnitude and Phase Bode Plot of LG(s)

Without plugging in any numbers, we can draw the magnitude and phase Bode plot of our PLL loop gain transfer function as shown in Figure 3.3. Note that the two poles, one contributed by the C_1 capacitor in the LF and the other by the VCO, occur at very low frequencies, and that is why the loop gain's magnitude |LG(s)| initially decreases at a rate of -40dB/decade. When our frequency reaches ω_z, |LG(s)| decreases at a rate of -20dB/decade due to the zero contributed by the resistor R in the LF. As we keep increasing loop gain frequency, we arrive at the unit-gain frequency ω_{ugf} which is also known as our PLL bandwidth ω_{PLL}. At very high frequency, |LG(s)| decreases again at a rate of -40dB/decade since it encounters ω_P, the pole contributed by C_2 in the LF. For the phase Bode plot of LG(s), we can observe that the phase margin PM at ω_{ugf} is 90°, indicating that it is a stable circuit. (For reference, we usually consider circuits whose PMs are greater than 45° to be stable)

Although we will discuss the poles and zeros quantitatively in Chapter 3.5, it is paramount that we get a good grasp of the intuition regarding the placement of the poles and zero in the Bode plot as is shown in Figure 3.3. Previously in Chapter 2.4.1, we learned that the capacitor C_2 should be extremely small to effectively filter out high-frequency components of the control voltage. We can appreciate another merit of the small C_2 from Figure 3.3 that ω_p, primarily contributed by C_2, should be very large, since should the pole frequency be smaller than the PLL unit-gain frequency (ex. $\omega_p < \omega_{ugf}$), our PLL would be unstable. We should also appreciate the presence of the resistor R in the LF responsible for I-to-V conversion that the introduction of a zero to the PLL loop gain transfer function stabilizes the PLL. Without R, the phase Bode plot of LG(s) would be -180° for all frequencies,

and thus the PLL PM would be 0°, indicating an unstable topology! Readers are encouraged to envision the above-mentioned circumstances and explore PLL's stability impacted from the different placements of poles and zeros.

Finally, it is important to know that although one might be tempted to perform the stability analysis in Cadence, there is, in fact, no way we can plot the correct magnitude and phase Bode plot of a PLL in Cadence, since we are interested in the large-scale analysis to obtain the correct Bode plot, while Cadence is only able to perform small-signal stability plots which is inapplicable for closed-loop systems like PLLs [4].

3.5 PLL Quantitative Analysis

In Chapter 3.2, we derived our PLL loop gain transfer function from the linear model. An in-depth analysis of LG(s) gives us the one zero and three poles listed as follows:

$$\omega_z = \frac{\omega_{ugf}}{\sqrt{\frac{C_1}{C_2}+1}} = \frac{1}{RC_1} \qquad \omega_{p1}, \omega_{p2} \ll \omega_z \qquad \omega_{p3} = \frac{C_1+C_2}{RC_1C_2} \tag{3.2}$$

As is discussed in Chapter 3.4, the poles and zero frequencies should satisfy:

$$\omega_{p1}, \omega_{p2} \ll \omega_z < \omega_{p3} \tag{3.3}$$

From LG(s) phase Bode plot, we can derive the relation between C_1, C_2, and the phase margin PM as shown in Equation 3.4:

$$\frac{C_1}{C_2} = 2\left(tan^2(PM) + \tan(PM) \cdot \sqrt{tan^2(PM)+1}\right) \tag{3.4}$$

From LG(s) magnitude Bode plot, we can arrive at Equation 3.5 regarding the charge pump output current I_{CP} as shown in Equation 3.5:

$$I_{CP} = \frac{2\pi C_2}{K_{VCO}} \cdot {\omega_{ugf}}^2 \cdot \sqrt{\frac{{\omega_{p3}}^2 + {\omega_{ugf}}^2}{{\omega_z}^2 + {\omega_{ugf}}^2}} \tag{3.5}$$

The PLL loop gain we were discussing throughout the thesis is the open-loop gain, and we can find its closed-loop gain CLG(s) to be:

$$CLG(s) = \frac{\emptyset_{out}(s)}{\emptyset_{REF}(s)} = \frac{LG(s)}{1+LG(s)/N} \tag{3.6}$$

Finally, to design a stable circuit, our CP-PLL's bandwidth should be much smaller than the reference clock frequency as follows:

$$f_{PLL} = f_{ugf} < \frac{f_{REF}}{10} \tag{3.7}$$

3.6 PLL Choice of Parameters

In our CP-PLL topology, there are four parameters we need to choose for simulation: R, C_1, C_2, and I_{CP}. We learned in Chapter 3.4 that Cadence cannot plot PLL's magnitude and phase Bode plot, so we need to make some assumptions of our PLL to come up with a successful design. This thesis assumes that our CP-PLL has a bandwidth f_{PLL} of 1.5MHz, a phase margin PM of 60°, and the charge pump current I_{CP} of $100\mu A$. Combining these assumptions with our simulated VCO gain as is discussed in Chapter 2.1.4 (K_{VCO} = 551MHz/V) and incorporating them with the quantitative analysis in Chapter 3.5, we arrive at our chosen parameters for our PLL topology as listed below:

1. PLL reference and output clock frequency: $f_{REF} = 20MHz, f_{OUT} = 1.28GHz$
2. LF parameters: $R = 11.8k\Omega, C_1 = 33.558pF, C_2 = 2.596pF$
3. PLL pole and zero frequency: $f_p = 5.6MHz, f_z = 0.402MHz$

3.7 Simulated PLL Characteristics

3.7.1 PLL Transient Simulation

We have thus far discussed all fundamental topics and conducted in-depth analysis of our PLL, and it's time to simulate the entire CP-PLL characteristics. Regarding the Cadence simulation of various individual PLL components' characteristics, readers can consult Chapter 2.

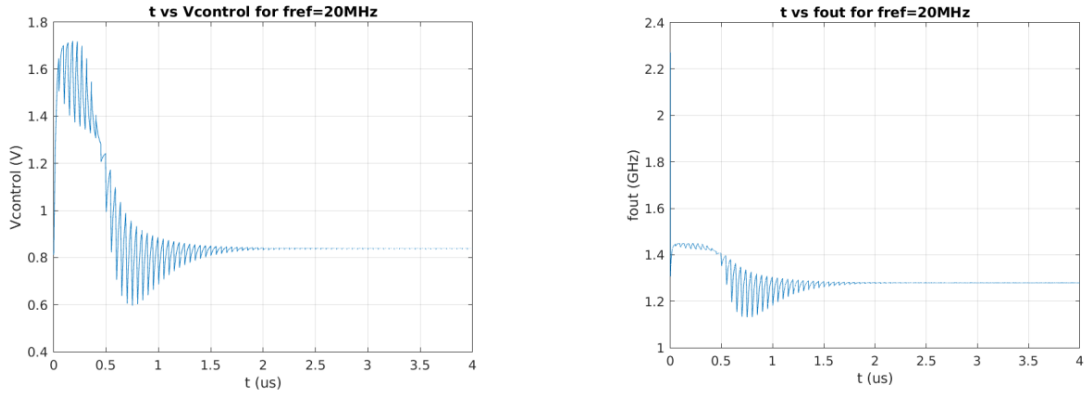

Figure 3.4 PLL $V_{control}$ and f_{out} Transient Simulation

One of the first and foremost characteristics of the PLL is its transient simulation, since it is the transient analysis that gives the designer a clear idea if the PLL can lock under steady state. Figure 3.4 illustrates the two ways to identify the correct functionality of a PLL: $V_{control}$ and f_{out} transient simulation. As we can see, after some long time in steady state, the control voltage of the VCO stays fixed at around 0.83V, while the PLL output frequency stays unchanged at 1.28GHz.

3.7.2 PLL Phase Noise and Jitter Simulation

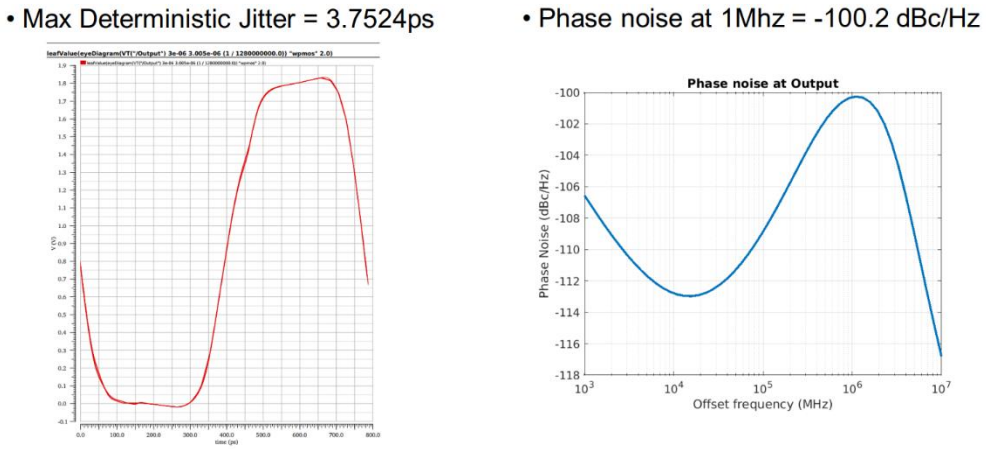

Figure 3.5 PLL Deterministic Jitter and Phase Noise Simulation

One key metric of a good PLL is its low phase noise and jitter. Here, phase noise refers to the random perturbation of the PLL output clock, while jitter is the predictable and repeatable noise of a signal usually expressed as a peak-to-peak value. Figure 3.5 plots the maximum deterministic jitter as well as the phase noise of our CP-PLL, and we can make the safe conclusion that our design is a relatively low-noise PLL.

To perform the jitter measurement in Cadence, one can generate an eye diagram in the transient analysis, zoom into one period of the signal-of-interest and measure the maximum deterministic jitter. To measure PLL phase noise, one can do a pss and pnoise analysis in Cadence.

3.7.3 PLL Lock and Capture Range Simulation

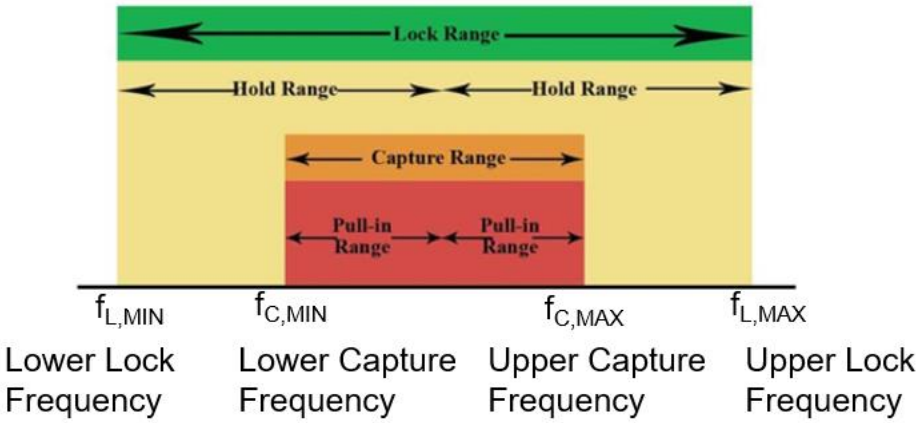

Figure 3.6 PLL Lock, Hold, Capture, and Pull-In Range Diagram

Other essential PLL characteristics include its lock, hold, capture, and pull-in range. Figure 3.6 offers a vivid demonstration of these concepts. The lock range of a PLL is quite straightforward: It is simply the range of the reference clock frequencies so that the PLL can lock under steady state. The capture range of a PLL describes the range of reference clock frequencies such that for a PLL operating in lock condition at a specific f_{REF}, the PLL is still able to maintain lock in steady state after f_{REF} changes. A PLL's capture range should be less than its lock range since if the reference clock undergoes significant frequency variations in a very short time, a PLL usually is not able to endure such drastic changes of f_{REF}. The hold range is half of the lock range, while the pull-in range is half of the capture range since they both start from the PLL's target or center frequency.

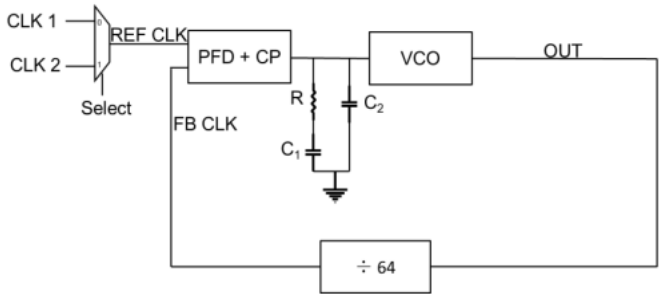

Figure 3.7 Schematic for Finding PLL's Capture Range

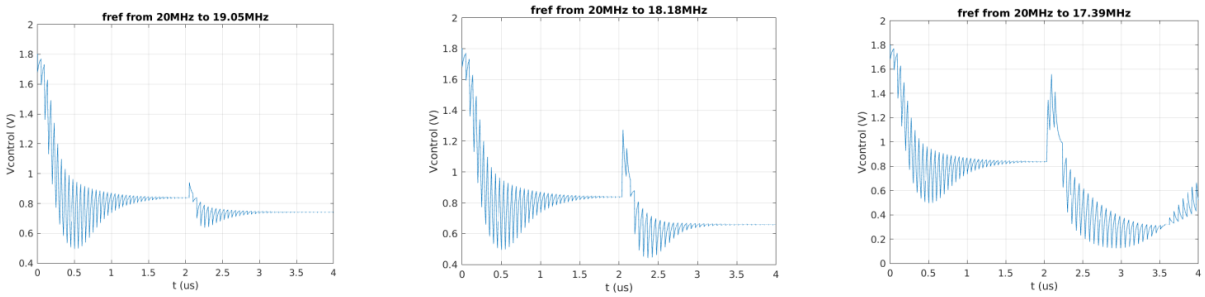

Figure 3.8 Simulation in Determining PLL's Capture Range

To find out CP-PLL's lock range, we simply sweep the reference clock frequency and perform transient analysis on either $V_{control}$ or f_{out} to see if our PLL can lock under steady state. The simulated lock range of our PLL is 16.67MHz to 22.23MHz for the reference clock frequency.

To find the capture range, we need to have a step change in the reference clock frequency. Figure 3.7 shows the implemented schematic, where we use a 2:1 MUX whose two inputs are the two different reference clock frequencies. The select signal of the MUX is a pulse voltage source that goes from low to high after our PLL is in steady state. Parametric sweeps of the reference clock frequency are implemented in the simulation of PLL's capture range. As we can see in Figure 3.8, as the PLL undergoes a step change in its reference clock frequency, it is able to lock for the first two cases but fails at the third case since the control voltage starts to oscillate. The simulated capture range of our PLL is 18.18MHz to 21.62MHz for the reference clock frequency.

CHAPTER 4

Conclusion and Future Work

4.1 Conclusion

To conclude, the thesis employs 180nm technology in the design of a charge pump phase-locked loop. The PLL output frequency is centered at 1.28GHz, with a reference clock frequency of 20MHz that can be generated by a crystal oscillator. For the designed voltage-controlled ring oscillator, it has an oscillation range from 1.09GHz to 1.46GHz, with a VCO gain of 551MHz/V at the target 1.28GHz PLL frequency. The PLL's phase frequency detector is comprised of NOR-based resettable DFFs, and its charge pump utilizes a differential topology with a biasing current of 100 μA that yields relatively small output current mismatches. The loop filter has the RC parameters of $R = 11.8k\Omega, C_1 = 33.558pF, C_2 = 2.596pF$, and a divide-by-64 frequency divider composed of TSPC-based DFFs is dedicated for the PLL's frequency synthesis. Overall, our Type-II, 3rd-Order CP-PLL has two poles at very low frequencies and the third pole at 5.6MHz and a zero at 0.402MHz. It is able to lock within $2\mu s$ of simulation and has a maximum deterministic jitter of 3.7524ps and phase noise less than -100dBc/Hz. The lock range of our PLL reference clock is 16.67MHz to 22.23MHz, and the capture range is 18.18MHz to 21.62MHz.

4.2 Future Work

This thesis provides readers with a solid foundation regarding the basic framework and fundamentals of a CP-PLL, and future work is needed to further improve the design.

From Figure 2.2 regarding the VCO frequency versus $V_{control}$ curve, we can clearly see that our VCO design in Figure 2.1 has a non-linear tuning characteristic since the VCO frequency does not change when the control voltage is less than the threshold voltage of the NMOS in the pull-down network of the inverters in the VCO. An improved version of the VCO as is shown in Figure 4.1 utilizes positive feedback and will have a much linear frequency tuning

range, since both the PMOS and NMOS in the pull-up and pull-down network will ensure the VCO is actively working at full swing of the control voltage.

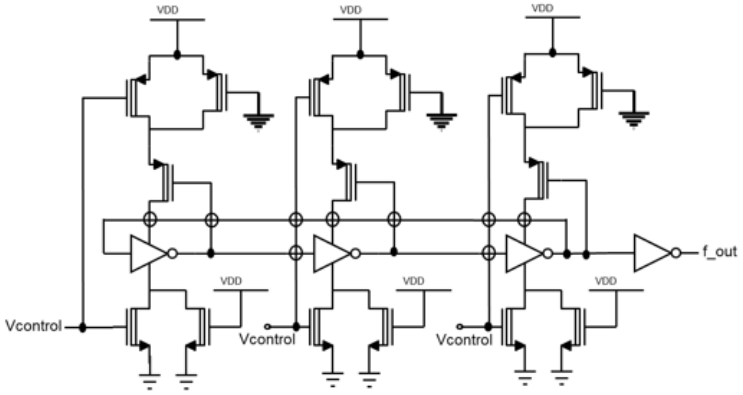

Figure 4.1 Improved VCO Configuration Utilizing Positive Feedback

It is worth noting that this thesis does not dive into many of the advanced yet essential topics of PLL, such as strategies to minimize phase noise [5], reduce power consumption [6], and enhance output frequency resolution [7], etc. Improved charge pump topology with lower biasing current and smaller current mismatches, novel phase frequency detectors that have higher gain and lower jitter under very high operating frequencies, and VCOs with more linear tuning characteristics are all potentials for future work for the design of a successful CP-PLL.

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