

{ 9zpm AMU#123 → password?
Username - afzalmalik }

→ How to design CMOS Inverter in cadence Virtuoso.

Connect

↓
yes.

Computer → (10.0.26.165)
display - True color (24 bit)

don't give ~~#~~ space in name of folder/file.

open - folder - Right click - terminal

writel C8h

source /home/cadence/cshrc

chip startup message appears.

→ Virtuoso

.log file opens

click on file → New → library. → New library window opens

Name → inverter

inside select "attach to an existing tech library" option.

click on apply. → New window appears.

Select gpdk090

generally process (90nm) ~~new~~
development kit

click apply

Flow →
1) SCH
2) Sym
3) Simulate

DATE / /
PAGE NO.

→ Click → file → New → cell view → library -> Select
: type schematic , with schematic
cell → "inverter_cell".

Click OK & wait.

New window appears. (maximize it)

Sometimes
instead of
window
pop appear

↓
click on
session
then
windows
appears.

→ This is schematic Editor window.

click on create instance (Short key → I)

Click browse → New window (library browser
add instance)

* Components are called instances.

Click on g_pdk090 → nmos1v → symbol
(library) (cell) (view)

→ Next Add Instance
→ window open
length → 100nm.
width → 120nm

click hide

NMOS will be attached.

click → ESC

→ click F on keyboard. → fullscreen.

Same process for PMOS

Add instance → library (g_pdk090) → cell (pmos)

{ same sizes should be undisturbed → Minimize (symbol) View }

Click hide

PMOS will be attached to cursor

Click → esc

→ Create pin. → Name (Vdd ~~Vin~~ space Vin space Vss).
direction (input) → hide

Place Vdd, Vin, Vss accordingly
click esc.

Create pin. → Name (Vout) → direction (output)-hide

Click → create narrow circle icon.

Click on Drain of pmos. then leave click and again take cursor to drain of nmos and then click.

In similar way connect gates of both transistors; connect output, connect Vdd and Vss).

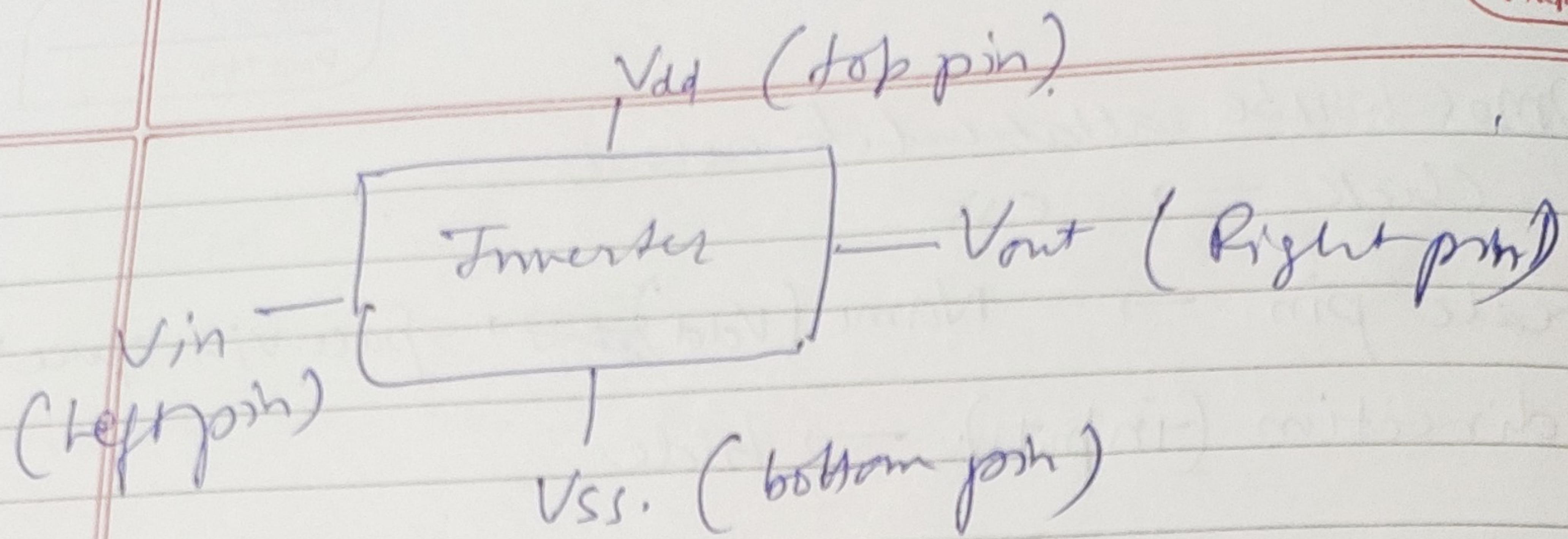
→ Connect body of both pmos and nmos

Click save:

Click check and save → go to virtuoso → no errors → check log file
Click close if errors shown then first resolve
and then click & save.

Create cell → cell view → from cell view.

Symbol generation options window opens.



Symbol Editor window opens.

Check & save

[@ part name] → ~~left click~~ → Right click
check & save ← "inverter" type

Minimize → then open virtinsto window

click file → ~~new~~ → cell view. → Cell (inverter_cell_tb)

press OK.

↓
test bench

New window opens

lib(gpk090).

create instance → browse → lib browser add, myname
lib(inverter). → cell(inverter_cell) → symbol.

Add Instance window

→ click hide.
click once → then esc.

Add Instance

lib(analoglib) → Cell(vde) → view(symbol)
Minimize.

Another window appears

DC voltage (1-8). → hide
voltage attached to cursor

Ctrl S key

Click Q for properties click Q when pin box
appears on icon.

→ Cell (vpulse) → view (symbol)
Voltage 1 (0V) → Voltage 2 (1.8V)
period (20n). → pulse width (10n).

$$PW = (\text{period}/2)$$

Delay time (0.).

Rise > (1n)
fall > (1n)

Hide → voltage source attached to cursor.
click and then esc.

Foregrounds Add instance

Lib (analog lib) → Cell (gnd) → view (symbol)

Gnd attached to cursor

placed at 3 place (1 - Vdd Keniche, 2 - Vss Keniche
3 - Vin Keniche)

Create pin - (Vin) → input

Create pin (vout) → output

Create narrow wire → ~~connect~~ ^{Made} all useful connections
some & check

On Leftmost → click launch (ADE-L)

Choose little icon showing AC, DC + click

→ pop up window (choose analysis) appears

→ select transient

Stop time → 100n

moderate

→ select DC

Same dc op. point

Component parameter

Select component → arrow appears

Sweep Ray

- Start Stop Plot 0 Stop 1.8

ADE L(1) — both analysis got added

click — outputs — to be plotted

current on wire — Selection design

vin (click) — free name of Vout

Now,

ADE L — out output

✓ vin
✓ vout

Now

▷ Next And Run

And wait

(lots of errors)

ADE L
window

selection → more tools
→ ok

Vinhouse window To close click

type exit enter

again (click to startup)

→ Now, again reopen using previous
commands

→ file - open — library — Inverter |
inverter-cell-tb

open for - edit

Look

again - launch - ADE L

again - selection - Ideal tools

again - error

=

again repeat steps

Intran waveform → click split

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