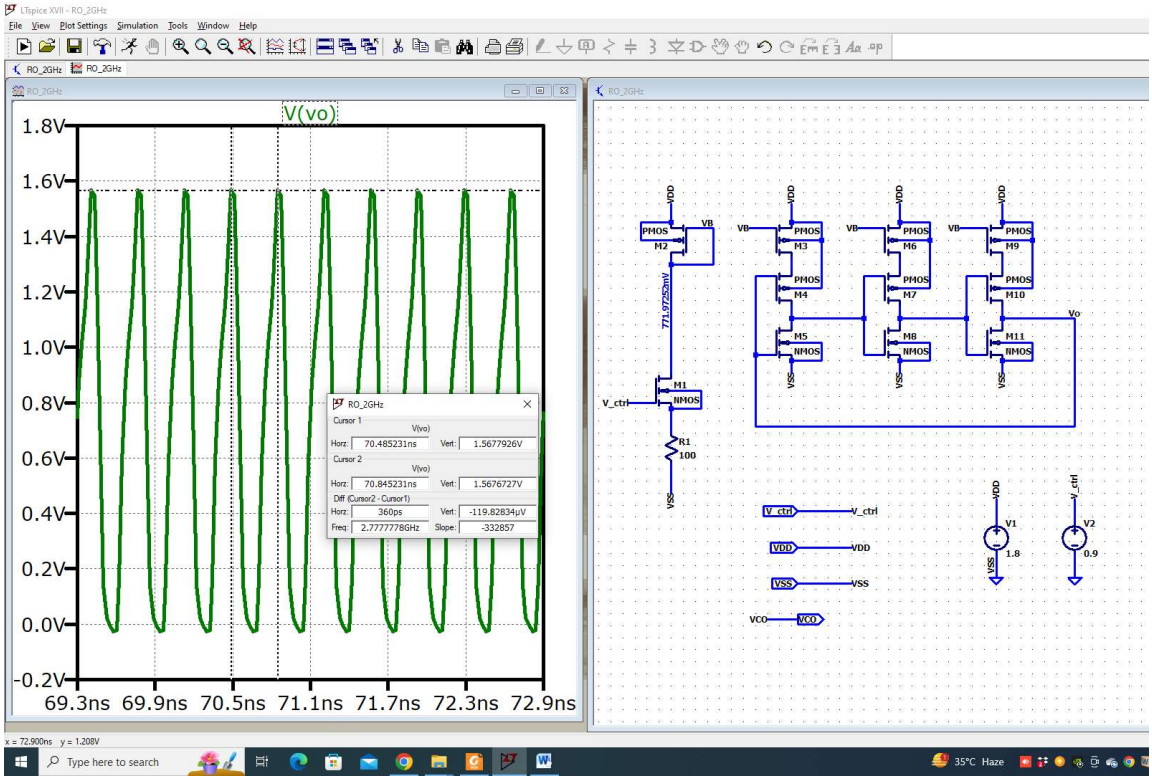
PLL for Clock Synthesis Design Steps

1. Let the available crystal oscillator frequency be F_{ref}
2. Design a VCO that generates the desired frequency ($F_{desired}$) at a control voltage V_control = $V_{dd}/2$
3. Design divide by N counter such that N = $F_{desired}$ / F_{ref}
4. Design Charge Pump PFD having charge pump current I_{CP}
5. Chose loop bandwidth of the loop filter $F_{loop} < F_{ref}/20$
6. Calculate R_s of the loop filter using the equation $F_c = \frac{Rs\ x\ Icp\ x\ Kvco}{2\pi N}$
7. Chose zero frequency of the loop filter $F_Z <= F_C/3$
8. Calculate C_S of the loop filter using the equation $F_Z = \frac{1}{2\pi Rs.Cs}$
9. Chose pole frequency of the loop filter $F_P >= 3F_C$
10. Calculate C_P of the loop filter using equation $F_p = \frac{1}{2\pi Rs.Cp}$
11. Adjust the values of C_S and C_P (while satisfying $3.F_Z < F_C < F_P/3$) so that $C_S/C_P \approx 10$. This is to ensure a phase margin of greater than 50^0 and stability of the PLL

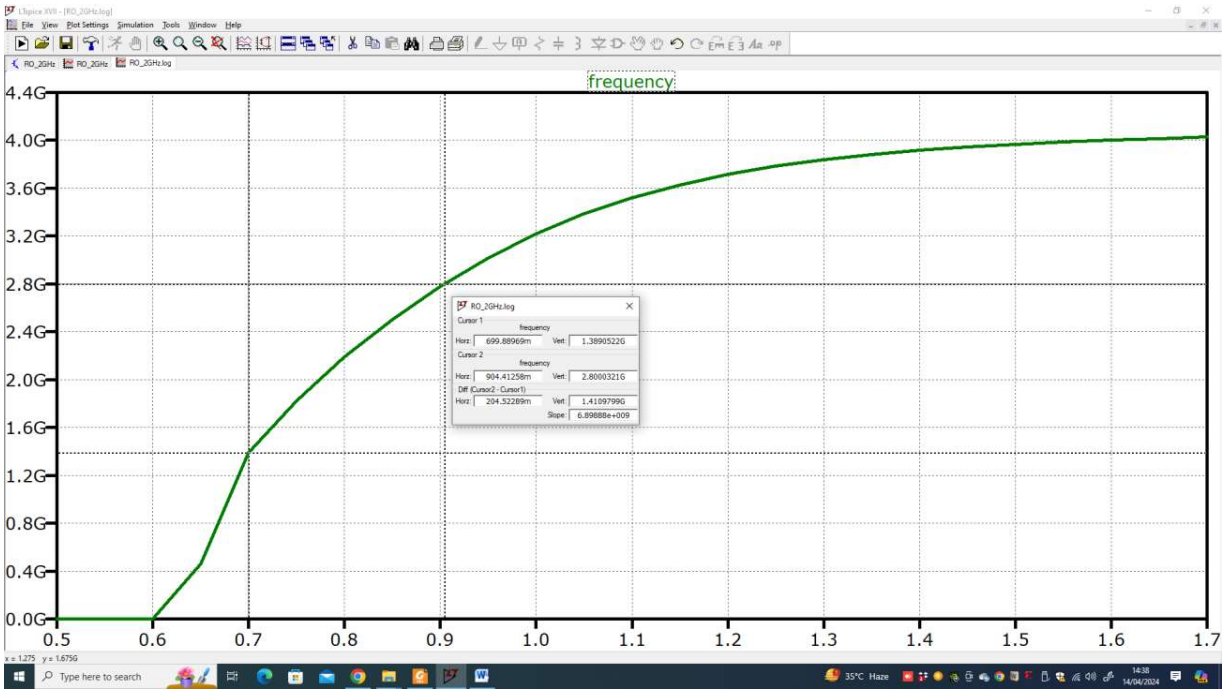
Example: Design a PLL to generate/synthesize a clock frequency of 2.5 GHz

Step-1: Let the available crystal oscillator be of F_{ref} = 62.5 MHz

Step-2(a): A 3 stage RO is designed to have a frequency 2.7789 GHz at V_control = 0.9V.



Step-2(b): Kvco of the designed oscillator is measured to be 6.8988 GHz/V



Step-3: A divide by 40 counter is designed. Since 2.5GHz / 62.5 MHz = 40.

Step-4: A PFD with I_{CP} = 15 uA is designed usind D Flip-flop, NAND gate and current mirror

Step-5: Let loop band width of loop filter be F_C = 62.5 MHz / 25 = 2.5 MHz

Step-6: R_S = (2πN x 2.5 MHz)/(15 uA x 6.8988 GHz/V) = 6 kOhm

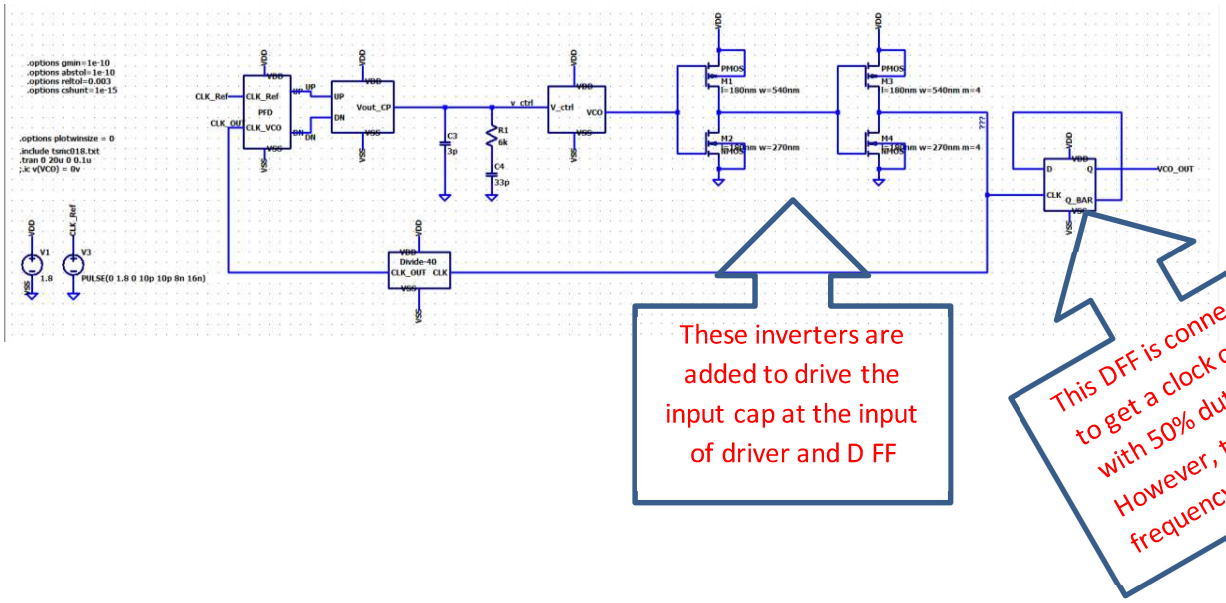
Step-7: Let zero frequency be F_Z = 2.5 MHz / 3 = 0.833 MHz

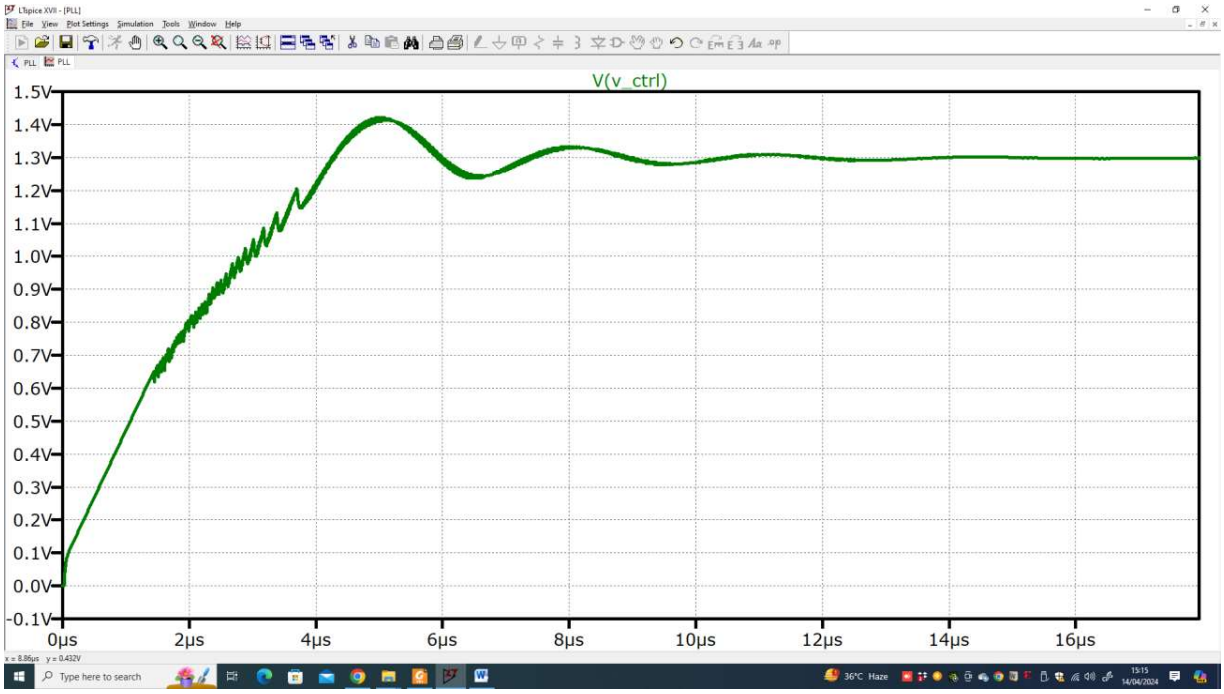
Step-8: Capacitor C_S = 1/(2π x 6 kΩ x 0.8333 MHz) = 31.8 pF

Step-9: Let pole frequency F_P = 3 x 2.5 MHz = 7.5 MHz

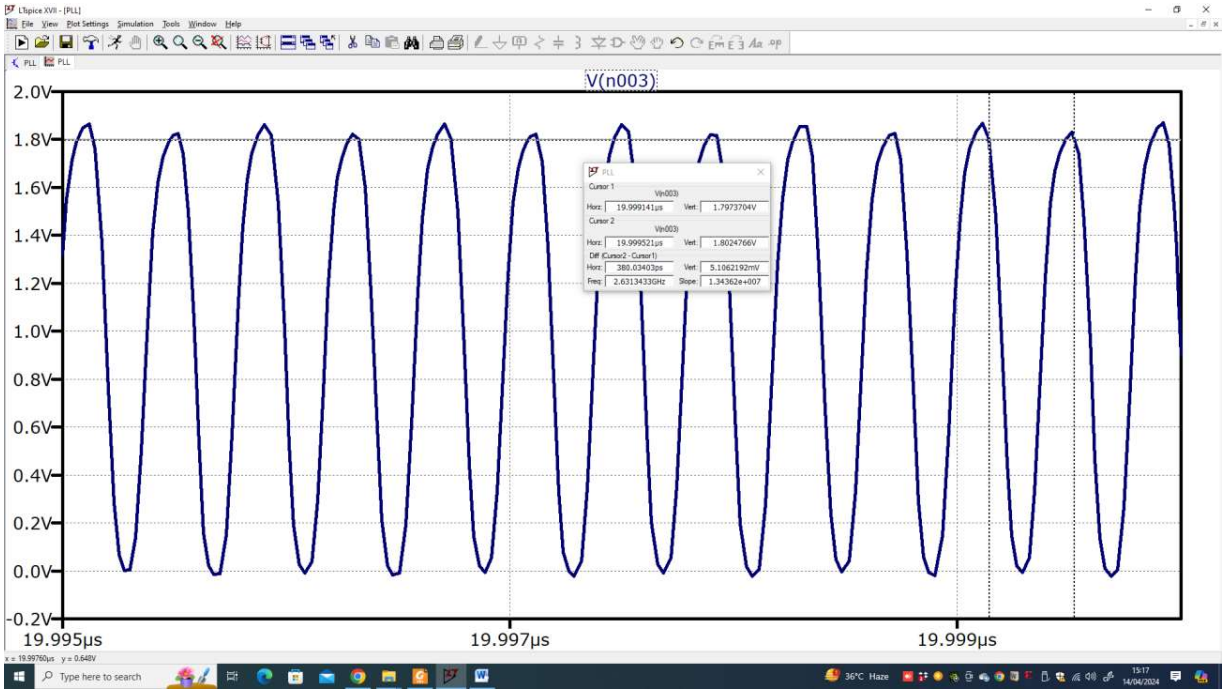
Step-10: Capacitor C_P = 1/(2π x 6 kΩ x 7.5 MHz) = 21 pF

Step-11: With the above values of C_S and C_P, the Phase Margin = 11^0 only. PLL not stable. Therefore, let C_P = 3.3p pF and C_S = 33 pF

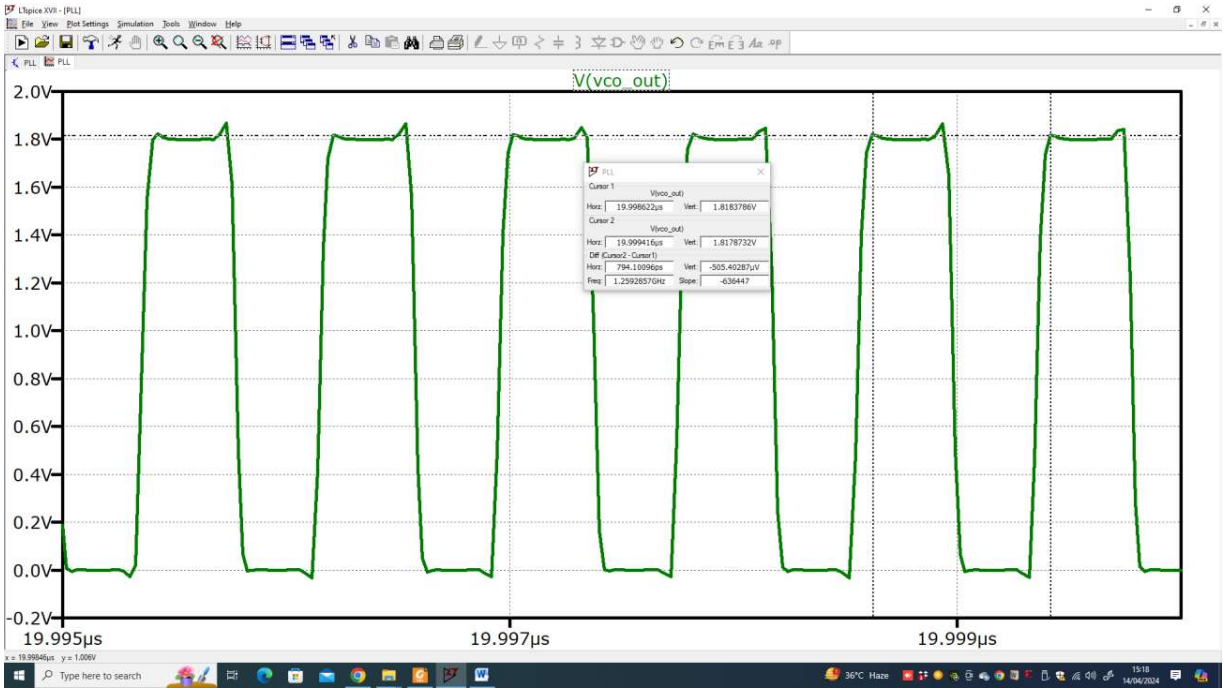




Transient response of the control voltage at the input (output) of VCO (PFD).



2.63 GHz frequency is obtained at the input of DFF/ divider



1.259 GHz frequency is obtained at the output of the DFF