Design of Phase Locked Loop

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***Abstract*—This project aims to design a Phase-Locked Loop (PLL) in LTSpice, utilizing a 180 nm technology node at supply voltage Vdd = 1.5V. The PLL is designed to operate at a frequency of 2.4 GHz, which aligns with the frequency bands commonly used in wireless communication systems such as Bluetooth and Wi-Fi. The architecture comprises a Phase Frequency Detector (PFD), Charge Pump (CP), second-order Low Pass Filter (LPF), and an LC-based Voltage-Controlled Oscillator (LC-VCO) to ensure stable frequency generation with low phase noise.**

***Index Terms*—Phase-Locked Loop (PLL),Phase Frequency Detector (PFD), Charge Pump (CP), Low Pass Filter (LPF), Voltage-Controlled Oscillator (VCO) .**

I. Introduction

A. Overview

Phase-Locked Loops (PLLs) are fundamental components in modern electronic systems, essential for generating stable, high-quality clock signals in a wide range of applications, from telecommunications to computer systems. They are highly valued for their flexibility, as they can be programmed to adjust their output frequency across a broad range, making them adaptable to various system requirements. This ability to operate at very high frequencies, while maintaining stability over extended periods, is particularly advantageous in systems where precise frequency generation is crucial. As a result, PLLs are ideal for applications that require a consistent clock signal without frequent adjustments [1, 2].

PLLs have traditionally combined both analog and digital components, resulting in complex designs that require specialized expertise. However, the rise of fully digital PLL designs has led to more compact and energy-efficient alternatives. Despite the advantages of digital PLLs in terms of size and power consumption, they still lag behind their analog counterparts in terms of output signal quality [2].

As semiconductor technology advanced and circuit speeds increased, generating high-frequency, high-quality clocks directly on-chip became a significant challenge, especially for frequencies exceeding a few hundred MHz. Transmitting these high-frequency clocks via traces on printed circuit boards (PCBs) introduced various issues such as signal degradation, waveform distortion, and noise coupling, which compromised data integrity. Furthermore, clock traces acted as antennas, emitting radiation that could interfere with other circuits [1].

In response to these challenges, PLL circuits emerged as a reliable solution for generating stable, low-jitter on-chip clock signals. Although traditionally bulky, PLLs are preferred in many systems for their ability to produce superior clock signal stability. They typically use an off-chip, high-quality reference clock source, such as a quartz crystal oscillator, to generate an output frequency that is a multiple of the reference, maintaining jitter levels close to that of the reference clock.

B. Design of PLL

The basic concept of a Phase-Locked Loop (PLL) is depicted in Figure 1. A PLL system utilizes an off-chip oscillator, typically a high-quality, stable quartz crystal oscillator, as the reference frequency (denoted as f_{REF}). The other components of the PLL circuit are integrated on-chip [2].

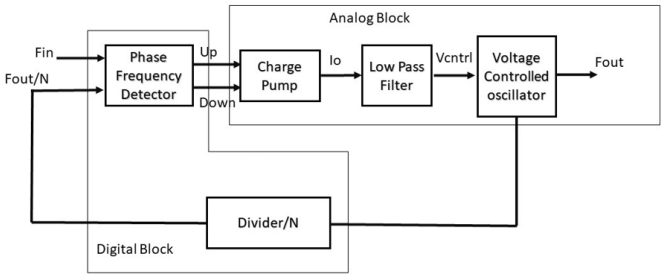

Fig. 1: Block diagram of PLL

The main elements of a PLL include [2, 3]:

- **Phase Frequency Detector (PFD):** The PFD compares the phase and frequency of the reference signal with the feedback signal from the output of the VCO. It generates an error signal proportional to the phase difference, which drives the loop.
- **Charge Pump (CP) and Loop Filter (LF):** The charge pump converts the error signal from the PFD into a control voltage. The loop filter then smoothens this voltage, minimizing high-frequency noise and stabilizing the control signal.
- **Voltage-Controlled Oscillator (VCO):** The VCO generates an oscillating signal whose frequency is determined by the control voltage. This block is crucial for producing

the desired output frequency and plays a central role in frequency synthesis.
- **Frequency Divider:** The divider scales down the frequency of the VCO output to match the reference frequency. This allows the PLL to lock to a lower reference frequency while maintaining high output frequencies.

The PLL operates in a feedback loop where the phase difference between the reference signal and the VCO output is continuously monitored and corrected. When the phase of f_{REF} precedes f_{PLL}, the phase detector triggers positive pulses that increase the control voltage to the VCO, raising its frequency. Conversely, if f_{PLL} leads f_{REF}, the phase detector generates negative pulses that lower the VCO frequency. This process ensures that the output frequency of the PLL matches the reference frequency while maintaining a consistent phase relationship [2].

The feedback mechanism of the PLL ensures that the output signal converges to the intended frequency and remains synchronized with the phase of the reference clock, providing a stable and reliable clock signal for various applications.

II. Design of Voltage-Controlled Oscillator (VCO)

A. Overview of Voltage-Controlled Oscillator (VCO)

A Voltage-Controlled Oscillator (VCO) generates an oscillating signal whose frequency is modulated by a control voltage. It is a critical component in high-frequency circuits such as Phase-Locked Loops (PLLs), frequency synthesizers, and clock recovery systems. The key design objectives of a VCO include achieving stable oscillations, wide tuning range, minimal phase noise, and high power efficiency. These parameters play a vital role in determining the overall performance of a VCO in its target application [3].

B. Comparison of Ring VCO and LC VCO

Two common topologies for VCO design are the Ring VCO and the LC VCO, each with distinct advantages and trade-offs [3, 4]:

a) Ring VCO: A Ring VCO consists of multiple cascaded inverting stages arranged in a ring configuration. The frequency of oscillation is determined by the propagation delay of each stage.

- **Advantages:**
  - Simple design and smaller chip area.
  - Wide tuning range due to its delay-based operation.
  - Easy integration in digital processes, as it relies on standard CMOS devices.
- **Disadvantages:**
  - Poor phase noise performance, particularly in high-frequency applications, due to the lack of a high-Q resonant structure.
  - Lower frequency stability, making it less suitable for applications demanding precise frequency control.

b) LC VCO: An LC VCO utilizes an LC resonant tank circuit to define the oscillation frequency. This topology achieves oscillations through the interaction of inductance (L) and capacitance (C).

- **Advantages:**
  - Superior phase noise performance due to the high Q-factor of the LC tank circuit.
  - Excellent frequency stability, particularly in GHz-range applications.
- **Disadvantages:**
  - Larger chip area due to the inductor and capacitor.
  - Slightly more complex design and layout compared to Ring VCOs.

C. Selected Topology (NMOS LC VCO with MOS Varactors):

For this design, the NMOS LC VCO topology was selected due to its superior performance in high-frequency applications like PLLs [4, 5].

a) Reasons for Selecting LC VCO:

- **Frequency Stability:** The LC oscillator's reliance on a high-Q resonant tank ensures frequency stability, especially at 2.4 GHz.
- **Low Phase Noise:** The LC topology inherently suppresses phase noise, producing cleaner signals critical for communication systems.
- **Power Efficiency:** This topology provides high power efficiency in high-frequency circuits, minimizing power consumption.
- **Tuning Capability:** The use of MOS varactors allows fine-tuning of the oscillation frequency over a specified range by varying the control voltage.

b) Negative Resistance Realization Using Cross-Coupled NMOS Transistors: In an LC VCO, the loss in the resonant tank circuit, primarily caused by the finite Q-factor of the inductor and capacitor, must be compensated to sustain oscillations. This is achieved by generating a negative resistance using a cross-coupled NMOS transistor pair [4].

1) **Concept of Negative Resistance:**
   - The cross-coupled NMOS pair introduces a negative conductance, $-G_m$, that cancels the tank's resistive losses.
   - This ensures that the energy dissipated in the tank is replenished continuously, maintaining sustained oscillations.
2) **Implementation:**
   - Two NMOS transistors are connected in a cross-coupled configuration, with their gates and drains cross-linked.
   - The transistors operate in the saturation region, and their transconductance (G_m) is designed to meet the condition:

$$G_m \geq \frac{1}{R}$$

   where R represents the equivalent resistance of the LC tank circuit.

3) **Advantages of Cross-Coupled NMOS Design:**
   - Compact and efficient implementation of negative resistance.
   - Facilitates stable oscillation startup.
   - Maintains minimal power consumption while compensating for tank losses.

The combination of the high-Q LC tank and cross-coupled NMOS negative resistance ensures robust oscillation at the desired frequency with low phase noise and high power efficiency.

D. Design Principles of LC VCO

The oscillatory behaviour of an LC VCO depends on satisfying two conditions [4]:

1) **Negative Conductance Cancellation:** The negative conductance introduced by the active device cancels out the positive conductance (loss) of the LC tank circuit as shown in Figure 2. This ensures sustained oscillations.
2) **Zero Phase Shift:** The closed-loop gain of the circuit must exhibit zero phase shift. This criterion ensures phase alignment for oscillation.

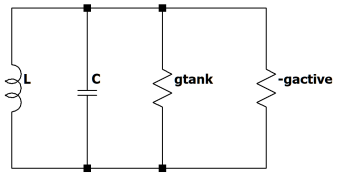

Fig. 2: Basic LC tank Circuit

To implement this design:

- An NMOS transistor provides the negative resistance required for oscillation.
- The LC tank circuit, consisting of an inductor (L) and a variable capacitor (C), determines the oscillation frequency. The capacitor is implemented using MOS varactors, allowing frequency tuning via the control voltage.

E. Design Calculations

The design of the LC VCO is based on achieving a target frequency of 2.4 GHz with a control voltage of $V_{\text{ctrl}} = 0.6$ V. The following calculations illustrate the design process:

1) **Tank Circuit Design:** Assume the following parameters:
   - Inductance (L) = 1 nH
   - Quality Factor (Q) = 10
   - Series Resistance (R) = 1.5 Ω

   Using the relationship:

$$Q = \frac{L \cdot \omega}{R}$$

   The angular frequency (ω) of the oscillation is determined as:

$$\omega = \frac{1}{\sqrt{L \cdot C}} \cdot \sqrt{1 - \frac{R^2 \cdot C}{L}}$$

   To achieve a frequency of $f = 2.4$ GHz:

$$C = 4.3\,\text{pF}$$

2) **Transconductance (Gm):** The transconductance of the NMOS transistor (G_m) must exceed the tank loss to sustain oscillation:

$$G_m > \frac{\alpha R}{L} C$$

   Taking $\alpha = 1$, $G_m > 6.45$ mS. The selected value for G_m is 10 mS.
   Using:

$$G_m = \frac{2I_D}{V_{\text{ov}}}$$

   For $I_D = 750\,\mu$A, transistor dimensions are obtained:
   - Length (L) = $0.36\,\mu$m
   - Width (W) = $153.8\,\mu$m

3) **MOS Varactor Implementation:** The capacitance in the tank circuit is implemented using MOS varactors, providing a tunable range to adjust the frequency as a function of V_{ctrl} [6].

III. Schematic and Design Parameters

Figure 3 shows the schematic of the designed NMOS LC VCO. It consists of a cross-coupled NMOS transistor pair (M1 and M2) to realize negative resistance and an LC tank circuit with MOS varactors (M3 and M4) for frequency tuning. The schematic also includes the bias current source and supply voltage setup.

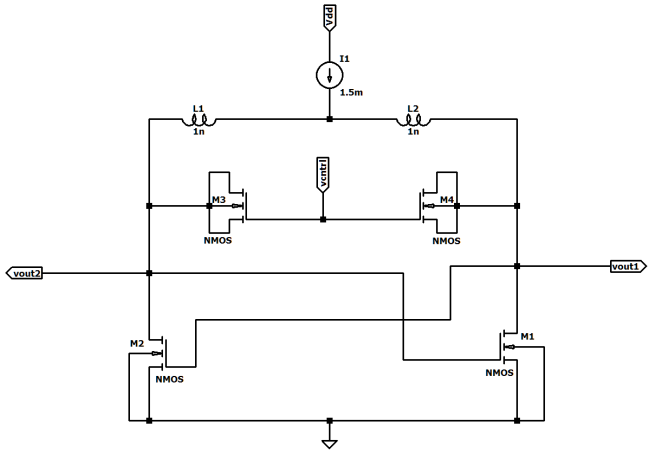

Fig. 3: Schematic of the NMOS LC VCO with MOS varactors.

The width and length of the MOS transistors used in the design are listed in Table I, and the key testbench conditions are summarized in Table II.

IV. VCO Simulation Results

To validate the functionality of the designed VCO, transient analysis was performed using LTSpice. The differential output of the VCO, represented as $v_{out1} - v_{out2}$, was analyzed, and the resulting oscillations are depicted in Figure 4.

TABLE I: Dimensions of MOS Transistors in the VCO Design.

Transistor	Width (W)	Length (L)	Parallel Devices
M1 (NMOS)	153.8 µm	0.36 µm	1
M2 (NMOS)	153.8 µm	0.36 µm	1
M3 (NMOS Varactor)	23.3 µm	0.36 µm	60
M4 (NMOS Varactor)	23.3 µm	0.36 µm	60

TABLE II: Testbench Setup for VCO Simulation.

Parameter	Value
Supply Voltage (V_{DD})	1.5 V
Control Voltage ($V_{control}$)	0.6 V
Bias Current (I_{bias})	1.5 mA
Inductance (L1, L2)	1 nH

A. Transient Analysis

The simulation results confirm that the VCO achieves an oscillation frequency of **2.4 GHz** at a control voltage of **0.6 V**. This meets the design specifications and demonstrates the accuracy of the proposed design.

The individual node voltages, v_{out1} and v_{out2}, were also recorded during transient analysis. The waveforms, shown in Figure 5, illustrate the sinusoidal behavior of the outputs, with the expected phase difference between the two nodes. These results corroborate the differential operation of the VCO.

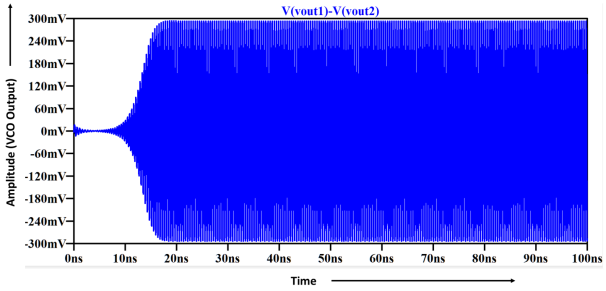

Fig. 4: Differential Output Waveform ($v_{out1} - v_{out2}$) of VCO at 2.4 GHz.

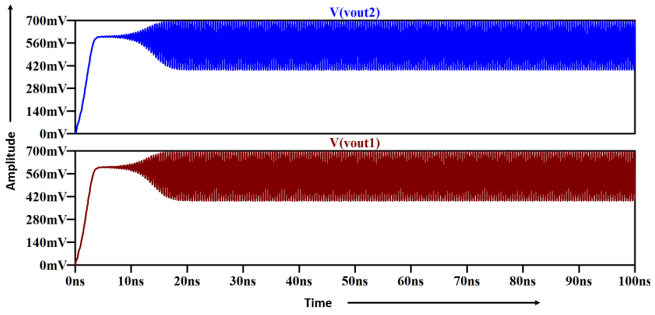

Fig. 5: Individual Node Waveforms (v_{out1} and v_{out2}).

B. Frequency vs. Control Voltage Analysis

A sweep of control voltage was performed to evaluate the VCO's tuning range. The frequency of oscillation was plotted against the control voltage, as shown in Figure 6. Using the slope of this graph, the gain of the VCO (K_{VCO}) was calculated to be :

$$K_{VCO} = 117\,\text{MHz/V}.$$

This value indicates the sensitivity of the VCO frequency to changes in control voltage and aligns with the design requirements.

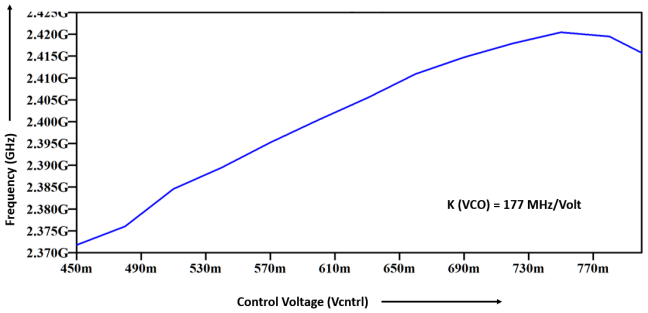

Fig. 6: Frequency vs. Control Voltage graph

V. Differential to Digital Pulse Conversion

A. Design Overview

The objective of this design is to convert the differential sinusoidal output of the VCO into a single-ended sinusoidal waveform and then further into a digital clock pulse at a frequency of 2.4 GHz. The process involves the following stages [7]:

- **Amplifier Design:**
  - Converts the differential output of the VCO (sinusoidal) into a single-ended output.
  - Boosts the peak-to-peak voltage of the sinusoidal signal to ensure compatibility with the inverters.
- **Inverters:**
  - Converts the single-ended sinusoidal signal into a digital clock pulse.
  - Generates a clean 2.4 GHz digital signal to serve as the input for the next block in the PLL system (the Divider Circuit).

B. Schematic & Transistor Dimensions

The complete schematic of the circuit used to convert the differential output of the VCO to a digital clock pulse is shown in Figure 7. It has LC VCO, the differential amplifier and inverters. The output of LC VCO is being fed into the amplifiers inputs and furthermore the amplifiers output is given to the inverters and the final output is "clk". The dimensions of the MOS transistors used in the amplifier and inverter circuits are summarized in Table III.

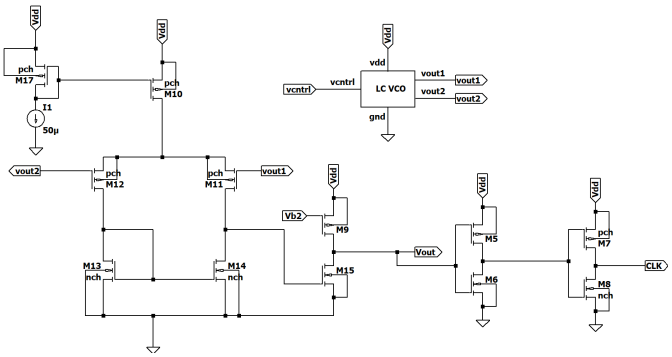

Fig. 7: Schematic of VCO Output Conversion to 2.4 GHz Digital Clock Using Amplifier and Inverters.

TABLE III: Dimensions of MOS Transistors in Amplifier and Inverter.

Transistor	Width (W)	Length (L)
M10 (PMOS)	408.5 µm	0.18 µm
M12 (PMOS)	150 µm	0.18 µm
M11 (PMOS)	150 µm	0.18 µm
M13 (NMOS)	80 µm	0.18 µm
M12 (NMOS)	80 µm	0.18 µm
M9 (PMOS)	430 µm	0.18 µm
M15 (NMOS)	380 µm	0.18 µm
M5 (PMOS)	3.5 µm	0.18 µm
M6 (NMOS)	1 µm	0.18 µm
M7 (PMOS)	0.7 µm	0.18 µm
M8 (NMOS)	0.2 µm	0.18 µm

C. Simulation Results

- **Amplifier Output:** The differential output from the VCO was successfully converted into a single-ended sinusoidal signal with increased peak-to-peak voltage.
- **Digital Pulse Output:** Using the inverters, the amplified single-ended signal was transformed into a digital pulse at a frequency of 2.4 GHz. This pulse serves as the clock signal for the Divider Circuit.

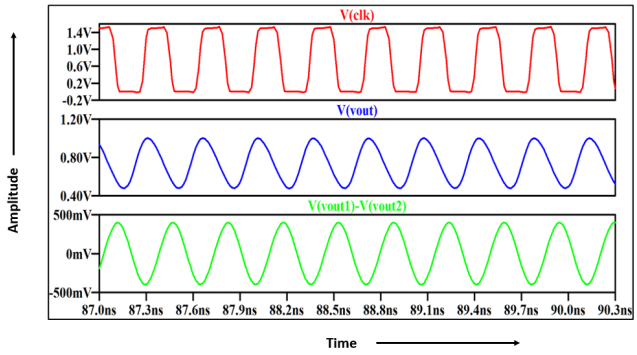

Fig. 8: Final Output Waveforms: Digital Clk of 2.4GHz

VI. Conclusion

In this report, we have presented the design and simulation of a Voltage-Controlled Oscillator (VCO) as a critical component for a Phase-Locked Loop (PLL) system, with a target frequency of 2.4 GHz. The design utilized NMOS transistors, with varactors incorporated to achieve the desired frequency modulation based on the control voltage. The simulation results, obtained through transient analysis in LTspice, confirmed that the VCO successfully generates a stable oscillation at 2.4 GHz when the control voltage is set to 0.6 V. The frequency response of the VCO was observed to be linear, indicating good frequency tuning characteristics, which is essential for PLL applications where frequency control is paramount.

Furthermore, to interface the VCO output with the subsequent PLL blocks, we developed a system to convert the differential sinusoidal output of the VCO to a single-ended sinusoidal signal. This was achieved using a differential amplifier. The single-ended signal was then fed into a chain of inverters to generate a digital clock signal at 2.4 GHz. The resulting digital pulse exhibited a stable frequency, suitable for feeding into the next stage of the PLL system, i.e., the frequency divider.

The primary goal of this work was to design a VCO and generate a 2.4 GHz digital clock. With the VCO design verified and the digital clock successfully generated, the system is now ready for further integration into the PLL system. The next phase of this project will involve incorporating other PLL components, such as the phase detector, loop filter, and frequency divider, to achieve phase-locking functionality and to demonstrate the full PLL system operation. The ability to precisely control the output frequency through the VCO's control voltage makes this design a promising candidate for high-performance PLL systems, particularly in communication and signal processing applications where frequency stability and accuracy are crucial.

References

[1] S. Hokrani, T. Thanuja, and K. Kumaraswamy, "Design and implementation of phase locked loop on 180nm technology node," in *2018 4th International Conference for Convergence in Technology (I2CT)*. IEEE, 2018, pp. 1–6.

[2] P. Kumar, A. Khele, and A. C. Joshi, "Design of phase locked loop in 180 nm technology," *arXiv preprint arXiv:2406.13462*, 2024.

[3] B. Razavi, *Design of Analog CMOS Integrated Circuits*, ser. Electrical Engineering Series. McGraw-Hill, 2001. [Online]. Available: https://books.google.co.in/books?id=hdavQgAACAAJ

[4] J. S. Hamel and R. Norris, "Lc tank voltage controlled oscillator tutorial," Presented to the UW ASIC Analog Group, Waterloo, Ontario, Canada, 2005, edited by Ryan Norris. [Online]. Available: https://www.academia.edu/26763368/LC_Tank_Voltage_Controlled_Oscillator_Tutorial

[5] K. Narasimhamurthy, "Design of voltage controlled oscillator for 2.4 ghz wireless applications," *International Journal of Computer Applications*, vol. 975, p. 8887, 2015.

[6] B.-H. Lee, Y.-Y. Lin, and T.-H. Huang, "2.4 ghz wide-tuning vco using switchable imos-based varactor in 180-nm cmos," in *2021 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*. IEEE, 2021, pp. 1–3.

[7] M. Nasrollahpour, C. Yen, and S. Hamedi-hagh, "Low-power and high-frequency symmetry load ring-vco for bluetooth application,," 09 2017.