Department of Electronics Engineering, AMU

Problem Presentation of UG Project

Design of Phase-Locked Loop (PLL)

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Project Details

Project Title: Design of Phase-Locked Loop (PLL)

Project Guide: Prof. Naushad Alam

Nature of the Project : Design & Simulation

- **Tools Required:** LT Spice & Cadence Virtuoso

- **Technology Node:** CMOS 180nm

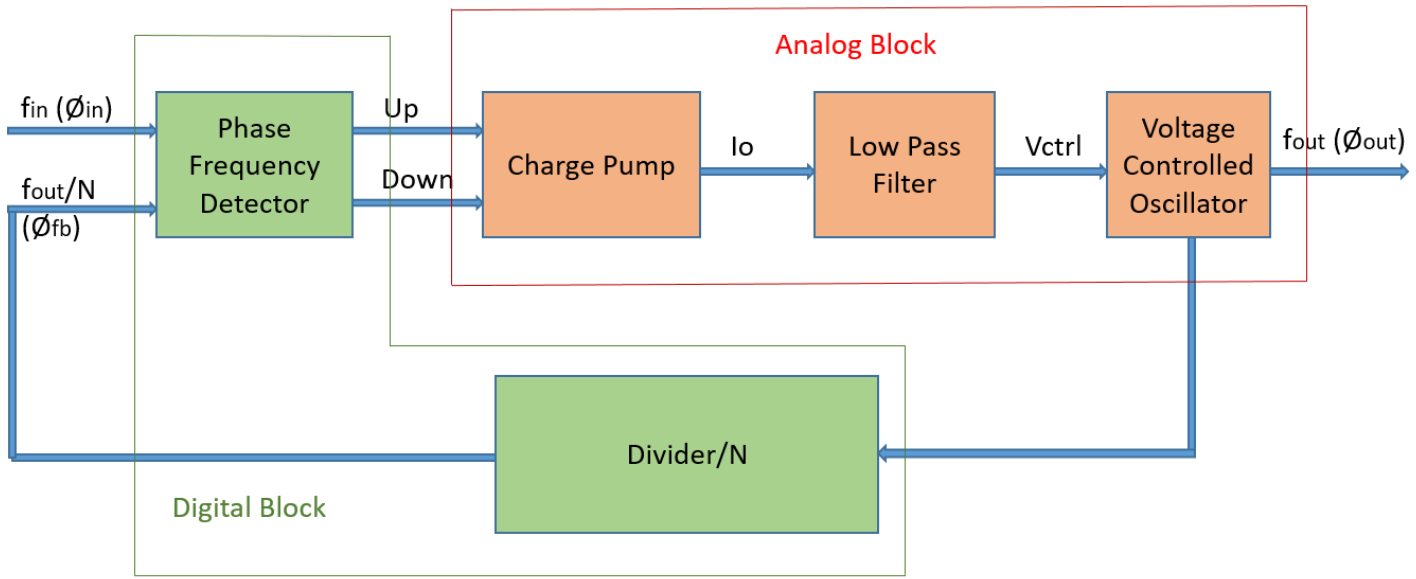
Abstract

This project involves designing a Phase-Locked Loop (PLL) for a 2.4 GHz frequency, targeting applications in wireless communication systems such as Wi-Fi and Bluetooth.

The project emphasizes creating a reliable PLL that ensures consistent frequency generation, crucial for minimizing signal distortion and improving overall system performance.

Introduction to PLL

- The Phase-Locked Loop (PLL) is a feedback system that creates a frequency from a Voltage Controlled Oscillator (VCO) that is synchronous to the input signal.
- It is a Mixed block which uses a Phase Frequency Detector (PFD) and Divide by N network as Digital Block and Charge Pump (CP), Low Pass Filter and Voltage Control Oscillator as Analog Block.

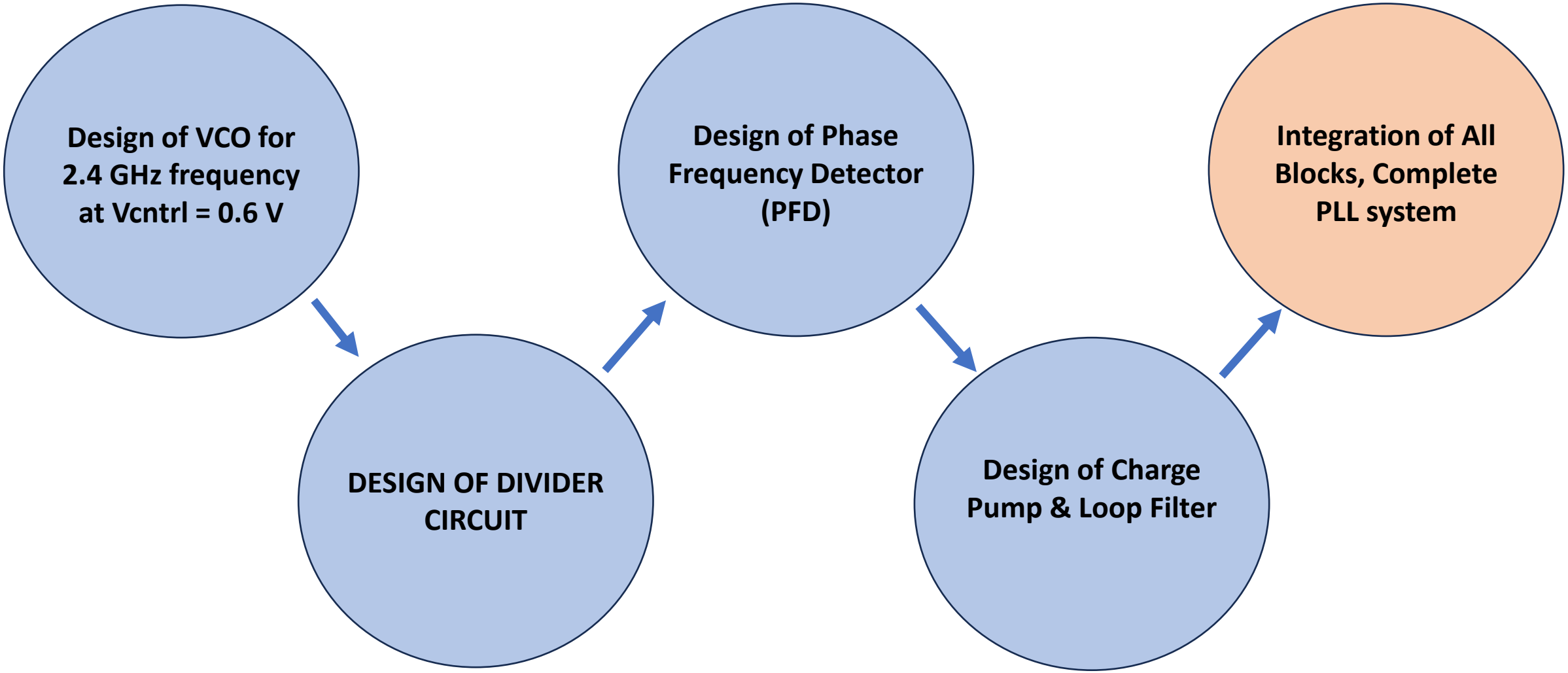


Block Diagram of Phase-Locked Loop

Overview of PLL Blocks

VOLTAGE CONTROLLED OSCILLATOR (VCO)	DIVIDER	PHASE FREQUENCY DETECTOR	CHARGE PUMP & Loop Filter
Generates an oscillating signal whose frequency is variable based on a control voltage.	It is used to scale down the frequency from the output of a Voltage Controlled Oscillator	It compares the reference frequency signal with the signal feedback from output of VCO , generates an output based on phase difference between them.	This combination averages out the voltage given out of the PFD, thus creating the control voltage for VCO.

Project Objectives & Deliverables



Gantt Chart

TASKS	AUGUST	SEPTEMBER	OCTOBER	NOVEMBER	JANUARY	FEBRUARY	MARCH	APRIL
LITERATURE SURVEY	⟷							
DESIGN OF VCO		⟷						
DESIGN OF DIVIDER			⟷					
DESIGN OF PFD, CHARGE PUMP & LPF				⟷	⟷			
COMPLETE PLL DESIGN						⟷	⟷	
REPORT WRITING							⟷	⟷

References

[1]. Santiago, David (2021). ECG 721 – MEMORY CIRCUIT DESIGN, FALL 2021: Design of Analog Phase-Locked Loops (A tutorial).

[2]. Phase Locked Loop - Tutorial. (n.d.). www.electronics-notes.com. https://www.electronics-notes.com/articles/radio/pll-phase-locked-loop/tutorial-primer-basics.php

[3]. S. R. Abdul Rahman, S. H. Md Ali, N. Kamal, A. A. Ahmad and M. Othman, "Design of 2.4 GHz CMOS LC Tank Voltage Controlled Oscillator (VCO) for PLL using 0.18 µm CMOS Technology," 2018 IEEE International Conference on Semiconductor Electronics (ICSE), Kuala Lumpur, Malaysia, 2018.

[4]. Razavi, B. (2020). Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level. Cambridge: Cambridge University Press.