DESIGN OF PHASE LOCKED LOOP (PLL)

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Poster presentation of the course: ELC4980

Summary

This project aims to design a Phase-Locked Loop (PLL) in LTSpice, utilizing a 180 nm technology node at supply voltage Vdd = 1.5V. The PLL is designed to operate at a frequency of 2.4 GHz. The architecture comprises a Phase Frequency Detector (PFD), Charge Pump (CP), Low Pass Filter (LPF), and an LC-based Voltage-Controlled Oscillator (LC-VCO).

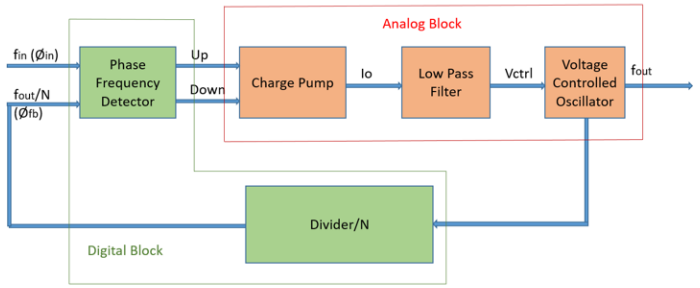


Fig. 1 : Block Diagram of Phase-Locked Loop

Description and Methods

DESIGN PRINCIPLE OF VCO:

The LC VCO design is based on two key principles: negative conductance cancellation to sustain oscillations and zero phase shift to ensure stable, aligned oscillations. The design uses two cross coupled NMOS transistor for negative resistance and an LC tank circuit with a variable capacitor (MOS varactors) to set and tune the oscillation frequency.

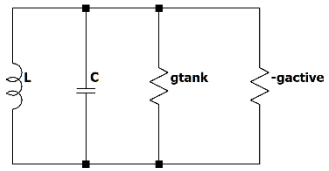


Fig.2: LC Tank Circuit

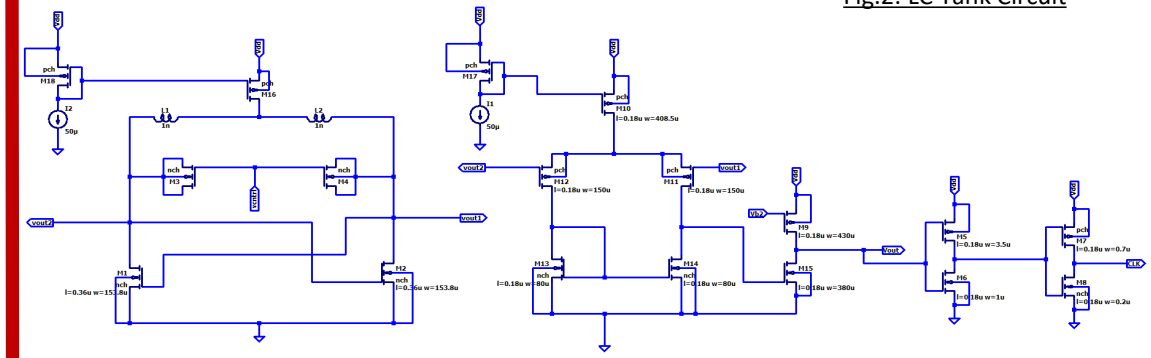
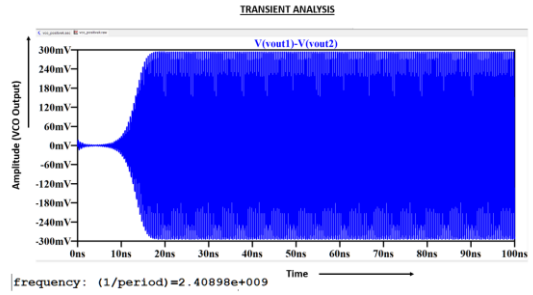
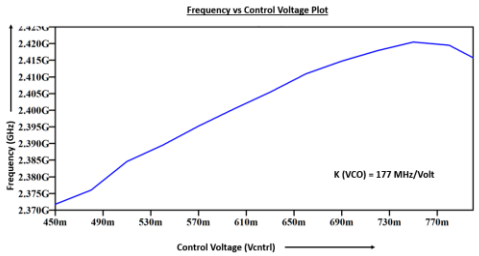
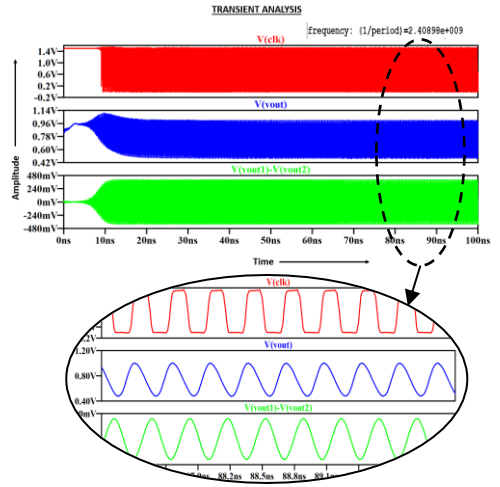


Fig.3: Schematic of NMOS LC VCO with MOS varactors and VCO Output Conversion to 2.4 GHz Digital Clock Using Amplifier and Inverters.

Results







Motivation

The motivation for designing this PLL lies in addressing the growing demand for high-frequency, low-jitter clock generation in wireless communication systems. With its operation at 2.4 GHz, this PLL design aligns with standard frequency bands like Bluetooth and Wi-Fi, enabling efficient and stable performance in modern electronics.

Conclusion

The designed VCO achieves stable 2.4 GHz oscillation at a control voltage of 0.6 V, and gain of the VCO (KVCO) is obtained to be 117 MHz/V and linear frequency tuning verified through LTspice simulations. The differential output is successfully converted to a single-ended sinusoidal signal with increased peak-to-peak voltage, which is further transformed into a 2.4 GHz digital pulse using inverters. This digital clock signal is optimized for driving the frequency divider, ensuring compatibility with the PLL system for reliable operation.

Key References

1. S. Hokrani, T. Thanuja, and K. Kumaraswamy, "Design and implementation of phase locked loop on 180nm technology node," in 2018 4th International Conference for Convergence in Technology (I2CT). IEEE, 2018, pp. 1–6.