Department of Electronics Engineering, AMU

Presentation of UG Project

Design of Phase-Locked Loop (PLL)

Project Guide: Prof. Naushad Alam

Name of student 1: Afzal Malik | Faculty No.: 21ELB173 | Enrolment No.: GM6541

Name of student 2: Mohammed Musayyeb Sherwani | Faculty No.: 21ELB283 | Enrolment No.: GK6347

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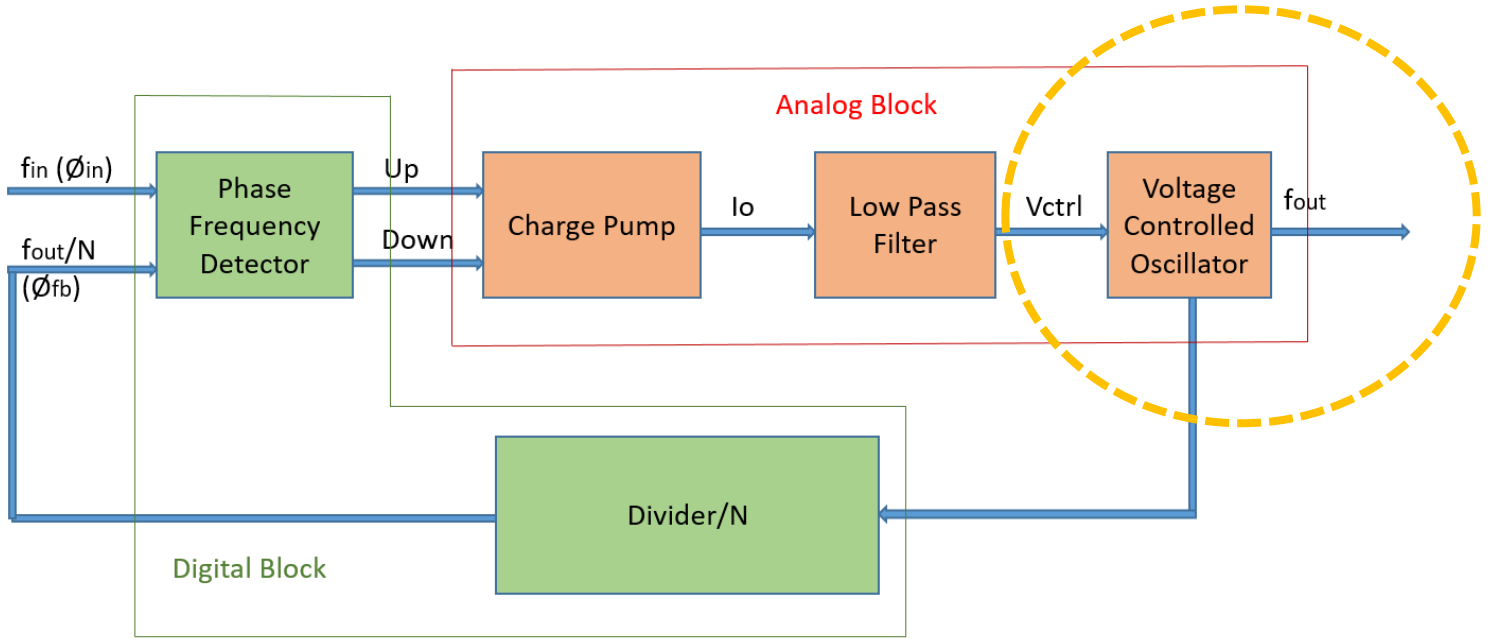
Design of PLL

- **Technology Node :** 180nm | **Tools Used :** LT Spice
- The Phase-Locked Loop (PLL) is a feedback system that creates a frequency from a Voltage Controlled Oscillator (VCO) that is synchronous to the input signal.
- It is a Mixed block which uses a Phase Frequency Detector (PFD) and Divide by N network as Digital Block and Charge Pump (CP), Low Pass Filter and Voltage Control Oscillator as Analog Block.



Block Diagram of Phase-Locked Loop

Design of Voltage Controlled Oscillator (VCO)

- Generates an oscillating signal whose frequency is variable based on a control voltage.

VCO Type	Pros	Cons
Ring Oscillator	Simple design, small area, high tuning range	Higher phase noise, lower frequency stability
LC Oscillator (LC VCO)	Stable at high frequencies, Lower phase noise	Larger area, complex design

Selected Topology	Reasons
NMOS LC VCO with MOS Varactors	1. Stable frequency at 2.4 GHz 2. Low phase noise for clean signal 3. Efficient power use at high frequencies

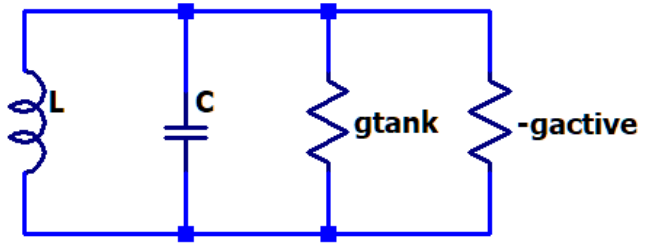
Design of LC VCO for 2.4 GHz frequency at Vcntrl = 0.6 V

Voltage Controlled Oscillator Analysis and Design

Oscillations can occur when:

i) the negative conductance of the active network cancels out the positive conductance (loss) of the tank

ii) the closed loop gain has zero phase shift



Design Calculations of NMOS LC VCO with MOS Varactors [2]

Assume L = 1nH, using Q (Quality Factor) = $\frac{L\,\omega}{R}$, Taking Q = 10

R (Series Resistance) = 1.5 ohms

Now, ω = $\frac{1}{\sqrt{LC}}\sqrt{1-\frac{R^2C}{L}}$

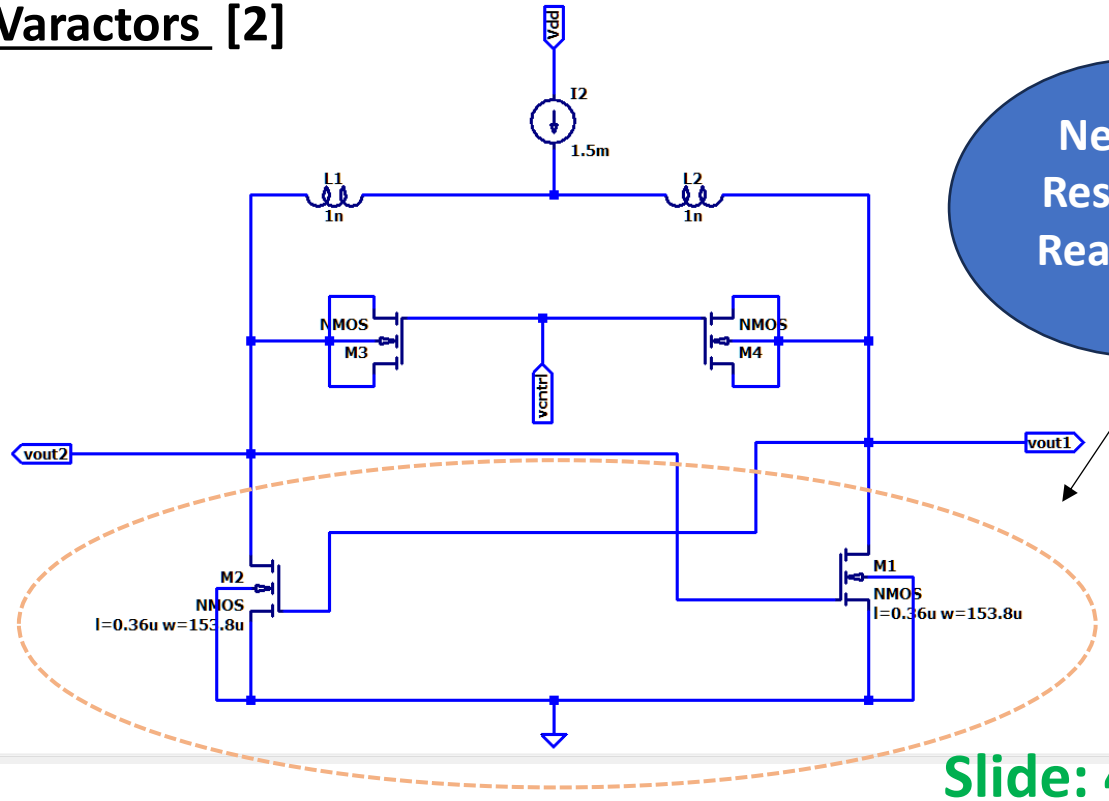
C=4.3 pF $(For\ getting\ f$=2.4$Ghz\ at\ Vcntrl$=0.6$V)$

Gm = $\frac{aRC}{L}$, Taking $\alpha = 1, gm > 6.45\ mS$ (Taken gm = 10mS)

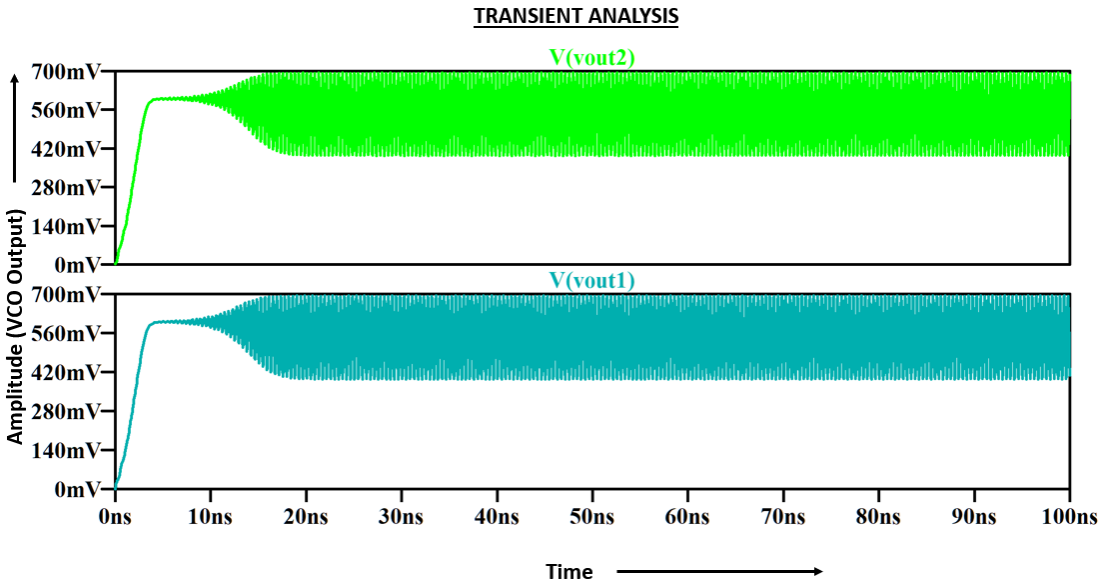
Gm =$\frac{2\ Id}{Vov}$, $Id = 750\ uA$, $Then, using\ sweep\ technique$

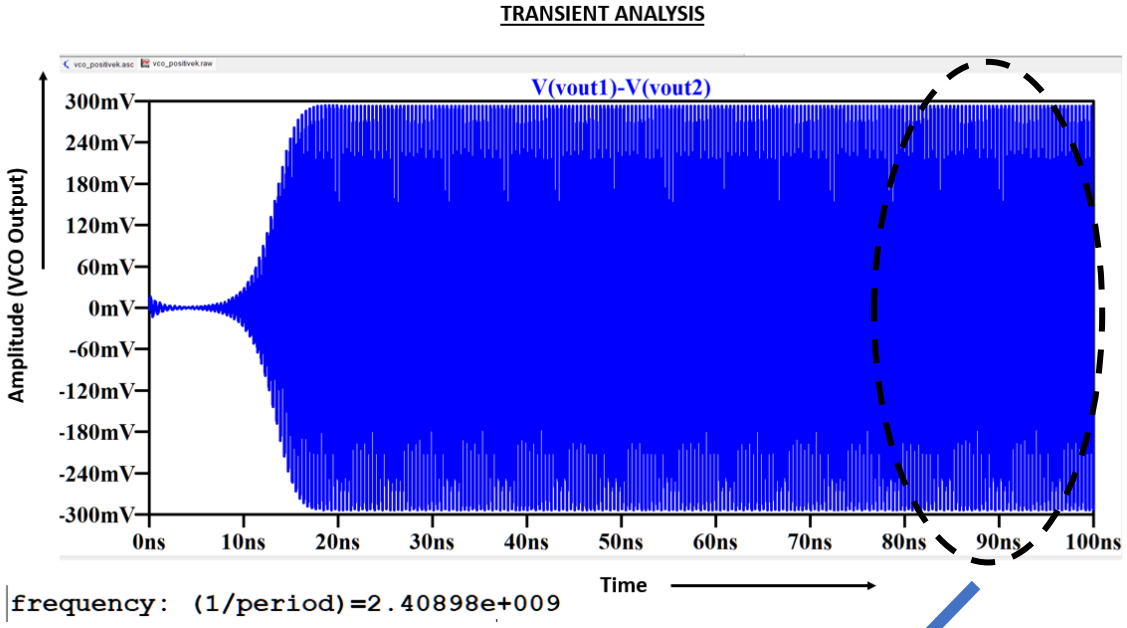
Transistor sizing is done, Length = 0.36u and Width = 153.8u

Then, the capacitors are realized using MOS Varactors.

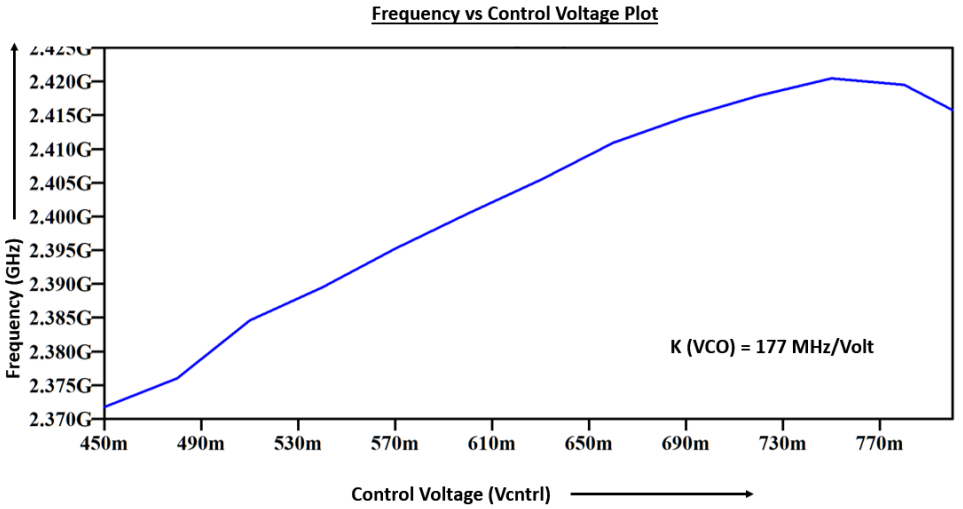


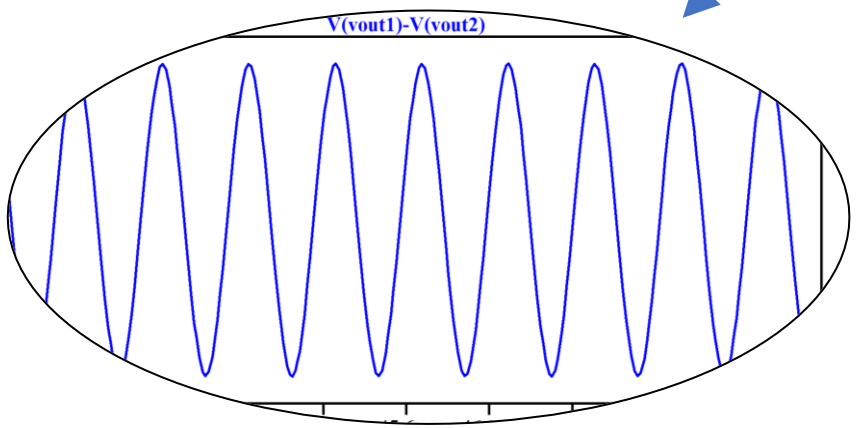
VCO RESULTS:





frequency: (1/period)=2.40898e+009





GOAL: DIGITAL PULSE (CLK) OF 2.4 GHZ:

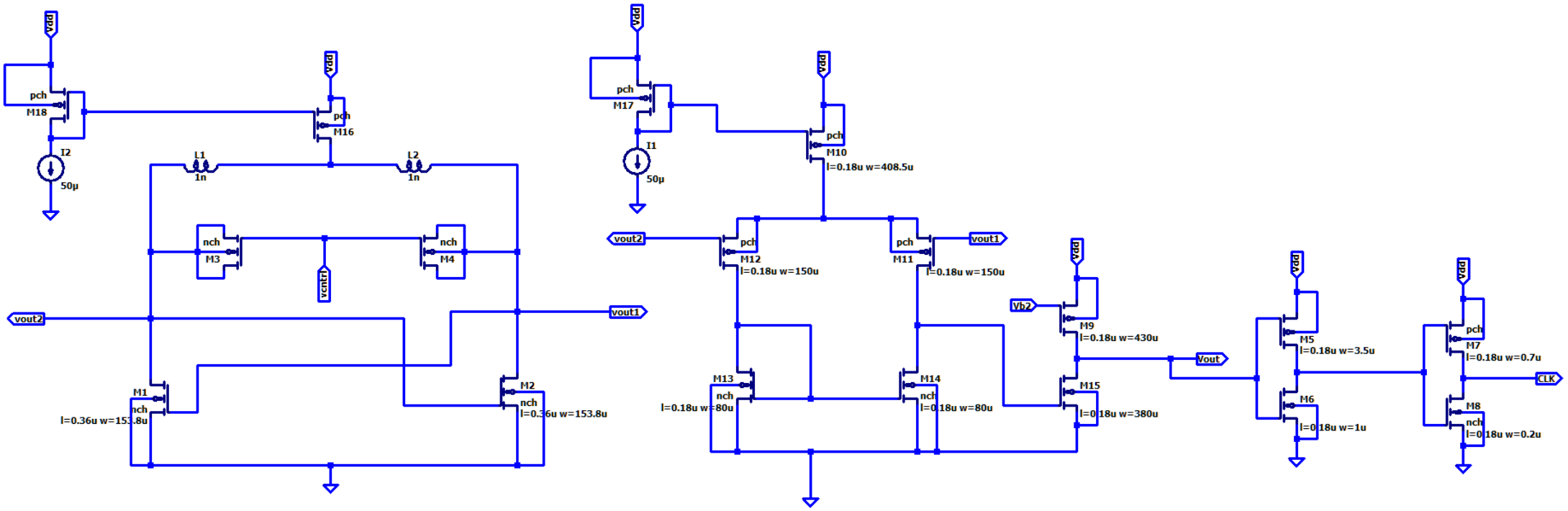
Design of Amplifier :

- To convert the Differential output of VCO (Sinusoidal) to Single ended Output (Sinusoidal) of 2.4GHz frequency .

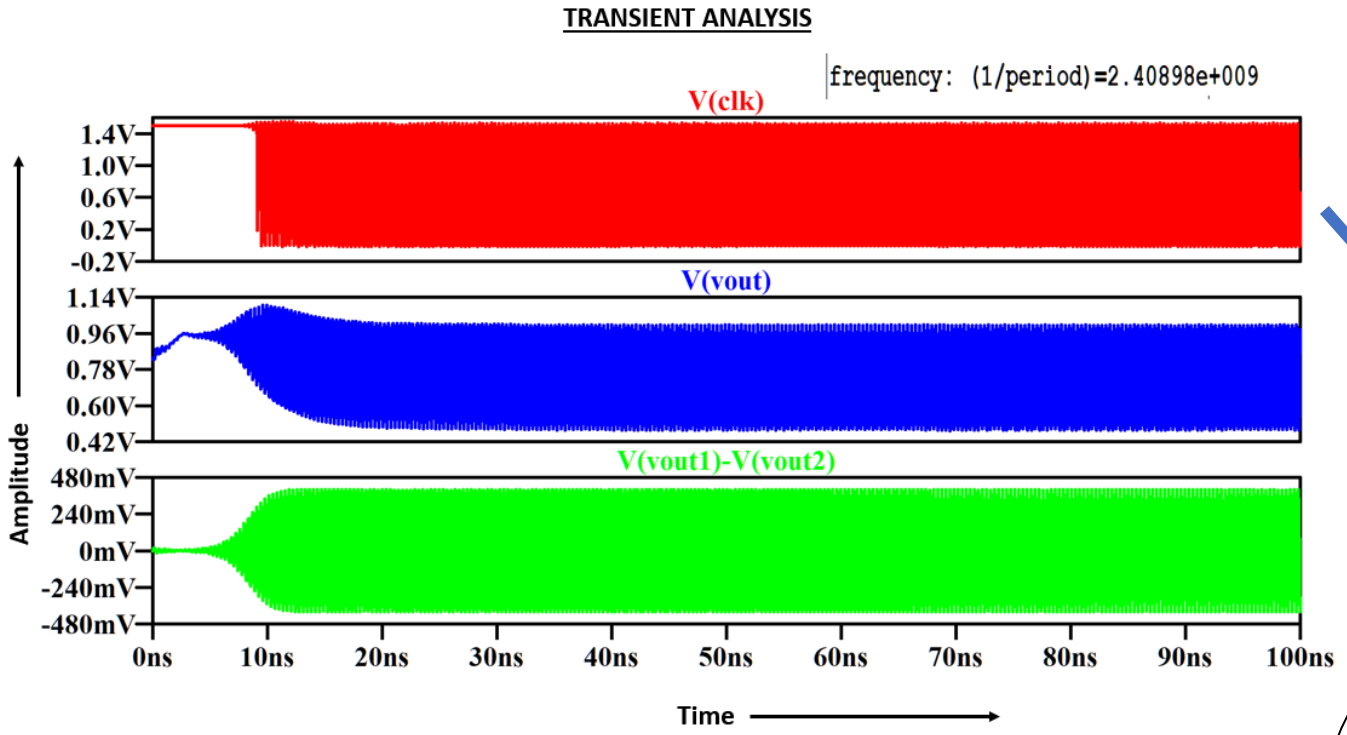
- To increase the peak to peak Voltage (To drive the Inverters)

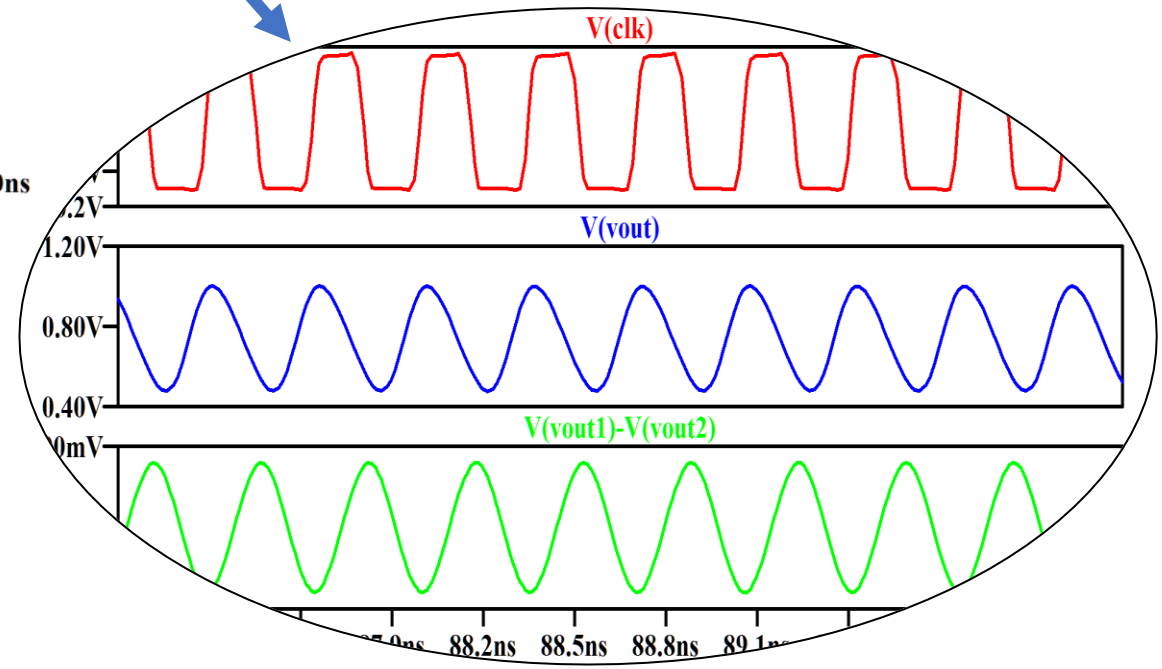
Inverters:

- To convert the VCO single ended output (Sinusoidal) to Digital Pulse (CLK) of 2.4 GHZ , In order to give it as Input to the Next Circuit Block " DIVIDER CIRCUIT".

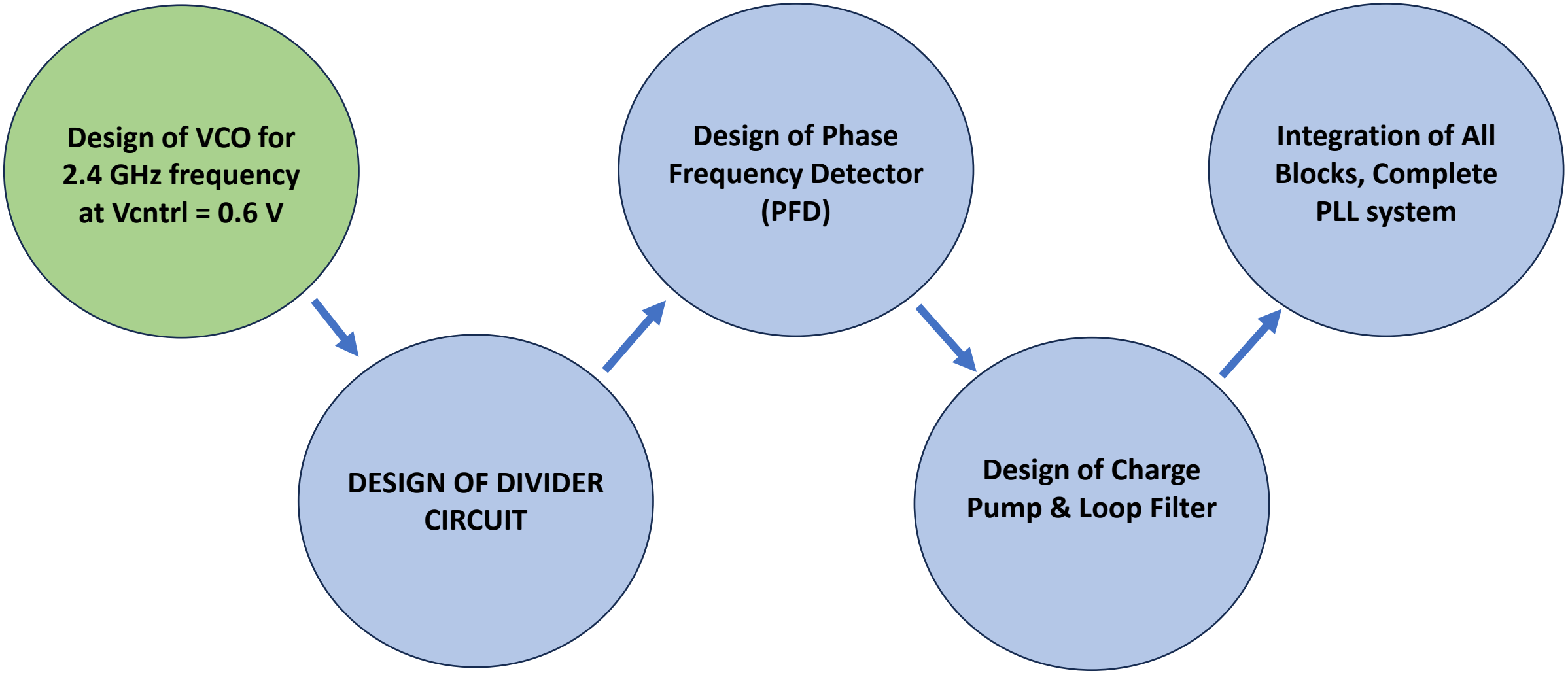


SIMULATION RESULTS:





FUTURE WORK:


Design of VCO for 2.4 GHz frequency at Vcntrl = 0.6 V
DESIGN OF DIVIDER CIRCUIT
Design of Phase Frequency Detector (PFD)
Design of Charge Pump & Loop Filter
Integration of All Blocks, Complete PLL system

References

[1]. Santiago, David (2021). ECG 721 – MEMORY CIRCUIT DESIGN, FALL 2021: Design of Analog Phase-Locked Loops (A tutorial).

[2]. LC Tank Voltage Controlled Oscillator tutorial. UW ASIC Analog Group, Waterloo, Ontario, Canada, 2005. https://www.academia.edu/26763368/LC_Tank_Voltage_Controlled_Oscillator_Tutorial

[3]. C. -H. Yen, M. Nasrollahpour and S. Hamedi-Hagh, "Low-power and high-frequency ring oscillator design in 65nm CMOS technology," 2017 IEEE 12th International Conference on ASIC (ASICON), Guiyang, China, 2017, pp. 533-536, doi: 10.1109/ASICON.2017.8252530.

[4]. Razavi, B. (2020). Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level. Cambridge: Cambridge University Press.