Final Year Project Report

Design of Phase Locked Loop (PLL)

Project Report

*s*ubmitted in partial fulfillment of the

*r*equirements for the award of

BACHELOR OF TECHNOLOGY

Submitted by

Afzal Malik - 21ELB173
Mohammed Musayyeb Sherwani - 21ELB283

Under the guidance of

Prof. Naushad Alam

Department of Electronics Engineering
Zakir Husain College of Engineering & Technology
Aligarh Muslim University
Aligarh, India-202002

May 2025

Design of Phase Locked Loop (PLL)

Candidate's Declaration

We hereby declare that our work submitted in the partial fulfillment of the requirements for the award of the degree of **Bachelor of Technology** in the Department of Electronics Engineering of the Aligarh Muslim University, titled as **"Design Of Phase Locked Loop"** is a record of our work carried out during the **VII Semester** from August 2024 to December 2024 and **VIII Semester** from January 2025 to May 2025 under the guidance of **Prof. Naushad Alam** , Professor, Department of Electronics Engineering, AMU.

The matter presented in this report has not been submitted by us for the award of any other degree of this or any other Institute/University.

We have also received a plagiarism report from MA Library and submitted it to our guide, where the similarity index is **12** percent.

Afzal Malik - 21ELB173

Mohammed Musayyeb Sherwani - 21ELB283

This is to certify that the above statement made by the candidates is true to the best of my knowledge and belief.

Prof. Naushad Alam
Supervisor

Date: April 28, 2025

Acknowledgement

We would like to start by expressing our sincerest gratitude to our Project supervisor **Prof. Naushad Alam**, Professor, Department of Electronics Engineering at the Aligarh Muslim University, for his expertise, guidance, and enthusiastic involvement during our coursework.

We are highly obliged to faculty members of the Electronics Engineering Department because without their valuable insights and constructive opinions during evaluations, our project would not have yielded the significant results and led us to explore a myriad of use cases that we have put forward in this report.

We express our special thanks to our parents for their encouragement, constant moral Support, and to our friends and colleagues for being inquisitive and supportive during the course of this project.

Afzal Malik - 21ELB173
Mohammed Musayyeb Sherwani - 21ELB283

Abstract

This project presents the design of a low-power Phase-Locked Loop (PLL) targeting a 2.4GHz output frequency for wireless communication applications such as Wi-Fi and Bluetooth. Operating in the ISM band and designed using 180nm CMOS technology with a supply voltage of 1.5 V, the PLL utilizes a 100MHz input reference clock and achieves frequency synthesis through a divide-by-24 architecture. LTspice is used as the primary design and simulation platform, enabling transistor-level verification of each sub-block and the complete feedback loop. The performance is evaluated through simulations and measurements, which demonstrate its ability to track and lock onto the input frequency.

The architecture comprises a Phase Frequency Detector (PFD), Charge Pump, Loop Filter, Voltage-Controlled Oscillator (VCO), and Frequency Divider. The VCO is tuned to 2.4GHz at a control voltage of 0.6V. The system is simulated using LTspice to validate performance metrics such as loop bandwidth, and power consumption. The final design demonstrates stable locking behavior with a power dissipation of 6.36 mW, making it suitable for integration into low-power RF systems.

This project's contributions are twofold.:

1. Design of a 2.4GHz Phase-Locked Loop optimized for ISM band communication using 180nm CMOS process.
2. Complete transistor-level implementation and verification using LTspice, achieving 6.36 mW power dissipation with successful loop locking.

Keywords

Phase-Locked Loop, Frequency Synthesizer, ISM Band, Voltage-Controlled Oscillator, CMOS 180nm, Charge Pump, LTspice, Low Power Design, Wireless Communication

---

Table of Contents

List of Figures

List of Tables

Introduction

1.1 Background and Motivation

In modern electronic systems, precise frequency generation and synchronization are fundamental requirements, particularly in wireless communication devices such as Wi-Fi routers, Bluetooth modules, GPS receivers, and mobile radios it is an important part of every System on Chip (SoC) because it is the main circuit used to create the system clock [1]. A Phase-Locked Loop (PLL) is a feedback control system that locks the output phase and frequency to a reference signal, ensuring stability and minimal jitter. Its ability to synthesize high-frequency signals from a low-frequency reference makes it indispensable in RF and mixed-signal integrated circuits [2].

As the demand for high-performance yet low-power RF transceivers continues to grow, especially within the Industrial, Scientific, and Medical (ISM) band (2.4–2.5 GHz), there is a pressing need to design compact and energy-efficient PLLs using scalable CMOS processes [1]. This project focuses on the design of a complete PLL system operating at 2.4GHz using the 180nm technology node and simulated using LTspice.

1.2 Applications of PLL

PLLs are key components in:

- Wireless transceivers (Wi-Fi, Bluetooth, ZigBee)
- Clock generation and recovery circuits
- Frequency synthesizers in RF systems
- Digital communication systems
- Signal modulation and demodulation schemes

Their ability to maintain frequency stability, suppress phase noise, and adapt to varying control voltages makes them ideal for high-speed, high-fidelity communication systems [1].

1.3 Overview of PLL Architecture

A typical PLL consists of the following sub-blocks:

- **Phase Frequency Detector (PFD):** Compares the input reference signal with the feedback signal from the divider and generates UP/DN signals based on the phase and frequency difference.
- **Charge Pump (CP):** Converts the digital output of the PFD into a current signal.

- **Loop Filter (LF):** Integrates the current from the charge pump into a smooth control voltage.
- **Voltage-Controlled Oscillator (VCO):** Generates an output signal whose frequency is controlled by the loop filter voltage.
- **Frequency Divider:** Scales down the VCO output to match the reference frequency.

1.4 Block Diagram of PLL

The overall structure of the PLL implemented in this project is shown below:

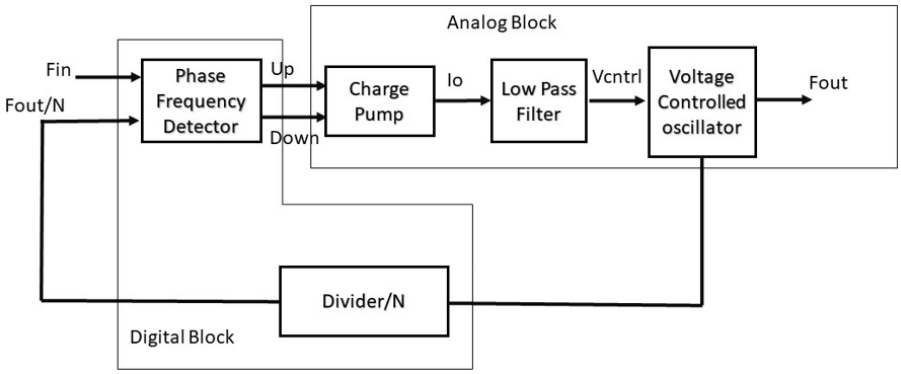

Figure 1.1: Block Diagram of PLL System

1.5 Design Objective

The goal of this project is to design a complete, low-power PLL operating at 2.4GHz using 180nm CMOS technology. The system uses a 100MHz reference frequency and a divide by 24 feedback mechanism. Key performance goals include:

- Achieving phase and frequency lock at 0.6V control voltage
- Simulating all sub-blocks using LTspice and integrating the full loop

1.6 Report Organization

This report is structured as follows:

- **Chapter 2:** Design of the Voltage-Controlled Oscillator (VCO)
- **Chapter 3:** Design of the Frequency Divider
- **Chapter 4:** Design of the Phase Frequency Detector
- **Chapter 5:** Design of the Charge Pump and Loop Filter
- **Chapter 6:** Integration and Simulation Results of the Full PLL
- **Chapter 7:** Conclusion and Future Work

Design of Voltage Controlled Oscillator (VCO)

2.1 Overview of Voltage-Controlled Oscillator (VCO)

A Voltage-Controlled Oscillator (VCO) generates an oscillating signal whose frequency is modulated by a control voltage. It is a critical component in high-frequency circuits such as Phase-Locked Loops (PLLs), frequency synthesizers, and clock recovery systems. The key design objectives of a VCO include achieving stable oscillations, wide tuning range, minimal phase noise, and high power efficiency. These parameters play a vital role in determining the overall performance of a VCO in its target application [2, 3].

2.1.1 Comparison of Ring VCO and LC VCO

Two common topologies for VCO design are the Ring VCO and the LC VCO, each with distinct advantages and trade-offs [4, 3]:

Ring VCO A Ring VCO consists of multiple cascaded inverting stages arranged in a ring configuration. The frequency of oscillation is determined by the propagation delay of each stage.

- **Advantages:**
  - Simple design and smaller chip area.
  - Wide tuning range due to its delay-based operation.
  - Easy integration in digital processes, as it relies on standard CMOS devices.
- **Disadvantages:**
  - Poor phase noise performance, particularly in high-frequency applications, due to the lack of a high-Q resonant structure.
  - Lower frequency stability, making it less suitable for applications demanding precise frequency control.

LC VCO An LC VCO utilizes an LC resonant tank circuit to define the oscillation frequency. This topology achieves oscillations through the interaction of inductance (L) and capacitance (C).

- **Advantages:**
  - Superior phase noise performance due to the high Q-factor of the LC tank circuit.

  - Excellent frequency stability, particularly in GHz-range applications.

- **Disadvantages:**
  - Larger chip area due to the inductor and capacitor.
  - Slightly more complex design and layout compared to Ring VCOs.

2.1.2 Selected Topology (NMOS LC VCO with MOS Varactors):

For this design, the NMOS LC VCO topology was selected due to its superior performance in high-frequency applications like PLLs [4, 5].

Reasons for Selecting LC VCO

- **Frequency Stability:** The LC oscillator's reliance on a high-Q resonant tank ensures frequency stability, especially at 2.4 GHz.
- **Low Phase Noise:** The LC topology inherently suppresses phase noise, producing cleaner signals critical for communication systems.
- **Power Efficiency:** This topology provides high power efficiency in high-frequency circuits, minimizing power consumption.
- **Tuning Capability:** The use of MOS varactors allows fine-tuning of the oscillation frequency over a specified range by varying the control voltage.

Negative Resistance Realization Using Cross-Coupled NMOS Transistors: In an LC VCO, the loss in the resonant tank circuit, primarily caused by the finite Q-factor of the inductor and capacitor, must be compensated to sustain oscillations. This is achieved by generating a negative resistance using a cross-coupled NMOS transistor pair [4].

1. **Concept of Negative Resistance:**
   - The cross-coupled NMOS pair introduces a negative conductance, $-G_m$, that cancels the tank's resistive losses.
   - This ensures that the energy dissipated in the tank is replenished continuously, maintaining sustained oscillations.
2. **Implementation:**
   - Two NMOS transistors are connected in a cross-coupled configuration, with their gates and drains cross-linked.
   - The transistors operate in the saturation region, and their transconductance (G_m) is designed to meet the condition:

$$G_m \geq \frac{1}{R}$$

     where R represents the equivalent resistance of the LC tank circuit.

   The combination of the high-Q LC tank and cross-coupled NMOS negative resistance ensures robust oscillation at the desired frequency with low phase noise and high power efficiency.

2.1.3 Design Principles of LC VCO

The oscillatory behaviour of an LC VCO depends on satisfying two conditions [4]:

(a) **Negative Conductance Cancellation:** The negative conductance introduced by the active device cancels out the positive conductance (loss) of the LC tank circuit as shown in Figure 2.1. This ensures sustained oscillations.

(b) **Zero Phase Shift:** The closed-loop gain of the circuit must exhibit zero phase shift. This criterion ensures phase alignment for oscillation.

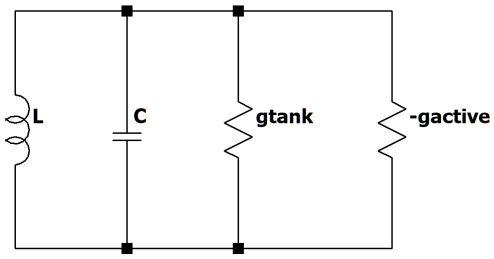

Figure 2.1: Basic LC tank Circuit

To implement this design:

- An NMOS transistor provides the negative resistance required for oscillation.
- The LC tank circuit, consisting of an inductor (L) and a variable capacitor (C), determines the oscillation frequency. The capacitor is implemented using MOS varactors, allowing frequency tuning via the control voltage.

2.1.4 Design Calculations

The design of the LC VCO is based on achieving a target frequency of 2.4 GHz with a control voltage of $V_{\text{ctrl}} = 0.6$ V. The following calculations illustrate the design process:

(a) **Tank Circuit Design:** Assume the following parameters:

- Inductance (L) = 1 nH
- Quality Factor (Q) = 10
- Series Resistance (R) = 1.5 Ω

Using the relationship:

$$Q = \frac{L \cdot \omega}{R}$$

The angular frequency (ω) of the oscillation is determined as:

$$\omega = \frac{1}{\sqrt{L \cdot C}} \cdot \sqrt{1 - \frac{R^2 \cdot C}{L}}$$

To achieve a frequency of $f = 2.4$ GHz:

$$C = 4.3\,\text{pF}$$

(b) **Transconductance (Gm):** The transconductance of the NMOS transistor (G_m) must exceed the tank loss to sustain oscillation:

$$G_m > \frac{\alpha R}{L} C$$

Taking $\alpha = 1$, $G_m > 6.45$ mS. The selected value for G_m is 10 mS.
Using:

$$G_m = \frac{2I_D}{V_{\text{ov}}}$$

For $I_D = 750\,\mu$A, transistor dimensions are obtained:

- Length (L) = $0.36\,\mu$m
- Width (W) = $153.8\,\mu$m

(c) **MOS Varactor Implementation:** The capacitance in the tank circuit is implemented using MOS varactors, providing a tunable range to adjust the frequency as a function of V_{ctrl} [6].

2.2 Schematic and Design Parameters

Figure 2.2 shows the schematic of the designed NMOS LC VCO. It consists of a cross-coupled NMOS transistor pair (M1 and M2) to realize negative resistance and an LC tank circuit with MOS varactors (M3 and M4) for frequency tuning. The schematic also includes the bias current source and supply voltage setup.

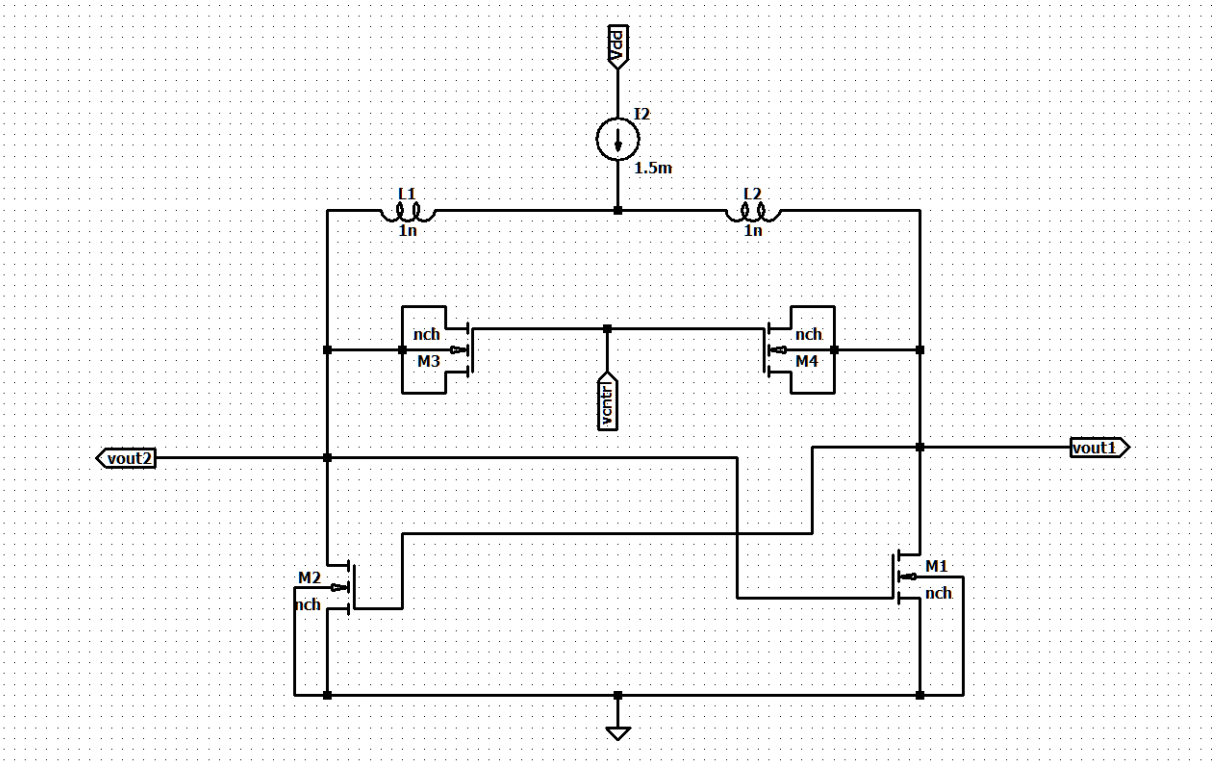

Figure 2.2: Schematic of the NMOS LC VCO with MOS varactors.

The width and length of the MOS transistors used in the design are listed in Table 2.1, and the key testbench conditions are summarized in Table 2.2.

Table 2.1: Dimensions of MOS Transistors in the VCO Design.

Transistor	**Width (W)**	**Length (L)**	**Parallel Devices**
M1 (NMOS)	153.8 µm	0.36 µm	1
M2 (NMOS)	153.8 µm	0.36 µm	1
M3 (NMOS Varactor)	31 µm	0.36 µm	60
M4 (NMOS Varactor)	31 µm	0.36 µm	60

Table 2.2: Testbench Setup for VCO Simulation.

Parameter	**Value**
Supply Voltage (V_{DD})	1.5 V
Control Voltage ($V_{control}$)	0.6 V
Bias Current (I_{bias})	1.5 mA
Inductance (L1, L2)	1 nH

2.3 VCO Simulation Results

To validate the functionality of the designed VCO, transient analysis was performed using LTSpice. The differential output of the VCO, represented as $v_{out1} - v_{out2}$, was analyzed, and the resulting oscillations are depicted in Figure 2.3.

2.3.1 Transient Analysis

The simulation results confirm that the VCO achieves an oscillation frequency of **2.4 GHz** at a control voltage of **0.6 V**. This meets the design specifications and demonstrates the accuracy of the proposed design.

The individual node voltages, v_{out1} and v_{out2}, were also recorded during transient analysis. The waveforms, shown in Figure 2.4, illustrate the sinusoidal behavior of the outputs, with the expected phase difference between the two nodes. These results confirm that the VCO is working in differential mode.

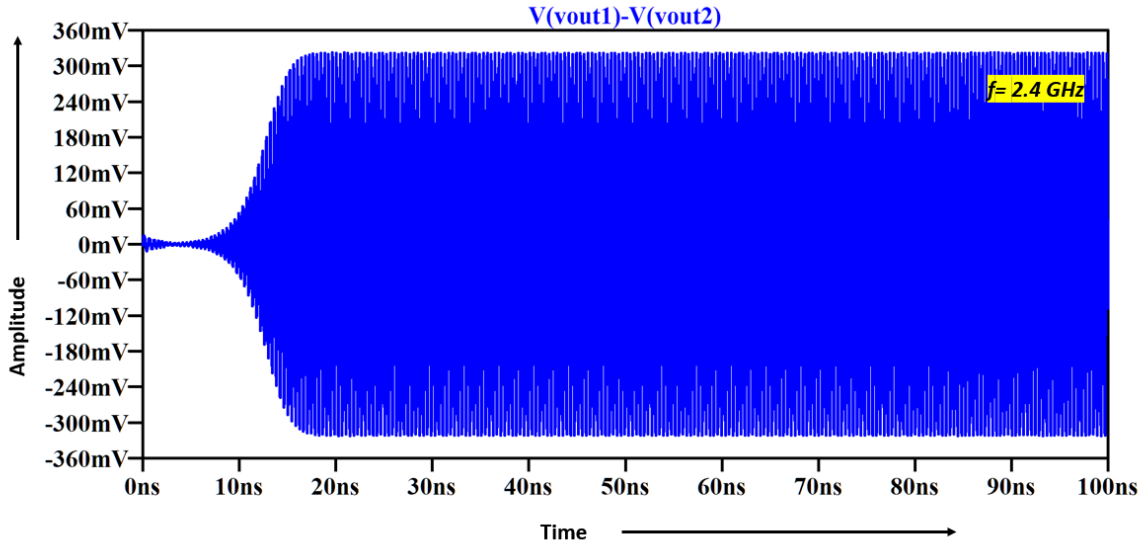

Figure 2.3: Differential Output Waveform ($v_{out1} - v_{out2}$) of VCO at 2.4 GHz.

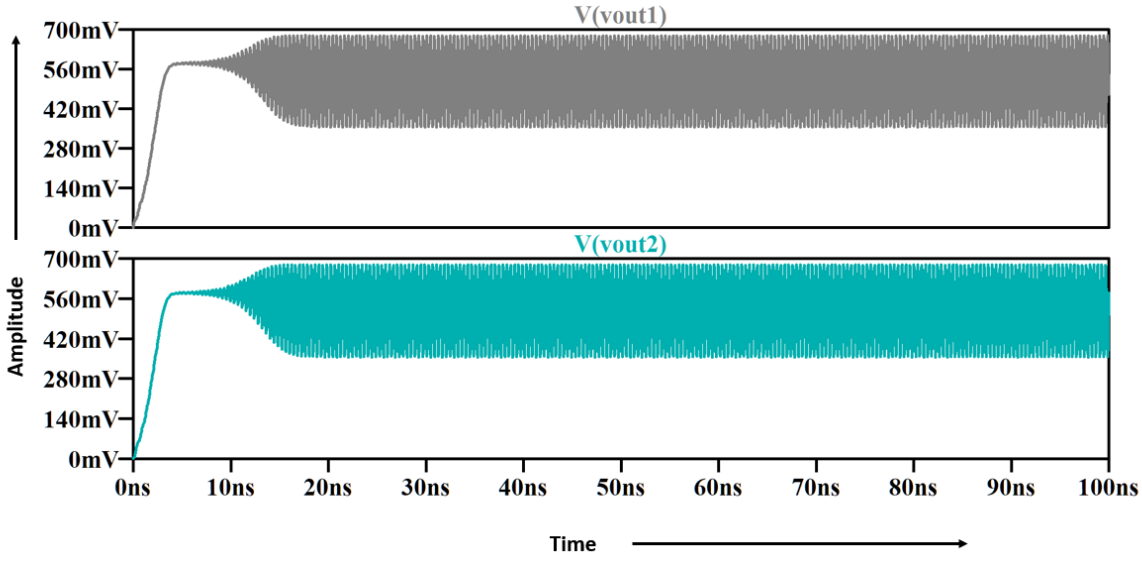

Figure 2.4: Individual Node Waveforms (v_{out1} and v_{out2}).

2.3.2 Frequency vs. Control Voltage Analysis

A sweep of control voltage was performed to evaluate the VCO's tuning range. The frequency of oscillation was plotted against the control voltage, as shown in Figure 2.5. Using the slope of this graph, the gain of the VCO (K_{VCO}) was calculated to be :

$$K_{VCO} = 177\,\text{MHz/V}.$$

This value indicates the sensitivity of the VCO frequency to changes in control voltage and aligns with the design requirements.

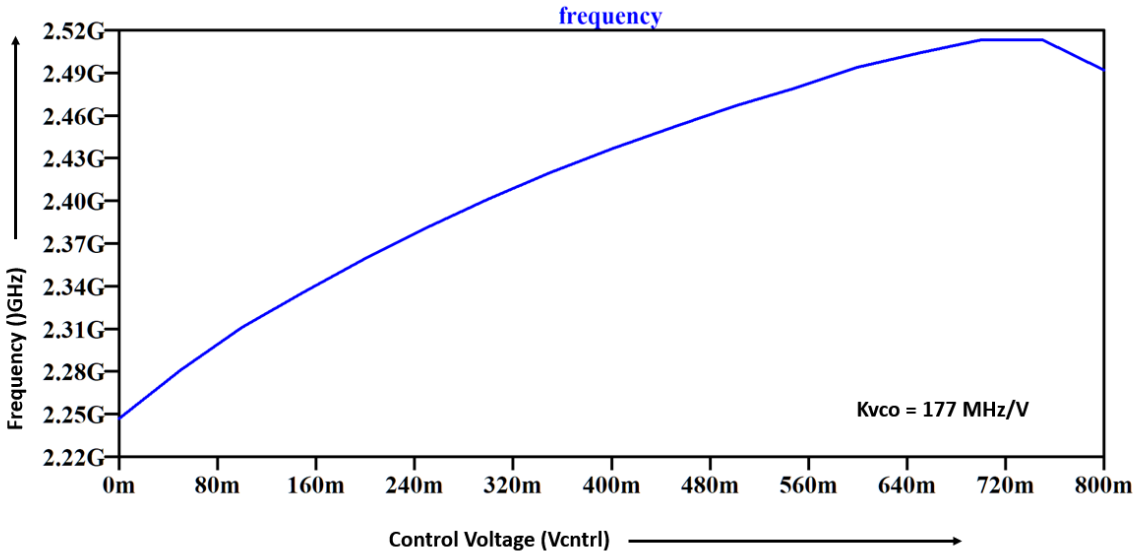

Figure 2.5: Frequency vs. Control Voltage Curve

2.4 Differential to Digital Pulse Conversion

2.4.1 Design Overview

The objective of this design is to convert the differential sinusoidal output of the VCO into a single-ended sinusoidal waveform and then further into a digital clock pulse at a frequency of 2.4 GHz. The process involves the following stages [7]:

- **Amplifier Design:**
  - Converts the differential output of the VCO (sinusoidal) into a single-ended output.
  - Boosts the peak-to-peak voltage of the sinusoidal signal to ensure compatibility with the inverters.
- **Inverters:**
  - Converts the single-ended sinusoidal signal into a digital clock pulse.
  - Generates a clean 2.4 GHz digital signal to serve as the input for the next block in the PLL system (the Divider Circuit).

2.4.2 Schematic & Transistor Dimensions

The complete schematic of the circuit used to convert the differential output of the VCO to a digital clock pulse is shown in Figure 2.6. It has LC VCO, the differential amplifier and inverters. The output of LC VCO is being fed into the amplifiers inputs and furthermore the amplifiers output is given to the inverters and the final output is "clk". The dimensions of the MOS transistors used in the amplifier and inverter circuits are summarized in Table 2.3.

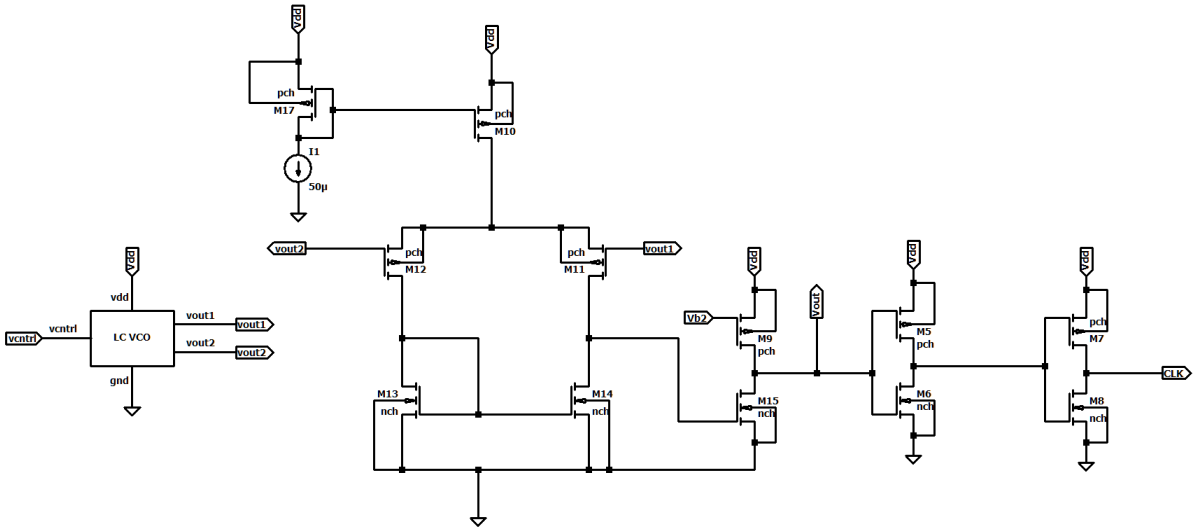

Figure 2.6: Schematic of VCO Output Conversion to 2.4 GHz Digital Clock Using Amplifier and Inverters.

Table 2.3: Dimensions of MOS Transistors in Amplifier and Inverter.

Transistor	**Width (W)**	**Length (L)**
M10 (PMOS)	408.5 µm	0.18 µm
M11 (PMOS)	150 µm	0.18 µm
M12 (PMOS)	150 µm	0.18 µm
M13 (NMOS)	80 µm	0.18 µm
M14 (NMOS)	80 µm	0.18 µm
M9 (PMOS)	41 µm	0.18 µm
M15 (NMOS)	87 µm	0.18 µm
M5 (PMOS)	14 µm	0.18 µm
M6 (NMOS)	3 µm	0.18 µm
M7 (PMOS)	7 µm	0.18 µm
M8 (NMOS)	3.5 µm	0.18 µm

2.4.3 Simulation and Functional Verification

- **Amplifier Output:** The differential output from the VCO was successfully converted into a single-ended sinusoidal signal with increased peak-to-peak voltage.
- **Digital Pulse Output:** Using the inverters, the amplified single-ended signal was transformed into a digital pulse at a frequency of 2.4 GHz as shown in 2.7. This pulse serves as the clock signal for the Divider Circuit.

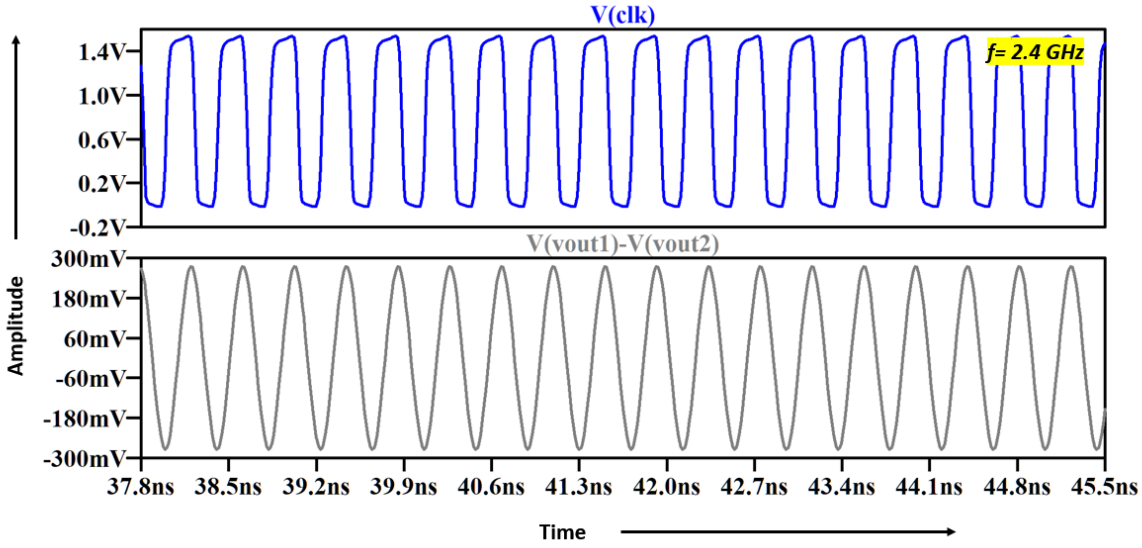

Figure 2.7: Final Output Waveforms: Digital Clk of 2.4GHz

Design of Frequency Divider

3.1 Divider Architecture and Frequency Requirements

The frequency divider is a fundamental component in the feedback path of a Phase-Locked Loop (PLL). Its function is to scale down the high-frequency output of the Voltage-Controlled Oscillator (VCO) to a lower frequency, enabling phase comparison with a reference signal [2]. In our design, the output of the VCO is centered at 2.4 GHz, while the reference frequency is set at 100 MHz. To ensure frequency and phase synchronization, the divider must reduce the VCO frequency by a factor of 24.

$$N = \frac{f_{out}}{f_{ref}} = \frac{2.4 \text{ GHz}}{100 \text{ MHz}} = 24 \tag{3.1}$$

Thus, we implemented a divide-by-24 (MOD-24) frequency divider.

3.2 Design of High-Speed D Flip-Flop using TSPC Logic

3.2.1 Overview of True Single Phase Clock (TSPC) Logic

As the divider must operate at the VCO output frequency of 2.4 GHz, conventional static CMOS flip-flops become inefficient due to their slower response time and higher clock loading. Hence, we adopted the True Single-Phase Clock (TSPC) technique, a dynamic CMOS logic style optimized for high-speed and low-power sequential design [8, 2].

TSPC logic allows edge-triggered flip-flops to be realized using a single clock phase, significantly minimizing clock routing complexity and power dissipation [9].

3.2.2 Design of TSPC D Flip-Flop

The TSPC D flip-flop is implemented in LT Spice; the schematic of its implementation at the transistor level is shown in Figure 3.1.

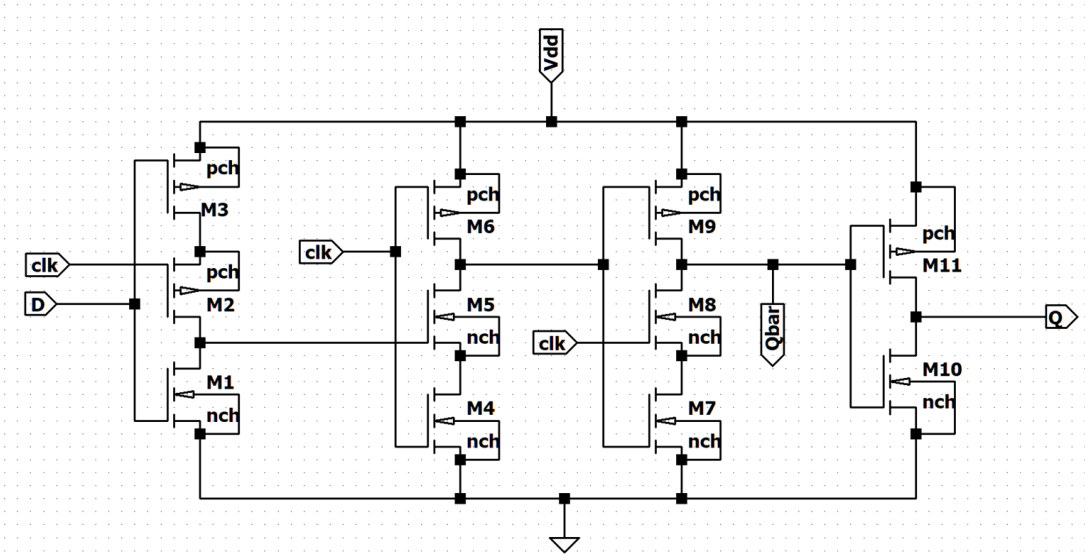

Figure 3.1: Transistor Level Implementation of TSPC D Flip Flop

The following table summarizes the transistor dimensions used in the LTspice schematic (for the 180 nm CMOS process):

Table 3.1: Transistor Dimensions for TSPC D Flip-Flop

Transistor	**Type**	**Length (L)**	**Width (W)**
M1	PMOS	180 nm	0.36 µm
M2	NMOS	180 nm	1.44 µm
M3	PMOS	180 nm	1.44 µm
M4	NMOS	180 nm	0.72 µm
M5	NMOS	180 nm	0.72 µm
M6	PMOS	180 nm	0.72 µm
M7	PMOS	180 nm	0.72 µm
M8	PMOS	180 nm	0.72 µm
M9	PMOS	180 nm	0.72 µm
M10	PMOS	180 nm	0.36 µm
M11	PMOS	180 nm	0.72 µm

Simulation and Verification

The D flip-flop was Successfully tested and Verified in LTspice under a 2.4 GHz clock. The waveform of output Q is shown in Figure 3.2.

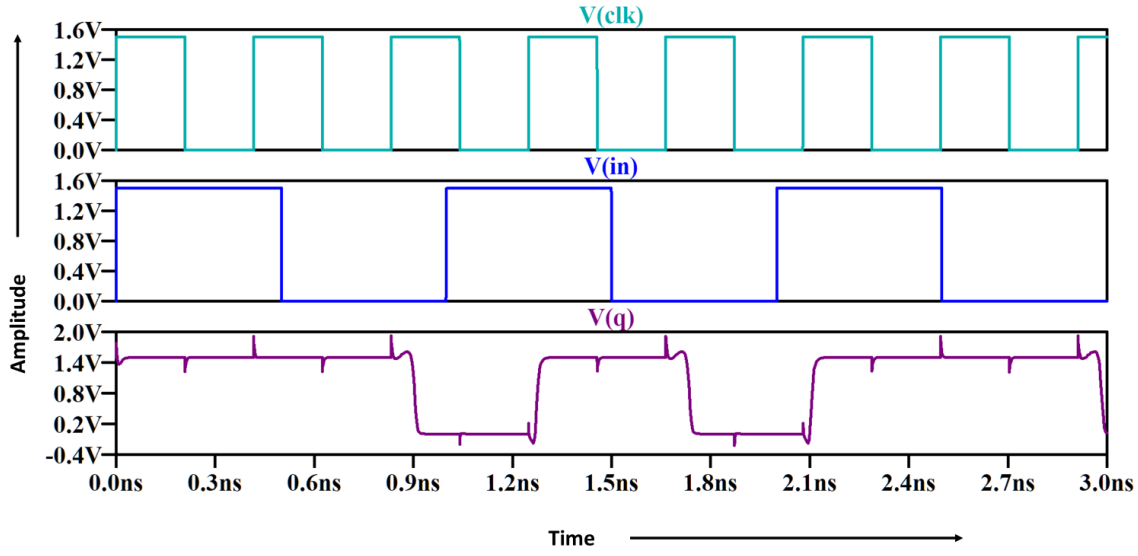

Figure 3.2: Output waveform of TSPC D Flip-Flop at 2.4 GHz

3.3 Mod-24 Divider Using Cascaded Johnson Counters

3.3.1 Architectural Approach

To achieve a divide-by-24 configuration, we implemented a cascade of two Johnson counters:

- A 3-stage Johnson counter (producing MOD-6)
- A 2-stage Johnson counter (producing MOD-4)

This configuration provides the necessary MOD-24 division, as:

$$MOD\ 6 \times MOD\ 4 = 24$$

Each Johnson counter is built from the TSPC D flip-flops designed previously.

Johnson Counter Operation: A Johnson counter operates by feeding the inverted output of the last flip-flop back to the input of the first. For an n-stage Johnson counter, the output cycles through $2n$ unique states. The decoded states from each stage are used to control subsequent stages or form the final output.

3.3.2 Divider Topology

The MOD-6 and MOD-4 counters were connected in a hierarchical manner where the MOD-6 output toggles the clock input of the MOD-4 stage, thus achieving the desired divide-by-24 functionality. This asynchronous configuration reduces power consumption and distributes timing load across stages.

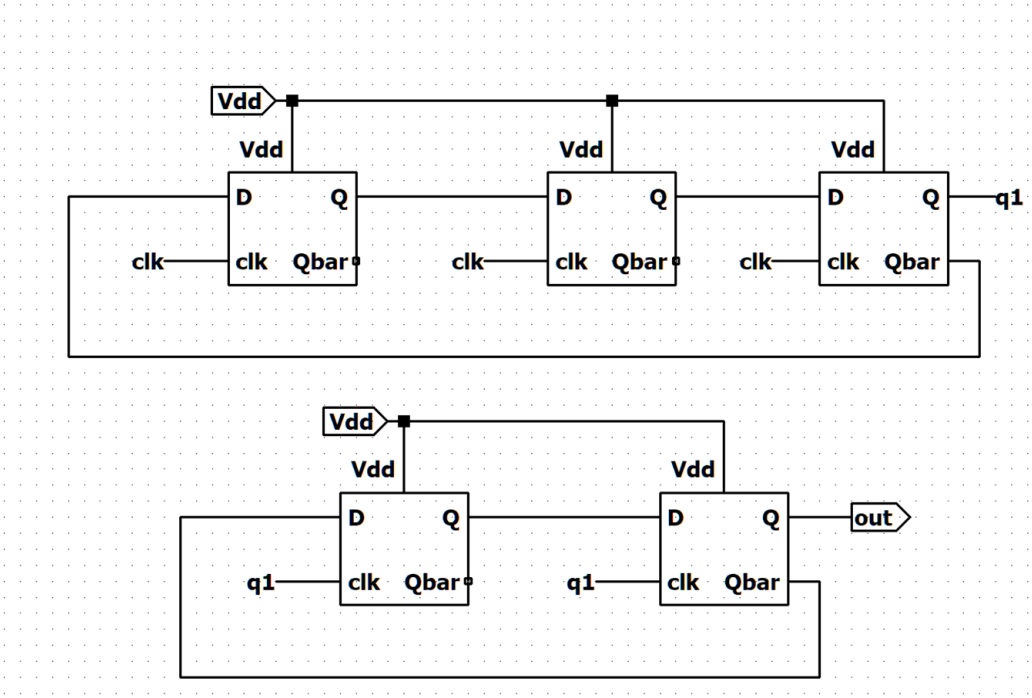

Figure 3.3: Schematic of Cascaded MOD-6 and MOD-4 Johnson Counters (MOD 24 Divider)

3.4 Simulation Results

3.4.1 Transient Analysis

The complete divider circuit was simulated in LTspice using a square wave input of 2.4 GHz. The outputs were verified at each stage of the Johnson counters to validate intermediate functionality. The output of the divider showed a clean square wave with frequency reduced to 100 MHz is shown in 3.4, verifying the correct behaviour of the MOD-24 divider.

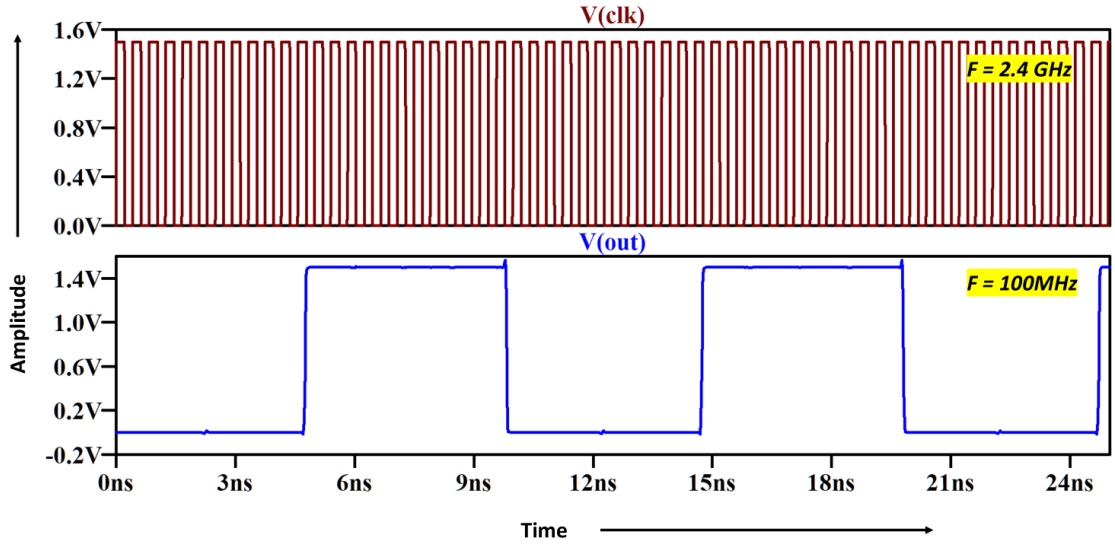

Figure 3.4: Input and Output Waveforms of MOD-24 Divider

3.5 Conclusion

The simulation results confirmed the functionality of the divider, demonstrating its suitability for integration into a PLL that operates at 2.4 GHz.

Design of Phase Frequency Detector

4.1 Overview of Phase Frequency Detector

Figure 4.1: Block Diagram of Phase Frequency Detector

In a Phase-Locked Loop (PLL), the Phase Frequency Detector (PFD) serves as an important block at the input of the feedback loop. It compares the phase and frequency of two input signals: the reference clock and the feedback signal derived from the divided output of the voltage-controlled oscillator (VCO). Based on this comparison, it generates two non-overlapping outputs that drive the charge pump. These outputs indicate whether the feedback signal is lagging or leading with respect to the reference signal, enabling the loop to make precise corrections[2, 10].

4.2 Working Principle

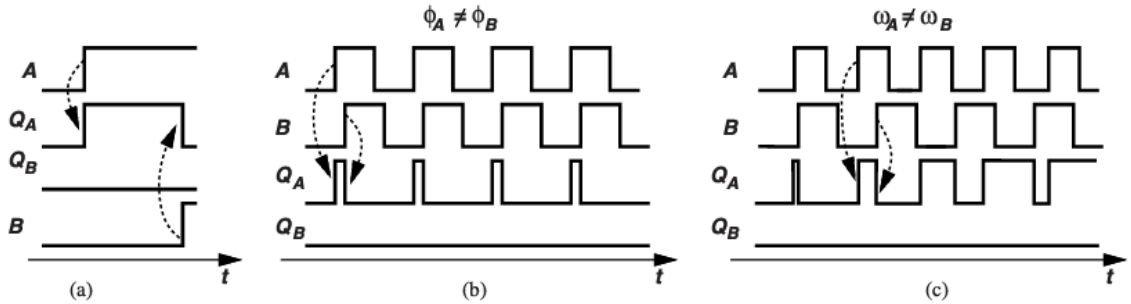

Figure 4.2: (a) Conceptual PFD operation, (b) case of input phase difference, and (c) case of input frequency difference.

The Phase Frequency Detector (PFD) operates on two core principles that enable it to sense both phase and frequency differences between two input signals: the

reference signal A and the feedback signal B. The outputs of the PFD, denoted as Q_A and Q_B, drive the charge pump in a Phase-Locked Loop (PLL).

The general behavior of the PFD can be summarized as follows [1, 2]:

(a) Initially, both Q_A and Q_B are low. When a rising edge is detected on input A while Q_A and Q_B are still low, the circuit sets Q_A to high. This condition signifies that the reference signal A is leading.

(b) If a rising edge is then observed on input B while Q_A is already high, the circuit sets Q_B to high. As soon as both outputs are high, a reset signal is generated (typically through a NAND gate), which pulls both Q_A and Q_B back to low.

(c) The same mechanism applies symmetrically if B leads A. If the rising edge of B arrives first, Q_B is set high. Upon the arrival of the rising edge of A, Q_A is set, and both outputs are subsequently reset.

This edge-triggered approach allows the PFD to detect not only which signal is leading but also how far apart they are in time. The pulse width of Q_A or Q_B corresponds to the time (phase) difference between the input signals. This is clearly illustrated in Fig. 4.2(b), where both signals have the same frequency but a phase offset—the output pulse width is proportional to that offset.

In the case where the input frequencies differ, as shown in Fig. 4.2(c), the average duration for which Q_A or Q_B stays high becomes proportional to the frequency difference. For example, if A has a higher frequency than B, Q_A will exhibit a longer average high period than Q_B.

Thus, the average difference between Q_A and Q_B over time provides a linear measure of phase or frequency error. This difference is subsequently used to control the charge pump, which adjusts the control voltage of the Voltage-Controlled Oscillator (VCO), ensuring that the PLL locks accurately onto the reference signal.

4.3 Design and Simulation of Phase Frequency Detector

4.3.1 Choice of Topology

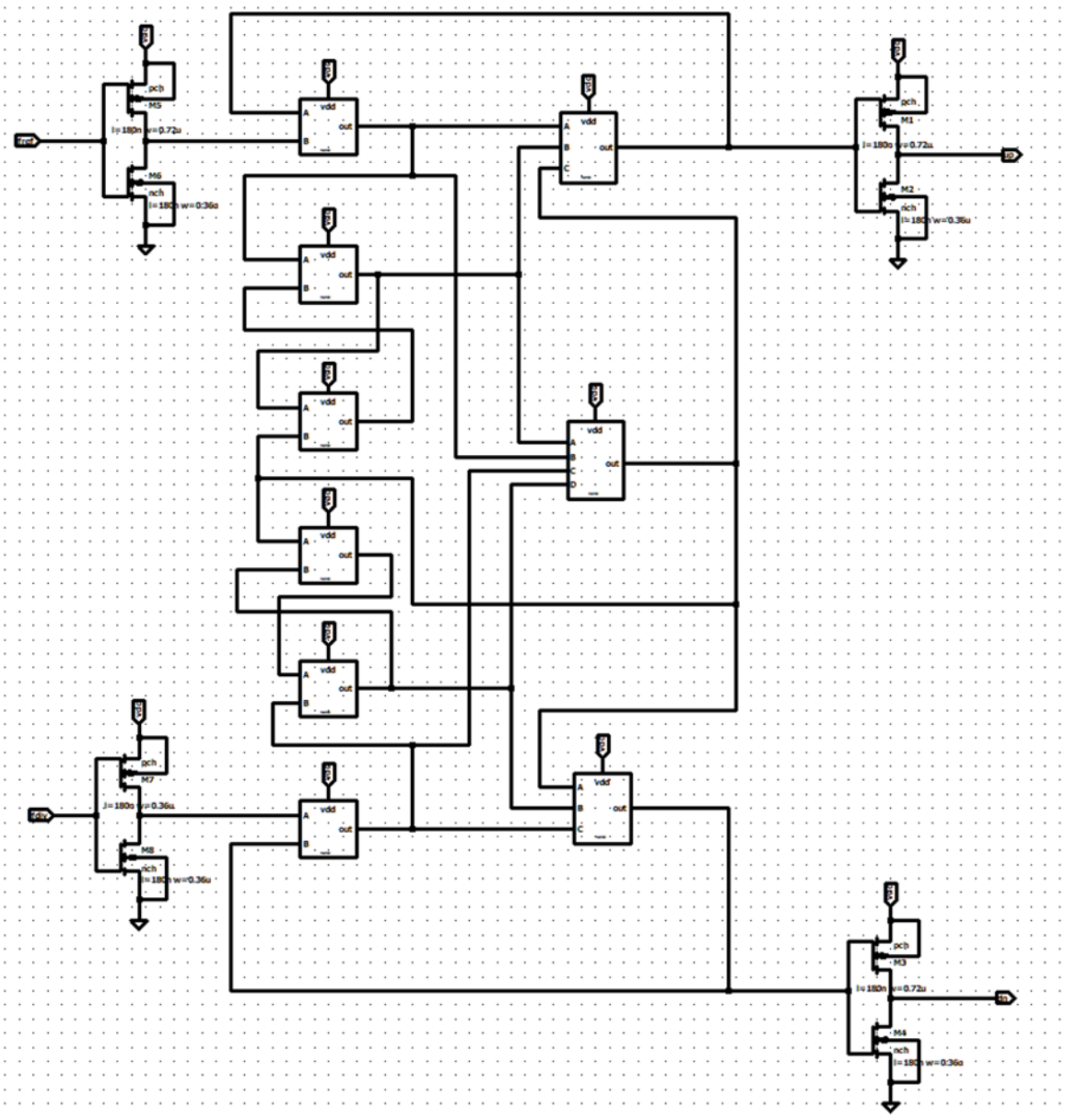

Figure 4.3: Schematic of NAND-based Phase Frequency Detector (PFD)

Figure 4.3 shows the circuit diagram of the NAND-based Phase Frequency Detector (PFD) which is implemented in LT spice. This design uses eleven NAND gates and two inverters. It has two output signals: UP and DOWN. When the reference and feedback signals have different frequencies, the UP and DOWN outputs show which signal is ahead or behind [11].

4.4 Simulation and Functional Verification

4.4.1 Transient Analysis

The transient analysis illustrates how the Phase Frequency Detector (PFD) responds to different conditions of the input signals. In Figure 4.4, both the reference signal and the feedback signal have the same frequency of 100 MHz, but the reference signal slightly lags behind. As a result, the UP and DOWN signals are generated with short pulses, showing that the PFD detects a small phase difference and tries to align both signals.

In Figure 4.5, the reference and feedback signals have different frequencies. This causes the UP and DOWN outputs to produce pulses of varying widths, depending on which signal is faster or slower. These variations reflect continuous adjustments by the PFD to reduce the frequency and phase difference between the two inputs.

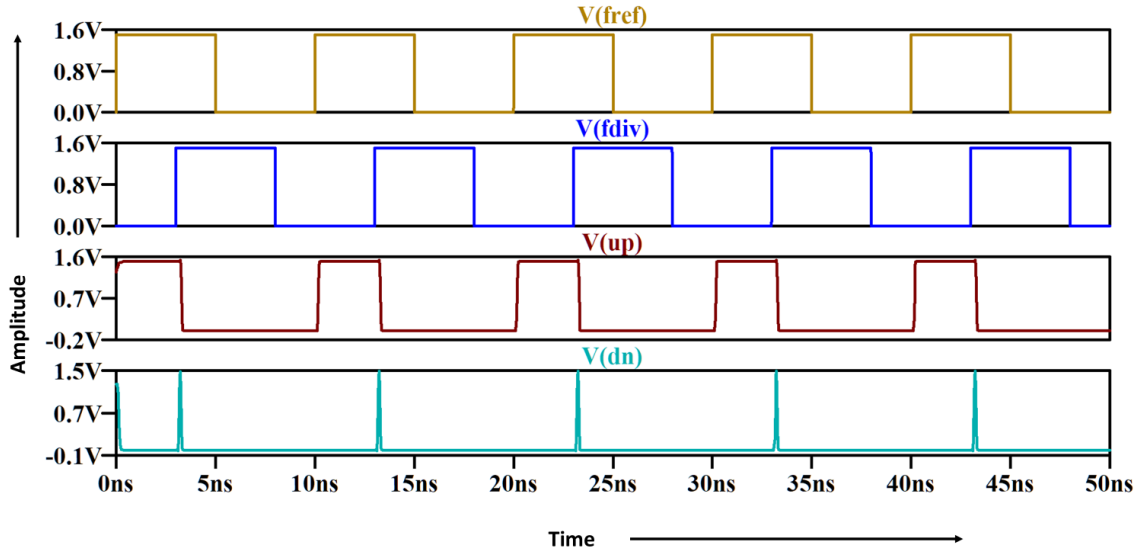

Figure 4.4: Simulated waveforms of UP and DOWN signals when the reference signal lags the feedback signal and both have the equal frequency of 100 MHz

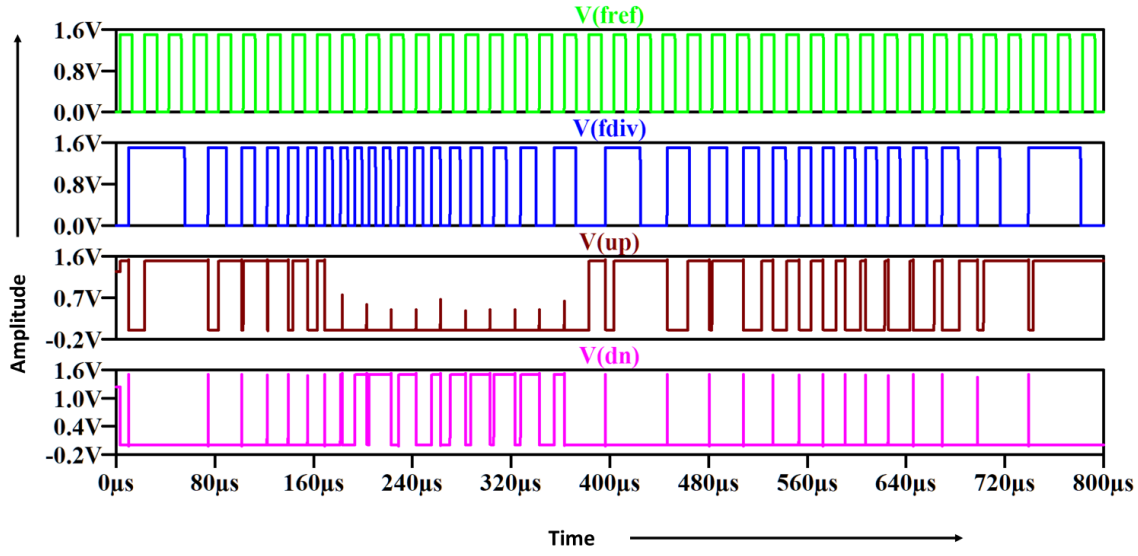

Figure 4.5: Simulated waveforms of UP and DOWN signals when the reference signal and the feedback signal have unequal frequency

Design of Charge Pump and Loop Filter

5.1 Overview of Charge Pump and Loop Filter

In a Phase-Locked Loop (PLL), the Charge Pump (CP) and Loop Filter (LF) together form a critical block that controls the dynamics of the system. The charge pump converts the digital output of the Phase Frequency Detector (PFD) into current pulses. These pulses are then filtered by the loop filter, producing a smooth control voltage that drives the Voltage Controlled Oscillator (VCO). The design of this block is crucial for ensuring stability, settling time, phase margin, and jitter performance of the PLL [2].

5.2 Circuit Description

The charge pump consists of two current sources controlled by the PFD. When the UP signal is active, current is pumped into the filter capacitor; when the DN signal is active, current is drawn from it. The loop filter used here is a passive second-order RC filter which provides a zero to help stabilize the system and a pole to limit high-frequency noise [1].

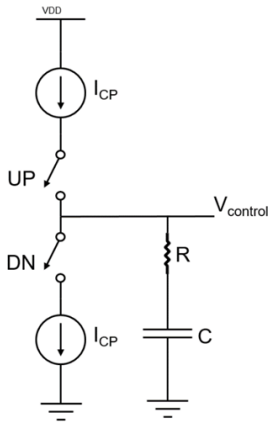

Figure 5.1: Charge Pump and Loop filter Diagram

5.3 Design Calculations

This section summarizes the critical design parameters and formulas used to derive component values.

(a) **Divider Ratio:**

$$N = \frac{2.4\,\text{GHz}}{100\,\text{MHz}} = 24$$

(b) **Charge Pump Current:**

$$I_{CP} = 100\,\mu\text{A}$$

(c) **Loop Bandwidth of the Filter:**

$$F_Loop < \frac{F_Ref}{20}$$

$$F_C = \frac{100\,\text{MHz}}{20} < 5\,\text{MHz}$$

Taking

$$F_C = 1.76\,\text{MHz}$$

(d) **VCO Gain (Calculated earlier from simulation):**

$$K_{VCO} = 177\,\text{MHz/V}$$

(e) **Loop Filter Resistor:**

$$R_S = \frac{2\pi N F_C}{I_{CP} \cdot K_{VCO}} \approx 15\,\text{k}\Omega$$

(f) **Zero Frequency and Capacitor C_S:**

$$F_Z <= \frac{F_C}{3} = 0.58\,\text{MHz}$$

$$C_S = \frac{1}{2\pi R_S F_Z} \approx 18\,\text{pF}$$

(g) **Pole Frequency and Capacitor C_P:**

$$F_P = 3 \cdot F_C = 10\,\text{MHz}$$

$$C_P = \frac{1}{2\pi R_S F_P} \approx 1\,\text{pF}$$

(h) **Final Selected Values:**

$$C_S = 18\,\text{pF}, \quad C_P = 1\,\text{pF}, R_S = 15\,\text{k}\Omega$$

5.4 Circuit Diagram

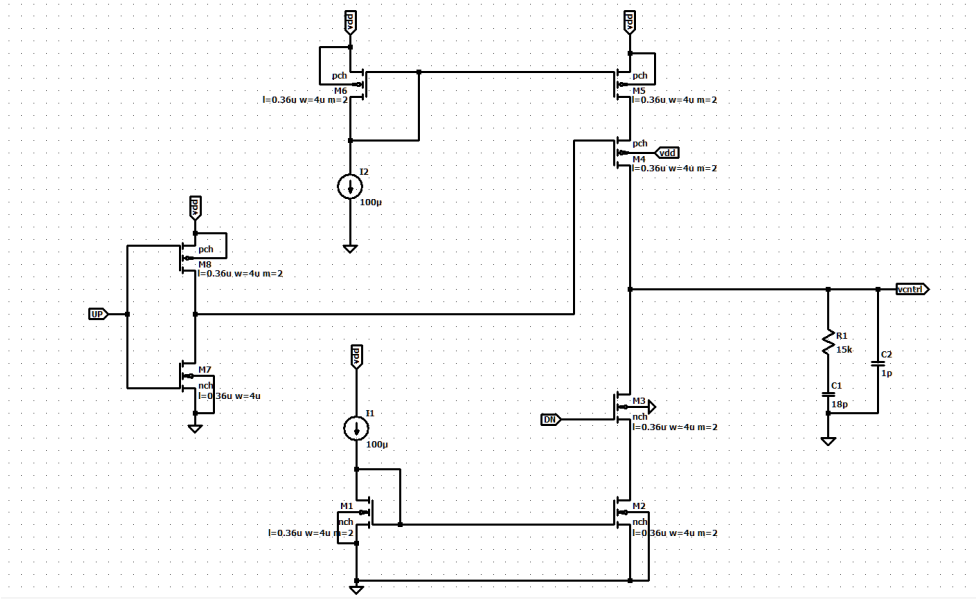

Figure 5.2: Schematic of Charge Pump + Loop Filter Circuit

5.5 Simulation Results

5.5.1 Transient Analysis

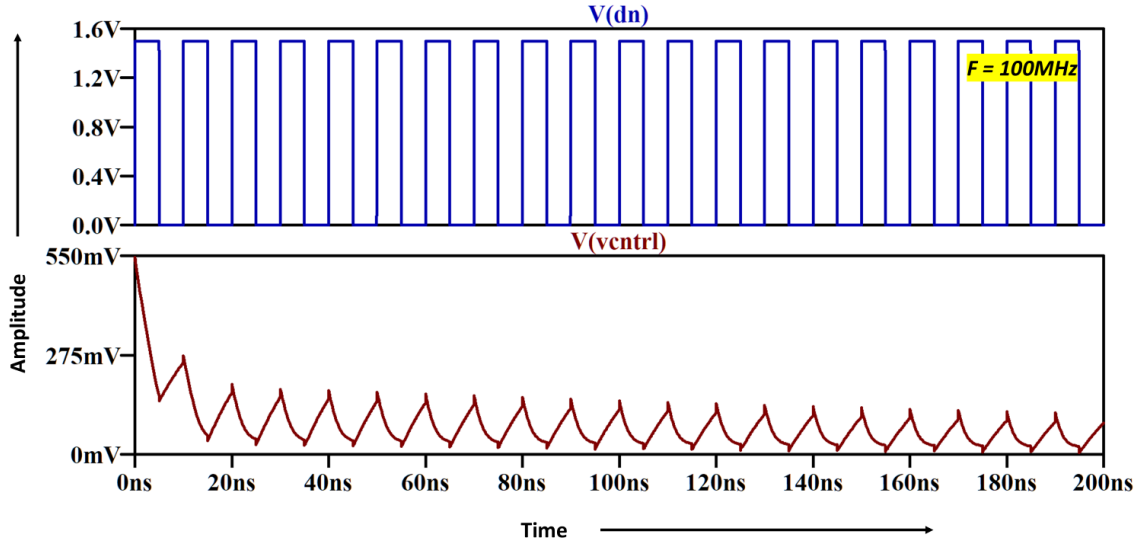

Figure 5.3: Transient Response of Charge Pump + Loop Filter: When Down signal of 100 MHz frequency is provided.

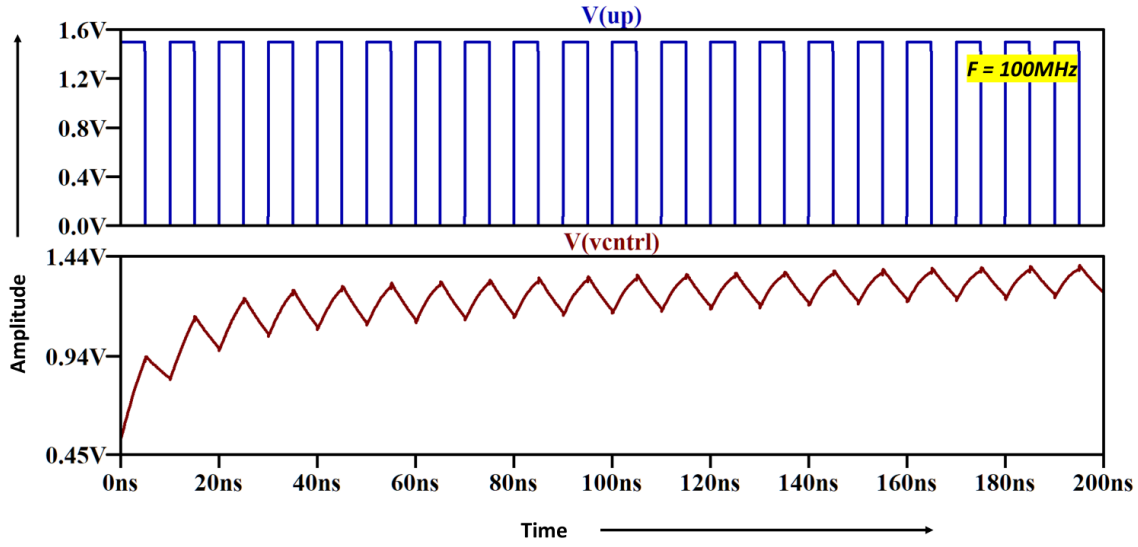

Figure 5.4: Transient Response of Charge Pump + Loop Filter: When UP signal of 100 MHz frequency is provided.

5.6 Conclusion

In this chapter, the design and analysis of the Charge Pump and Loop Filter block were discussed in detail. Component values were calculated to achieve appropriate loop bandwidth and phase margin. The stability of the PLL was ensured by tuning C_S and C_P, and the circuit implementation was verified through simulation.

Design of Phase Locked Loop (PLL)

6.1 Final PLL Integration and Simulation

This section describes the complete integration of all individual PLL blocks in LTspice and the transient simulation carried out to evaluate the performance. The design includes the Phase Frequency Detector (PFD), Charge Pump, Loop Filter, Voltage-Controlled Oscillator (VCO), and Frequency Divider. Each block was represented using a custom symbol in LTspice and connected as shown in the block diagram.

6.1.1 PLL Block Diagram

Figure 6.1 shows the complete PLL block diagram used in this design. The components were interconnected after individual testing. Some fine-tuning of parameters such as transistor widths in the VCO's inverter chain and the loop filter values was performed after complete integration to achieve the desired performance.

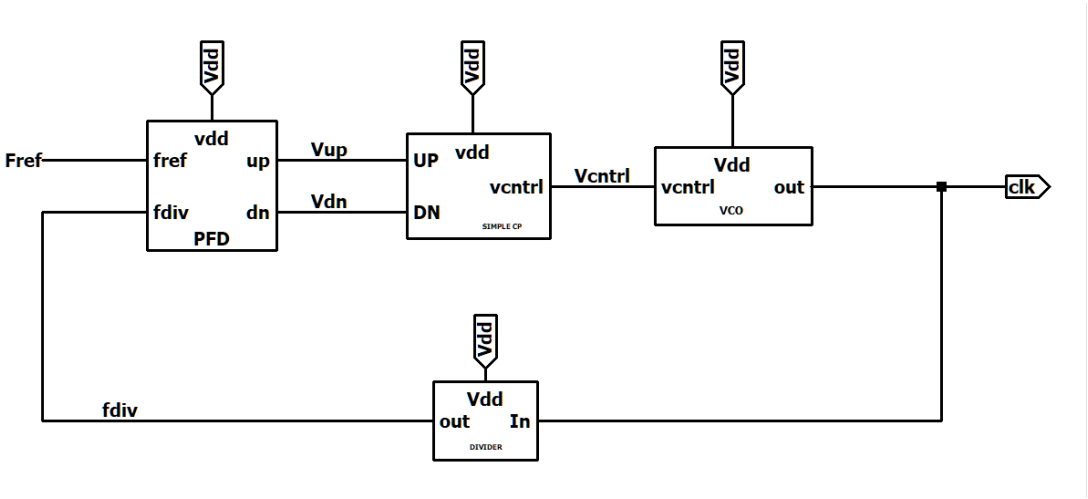

Figure 6.1: Integrated PLL block diagram in LTspice

6.2 Simulation Setup and Results

A reference clock of 100 MHz was provided using a pulse voltage source. The power supply voltage (V_{DD}) for all blocks was set to 1.5 V. The transient simulation was run for a sufficient duration to observe the locking behaviour. The control voltage (V_{ctrl}),

UP/DOWN signals from the charge pump, and the feedback (fdiv) and reference (fref) signals were plotted to verify the phase and frequency locking.

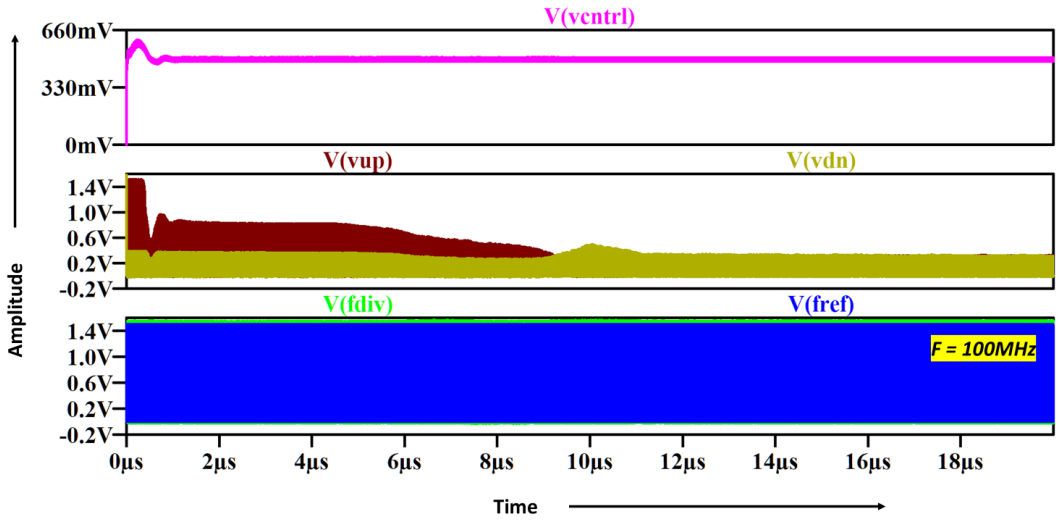

Figure 6.2: PLL transient waveforms showing V_{ctrl},Up and down signals, fref and fdiv

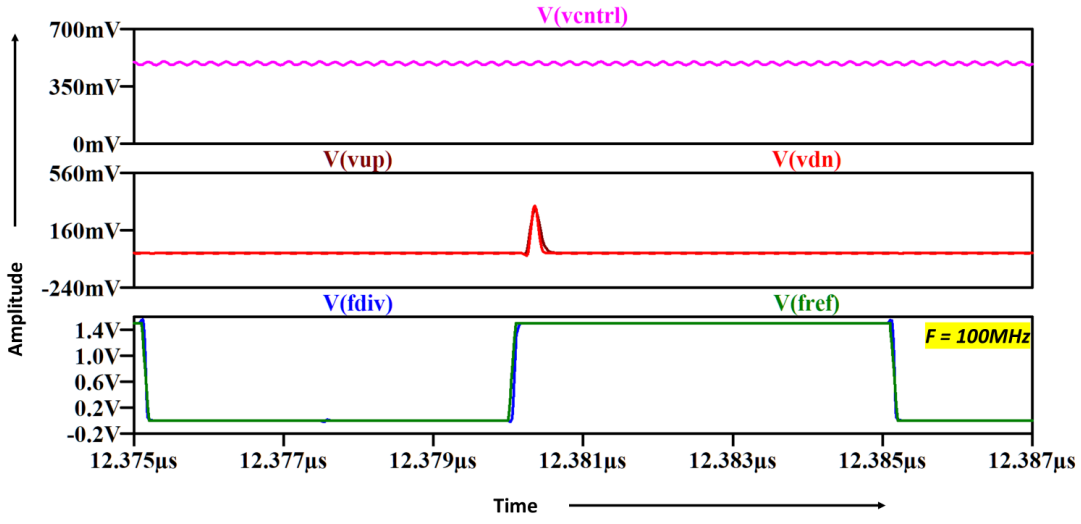

Figure 6.3: Zoomed-in view of the PLL waveforms from Figure 6.2, showing the fine fluctuations in control voltage and the phase alignment of fref and fdiv after locking.

6.2.1 Locking Behavior

The PLL successfully achieves lock after approximately **12** μ**s** as shown in figure Figure 6.3. This is identified by the stabilization of the control voltage (V_{ctrl}) and

the overlap of the reference and feedback clocks. After locking:

- The control voltage settles at approximately **0.5 V**.
- There remains a small fluctuation (**20 mV**) in V_{ctrl}, which is expected due to loop dynamics and inverter-based VCO noise.
- The feedback clock (fdiv) nearly overlaps with the reference clock (fref) with minor non-overlap, indicating a good phase alignment.

The average power dissipation measured across the entire PLL circuit was found to be approximately **6.36 mW**. This value accounts for dynamic and static power consumption of the constituent blocks under a 1.5 V supply. The result shows that the PLL operates efficiently at gigahertz frequency while maintaining moderate power usage.

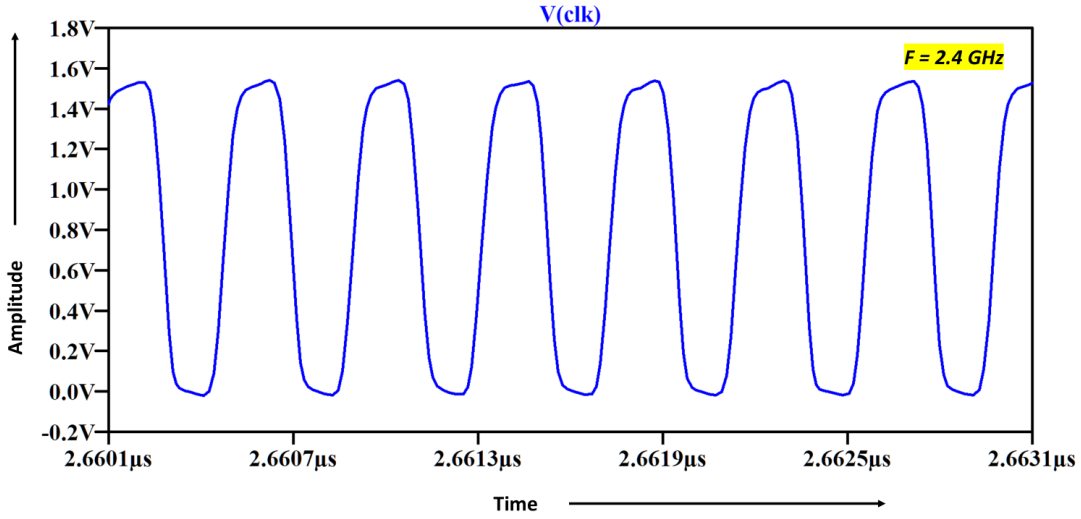

Figure 6.4: Simulation Waveform for output frequency (clk)

6.2.2 Summary of Observations

Table 6.1: Final PLL Performance Summary

Parameter	**Observed Value**
Reference Frequency (f_{ref})	100 MHz
Supply Voltage (V_{DD})	1.5 V
Locking Time	12 μs
Locking Control Voltage (V_{ctrl})	0.5 V
Control Voltage Ripple	20 mV
Output Frequency	2.4 GHz
Power Dissipation	6.36 mW

Conclusion and Future Scope

7.1 Conclusion

A complete 2.4 GHz Phase-Locked Loop (PLL) system was successfully designed and simulated using LTspice in 180 nm CMOS technology, operating at a supply voltage of 1.5 V. The individual building blocks—namely the Phase Frequency Detector (PFD), Charge Pump (CP), Loop Filter, Voltage Controlled Oscillator (VCO), and Frequency Divider—were developed and verified independently before being integrated into a complete system. Each module was encapsulated with custom symbols to support modular design and ease of simulation.

The system was driven by a 100 MHz reference clock signal, and transient analysis was conducted to assess the loop's dynamic locking characteristics. The PLL effectively generated a stable 2.4 GHz output frequency. The control voltage (V_{cntrl}) settled at approximately 0.5 V, and the feedback signal (f_{div}) closely tracked the reference signal (f_{ref}), indicating successful locking behavior. However, minor control voltage fluctuations were observed post-locking, and a small phase discrepancy remained, as the f_{ref} and f_{div} signals did not exhibit perfect overlap.

7.2 Future Work

Although the 2.4 GHz PLL system was successfully designed and simulated, several enhancements can be explored in future work to improve performance and broaden applicability:

(a) **Reduction of Phase Error and Control Voltage Fluctuations**
The observed minor fluctuations in control voltage and the small phase mismatch between f_{ref} and f_{div} suggest scope for optimization. Techniques such as improved charge pump matching, loop filter redesign can be considered to achieve better phase alignment and minimize jitter.

(b) **Layout Design and Post-Layout Simulation**
The current work is limited to schematic-level simulation. Future efforts can focus on full custom layout of the PLL blocks followed by post-layout simulations including parasitic extraction.

(c) **Power Optimization**
The total power dissipation of the system is measured at 6.36 mW. Future work can target low-power design techniques.

Bibliography

[1] S. Hokrani, T. Thanuja, and K. Kumaraswamy, "Design and implementation of phase locked loop on 180nm technology node," in *2018 4th International Conference for Convergence in Technology (I2CT)*. IEEE, 2018, pp. 1–6.

[2] B. Razavi, *Design of Analog CMOS Integrated Circuits*, ser. Electrical Engineering Series. McGraw-Hill, 2001.

[3] S. S. S and S. S. Yellampalli, "Design of 6.7 ghz ˜ 7. 518 ghz cross coupled lc-vco in 180nm cmos technology," in *2021 5th International Conference on Computing Methodologies and Communication (ICCMC)*, 2021, pp. 665–671.

[4] J. S. Hamel and R. Norris, "Lc tank voltage controlled oscillator tutorial," Presented to the UW ASIC Analog Group, Waterloo, Ontario, Canada, 2005, edited by Ryan Norris. [Online]. Available: https://www.academia.edu/26763368/LC_Tank_Voltage_Controlled_Oscillator_Tutorial

[5] K. Narasimhamurthy, "Design of voltage controlled oscillator for 2.4 ghz wireless applications," *International Journal of Computer Applications*, vol. 975, p. 8887, 2015.

[6] B.-H. Lee, Y.-Y. Lin, and T.-H. Huang, "2.4 ghz wide-tuning vco using switchable imos-based varactor in 180-nm cmos," in *2021 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*. IEEE, 2021, pp. 1–3.

[7] M. Nasrollahpour, C. Yen, and S. Hamedi-hagh, "Low-power and high-frequency symmetry load ring-vco for bluetooth application„" 09 2017.

[8] P. B.S., D. T.N., S. Parashar, and D. Bharadwaj, "Design and implementation of high frequency and low-power phase-locked loop," *U.Porto Journal of Engineering*, vol. 7, pp. 70–86, 11 2021.

[9] J.-H. Tsai, S.-W. Huang, and J.-P. Chou, "A 5.5 ghz low-power pll using 0.18-µm cmos technology," in *2014 IEEE Radio and Wireless Symposium (RWS)*, 2014, pp. 205–207.

[10] P. Kumar, A. Khele, and A. C. Joshi, "Design of phase locked loop in 180 nm technology," *arXiv preprint arXiv:2406.13462*, 2024.

[11] L. Bitla, V. Saraswathi, and R. Vairagade, "Recent analysis of nand gate based phase frequency detector for phase locked loop (pll)," *Research and Developments in Engineering Research*, p. 94.

draft_plag.pdf

ORIGINALITY REPORT

12%	7%	6%	8%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	Submitted to Asia Pacific University College of Technology and Innovation (UCTI) Student Paper	1%
2	Submitted to B.V. B College of Engineering and Technology, Hubli Student Paper	1%
3	dokumen.pub Internet Source	1%
4	www.researchgate.net Internet Source	1%
5	theses.fr Internet Source	1%
6	Submitted to Manipal University Jaipur Online Student Paper	1%
7	www.freepatentsonline.com Internet Source	1%
8	catalog.gaw.ru Internet Source	<1%
9	Andrei Grebennikov. "RF and Microwave Transmitter Design", Wiley, 2011 Publication	<1%
10	www.science.gov Internet Source	<1%

11	"Recent Trends in Electronics and Communication", Springer Science and Business Media LLC, 2022 Publication	<1 %
12	ir.lib.ncu.edu.tw:88 Internet Source	<1 %
13	Submitted to Eskisehir Osmangazi University Student Paper	<1 %
14	Submitted to VIT University Student Paper	<1 %
15	db.carnewschina.com Internet Source	<1 %
16	archive.org Internet Source	<1 %
17	Submitted to UT, Dallas Student Paper	<1 %
18	Submitted to CSU, San Jose State University Student Paper	<1 %
19	Submitted to University of Queensland Student Paper	<1 %
20	Hui-min Liu, Xiao-xing Zhang, Yu-jie Dai, Ying-jie Lv. "Low power consumption high speed CMOS dual-modulus 15/16 prescaler for optical and wireless communications", Optoelectronics Letters, 2011 Publication	<1 %
21	Submitted to IIT Delhi Student Paper	<1 %
22	Submitted to Information and Communication University	<1 %

	Student Paper	
23	etd.ohiolink.edu Internet Source	<1 %
24	pdffox.com Internet Source	<1 %
25	Submitted to Aligarh Muslim University, Aligarh Student Paper	<1 %
26	Hao Shang, J.W.M. Rogers, J. Chiu. "A Fully Differential 24GHz Transmit PLL in a 0.13µm CMOS Technology", 2006 IEEE North-East Workshop on Circuits and Systems, 2006 Publication	<1 %
27	Submitted to Nanyang Technological University, Singapore Student Paper	<1 %
28	Submitted to Ho Chi Minh University of Technology and Education Student Paper	<1 %
29	Submitted to Wright State University Student Paper	<1 %
30	academic.oup.com Internet Source	<1 %
31	ia800507.us.archive.org Internet Source	<1 %
32	naehwaren.de Internet Source	<1 %

Exclude quotes On Exclude matches < 10 words

Exclude bibliography On