Half Adder Design: Schematic to GDSII using GPDK90 in Cadence

Contents

1 Introduction

This report details the complete design flow of a Half Adder, starting from schematic creation to GDSII generation, using Cadence tools with the GPDK90 process library. A half adder is a fundamental digital circuit that performs binary addition on two single-bit inputs, generating a sum and a carry output. The design flow covered in this report includes schematic design, layout, design rule checks (DRC), layout versus schematic checks (LVS), and RC extraction.

2 Half Adder: Definition and Truth Table

A half adder is a combinational circuit that adds two single-bit binary numbers (A and B). It produces two outputs:

- **Sum (S):** The result of the binary addition.
- **Carry (C):** Represents any overflow into the next higher bit.

Input A	Input B	Sum (S)	Carry (C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

3 Design Flow

The Half Adder design follows a standard ASIC design flow:

1. **Schematic Creation**
2. **Symbol and Testbench Setup**
3. **Pre-Layout Simulation**
4. **Layout Creation (DRC and LVS checks)**
5. **Post-Layout Simulation**
6. **RC Extraction**
7. **GDSII Generation**

4 Detailed Process and Results

4.1 Schematic Creation

The initial schematic of the Half Adder was created using GPDK90 in Cadence. The schematic forms the base for further simulations and layout design.

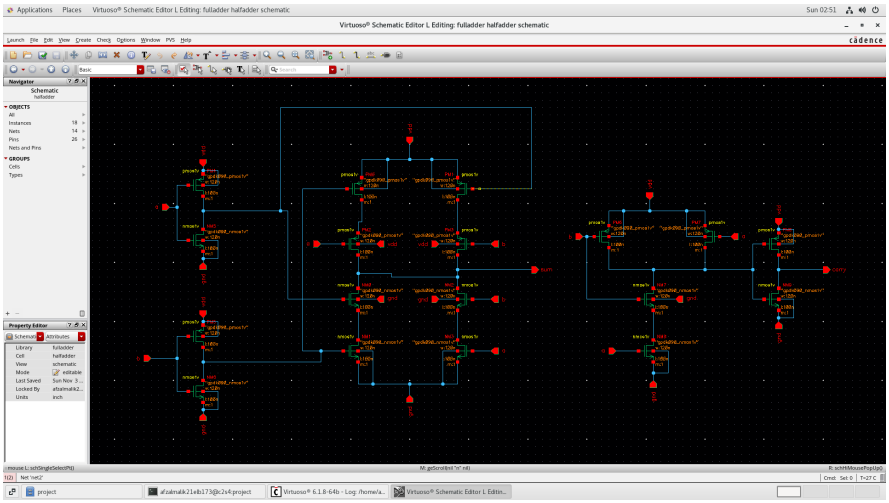

Figure 1: Half Adder Schematic

4.2 Symbol and Testbench Creation

A symbol view was generated for the Half Adder, and a testbench was set up to verify its functionality through transient and delay analysis.

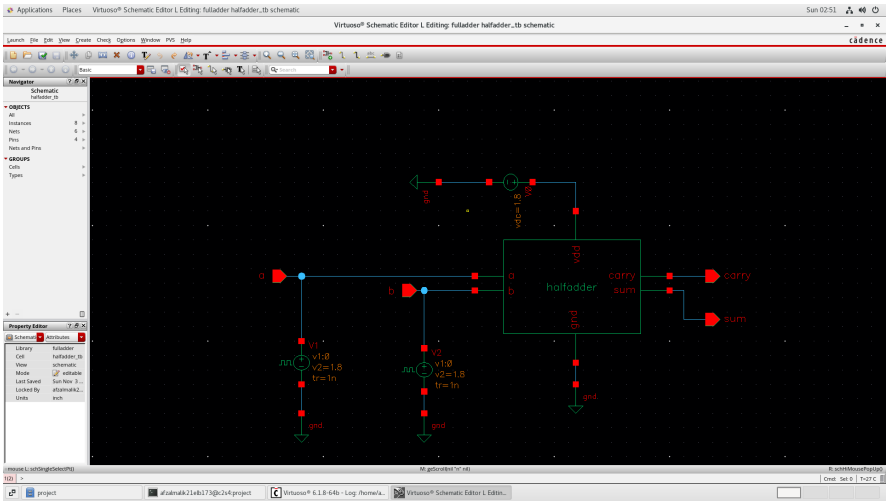

Figure 2: Symbol and Testbench

4.3 Pre-Layout Simulation Results

Simulations were run to verify the functionality and performance of the Half Adder. Critical parameters such as delay from input **A** to **Sum** and **Carry** were analyzed.

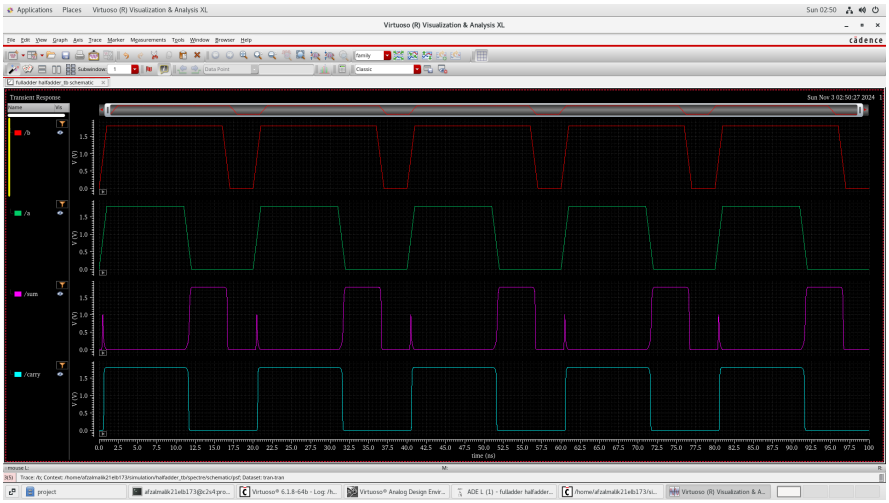

Figure 3: Pre-Layout Simulation

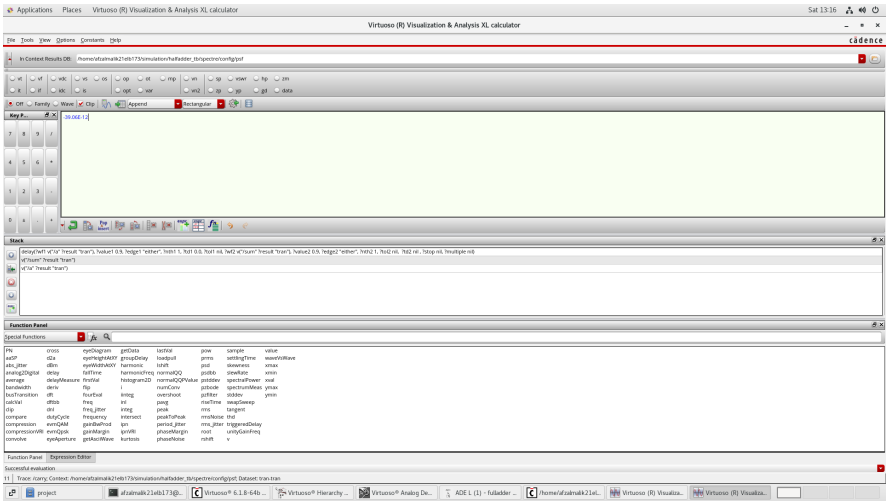

Figure 4: Delay from Terminal A to Sum (Pre-Layout)

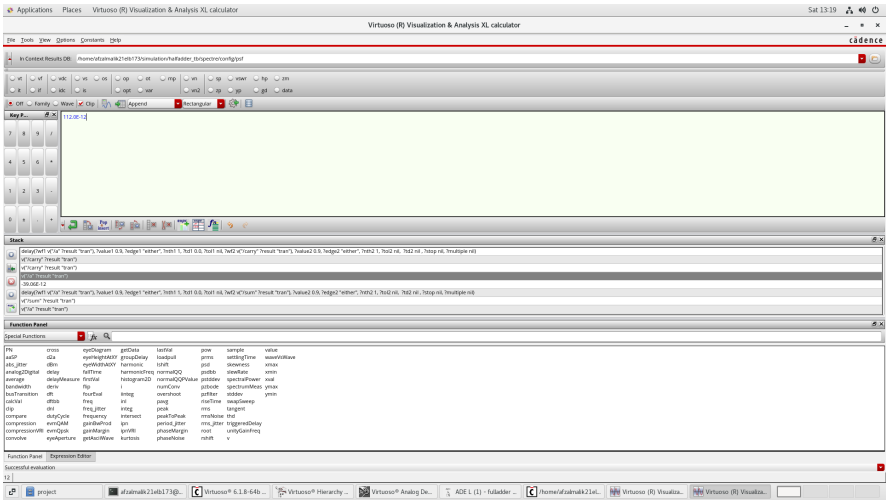

Figure 5: Delay from Terminal A to Carry (Pre-Layout)

4.4 Layout Creation and Verification

The Half Adder layout was designed in Cadence Virtuoso with GPDK90. After completing the layout, **Design Rule Check (DRC)** and **Layout Versus Schematic (LVS)** checks were performed to ensure compliance and correctness.

- **DRC:** Passed successfully

- **LVS:** Passed successfully

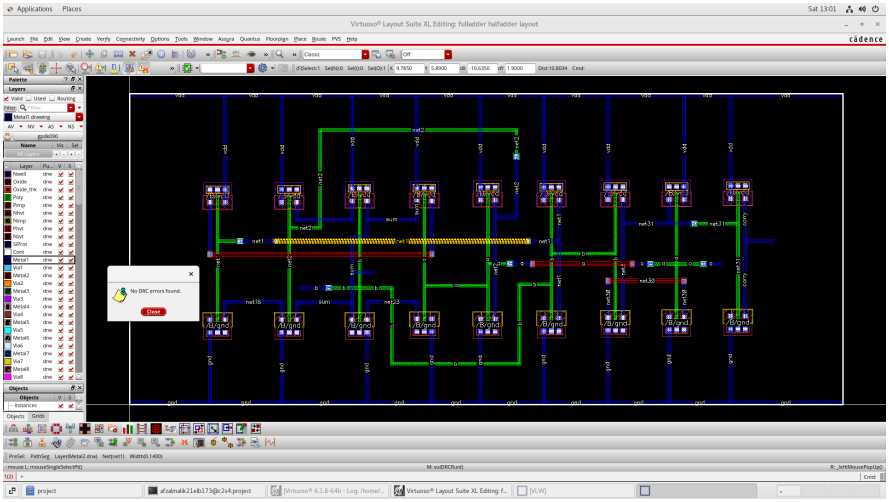

Figure 6: DRC Result

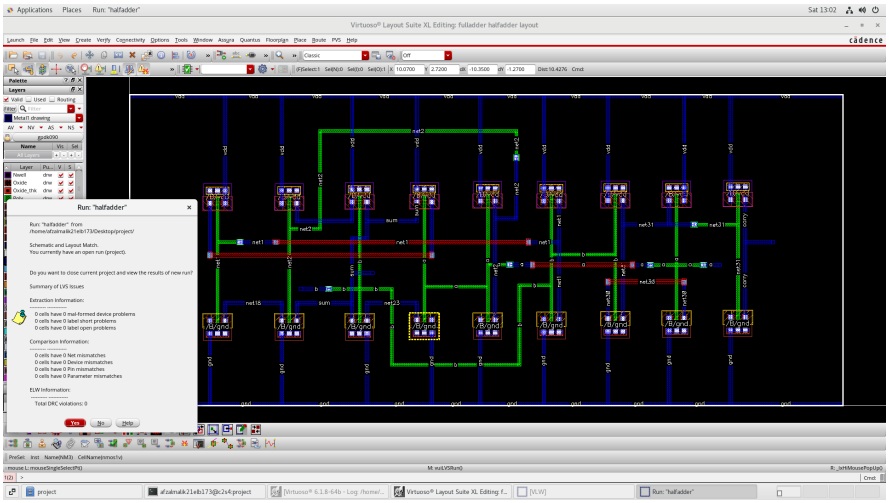

Figure 7: LVS Check

4.5 Post-Layout Simulation Results

After layout, post-layout simulations were conducted to examine performance changes due to parasitic elements. Delays from terminal **A** to **Sum** and **Carry** were analyzed again.

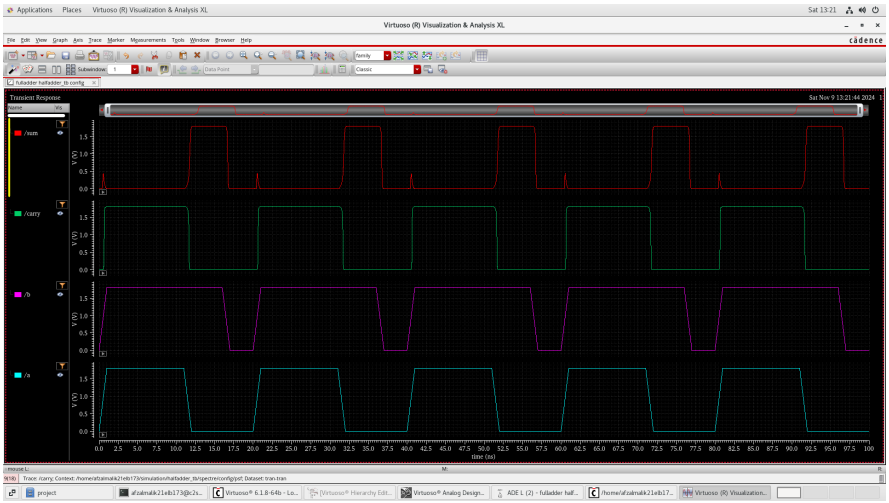

Figure 8: Post-Layout Simulation

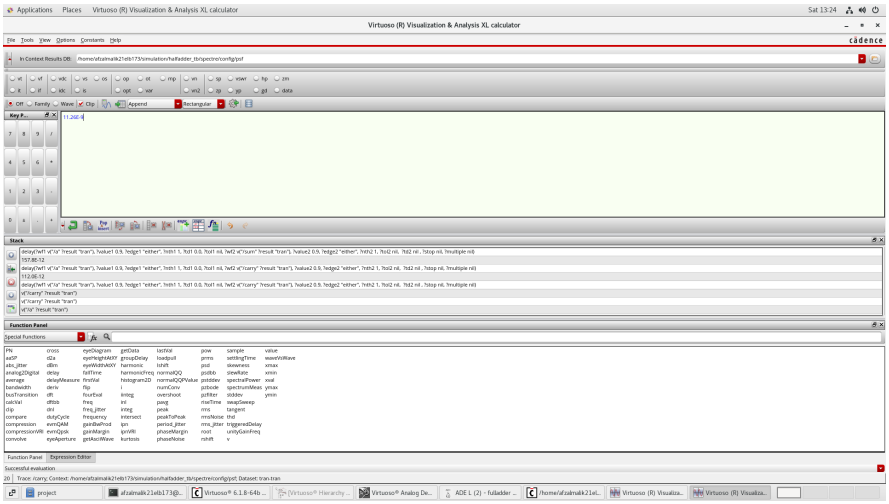

Figure 9: Delay from Terminal A to Sum (Post-Layout)

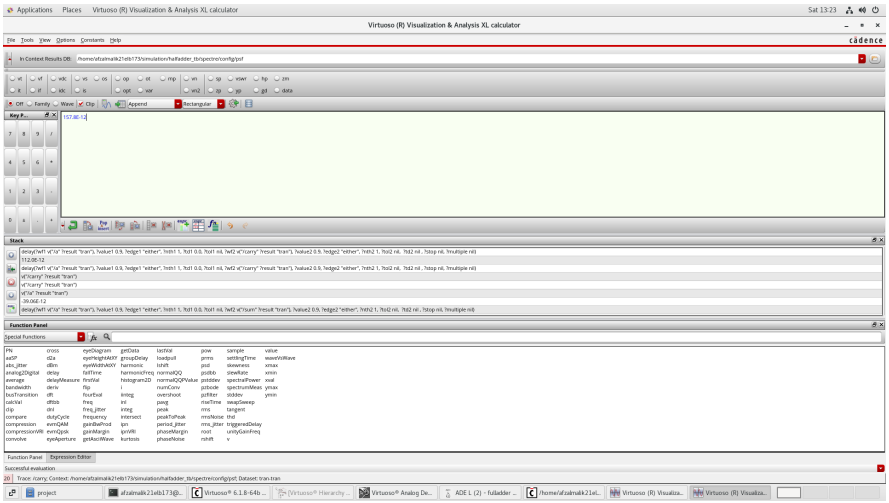

Figure 10: Delay from Terminal A to Carry (Post-Layout)

4.6 RC Extraction

RC extraction was performed to capture parasitic capacitance and resistance, ensuring post-layout simulations reflect realistic circuit behavior.

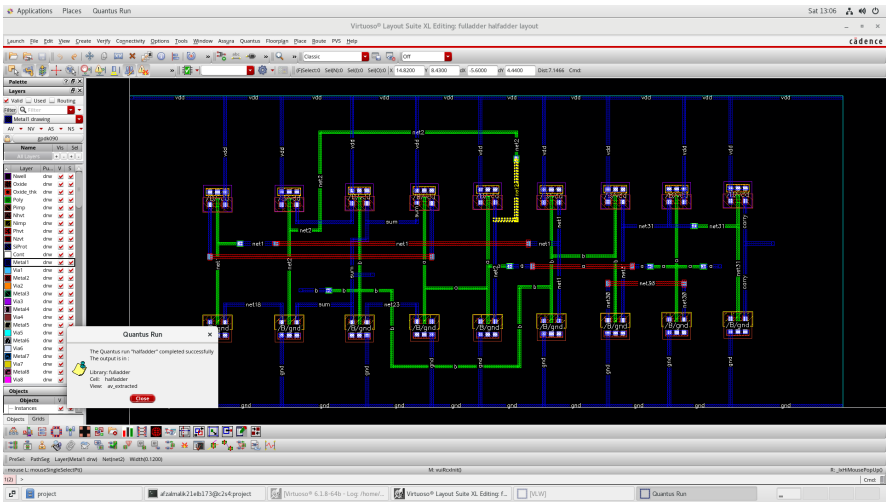

Figure 11: RC Extraction Results

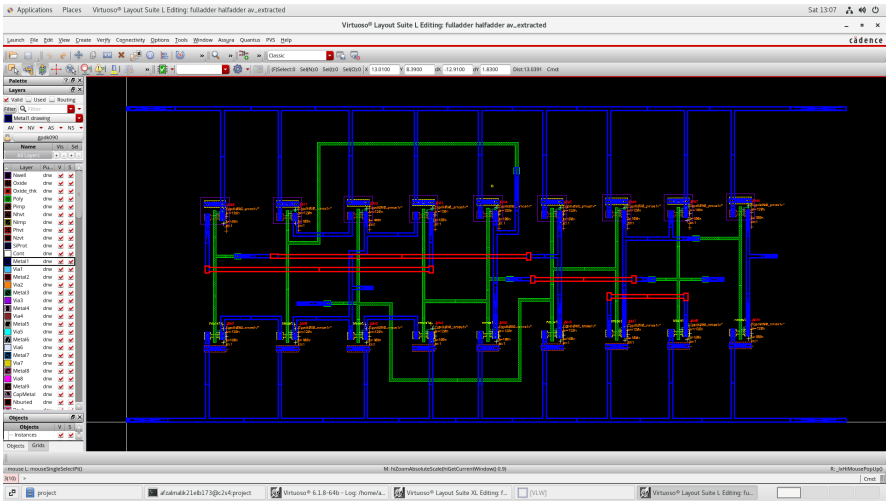

Figure 12: RC Extracted Layout

4.7 GDSII Generation

The final design was exported in GDSII format for tape-out or further processing steps.

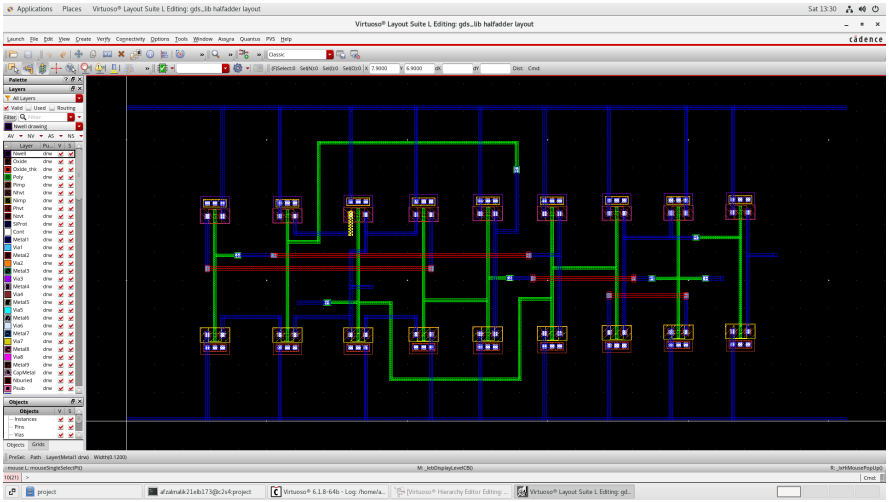

Figure 13: GDSII File

5 Technical Details

5.1 Important Definitions

- **DRC (Design Rule Check):** Ensures that the layout complies with specific design rules set by the fabrication process.
- **LVS (Layout Versus Schematic):** Verifies that the layout corresponds accurately to the schematic netlist.
- **RC Extraction:** Process of modeling parasitic resistances (R) and capacitances (C) after layout, which impact signal delay and power consumption.
- **GDSII Format:** A binary format for transferring IC layout data to silicon foundries.

6 Tools Used

- **Cadence Virtuoso** for Schematic, Layout, and GDSII generation.
- **Spectre Simulator** for pre- and post-layout simulations.
- **GPDK90:** A generic process design kit based on 90 nm technology.

7 Conclusion

This report presented the Half Adder design flow, from schematic to GDSII generation. The successful completion of DRC, LVS, and RC extraction, along with pre- and post-layout simulations, validates the functionality and performance of the designed Half Adder.