CHAPTER 5

The CMOS Inverter

Hydrogen, photons, and electronic inverters are indivisible units of the elements, light, and computers.

Anonymous

Logic gate electronics begins with the inverter whose simple two-transistor appearance hides its complexity. The inverter has about a dozen important properties that are shared by multi-input gates such as NAND and NOR gates. We will become proficient in understanding these electronic properties.

CMOS refers to a particular method or technology for designing and building integrated circuits. The word complementary means that *n*MOS and *p*MOS transistor pairs are linked to make logic gates. Originally, CMOS integrated circuits (ICs) used metal for the transistor gate material. Then polysilicon replaced metal for many years, but new technology has returned to metal gates. CMOS is one of several technologies with which we can build digital circuits. It was first manufactured by the RCA Corp. in 1964. Its popularity grew slowly, but it has been the dominant digital technology since the early 1980s.

5.1. The CMOS Inverter

The inverter is the most abundant logic gate in digital ICs. An inverter converts a logic high input voltage, such as $V_{DD} = 1.5$ V to a low logic voltage of 0 V, and converts a logic low input voltage to a logic high voltage (i.e., 0 V to 1.5 V). V_{DD} is the standard symbol for CMOS power supply voltage. The inverter electronic symbol, truth table, and schematic are shown in Figure 5-1. The logic statement is $V_O = \overline{V}_{in}$. When V_{in} is a high voltage, the *n*MOS transistor turns on and the *p*MOS transistor turns off driving the output node to ground. A low input voltage turns the *p*MOS transistor *on* and the *n*MOS *off* driving the output node to a high logic voltage of V_{DD}. This *on–off* tandem operation guarantees there is no current from V_{DD} to ground (GND) when the logic values are settled. This is a significant low power feature of CMOS.

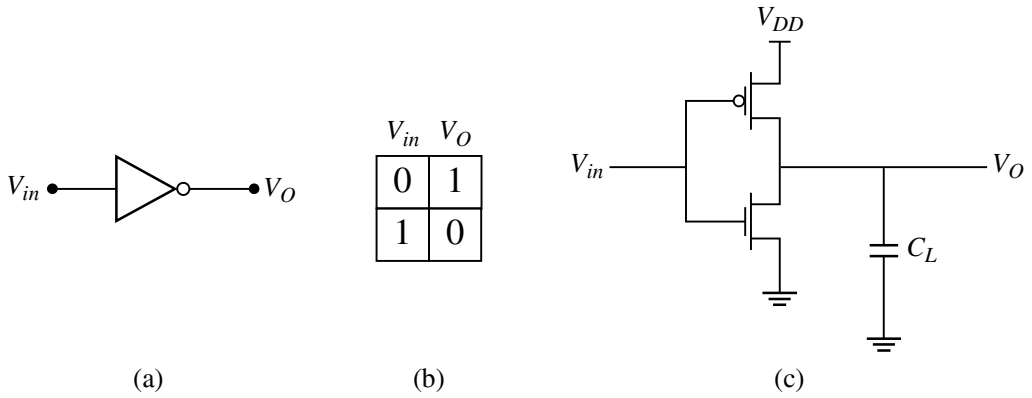


FIGURE 5-1.

Inverter. (a) Symbol. (b) Truth table. (c) Schematic.

Boolean values are detected in the inverter quiescent state when all signal nodes settle to their steady state. Only one transistor is *on* in the steady state connecting the output terminal V_O to one of the power rails. There is no current in the circuit since the other transistor is *off,* eliminating a direct current (DC) path between the rails. The capacitive load C_L shown in Figure 5-1 is unavoidable in any circuit. The capacitance is a lumped value including transistor internal nodes, load wiring, and downstream logic gates. C_L does not affect static properties, but hinders the speed of logic transitions. We will analyze the dynamic operation later.

V_{DD} varies with the application and advances in circuit design. V_{DD} may be lower than 1 V for certain leading-edge circuits or range from 1.2 V to 3.3 V for older still viable technologies. Battery operated digital circuits use V_{DD} values that are typically on the order of 1.5 V. This chapter uses a range of circuit power supply voltages in its examples to adjust our thinking to the diversity expected in real environments.

The logic gate output voltage responds to a small range of input voltages but functionally maps into just one of the two logic states. For example, a 2.5 V power supply technology has nominal logic levels of 2.5 V (high) and 0 V (low). When the input high ranges from 2 V to 2.5 V, the inverter output retains a stable logic low of about 0 V. An input logic-0 ranging from about 0 V to 0.5 V will deliver a stable 2.5 V output. Mapping an input voltage range to a stable output logic state implies noise immunity in the digital circuits. Logic circuit immunity to electronic noise is a design specification.

A third range of digital voltage levels is not mapped to any logic state and that is the voltage transition range that occurs during a logic change of state. Nodes voltages in the transition have no logic meaning. They are the voltages between a logic-1 and logic-0. But the transition region is extremely important since it determines the time to change logic states.

The transistor cross section for an inverter is shown in Figure 5-2. The *n*-channel transistors have a *p*-bulk to attract minority carriers. The *p*-doped bulk is called a *p*-well. Notice the *n*MOS source is tied to the grounded *p*-well and the *p*MOS source is tied to

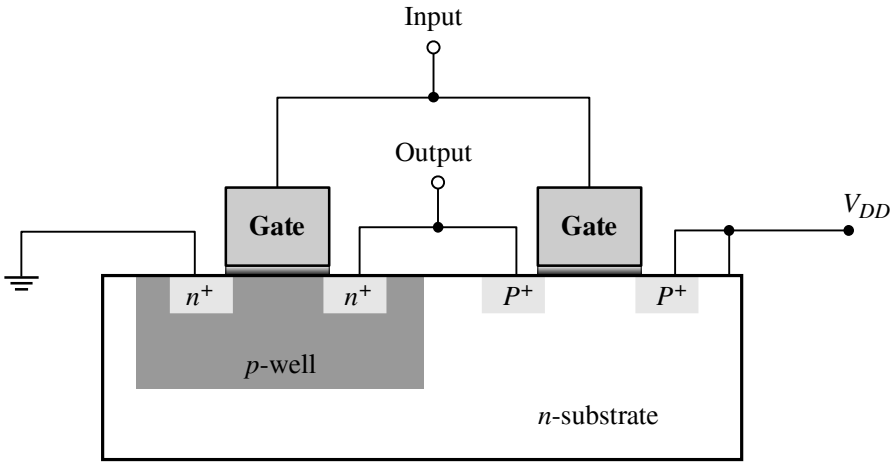


FIGURE 5-2.

CMOS inverter cross section.

the substrate at V_{DD}. The diagram sketches a p-well, but n-wells are also used with the p-channel transistors lying in an n-well. The p-channel transistors have an n-substrate to attract minority carriers.

5.2. Voltage Transfer Curve

The *voltage transfer curve* (VTC) measures the output voltage over the range of input voltages. The VTC in Figure 5-3a shows that $V_O = V_{DD} = 1.2$ V when $V_{in} = 0$ V, and that $V_O = 0$ V when $V_{in} = V_{DD} = 1.2$ V. The general inverted S-shape of the VTC does not change much as V_{DD} changes. The V_{DD} on IC products may range from 0.8 V to 5 V. Modern V_{DD} values lie at the lower end. $V_{DD} = 1.2$ V was chosen as a typical value in this VTC example.

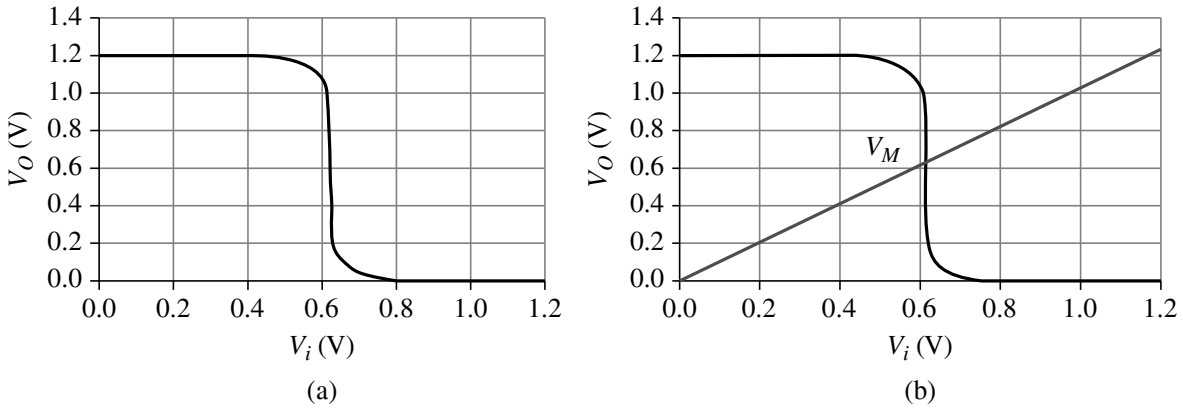


FIGURE 5-3.

(a) Voltage transfer curve (VTC) of CMOS inverter. (b) VTC showing threshold logic point V_M.

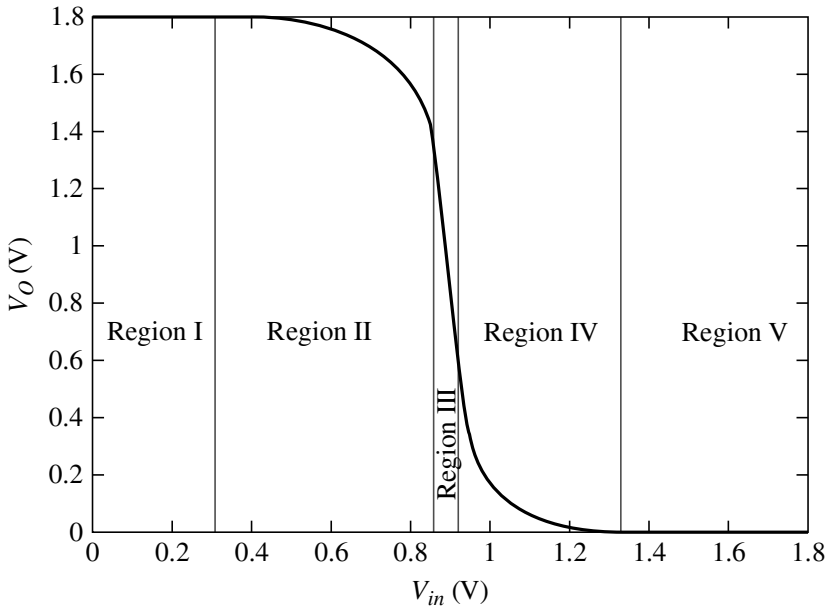


FIGURE 5-4.

V_O versus V_{in} voltage transfer curve (VTC) with five bias states. The input voltage V_{in} is swept from 0 – V_{DD} while V_O is measured.

Inverter designs often seek a symmetric static voltage transfer characteristic (Figure 5-3a), so $V_O = V_{in}$ at about $V_{DD}/2$. To be more exact, a plot of $V_{in} = V_O$ forms a 45° straight line from the origin in Figure 5-3b. The voltage at which $V_{in} = V_O$ is the logic threshold voltage V_M. The intersection of the measured VTC and the 45° line locates V_M, which is $V_M \approx 0.62$ V for this inverter.

The intermediate points in the VTC convey much about the dynamics of the inverter (Figure 5-3). Transistors experience the *off,* saturated, and nonsaturated bias states during the sweep. At $V_{in} = 0$ V, the nMOS transistor is *off* and the pMOS transistor is driven fully into the ohmic state with $V_{GSp} = -1.2$ V. As V_{in} increases, the nMOS transistor remains off until V_{tn} is reached. At that point, the two transistors compete with each other for control of the output voltage. As V_{in} increases further, the pMOS drive weakens and the nMOS drive strengthens. The nMOS transistor now pulls the output voltage lower and eventually to 0 V as V_{in} goes to 1.2 V. At this point the pMOS transistor is *off* since $V_{GSp} = 0$ V.

Figure 5-4 shows an inverter static voltage transfer curve partitioned into five regions corresponding to five distinct transistor bias states. $V_{DD} = 1.8$ V in this example.

These five bias regions in Figure 5-4 are as follows.

Region I. *nMOS off, pMOS ohmic*: This voltage range exists for $V_{in} < V_{tn}$. The nMOS transistor is off, and the pMOS transistor is driven into nonsaturation since $V_{GSp} \approx -V_{DD} < V_{DSp} + V_{tp}$. The pMOS drain node at V_O is pulled up to a logic high V_{DD} through the low impedance of the pMOS channel.

Region II. *nMOS saturated, pMOS ohmic*: When V_{in} goes just above the nMOS threshold voltage ($V_{in} > V_{tn}$), the nMOS transistor barely turns on and is in saturation ($V_{in} < V_O + V_{tn}$). Current now passes through both transistors and V_O drops as V_{in} increases. The pMOS transistor remains in the ohmic state, but with decreasing gate drive.

Region III. *nMOS saturated, pMOS saturated*: When $V_O < V_{in} - V_{tp}$ and $V_O > V_{in} - V_{tn}$, the nMOS and pMOS transistors are both in saturation and the region has a straight line. Since V_O and V_{in} are linearly related, analog amplification occurs here. Small changes in the input waveform are amplified by a value equal to the slope of the straight line. MOS analog circuit designs use this property. It is also good for digital circuits that demand rapid V_O change during logic transitions of V_{in}. A digital goal is to get through the transition region as quickly as possible, and what better way than to have the circuit behave as an amplifier?

Region IV. *nMOS ohmic, pMOS saturated*: As V_{in} increases, it approaches a value such that the difference between V_{in} and V_{DD} is close to the pMOS transistor threshold voltage. This is similar to Region II, but the transistor roles are reversed. The pMOS transistor is in saturation and the nMOS enters nonsaturation.

Region V. *nMOS ohmic, pMOS off*: When V_{in} goes to a logic high voltage, then $V_{in} \gg V_O + V_{tn}$. The nMOS transistor is in its ohmic state pulling the drain voltage to ground, and the pMOS transistor is off.

Voltages slightly less than the logic high or slightly more than logic low voltages are called *weak* logic voltages. Weak logic states are read correctly, but noise margins and gate driving voltage strengths are compromised. The inverter switching threshold voltage (V_M) at which $V_{in} = V_O$ is a unique condition since the theoretical logic state changes at a point as V_O moves through V_M. Inverter voltages in the linear region are not logically defined.

5.3. Noise Margins

The rectangles in Figure 5-5 represent the voltage levels and ranges for the logic high and low as logic gate-A output drives the inputs of logic gate-B. The shaded areas represent a range of logic high and low voltages that logic gates must recognize as valid.

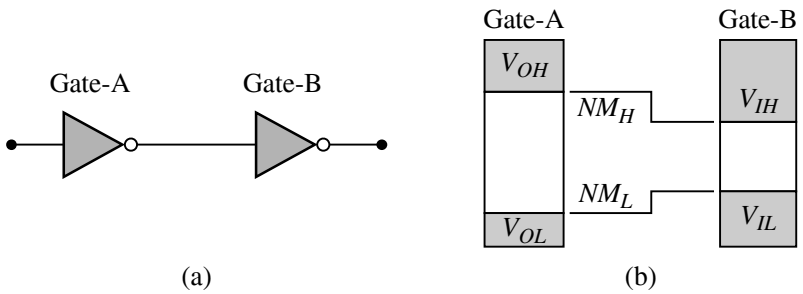


FIGURE 5-5.

(a) Series inverters. (b) Voltage ranges mapped to logic Boolean values.

The following terms are defined:

V_{OL} *Output low voltage*: maximum voltage at a gate output for a logic low to be read correctly by a load gate.

V_{OH} *Output high voltage*: minimum voltage at a gate output for a logic high to be read correctly by a load gate.

V_{IL} *Input low voltage*: maximum input voltage recognized as a logic low.

V_{IH} *Input high voltage*: minimum input voltage recognized as a logic high.

These logic voltages define the noise margin or immunity needed when connecting logic gates. The high and low *noise margins* (NM_H, NM_L) are obtained from these four voltage parameters and are typically specified by the manufacturer. NM_H and NM_L for the high and low logic values are

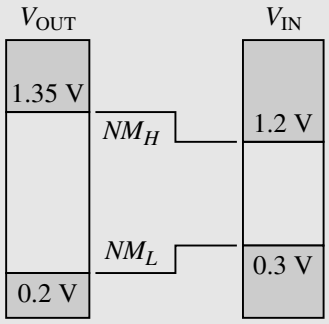
$$\begin{aligned} NM_H &= V_{OH} - V_{IH} \\ NM_L &= V_{IL} - V_{OL} \end{aligned} \tag{5-1}$$

Noise margins must be positive for proper logic operation, and the larger these values, the better the circuit noise immunity. If an input voltage rises and makes NM_H negative, then there is risk of a noise-induced change of logic state. These parameters are an essential measurement during production testing of ICs. Board designers must know that ICs connected to each other are within specification and interface properly.

Noise margins reflect design and manufacturing capability. It is what a manufacturer can guarantee to a customer. Another *NM* definition picks the two points in the VTC where the slope is –1. This is arbitrary but does observe that when the absolute slope is >1, then amplification of V_{in} takes place, and that is not good from a noise standpoint. It is a high-risk region when a logic signal is moved to a point where the slope is greater than one. It is helpful to sketch the *NM* rectangles in Figure 5-5 and label values before solving the problems that follow.

EXAMPLE 5-1

An IC with $V_{DD} = 1.5$ V shows $V_{OH} = 1.35$ V, $V_{OL} = 0.2$ V, $V_{IH} = 1.2$ V, and $V_{IL} = 0.3$ V. Calculate the NM_L and NM_H for this IC.



Sketch the *NM* rectangles

$NM_H = 1.35 - 1.2 = 150$ mV

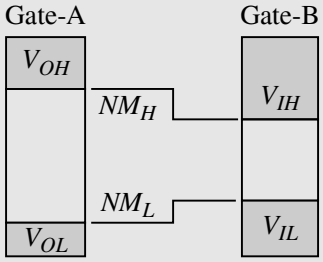
$NM_L = 0.3 - 0.2 = 100$ mV

Self-Exercise 5-1
IC_A and IC_B have $V_{DD} = 2$ V. IC_A is sending data to IC_B and their input–output (I/O) specifications are

$$IC_A: \quad V_{IH} = 1.6 \text{ V}, V_{IL} = 0.4 \text{ V}, V_{OH} = 1.5 \text{ V}, \text{ and } V_{OL} = 0.3 \text{ V}.$$

$$IC_B: \quad V_{IH} = 1.6 \text{ V}, V_{IL} = 0.5 \text{ V}, V_{OH} = 1.5 \text{ V}, \text{ and } V_{OL} = 0.3 \text{ V}.$$

(a) Show calculations as to whether there is a problem.
(b) If there is a problem what should be done?



Answer: **(a)** The problem lies in the high voltage levels. **(b)** Answer intentionally not given.

Self-Exercise 5-2

(a) If $V_{DD} = 1.8$ V, $V_{OH} = 1.75$ V, and $NM_H = 130$ mV, calculate V_{IH}.
(b) If $V_{IL} = 0.35$ V and $NM_L = 180$ mV, calculate V_{OL}.

Answers: **(a)** $V_{IH} = 1.62$ V. **(b)** $V_{OL} = 170$ mV

5.4. Symmetrical Voltage Transfer Curve (VTC)

The aspect ratio W_p/W_n for a symmetric transfer characteristic is found by equating the saturation current for nMOS and pMOS transistors and setting the input voltage equal to $V_M = V_{DD}/2$. Eq. (5-2) gives the W_p/W_n ratio for achieving a symmetrical inverter where $V_M = V_{DD}/2$.

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}\left[\frac{1 - \dfrac{2V_{tn}}{V_{DD}}}{1 - \dfrac{2|V_{tp}|}{V_{DD}}}\right]^2 \tag{5-2}$$

$V_M = 0.5\ V_{DD}$ in Eq. (5-2) when the pull-up and pull-down transistor current drive strengths are equal, but designers may need faster pull-up or pull-down in a given design situation. If $V_M < 0.5\ V_{DD}$ then the nMOS pull-down transistor is stronger than the pull-up,

and the VTC is skewed to the left. If $V_M > 0.5\ V_{DD}$ then the pMOS pull-up is stronger, and the VTC is skewed to the right. In reality, it is difficult to make the VTC exactly symmetrical. Mobility's are uncertain, and W_p is typically not made a small fractional dimension relative to W_n. In our examples, we will pretend that exact symmetry can be attained.

EXAMPLE 5-2

Compute the ratio of nMOS and pMOS transistor width to obtain a symmetric inverter for a 0.18 μm technology in which $\mu_n = 360\ \text{cm}^2/\text{V}\cdot\text{s}$, $\mu_p = 109\ \text{cm}^2/\text{V}\cdot\text{s}$, $V_{tn} = 0.35$ V, $V_{tp} = -0.4$ V, and $V_{DD} = 1.8$ V.

$$\frac{W_p}{W_n} = \frac{360\ \text{cm}^2/\text{V}}{109\ \text{cm}^2/\text{V}} \left[\frac{1 - \dfrac{2(0.35)}{1.8}}{1 - \dfrac{2|-0.4|}{1.8}} \right]^2 = 4.0$$

Self-Exercise 5-3
Derive Eq. (5-2).

Self-Exercise 5-4
If $\mu_n = 360\,\text{cm}^2/\text{V}\cdot\text{s}$, $\mu_p = 109\,\text{cm}^2/\text{V}\cdot\text{s}$, $V_{tn} = 0.35$ V, $V_{tp} = -0.4$ V, and $V_{DD} = 1.5$ V, what W_p/W_n ratio provides the inverter with a symmetrical VTC?

Answer: $\dfrac{W_p}{W_n} = 4.31$

5.5. Current Transfer Curve

The DC power supply *current transfer curve* (ITC) is equally important. Figure 5-6 shows the I_{DD} versus V_{in} characteristic. At $V_{in} < V_{tn}$ in bias Region I, the nMOS transistor is off and no current passes through the circuit. When $V_{in} = V_{DD}$ in Region V, the pMOS transistor is off, and again no current passes from the power supply to ground. Typical inverter current at these long channel quiescent logic levels is in the low pA's and is mostly drain-substrate reverse bias saturation current. Virtually no power is dissipated in the quiescent logic states when the Off-current is this low.

The peak current near $V_{DD}/2$ depends upon transistor strength (the size of the width to length ratio, threshold voltage, and carrier mobility). Both transistors are in the saturated state at the current peak. When an inverter changes logic state, this transient current is wasted power. Peak total power supply currents in large microprocessor designs are many amperes since this is the sum of the transient currents of millions of switching logic gates.

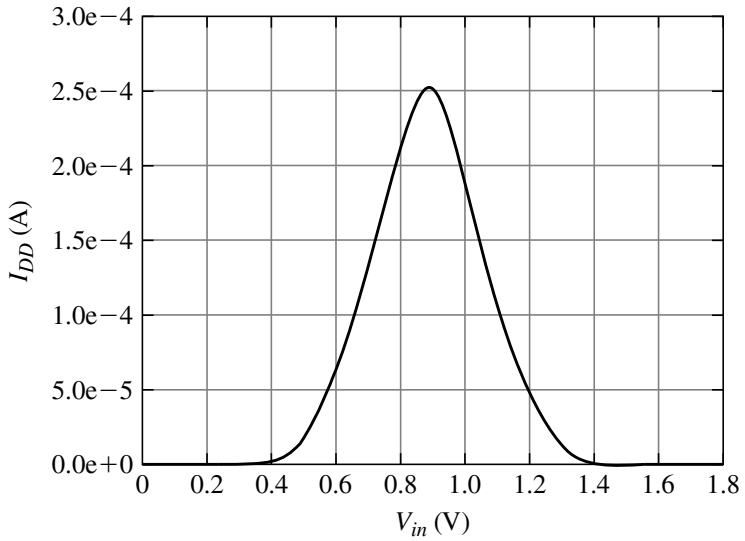


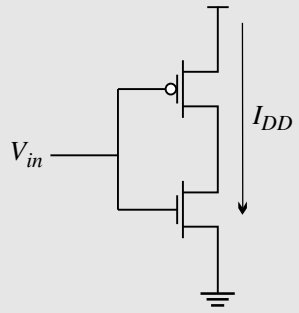
FIGURE 5-6.

Inverter power supply current transfer curve.

Peak current is easy to calculate. The nMOS and pMOS transistors are both in saturation at $V_{DD}/2$ for a symmetrically designed inverter. Either saturation equation for the nMOS and pMOS transistors will solve for the peak current. Examples for symmetrical inverters will illustrate.

EXAMPLE 5-3

If $V_{DD} = 2$ V, $V_{tn} = 0.5$ V, $V_{tp} = -0.5$ V, $K_n = 75\ \mu$A/V^2, $K_p = 50\ \mu$A/V^2, $(W/L)_n = 2$, and $(W/L)_p = 3$, calculate I_{peak}.



The nMOS saturated state equation gives

$$I_{peak} = I_{Dn} = 75\left(\frac{\mu\text{A}}{\text{V}^2}\right)\left(\frac{2}{1}\right)[1-0.5]^2 = 37.5\ \mu\text{A}$$

The pMOS saturated state equation also gives

$$I_{peak} = I_{Dp} = 50\left(\frac{\mu\text{A}}{\text{V}^2}\right)\left(\frac{3}{1}\right)[1-2+0.5]^2 = 37.5\ \mu\text{A}$$

Self-Exercise 5-5
If $V_{DD} = 1.5$ V, $V_{tn} = 0.4$ V, $V_{tp} = -0.4$ V, $K_n = 100\ \mu$A/V^2, and $K_p = 50\ \mu$A/V^2:

(a) The peak current of 35 μA occurs at 0.6 V. What is $(W/L)_n$?
(b) What is the $(W/L)_p$?

Answers: **(a)** $\left(\frac{W}{L}\right)_n = 8.75$, **(b)** $\left(\frac{W}{L}\right)_p = 2.8$

Self-Exercise 5-6
Given an inverter with $V_{tn} = 0.6$ V, $V_{tp} = -0.7$ V, $\mu_n = 1350$ V^2/(V $\cdot$ s), $\mu_p = 350$ V^2/(V $\cdot$ s), and $W_p/W_n = 9$, calculate V_{DD} for a symmetrical CMOS inverter.

Answer: $V_{DD} = 1.78$ V

5.6. Graphical Analysis of VTC

5.6.1. Static Transfer Curves

Figure 5-7 relates the bias state regions with the voltage transfer function and two 45° lines. Eq. (5-3) is the bias boundary condition for the *n*MOS transistor and is a straight line (a) when plotted on Figure 5-7. The lower unity-slope line-*a* defines the *n*MOS saturation and nonsaturation regions. All points on the transfer curve lying above line-*a* represent the *n*MOS transistor in either saturation or the off-state. All points below line-*a* represent

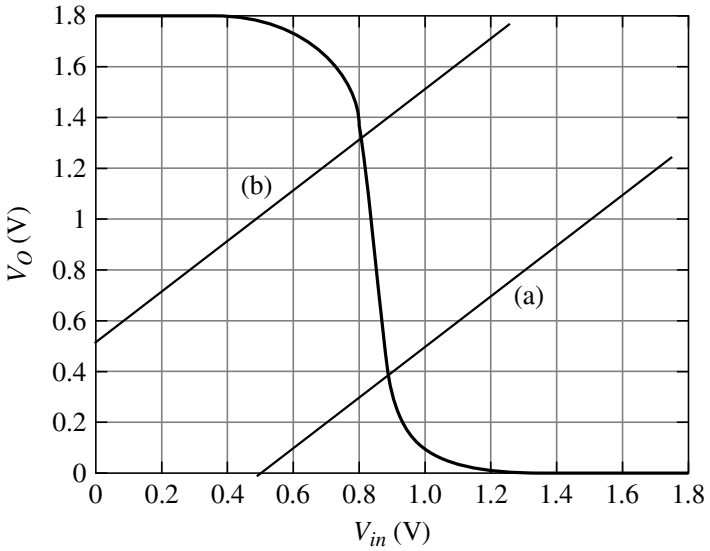


FIGURE 5-7.

Inverter VTC and transistor state.

the *n*MOS transistor in the ohmic state. V_{tn} is located on the x-intercept.

$$V_{GS} = V_{DS} + V_{tn} \tag{5-3}$$

or

$$V_{in} = V_O + V_{tn} \tag{5-4}$$

and

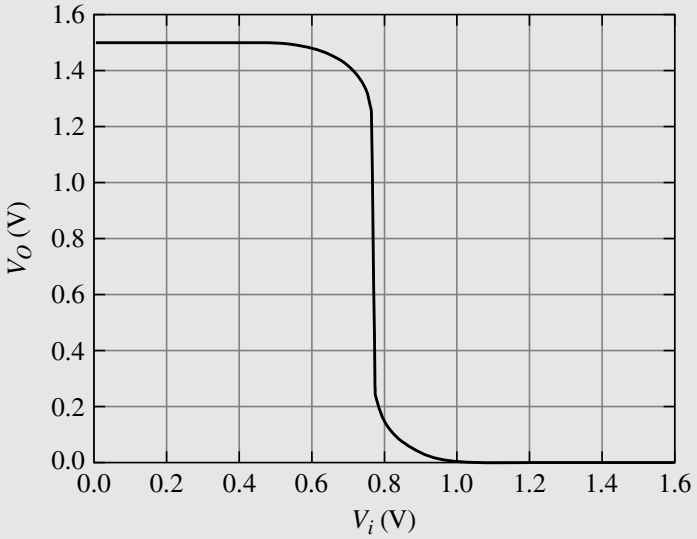
$$V_{tn} = V_{in} \text{ at } V_O = 0$$

A similar derivation leads to the *p*MOS transistor bias boundary line labeled (b) in Figure 5-7 and given in Eq. (5-4). The y-axis intercept is $V_O = -V_{tp}$. The *p*MOS transistor is either saturated or off for all points on the curve below line-*b* and is in the ohmic state above line-*b*. Both transistors are in saturation in the important region between the two lines.

$$V_{in} = V_O + V_{tp}$$
$$V_{tp} = -V_{in} \text{ at } V_O = 0 \tag{5-5}$$

EXAMPLE 5-4

Given a simulated inverter transfer curve. Estimate V_{tn} and V_{tp} using bias line concepts.



CMOS inverter voltage transfer curve.

Put a small mark on the estimated ends of the linear region and draw 45° lines. The threshold values are the intercepts approximately. $V_{tn} \approx 0.52$ V and $V_{tp} \approx -0.43$ V.

Graphical analysis allows visualization of transistor states during logic transitions. The maximum gain region occurs when both transistors are saturated as seen between the two bias lines (a, b) in Figure 5-7. An example emphasizes this thinking.

EXAMPLE 5-5

When V_O switches in an inverter from V_{DD} to 0 V, estimate the fraction of V_{DD} that the nMOS transistor is in saturation. Let $V_{tn} = 0.2\ V_{DD}$, $V_{tp} = -0.2\ V_{DD}$, and $K'_n = K'_p$, where $K'_n = K_n(W/L)_n$, and $K'_p = K_p(W/L)_p$.

We know $I_{Dn} = |I_{Dp}|$ for all the points in the static curve including the point on line-a where the nMOS transistor leaves saturation. At this point both transistors can be treated in the saturation state. This is the transition between Regions III and IV, and we will calculate V_O at that point.

$$K'_n\,(V_{GS} - V_{tn})^2 = K'_p(V_{GS} - V_{tp})^2$$

Substitute for $V_{GS} = V_{in}$, $K'_n = K'_p$, $V_{in} = 0.2 \times V_{DD}$, $V_{in} = V_O + V_{tn}$ and get

$$K'_n\,(V_{in} - V_{tn})^2 = K'_p(V_{in} - V_{DD} - V_{tp})^2$$

$$V_O^2 = V_O^2 - 1.2\ V_{DD}(V_O) + 0.36\ V_{DD}^2$$

$$V_O = 0.3\ V_{DD}$$

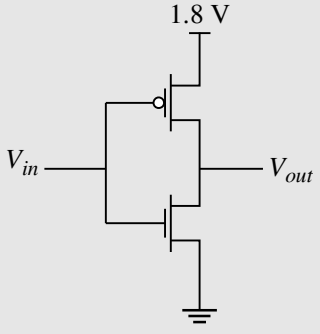
The fraction is

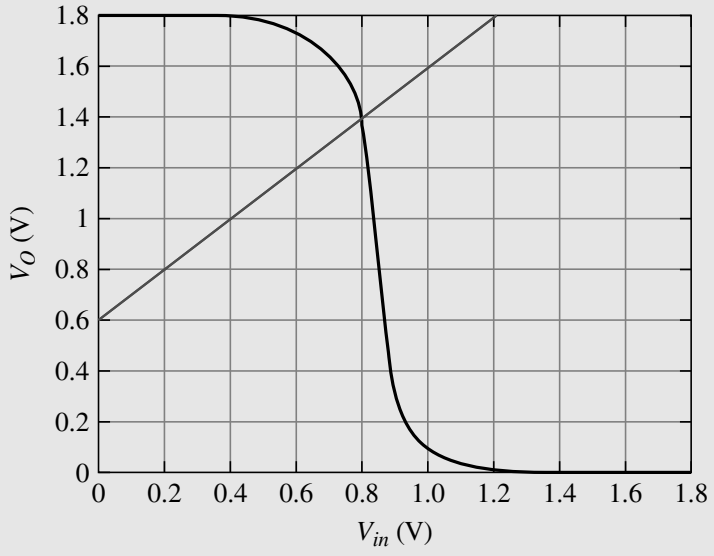
$$\frac{V_{DD} - V_O}{V_{DD}} = 0.7 = 70\%$$

The nMOS is in saturation for about 70% of the transition. This saturation bias is significant when we model the inverter logic transition speed.

EXAMPLE 5-6

If $K_p = 55\mu A$, $V_{in} = 1.0$ V, and $I_{DD} = 15\ \mu$A, and the inverter is symmetrical, what is $(W/L)_p$?





Use the VTC to estimate $V_{tp} \approx 0.6$ V

$$15\,\mu\text{A} = 55\,\mu\text{A}(W/L)_p\,(1.0 - 1.8 + 0.6)^2$$
$$(W/L)_p = 6.8$$

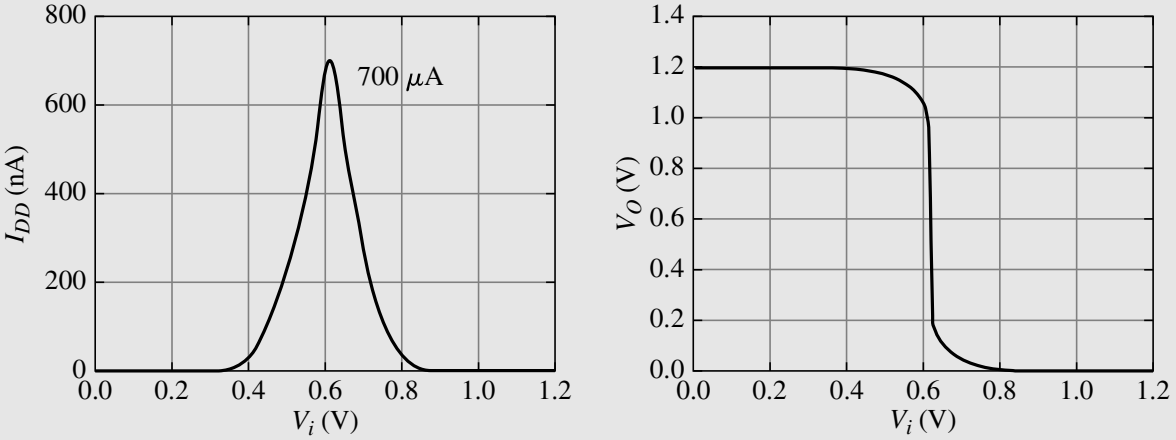
Self-Exercise 5-7

A CMOS inverter has transistor parameters: $K_n\,(W/L)_n = 265\ \mu\text{A/V}^2$, $K_p\,(W/L)_p = 200\,\mu\text{A/V}^2$, $V_{tn} = 0.55$ V, $V_{tp} = -0.63$ V, and $V_{DD} = 2.5$ V. What fraction percentage of the total output voltage swing will the nMOS transistor be in saturation?

Answer: 75.4%

Self-Exercise 5-8

The ITC and VTC are shown for an inverter. If $(W/L)_n = 50$, estimate V_t and solve for $K_n = \dfrac{\mu\varepsilon}{2T_{ox}}$ from the data.



Answer: $K_n \approx 350\,\mu\text{A/V}^2$

Self-Exercise 5-9

A CMOS inverter has transistor parameters $K_n\,(W/L)_n = 265\ \mu\text{A/V}^2$, $K_p\ (W/L)_p = 200\,\mu\text{A/V}^2$, $V_{tn} = 0.55$ V, $V_{tp} = -0.63$ V, and $V_{DD} = 2.5$ V. What fraction of the total output voltage swing will the pMOS transistor be in saturation?

Answer: 71.8%

Self-Exercise 5-10
Estimate the analog voltage gain for the inverter whose transfer curve is in Figure 5-7.

Answer: $A_v \approx -13$

5.6.2. Dynamic Transfer Curves

The voltage transfer curve of Figure 5-4 gave essential inverter information but was swept slowly (static curve). It did not represent the circuit behavior during its rapid transition. The input signal switching time for modern inverters can be tens of picoseconds, and parasitic capacitance of the transistors and the external wiring load alter the phase relation between V_i and V_O. An inverter and its transfer curve phase relation are shown in Figure 5-8 for different input speed transitions, showing that for rapid transitions the drain voltage lags the input gate voltage changes.

The circuit model for the inverter dynamic analysis in Figure 5-8a shows two parasitic capacitances that are important during the transition. C_L represents the combined effects of the drain diffusion region capacitance, interconnect wiring, and a load gate input capacitance. The second capacitance is the input–output capacitance (called the coupling capacitance C_{coup}). It is strongly bias dependent and is the parallel overlapping gate-drain capacitance from the nMOS and pMOS devices.

Figure 5-8b shows simulated transfer curves for static, (1) medium speed, (2) higher speed, and (3) very high-speed input voltage transitions. These curves show hysteresis.

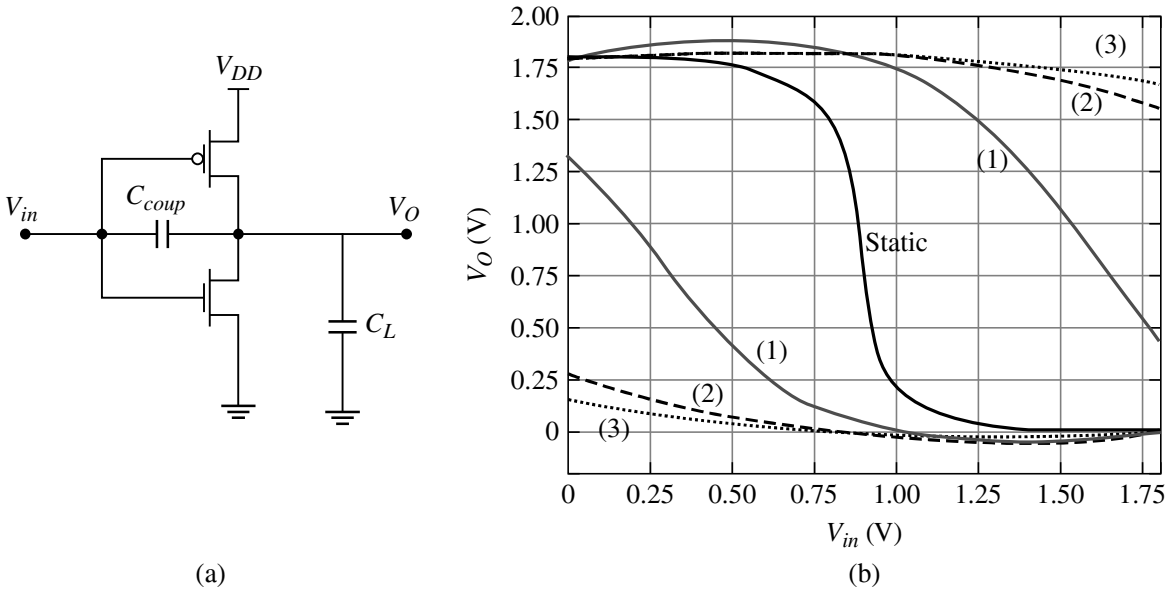


FIGURE 5-8.

(a) Dynamic CMOS inverter circuit model. (b) Transfer curves for output high to low and output low to high for different input ramp speeds.

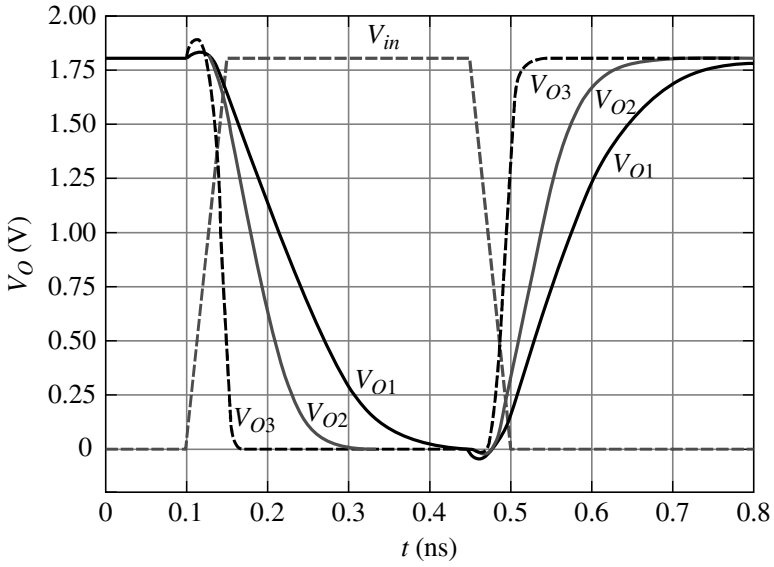


FIGURE 5-9.

Timing responses for different cases for a dynamic inverter transition.

The forward VTCs of V_O are shown in the upper portion of Figure 5-8b, and the reverse transition is shown in the lower portion. Curves (2) and (3) in Figure 5-8b show that the output drain node remains at a relatively high voltage when the gate input has almost completed its low to high transition. The same phenomenon holds when the gate input switches rapidly from high to low. The drain remains in a low voltage state until the input has almost completed its transition. The circuit parasitic capacitance causes this phase relation. A slow transition of the static curve allows time for the drain nodes to exactly follow the input gate voltage in time. Curve (1) is an intermediate case where the output is larger than $V_{DD}/2$ when the input reaches its final value, although it is far from the static transfer curve. These curves are dominantly a function of C_L and the switching speed.

Figure 5-9 plots the output voltage timing responses for different values of C_L when the input transition times are set to a constant rate of change. Curve V_{O3} corresponds to a small output capacitance, and the output voltage is almost zero when the input reaches V_{DD}. This case is similar to the static transfer curve. As the load capacitance increases for curve V_{O2} the output transition time increases. Further increase in load capacitance slows the transition time even more (V_{O1}). In all cases the output voltage initially goes beyond V_{DD} due to overshoot caused by the charge injected from the input through the coupling capacitance C_{coup}. During this period there is a small current from the output node through the pMOS transistor back to the supply terminal.

For high-speed transitions the coupling capacitance C_{coup} tries to maintain its initial voltage difference between the input and the output ($-V_{DD}$ for a low-high input transition and $+V_{DD}$ for a high-low one). But charge is delivered through C_{coup} to node V_O, and C_L cannot respond other than to accept new charge. The charge injection is more rapid than

C_L can move charge through the transistor paths to the rails. The change in output node voltage is $dv = dq/C$. This temporarily drives the output voltage beyond V_{DD} (overshoot) for an input rising transition and below ground for a falling edge (undershoot) (Figure 5-9). Circuit simulators are the best tool to compute the timing waveforms.

5.7. Inverter Transition Speed Model

An exact calculation of the propagation delay of an inverter requires complex differential equations. We will derive a simple model assuming that the transistor is an ideal current source, i.e. the transistor is always in saturation during the transition. The current source I_o in Figure 5-10a represents the pMOS transistor in saturation since that bias state dominates the transition rise time and C_L is the load capacitance. The nMOS transistor is assumed off for this simple model of rise time. The saturated state model for a pMOS pull-up is

$$I_O = I_{Dp} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{tp})^2 \tag{5-6}$$

where $C_{ox} = \dfrac{\mu\varepsilon}{T_{ox}}$

The capacitance expression for current, voltage, and time is

$$i(t) = C_L \frac{dV(t)}{dt}$$

If $i(t) = I_O$ (a constant current) and we approximate $dv(t)/dt = \Delta v(t)/\Delta t$, then

$$\Delta V(t) = \frac{I_o}{C_L}\Delta t \tag{5-7}$$

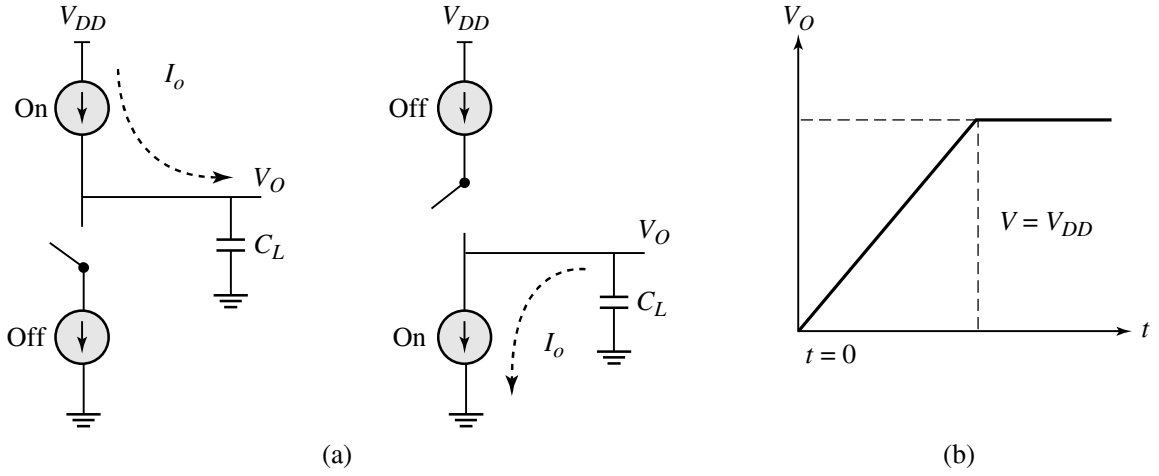


FIGURE 5-10.

(a) Circuit model to estimate rise and fall delays in a CMOS inverter. (b) Capacitance voltage response to constant current.

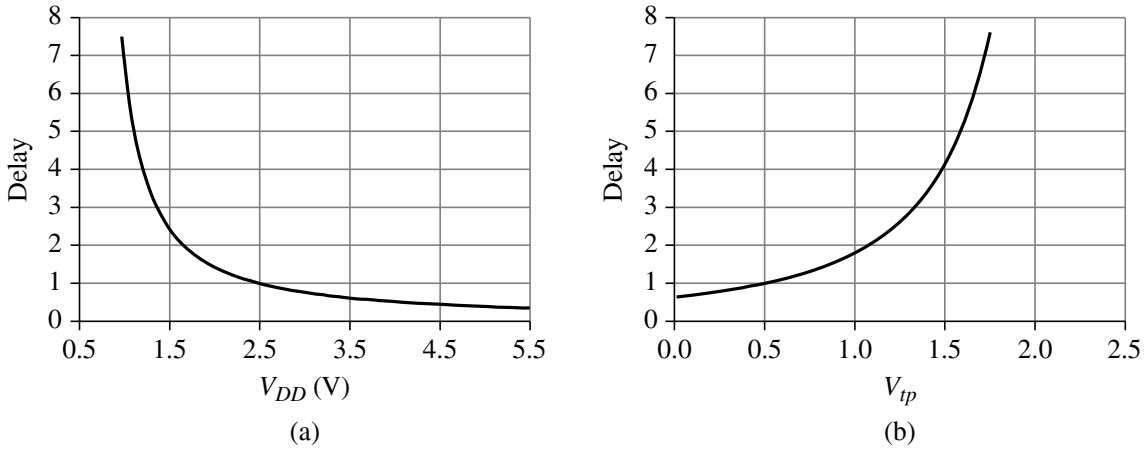


FIGURE 5-11.

(a) Normalized delay versus supply voltage for a constant V_t for the model in Eq. (5-9). (b) Normalized delay versus threshold voltage for a constant V_{DD} for the model in Eq. (5-9).

If Δt is the delay or rise time τ_r in Figure 5-10b for the signal to rise to $\Delta V(t) = V_{DD}$ then Eq. (5-7) is rewritten as

$$\tau_r = \frac{C_L V_{DD}}{I_o} \tag{5-8}$$

Substituting Eq. (5-6) into Eq. (5-8) with $V_{GS} = V_{DD}$ gives

$$\tau_r = C_L V_{DD} \left(\frac{2L}{W \mu_p C_{ox}} \right) \frac{1}{(-V_{DD} - V_{tp})^2} \tag{5-9}$$

Eq. (5-9) shows that time delay is asymptotically related to the difference in V_{DD} and the threshold voltage. Figure 5-11a plots the time delay versus V_{DD} for $C_L = 20$ fF, $K_p = 75\ \mu\text{A/V}^2$, $V_{tp} = -0.5$ V, and $W/L = 2$. Time delay asymptotically approaches infinity as V_{DD} approaches V_{tp}. The plot also shows a significant property when $V_{DD} \gg |V_{tp}|$. The change in transition delay time is small for small variations in the power supply level. If V_{DD} drops from 5 V to 4.5 V, the change in delay is small. This is an important noise protection since power supply and GND levels are noisy from clock to clock period.

The result is similar if V_t varies for a fixed V_{DD}. Figure 5-11b is similar to Figure 5-10a, but with time delay plotted against V_t *for* $V_{DD} = 2.5$ V. The plots show that circuit delay is very sensitive to the difference in V_{DD} and V_t in certain regions of the curves.

A similar derivation for the pull-down delay or fall time τ_f using the *n*MOS transistor gives

$$\tau_f = C_L V_{DD} \left(\frac{2L}{W \mu_n C_{ox}} \right) \frac{1}{(V_{DD} - V_{tn})^2} \tag{5-10}$$

EXAMPLE 5-7

(a) An inverter has $C_L = 100$ fF and a current drive $I_O = 400\,\mu$A. What value of V_{DD} is required to hold the signal rise time to 300 ps?

Use Eq. (4.7)

$$V_{DD} = \frac{\tau_r \times I_O}{C_L} = \frac{(300\text{ ps})(400\ \mu\text{A})}{100\text{ fF}} = 1.2\text{ V}$$

(b) If $V_{DD} = 1.5$ V, what is τ_r?

$$\tau = \frac{(100\,\text{fF})(1.5\,\text{V})}{400\ \mu\text{A}} = 375\,\text{ps}$$

In this case, τ_r increased to 375 ps because the transition output voltage amplitude increased with V_{DD} increase. The example assumed that the drive current was constant.

EXAMPLE 5-8

Given that $C_L = 10$ fF, $\mu\varepsilon/2T_{ox} = 59\ \mu\text{A/V}^2$, $W/L = 6$, and $V_{DD} = 2.3$ V, initially $V_{tn} = 0.6$ V. If V_{tn} is reduced to 0.2 V, what is the ratio decrease in fall time?

You can substitute the values into Eq. (5-9) and take the ratio or divide Eq. (5-9) by itself substituting $V_t = 0.6$ V and $V_t = 0.2$ V. You get

$$\frac{\tau_f\,(V_t = 0.6\text{ V})}{\tau_f\,(V_t = 0.2\text{ V})} = \frac{(2.3 - 0.2)^2}{(2.3 - 0.6)^2} = 1.526$$

Self-Exercise 5-11

A pMOS transistor has $V_{tp} = -0.5$ V, $K_p = 70\ \mu\text{A/V}^2$, $(W/L)_p = 4$, and $V_{DD} = 2$ V. Estimate the rise time delay for an inverter with a load of 100 fF.

Answer: $\tau_r = 317.5$ ps

Self-Exercise 5-12

An nMOS transistor has $V_{tn} = 0.35$ V, $K_n = 120\ \mu\text{A/V}^2$, $(W/L)_n = 3$, and $V_{DD} = 1$ V. Estimate the 90% fall time delay (0.9 V_{DD}) for an inverter with a load of 10 fF.

Answer: $\tau_f = 59.2$ ps

Self-Exercise 5-13
Transistors in a CMOS inverter have $C_L = 50$ fF, $V_{tn} = 0.4$ V, $V_{tp} = -0.4$ V, $K_n = 100\ \mu\text{A/V}^2$, $K_p = 50\ \mu\text{A/V}^2$, and $V_{DD} = 1.5$ V. What should the W/L ratios be for both transistors if the circuit is to have equal rise and fall times of 200 ps?

Answer: $\left(\frac{W}{L}\right)_n = 3.1$

$\left(\frac{W}{L}\right)_p = 6.2$

The time delay τ is actually slower than calculated by the simple model of a single transistor pulling the output node up or down. One reason is that the pMOS and nMOS transistors as a pair siphon charge from each other that is intended for C_L. While the pMOS is trying to charge C_L, the nMOS bleeds some of that charge to ground thus lengthening the change of state. However, the simple model does identify the major parameters that control logic transitions.

5.8. CMOS Inverter Power

An inverter has dynamic and static energy components. Dynamic dissipation has two major components: (1) the charge–discharge of the logic gate load capacitance (transient component); and (2) the short-circuit current from the supply to ground created during the transition (Figure 5-6). Static dissipation for long channel transistors is due mainly to reverse bias drain-substrate (well) *pn* junction leakage current from transistors in the off-state. The dynamic power calculation requires computation of transient and short-circuit components. This is typically small for a single logic gate, but it can be significant when switching power includes millions of gates. Off-state leakage is a major concern for modern, very short channel transistors, but that is a topic for an advanced course.

5.8.1. Transient Power

The dynamic power (P_d) to charge and discharge a capacitance C_L for a clock period T_{clk} is

$$P_d = \frac{1}{T_{clk}} \int_0^{T_{clk}} i_{load}(t) v_o(t) dt \tag{5-11}$$

In one period, the output voltage changes from 0 V to V_{DD} and then from V_{DD} to 0 V. Eq. (5-11) is rewritten using

$$i_{load}(t) = \frac{dq}{dt} = C\frac{dv_{load}}{dt} = C\frac{dv_o}{dt}$$

and

$$P_d = \frac{1}{T_{clk}}\left[\int_0^{V_{DD}} C_L v_o dv_o + \int_{V_{DD}}^{0} C_L (V_{DD} - v_o) dv_o\right] \tag{5-12}$$

giving

$$P_d = \frac{C_L V_{DD}^2}{T_{clk}} = C_L V_{DD}^2 f_{clk} \tag{5-13}$$

Eq. (5-13) shows that reducing the output capacitance, the supply voltage, or the operating frequency will lower transient power. Since the power dependence on the supply voltage is quadratic, lowering V_{DD} is more efficient for reducing power dissipation than the other two parameters. Notice Eq. (5-13) assumes an up and down transition in one clock period. If a single transition occurred during one clock period, then P_d is reduced by half. A single transition is typical for combinational logic circuits. A double transition per clock period is typical of logic gates in the clock timing networks. Eq. (5-13) is often used as an estimate of gross IC power despite inaccuracies as to how many gates are double transitioning, or what fraction of the gates actually switch at all in a given clock period.

When a clock pulse drives the registers in an integrated circuit, a single switching occurs in the combinational logic load gates. However, not every logic gate in the IC switches. Typically, about 5–30% of the total combinational logic gates in an IC switch and draw dynamic power in a single clock pulse. We define an activity coefficient α as the fraction of logic gates in the IC that are expected to change state (switch) on a clock pulse. The power equation Eq. (5-13) for a single transition period becomes

$$P_d = \frac{1}{2}\alpha C_L V_{DD}^2 f_{clk} \tag{5-14}$$

$\alpha = 1$ in a typical clock network, but some networks in the IC are intentionally gated off from the clock to reduce power, and their activity coefficient is zero.

EXAMPLE 5-9

Given that a gated IC clock network has $V_{DD} = 1.5$ V, $\alpha = 0.84$, a total load capacitance $C_L = 5$ nF, and $f_{clk} = 2.6$ GHz, what is the power dissipation in the clock network?

$$P_d = (1)(0.84)(5 \times 10^{-9})(1.5^2)(2.6 \times 10^9) = 24.57 \text{ W}$$

Self-Exercise 5-14

For a combinational logic gate, $\alpha = 0.2$, $C_L = 150$ fF, $V_{DD} = 2$ V, and $f_{clk} = 2$ GHz.

(a) Calculate the circuit power dissipation.
(b) Calculate the power dissipation if $V_{DD} = 1.5$ V.

Answer: **(a)** $P_d = 120\ \mu$W. **(b)** $P_d = 67.5\ \mu$W

Self-Exercise 5-15
An IC has six combinational logic blocks driven by a clock. Each block has a 750 pF load, $V_{DD} = 1.1$ V, and $f_{clk} = 3$ GHz. How many blocks must be turned off at any instant if the total power of the IC clock network is to be less than 5 W. Use the gross assumption that all the logic gates make either a single charge or discharge during a clock cycle.

Answer: Power per block is 1.36 W so only three blocks can be on at one time.

Self-Exercise 5-16
V_{DD} goes from 1.2 V to $\frac{2}{3}V_{DD}$ in a circuit with $\alpha = 1$.

(a) Calculate the power dissipated in a combinational logic gate for both V_{DD} values when $C_L = 10$ nF, and $f_{clk} = 1.5$ GHz.
(b) Calculate the power dissipated in a clock logic gate when $C_L = 10$ nF, $V_{DD} = 1.2$ V, and $f_{clk} = 1.5$ GHz.

Answer: **(a)** $P = 4.8$ W, $P = 10.8$ W. **(b)** $P = 21.6$ W

5.8.2. Short-Circuit Power

Both transistors conduct when the input is changing, and the transition voltage is between V_{tn} and $V_{DD} - |V_{tp}|$. This creates a circuit current path from V_{DD} to ground (Figure 5-6) that may generate from 5 to 30% of the total switching power. This short-circuit power component depends on device current strength, input transition time, and output capacitance. If the transition time is long, then CMOS short-circuit current is active for a longer time. The exact computation of short-circuit current is complex so we present an approximation.

Consider a symmetric inverter (i.e., $K'_n = K'_p$, and $V_{tn} = -V_{tp}$) with no output load and an input voltage transition having equal rise and fall times. The time interval when both transistors conduct is from t_1 to t_3 in Figure 5-12. During the interval $t_1 - t_2$ the short circuit current increases from zero to its maximum value I_{max} and the nMOS transistor is saturated. Its drain current is

$$I_D = K_n \frac{W}{L}(V_i - V_{tn})^2 \quad \text{for } 0 < I < I_{max}$$

Since the inverter was assumed symmetric with no load, the maximum current occurs at $V_{in} = V_{DD}/2$ and its shape is symmetric along the vertical axis at $t = t_2$. We compute a mean current by integrating from $t = 0$ to $t = T$ and dividing by the period T. There are

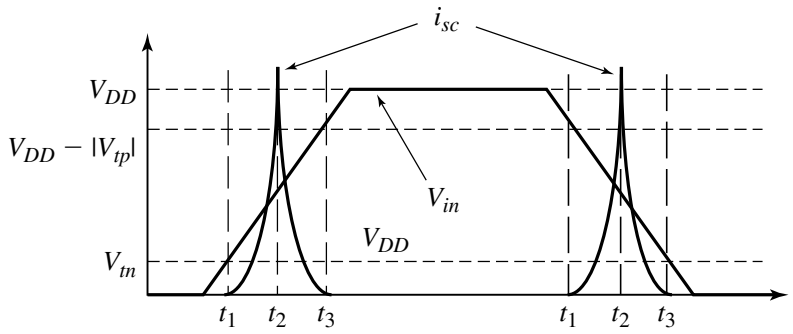


FIGURE 5-12.

A simplified view of the short-circuit current contribution over one clock period.

four equal area current segments to integrate in Figure 5-12 over the whole period T.

$$I_{mean} = \frac{1}{T}\int_0^T I(t)dt = \frac{4}{T}\int_{t_1}^{t_2} K_n \frac{W}{L}\,(V_{in}(t) - V_{tn})^2\,dt \tag{5-15}$$

If the input voltage is a linear ramp of duration τ

$$V_{in} = \frac{V_{DD}}{\tau}t \tag{5-16}$$

t_1 and t_2 are given by

$$t_1 = \frac{V_t}{V_{DD}}\tau \quad \text{and} \quad t_2 = \frac{\tau}{2} \tag{5-17}$$

Substituting Eqs. (5-16 and 5-17) into Eq. (5-15)

$$I_{mean} = K_n\left(\frac{W}{L}\right)\frac{1}{T}\int_{\frac{V_T}{V_{DD}}\tau}^{\frac{\tau}{2}} \left(\frac{V_{DD}}{\tau}t - V_{tn}\right)^2 dt \tag{5-18}$$

This integral is of the type $\int x^2 dx$ with $x = (V_{DD}/\tau)t - V_t$ so the result is

$$I_{mean} = \frac{1}{6}K_n\left(\frac{W}{L}\right)\frac{1}{V_{DD}}\,(V_{DD} - V_{tn})^3\,\frac{\tau}{T} \tag{5-19}$$

Finally the power contribution is given by

$$P_{sc} = V_{DD}\,I_{mean} \tag{5-20}$$

EXAMPLE 5-10

What is the short-circuit power in an inverter if $V_{DD} = 2$ V, $V_{tn} = -V_{tp} = 0.5$ V, $T = 500$ ps, $f_{clk} = 2$ GHz, $K_n = 140\ \mu$A/V^2, $W/L = 2$, and the pulse rise and fall times are 100 ps?

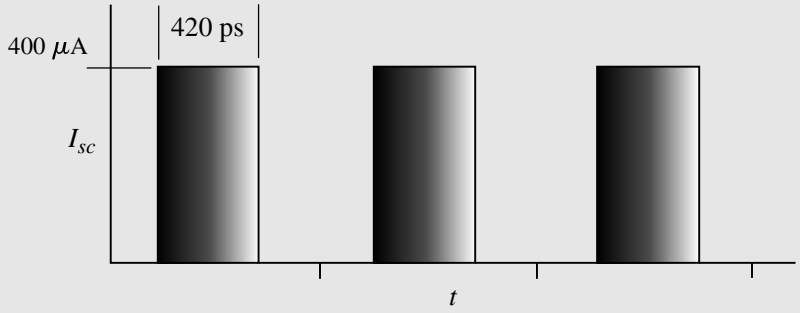
$$I_{mean} = \left(\frac{1}{6}\right)(140\ \mu\text{A})\left(\frac{2}{1}\right)\left(\frac{1}{2\text{V}}\right)(2 - 0.5)^3\left(\frac{100\text{ ps}}{500\text{ ps}}\right) = 15.75\ \mu\text{A}$$

so

$$P_{sc} = 2\text{ V} \times 15.75\ \mu\text{A} = 31.5\ \mu\text{W}$$

Self-Exercise 5-17

The short-circuit current pulses in a CMOS inverter are modeled as rectangular pulses of 400 μA peak and 420 ps width. The clock frequency is 800 MHz and $V_{DD} = 1.2$ V. Calculate the short circuit power dissipation using Eq. (5-18).



Answer: $P_{sc} = 161.3\ \mu$W

5.8.3. Quiescent Leakage Power

The current transfer curve in Figure 5-6 showed that the quiescent current at the two logic states (0, V_{DD}) was quite low in the low nA range. Low leakage transistors lead to low power ICs. However, as the transistors become smaller, other leakage mechanisms kick in and the leakage can increase by orders of magnitude leading to ICs with DC leakages ranging from 20 to 40 amps in high-frequency ICs such as in Internet servers. It is called short channel leakage. Battery-operated ICs cannot stand this and use many tricks to bring the current leakage under control. This is a huge problem and is beyond this introductory course.

5.9. Power and Power Supply Scaling

The ratio of V_{tn} to V_{DD} impacts several inverter properties. The saturated current equation is

$$I_D = \frac{\mu_n \varepsilon}{2T_{ox}}\frac{W}{L}(V_{GS} - V_{tn})^2 \tag{5-21}$$

When $V_{GS} = V_{DD}$ for logic circuits, Eq. (5-21) becomes

$$I_D = \frac{\mu_n \varepsilon}{2T_{ox}} \frac{W}{L} (V_{DD} - V_{tn})^2 \tag{5-22}$$

When V_{DD} decreases, several trade-offs occur:

- The voltage difference in the parenthesis (the gate overdrive) is smaller so the current drive is less, and transistor speed is degraded. Load capacitance is charged and discharged slower.
- As V_{DD} drops, the the logic voltage traverses a smaller range giving a slight speed compensating feature.

When $V_{DD} < (V_t - V_{tp}) \approx |2V_t|$ the transition slows, but interestingly only one transistor is on at a time. There is essentially no transient current spike. Figure 5-13 shows a transfer curve measurement at $V_{DD} = 1$ V and $V_{DD} = 0.5$ V for transistors with thresholds on the order of 0.35 V. There is no current spike for the $V_{DD} = 0.5$ V measurement since $V_{DD} < V_{tn} + |V_{tp}|$. The power reduction for this condition is large.

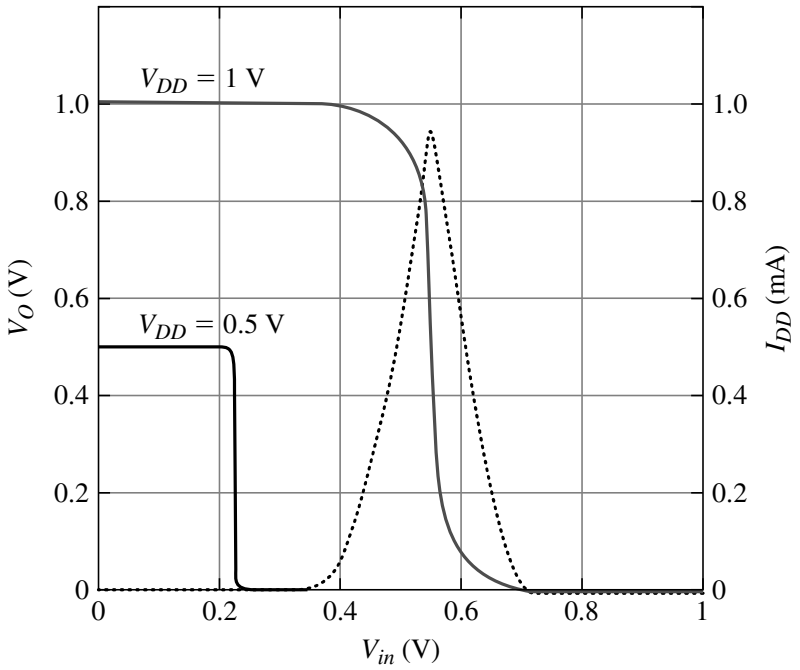


FIGURE 5-13.

Inverter transfer curves at two V_{DD} values. Notice the absence of a short-circuit current spike for $V_{DD} = 0.5$ V where V_{in} was swept from 0.5 V to 0 V. You can understand this low power operation if you sketch an inverter with $V_{DD} = 0.5$ V. Follow both transistor's on–off action as V_{in} goes from 0 V to 0.5 V.

Low-power, battery-operated products such as electronic watches and medical implants use this technique.

EXAMPLE 5-11

$V_{tn} = 0.4$ V and $K'_n = 400\ \mu$A/V^2. What is the instantaneous peak power dissipation in a symmetrical inverter during a switching event for (a) $V_{DD} = 2$ V, and (b) $V_{DD} = 1.5$ V?

(a) $$I_D = 400\,\mu\text{A}\left(\frac{2.0\,\text{V}}{2} - 0.4\right)^2 = 144\ \mu\text{A}$$

$$P_{sc} = (1\,\text{V})(144\,\mu\text{A}) = 144\ \mu\text{W}$$

(b) $$I_D = 400\ \mu\text{A}\left(\frac{1.5\,\text{V}}{2} - 0.4\right)^2 = 49\ \mu\text{A}$$

$$P_{sc} = (0.75\,\text{V})(49\,\mu\text{A}) = 36.75\ \mu\text{W}$$

The power and peak current show a marked reduction with decrease in V_{DD}.

Self-Exercise 5-18

An inverter is driven by $V_{DD} = 1.0$ V pulses.

(a) What is the mean drain current limit to keep power dissipation to $<1\ \mu$W per pulse.
(b) If 10^5 inverters on a chip switch simultaneously for the values in part (a), what is the mean current of the chip over one clock period.

Answers: **(a)** $I_{mean} = 1\ \mu$A. **(b)** $I_{mean} = 100$ mA

Self-Exercise 5-19

The parameters for a symmetrical inverter are $V_{tn} = 0.6$ V, $V_{tp} = -0.6$ V, $K_n = 100\ \mu$A/V^2, $K_p = 50\ \mu$A/V^2, off-state leakage current is 1 pA, $(W/L)_n = 2$, and $(W/L)_p = 5$. Compare peak current and peak power at

(a) $V_{DD} = 2$ V
(b) $V_{DD} = 1.4$ V
(c) $V_{DD} = 1.0$ V

Answers: **(a)** $I_{peak} = 32\,\mu$A, $P_{peak} = 32\,\mu$W. **(b)** $I_{peak} = 2\,\mu$A, $P_{peak} = 1.4\,\mu$W. **(c)** $I_{peak} = 1$ pA, $P_{peak} = 0.5$ pW

Self-Exercise 5-20
Figure 5.13 showed an inverter voltage transfer curve for $V_{DD} = 0.5$ V. The curve actually is for a reverse sweep of V_i from 0.5 V to 0 V.

(a) Draw the transfer curve if the sweep for V_i goes from 0 V to 0.5 V. Approximate this forward sweep estimating V_{tp} from the 1.0 V VTC, and assume that $V_{tn} = -V_{tp}$.
(b) What is the width of the hysteresis zone?

Answer: **(b)** 0.26 V

5.10. Sizing Inverter Buffers to Drive Large Loads

A problem exists when a small logic gate must drive a large capacitive load C_L. A fast charge–discharge of a large load capacitance requires a large W/L of the driving transistors. However, a large W/L is defeating, since its larger transistor gate area increases its own logic input capacitance. Working backward, that would cause all preceding logic gates to have ever larger W/L ratios. A better solution exists.

Instead, one approach for driving large loads at high speed uses successively larger channel widths in a cascade of inverters to sufficiently increase the current drive of the last stage. A circuit driving a large load is commonly known as a buffer, and a circuit designed with successively larger inverters is known as a tapered buffer (Figure 5-14). When the area of each stage increases by the same factor the circuit is called a fixed tapered buffer.

The fixed tapered buffer structure was proposed by Linholm in 1975 [1]. He used a simple capacitance model making the W/L of a stage proportional to the size of the input capacitance of the next stage, while the area of each inverter was proportional to the channel width of the transistors. The overall buffer delay was optimized by minimizing the delay of each stage.

Let each succeeding stage in the buffer in Figure 5-14 have transistor widths larger than the previous one by a scale factor α. The first inverter is the smallest with an input

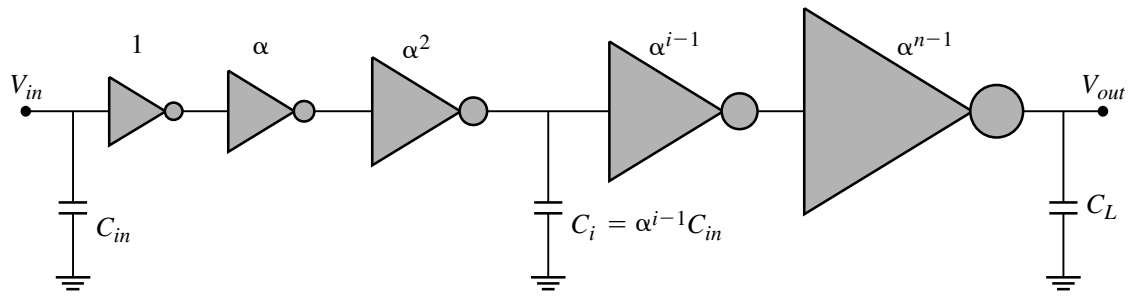


FIGURE 5-14.

Tapered buffer structure.

capacitance C_{in}, while the i-th stage has an input capacitance given by

$$C_i = \alpha^{i-1} C_{in} \quad i = 1, 2, \ldots, n$$

The number of stages n is computed from

$$C_L = \alpha^n C_n$$

then

$$\alpha^n = \frac{C_L}{C_{in}}$$

and

$$n = \frac{\ln\left(\frac{C_L}{C_{in}}\right)}{\ln \alpha} \tag{5-23}$$

α is computed by optimizing the delay. Assuming that the delay of the first stage driving an identical one is τ_0, the delay of the i-th stage is

$$t_{di} = \alpha \tau_0 \quad i = 1, 2, \ldots, n$$

The global delay of the n stages is

$$t_d = \sum_{i=1}^{n} t_{di} = n\alpha\tau_0$$

giving

$$t_d = \ln\left(\frac{C_L}{C_{in}}\right) \frac{\alpha}{\ln \alpha} \tau_0 \tag{5-24}$$

Differentiating (5-24) with respect to α and equating to zero, gives the optimum α_{opt} as

$$\alpha_{opt} = e \approx 2.7$$

while the optimum number of stages n_{opt} is

$$n_{opt} = \ln\left(\frac{C_L}{C_{in}}\right) \tag{5-25}$$

This section seeks to impress that care must be taken in a design when a logic gate drives a large capacitance. This occurs when an IC drives large capacitive loads such as an off-chip board capacitance or on-chip bus lines.

EXAMPLE 5-12

How many buffer stages are need to optimally drive a 1 pF load if the driving gate has an input capacitance of $C_{in} = 25$ fF?

$$n = \ln\left(\frac{C_L}{C_{in}}\right) = \ln\left(\frac{1\,\text{pf}}{25\,\text{fF}}\right) = 3.7$$

Therefore, a total of four buffer stages are needed.

Self-Exercise 5-21

An IC with a tapered buffer drives a load capacitance on a board that is 100 pF. The input capacitance of the logic gate originating the signal is 100 fF, and that gate has $W/L = 4$.

(a) How many buffer gates are required to optimally drive that load using the fixed tapered buffer model?

Answer: $n = 6.9$

Seven total stages are needed. We must insert five tapered stages between the original gate and the output driver.

(b) Write the equation that predicts the W/L ratio of the final buffer in terms of the scaling factor and the originating gate W/L

(c) What is the W/L ratio of the final output buffer driver to the board?

Answer: $W/L = 1{,}614$

Self-Exercise 5-22

A tapered buffer design has an input capacitance of 20 fF and a load capacitance of 5 pF.

(a) What is the required number of buffer stages to minimize the propagation delay?

(b) If the propagation delay of the first stage is 1.5 ns, what is the overall delay?

Answers: **(a)** $n_{opt} = 5.52 \Rightarrow 6$ stages. **(b)** $T_d = 24.5$ ns

5.11. Summary

This chapter examined detailed electronic properties of the inverter. The inverter properties align with NAND, NOR, and other multi-input logic gates studied in the next chapter. Static and dynamic transfer curves explain much of the speed and power behavior of integrated circuits. Tapered buffers are commonly used in design to match small logic gate drive to larger high input capacitance load gates. The next chapter expands these concepts to show how the inverter leads to multi-input logic gates.

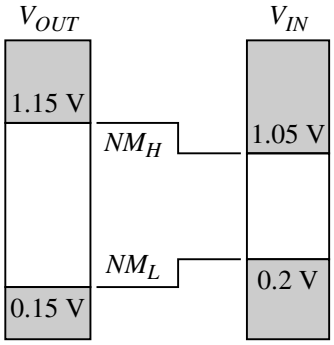
References

[1] F. A. Linholm IEEE J. Solid State Circuits, SC-10, 2, pp. 106–109, April 1975.

Exercises

Inverter Static Voltage Characteristics

5-1. A CMOS inverter has $V_{DD} = 1.2$ V. $V_{OH} = 1.15$ V, $V_{OL} = 0.15$ V, $V_{IH} = 1.05$ V, and $V_{IL} = 0.2$ V. Calculate NM_H, NM_L, and draw the noise margin map with appropriate labels of numbers.



5-2. A logic gate noise margin parameters are $V_{IH} = 1.6$ V, $V_{IL} = 0.3$ V, $V_{OH} = 1.7$ V, and $V_{OL} = 0.2$ V.

(a) Calculate NM_H.

(b) Calculate NM_L.

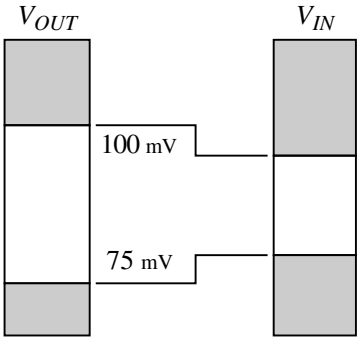
(c) The input voltage is down to 1.7 V and a negative 50 mV noise spike appears. What happens to the circuit fidelity?

(d) The input voltage is down to 1.7 V and a negative 150 mV noise spike appears. What happens to the circuit fidelity?

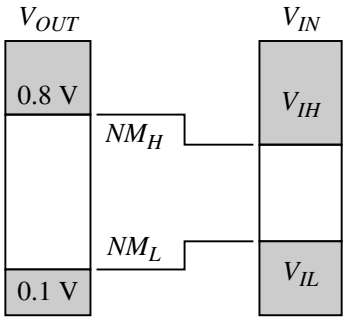
5-3. Given the logic gate noise margins: $NM_H = 100$ mV, $NM_L = 75$ mV, and $V_{DD} = 2$ V.

(a) If $V_{IH} = 1.75$ V, what is V_{OH}?

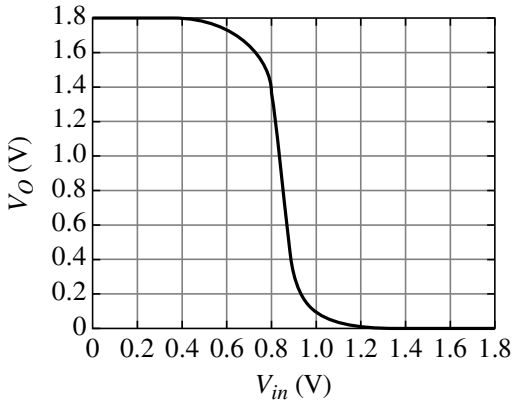
(b) If $V_{IL} = 0.3$ V, what is V_{OL}?



5-4. A CMOS inverter uses $V_{DD} = 0.9$ V. $V_{OH} = 0.8$ V, and $V_{OL} = 0.1$ V. If the noise margins must be 20% of V_{DD}, what are V_{IL} and V_{IH}? Draw the noise margin map and label.

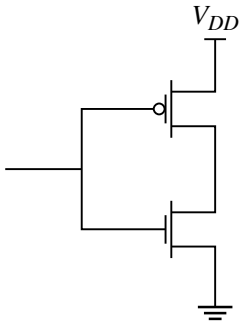


5-5. Graphically determine the change in logic threshold of the CMOS inverter transfer curve in the figure if the curve shifts 0.2 V to the right in the midregion.



5-6. **(a)** Design the W_p/W_n ratios of a CMOS inverter for symmetrical static voltage transfer characteristic. $\mu_n = 1400$ cm^2/V · s, $\mu_p = 500$ cm^2/V · s, $V_{tn} = 0.35$ V, $V_{tp} = -0.35$ V, and $V_{DD} = 1.3$ V.

(b) Redesign if $V_{tp} = -0.45$ V.



5-7. An inverter with a symmetrical voltage transfer curve has a restriction that $W_p/W_n = 4.6$. $V_{DD} = 1.2$ V, $\mu_n = 1530\,\text{cm}^2/\text{V}\cdot\text{s}$, $\mu_p = 540$ $\text{cm}^2/\text{V}\cdot\text{s}$, and $V_{tp} = -0.4$. What must V_{tn} be set to satisfy this condition?

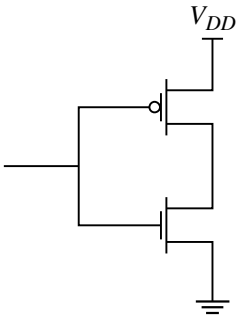
5-8. A CMOS inverter has transistor parameters: $K_n(W/L)_n = 100\ \mu\text{A/V}^2$, $K_p(W/L)_p = 300\ \mu\text{A/V}^2$, $V_{tn} = 0.7$ V, $V_{tp} = -0.75$ V, and $V_{DD} = 2.5$ V. What fraction of the total output voltage swing will the *n*MOS transistor be in saturation?

5-9. A CMOS inverter has its *n*MOS transistor in nonsaturation and its *p*MOS transistor in saturation. Given $K_n = 50\ \mu\text{A/V}^2$, $K_p = 25\ \mu\text{A/V}^2$, $V_{tn} = 0.5$ V, $V_{tp} = -0.6$ V, $(W/L)_n = 2$, $(W/L)_p = 4$, $I_{DD} = 11\ \mu$A, and $V_{DD} = 2$ V, calculate the inverter output voltage V_O.

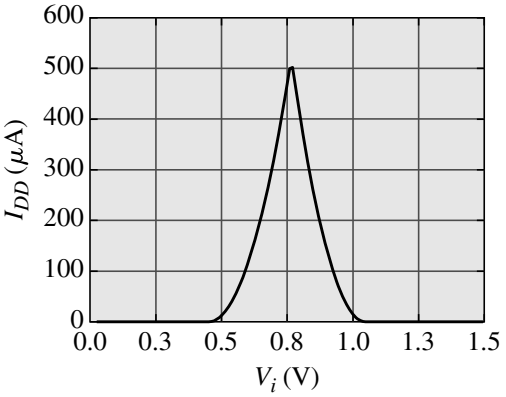
Inverter Static Current Characteristics

5-10. Given an inverter with $V_{DD} = 1.5$ V, $V_{tn} = 0.4$ V, and $V_{tp} = -0.4$ V, calculate the peak current during the transition if $(W/L)_n = 3$, $(W/L)_p = 7.5$, $K_p = 50\,\mu\text{A/V}^2$, and $K_n = 125\ \mu\text{A/V}^2$.

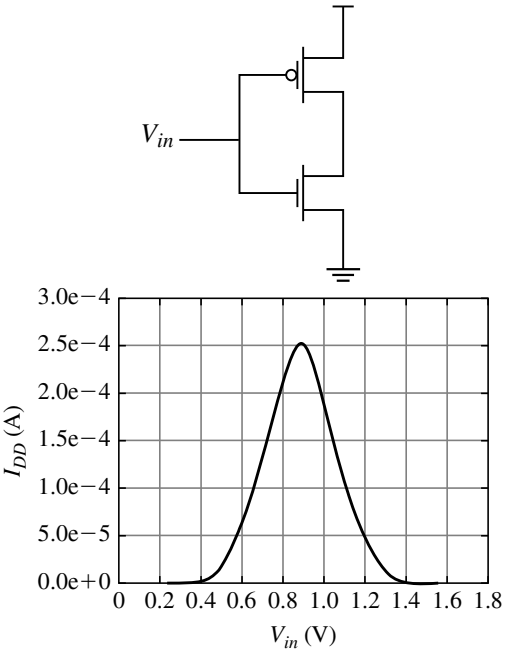
5-11. An inverter has $V_{DD} = 2$ V, $V_{tn} = 0.5$ V, $V_{tp} = -0.5$ V, $K_n = 300\ \mu\text{A/V}^2$, $K_p = 200\ \mu\text{A/V}^2$, $(W/L)_n = 2$, and $(W/L)_p = 3$.
(a) If $V_{IN} = 0.8$ V, what is I_{DD}?
(b) The I_{DD} solution in part (a) appears twice in the current transfer curve. Use the *p*MOS equations to calculate the other V_{IN} value to satisfy the current in part (a).



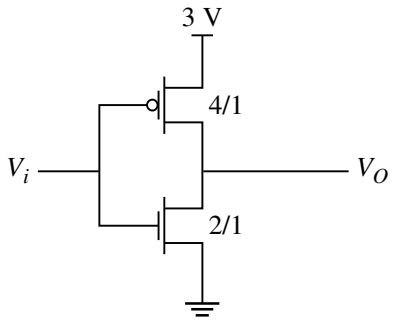
5-12. Given $V_{DD} = 1.5$ V, $K_p = 70\ \mu$A. $K_n = 120\ \mu$A, $(W/L)_p = 150$, and $(W/L)_n = 75$, use the ITC to calculate V_{tp}.



5-13. Given that $V_{DD} = 1.8$ V, $V_{tn} = 0.5$ V, and $K_n = 100\ \mu\text{A/V}^2$, what is W/L of the *n*MOS transistor?



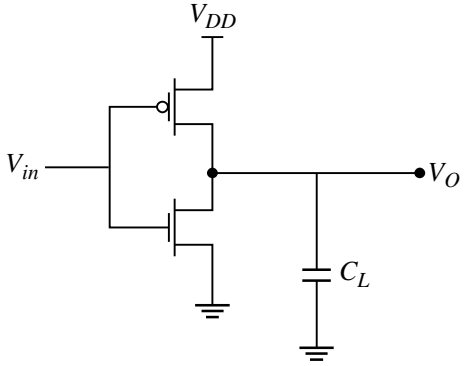
5-14. $I_{DD} = 40\ \mu$A, $(W/L)_n = 2$, $K_n = 100\ \mu$A, $V_{tn} = 0.5$ V, $K_p = 50\ \mu$A, $V_{tp} = -0.5$ V, and $V_i < 1.5$ V. What is V_i?



5-15. Given an inverter with $V_{tn} = 0.4$ V, $V_{tp} = -0.35$ V, $K_n = 200\ \mu$A/V^2, $K_p = 100\ \mu$A/V^2, $(W/L)_n = 2$, and $(W/L)_p = 3$, calculate the peak drain current I_{peak} during an inverter transition for **(a)** $V_{DD} = 1.5$ V and **(b)** $V_{DD} = 1.0$ V.

Inverter Speed Property

5-16. Use the transition time delay model where $C_L = 30$ fF, $V_{DD} = 1.5$ V, $(W/L)_n = 2$, $K'_n = 100\ \mu$A/V^2, $(W/L)_p = 5$, $K'_p = 25\ \mu$A/V^2, $V_{tp} = -0.35$ V, and $V_{tn} = 0.35$ V. What is the difference between rise and fall time of the transition if defined between 0 V and 1.5 V?



5-17. If a pMOS transistor in an inverter has $\mu\varepsilon/2T_{ox} = 28\ \mu$A/V^2, $V_{tp} = -0.6$ V, and $W/L = 6$, what is the expected additional rise time delay if the gate power supply voltage is reduced from a normal $V_{DD} = 2.5$ V to $V_{DD} = 1.8$ V with $C_L = 25$ fF.

5-18. A CMOS inverter has $W/L = 6$ for both transistors, $V_{tn} = 0.6$ V, $V_{tp} = -0.6$ V, and $V_{DD} = 2.3$ V. If V_t is reduced to $|V_t| = 0.2$ V for both transistors, what is the percent decrease in speed of transition?

Inverter Power

5-19. Calculate the power dissipated by a cardiac pacemaker circuit if $f_{clk} = 32.6$ kHz, $\alpha = 0.1$, $V_{DD} = 1.5$ V, C_L (per gate) $= 300$ fF, and the number of logic gates $= 10$ k.

5-20. A clock network has $C_L = 10$ nF, $\alpha = 1$, and $V_{DD} = 1.2$ V. The maximum power dissipation allowed is 5 W. What is the maximum clock frequency?

5-21. Use Figure 5-12. $V_{DD} = 0.9$ V, $V_{tn} = 0.2$ V, $V_{tp} = -0.2$ V, $f_{clk} = 3$ GHz, $W/L = 3$, $K_n = 250\ \mu$A/V^2, and $t_r = t_f = 40$ ps. Calculate the mean current during the logic transition and the average power dissipated in the chip.

Power Supply Scaling

5-22. Given an inverter with: $V_{tn} = 0.4$ V, $V_{tp} = -0.4$ V, $K_n = 200\ \mu$A/V^2, $K_p = 100\ \mu$A/V^2, $(W/L)_n = 2$, and $(W/L)_p = 3$. Calculate the peak drain current I_{peak} during an inverter transition for **(a)** $V_{DD} = 1.5$ V and **(b)** $V_{DD} = 1.0$ V.

5-23. P_{sc} must be kept under 1 W. The chip has $V_{DD} = 1.5$ V, one million transistors, and $\alpha = 0.1$. Assume that 10^6 transistors represent an equivalent 500 k inverters for analysis. What is the mean drain current per inverter?

Sizing and Inverter Buffers

5-24. An output buffer has an input capacitance of 95 fF and a load capacitance of 100 pF. How many inverters are required in a fixed tapered design to minimize the propagation delay?

5-25. A fixed tapered buffer has an input capacitance of 1 pF. If the output stage must drive a load of 54 pF, how many stages are needed?

5-26. The number of tapered buffers in a design must be kept at no more than five to accommodate chip area constraints.

(a) If the input gate capacitance is 50 fF, what is the maximum load capacitance that can be driven?

(b) What is the width ratio of the last inverter W_L to the first inverter in the chain W_{in}?