

### Example

Assuming  $ci = 0$ , the approach you know sets  $b = 10$

$$\begin{array}{rclcl}
 x & = & 107_{(10)} & \mapsto & 1\ 0\ 7 \\
 y & = & 14_{(10)} & \mapsto & \underline{0\ 1\ 4} + \\
 c & = & & & \\
 r & = & & & \underline{\hspace{1cm}}
 \end{array}$$

but it *also* applies for  $b = 2$

$$\begin{array}{rclcl}
 x & = & 107_{(10)} & \mapsto & 0\ 1\ 1\ 0\ 1\ 0\ 1\ 1 \\
 y & = & 14_{(10)} & \mapsto & \underline{0\ 0\ 0\ 0\ 1\ 1\ 1\ 0} + \\
 c & = & & & \\
 r & = & & & \underline{\hspace{1cm}}
 \end{array}$$

► Note that:

- adding two  $n$ -digit integers produces an  $(n + 1)$ -digit result, and
- instead of producing this directly (per the example), Add outputs the extra digit as a separate carry-out.

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 c & = & \quad \quad \quad \underline{0 \ 1 \ 0} \\
 r & = & \quad \quad \quad \underline{\quad 2 \ 1}
 \end{array}$$

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 x & = & 107_{(10)} \quad \mapsto \quad 0 \ 1 \ 1 \ 0 \ 1 \ 0 \ 1 \ 1 \\
 y & = & 14_{(10)} \quad \mapsto \quad \underline{0 \ 0 \ 0 \ 0 \ 1 \ 1 \ 1 \ 0} + \\
 c & = & \\
 r & = & \underline{\hspace{2cm}}
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 c & = & & & \\
 r & = & & & \underline{\hspace{2cm}}
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 c & = & & 0 \\
 r & = & & \underline{\hspace{1.5cm}}
 \end{array}$$

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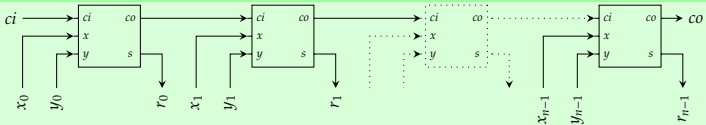
### Algorithm (ADD)

**Input:** Two unsigned,  $n$ -digit, base- $b$  integers  $x$  and  $y$ , and a 1-digit carry-in  $c_i$

**Output:** An unsigned,  $n$ -digit, base- $b$  integer  $r = x + y$ , and a 1-digit carry-out  $co$

```
1  $r \leftarrow 0, c_0 \leftarrow c_i$ 
2 for  $i = 0$  upto  $n - 1$  step  $+1$  do
3    $r_i \leftarrow (x_i + y_i + c_i) \bmod b$ 
4   if  $(x_i + y_i + c_i) < b$  then  $c_{i+1} \leftarrow 0$  else  $c_{i+1} \leftarrow 1$ 
5 end
6  $co \leftarrow c_n$ 
7 return  $r, co$ 
```

## Circuit





## Algorithm (SUB)

**Input:** Two unsigned,  $n$ -digit, base- $b$  integers  $x$  and  $y$ , and a 1-digit borrow-in  $bi$

**Output:** An unsigned,  $n$ -digit, base- $b$  integer  $r = x - y$ , and a 1-digit borrow-out  $bo$

```

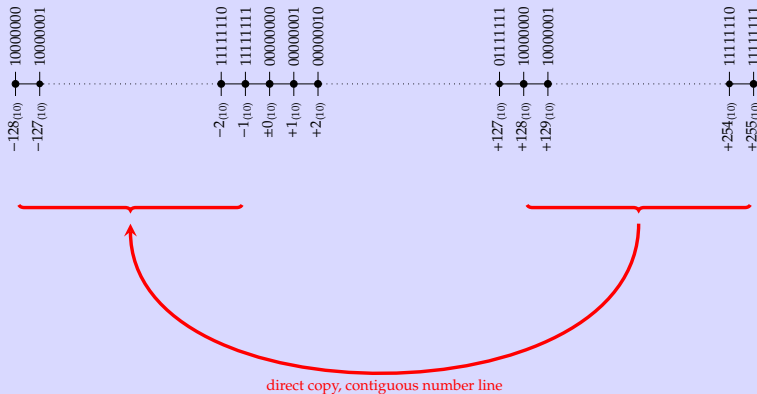
1  $r \leftarrow 0, c_0 \leftarrow bi$ 
2 for  $i = 0$  upto  $n - 1$  step  $+1$  do
3    $r_i \leftarrow (x_i - y_i - c_i) \bmod b$ 
4   if  $(x_i - y_i - c_i) \geq 0$  then  $c_{i+1} \leftarrow 0$  else  $c_{i+1} \leftarrow 1$ 
5 end
6  $bo \leftarrow c_n$ 
7 return  $r, bo$ 

```

## Definition

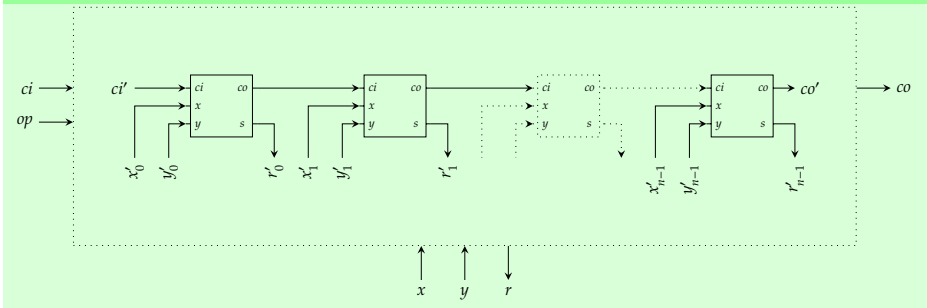
In two's-complement representation, for some  $y$  we have  $-y \mapsto \neg y + 1$ . Put more simply, to negate  $y$  we invert each bit  $y_i$  via a NOT gate, then add 1 to the result.

## Example



- **Question:** we know  $x - y \equiv x + (-y)$ , and can already compute  $x + y$ , so

## Circuit



given we want

$$r = \begin{cases} x + y + ci & \text{if } op = 0 \\ x - y - ci & \text{if } op = 1 \end{cases} ,$$

how do we control  $x'$ ,  $y'$  and  $ci'$  to get the correct result?

► So,

<i>op</i>	<i>ci</i>	<i>r</i>				
0	0	<i>x</i>	+	<i>y</i>	+	<i>ci</i>
0	1	<i>x</i>	+	<i>y</i>	+	<i>ci</i>
1	0	<i>x</i>	-	<i>y</i>	-	<i>ci</i>
1	1	<i>x</i>	-	<i>y</i>	-	<i>ci</i>

► So,

$op$	$ci$	$r$				
0	0	$x$	+	$y$	+	0
0	1	$x$	+	$y$	+	1
1	0	$x$	-	$y$	-	0
1	1	$x$	-	$y$	-	1

► So,

$op$	$ci$	$r$					
0	0	$x$	+	$y$	+	0	
0	1	$x$	+	$y$	+	1	
1	0	$x$	+	$\neg y + 1$	-	0	
1	1	$x$	+	$\neg y + 1$	-	1	

► So,

$op$	$ci$	$r$				
0	0	$x$	+	$y$	+	0
0	1	$x$	+	$y$	+	1
1	0	$x$	+	$\neg y$	+	1
1	1	$x$	+	$\neg y$	+	0

► So,

<i>op</i>	<i>ci</i>	<i>r</i>				
0	0	<i>x</i>	+	<i>y</i>	+	0
0	1	<i>x</i>	+	<i>y</i>	+	1
1	0	<i>x</i>	+	$\neg y$	+	1
1	1	<i>x</i>	+	$\neg y$	+	0

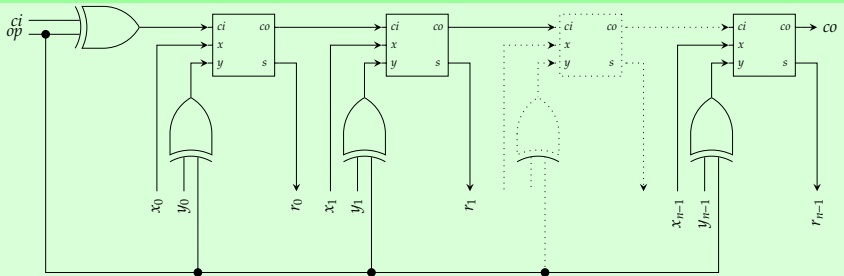
► We can compute  $x' + y' + ci'$ , so we translate via

<i>op</i>	<i>ci</i>	<i>x<sub>i</sub></i>	<i>y<sub>i</sub></i>	<i>ci'</i>	<i>x'<sub>i</sub></i>	<i>y'<sub>i</sub></i>
0	0	0	0	0	0	0
0	1	1	1	1	1	1
1	0	0	0	1	0	1
1	1	1	1	0	1	0

i.e.,  $ci' = ci \oplus op$ ,  $x'_i = x_i$  and  $y'_i = y_i \oplus op$ .



## Circuit



## Example

Consider a signed, 16-bit integer  $x$ , used within (or **cast** into) a signed, 32-bit integer; use as is produces the wrong result, whereas **sign extension** by padding with the sign bit is correct:

$$\begin{array}{rclcl}
 x & = & & 1111111111111111_{(2)} & = & -1_{(10)} \\
 & & 0000000000000000 & 1111111111111111_{(2)} & = & 65535_{(10)} \\
 & & 1111111111111111 & 1111111111111111_{(2)} & = & -1_{(10)}
 \end{array}$$

- It's common to think of a left-shift (resp. right-shift) of  $x$  by  $y$  bits as multiplication (resp. division) by  $2^y$ , e.g.,

$$2^y \cdot x = 2^y \cdot \sum_{i=0}^{n-1} x_i \cdot 2^i = \sum_{i=0}^{n-1} x_i \cdot 2^{i+y}.$$

- So one reason for having **arithmetic shift** is to preserve sign:

### Example

Note that

$$\begin{aligned} -38_{(10)} & \mapsto 11011010 \\ -38_{(10)}/2 &= -19_{(10)} \mapsto 11101101 \end{aligned}$$

and right-shift by  $y = 1$  bit should mean “divide by two”. But if we use logical right-shift we get

$$\begin{aligned} r &= x \gg_u y = 11011010 \gg_u 1 \\ &= 01101101 \\ &\mapsto 109_{(10)} \end{aligned}$$

whereas if we use arithmetic right-shift we get

$$\begin{aligned} r &= x \gg_s y = 11011010 \gg_s 1 \\ &= 11101101 \\ &\mapsto -19_{(10)} \end{aligned}$$

as expected.

### Example

Consider use of an *unsigned* representation:

$$\begin{array}{rclcl}
 x & = & 15_{(10)} & \mapsto & 1 & 1 & 1 & 1 \\
 y & = & 1_{(10)} & \mapsto & 0 & 0 & 0 & 1 \\
 c & = & & & \hline & & 1 & 1 & 1 & 1 & 0 \\
 r & = & 0_{(10)} & \mapsto & 0 & 0 & 0 & 0
 \end{array}
 +$$

Here, the carry-out indicates an error: the correct result  $r = 16$  is too large for  $n = 4$  bits.

## Example

Consider use of a *signed* representation:

$$\begin{array}{rcll}
 x & = & -1_{(10)} & \mapsto & \begin{array}{cccc} 1 & 1 & 1 & 1 \end{array} \\
 y & = & 1_{(10)} & \mapsto & \begin{array}{cccc} 0 & 0 & 0 & 1 \end{array} \\
 c & = & & & \begin{array}{cccc} 1 & 1 & 1 & 1 \\ \hline & 0 & 0 & 0 \end{array} \\
 r & = & 0_{(10)} & \mapsto & \begin{array}{cccc} & 0 & 0 & 0 \end{array}
 \end{array} +$$

Irrespective of the carry-out, the signs of inputs and output make sense: there is no overflow, so  $r = 0$  is correct.

## Example

Consider use of a *signed* representation:

$$\begin{array}{rcll}
 x & = & 7_{(10)} & \mapsto & \begin{array}{cccc} 0 & 1 & 1 & 1 \end{array} \\
 y & = & 1_{(10)} & \mapsto & \begin{array}{cccc} 0 & 0 & 0 & 1 \end{array} \\
 c & = & & & \begin{array}{cccc} 0 & 1 & 1 & 1 \\ \hline & 1 & 0 & 0 \end{array} \\
 r & = & -8_{(10)} & \mapsto & \begin{array}{cccc} & 1 & 0 & 0 \end{array}
 \end{array} +$$

Irrespective of the carry-out, the signs of inputs and output make no sense: there is an overflow, so  $r = -8$  is incorrect.

### Listing (C)

```
1 uint8_t add( uint8_t x, uint8_t y ) {
2     asm goto( "add %0, %1          ;"
3              "jo  %1[overflow] ;"
4              "jc  %1[carry]   ;"
5              "jmp %1[correct]  ;"
6
7              : : "r" (x), "r" (y) : "cc" : overflow, carry, correct );
8
9     overflow:
10    printf( "overflow\n" );
11    goto correct;
12
13    carry:
14    printf(      "carry\n" );
15    goto correct;
16
17    correct:
18    return x + y;
19 }
```