Analysis of LU Decomposition on UMS

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In this report, I will analyze the performance evaluations of LU decomposition in the following scenarios:-

1. One PE, largest square matrix to fit in local memory.
2. One PE, largest square matrix to fit in SDRAM.
3. *Block Decomposition*
   3.1. PE to do data transfer from SDRAM.
   3.2. MTE to do data transfer from SDRAM.
4. *Cyclic Decomposition*
   4.1. PE to do data transfer from SDRAM.
   4.2. MTE to do data transfer from SDRAM.

I. *One PE, largest square matrix to fit in local memory*

The UMS has a number of Quads, each Quad having 4 PES, a 32 KB of instruction memory/cache and a 64 KB of data memory/cache.

a) UMS Statistics

Matrix Size	Active Cycles	Delay Cycles	Read Wait Cycles	Instruction Cache Misses
4 x 4	*379586*	*1950*	*275750*	*215*
24 x 24	*3665583*	*1300*	*2548550*	*219*
48 x 48	*24487775*	*1560*	*16816150*	*219*
96 x 96	*183938399*	*1560*	*125529750*	*219*
128 x 128	*429876354*	*1560*	*292901950*	*219*

Data Cache Misses = *0*

b) Local Bus Statistics

Matrix Size	Local Bus Utilization	Local Bus Read Transactions	Local Bus Read Bytes	Local Bus Write Transactions	Local Bus Write Bytes
4 x 4	*1.051 %*	*2834*	*4807*	*1156*	*4264*
24 x 24	*1.531%*	*39032*	*104134*	*17105*	*68051*
48 x 48	*1.626 %*	*277600*	*773054*	*120689*	*482387*
96 x 96	*1.662%*	*2135400*	*6029982*	*922289*	*3688787*
128 x 128	*1.671%*	*5017938*	*14212681*	*2163278*	*8652734*

c) *DRAM Statistics*

Matrix Size	*Read data Transactions*	*Read Bytes*	*Read Page Misses*	*Write data Transactions*	*Write Bytes*	*Write Page Misses*
4 x 4	*1590*	*11411*	*185*	*1098*	*4060*	*106*
24 x 24	*12958*	*56986*	*193*	*11907*	*47287*	*59*
48 x 48	*84296*	*342338*	*186*	*81515*	*325719*	*107*
96 x 96	*627864*	*2516610*	*227*	*618171*	*2472343*	*54*
128 x 128	*1464725*	*5864045*	*189*	*1447864*	*5791106*	*106*

d) *Total Simulation Time*

Matrix Size	Total Simulation Cycles
4 x 4	*379607*
24 x 24	*3665596*
48 x 48	*24487815*
96 x 96	*183938409*
128 x 128	*429876395*

II. *One PE, largest square matrix to fit in SDRAM*

a. *UMS Statistics*

Matrix Size	Active Cycles	Delay Cycles	Read Wait Cycles	Instruction Cache Misses
4 x 4	*391818*	*2210*	*286950*	*217*
24 x 24	*6385503*	*1820*	*5254150*	*219*
48 x 48	*46461313*	*1690*	*38699550*	*219*
96 x 96	*360608301*	*1430*	*301545550*	*219*
128 x 128	*849168852*	*1690*	*710681350*	*219*

Data Cache Misses = *0*

b. *Local Bus Statistics*

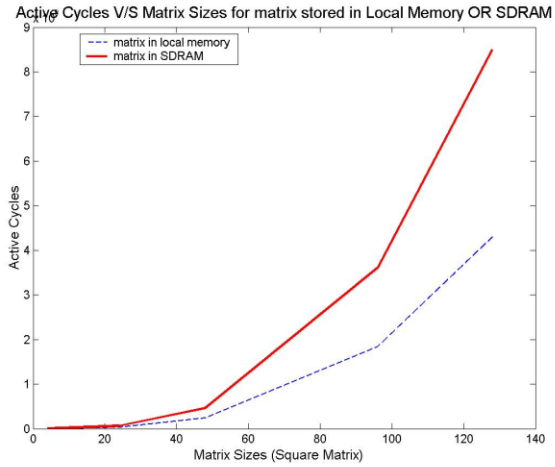
Matrix Size	Local Bus Utilization	Local Bus Read Transactions	Local Bus Read Bytes	Local Bus Write Transactions	Local Bus Write Bytes
4 x 4	*1.033%*	*2892*	*4815*	*1156*	*4264*
24 x 24	*1.091%*	*52564*	*104150*	*17105*	*68051*
48 x 48	*1.093%*	*387018*	*773058*	*120689*	*482387*
96 x 96	*1.092%*	*3015478*	*6029978*	*922289*	*3688787*
128 x 128	*1.092%*	*7106836*	*14212685*	*2163278*	*8652734*

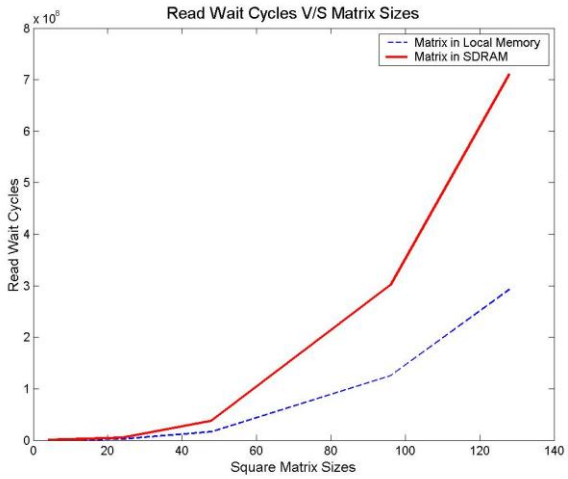
c. *DRAM Statistics*

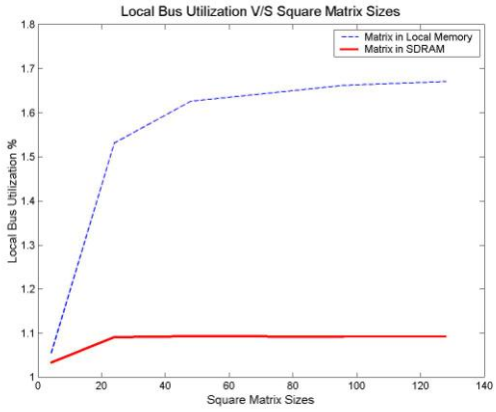
Matrix Size	*Read data Transactions*	*Read Bytes*	*Read Page Misses*	*Write data Transactions*	*Write Bytes*	*Write Page Misses*
4 x 4	*1648*	*11699*	*252*	*1134*	*4204*	*148*
24 x 24	*26486*	*111098*	*13399*	*17083*	*67991*	*8903*
48 x 48	*193713*	*780006*	*37932*	*120667*	*482327*	*26596*
96 x 96	*1507943*	*6036926*	*372308*	*922267*	*3688727*	*208814*
128 x 128	*3553622*	*14219633*	*834542*	*2163256*	*8652674*	*491042*

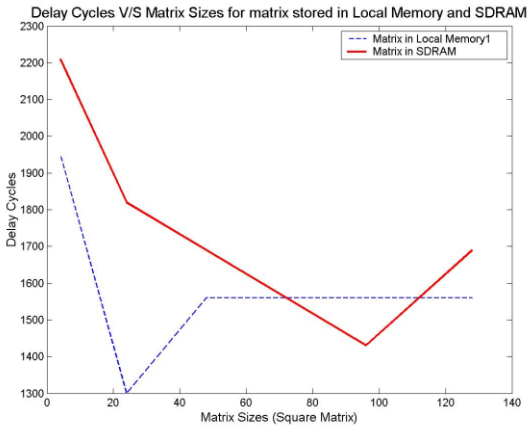
d. *Total Simulation Time*

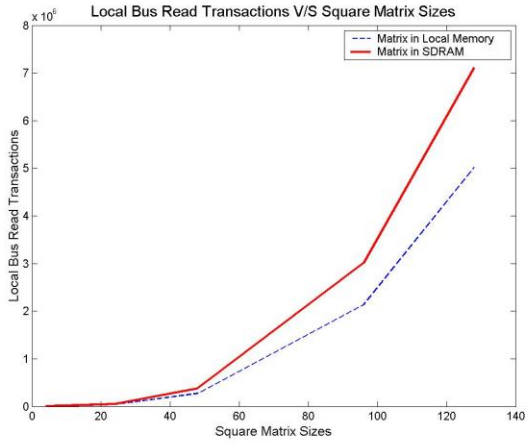
Matrix Size	Total Simulation Cycles
4 x 4	*391833*
24 x 24	*6385539*
48 x 48	*46461350*
96 x 96	*360608307*
128 x 128	*849168860*

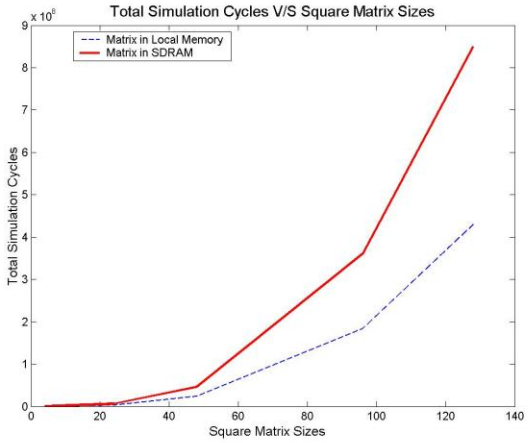


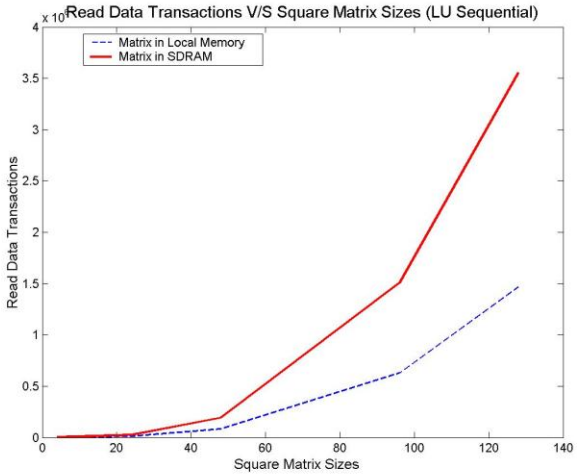












III. *Block Decomposition*

1. ***Using MTE to do data Transfer***

a. *UMS Statistics*

Matrix Size	Processor	Active Cycles	Delay Cycles	Read Wait Cycles	Instruction Cache Misses
16 x 16	*PE 0*	*5712846*	*524550*	*3975100*	*320*
	PE 1	*5712846*	*971100*	*3428900*	*77*
	PE 2	*5712846*	*961285*	*3439850*	*61*
	PE 3	*5712846*	*959530*	*3449500*	*59*
48 x 48	*PE 0*	*73758158*	*4074525*	*55586000*	*320*
	PE 1	*73758158*	*13056940*	*43353100*	*77*
	PE 2	*73758158*	*12920635*	*43208700*	*61*
	PE 3	*73758158*	*12902825*	*43077050*	*59*
64 x 64	*PE 0*	*164120601*	*8514935*	*124627600*	*323*
	PE 1	*164120601*	*29303430*	*96136150*	*80*
	PE 2	*164120601*	*29029130*	*95710200*	*63*
	PE 3	*164120601*	*29028220*	*95316350*	*61*

96 x 96	*PE 0*	*524928161*	*26013130*	*401176400*	*323*
	PE 1	*524928161*	*94450265*	*306500800*	*79*
	PE 2	*524928161*	*93628860*	*304855000*	*63*
	PE 3	*524928161*	*93745340*	*303300700*	*61*
128 x 128	*PE 0*	*1215669483*	*59270640*	*931469600*	*323*
	PE 1	*1215669483*	*219457680*	*708826950*	*80*
	PE 2	*1215669483*	*217593090*	*704760800*	*64*
	PE 3	*1215669483*	*217928815*	*700930200*	*61*

Data Cache Misses = *0*

b. *Local Bus Statistics*

Matrix Size	Processor	Local Bus Utilization	Local Bus Read Transactions	Local Bus Read Bytes	Local Bus Write Transactions	Local Bus Write Bytes
16 x 16	*PE 0*	*3.358 %*	*43317*	*85633*	*9723*	*38067*
	PE 1		*37505*	*76837*	*3372*	*13272*
	PE 2		*38919*	*80561*	*4184*	*16520*
	PE 3		*40269*	*83773*	*4868*	*19256*
48 x 48	*PE 0*	*3.353%*	*571503*	*1164869*	*141235*	*564115*
	PE 1		*464993*	*987429*	*26364*	*105240*
	PE 2		*476299*	*1033705*	*33984*	*135720*
	PE 3		*482619*	*1059641*	*38148*	*152376*
64 x 64	*PE 0*	*3.364%*	*1278127*	*2610221*	*317215*	*1268035*
	PE 1		*1032805*	*2202413*	*53908*	*215416*
	PE 2		*1057865*	*2309237*	*70596*	*282168*
	PE 3		*1070865*	*2367365*	*79092*	*316152*
96 x 96	*PE 0*	*3.378%*	*4109722*	*8404353*	*1019543*	*4077347*
	PE 1		*3300347*	*7064121*	*159652*	*638392*
	PE 2		*3381629*	*7420701*	*213484*	*853720*
	PE 3		*3422657*	*7613829*	*239668*	*958456*
128 x 128	*PE 0*	*3.386%*	*9539955*	*19518536*	*2362284*	*9448302*
	PE 1		*7642249*	*16384213*	*357684*	*1430520*
	PE 2		*7833993*	*17230613*	*484244*	*1936760*
	PE 3		*7929607*	*17688145*	*545268*	*2180856*

Matrix Size	Memory Transfer Units	Local Bus Utilization	Local Bus Read Transactions	Local Bus Read Bytes	Local Bus Write Transactions	Local Bus Write Bytes
16 x 16	*MTE 0*	*3.358%*	*43317*	*85633*	*9723*	*38067*
	MTE 1		*37505*	*76837*	*3372*	*13272*
	MTE 2		*38919*	*80561*	*4184*	*16520*
	MTE 3		*40269*	*83773*	*4868*	*19256*
48 x 48	*MTE 0*	*3.353%*	*36948*	*183144*	*22542*	*180024*
	MTE 1		*35196*	*183144*	*22542*	*180024*
	MTE 2		*40452*	*183144*	*22542*	*180024*
	MTE 3		*35196*	*183144*	*22542*	*180024*
64 x 64	*MTE 0*	*3.364%*	*86896*	*430560*	*53352*	*426400*
	MTE 1		*82768*	*430560*	*53352*	*426400*
	MTE 2		*95152*	*430560*	*53352*	*426400*
	MTE 3		*82768*	*430560*	*53352*	*426400*
96 x 96	*MTE 0*	*3.378%*	*291624*	*1444560*	*179868*	*1438320*
	MTE 1		*277752*	*1444560*	*179868*	*1438320*
	MTE 2		*319368*	*1444560*	*179868*	*1438320*
	MTE 3		*319368*	*1444560*	*179868*	*1438320*
128 x 128	*MTE 0*	*3.386%*	*689888*	*3417024*	*426192*	*3408704*
	MTE 1		*657056*	*3417024*	*426192*	*3408704*
	MTE 2		*755552*	*3417024*	*426192*	*3408704*
	MTE 3		*657056*	*3417024*	*426192*	*3408704*

Total Local Bus Cycles

Matrix Size	Local Bus Read Transactions	Local Bus Read Bytes	Local Bus Write Transactions	Local Bus Write Bytes
16 x 16	*166266*	*358004*	*25579*	*114155*
48 x 48	*2143206*	*4978220*	*329899*	*1677547*
64 x 64	*4787246*	*11211476*	*734219*	*3787371*
96 x 96	*15380851*	*36281244*	*2351819*	*12281195*
128 x 128	*35705356*	*84489603*	*5454248*	*28631254*

c. DRAM Statistics

Matrix Size	Processor	Read Data Transactions	Read Bytes	Read Page Misses	Write Data Transactions	Write Bytes	Write Page Misses
16 x 16	*PE 0*	*19684*	*85701*	*2475*	*9323*	*36507*	*266*
	PE 1	*16875*	*69209*	*1861*	*2767*	*10852*	*246*
	PE 2	*16771*	*68345*	*3123*	*3403*	*13396*	*1018*
	PE 3	*16651*	*67809*	*3128*	*3975*	*15684*	*1182*

48 x 48	*PE 0*	*277631*	*1117489*	*111282*	*136447*	*545003*	*63670*
	PE 1	*216423*	*867401*	*67452*	*16475*	*65684*	*504*
	PE 2	*215532*	*863389*	*56510*	*20687*	*82532*	*771*
	PE 3	*214707*	*860033*	*30084*	*23171*	*92468*	*908*
64 x 64	*PE 0*	*622816*	*2498313*	*273730*	*306983*	*1227155*	*152088*
	PE 1	*480291*	*1922957*	*179650*	*31617*	*126252*	*551*
	PE 2	*477983*	*1913249*	*39472*	*40305*	*161004*	*1023*
	PE 3	*475866*	*1904725*	*141603*	*44897*	*179372*	*819*
96 x 96	*PE 0*	*2005454*	*8028865*	*624908*	*988411*	*3952867*	*276532*
	PE 1	*1532016*	*6129829*	*214806*	*87757*	*350812*	*1531*
	PE 2	*1523649*	*6095913*	*98244*	*114612*	*458236*	*5372*
	PE 3	*1515703*	*6064073*	*166147*	*127645*	*510364*	*112061*
128 x 128	*PE 0*	*4656847*	*18634428*	*1472082*	*2292204*	*9168030*	*621035*
	PE 1	*3543565*	*14176053*	*572662*	*190745*	*762764*	*8402*
	PE 2	*3523060*	*14093585*	*226999*	*253177*	*1012492*	*8503*
	PE 3	*3503776*	*14016365*	*402548*	*282841*	*1131148*	*261390*
Matrix Size	Memory Transfer Units	Read Data Transactions	Read Bytes	Read Page Misses	Write Data Transactions	Write Bytes	Write Page Misses
16 x 16	*MTE 0*	*144*	*4608*	*20*	*80*	*2560*	*10*
	MTE 1	*126*	*4032*	*19*	*96*	*3072*	*12*
	MTE 2	*180*	*5760*	*23*	*48*	*1536*	*6*
	MTE 3	*126*	*4032*	*15*	*96*	*3072*	*12*
48 x 48	*MTE 0*	*3504*	*112128*	*111*	*2160*	*69120*	*45*
	MTE 1	*3066*	*98112*	*105*	*2592*	*82944*	*76*
	MTE 2	*4380*	*140160*	*147*	*1296*	*41472*	*33*
	MTE 3	*3066*	*98112*	*81*	*2592*	*82944*	*87*
64 x 64	*MTE 0*	*8320*	*264192*	*176*	*5160*	*163840*	*80*
	MTE 1	*7280*	*231168*	*152*	*6192*	*196608*	*113*
	MTE 2	*10400*	*330240*	*208*	*3096*	*98304*	*48*
	MTE 3	*7280*	*231168*	*136*	*6192*	*196608*	*96*
96 x 96	*MTE 0*	*27840*	*887808*	*528*	*17340*	*552960*	*240*
	MTE 1	*24360*	*776832*	*456*	*20808*	*663552*	*372*
	MTE 2	*34800*	*1109760*	*624*	*10404*	*331776*	*168*
	MTE 3	*24360*	*776832*	*384*	*20808*	*663552*	*348*
128 x 128	*MTE 0*	*65792*	*2101248*	*1152*	*41040*	*1310720*	*720*
	MTE 1	*57568*	*1838592*	*1008*	*49248*	*1572864*	*864*
	MTE 2	*82240*	*2626560*	*1440*	*24624*	*786432*	*432*
	MTE 3	*57568*	*1838592*	*1008*	*49248*	*1572864*	*864*

Total DRAM Cycles

Matrix Size	Read Data Transactions	Read Bytes	Read Page Misses	Write Data Transactions	Write Bytes	Write Page Misses
16 x 16	*70557*	*309496*	*10664*	*19788*	*86679*	*2752*
48 x 48	*938309*	*4156824*	*265772*	*205420*	*1062167*	*66094*
64 x 64	*2090236*	*9296012*	*635127*	*444442*	*2349143*	*154818*
96 x 96	*6688182*	*29869912*	*1106097*	*1387785*	*7484119*	*396624*
128 x 128	*15490416*	*69325423*	*2678899*	*3183127*	*17317314*	*902210*

d. *Total Simulation Time*

Matrix Size	Total Simulation Cycles
16 x 16	*5712887*
48 x 48	*73758172*
64 x 64	*164120626*
96 x 96	*524928175*
128 x 128	*1215669525*

2. Using PE to do data Transfer

a. UMS Statistics

Matrix Size	Processor	Active Cycles	Delay Cycles	Read Wait Cycles	Instruction Cache Misses
16 x 16	*PE 0*	*6076817*	*593190*	*4155200*	*310*
	PE 1	*6076817*	*1024660*	*3576600*	*79*
	PE 2	*6076817*	*1007890*	*3549450*	*60*
	PE 3	*6076817*	*995345*	*3524350*	*59*
48 x 48	*PE 0*	*108690794*	*10149750*	*75760900*	*310*
	PE 1	*108690794*	*18220800*	*63476850*	*79*
	PE 2	*108690794*	*17175665*	*63280600*	*61*
	PE 3	*108690794*	*16245645*	*63100650*	*59*
64 x 64	*PE 0*	*250515771*	*23527725*	*174611050*	*313*
	PE 1	*250515771*	*42052075*	*146092850*	*79*
	PE 2	*250515771*	*39512915*	*145642050*	*64*
	PE 3	*250515771*	*37247990*	*145223250*	*61*
96 x 96	*PE 0*	*823653578*	*77879165*	*574253450*	*313*
	PE 1	*823653578*	*138429525*	*479836550*	*80*
	PE 2	*823653578*	*129735905*	*478437750*	*64*
	PE 3	*823653578*	*93745340*	*477141300*	*61*
128 x 128	*PE 0*	*1929519970*	*183164930*	*1345281900*	*313*
	PE 1	*1929519970*	*324464140*	*1123536950*	*79*

	PE 2	*1929519970*	*303727645*	*1120354700*	*64*
	PE 3	*1929519970*	*285190230*	*1117409600*	*60*

Data Cache Misses = *0*

b. *Local Bus Statistics*

Matrix Size	Processor	Local Bus Utilization	Local Bus Read Transactions	Local Bus Read Bytes	Local Bus Write Transactions	Local Bus Write Bytes
16 x 16	*PE 0*	*3.132%*	*45391*	*90141*	*9835*	*38515*
	PE 1		*39213*	*80901*	*3652*	*14392*
	PE 2		*40501*	*84661*	*4632*	*18312*
	PE 3		*41607*	*87673*	*5484*	*21720*
48 x 48	*PE 0*	*2.994%*	*778349*	*1588809*	*153859*	*614611*
	PE 1		*676333*	*1430389*	*57924*	*231480*
	PE 2		*692219*	*1495857*	*84480*	*337704*
	PE 3		*703015*	*1540777*	*107580*	*430104*
64 x 64	*PE 0*	*2.987%*	*1790049*	*3658201*	*348383*	*1392707*
	PE 1		*1556303*	*3297217*	*131828*	*527096*
	PE 2		*1592923*	*3450841*	*195268*	*780856*
	PE 3		*1617509*	*3555821*	*250516*	*1001848*
96 x 96	*PE 0*	*2.986%*	*5881089*	*12027977*	*1127735*	*4510115*
	PE 1		*5113515*	*10850345*	*430132*	*1720312*
	PE 2		*5237023*	*11370385*	*646252*	*2584792*
	PE 3		*5319907*	*11726233*	*834724*	*3338680*
128 x 128	*PE 0*	*2.986%*	*13773849*	*28177440*	*2621228*	*10484078*
	PE 1		*11977825*	*25432773*	*1005044*	*4019960*
	PE 2		*12271743*	*26669825*	*1520020*	*6079864*
	PE 3		*12469493*	*27517933*	*1969460*	*7877624*

Total Local Bus Cycles

Matrix Size	Local Bus Read Transactions	Local Bus Read Bytes	Local Bus Write Transactions	Local Bus Write Bytes
16 x 16	*166712*	*343376*	*23603*	*92939*
48 x 48	*2849916*	*6055832*	*403843*	*1613899*
64 x 64	*6556784*	*13962080*	*925995*	*3702507*
96 x 96	*21551534*	*45974940*	*3038843*	*12153899*
128 x 128	*50492910*	*107797971*	*7115752*	*28461526*

c. *DRAM Statistics*

Matrix Size	PEs	Read Data Transactions	Read Bytes	Read Page Misses	Write Data Transactions	Write Bytes	Write Page Misses
16 x 16	*PE 0*	*20559*	*88921*	*1237*	*9227*	*36123*	*263*
	PE 1	*17631*	*72289*	*940*	*2399*	*9380*	*226*
	PE 2	*17315*	*70493*	*1621*	*2763*	*10836*	*566*
	PE 3	*17029*	*69321*	*1515*	*3063*	*12036*	*582*
48 x 48	*PE 0*	*378500*	*1520685*	*127789*	*142303*	*568427*	*63407*
	PE 1	*317050*	*1269965*	*81740*	*27659*	*110420*	*435*
	PE 2	*315884*	*1264797*	*92359*	*37199*	*148580*	*13301*
	PE 3	*314827*	*1260513*	*39426*	*45011*	*179828*	*2490*
64 x 64	*PE 0*	*872720*	*3497649*	*315934*	*321959*	*1287059*	*151640*
	PE 1	*730069*	*2922041*	*254565*	*60865*	*243244*	*13160*
	PE 2	*727644*	*2911921*	*75620*	*83825*	*335084*	*924*
	PE 3	*725402*	*2902869*	*186628*	*102689*	*410540*	*24224*
96 x 96	*PE 0*	*2870804*	*11489985*	*763943*	*1041595*	*4165603*	*285598*
	PE 1	*2398718*	*9596665*	*336186*	*193069*	*772060*	*20637*
	PE 2	*2391544*	*9567521*	*324775*	*272053*	*1087996*	*43594*
	PE 3	*2384924*	*9540957*	*343334*	*337213*	*1348636*	*163009*
128 x 128	*PE 0*	*6725863*	*26910212*	*1754093*	*2420460*	*9681054*	*646038*
	PE 1	*5617152*	*22470373*	*787722*	*445849*	*1783180*	*55423*
	PE 2	*5601037*	*22405493*	*748635*	*635129*	*2540300*	*79092*
	PE 3	*5586158*	*22345865*	*694031*	*791640*	*3166348*	*356281*

Total DRAM Cycles

Matrix Size	Read Data Transactions	Read Bytes	Read Page Misses	Write Data Transactions	Write Bytes	Write Page Misses
16 x 16	*72534*	*301024*	*5313*	*17452*	*68375*	*1637*
48 x 48	*1326261*	*5315960*	*341314*	*252172*	*1007255*	*79633*
64 x 64	*3055835*	*12234480*	*832747*	*569338*	*2275927*	*189948*
96 x 96	*10045990*	*40195128*	*1768238*	*1843930*	*7374295*	*512838*
128 x 128	*23530210*	*94131943*	*3984481*	*4293078*	*17170882*	*1136834*

d. *Total Simulation Time*

Matrix Size	Total Simulation Cycles
16 x 16	*6076840*
48 x 48	*108690823*
64 x 64	*250515779*

96 x 96	*823653599*
128 x 128	*1929519974*

IV. Cyclic Decomposition

1. Using MTE to do data Transfer

a. UMS Statistics

Matrix Size	Processor	Active Cycles	Delay Cycles	Read Wait Cycles	Instruction Cache Misses
16 x 16	*PE 0*	*5667790*	*209170*	*4136450*	*319*
	PE 1	*5667790*	*822900*	*3395450*	*82*
	PE 2	*5667790*	*845845*	*3373450*	*73*
	PE 3	*5667790*	*895895*	*3325250*	*73*
48 x 48	*PE 0*	*69005609*	*1787760*	*53025450*	*319*
	PE 1	*69005609*	*11356735*	*40528750*	*83*
	PE 2	*69005609*	*11367590*	*40500100*	*73*
	PE 3	*69005609*	*11399635*	*40450700*	*72*
64 x 64	*PE 0*	*149065401*	*3669445*	*115583100*	*319*
	PE 1	*149065401*	*25073360*	*87385150*	*85*
	PE 2	*149065401*	*25076285*	*87347050*	*73*
	PE 3	*149065401*	*25091365*	*87299350*	*72*
96 x 96	*PE 0*	*460003442*	*10555220*	*359973450*	*319*
	PE 1	*460003442*	*78973505*	*269097750*	*85*
	PE 2	*460003442*	*78963365*	*269029100*	*73*
	PE 3	*460003442*	*78927615*	*268983500*	*73*
128 x 128	*PE 0*	*1044310925*	*23560680*	*820737950*	*319*
	PE 1	*1044310925*	*180975535*	*610161150*	*84*
	PE 2	*1044310925*	*180867310*	*610121050*	*72*
	PE 3	*1044310925*	*180749855*	*610088150*	*73*

Data Cache Misses = *0*

b. Local Bus Statistics

Matrix Size	Processor	Local Bus Utilization	Local Bus Read Transactions	Local Bus Read Bytes	Local Bus Write Transactions	Local Bus Write Bytes
16 x 16	*PE 0*	*3.553%*	*45705*	*92969*	*15517*	*61243*
	PE 1		*37437*	*76397*	*5414*	*21440*
	PE 2		*38273*	*78237*	*5450*	*21584*

	PE 3		*39993*	*81821*	*5490*	*21744*
48 x 48	*PE 0*	*3.442%*	*580723*	*1246477*	*184262*	*736223*
	PE 1		*440693*	*935421*	*38875*	*155284*
	PE 2		*442325*	*940341*	*39355*	*157204*
	PE 3		*444555*	*946385*	*39811*	*159028*
64 x 64	*PE 0*	*3.442%*	*1269475*	*2741245*	*397124*	*1587671*
	PE 1		*951383*	*2031921*	*75603*	*302196*
	PE 2		*953471*	*2039073*	*76419*	*305460*
	PE 3		*956615*	*2048241*	*77365*	*309244*
96 x 96	*PE 0*	*3.446%*	*3962149*	*8604001*	*1222803*	*4890387*
	PE 1		*2936275*	*6311113*	*209492*	*837752*
	PE 2		*2941665*	*6328661*	*211652*	*846392*
	PE 3		*2946153*	*6344261*	*213764*	*854840*
128 x 128	*PE 0*	*3.450%*	*9057825*	*19735784*	*2773663*	*11093818*
	PE 1		*6668269*	*14378653*	*451247*	*1804772*
	PE 2		*6675329*	*14404869*	*455200*	*1820584*
	PE 3		*6681267*	*14428649*	*458942*	*1835552*

Matrix Size	MTCs	Local Bus Utilization	Local Bus Read Transactions	Local Bus Read Bytes	Local Bus Write Transactions	Local Bus Write Bytes
16 x 16	*MTE 0*	*3.553%*	*1656*	*6672*	*780*	*6192*
	MTE 1		*840*	*6672*	*780*	*6192*
	MTE 2		*1656*	*6672*	*780*	*6192*
	MTE 3		*840*	*6672*	*780*	*6192*
48 x 48	*MTE 0*	*3.442%*	*33096*	*132720*	*16212*	*129360*
	MTE 1		*16632*	*132720*	*16212*	*129360*
	MTE 2		*33096*	*132720*	*16212*	*129360*
	MTE 3		*16632*	*132720*	*16212*	*129360*
64 x 64	*MTE 0*	*3.442%*	*75168*	*301248*	*37008*	*295488*
	MTE 1		*37728*	*301248*	*37008*	*295488*
	MTE 2		*75168*	*301248*	*37008*	*295488*
	MTE 3		*37728*	*301248*	*37008*	*295488*
96 x 96	*MTE 0*	*3.446%*	*242736*	*972192*	*120120*	*959712*
	MTE 1		*121680*	*972192*	*120120*	*959712*
	MTE 2		*242736*	*972192*	*120120*	*959712*
	MTE 3		*121680*	*972192*	*120120*	*959712*
128 x 128	*MTE 0*	*3.450%*	*562496*	*2252160*	*279072*	*2230400*
	MTE 1		*281792*	*2252160*	*279072*	*2230400*
	MTE 2		*562496*	*2252160*	*279072*	*2230400*
	MTE 3		*281792*	*2252160*	*279072*	*2230400*

Total Local Bus Cycles

Matrix Size	Local Bus Read Transactions	Local Bus Read Bytes	Local Bus Write Transactions	Local Bus Write Bytes
16 x 16	*166400*	*356112*	*34991*	*150779*
48 x 48	*2007752*	*4599504*	*367151*	*1725179*
64 x 64	*4356736*	*10065472*	*774543*	*3686523*
96 x 96	*13515074*	*31476804*	*2338191*	*11268219*
128 x 128	*30771266*	*71956595*	*5255340*	*25476326*

c. DRAM Statistics

Matrix Size	PEs	Read Data Transactions	Read Bytes	Read Page Misses	Write Data Transactions	Write Bytes	Write Page Misses
16 x 16	*PE 0*	*20574*	*89233*	*1506*	*14572*	*57507*	*499*
	PE 1	*16643*	*68421*	*1410*	*4868*	*19260*	*573*
	PE 2	*16362*	*67045*	*4583*	*4873*	*19276*	*1766*
	PE 3	*15766*	*64661*	*4626*	*4877*	*19292*	*1916*
48 x 48	*PE 0*	*264287*	*1064085*	*74834*	*170983*	*683151*	*46314*
	PE 1	*201366*	*807341*	*29820*	*28108*	*112216*	*11808*
	PE 2	*201031*	*805721*	*21009*	*28308*	*113016*	*2875*
	PE 3	*200461*	*803413*	*9585*	*28496*	*113768*	*2141*
64 x 64	*PE 0*	*576318*	*2312209*	*164701*	*368269*	*1472295*	*87988*
	PE 1	*434889*	*1741489*	*50690*	*51060*	*204024*	*4652*
	PE 2	*434523*	*1739689*	*74314*	*51428*	*205496*	*30272*
	PE 3	*433920*	*1737249*	*43539*	*51834*	*207120*	*30423*
96 x 96	*PE 0*	*1796592*	*7193305*	*521658*	*1133994*	*4535195*	*253389*
	PE 1	*1341275*	*5367033*	*183396*	*129855*	*519204*	*87974*
	PE 2	*1340471*	*5363481*	*184202*	*130847*	*523172*	*87999*
	PE 3	*1339971*	*5361481*	*43189*	*131815*	*527044*	*7897*
128 x 128	*PE 0*	*4097446*	*16396712*	*2150443*	*2572355*	*10288634*	*1168074*
	PE 1	*3043327*	*12175213*	*1253809*	*266152*	*1064392*	*15220*
	PE 2	*3042879*	*12173085*	*1356482*	*268003*	*1071796*	*198599*
	PE 3	*3042663*	*12172249*	*374040*	*269773*	*1078876*	*198692*
Matrix Size	MTCs	Read Data Transactions	Read Bytes	Read Page Misses	Write Data Transactions	Write Bytes	Write Page Misses
16 x 16	*MTE 0*	*216*	*6528*	*5*	*0*	*0*	*0*
	MTE 1	*0*	*0*	*0*	*204*	*6144*	*4*
	MTE 2	*216*	*6528*	*12*	*0*	*0*	*0*
	MTE 3	*0*	*0*	*0*	*204*	*6144*	*12*
48 x 48	*MTE 0*	*4200*	*131712*	*148*	*0*	*0*	*0*
	MTE 1	*0*	*0*	*0*	*4116*	*129024*	*148*

	MTE 2	*4200*	*131712*	*164*	*0*	*0*	*0*
	MTE 3	*0*	*0*	*0*	*4116*	*129024*	*164*
64 x 64	*MTE 0*	*9504*	*299520*	*288*	*0*	*0*	*0*
	MTE 1	*0*	*0*	*0*	*9360*	*294912*	*288*
	MTE 2	*9504*	*299520*	*288*	*0*	*0*	*0*
	MTE 3	*0*	*0*	*0*	*9360*	*294912*	*288*
96 x96	*MTE 0*	*30576*	*968448*	*708*	*0*	*0*	*0*
	MTE 1	*0*	*0*	*0*	*30264*	*958464*	*708*
	MTE 2	*30576*	*968448*	*876*	*0*	*0*	*0*
128 x 128	*MTE 0*	*70720*	*2245632*	*1632*	*0*	*0*	*0*
	MTE 1	*0*	*0*	*0*	*70176*	*2228224*	*1632*
	MTE 2	*70720*	*2245632*	*1632*	*0*	*0*	*0*
	MTE 3	*0*	*0*	*0*	*70176*	*2228224*	*1632*

Total DRAM Cycles

Matrix Size	Read Data Transactions	Read Bytes	Read Page Misses	Write Data Transactions	Write Bytes	Write Page Misses
16 x 16	*69777*	*302416*	*12142*	*29598*	*127623*	*4770*
48 x 48	*875545*	*3743984*	*135560*	*264127*	*1280199*	*63450*
64 x 64	*1898658*	*8129676*	*333820*	*541311*	*2678759*	*153911*
96 x 96	*5879461*	*25222196*	*934029*	*1587039*	*8021543*	*438843*
128 x 128	*13367755*	*57408523*	*5138038*	*3516635*	*17960146*	*1583849*

d. *Total Simulation Time*

Matrix Size	Total Simulation Cycles
16 x 16	*5667808*
48 x 48	*69005651*
64 x 64	*149065408*
96 x 96	*460003470*
128 x 128	*1044310957*

2. Using PE to do data Transfer

I. *UMS Statistics*

Matrix Size	Processor	Active Cycles	Delay Cycles	Read Wait Cycles	Instruction Cache Misses
16 x 16	*PE 0*	*6334626*	*178945*	*4317050*	*309*
	PE 1	*6334626*	*951275*	*3782500*	*83*
	PE 2	*6334626*	*975260*	*3759350*	*73*
	PE 3	*6334626*	*1019460*	*3716750*	*73*
48 x 48	*PE 0*	*89629367*	*871390*	*62867650*	*309*
	PE 1	*89629367*	*15264795*	*52554100*	*84*
	PE 2	*89629367*	*15277860*	*52523950*	*73*
	PE 3	*89629367*	*15303795*	*52480200*	*72*
64 x 64	*PE 0*	*198092271*	*1468350*	*139834450*	*309*
	PE 1	*198092271*	*34368945*	*115968850*	*84*
	PE 2	*198092271*	*34367580*	*115934600*	*73*
	PE 3	*198092271*	*34381490*	*115887200*	*72*
96 x 96	*PE 0*	*625513563*	*3135210*	*444447800*	*309*
	PE 1	*625513563*	*110370195*	*365577350*	*85*
	PE 2	*625513563*	*110323915*	*365544300*	*73*
	PE 3	*625513563*	*110283030*	*365501100*	*73*
128 x 128	*PE 0*	*1435521587*	*5547750*	*1023686200*	*309*
	PE 1	*1435521587*	*255072805*	*838311750*	*85*
	PE 2	*1435521587*	*255013785*	*838228300*	*73*
	PE 3	*1435521587*	*254864675*	*838223750*	*72*

Data Cache Misses = *0*

II. *Local Bus Statistics*

Matrix Size	Processor	Local Bus Utilization	Local Bus Read Transactions	Local Bus Read Bytes	Local Bus Write Transactions	Local Bus Write Bytes
16 x 16	*PE 0*	*3.358%*	*49623*	*105173*	*19258*	*76207*
	PE 1		*41429*	*84381*	*5423*	*21476*
	PE 2		*42255*	*86201*	*5450*	*21584*
	PE 3		*43767*	*89369*	*5484*	*21720*
48 x 48	*PE 0*	*3.157%*	*726563*	*1632909*	*296483*	*1185107*
	PE 1		*560885*	*1175805*	*38863*	*155236*
	PE 2		*562697*	*1181085*	*39367*	*157252*
	PE 3		*564697*	*1186669*	*39814*	*159040*
64 x 64	*PE 0*	*3.146%*	*1619663*	*3658773*	*663116*	*2651639*
	PE 1		*1237625*	*2604405*	*75651*	*302388*
	PE 2		*1239651*	*2611433*	*76482*	*305712*

	PE 3		*1242507*	*2620025*	*77374*	*309280*
96 x 96	*PE 0*	*3.139%*	*5158197*	*11704961*	*2118411*	*8472819*
	PE 1		*3902733*	*8244029*	*209579*	*838100*
	PE 2		*3907921*	*8261173*	*211934*	*847520*
	PE 3		*3911341*	*8274637*	*213851*	*855188*
128 x 128	*PE 0*	*3.137%*	*11900101*	*27056696*	*4892109*	*19567602*
	PE 1		*8949445*	*18941005*	*451517*	*1805852*
	PE 2		*8958551*	*18971313*	*455584*	*1822120*
	PE 3		*8963235*	*18992585*	*459266*	*1836848*

Total Local Bus Cycles

Matrix Size	Local Bus Read Transactions	Local Bus Read Bytes	Local Bus Write Transactions	Local Bus Write Bytes
16 x 16	*177074*	*365124*	*35615*	*140987*
48 x 48	*2414842*	*5176468*	*414527*	*1656635*
64 x 64	*5339446*	*11494636*	*892623*	*3569019*
96 x 96	*16880192*	*36484800*	*2753775*	*11013627*
128 x 128	*38771332*	*83961599*	*6258476*	*25032422*

III. *DRAM Statistics*

Matrix Size	Processor	Read Data Transactions	Read Bytes	Read Page Misses	Write Data Transactions	Write Bytes	Write Page Misses
16 x 16	*PE 0*	*21479*	*92573*	*1431*	*15531*	*61343*	*532*
	PE 1	*18559*	*76113*	*1436*	*4872*	*19272*	*553*
	PE 2	*18271*	*74681*	*4554*	*4873*	*19276*	*2014*
	PE 3	*17747*	*72585*	*4623*	*4875*	*19284*	*2109*
48 x 48	*PE 0*	*313481*	*1260581*	*93881*	*220710*	*882059*	*60633*
	PE 1	*261504*	*1047921*	*40942*	*28104*	*112200*	*11854*
	PE 2	*261128*	*1046109*	*31487*	*28312*	*113032*	*2878*
	PE 3	*260634*	*1044105*	*20710*	*28497*	*113772*	*2210*
64 x 64	*PE 0*	*697715*	*2797517*	*213754*	*490341*	*1960583*	*126005*
	PE 1	*577739*	*2312861*	*80925*	*51076*	*204088*	*4795*
	PE 2	*577410*	*2311237*	*102042*	*51449*	*205580*	*30008*
	PE 3	*576857*	*2308997*	*70964*	*51837*	*207132*	*30130*
96 x 96	*PE 0*	*2219475*	*8884557*	*660362*	*1558162*	*6231867*	*361597*
	PE 1	*1823396*	*7295517*	*265059*	*129884*	*519320*	*88490*
	PE 2	*1822863*	*7293049*	*266637*	*130941*	*523548*	*88619*

	PE 3	*1822557*	*7291825*	*126168*	*131844*	*527160*	*8312*
128 x 128	*PE 0*	*5113075*	*20458948*	*2422644*	*3590397*	*14360802*	*136 8835*
	PE 1	*4184136*	*16738477*	*1413995*	*266242*	*1064752*	*13372*
	PE 2	*4183058*	*16733829*	*1507441*	*268131*	*1072308*	*196058*
	PE 3	*4183238*	*16734521*	*532641*	*269881*	*1079308*	*196109*

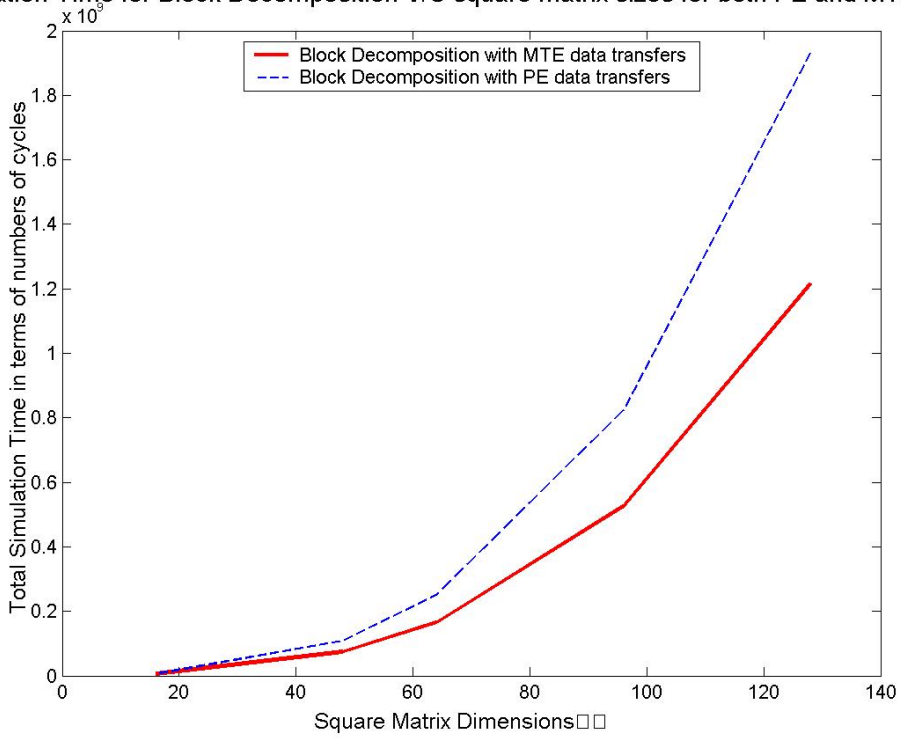
Total DRAM Cycles

Matrix Size	Read Data Transactions	Read Bytes	Read Page Misses	Write Data Transactions	Write Bytes	Write Page Misses
16 x 16	*76056*	*315952*	*12044*	*30151*	*119175*	*5208*
48 x 48	*1096747*	*4398716*	*187020*	*305623*	*1221063*	*77575*
64 x 64	*2429721*	*9730612*	*467685*	*644703*	*2577383*	*190938*
96 x 96	*7688291*	*30764948*	*1318226*	*1950831*	*7801895*	*547018*
128 x 128	*17663507*	*70665775*	*5876721*	*4394651*	*17577170*	*1774374*

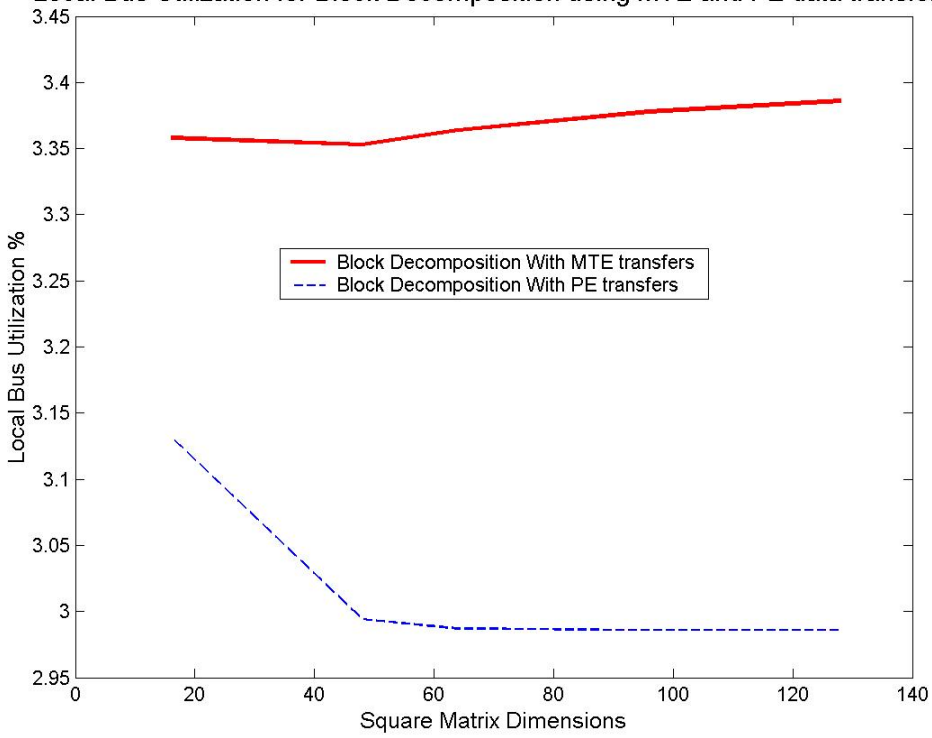
IV. *Total Simulation Time*

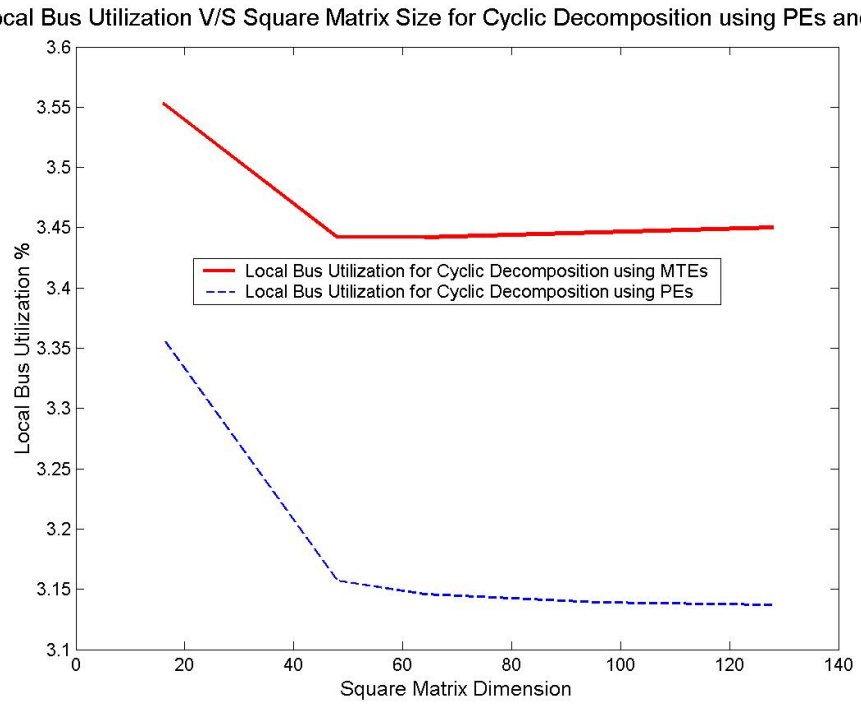
Matrix Size	Total Simulation Cycles
16 x 16	*6334646*
48 x 48	*89629369*
64 x 64	*198092289*
96 x 96	*625513591*
128 x 128	*1435521624*

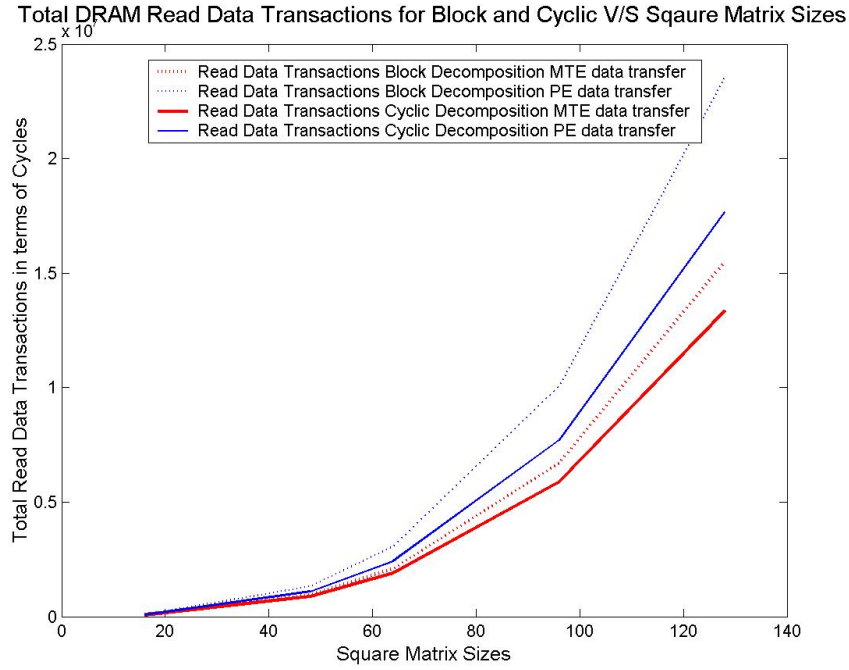
Simulation Time for Block Decomposition V/S square matrix sizes for both PE and MTE data

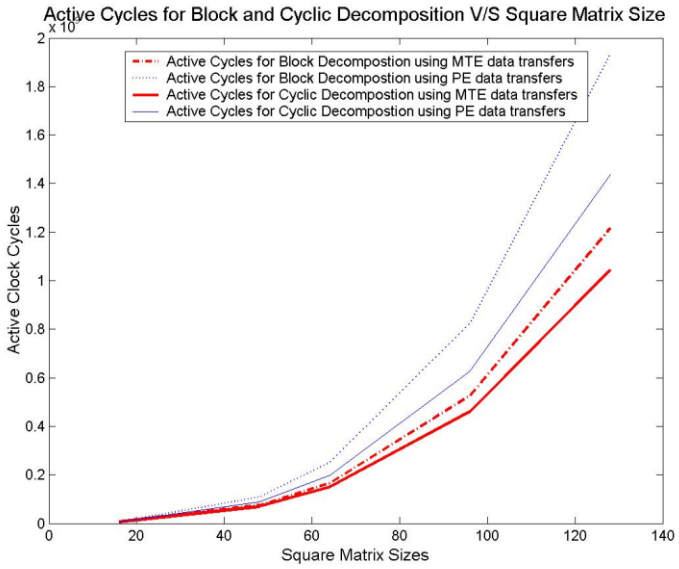


Local Bus Utilization for Block Decomposition using MTE and PE data transfers




Local Bus Utilization V/S Square Matrix Size for Cyclic Decomposition using PEs and MTEs
Local Bus Utilization for Cyclic Decomposition using MTEs
Local Bus Utilization for Cyclic Decomposition using PEs
Local Bus Utilization %
Square Matrix Dimension
3.6
3.55
3.5
3.45
3.4
3.35
3.3
3.25
3.2
3.15
3.1
0
20
40
60
80
100
120
140


Total DRAM Read Data Transactions for Block and Cyclic V/S Sqaure Matrix Sizes
x 10
Read Data Transactions Block Decomposition MTE data transfer
Read Data Transactions Block Decomposition PE data transfer
Read Data Transactions Cyclic Decomposition MTE data transfer
Read Data Transactions Cyclic Decomposition PE data transfer
Total Read Data Transactions in terms of Cycles
Square Matrix Sizes
2.5
2
1.5
1
0.5
0
0
20
40
60
80
100
120
140



V. *Summary of results from the above graphs and tables*

1. LU Decomposition would work faster i.e. reduced active cycles if an attempt is made to put maximum possible matrix data in the local memory rather than the slow SDRAM. This can be verified with graphs showing the variation of active clock cycles, local bus utilization, read wait cycles and delay cycles with increasing matrix sizes.
2. For Block Decomposition, increasing the local_mat_row matrix size would enable one to bring a larger chunk of the matrix from SDRAM. In this case, Block Decomposition will almost be like row-cyclic except here rows are blocks. However, a compromise has to be made between local bus utilization time and the active clock cycles available for each PE.
3. For Cyclic Decomposition, increasing matrix sizes will degrade its performance more in comparison to Block Decomposition.
4. Square Matrices of dimension less than 55 have almost the same performance for both Cyclic and Block Decomposition with PE and/OR MTE data transfers.
5. PE data transfers are worst in comparison to MTE data transfers with respect to the local bus utilization times, for both the cyclic and block decomposition.

VI. *Probable UMS Inspector Bugs*

My code works fine only when the profiling option is turned on in the Inspector. When the profiling option is not turned ON, the code hangs inside the barrier. The logic of the barrier function has been tested positive. Here, is my implementation of barrier …

```
/*
 * barrier(int k, int my_peid)
 *
 * The Barrier Function implements a barrier for synchronizing all
 * the intermediate results of one PE for use by other PEs.  It
 * uses the global semaphore to check how many PEs have entered the barrier.
 * The last PE to enter the barrier then Frees all other waiting Processes
 * including itself ...
*/
void barrier(int k, int my_peid)
{
  int toOpenBarrier = -1;
  int tempDone;

semaphore_lock(CheckSem.p);

  tempDone = done_pe;
  tempDone++;
  if(tempDone == PES)
     toOpenBarrier = my_peid;
  else
    done_pe++;

semaphore_unlock(CheckSem.p);

 while (done_pe < PES)
 {
    if(toOpenBarrier != -1)
     {
       semaphore_lock(CheckSem.p);
       done_pe++;
       semaphore_unlock(CheckSem.p);
     }
  _pe_delay(1);
}

if(toOpenBarrier != -1)
 {
   semaphore_lock(CheckSem.p);
  done_pe=0;
  //printf("\n PE %d has reinitialized done_pe to 0\n",my_peid);
  semaphore_unlock(CheckSem.p);
 }

 }// end of barrier.
```

VII. Conclusions

LU decomposition can be parallelized efficiently and such parallel algorithms are already available. Reducing complex problems to matrix form and then applying various operators on them in a parallelized manner can provide efficiency depending upon various factors like

a. Parallel Algorithm
b. Architecture on which it will be run, in this case, it was the Cradle's UMS (Sizes of Caches, PEs, bus efficiency etc)
c. Size of the matrix, and its dependencies.