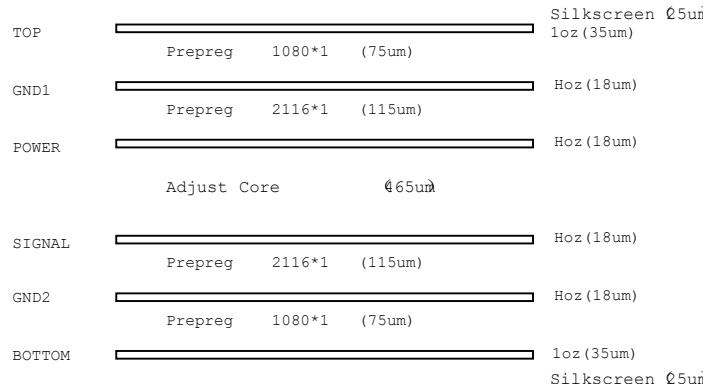


ROCK_PI_4_MODEL_B_V1.1

CONTENT INDEXING

- 01.Index
- 02.Change List
- 03.Power Tree
- 04.I2C Map
- 05.Power Domain Map
- 06.RK3399 Power
- 07.RK3399 PMU Controller
- 08.RK3399 DDR Controller
- 09.RK3399 Flash&SDMMC Controller
- 10.RK3399 USB/USIC Controller
- 11.RK3399 SARADC/Key
- 12.RK3399 DVP Interface
- 13.RK3399 Display Interface
- 14.RK3399 GPIO
- 15.RK3399 PCIE
- 16.Power-DC IN
- 17.Power-PMIC RK808-D
- 18.USB OTG/HOST Port
- 19.USB Type-C Port
- 20.RAM-LPDDR3(178P)
- 21.Memory-eMMC
- 22.WIFI/BTMIMO-AP6354
- 23.TF Card
- 24.HDMI Output
- 25.PCle NGFF/M.2
- 26.CONNECTOR

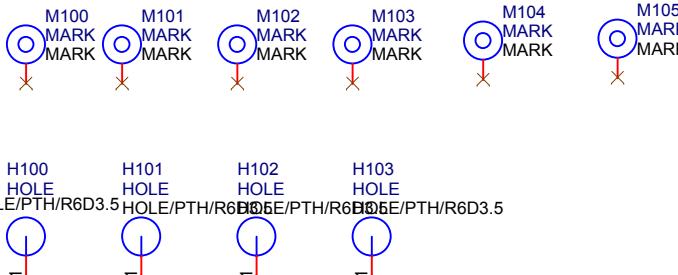
6 LAYERS PCB STACK e.g. PCB=16 mm



Note:

器件参数说明

1:如果 Value 为 DP, 说明暂时不贴。
2:如果 Option 有 DP, 说明预留先不贴。



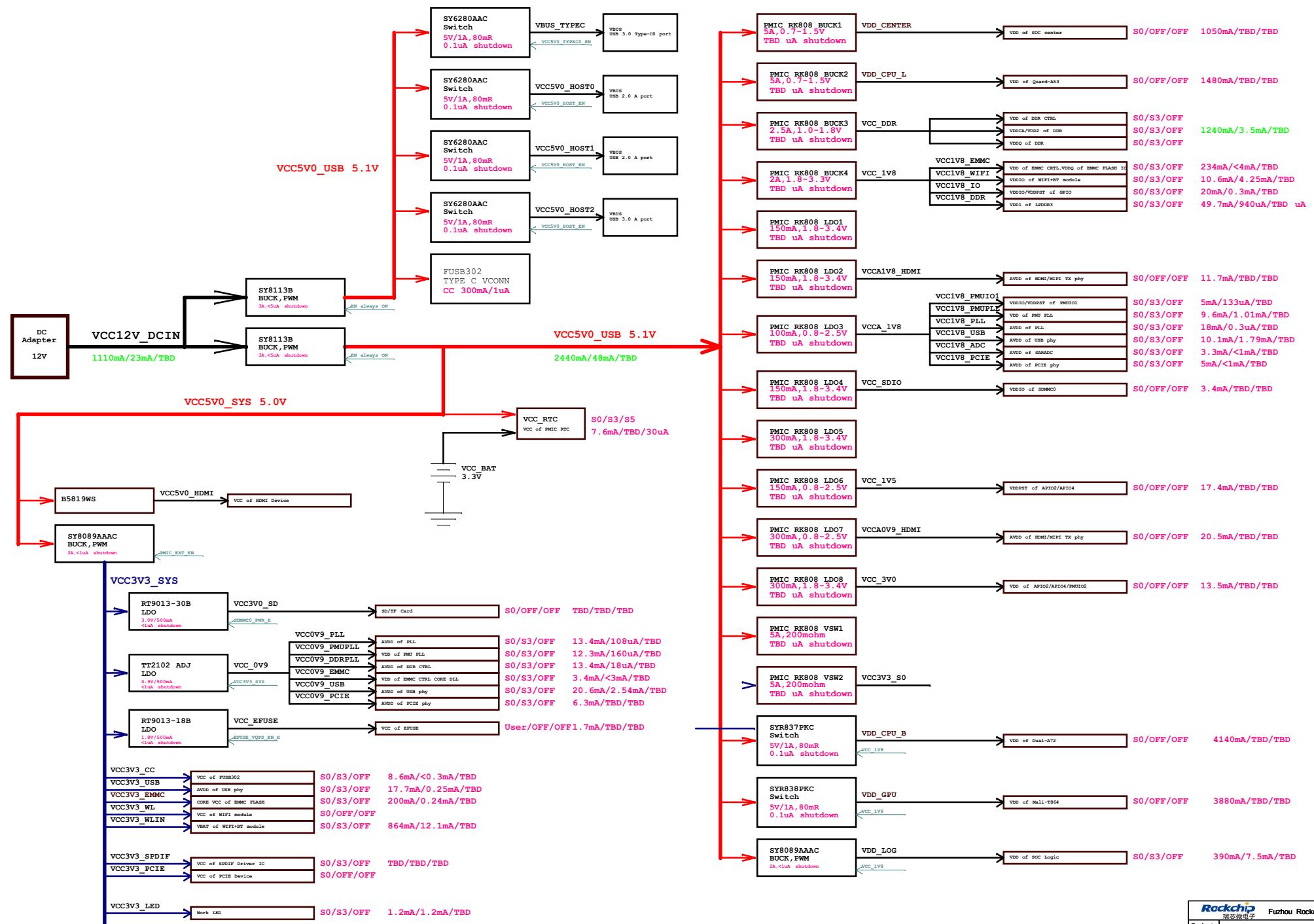
	Fuzhou Rockchip Electronics
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Change List

Version	Date	Author	Change Note	Approved
V1.0	201708	Charlie	First edition	



RK3399 POWER DIAGRAM

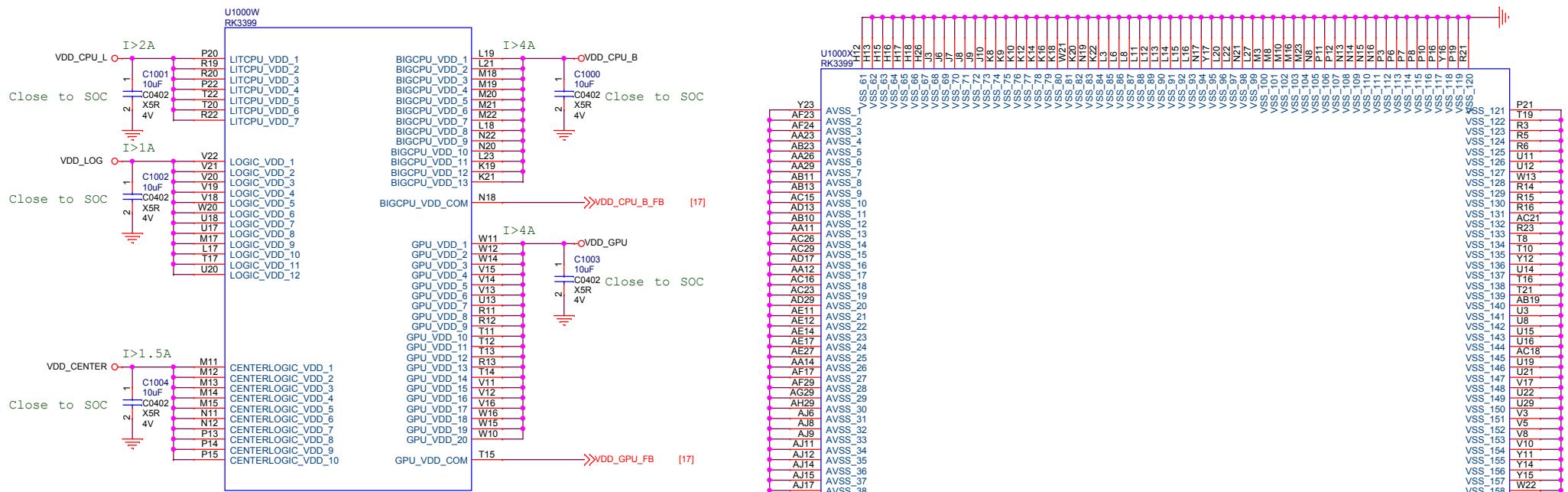


I2C MAP

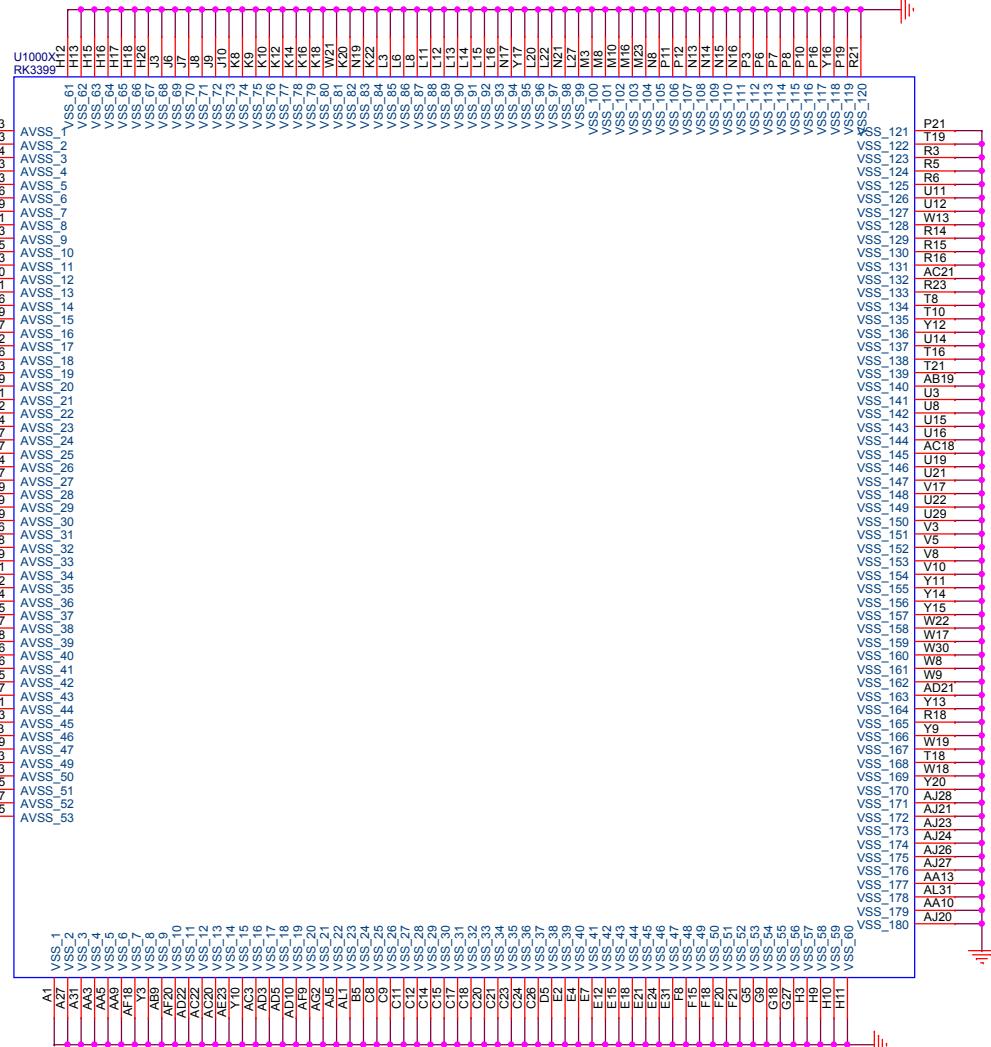
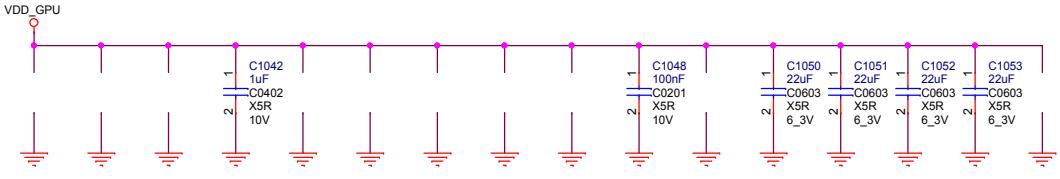
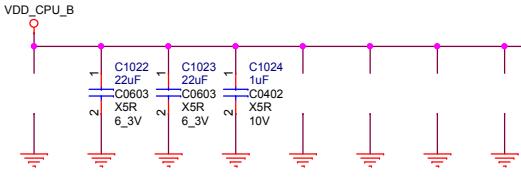
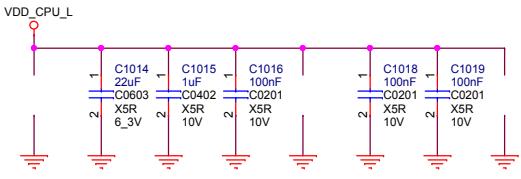
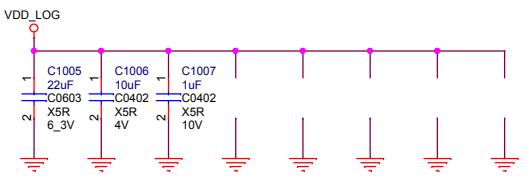
Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_1V8	Rockchip RK808	0x1b	PMIC	100kHz, 400kHz
					SYR837PKC	0x40	DC-DC BUCK	100kHz, 400kHz, 3.4MHz
					SYR838PKC	0x41	DC-DC BUCK	100kHz, 400kHz, 3.4MHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5		VCC_1V8			Low Speed CONNECTOR	
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2		VCC_1V8			High Speed CONNECTOR	
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C_SDA_HDMI I2C_SCL_HDMI	VCC_3V0				
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C_SDA_MEMS I2C_SCL_MEMS	VCC_1V8	Fairchild FUSB302B	0x44, 0x46	USB-TypeC Mux	100kHz, 400kHz, 1MHz
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	Other pin function					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2		VCC_1V8			Low Speed CONNECTOR	
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2		VCC_1V8			High Speed CONNECTOR	

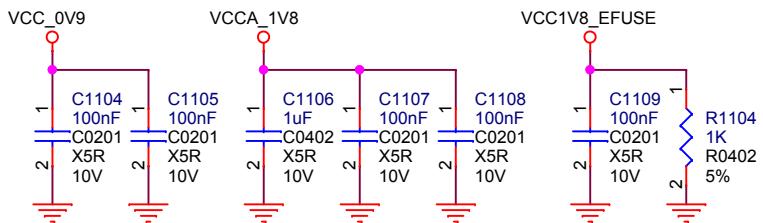
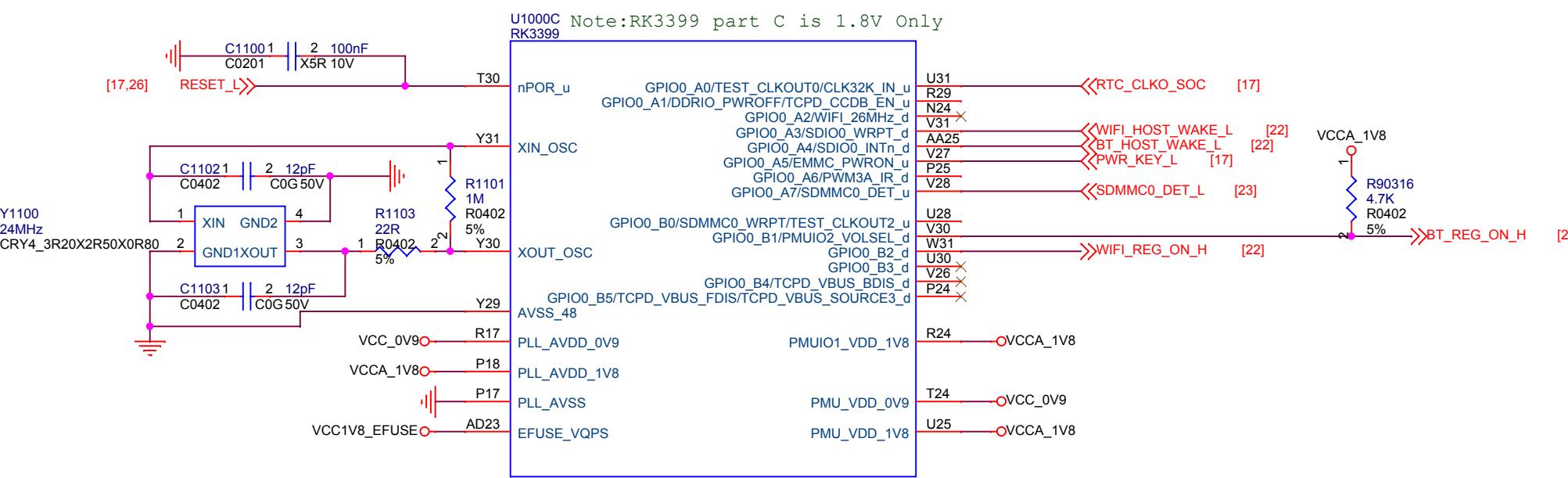
Power Domain Map

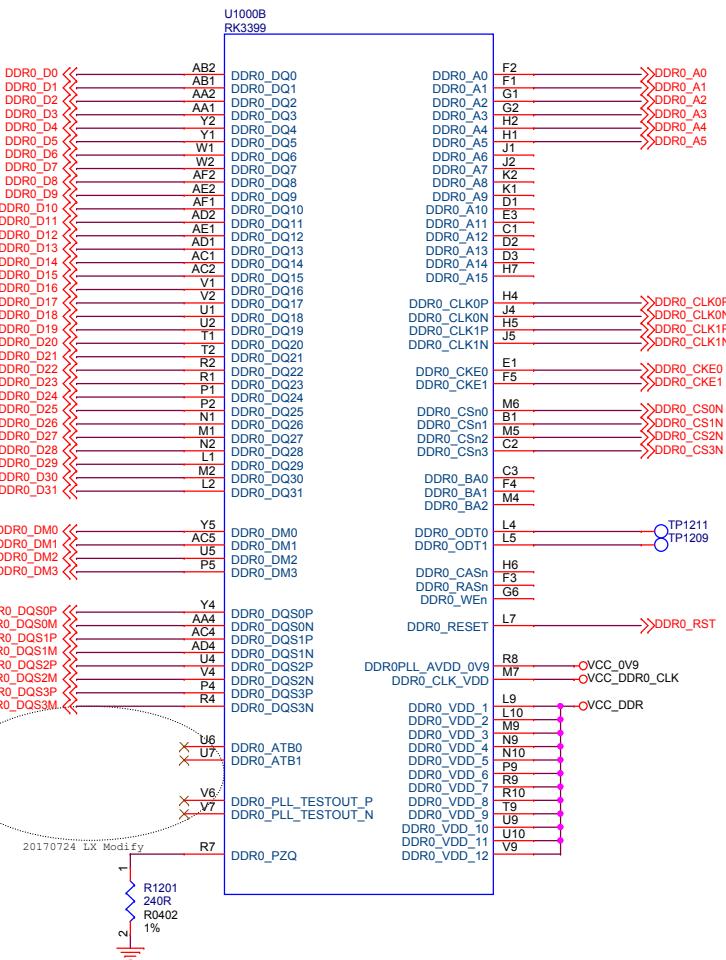
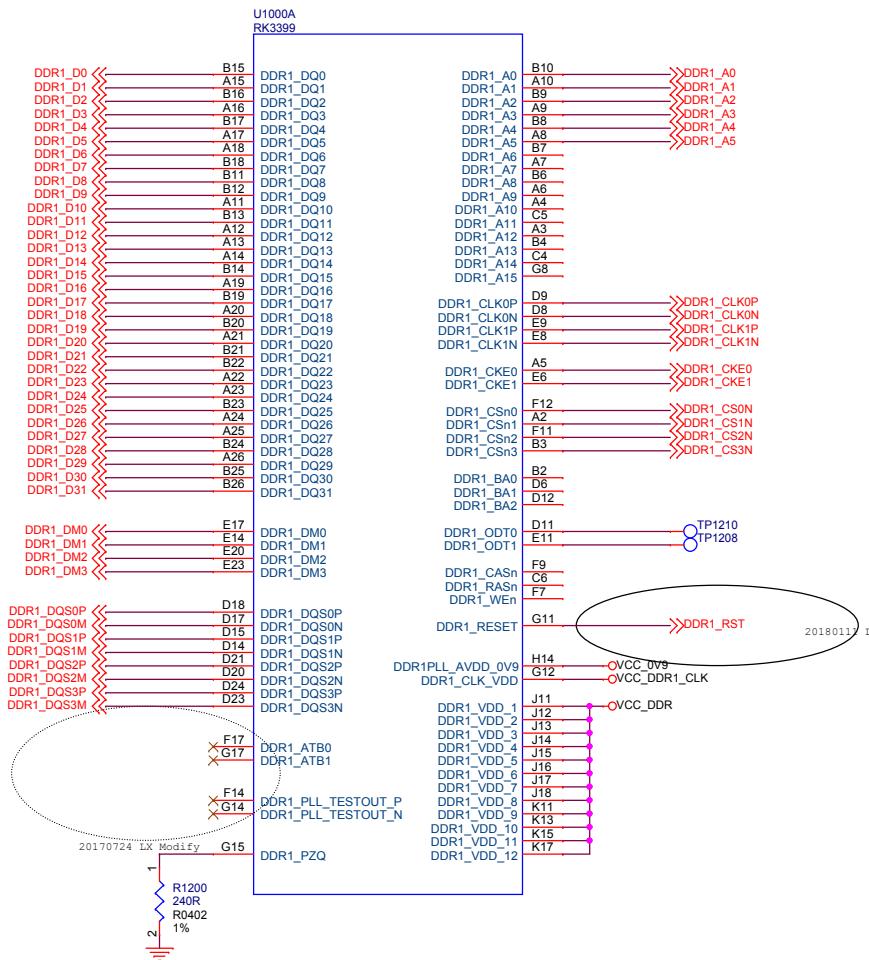
Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUIO1	pmui01_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLDO3
Part E	PMUIO2	pmu1830_gpio1abcd	1.8V(Default) 3.0V	VCC_1V8	RK808-D Buck4
Part I	APIO1	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_SYS	RK808-D Buck4
Part L	APIO2	bt656_gpio2ab	1.8V(Default) 3.0V	VCC_1V8	RK808-D VLDO3
Part G	APIO3	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	APIO4	gpio1830_gpio4cd	1.8V 3.0V(Default)	VCC_1V5 VCC_3V0	RK808-D VLDO6 RK808-D VLDO8
Part J	APIO5	audio_gpio3d_gpio4a	1.8V(Default) 3.0V	VCC_1V8	RK808-D Buck4
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V(Default)	VCC_SDIO	RK808-D VLDO4



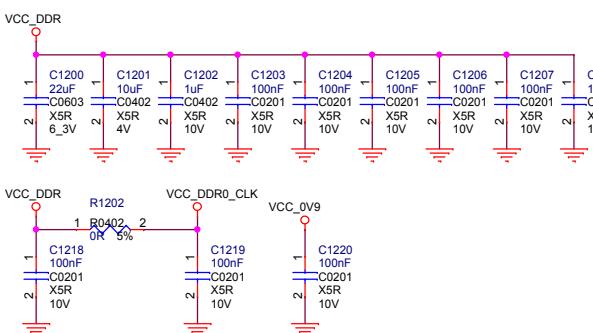
Note:Power filter CAP please place back of SOC or close to SOC



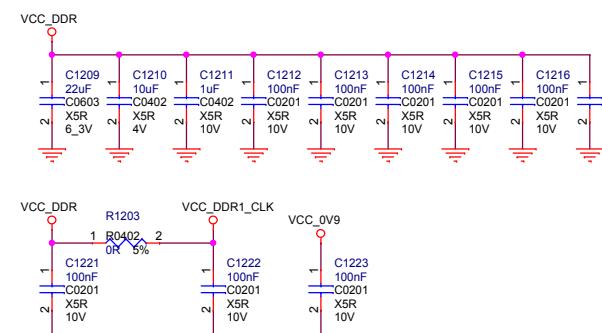


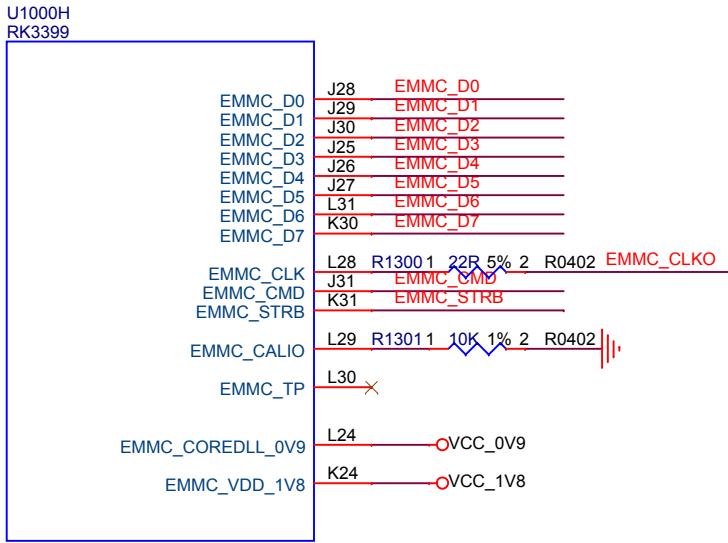


DDR FILTER Note:R1202 cannot be deleted

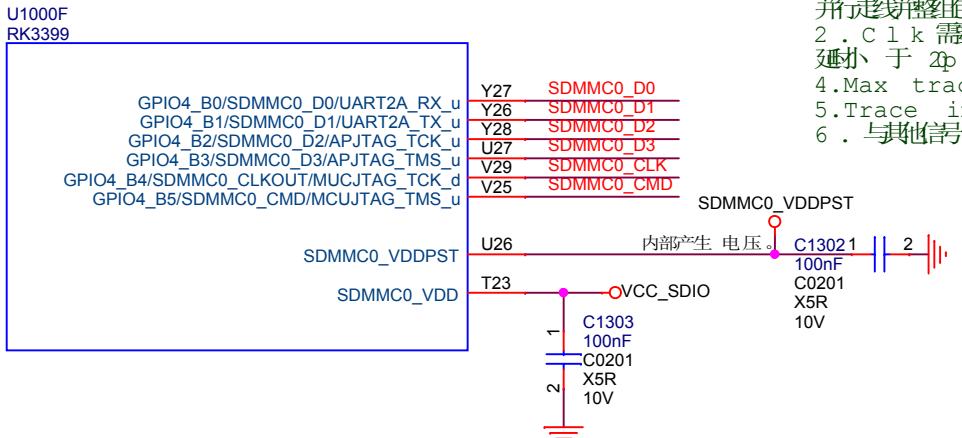
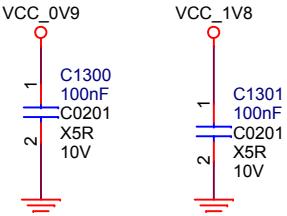
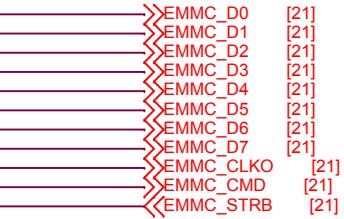


DDR FILTER Note:R1203 cannot be deleted

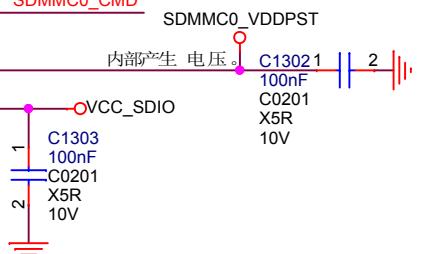
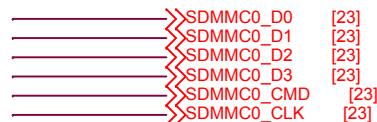




EMMC design rule:
 1. Data[0:7]、cmd strobe 做为一组，并走线整体包地，组内等长要求为 +/-100 mil；
 2. Clock 需要单独走线并包地处理，与 data 间的延时小于 20ps；
 3. Max trace length < 3.93 inches；
 4. Trace impedance 50ohm +/-10%；
 5. 与其他信号间距遵循 3W 原则；
 6. R1300 置 S0 放置；

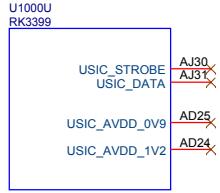


SDMMC design rule:
 1. Data[0:3]、cmd strobe 为一组，并走线整体包地，组内等长要求为 +/-100 mil；
 2. Clock 需要单独走线并包地处理，与 data 间的延时小于 20ps；
 4. Max trace length < 3.93 inches；
 5. Trace impedance 50ohm +/-10%；
 6. 与其他信号间距遵循 3W 原则；

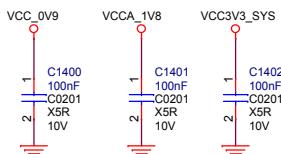
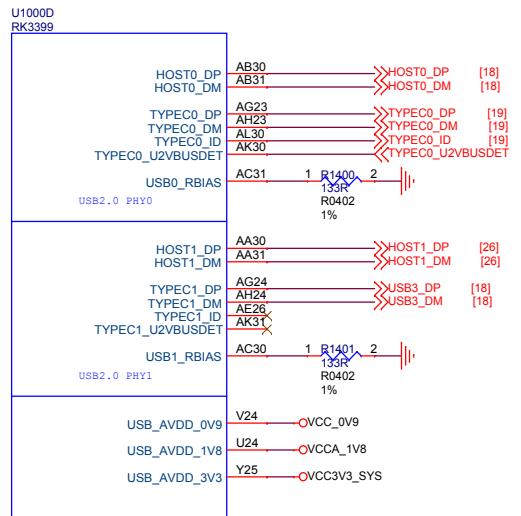


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瑞芯微电子

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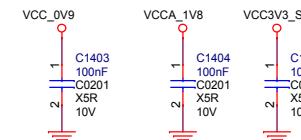
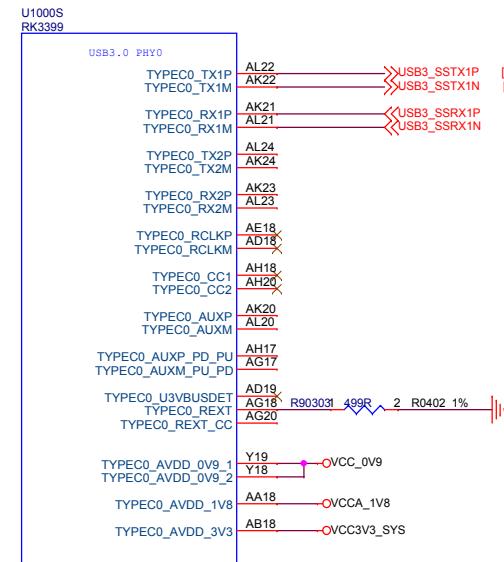


USB2.0

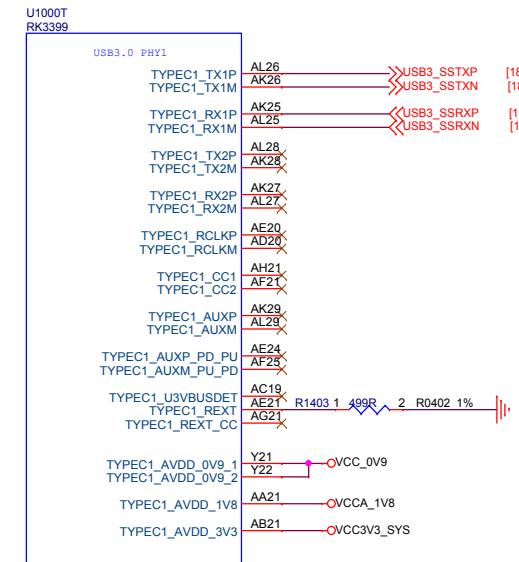


USB2.0 design rule:
 1. Max intra-pair skew < 4 ps;
 2. Max trace length < 6 inches;
 3. Max allowed via < 6;
 4. Trace impedance 90ohm +/-10%;
 5. 与其它信号间距遵循 3D 原则；

USB3.0

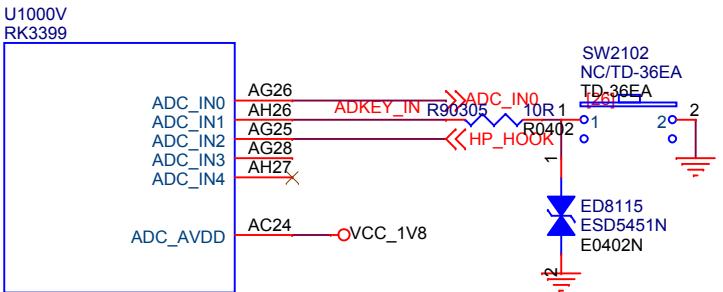


USB3.0 design rule:
 1. Max intra-pair skew < 4 ps;
 2. Max length skew between TX and RX < 1.6 ns;
 3. Max trace length < 6 inches;
 4. Max allowed via < 4;
 5. Trace impedance 90ohm +/-10%;
 6. 与其它信号间距遵循 3D 原则；



DP design rule:
 1. Max intra-pair skew < 4 ps;
 2. Max trace length < 6 inches;
 3. Max allowed via < 4;
 4. Trace impedance 90ohm +/-10%;
 5. 与其它信号间距遵循 3D 原则；

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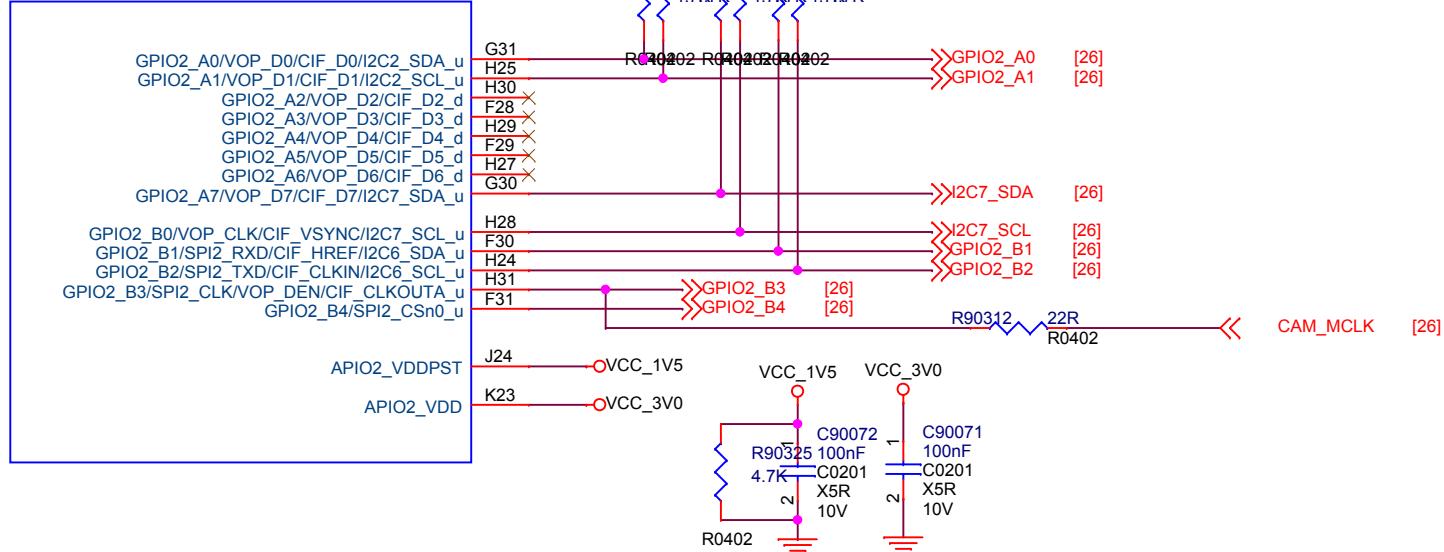
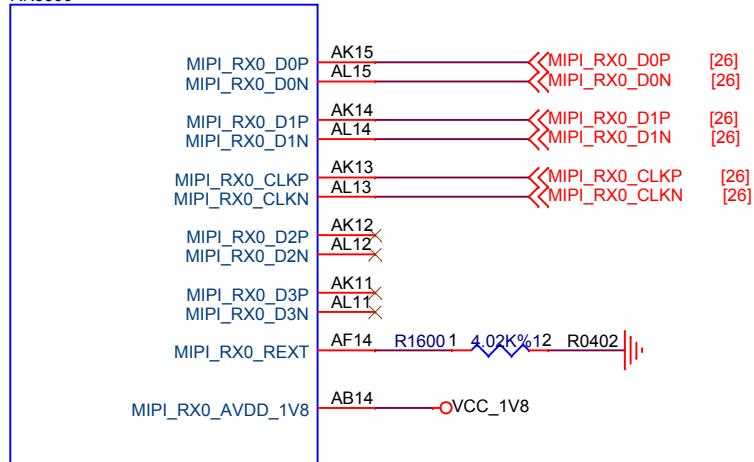
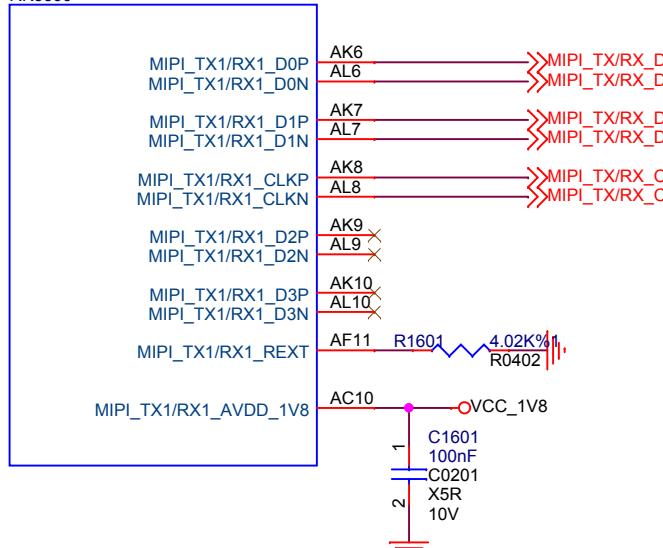
VCC_1V8
C1501
100nF
C0201
X5R
10V

KEY BAORD

Note:
 系统时，如果 ADKEY_IN 电平为 0V，
 则 RK3399 进入 Recovery 模式；
 测量时 R1503, SW1500, ED1500 不用贴片

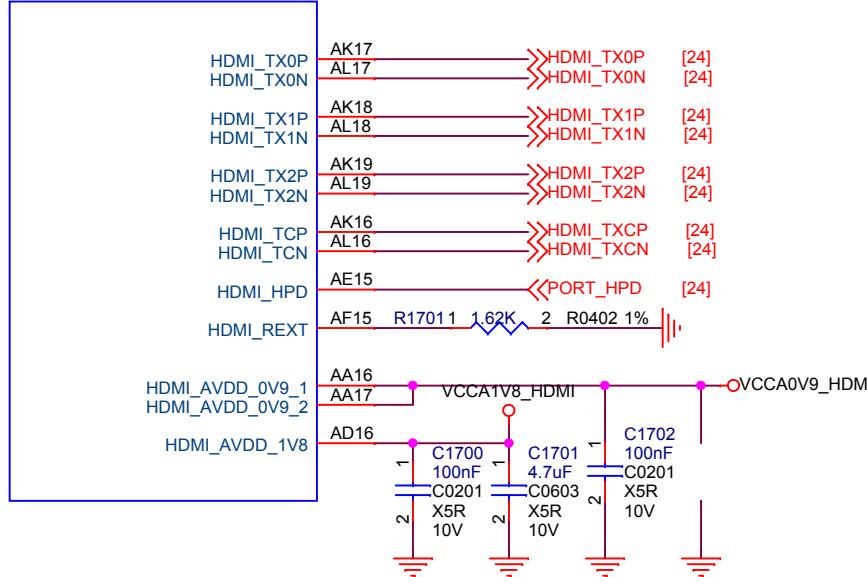
ADKEY_IN ————— R1502 1 10K 1% 2 ————— O VCC_1V8
 R0402

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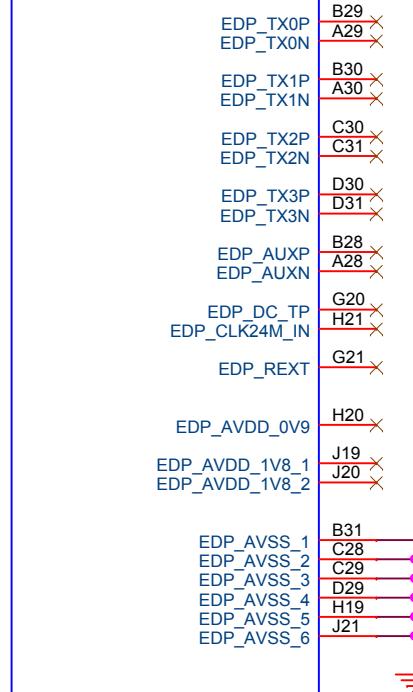
U1000L
RK3399U1000R
RK3399U1000P
RK3399Dual
MIPI
Right

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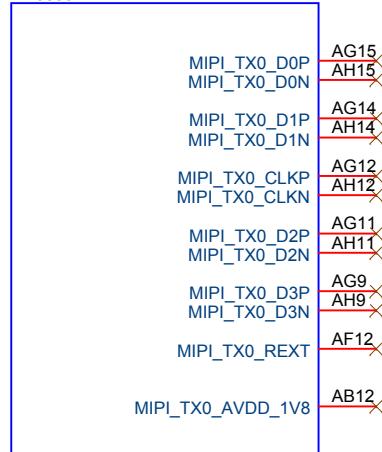
U1000N
RK3399



U1000M
RK3399



U1000Q
RK3399



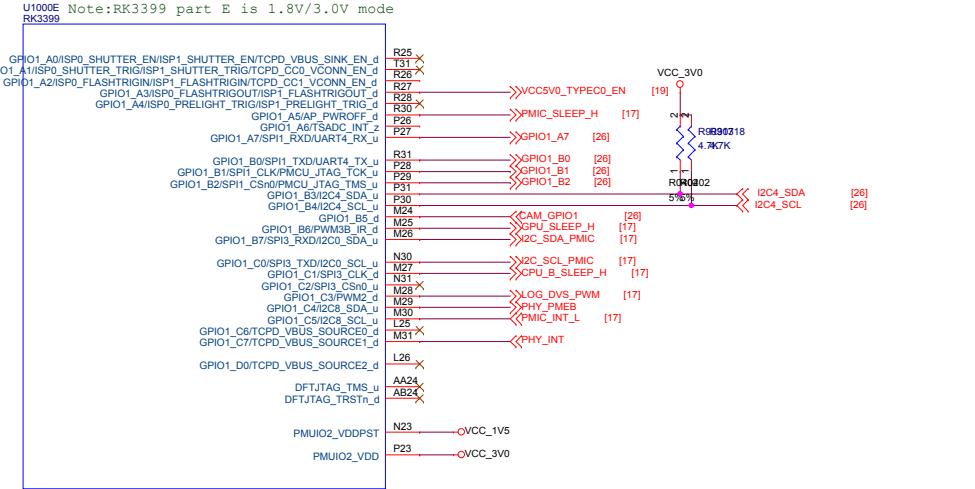
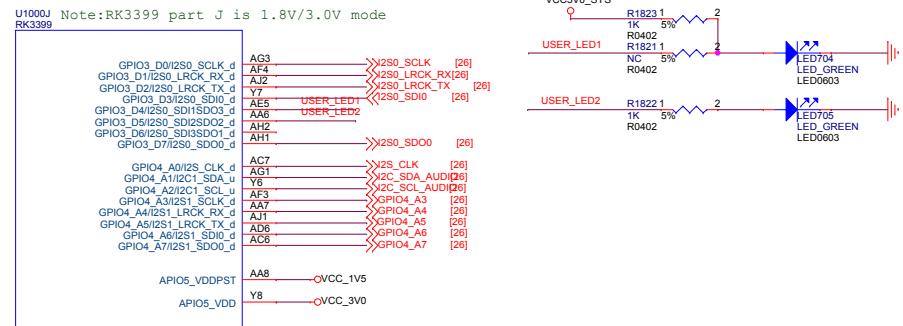
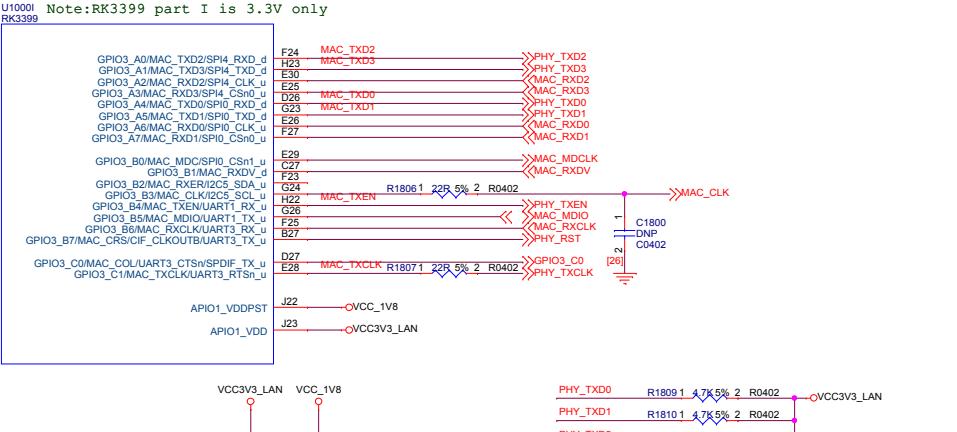
eDP design rule:

- Max intra-pair skew < 4 ps;
- Max trace length < 6 inches;
- Max allowed via < 4;
- Trace impedance 90ohm+/-10%;
- . 与其他信号间距遵循3W原则；

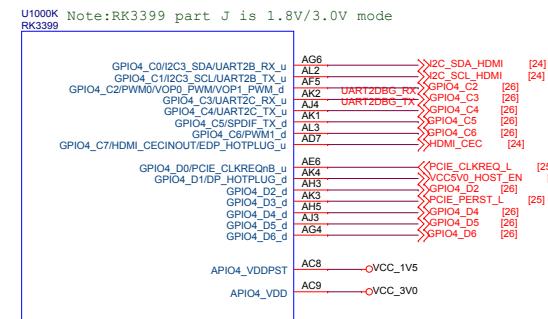
MIPI design rule:

- Max intra-pair skew < 4 ps;
- Max length skew between clk and data < 7ps;
- Max trace length < 7.2 inches;
- Max allowed via < 4;
- Trace impedance 100ohm+/-10%;
- . 与其他信号间距遵循3W原则；

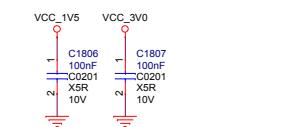
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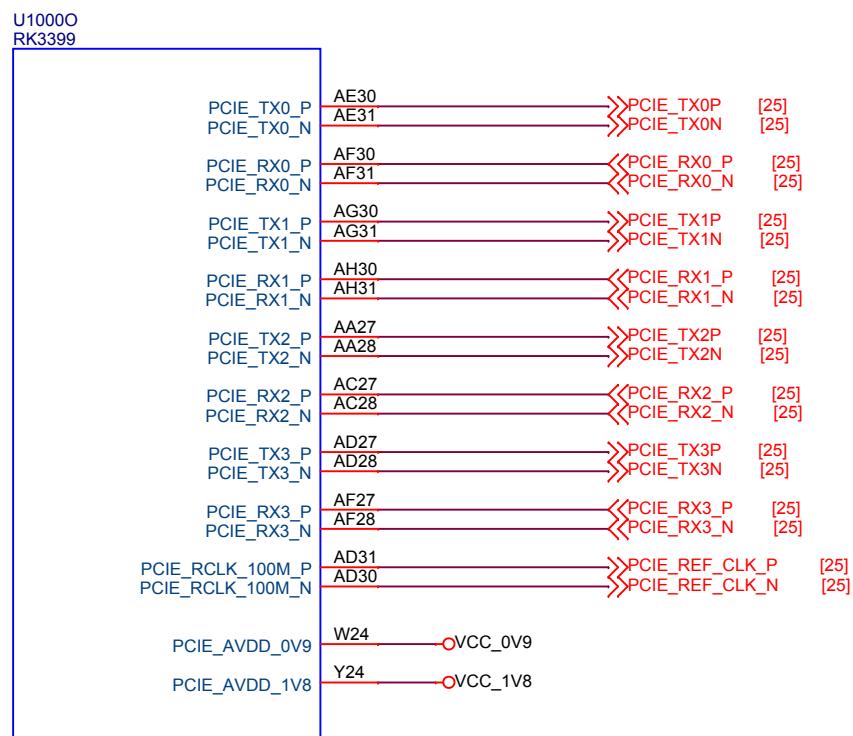


1.8V Only	VDDPST=VDDIO=1.8V
3.3V Only	VDDPST=1.8V, VDDIO=3.3V
other	3.0V mode:VDDPST=1.5V, VDDIO=3.0V 1.8V mode:VDDPST=1.8V, VDDIO=1.8V



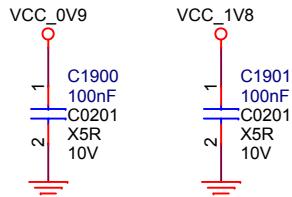
The diagram illustrates the connections between several components. A blue triangle connects SDA_PMIC (pin 1) to R1815 (pin 1). Another blue triangle connects SCL_PMIC (pin 1) to R1816 (pin 1). A red triangle connects R1815 (pin 2) to R0402 (pin 2). A red triangle connects R1816 (pin 2) to R0402 (pin 2). A red line connects R0402 (pin 3) to OVCC_3V0. A blue triangle connects R0402 (pin 4) to ground.



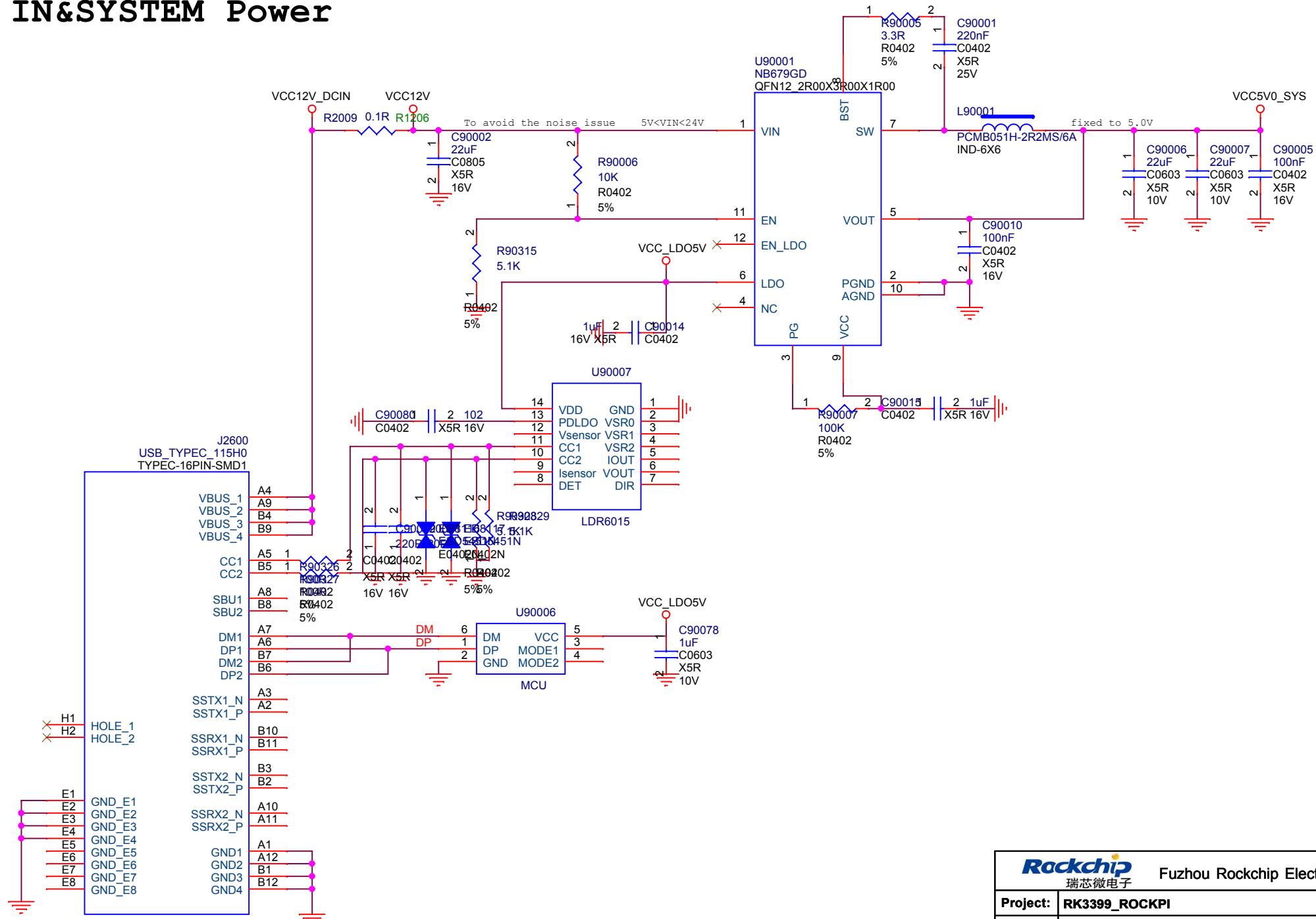


PCIE design rule:

1. Max intra-pair skew < 4ps;
2. Max inter-pair skew < 1.6 ns;
3. Max trace length < 14 inches;
4. Max allowed via < 4;
5. Trace impedance 100ohm+/-10%;
6. 与其他信号间距遵循3原 则；

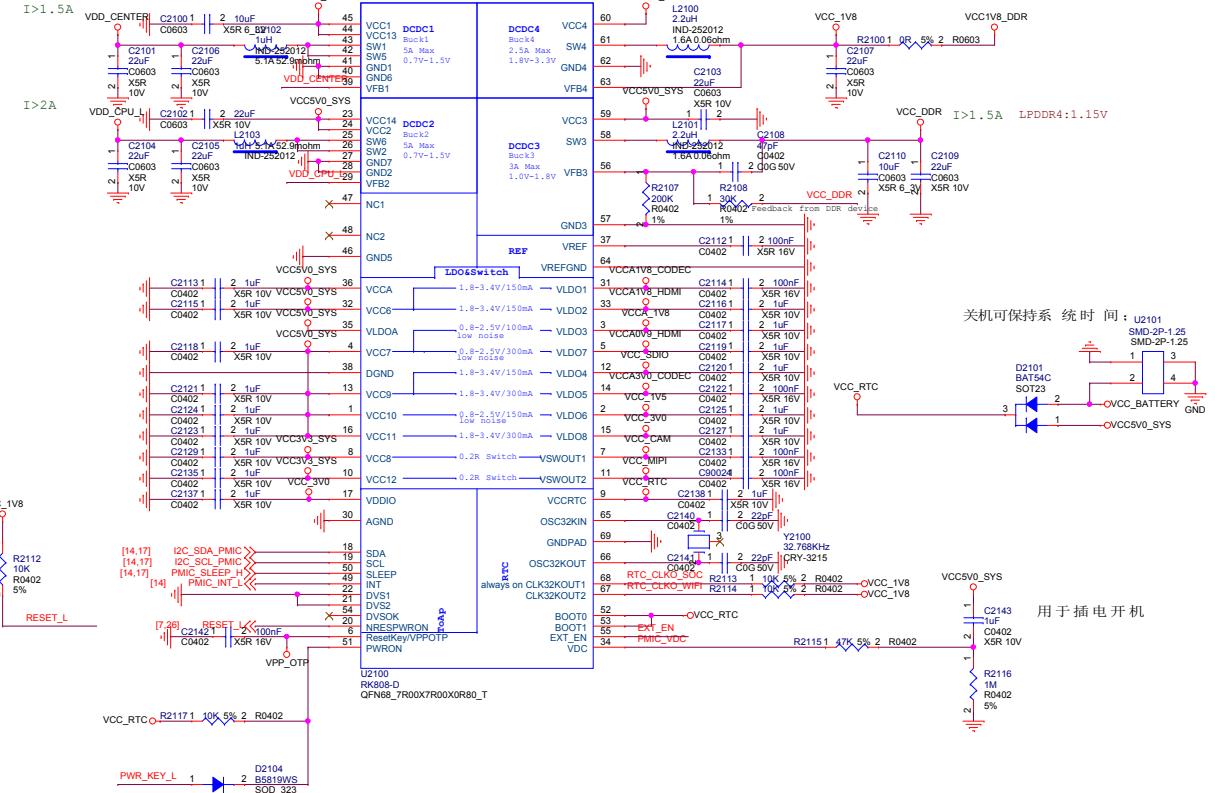


DC IN&SYSTEM Power

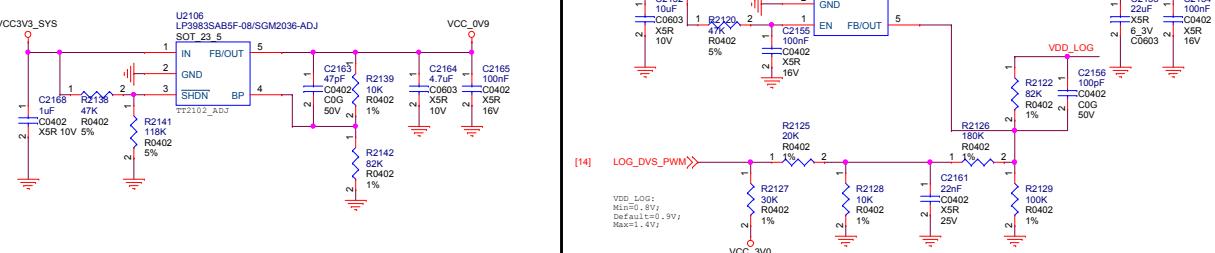


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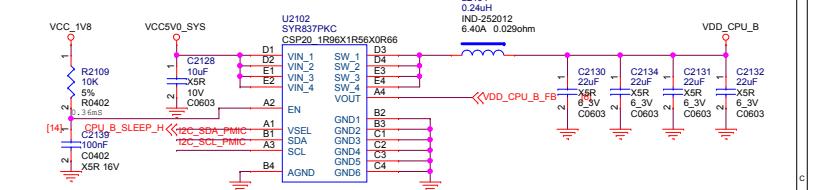
PMIC



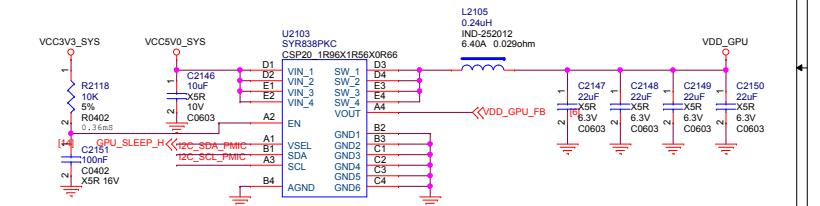
VCC 0V9 power



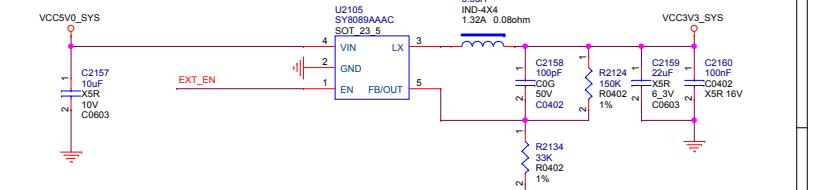
VDD CPU B power



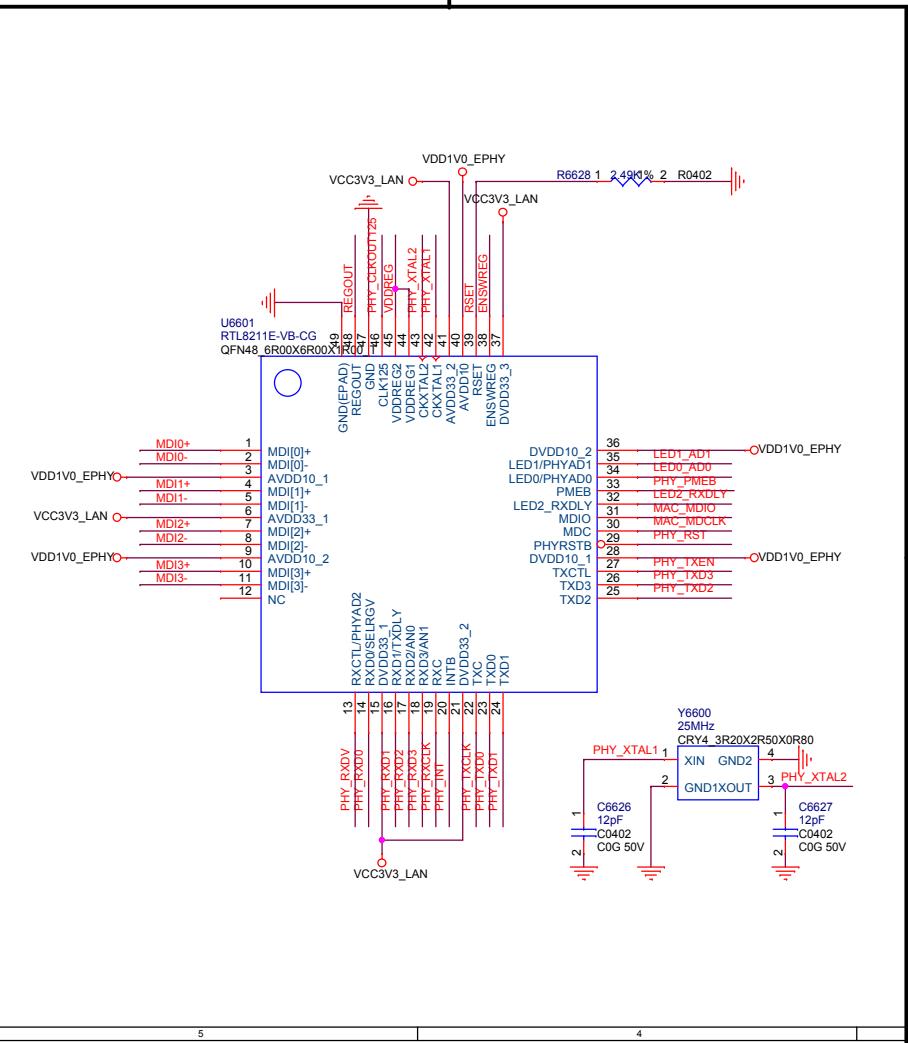
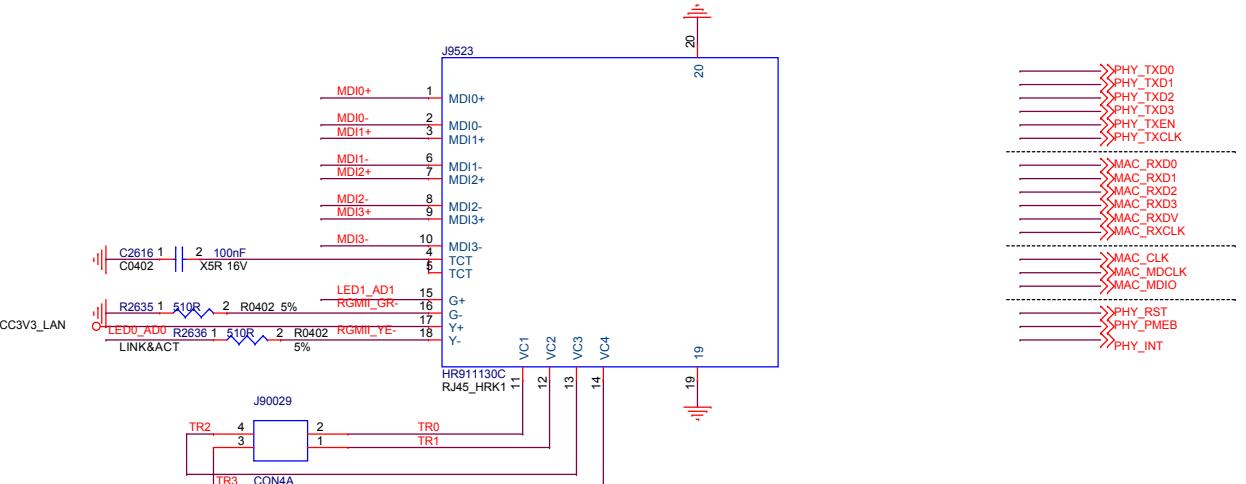
VDD GPU power



VCC3V3 SYS power



GMAC 10/100/1000 RGMII Ethernet PHY



PHY Address=001(RTL8211E)

Config for all capability

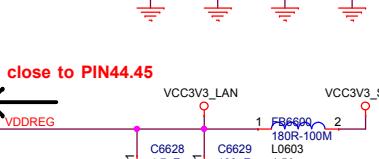
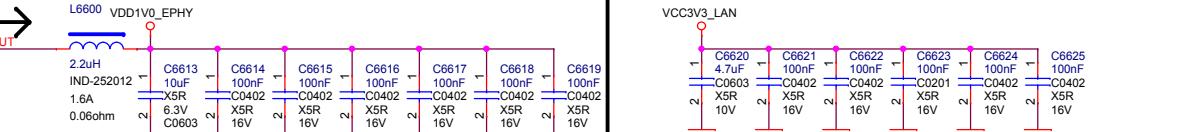
Without RX Delay

Without TX Delay

Inductance close to PIN48

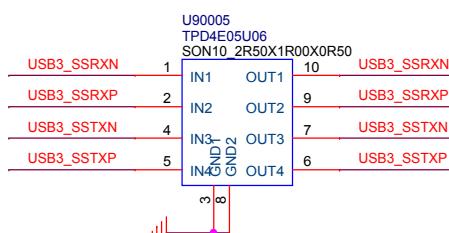
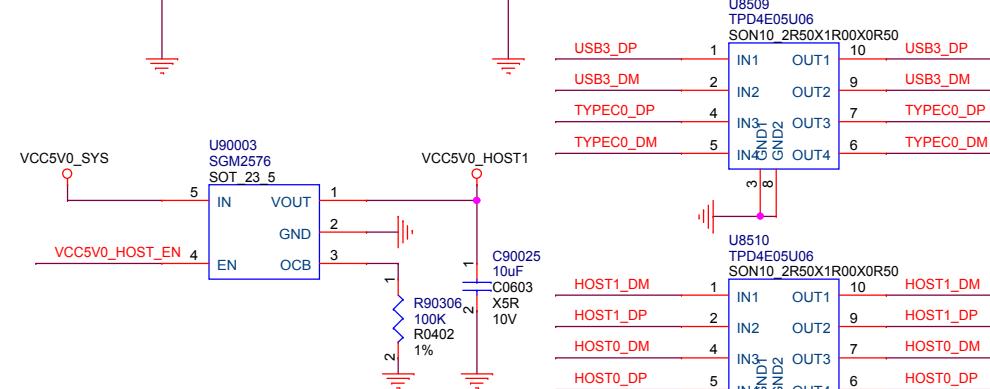
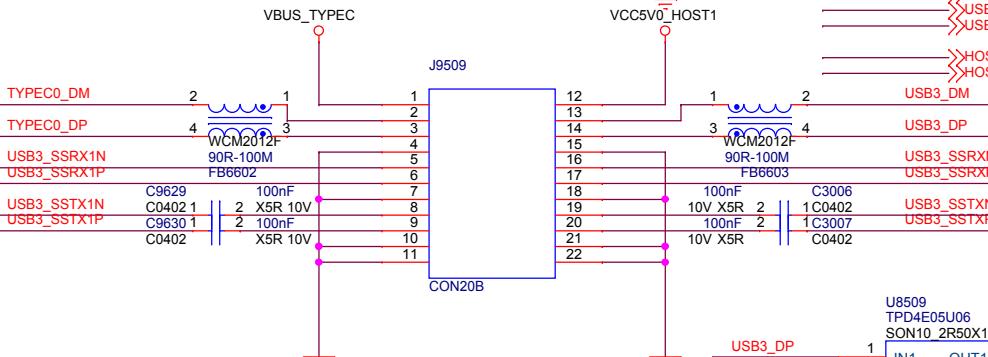
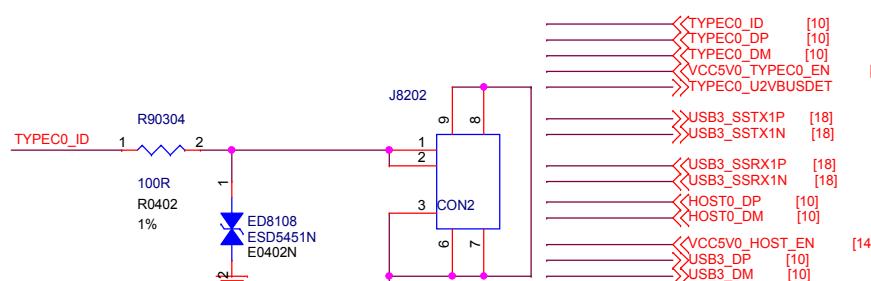
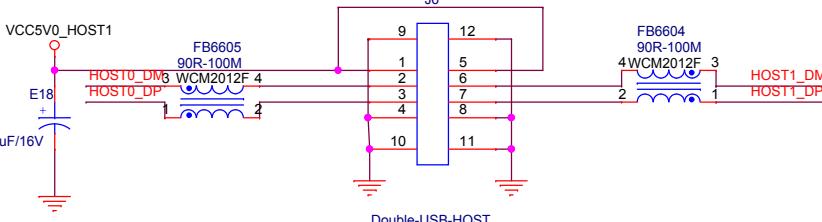
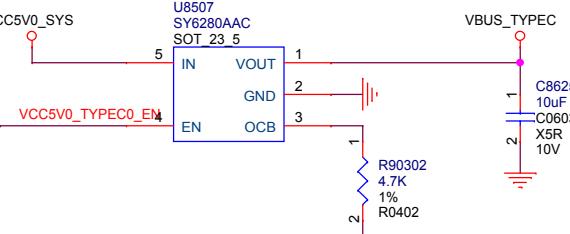
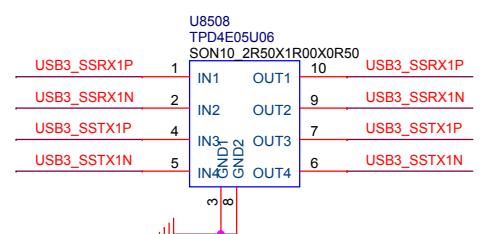
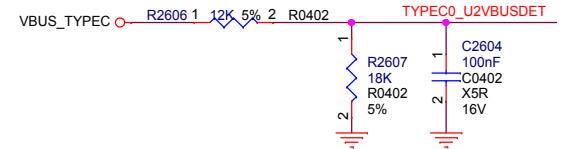
CAP. close to PIN44,45

Connect ENSWREG to AVDD33 to enable Switching regulator or connect ENSWREG to GND to disable Switching regulator.

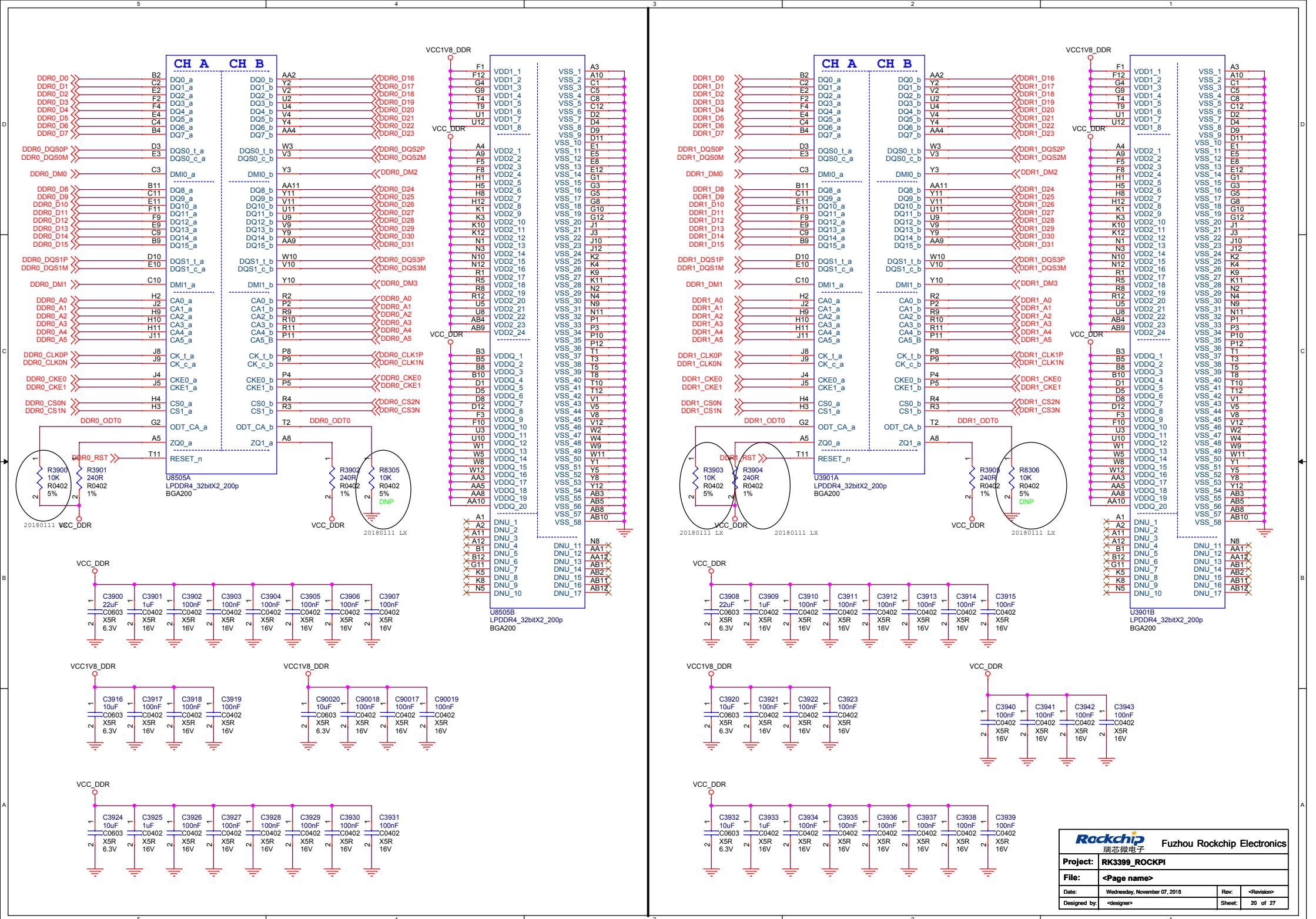


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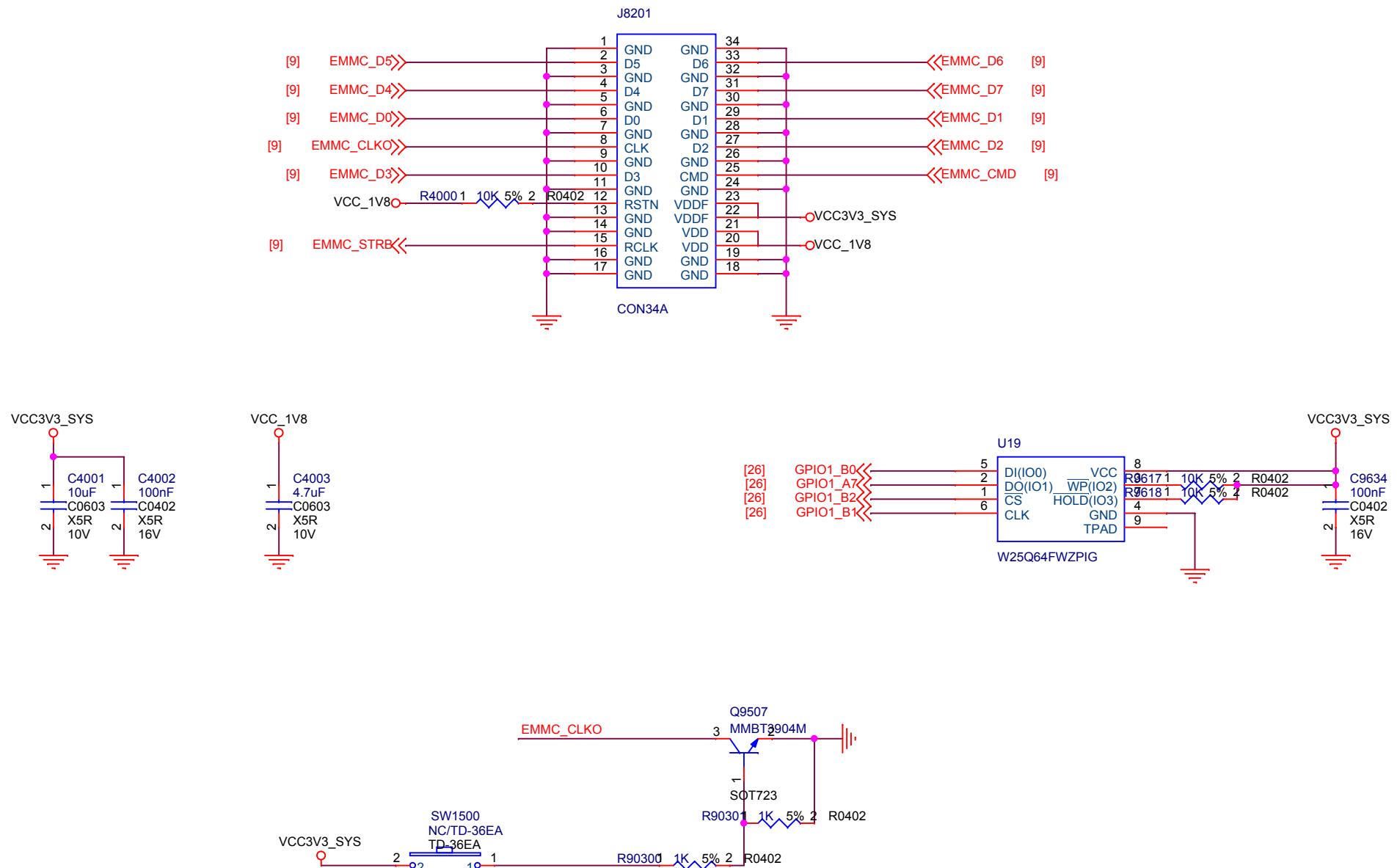
USB3.0 OTG port

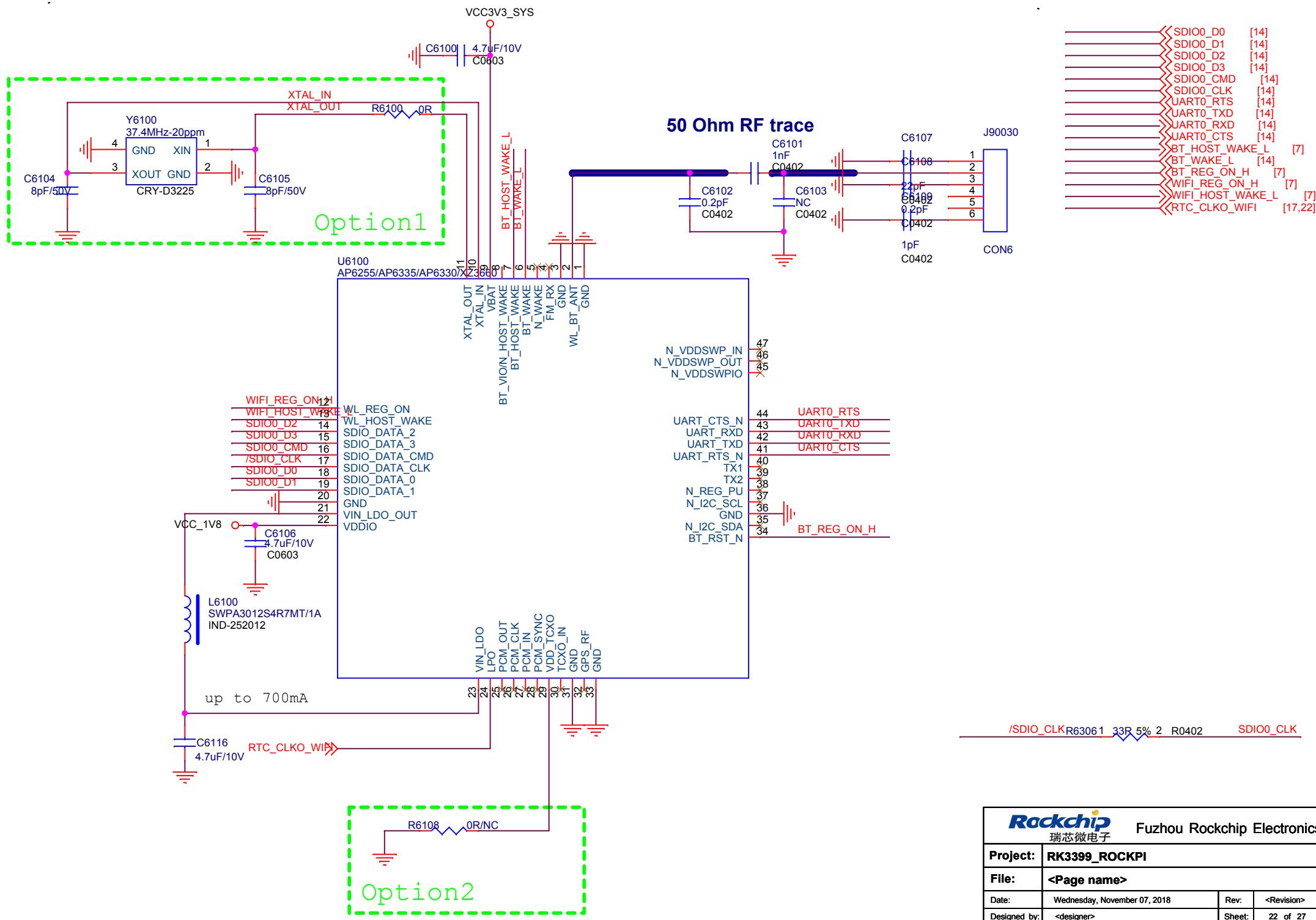


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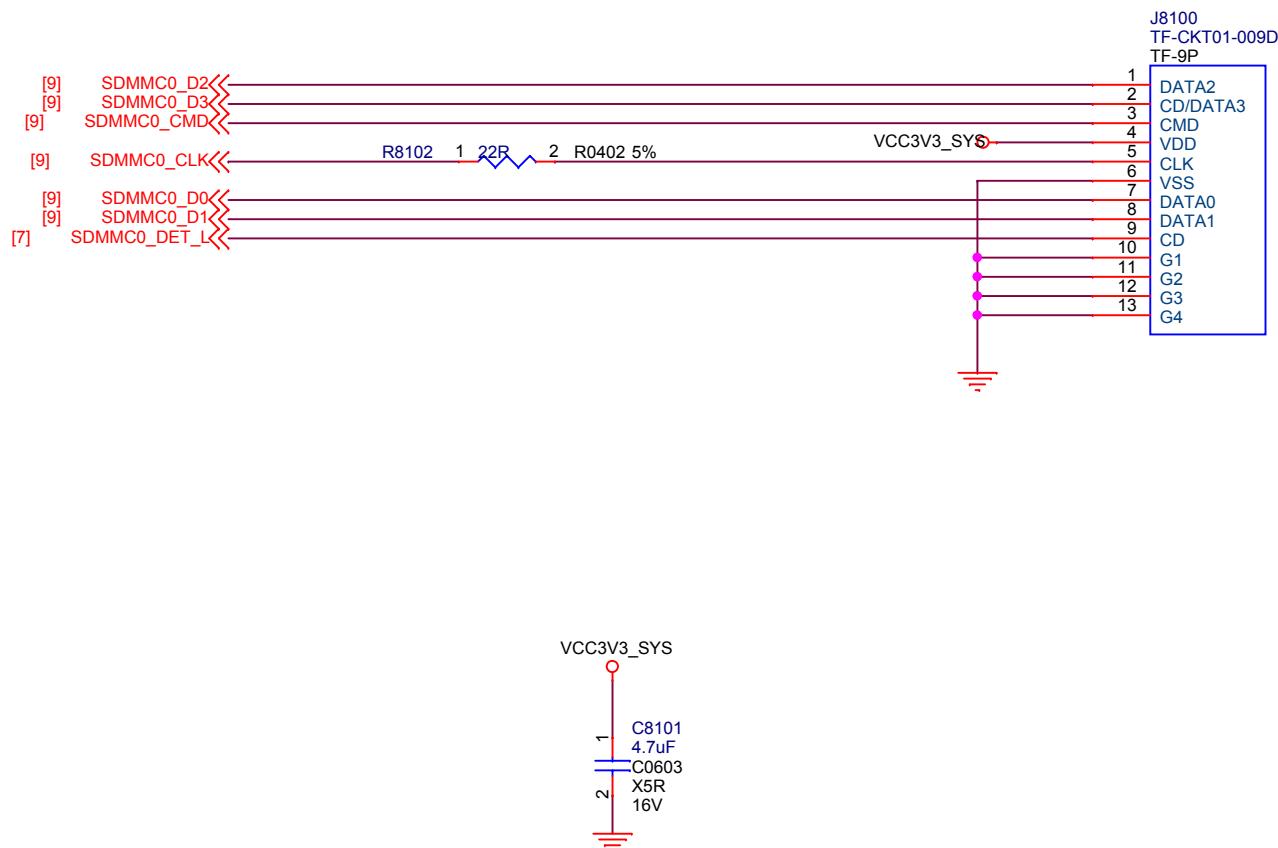
eMMC FLASH



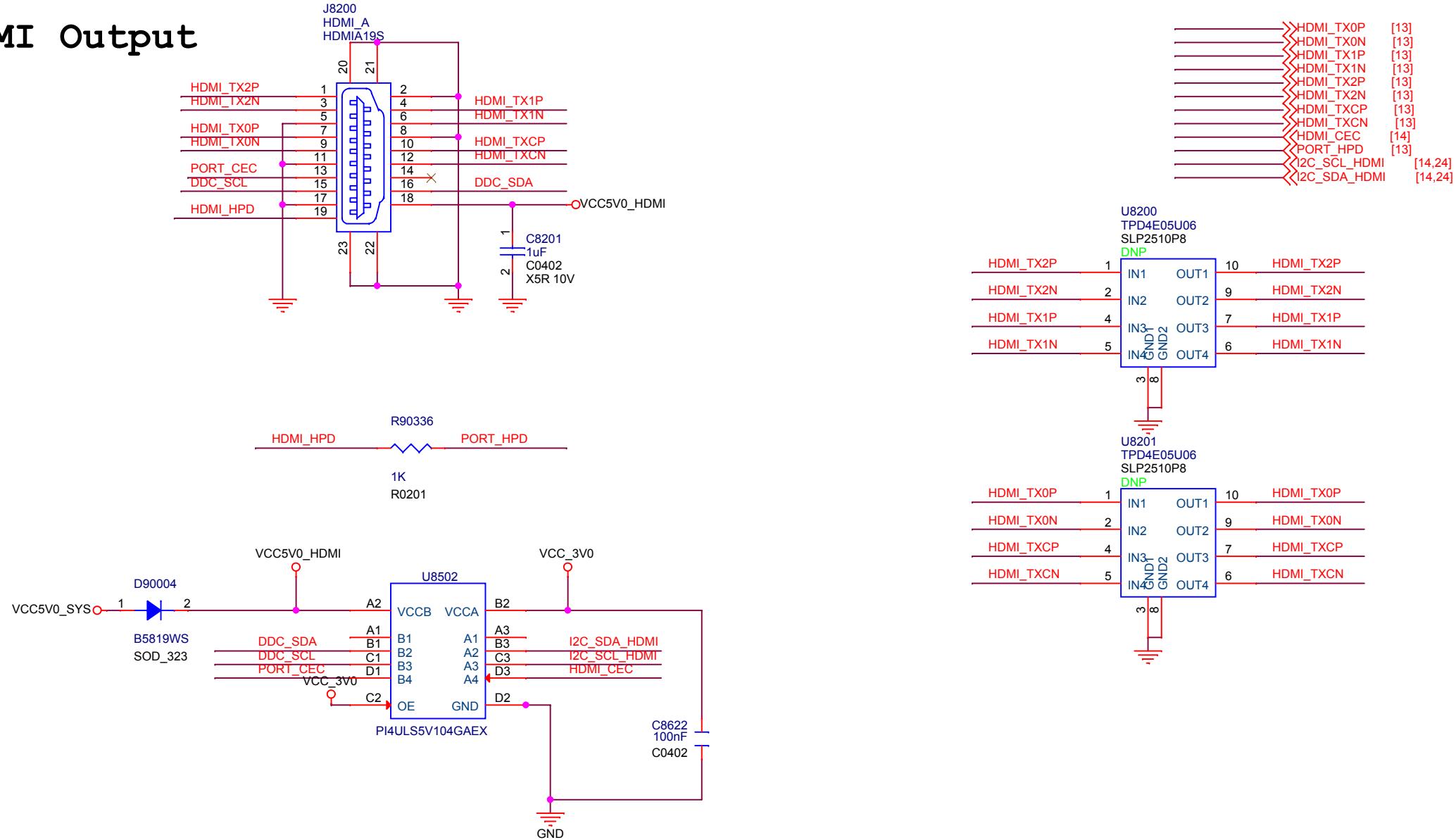


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TF CARD



HDMI Output



PCIe NGFF/M.2

