

ROCK_Pi_4_Model_B_V1.3

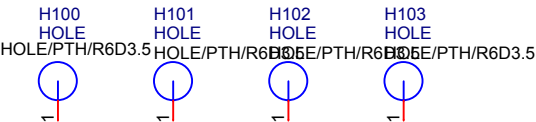
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6 LAYERS PCB STACK é g PCB=1.6mm

TOP	<div><div></div></div>	Silkscreen 0.25mm 1oz (35um)
	Prepreg 1080*1 (75um)	
GND1	<div><div></div></div>	Hoz (18um)
	Prepreg 2116*1 (115um)	
POWER	<div><div></div></div>	Hoz (18um)
	Adjust Core 0.65mm	
SIGNAL	<div><div></div></div>	Hoz (18um)
	Prepreg 2116*1 (115um)	
GND2	<div><div></div></div>	Hoz (18um)
	Prepreg 1080*1 (75um)	
BOTTOM	<div><div></div></div>	1oz (35um) Silkscreen 0.25mm

Note:
器件参数说明
1:如果 Value 为 **DR** 说明暂时不贴。
2:如果 Option 有 **DR** 说明预留先不贴。



5

4

3

2

1

Change List

Version	Date	Author	Change Note	Approved
V1.3	20180901	Charlie	V1.3 release.	

D

D

C

C

B

B

A

A

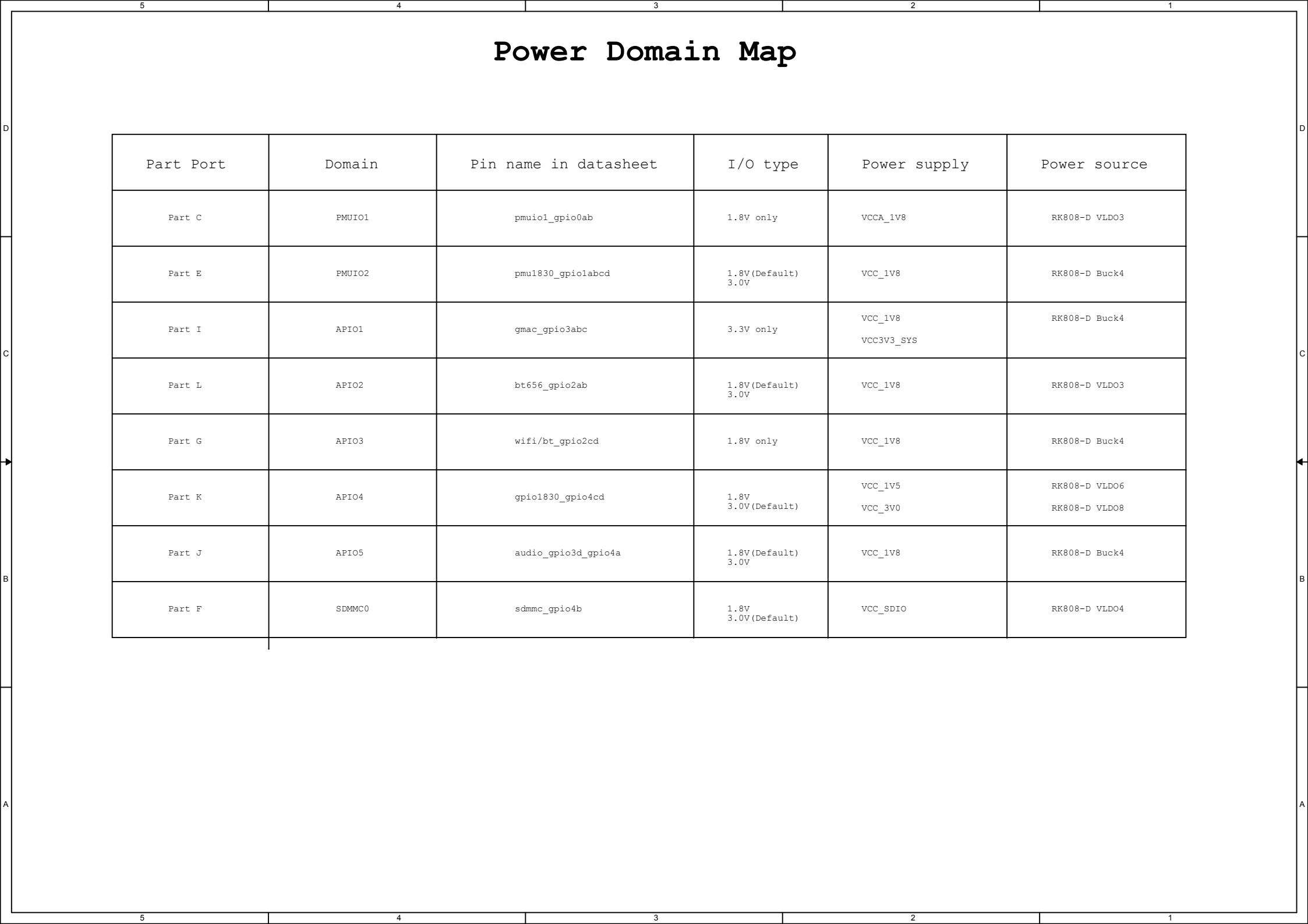
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4

3

2

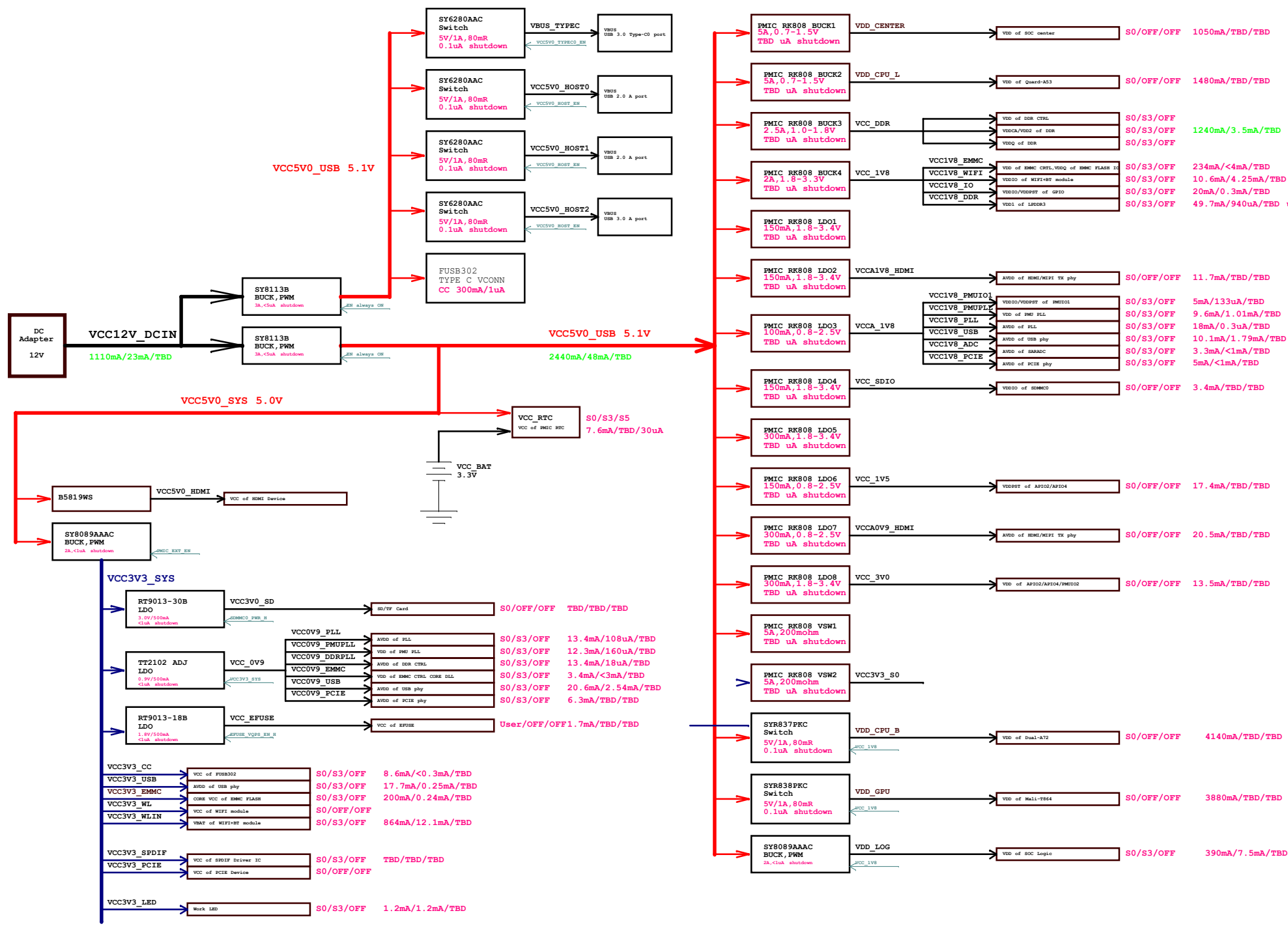
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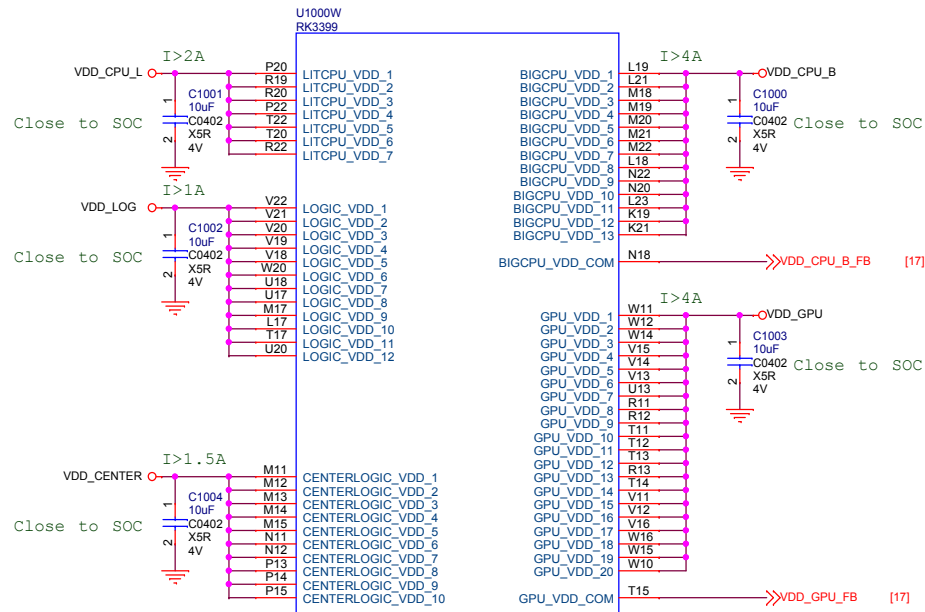


I2C MAP

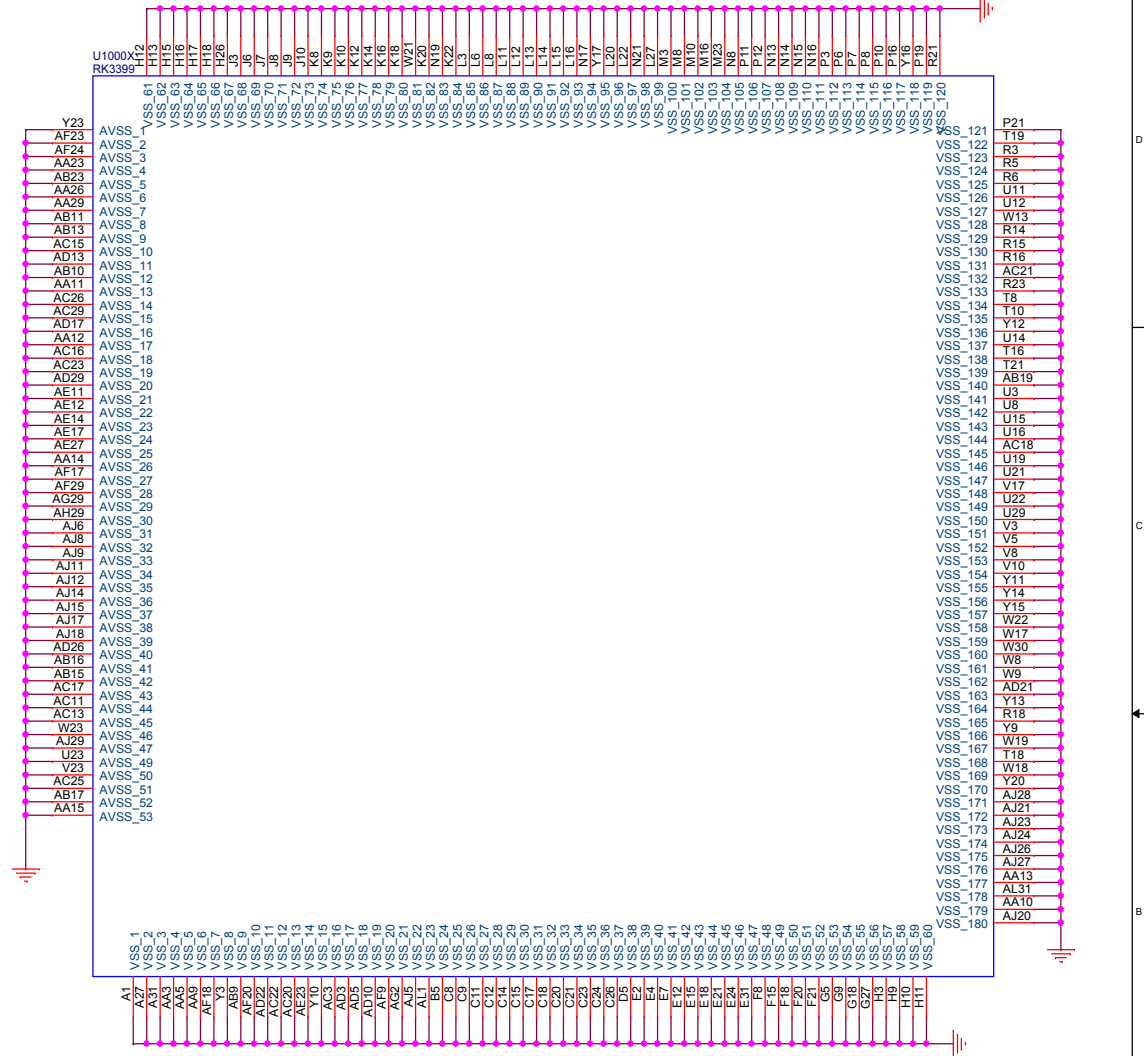
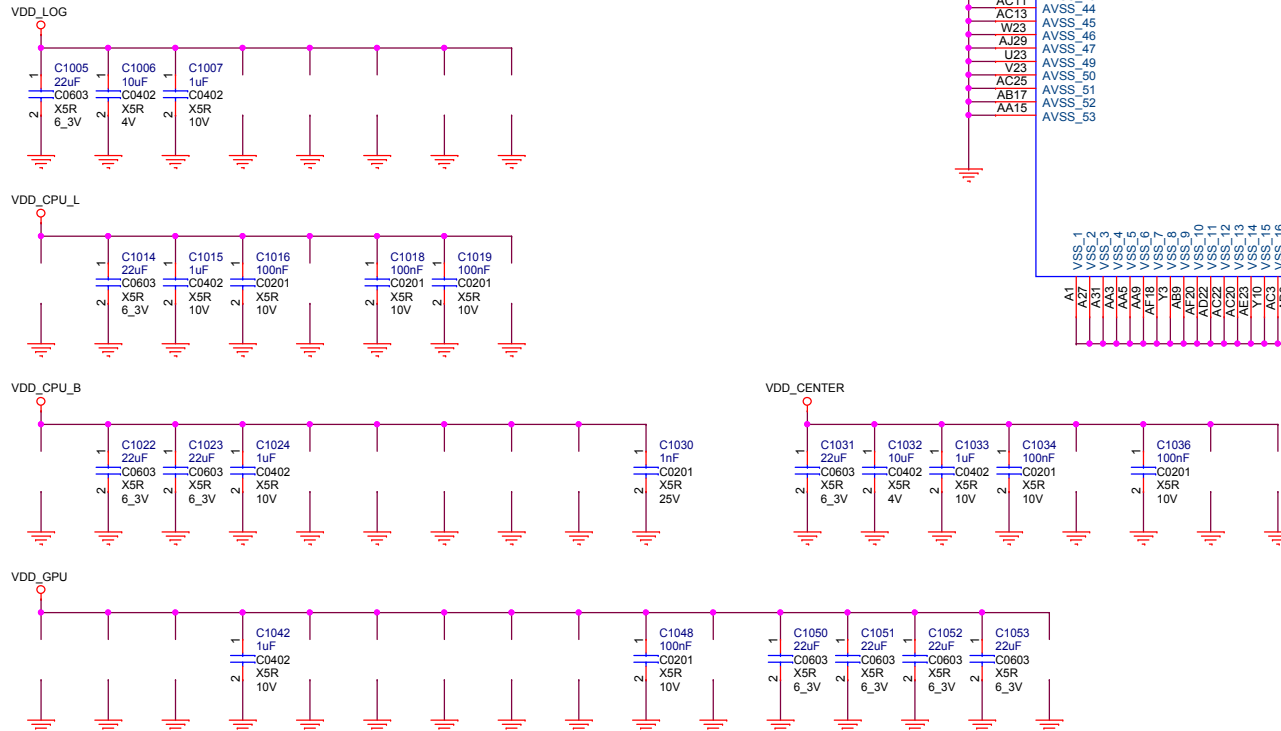
Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_1V8	Rockchip RK808	0x1b	PMIC	100kHz,400KHz
					SYR837PKC	0x40	DC-DC BUCK	100kHz,400KHz,3.4MHz
					SYR838PKC	0x41	DC-DC BUCK	100kHz,400KHz,3.4MHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5		VCC_1V8			Low Speed CONNECTOR	
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2		VCC_1V8			High Speed CONNECTOR	
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C_SDA_HDMI I2C_SCL_HDMI	VCC_3V0				
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C_SDA_MEMS I2C_SCL_MEMS	VCC_1V8	Fairchild FUSB302B	0x44,0x46	USB-TypeC Mux	100kHz,400KHz,1MHz
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	Other pin function					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2		VCC_1V8			Low Speed CONNECTOR	
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2		VCC_1V8			High Speed CONNECTOR	

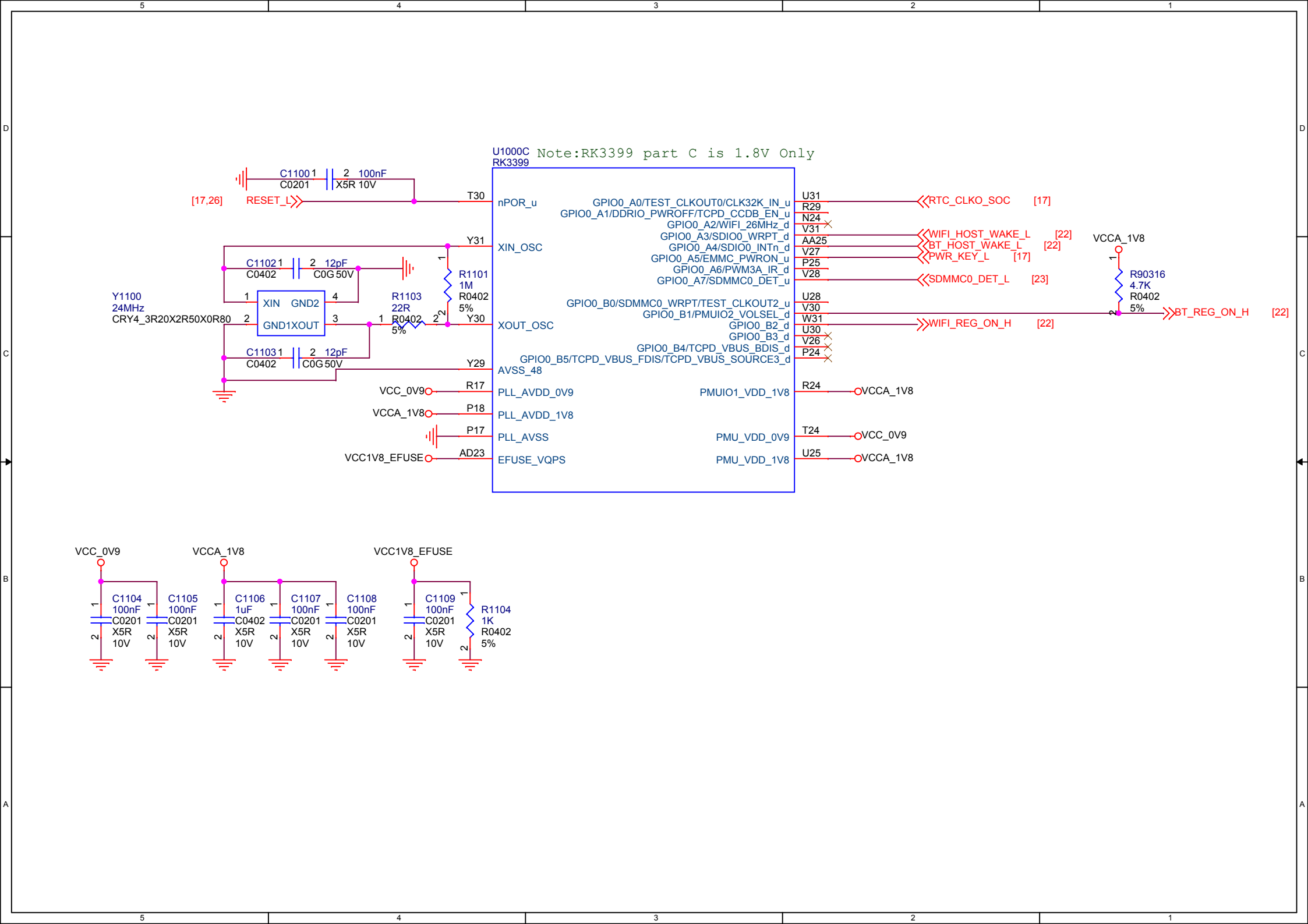
RK3399 POWER DIAGRAM

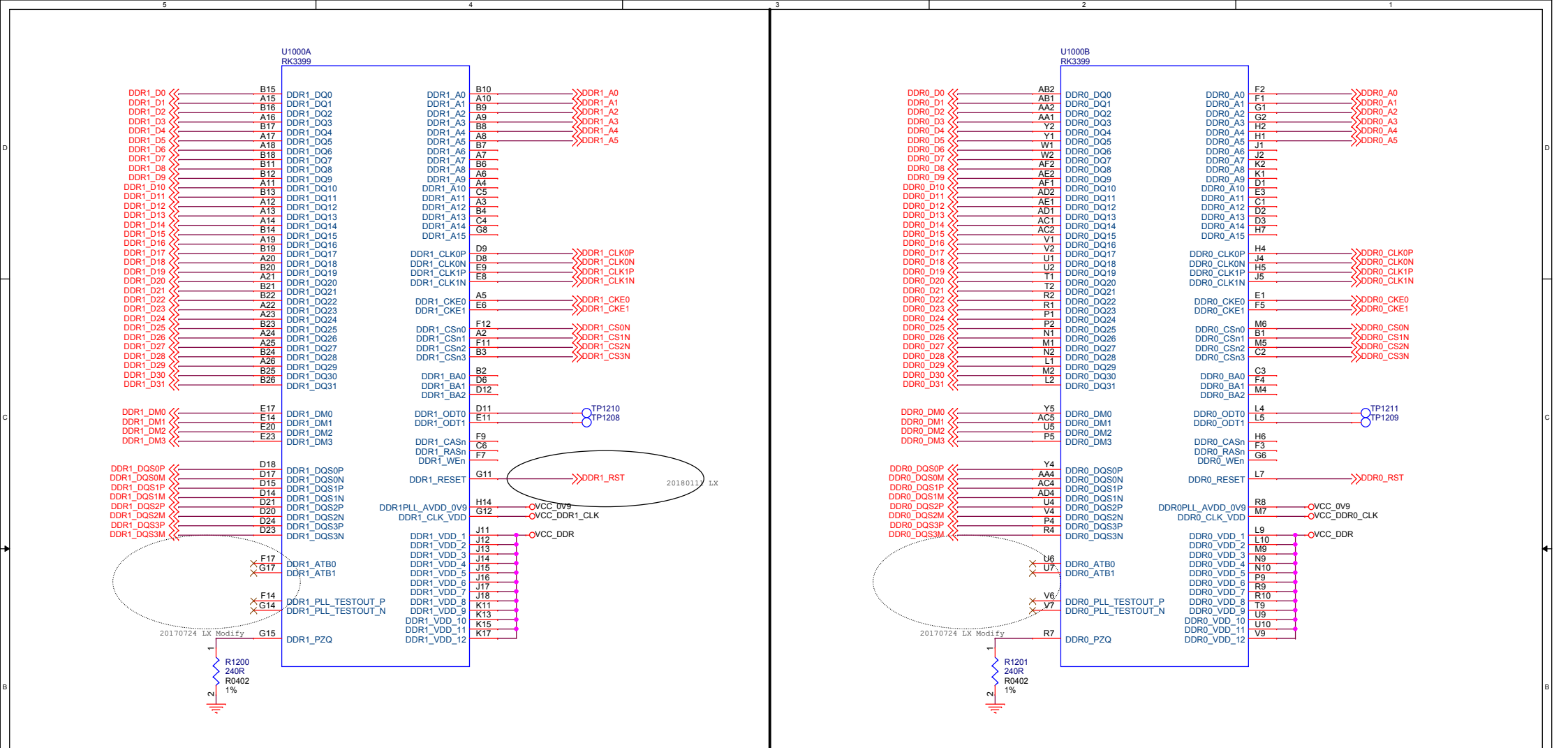




Note: Power filter CAP please place back of SOC or close to SOC

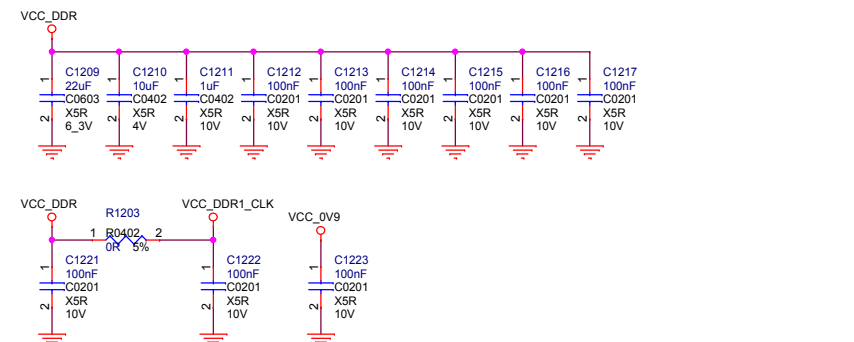
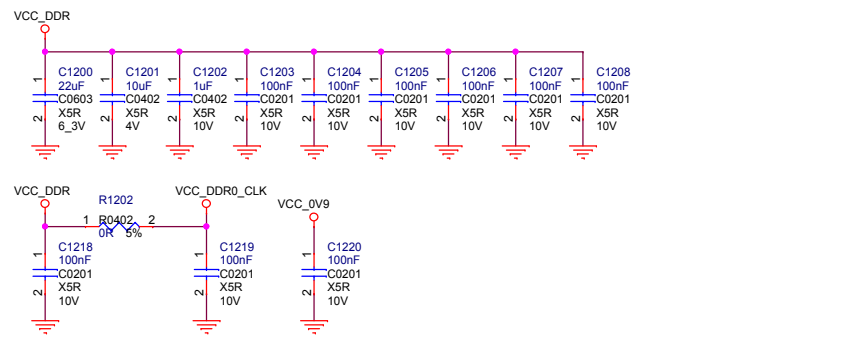




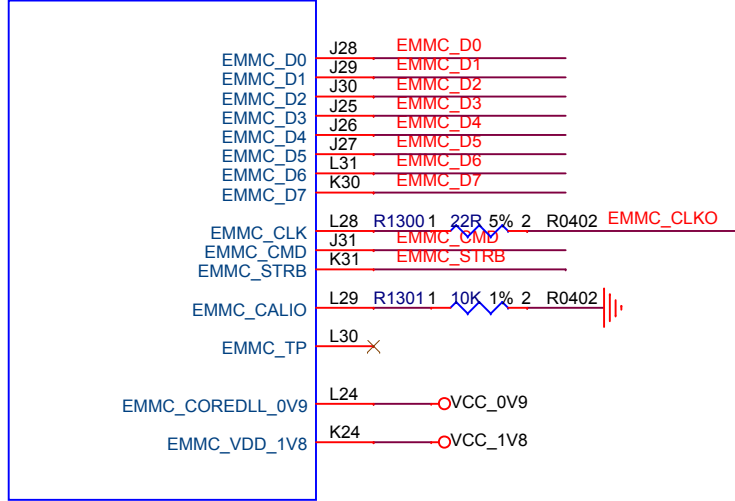


DDR FILTER Note:R1202 cannot be deleted

DDR FILTER Note:R1203 cannot be deleted

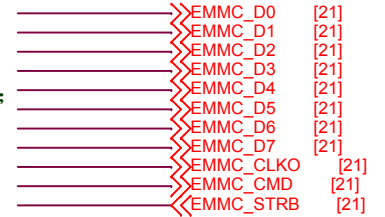


U1000H
RK3399

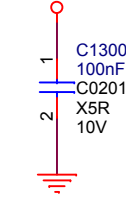


EMMC design rule:

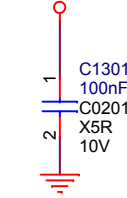
1. Data[0:7]、cmd strobe 线做为一组并行走线并包地，组内等长要求为 ± 100 mil；
2. Clk 需要单独走线并包地处理，与 data 间的延时小于 2ps；
3. Max trace length < 3.93 inches；
4. Trace impedance 50ohm $\pm 10\%$ ；
5. 与其他信号间距遵循 3 原则；
6. R1300 靠 SOC 放置；



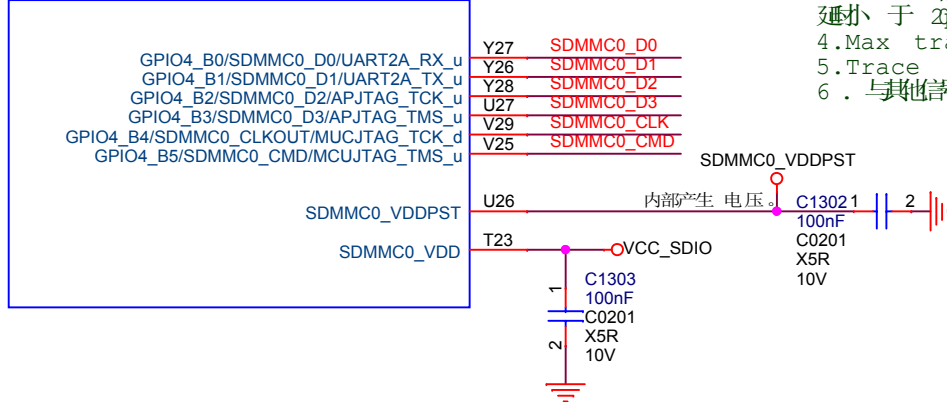
VCC_0V9



VCC_1V8



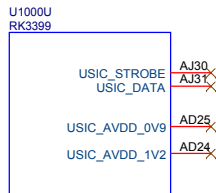
U1000F
RK3399



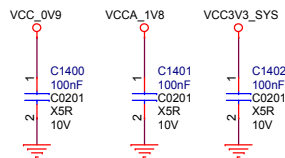
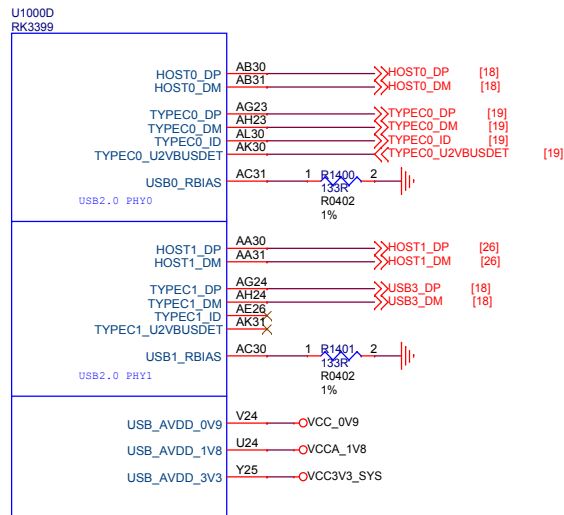
SDMMC design rule:

1. Data[0:3]、cmd 线做为一组，并行走线并包地，组内等长要求为 ± 100 mil；
2. Clk 需要单独走线并包地处理，与 data 间的延时小于 2ps；
3. Max trace length < 3.93 inches；
4. Trace impedance 50ohm $\pm 10\%$ ；
5. 与其他信号间距遵循 3 原则；





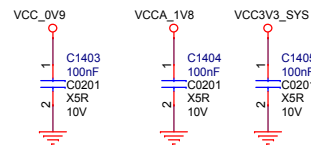
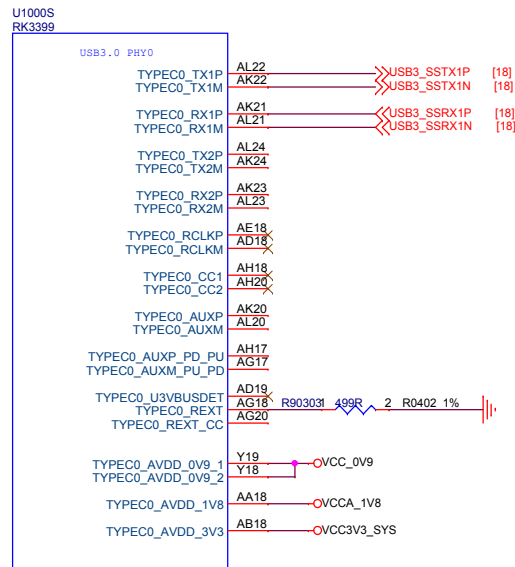
USB2.0



USB2.0 design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max trace length < 6 inchs;
- 3.Max allowed via < 6;
- 4.Trace impedance 90ohm+/-10%;
5. 与其他信号间距遵循 3原则;

USB3.0



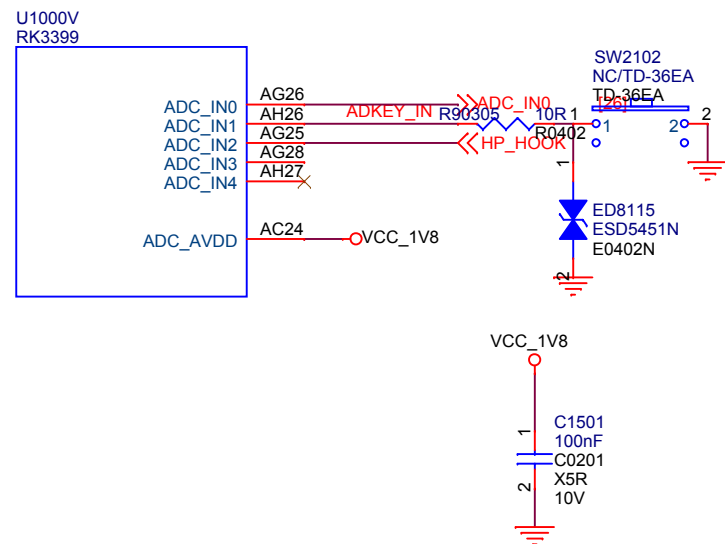
USB3.0 design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between TX and RX < 1.6 ns;
- 3.Max trace length < 6 inchs;
- 4.Max allowed via < 4;
- 5.Trace impedance 90ohm+/-10%;
6. 与其他信号间距遵循 3原则;



DP design rule:

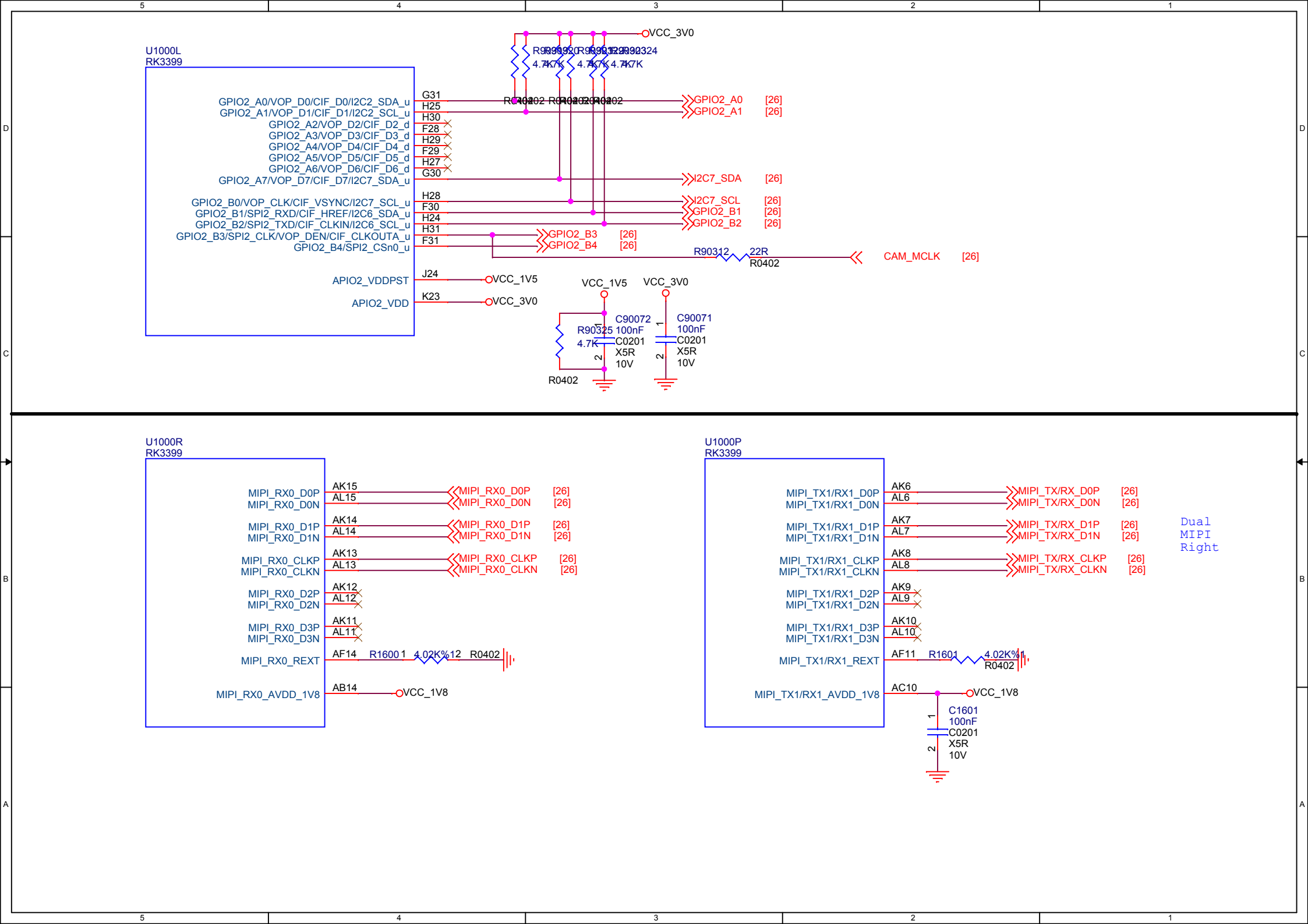
- 1.Max intra-pair skew < 4 ps;
- 2.Max trace length < 6 inchs;
- 3.Max allowed via < 4;
- 4.Trace impedance 90ohm+/-10%;
5. 与其他信号间距遵循 3原则;



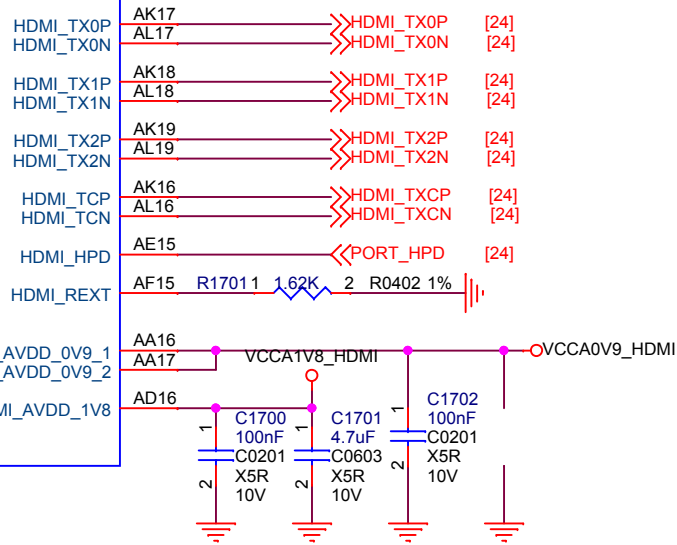
KEY BAORD

Note:
系统上电时，如果AEYIN电平为0V，
则RK3399进入Recovery模式；
上电量时R1503, SW1500, ED1500可以不
用贴片。





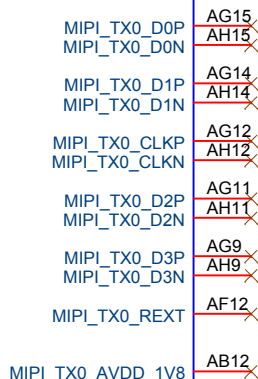
U1000N
RK3399



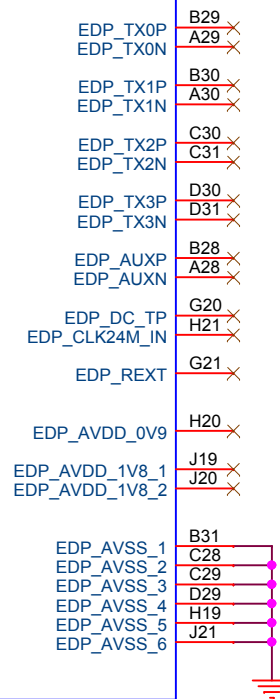
HDMI design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between clk and data < 80 ps;
- 3.Max trace length < 9.8 inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
6. 与其他信号间距遵循 3W 原则；

U1000Q
RK3399



U1000M
RK3399



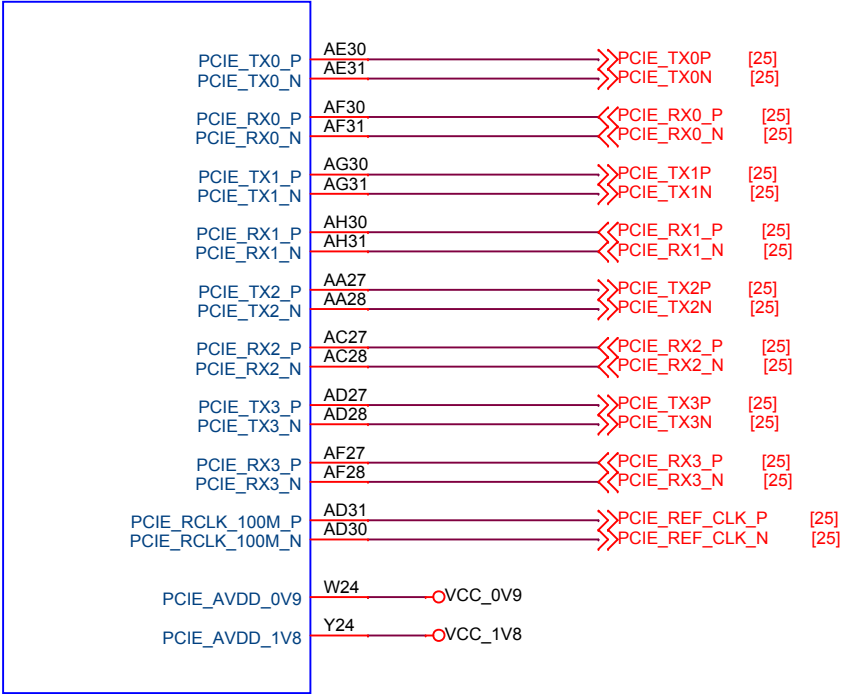
eDP design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max trace length < 6 inches;
- 3.Max allowed via < 4;
- 4.Trace impedance 90ohm+/-10%;
5. 与其他信号间距遵循 3W 原则；

MIPI design rule:

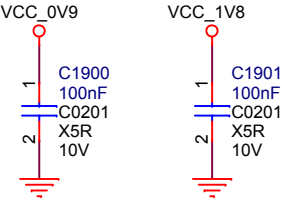
- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between clk and data < 7ps;
- 3.Max trace length < 7.2 inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
6. 与其他信号间距遵循 3W 原则；

U10000
RK3399

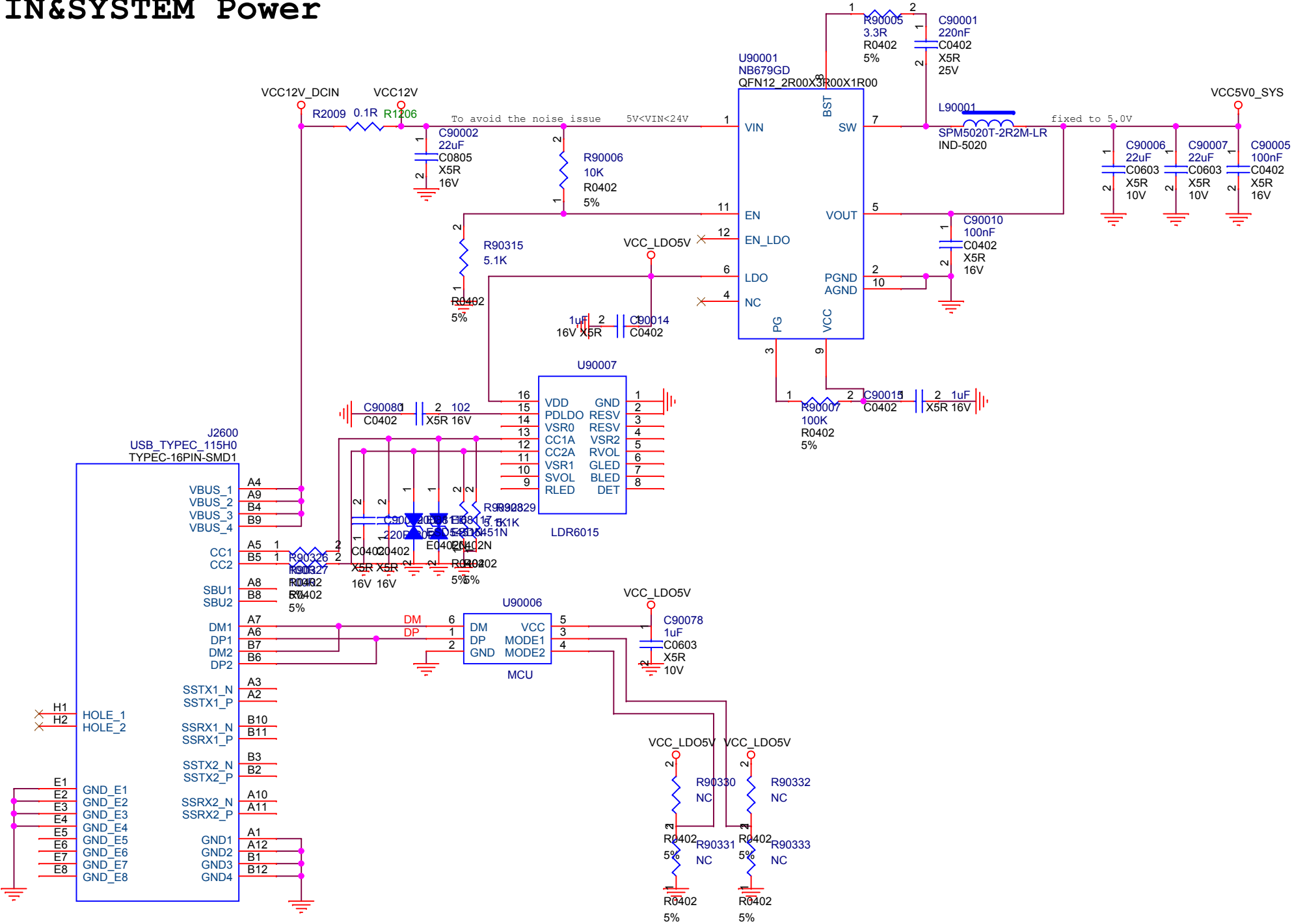


PCIE design rule:

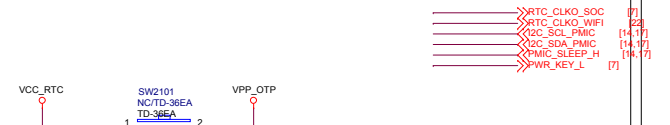
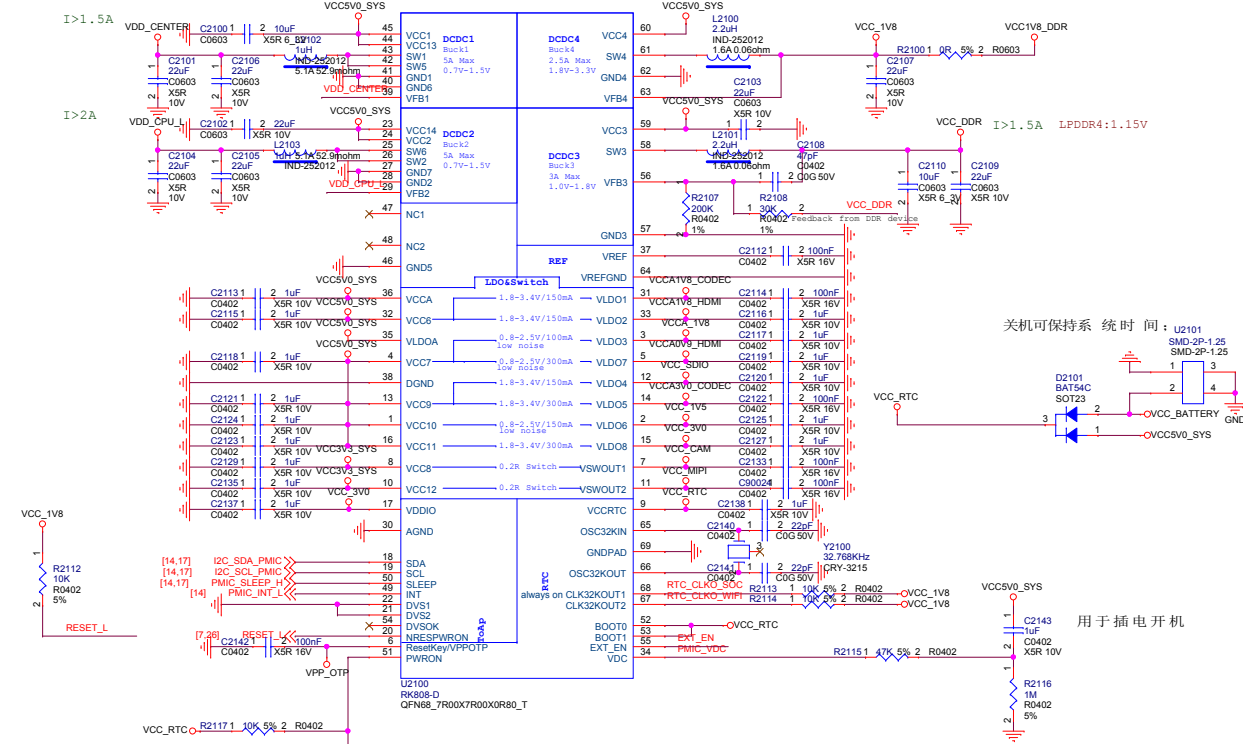
- 1.Max intra-pair skew < 4ps;
- 2.Max inter-pair skew < 1.6 ns;
- 3.Max trace length < 14 inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
6. 与其他信号间距遵循3原则;



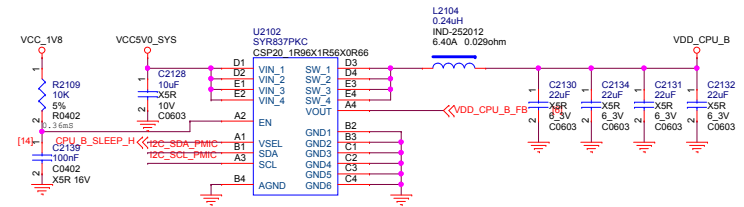
DC IN&SYSTEM Power



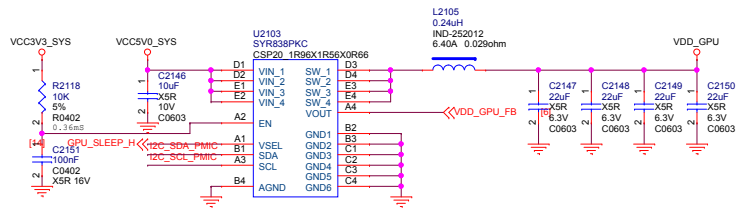
PMIC



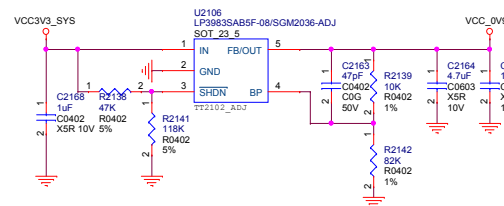
VDD_CPU_B power



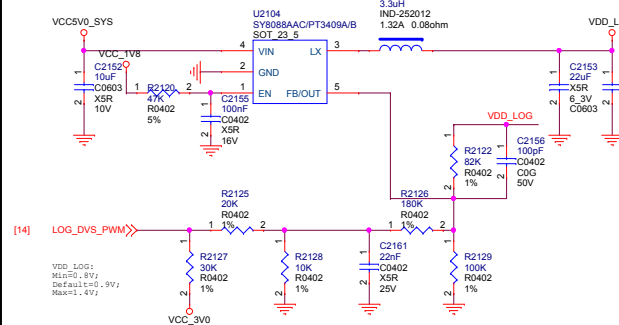
VDD_GPU power



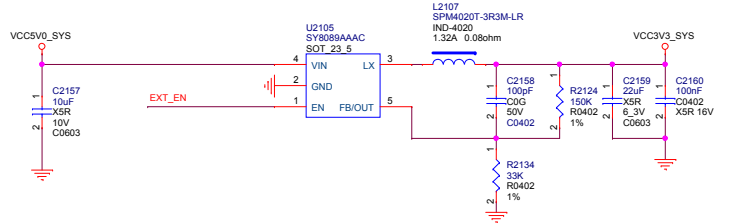
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VCC_0V9 power
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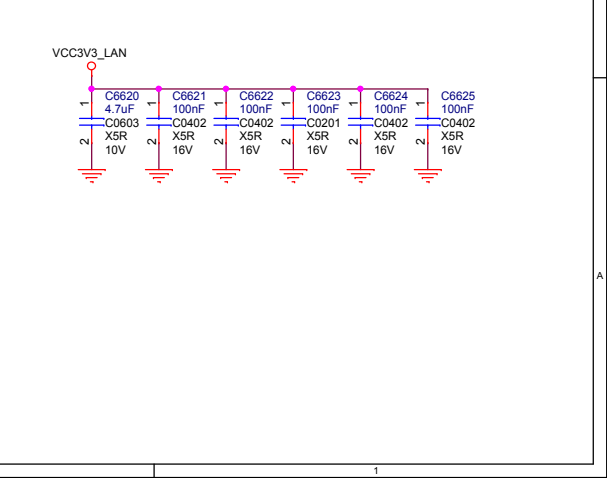
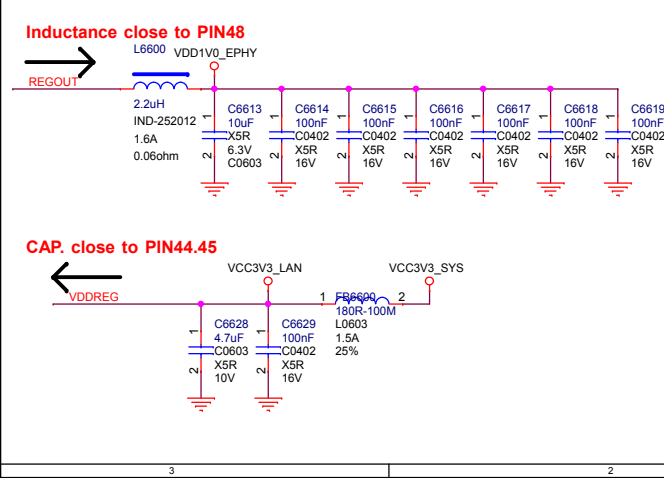
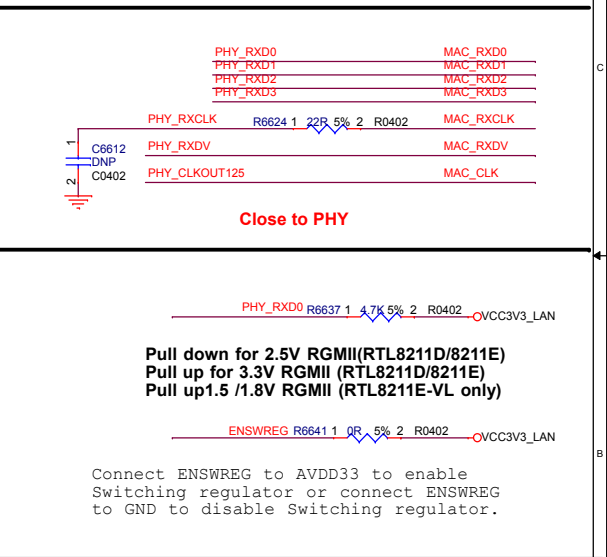
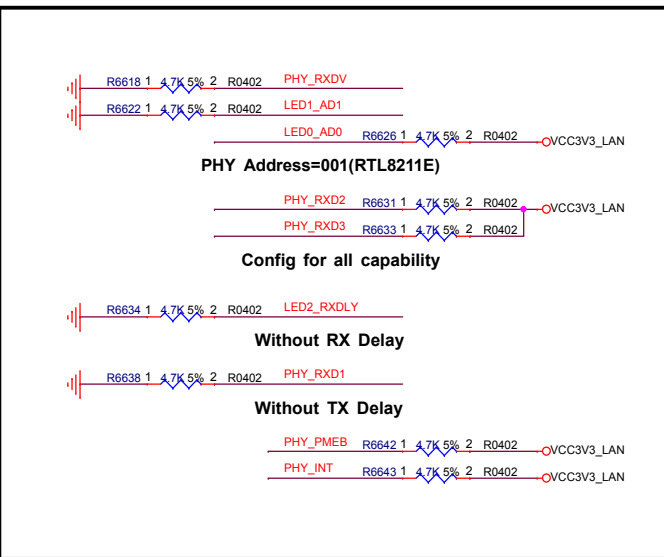
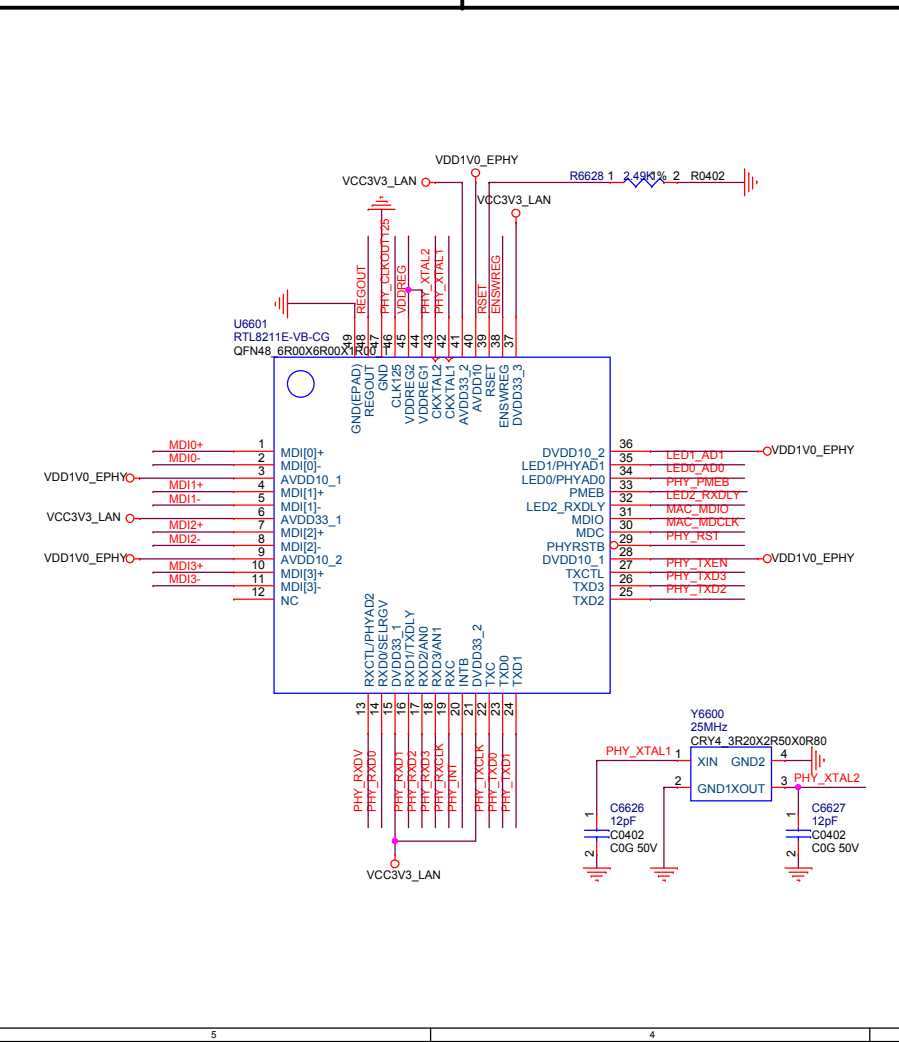
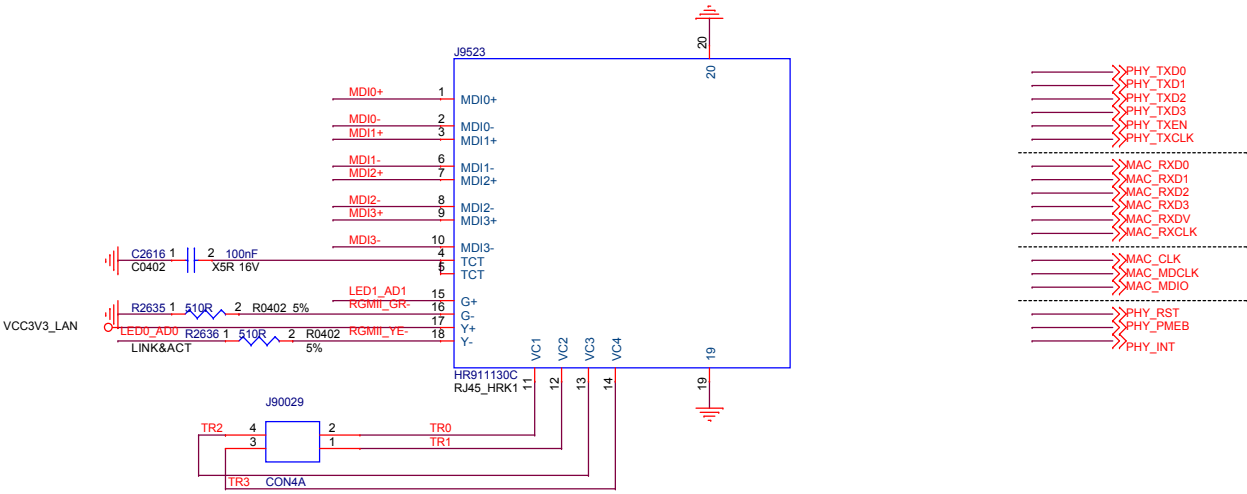
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VDD_LOG power
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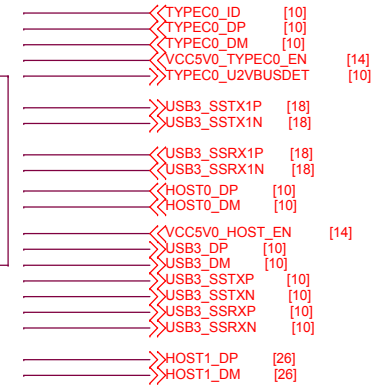
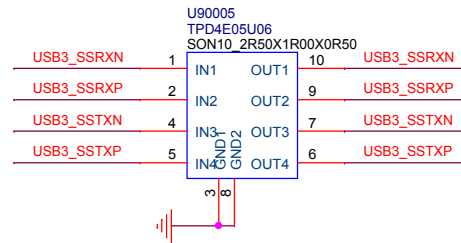
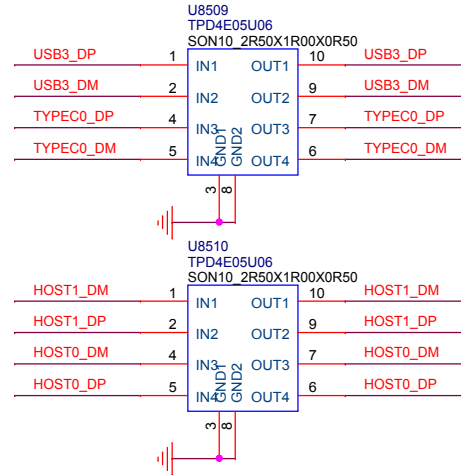
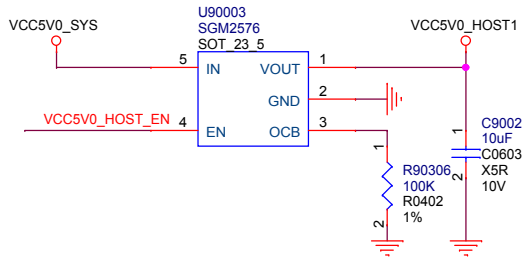
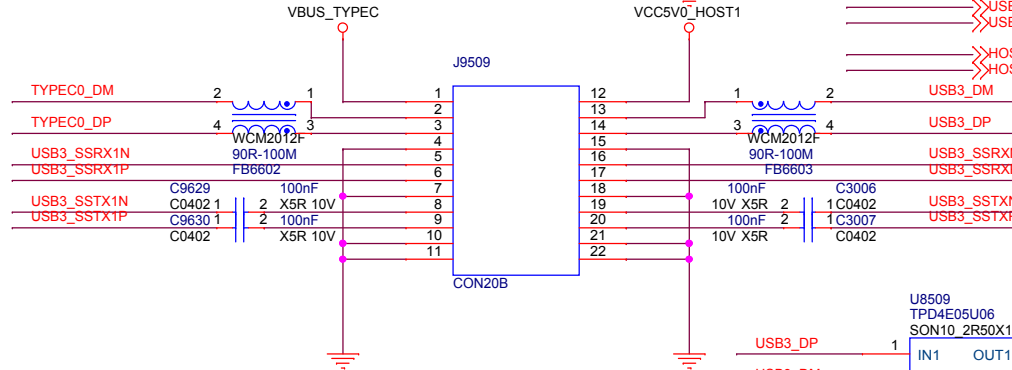
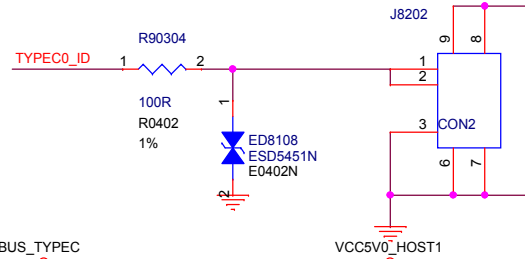
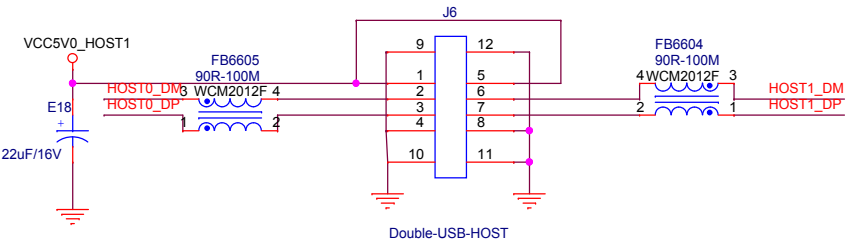
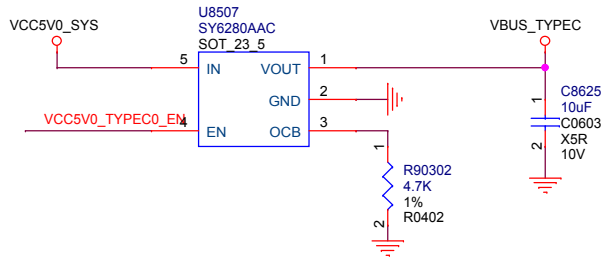
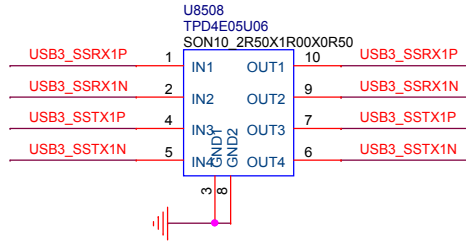
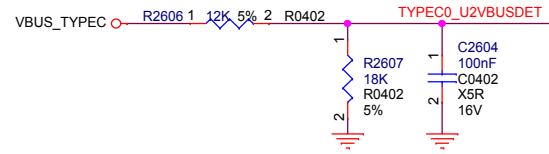
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VCC3V3_SYS power
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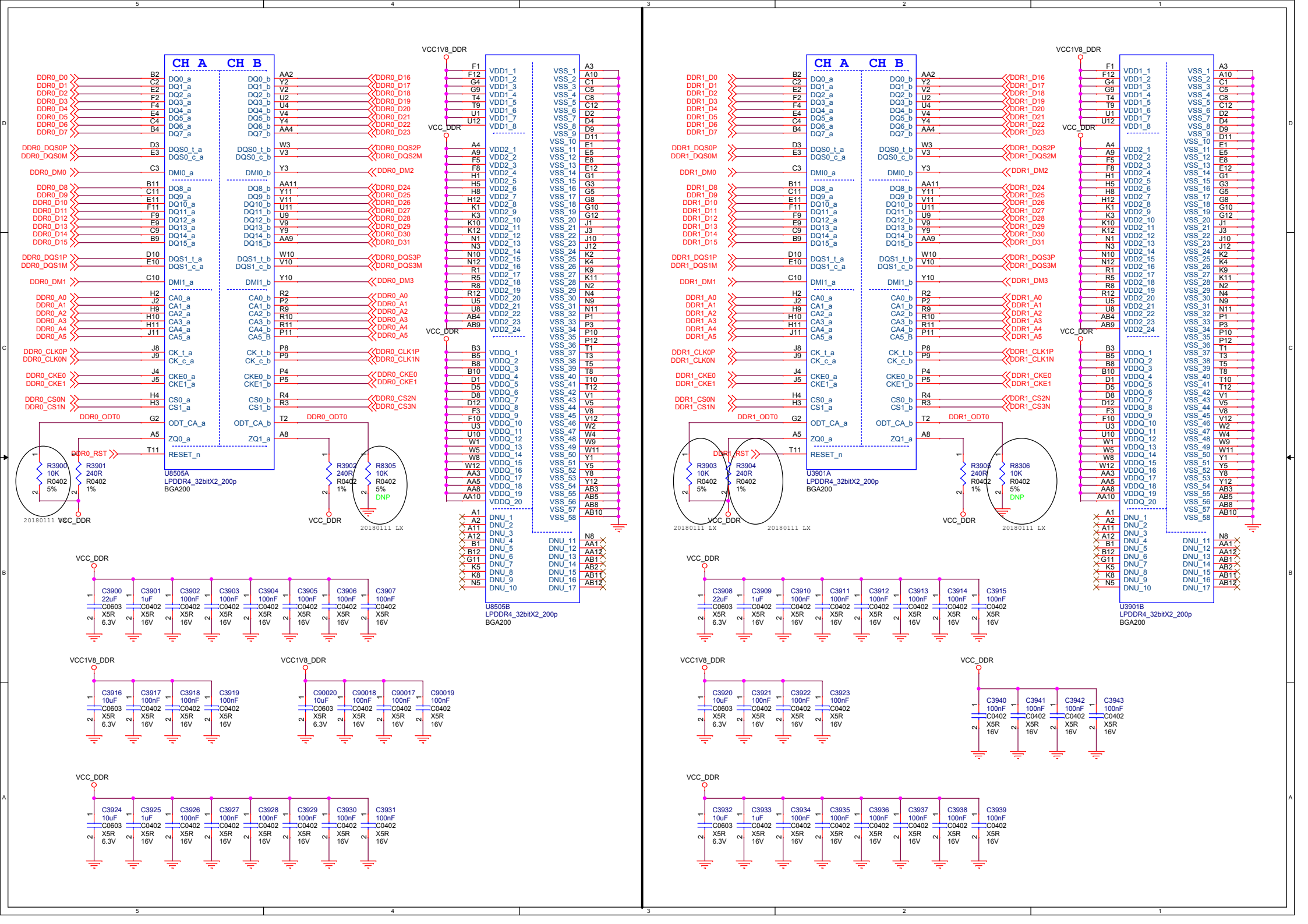


GMAC 10/100/1000 RGMII Ethernet PHY

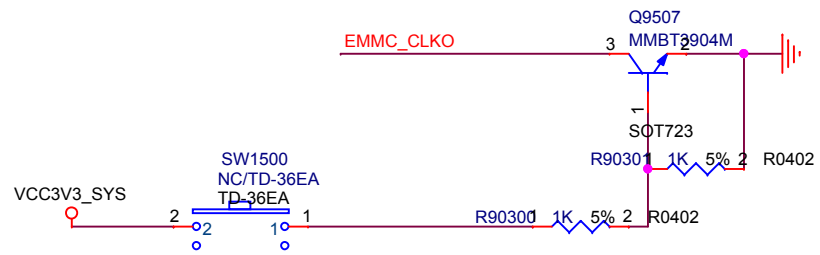
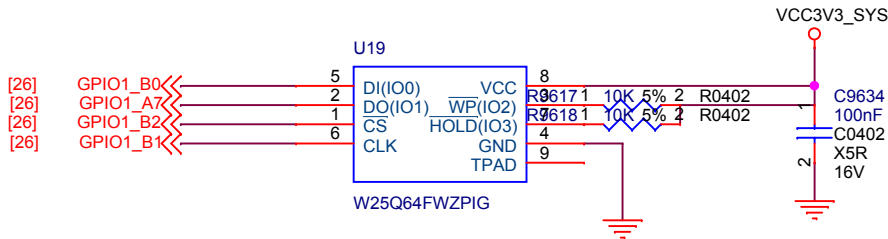
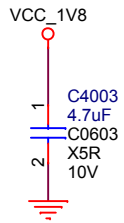
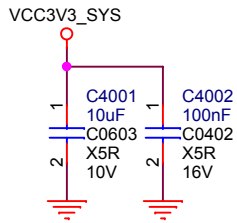
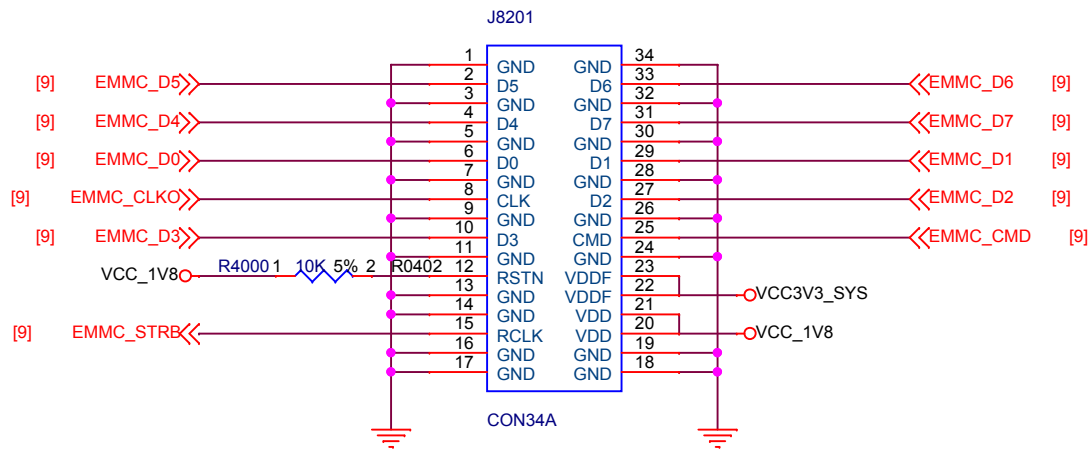


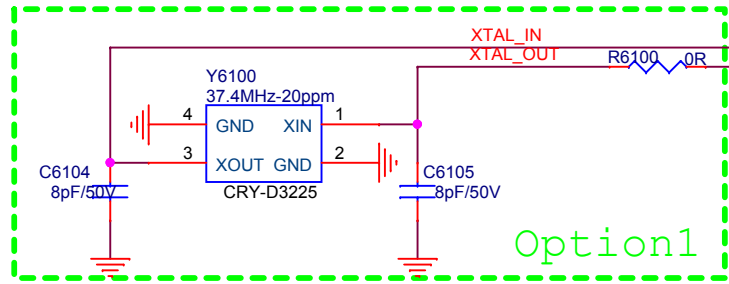
USB3.0 OTG port



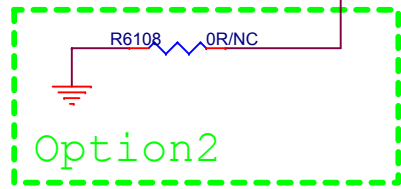
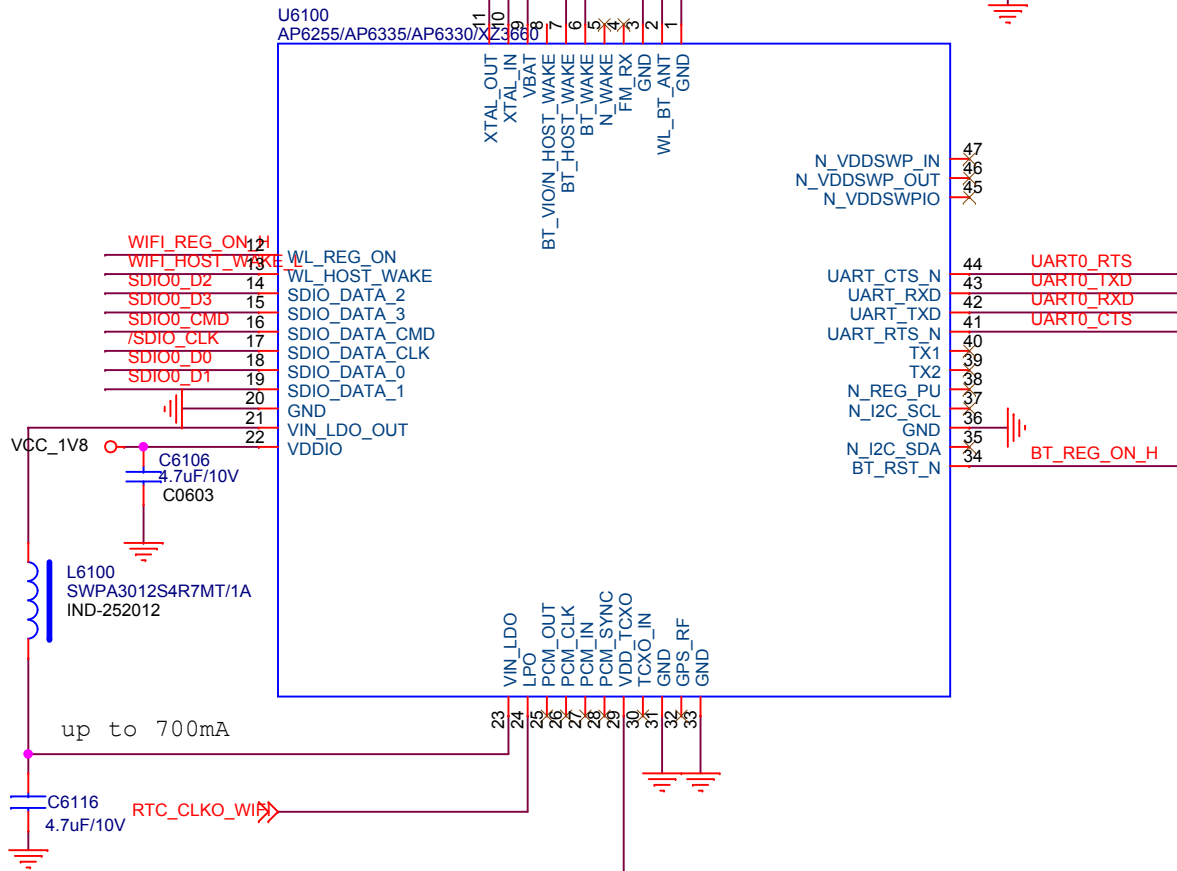
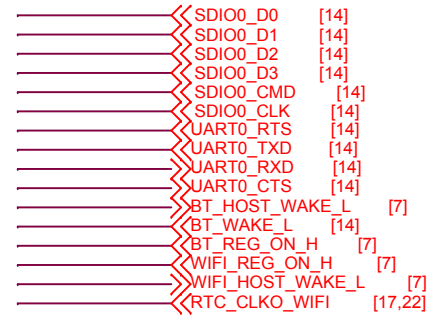
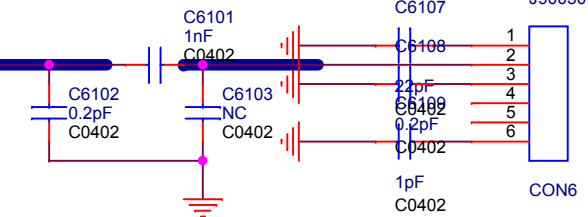


eMMC FLASH

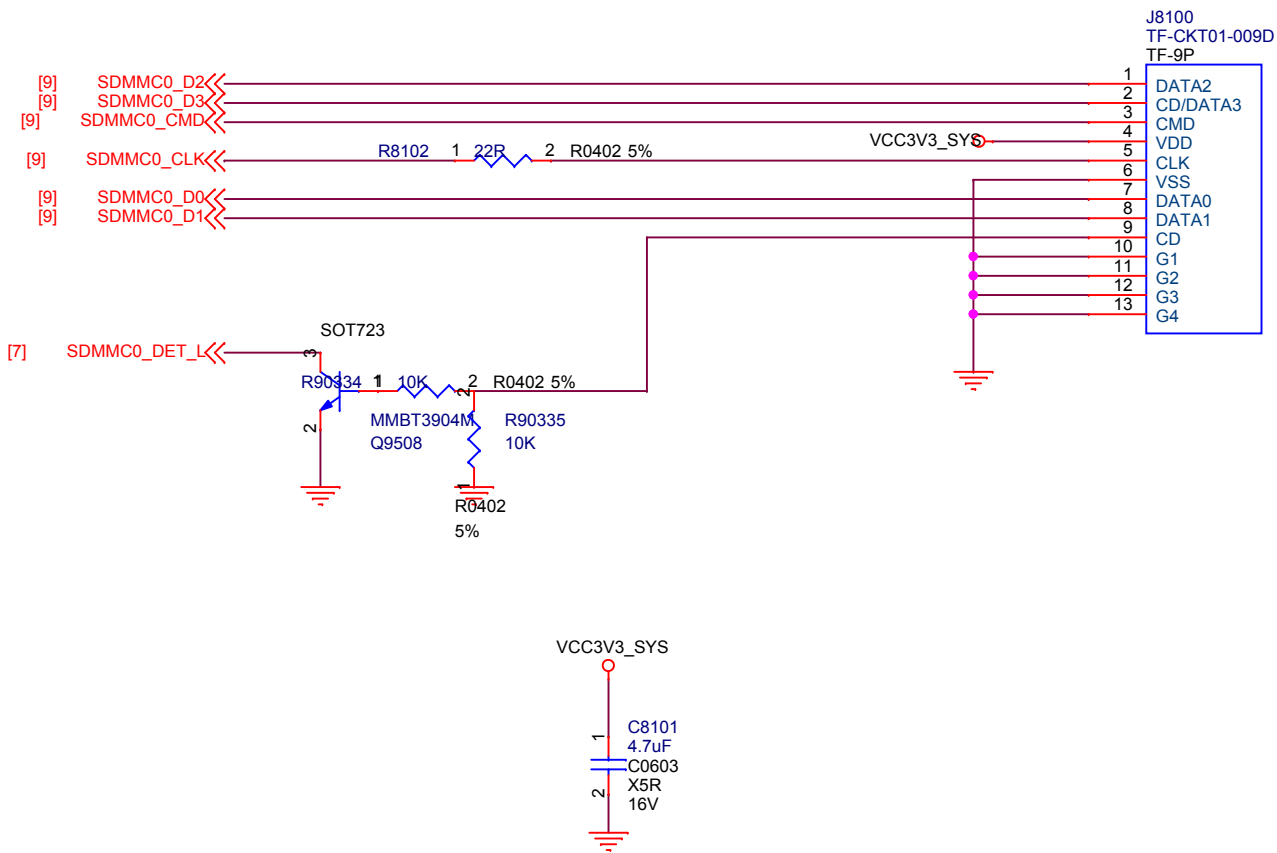




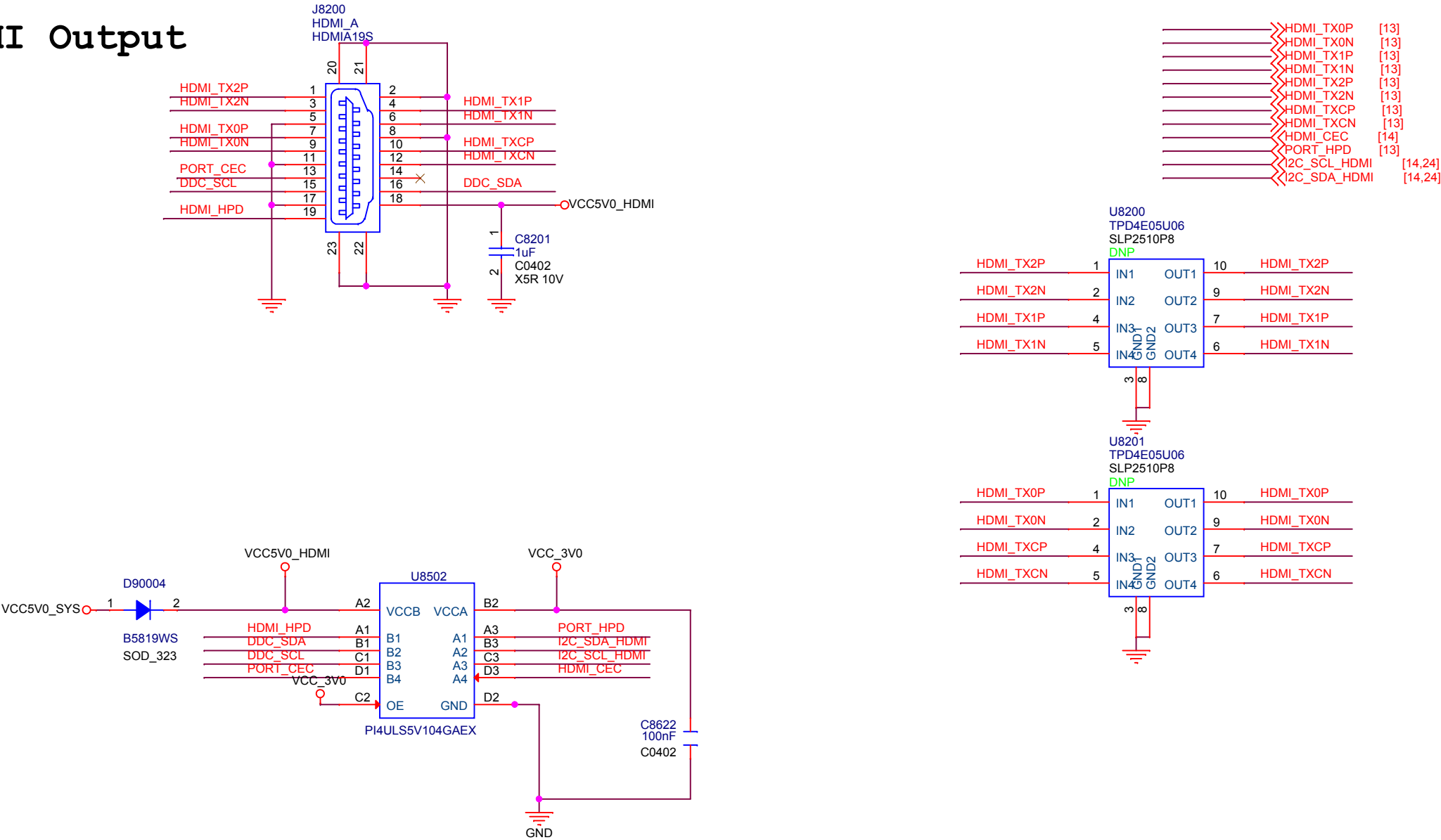
50 Ohm RF trace



TF CARD



HDMI Output



PCIe NGFF/M.2

