Front-end channels in a 28 nm CMOS process for Pixel detectors in future High Energy physics colliders and advanced X-ray imaging instrumentation

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Abstract

Next generation pixel detectors for high energy physics (HEP) experiments and imaging at advanced X-ray sources call for ultra-low noise, high data rate readout chips to be operated in extremely harsh radiation environments.
This project aims at improving the state-of-the-art of pixel readout chip technology at high luminosity colliders and X-ray imagers at the next generation free electron lasers (FELs) by developing, in a 28 nm CMOS technology, the fundamental microelectronic building blocks for the pixel readout chips. Such blocks, implementing innovative circuit ideas, will enable the integration of a readout chip meeting a set of challenging requirements, such as high spatial resolution, high signal-to-noise ratio, very wide dynamic range and the capability to withstand unprecedented radiation levels.
Two different front-end architectures, one optimized for HEP applications and the other for X-ray imaging applications at FELs will be developed. As a final demonstrator, the project will produce a prototype ASIC (Application Specific Integrated Circuit) including two matrices of 16×16 front-end channels conceived for HEP and FEL applications.

1 Introduction

Hybrid pixel detectors have been technology drivers in High Energy Physics (HEP), having to integrate complex electronics in a small space, coping with high data rates per unit area and a very granular sensor. In particular, Large Hadron Collider (LHC) experiments strongly rely on pixel detectors for resolving the track elements in the volume around the interaction point. High luminosity upgrades of LHC and future HEP colliders are pushing further the requests on the pixel readout chips.

Also, hybrid pixels with improved performance in terms of readout rate, dynamic range and radiation tolerance are in high demand in X-ray Free-Electron Lasers (FEL) applications, which are now driving the state-of-the-art of X-ray science. X-ray FELs can offer unprecedented capabilities in penetrating the microscopic structure of organic and inorganic systems, new materials and matter under extreme conditions, and in recording and understanding the time evolution of fast biochemical phenomena at the nanoscale.

2 State of the art

Hybrid pixel detectors, with sensors bonded to dedicated readout ASICs, are currently used for particle tracking in the main experiments at the LHC and for X-ray imaging in advanced applications at FELs.

The LHC [1] has generated astounding science in the last decade, including the discovery of the Higgs boson. The High-Luminosity LHC (HL-LHC) [2] is a major upgrade of the collider which plans to boost the instantaneous luminosity to $7 \times 10^{34} cm^{-2} s^{-1}$. While the HL-LHC remains the top near-term priority, a number of studies for post-LHC projects are being pursued. Such studies include an electron-positron Higgs factory (FCC-hh) [3] targeting 100 TeV. The state-of-the-art in pixel readout chip technology for HEP instrumentation is being developed by the CERN RD53 collaboration [4] for the so called Phase-2 upgrades of the ATLAS and CMS experiments at the HL-LHC. In RD53 chips [5], with which I have dealt during my master's thesis, the pixel readout circuits, designed in a 65 nm CMOS technology, are packed in $50 \times 50 \mu m^2$ cells. They withstand a Total Ionizing Dose (TID) larger than 500 Mrad, sustaining hit rates up to $3 GHz/cm^2$. Anyway, it is known that 65 nm CMOS chips cannot face the extremely large TIDs expected in the inner/intermediate layers of the FCC-hh tracker.

Hybrid pixel detectors have also been proposed to address the formidable challenges set by X-ray imaging at FELs, where the minimum wavelength, of the order of one Ångström, and the intensity of the laser beam make it possible to see objects with nanometer feature size. Three main hybrid pixel detectors have been developed for the European XFEL (EU-XFEL) [6]. Different solutions were proposed to face challenges such as the wide dynamic range (80dB) and the beam structure, with bursts of high repetition rate (4.5 MHz) X-rays, with about 100 ms intervals between two subsequent bursts. In the developed readout chips (130 nm CMOS), the images are stored in the pixels and read out during the long inter-train period. Future upgrades of the EU-XFEL, started in the second half of the 2020's, include continuous wave (CW) operation at a constant pulse rate close to 100 kHz [7]. At these rates, it becomes feasible to move or exchange solid samples during a burst, which significantly reduces sample radiation damage and thus opens EU-XFEL to new classes of experiments and materials. To fully exploit continuous operation mode with high repetition rates, detectors with improved readout rate and radiation tolerance are needed.

3 Objectives of the project

This project aims to advance the performance of radiation instrumentation for particle tracking in HEP experiments and for X-ray imaging at the next generation FELs. For this purpose, the work will develop, in a 28 nm CMOS technology, innovative circuit solutions for the design of mixed-signal front-end ASICs with improved performance in terms of spatial resolution, efficiency and radiation hardness for future high-rate pixel detectors.

The HEP community is now starting to invest in 28 nm processes. Such a technology brings along a considerable improvement in terms of radiation hardness [8] [9] [10] as well as speed and density of digital circuits, allowing designers to squeeze the size of pixel cells and to increase the speed of readout logic and of I/O circuits. A new 28 nm CMOS pixel readout chip is being devised for a further partial upgrade, in the so-called Phase-3, of the inner tracker of CMS and ATLAS. It has to be noticed that the replacement of the innermost layer of the pixel system of the HL-LHC experiments after 2030 is currently under consideration as it can be relatively limited in cost and with a substantial boost of the physics reach of the experiments. A new layer with smaller pixel cells providing improved pile-up mitigation and vertex reconstruction capabilities will naturally benefit from a front-end circuit fitting an area smaller then the RD53 ones.

4 Description of the project: methodologies, intermediate phases, tools to be used

A main objective of the project is to build-up experience in the use of the 28nm CMOS node for pixel detector readout chip technology and disseminate know-how and guidelines to the designers in the HEP and FEL communities. This is why it is appropriate to provide an initial phase in which the foundamental electronic blocks are designed by deepening in the literature alternative building methods. After that it will be important to design two front-end architecture optimized for HEP and FEL applications, submit the prototype chips and prepare the test instrumentation, including the Data Aquisition System and the test-hardware. Also, the submitted structures will becharacterized in terms of radiation hardness in the Grad regime. The collaboration between Padova and Bergamo Universities will make it possible to run a radiation test campaign.

It has to be noticed that the radiation hardness of single transistors has been assessed in a test campaign with TIDs up to 1 Grad [8] [9] [10], and results show that the 28 nm node can operate with limited performance losses up to several hundreds of Mrad, with a proper transistor geometry choice. However, its actual level of radiation hardness has still to be demonstrated for small/medium size chips, together with the performance of analog circuits in pixel cells smaller than the RD53 ones. Testing after irradiation of the demonstrator is thus expected to provide extremely important insights for the design of rad-hard, low-noise readout ASICs for pixel detectors. The activities carried out for the development of the final demonstrator are expected to be synergetic and complementary with respect to the ones going on in the framework of the INFN Falaphel project, where I am currently working as fellow researcher, focused on the system-in-package integration of Silicon Photonics optical devices and high-speed electronics for high rate data transmission in high energy physics experiments.

As a final demonstrator, the project will produce a prototype ASIC including two matrices of 16×16 front-end channels conceived for HEP and FEL applications.

A possible work schedule could be summarized as follows:

First Year: Study of advanced design techniques in literature, definition of the specifications for the analog front-end channels and the metrics for testing. Design of the foundamental analog building blocks.

- Investigating design architecture and techniques. (4 months)
- Specifications of a Front-End and metric for testing. (2 months)
- Design of foundamental analog building blocks. (6 months)

Second Year: Design of single front-end channels for HEP and FEL applications and integration in the first prototype.

- Design of the HEP and FEL front-ends and integration of test structures in a prototype chip. (6 months)
- Design of the test setup. (3 months)
- Characterisation of the prototype (3 months)

Third Year: Development, test, characterisation and application of the final demonstrator.

- Design and production of the final chip integrating two 16×16 matrices of HEP and FEL front-ends. (6 months).
- Design of test setup. (3 months)
- Testing and characterisation (3 months)

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