REVISION	DESCRIPTION	DATE	APPROVED

DC_VDD

ASIC_SDI_P / ASIC_SDI_N → U_adatpterLVDS_1 adatpterLVDS.SchDoc → dc_ASIC_SDI_P / dc_ASIC_SDI_N

DC_VDD

ASIC_SCLK_P / ASIC_SCLK_N → U_adatpterLVDS_2 adatpterLVDS.SchDoc → dc_ASIC_SCLK_P / dc_ASIC_SCLK_N

DC_VDD

ASIC_SS_P / ASIC_SS_N → U_adatpterLVDS_3 adatpterLVDS.SchDoc → dc_ASIC_SS_P / dc_ASIC_SS_N

DC_VDD

RESETN_P / RESETN_N → U_adatpterLVDS_4 adatpterLVDS.SchDoc → dc_RESETN_P / dc_RESETN_N

DC_VDD

CLK640_P / CLK640_N → U_couplerAC couplerAC.SchDoc → dc_CLK640_P / dc_CLK640_N

DC_VDD

CLK40_P / CLK40_N → U_couplerAC couplerAC.SchDoc → dc_CLK40_P / dc_CLK40_N

DC_VDD

INJ_PULSE_P / INJ_PULSE_N → U_adatpterLVDS_7 adatpterLVDS.SchDoc → dc_INJ_PULSE_P / dc_INJ_PULSE_N

DC_VDD

SCK_DAC_P / SCK_DAC_N → U_adatpterLVDS_8 adatpterLVDS.SchDoc → dc_SCK_DAC_P / dc_SCK_DAC_N

DC_VDD

CS_LD_DAC_P / CS_LD_DAC_N → U_adatpterLVDS_9 adatpterLVDS.SchDoc → dc_CS_LD_DAC_P / dc_CS_LD_DAC_N

DC_VDD

SDI_DAC_P / SDI_DAC_N → U_adatpterLVDS_10 adatpterLVDS.SchDoc → dc_SDI_DAC_P / dc_SDI_DAC_N

DC_VDD

CLR_DAC_P / CLR_DAC_N → U_adatpterLVDS_11 adatpterLVDS.SchDoc → dc_CLR_DAC_P / dc_CLR_DAC_N

VDDPST, VDD, VDDA

U_ASIC ASIC.SchDoc

VDDA, VDD, VDDPST

ORWIDE_HIT_OUT_N, ORWIDE_HIT_OUT_P, INJ_OUT_N, INJ_OUT_P → ORWIDE_ASIC_N, ORWIDE_ASIC_P, INJ_ASIC_N, INJ_ASIC_P

dc_RESETN_N, dc_RESETN_P, dc_CLK640_N, dc_CLK640_P, dc_CLK40_N, dc_CLK40_P, dc_INJ_PULSE_N, dc_INJ_PULSE_P

SDO_N, SDO_P → SDO_IN_N, SDO_IN_P

dc_ASIC_SDI_N, dc_ASIC_SDI_P, dc_ASIC_SCLK_N, dc_ASIC_SCLK_P, dc_ASIC_SS_N, dc_ASIC_SS_P

U_Buffer_LVDS Buffer_LVDS.SchDoc

ORWIDE_IN_N, ORWIDE_IN_P, INJ_OUT_IN_N, INJ_OUT_IN_P → ORWIDE_BUF_N, ORWIDE_BUF_P, INJ_OUT_BUF_N, INJ_OUT_BUF_P

SDO_IN_N, SDO_IN_P → SDO_OUT_N, SDO_OUT_P → ASIC_SDO_N, ASIC_SDO_P

U_Trimmer_BIAS Trimmer_BIAS.SchDoc

BIAS_DAC, COMP_BIAS, VGG_PAD, AMP_BIAS, PMOS_BIAS, PRE_BIAS

CAL_HIGH, CAL_LOW, VREF_LKG, VTH → CAL_HI_MZN, CAL_LO_MZN, VREF_LKG_MZN, VTH_MZN

Gestisce le correnti di bias del frontend.

U_VoltageDAC VoltageDAC.SchDoc

dc_SCK_DAC_P, dc_SCK_DAC_N, dc_CS_LD_DAC_P, dc_CS_LD_DAC_N, dc_SDI_DAC_N, dc_SDI_DAC_P, dc_CLR_DAC_N, dc_CLR_DAC_P

CAL_HI, CAL_LO, VREF_LKG, VTH → CAL_HI_DAC, CAL_LO_DAC, VREF_LKG_DAC, VTH_DAC

SCK_DAC, CS_LD_DAC, SDI_DAC, CLR_DAC arrivano dalla fpga. Il DAC consente di gestire via software i riferimenti in tensione.

J5

SCK_DAC_N	1	2	SCK_DAC_P
CS_LD_DAC_N	3	4	CS_LD_DAC_P
SDI_DAC_N	5	6	SDI_DAC_P
CLR_DAC_N	7	8	CLR_DAC_P
	9	10	
ASIC_SCLK_N	11	12	ASIC_SCLK_P
ASIC_SS_N	13	14	ASIC_SS_P
ASIC_SDI_N	15	16	ASIC_SDI_P
	17	18	
	19	20	
CLK40_N	21	22	CLK40_P
	23	24	
CLK640_N	25	26	CLK640_P
	27	28	
INJ_PULSE_N	29	30	INJ_PULSE_P
	31	32	
RESETN_N	33	34	RESETN_P
	35	36	
ORWIDE_BUF_N	37	38	ORWIDE_BUF_P
	39	40	
INJ_OUT_BUF_N	41	42	INJ_OUT_BUF_P
	43	44	
ASIC_SDO_N	45	46	ASIC_SDO_P
	47	48	
	49	50	

SBH11-PBPC-D25-ST-BK

IDC_50

RR 100Ω

GND

Con i jumper J1, J2, J3, J4 posso scegliere se utilizzare le tensioni provenienti dal DAC oppure quelle fornite esternamente al connettore LEMO tramite alimentatore da banco

LEMO1 EPA.00.250.DTN → J1 22-28-4035 → GND

CAL_HI_MZN, CAL_HI_DAC

LEMO2 EPA.00.250.DTN → J2 22-28-4035 → GND

CAL_LO_MZN, CAL_LO_DAC

LEMO3 EPA.00.250.DTN → J3 22-28-4035 → GND

VTH_MZN, VTH_DAC

LEMO4 EPA.00.250.DTN → J4 22-28-4035 → GND

VREF_LKG_MZN, VREF_LKG_DAC

VDDA → U_LDO_1 LDO.SchDoc (VOUT) — Alimentazione analogica AVDD=900mV

VDD → U_LDO_2 LDO.SchDoc (VOUT) — Alimentazione digitale DVDD=900mV

VDDPST → U_LDO_5 LDO.SchDoc (VOUT) — Alimentazione ring 1.2V

3V3 → U_LDO_3 LDO.SchDoc (VOUT) — Alimentazione circuiti ausiliari

DC_VDD → U_LDO_4 LDO.SchDoc (VOUT) — DC_VDD 2.5V per accoppiamento da FPGA a ASIC

APPROVALS	DATE
ENG: Andrea Galliani	
DSN: Andrea Galliani	
CHK: *	

REFERENCE DOCUMENTS

BOM:

ASSY DWG:

FAB DWG:

PCB DWG:

PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control

DOCUMENT REVISION: Not in version control

DESIGN ITEM:

TITLE: motherboard

SIZE: A3

CAGE CODE:

DWG NO.

REV

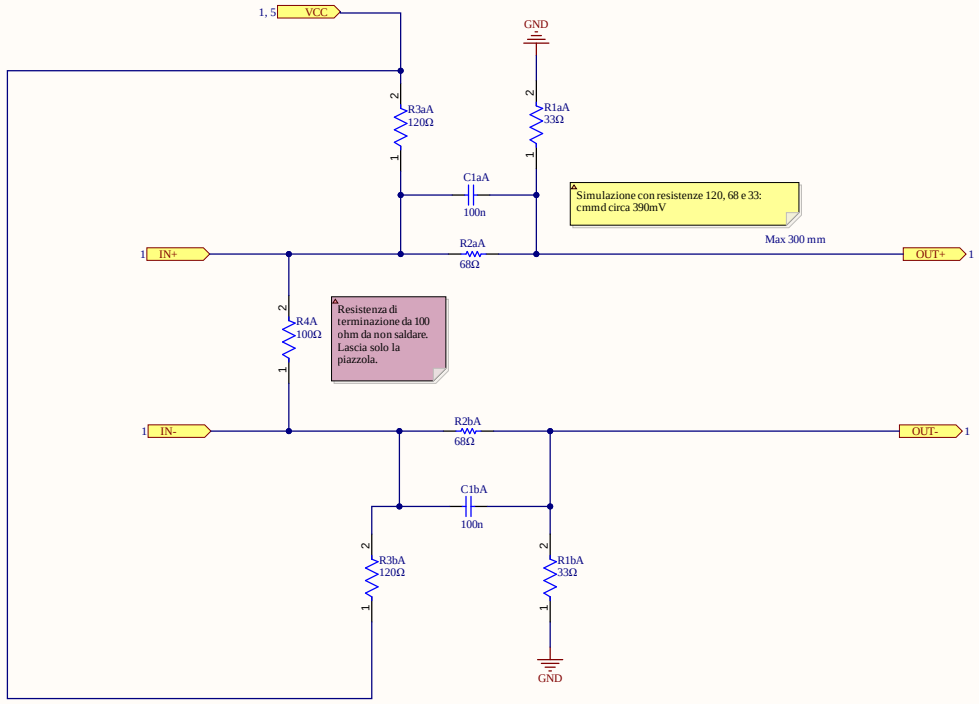
SCALE:

FILE NAME: motherboard.SchDoc

SHEET 1 OF 8

REVISION	DESCRIPTION	DATE	APPROVED

Vedi pagina 10 del pdf:
https://docs.amd.com/v/u/en-US/xapp894-d-phy-solutions



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ENG: Andrea Galliani	
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BOM:

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FAB DWG:

PCB DWG:

PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control

DOCUMENT REVISION: Not in version control

DESIGN ITEM:

TITLE: DC-coupling Circuit from LVDS to SLVS

SIZE	CAGE CODE	DWG NO.	REV
A3			

SCALE:

FILE NAME: adatpterLVDS.SchDoc

SHEET 2 OF 8

REVISION	DESCRIPTION	DATE	APPROVED

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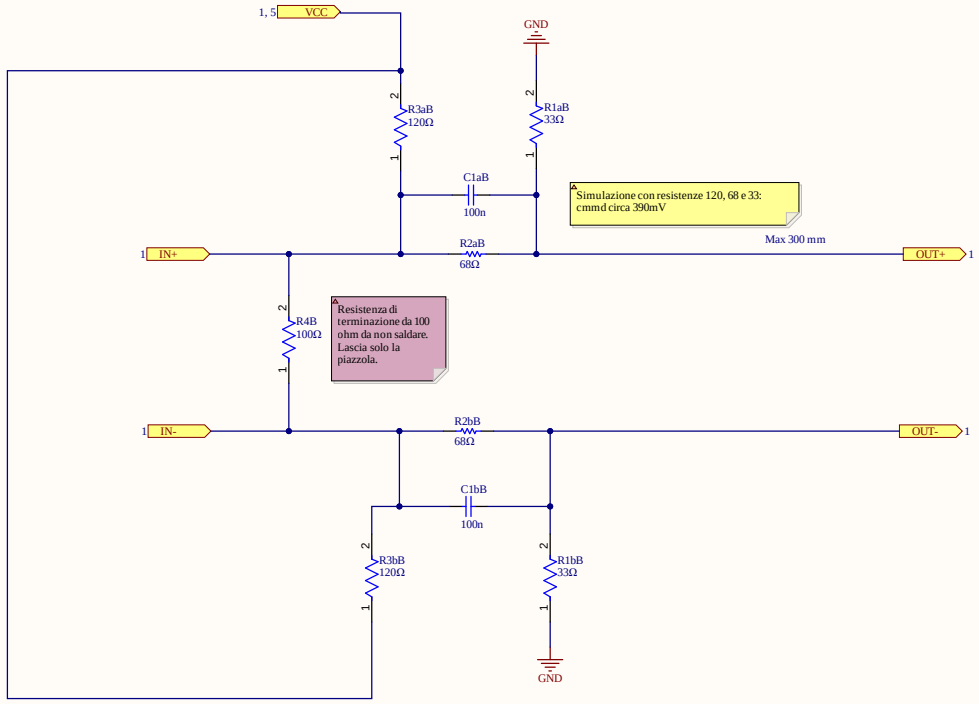
https://docs.amd.com/v/u/en-US/xapp894-d-phy-solutions



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PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control

DOCUMENT REVISION: Not in version control

DESIGN ITEM:

TITLE: DC-coupling Circuit from LVDS to SLVS

SIZE	CAGE CODE	DWG NO.	REV
A3			

SCALE:

FILE NAME: adatpterLVDS.SchDoc

SHEET 2 OF 8

REVISION	DESCRIPTION	DATE	APPROVED

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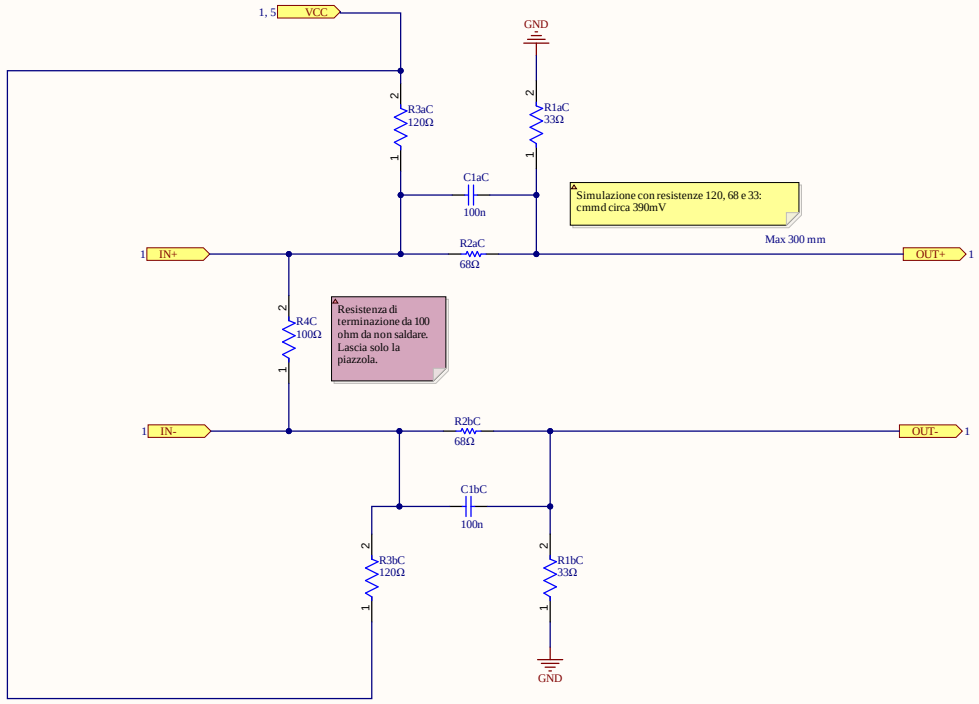

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TITLE: DC-coupling Circuit from LVDS to SLVS

SIZE	CAGE CODE	DWG NO.	REV
A3			

SCALE:

FILE NAME: adatpterLVDS.SchDoc

SHEET 2 OF 8

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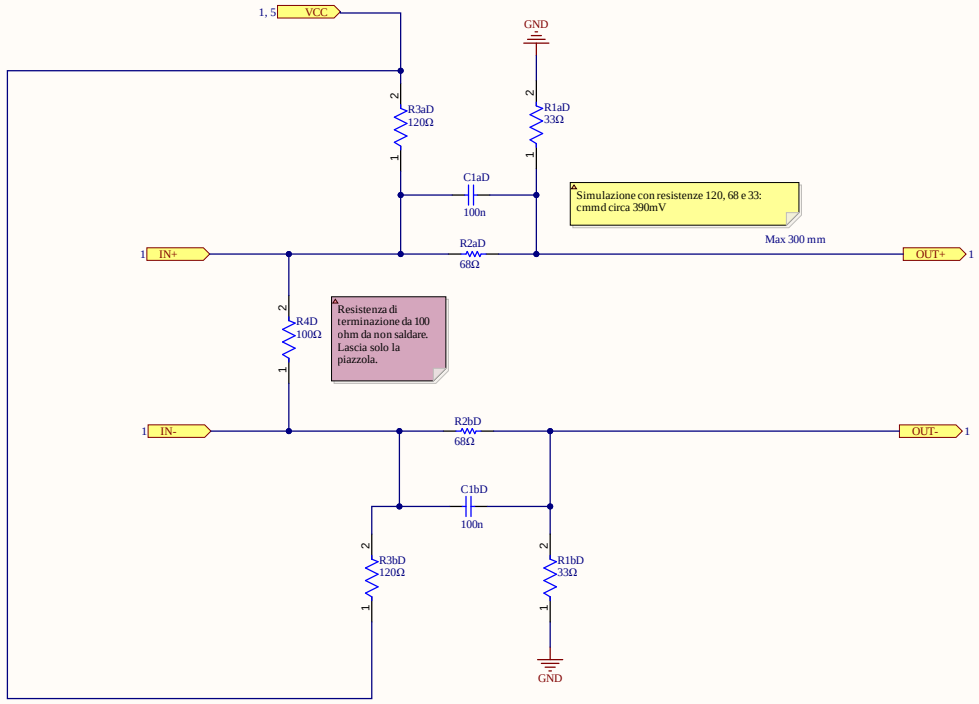

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SIZE	CAGE CODE	DWG NO.	REV
A3			

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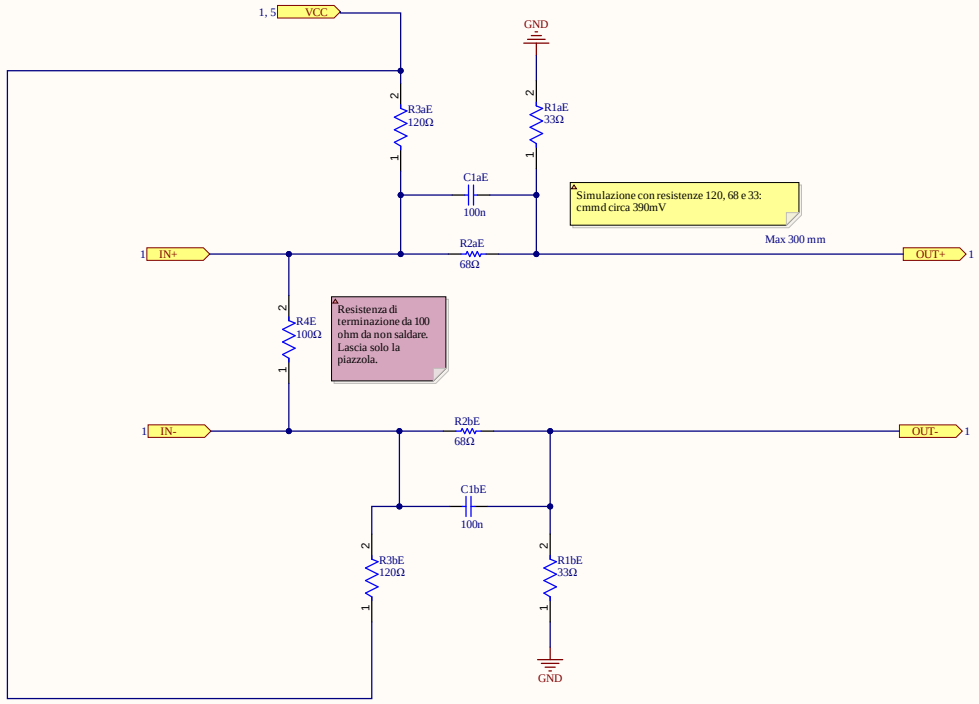

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PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control | DOCUMENT REVISION: Not in version control | DESIGN ITEM:

TITLE: DC-coupling Circuit from LVDS to SLVS

SIZE	CAGE CODE	DWG NO.	REV
A3			

SCALE: | FILE NAME: adatpterLVDS.SchDoc | SHEET 2 OF 8

REVISION	DESCRIPTION	DATE	APPROVED

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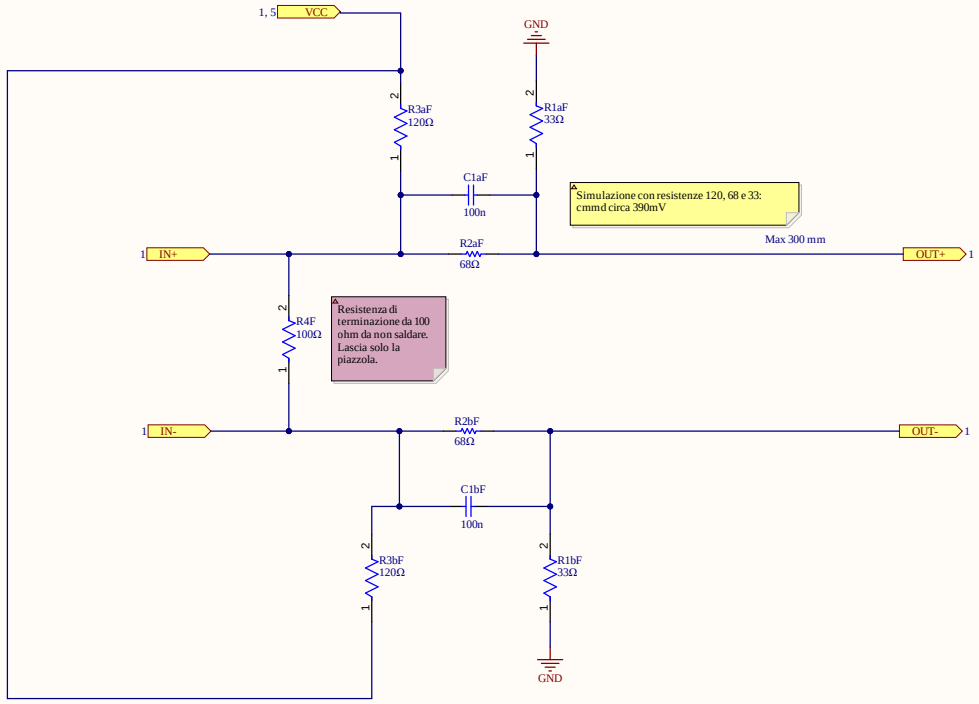

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PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control

DOCUMENT REVISION: Not in version control

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TITLE: DC-coupling Circuit from LVDS to SLVS

SIZE	CAGE CODE	DWG NO.	REV
A3			

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SHEET 2 OF 8

REVISION	DESCRIPTION	DATE	APPROVED

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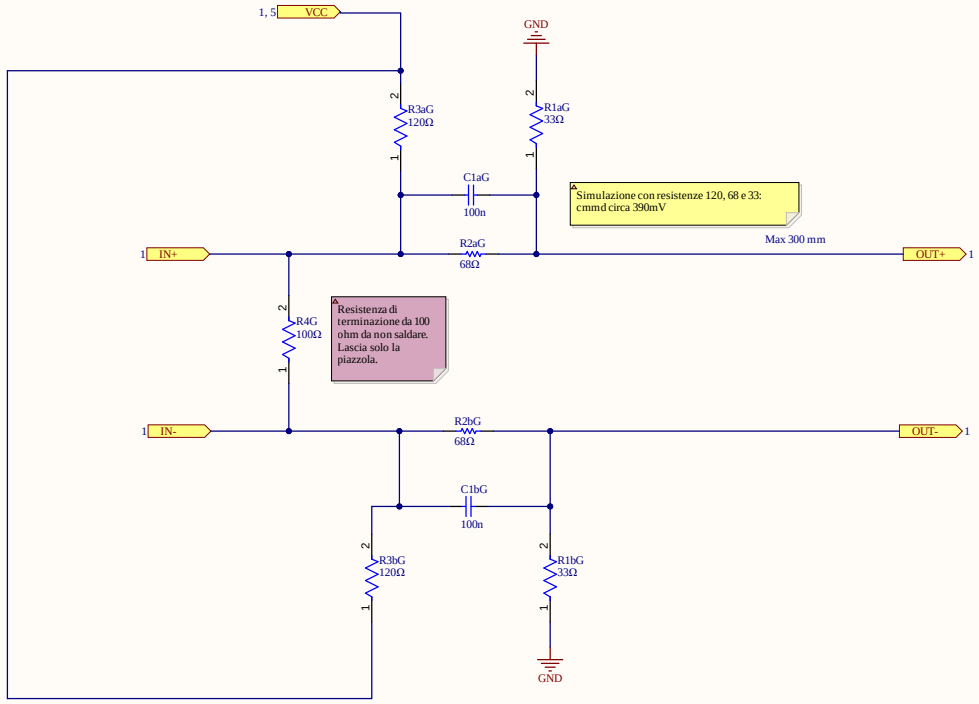

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PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control | DOCUMENT REVISION: Not in version control | DESIGN ITEM:

TITLE: DC-coupling Circuit from LVDS to SLVS

SIZE	CAGE CODE	DWG NO.	REV
A3			

SCALE: | FILE NAME: adatpterLVDS.SchDoc | SHEET 2 OF 8

REVISION	DESCRIPTION	DATE	APPROVED

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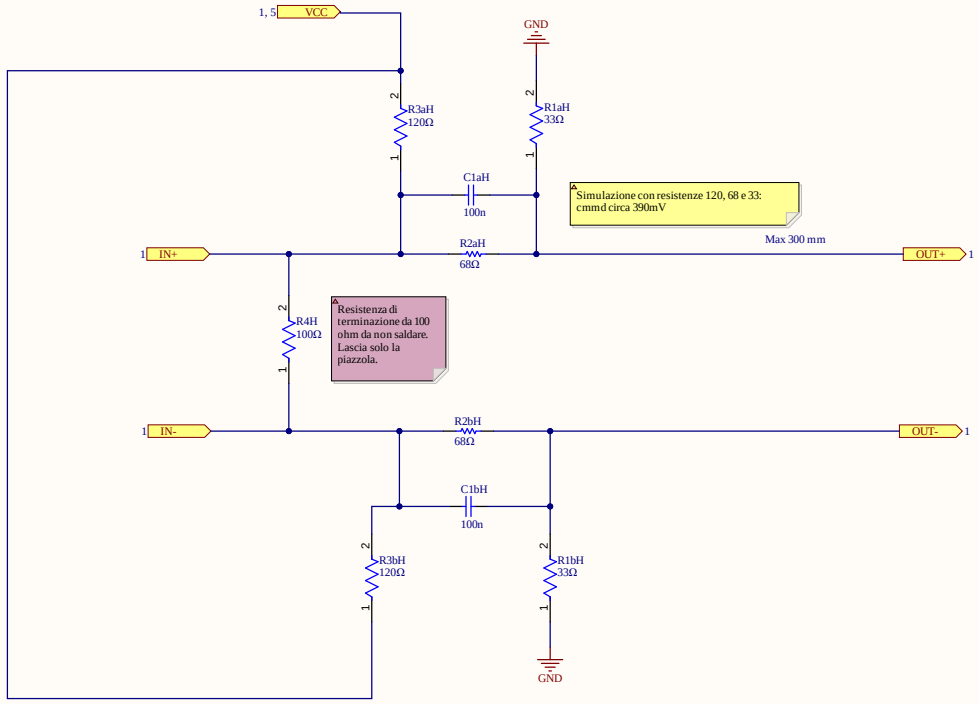

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FAB DWG:

PCB DWG:

PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control

DOCUMENT REVISION: Not in version control

DESIGN ITEM:

TITLE: DC-coupling Circuit from LVDS to SLVS

SIZE	CAGE CODE	DWG NO.	REV
A3			

SCALE:

FILE NAME: adatpterLVDS.SchDoc

SHEET 2 OF 8

REVISION	DESCRIPTION	DATE	APPROVED

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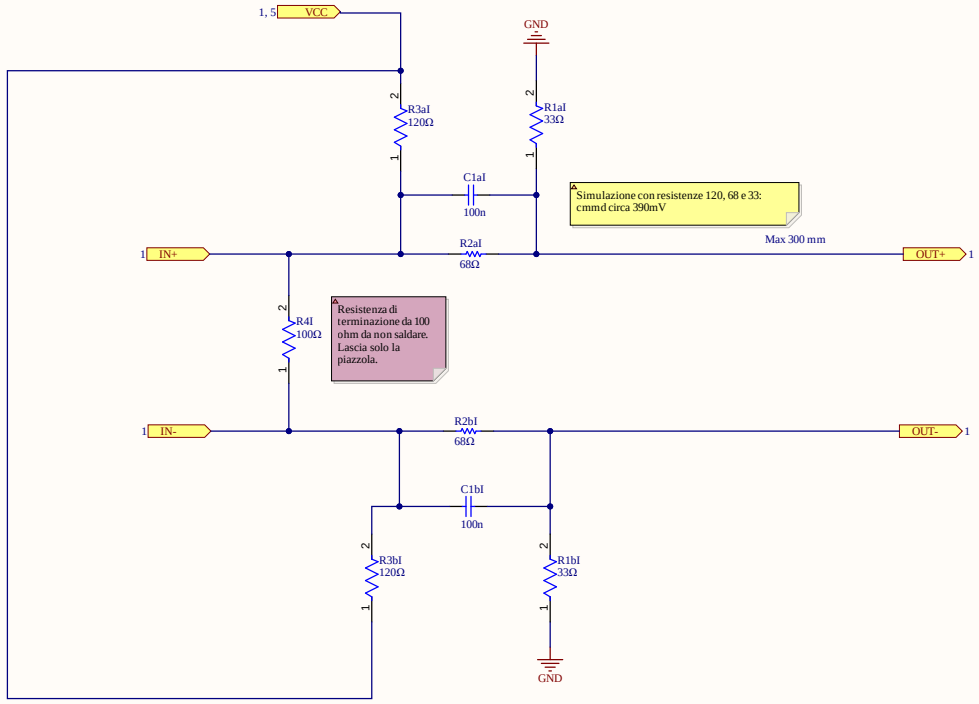

APPROVALS	DATE
ENG: Andrea Galliani	
DSN: Andrea Galliani	
CHK: *	

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FAB DWG:

PCB DWG:

PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control

DOCUMENT REVISION: Not in version control

DESIGN ITEM:

TITLE: DC-coupling Circuit from LVDS to SLVS

SIZE	CAGE CODE	DWG NO.	REV
A3			

SCALE:

FILE NAME: adatpterLVDS.SchDoc

SHEET 2 OF 8

REVISION	DESCRIPTION	DATE	APPROVED

N.B.:
I connettori devono essere fisicamente allineati a quelli della mezzanina.

J4_M 61301811821

ORWIDE_HIT_OUT_N, ORWIDE_HIT_OUT_P, INJ_OUT_N, INJ_OUT_P, dc_RESETN_N, dc_RESETN_P, dc_INJ_PULSE_N, dc_INJ_PULSE_P, VDDPST, VDDA, GND, dc_CLK640_N, dc_CLK640_P, dc_CLK40_N, dc_CLK40_P, SDO_N, SDO_P

ORWIDE_HIT_OUT_N
ORWIDE_HIT_OUT_P
INJ_OUT_N
INJ_OUT_P

Output digitali

dc_RESETN_N
dc_RESETN_P
dc_INJ_PULSE_N
dc_INJ_PULSE_P
dc_CLK40_P
dc_CLK40_N
dc_CLK640_P
dc_CLK640_N

Input digitali

VDDA alimentazione matrice 900mV

DVDD alimentazione matrice digitale 900mV

VDDPST alimentazione ring 1.2V

VDDA, VDD, VDDPST

SDO_P
SDO_N

U_MEZZANINA
ToT_Mezzanina

GND, NC, VDD_OVEST1, VDD_OVEST2, VDD_OVEST3, VDDPST_OVEST, VDD_OVEST4, VDD_OVEST5, VDD_OVEST6

GND, VDD_EST1, VDD_EST2, VDDPST_EST, SDI_P, SDI_N, SS_P, SS_N, SCLK_P, SCLK_N

ORWIDE_HIT_OUT_N, ORWIDE_HIT_OUT_P, INJ_OUT_N, INJ_OUT_P, RESETN_N, RESETN_P, INJ_PULSE_N, INJ_PULSE_P, VDDPST_NORD, GND, VDDA_NORD, GND, CLK640_N, CLK640_P, CLK40_N, CLK40_P, SDO_N, SDO_P

VDD_SUD, GND, VTH, VREF_LKG, CAL_HIGH, CAL_LOW, VGG, VDDPST_SUD2, GND, VDDA_SUD, GND, PMOS_BIAS, AMP_BIAS, PRE_BIAS, COMP_BIAS, BIAS_DAC, VDDPST_SUD1, GND

J1_M 61301211821

12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1

VDDPST, VDD, GND

J3_M 61301211821

1, 2, 3, 4, 5, 6, dc_ASIC_SDI_P, dc_ASIC_SDI_N, dc_ASIC_SS_P, dc_ASIC_SS_N, dc_ASIC_SCLK_P, dc_ASIC_SCLK_N

VDDPST, VDD, GND

dc_ASIC_SDI_P
dc_ASIC_SDI_N
dc_ASIC_SS_P
dc_ASIC_SS_N
dc_ASIC_SCLK_P
dc_ASIC_SCLK_N

CAL_LOW
CAL_HIGH
VREF_LKG
VTH

Riferimenti in tensione

PMOS_BIAS
AMP_BIAS
PRE_BIAS
COMP_BIAS
BIAS_DAC
VGG_PAD

Bias in corrente

VDD, VDDA, VDDPST, GND

VTH, VREF_LKG, CAL_HIGH, CAL_LOW, VGG_PAD, PMOS_BIAS, AMP_BIAS, PRE_BIAS, COMP_BIAS, BIAS_DAC

J2_M 61301811821

APPROVALS	DATE
ENG: *	
DSN: Andrea Galliani	
CHK: *	

REFERENCE DOCUMENTS

BOM:

ASSY DWG:

FAB DWG:

PCB DWG:

PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control

DOCUMENT REVISION: Not in version control

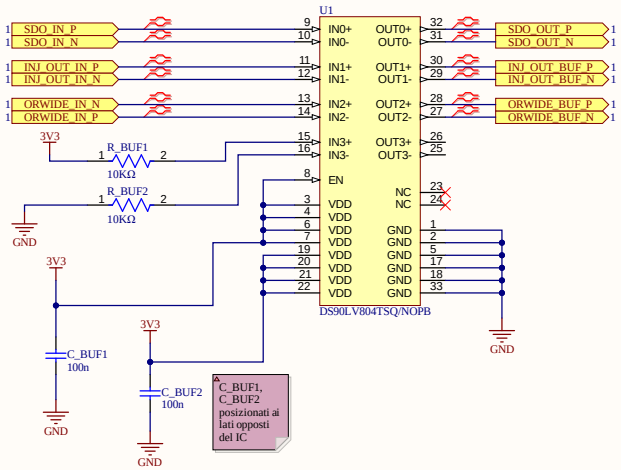
DESIGN ITEM:

TITLE: ASIC

SIZE	CAGE CODE	DWG NO.	REV
A3			

SCALE: FILE NAME: ASIC.SchDoc SHEET 3 OF 8

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
ENG: Andrea Galliani	
DSN: Andrea Galliani	
CHK: *	
REFERENCE DOCUMENTS	
BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT: FALAPHEL3

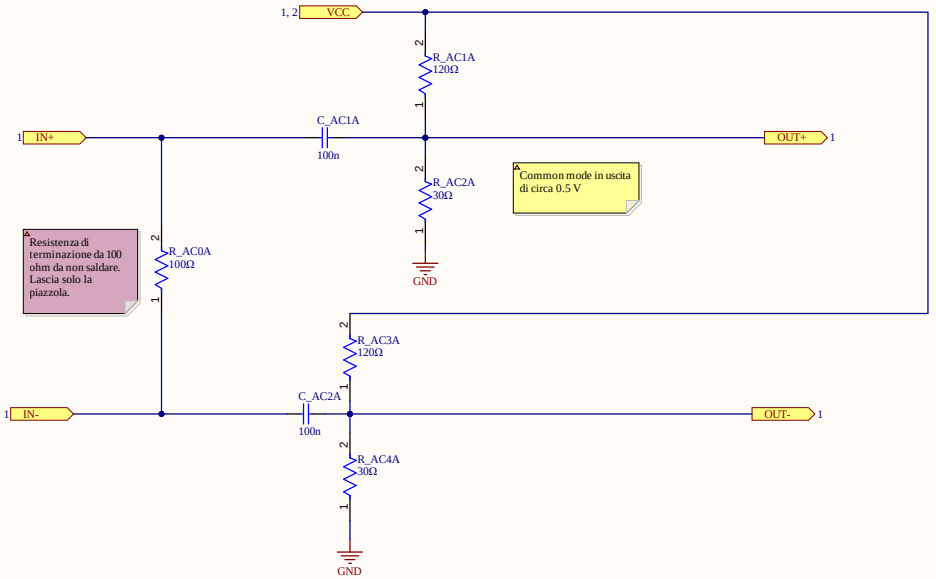
PROJECT REVISION: Not in version control | DOCUMENT REVISION: Not in version control | DESIGN ITEM:

TITLE: Buffer LVDS

SIZE	CAGE CODE	DWG NO.	REV
A3			

SCALE: | FILE NAME: Buffer_LVDS.SchDoc | SHEET 4 OF 8

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
ENG: *	
DSN: *	
CHK: *	
REFERENCE DOCUMENTS	
BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT: FALAPHEL3

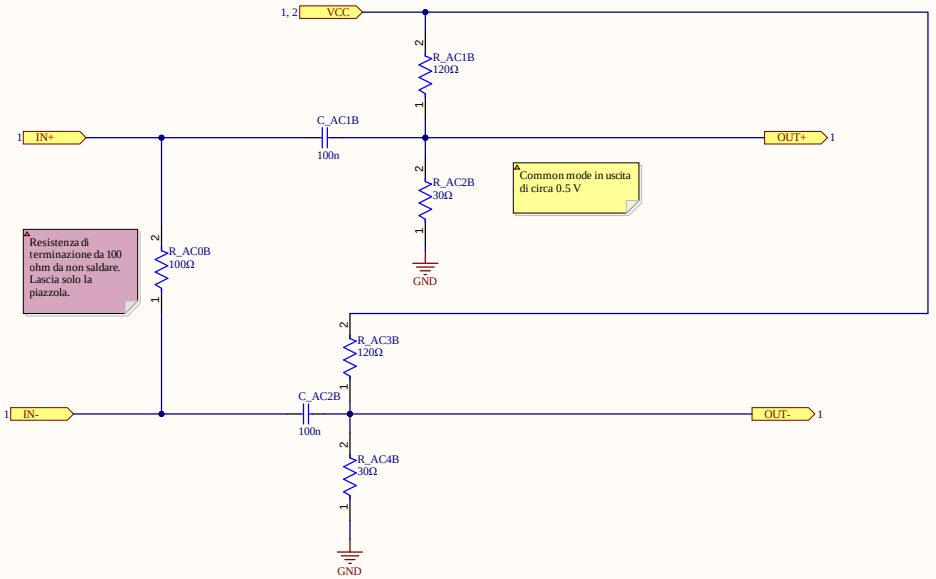
PROJECT REVISION: Not in version control | DOCUMENT REVISION: Not in version control | DESIGN ITEM:

TITLE: Accoppiamento AC per i clock

SIZE	CAGE CODE	DWG NO.	REV
A3			

SCALE: | FILE NAME: couplerAC.SchDoc | SHEET 5 OF 8

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
ENG:	
DSN:	
CHK:	
REFERENCE DOCUMENTS	
BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control | DOCUMENT REVISION: Not in version control | DESIGN ITEM:

TITLE: Accoppiamento AC per i clock

SIZE	CAGE CODE	DWG NO.	REV
A3			

SCALE: | FILE NAME: couplerAC.SchDoc | SHEET 5 OF 8

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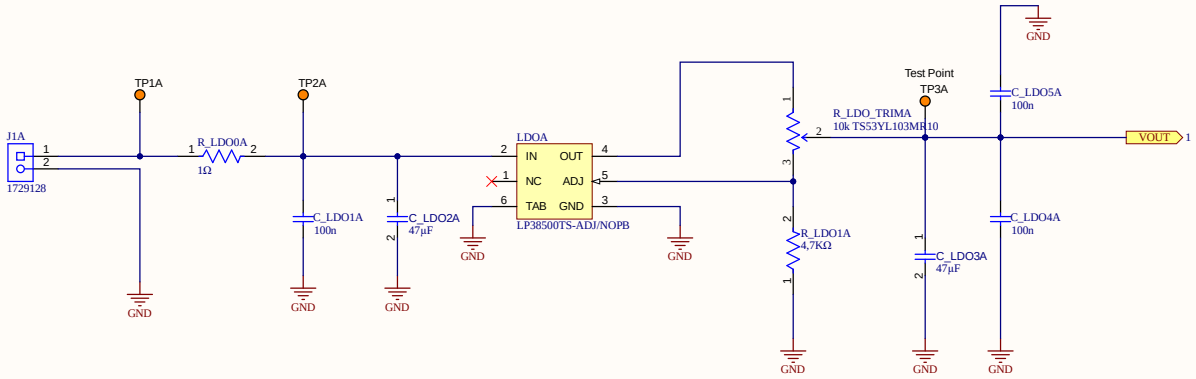

APPROVALS	DATE
ENG: Andrea Galliani	
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BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT: FALAPHEL3

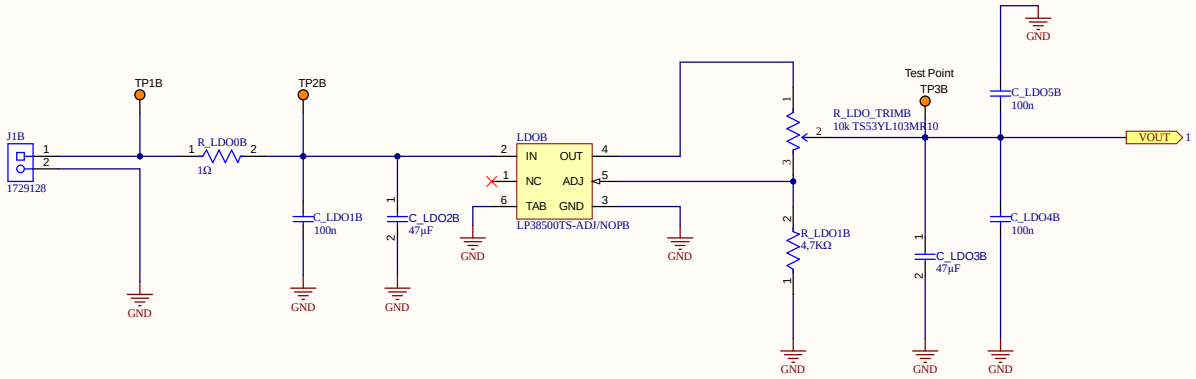
PROJECT REVISION: Not in version control | DOCUMENT REVISION: Not in version control | DESIGN ITEM:

TITLE: LDO

SIZE	CAGE CODE	DWG NO.	REV
A3			

SCALE: | FILE NAME: LDO.SchDoc | SHEET 6 OF 8

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
ENG: Andrea Galliani	
DSN: Andrea Galliani	
CHK: *	
REFERENCE DOCUMENTS	
BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control

DOCUMENT REVISION: Not in version control

DESIGN ITEM:

TITLE: LDO

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FILE NAME: LDO.SchDoc

SHEET 6 OF 8

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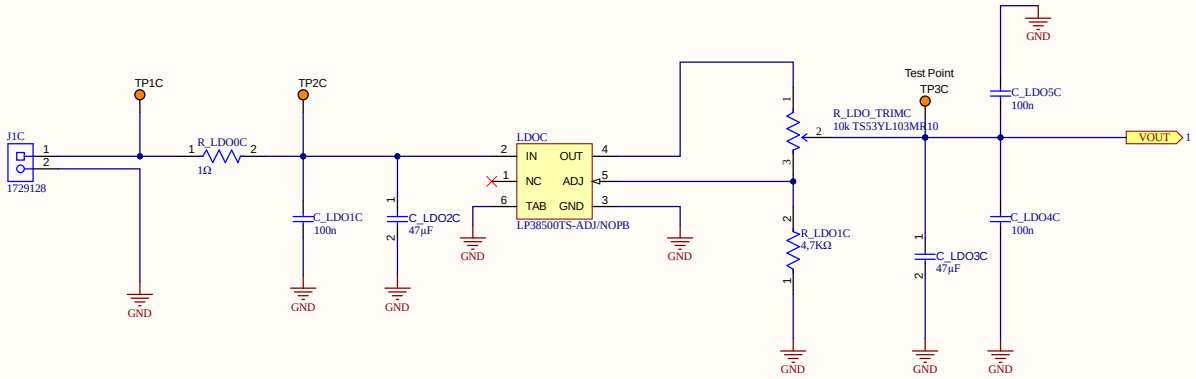

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REFERENCE DOCUMENTS	
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PCB DWG:	

PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control

DOCUMENT REVISION: Not in version control

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FILE NAME: LDO.SchDoc

SHEET 6 OF 8

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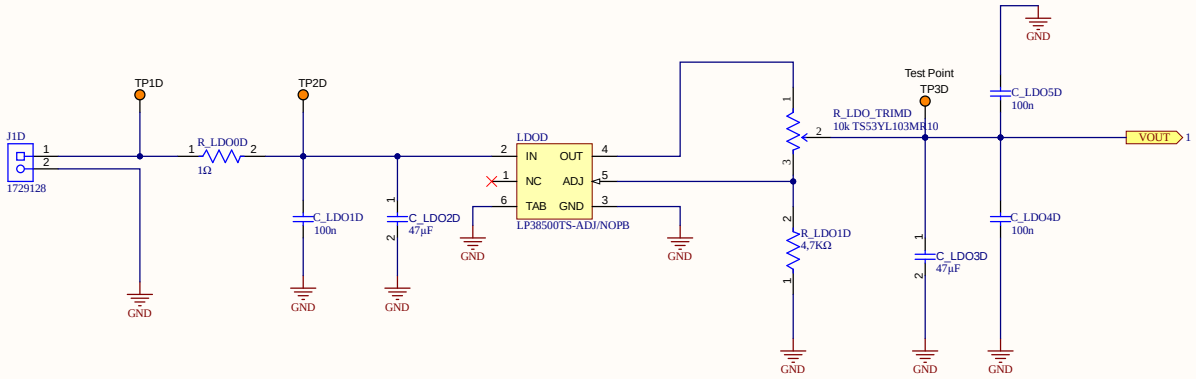

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PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control | DOCUMENT REVISION: Not in version control | DESIGN ITEM:

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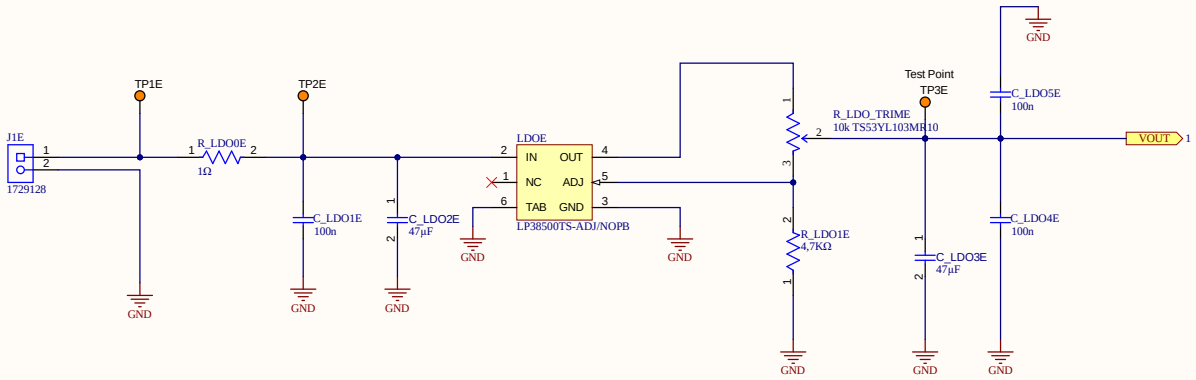
SCALE: | FILE NAME: LDO.SchDoc | SHEET 6 OF 8

REVISION	DESCRIPTION	DATE	APPROVED



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FAB DWG:	
PCB DWG:	

PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control | DOCUMENT REVISION: Not in version control | DESIGN ITEM:

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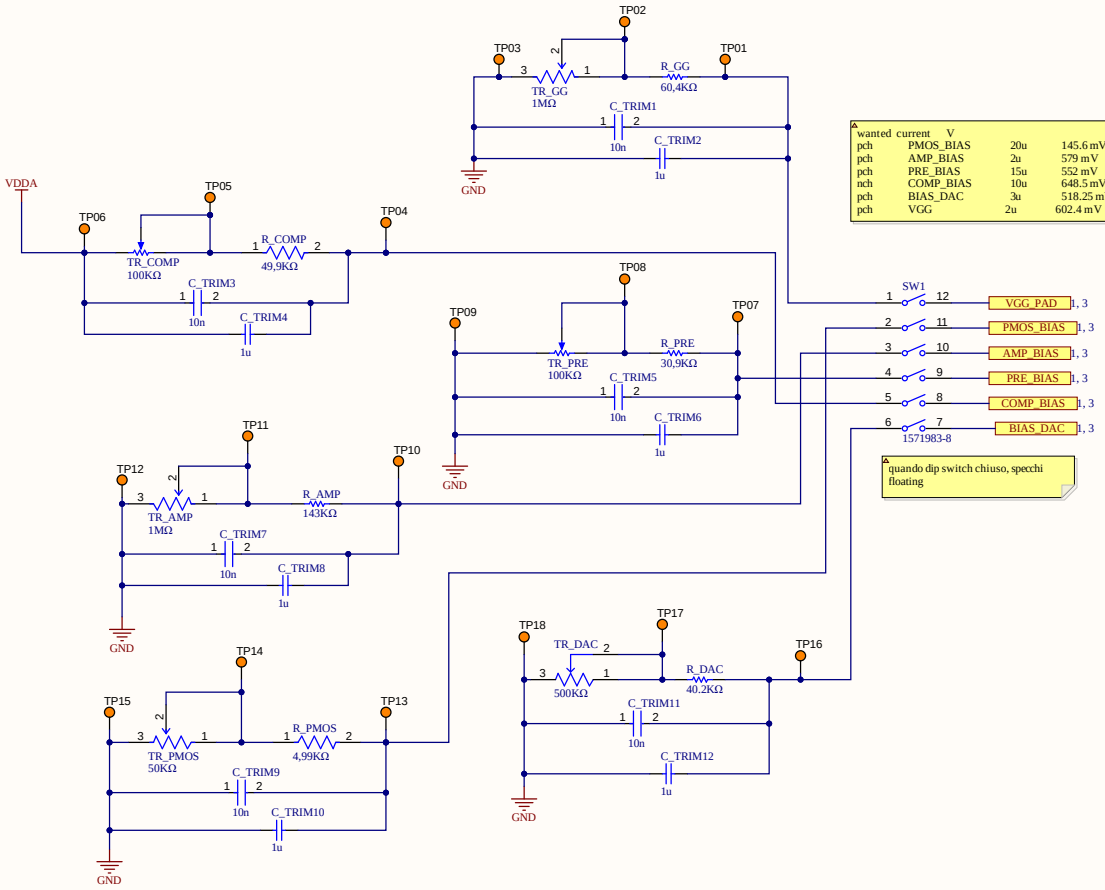
A3			

SCALE: | FILE NAME: LDO.SchDoc | SHEET 6 OF 8

REVISION	DESCRIPTION	DATE	APPROVED



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ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control

DOCUMENT REVISION: Not in version control

DESIGN ITEM:

TITLE: Trimmer BIAS periferia

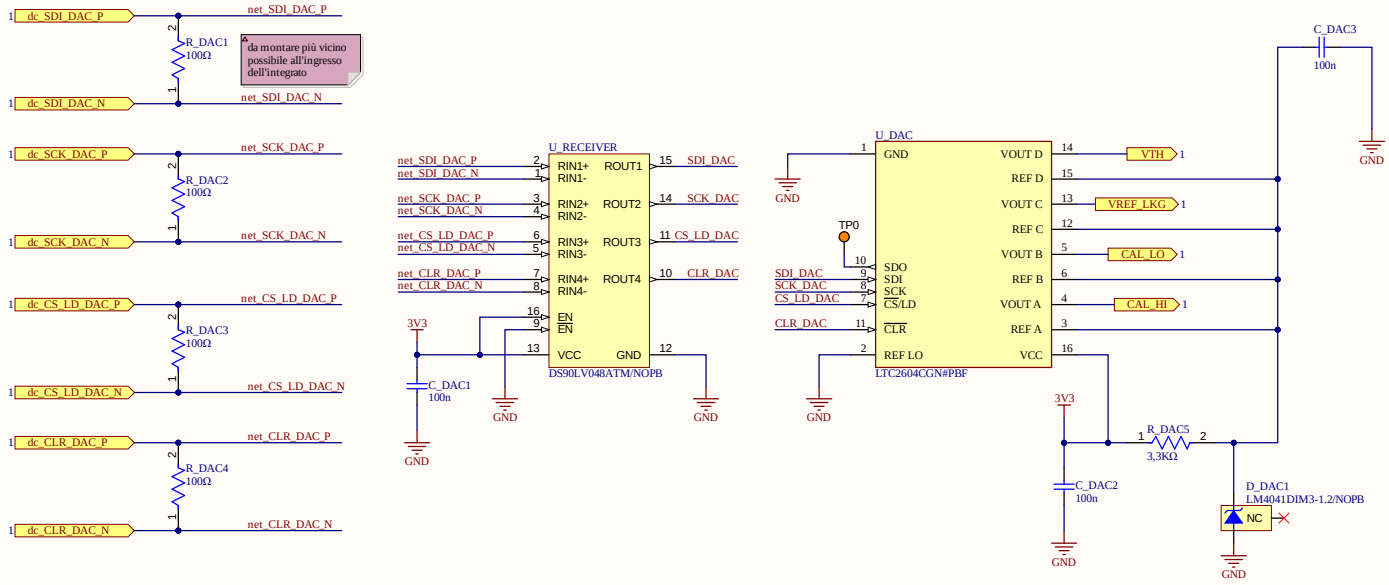
SIZE	CAGE CODE	DWG NO.	REV
A3			

SCALE:

FILE NAME: Trimmer_BIAS.SchDoc

SHEET 7 OF 8

REVISION	DESCRIPTION	DATE	APPROVED



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REFERENCE DOCUMENTS	
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ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT: FALAPHEL3

PROJECT REVISION: Not in version control

DOCUMENT REVISION: Not in version control

DESIGN ITEM:

TITLE: Voltage DAC

SIZE	CAGE CODE	DWG NO.	REV
A3			

SCALE:

FILE NAME: VoltageDAC.SchDoc

SHEET 8 OF 8