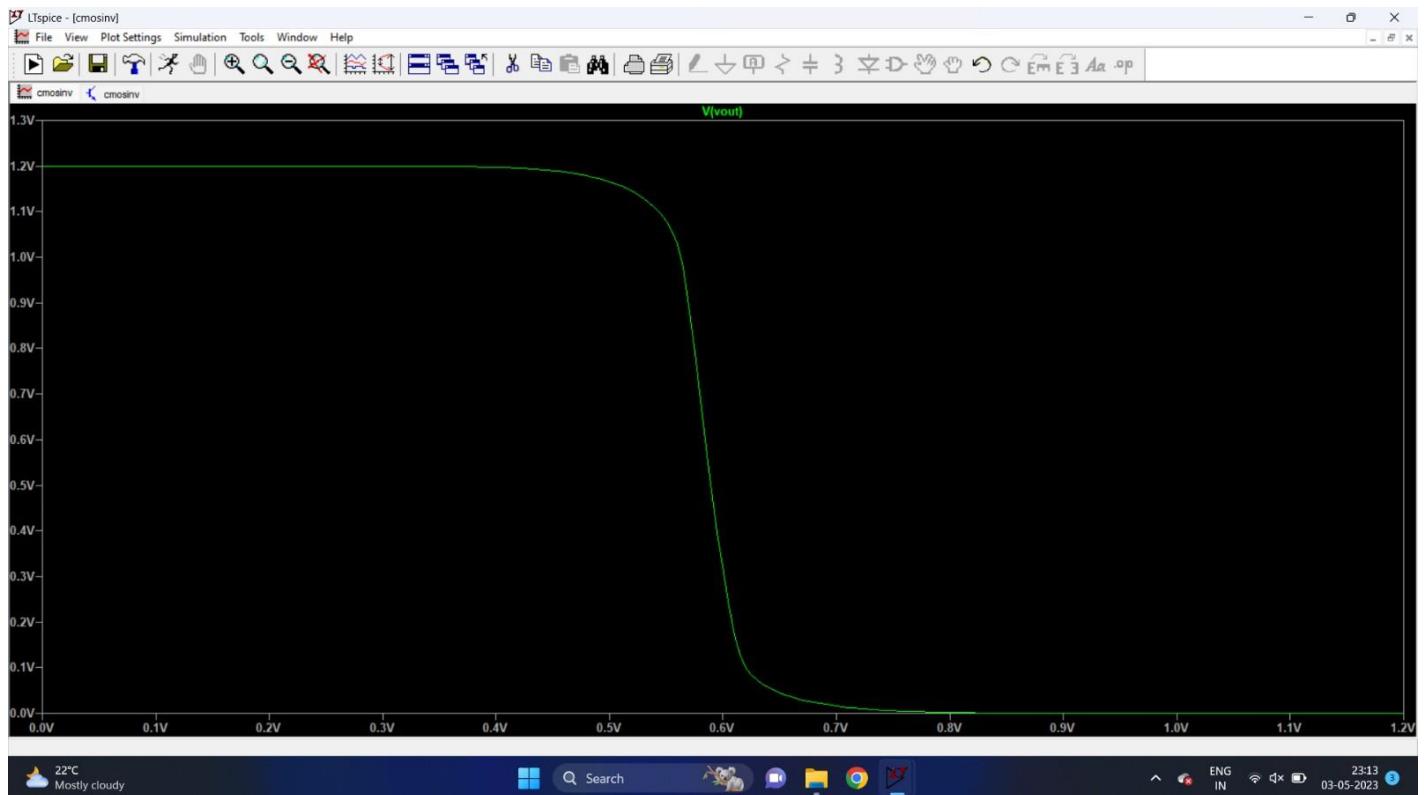
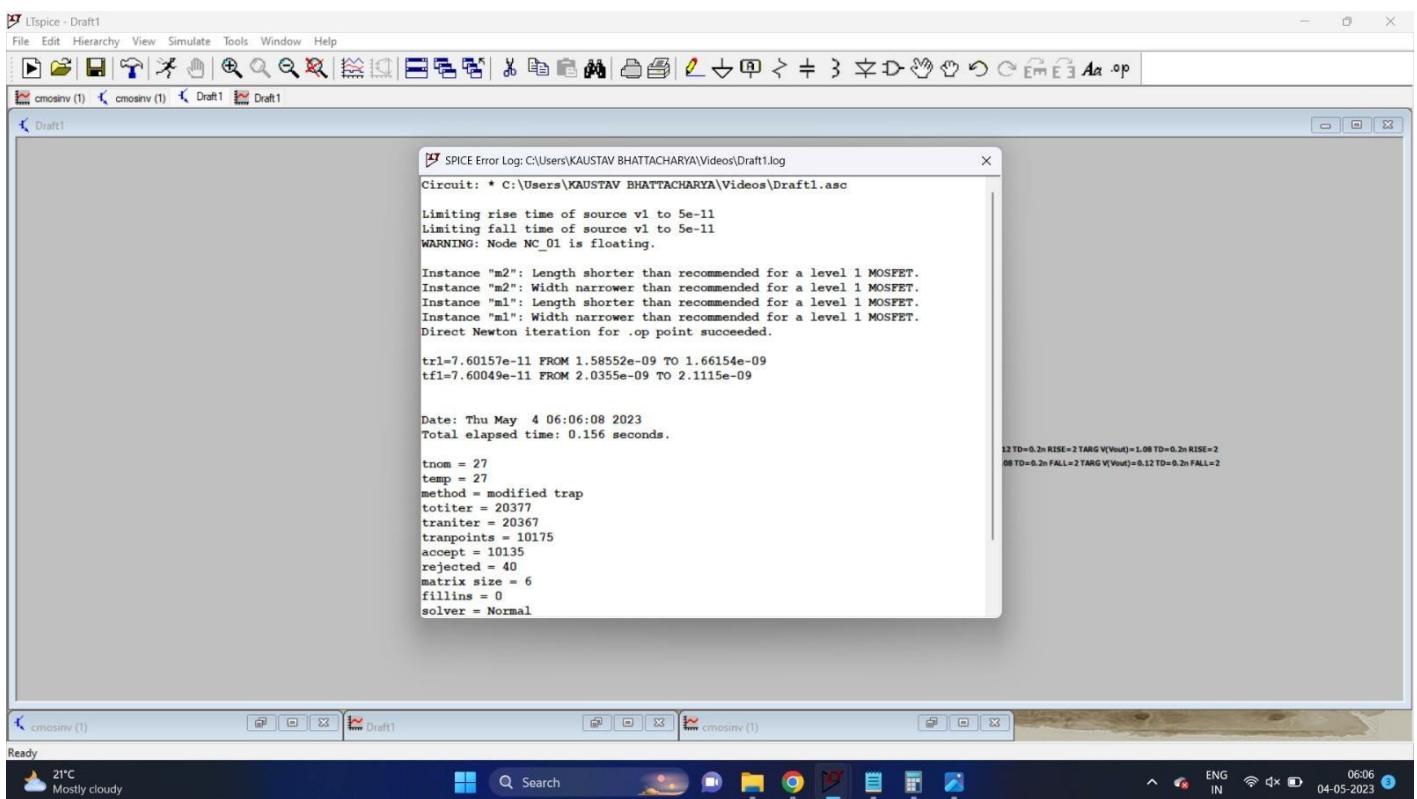
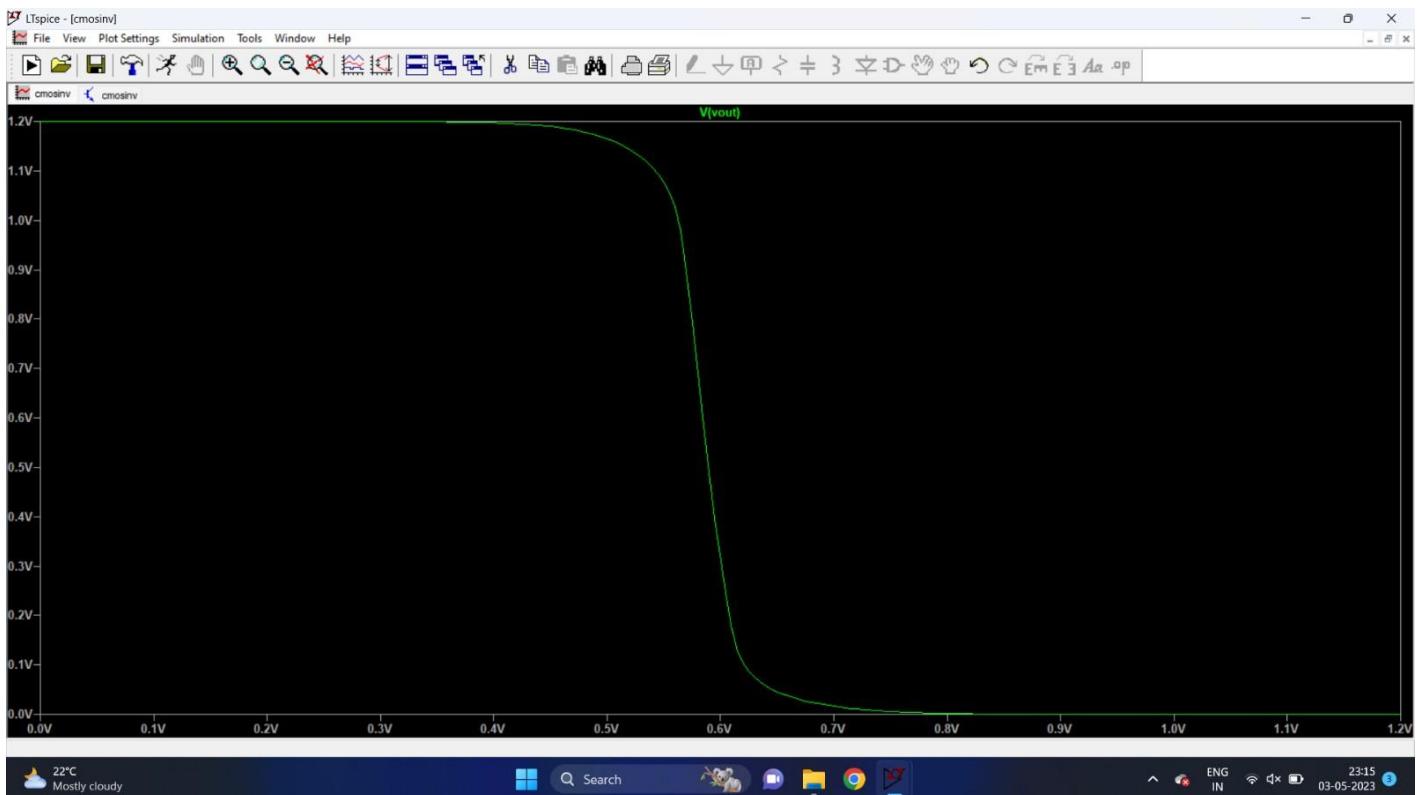


SPICE ProjectProblem 1:

Do an analysis to find out the PMOS to NMOS size ratio of the minimum-sized CMOS inverter to have equal rise and fall time. Simulate the static VTC of that inverter, and find out signalling threshold values (V_{IL} , V_{IH} , V_{OL} , V_{OL}) using the slope = -1 criterion from the VTC. Write down high and low noise margins, and the noise immunity of the inverter. Also, simulate the static VTC of an inverter which is sized S times the minimum-sized inverter (both NMOS and PMOS are S times the size of the corresponding NMOS and PMOS of the minimum-sized inverter) for $S = 1, 2, 4$, and plot all VTCs in a single graph with clear legends indicating how the sizing affects the VTC.

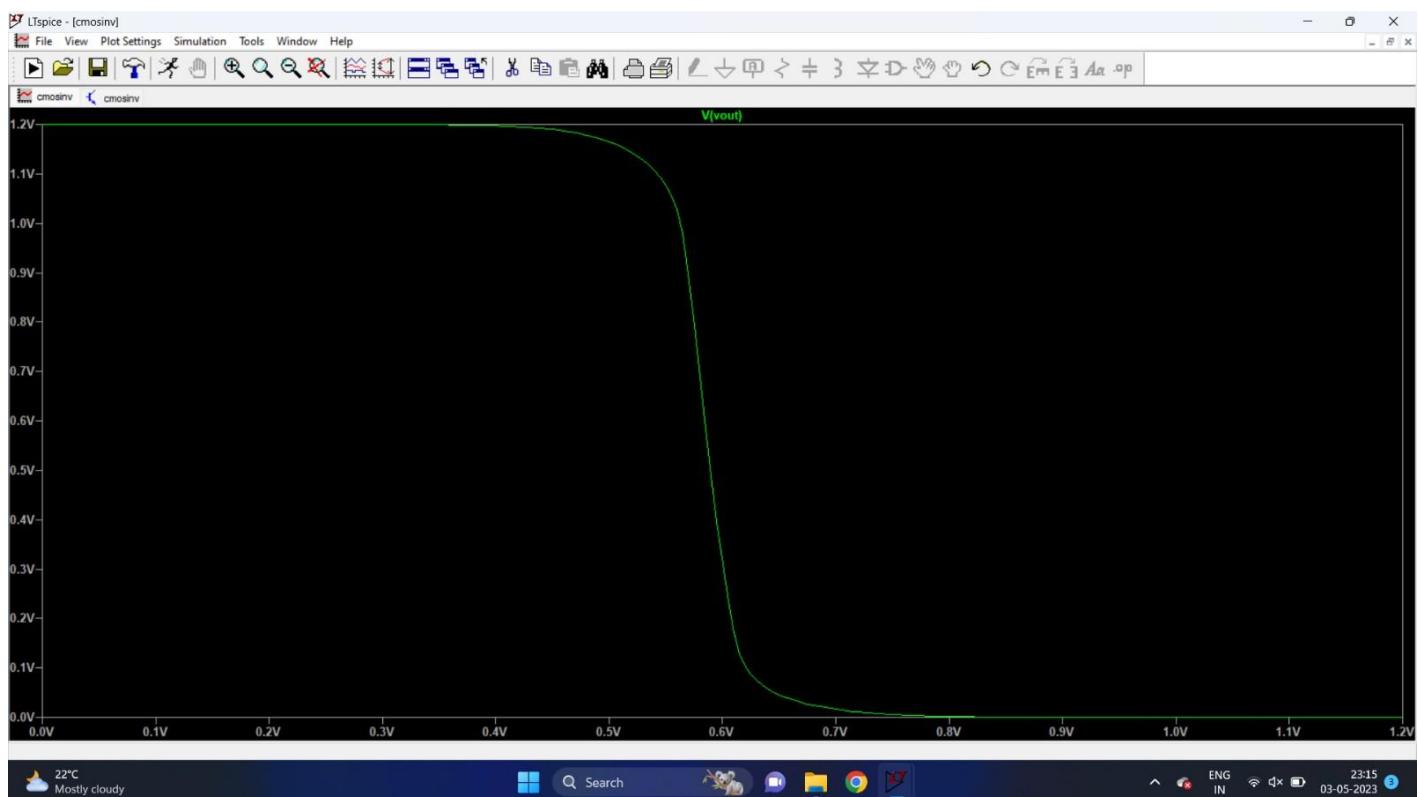
Solution:

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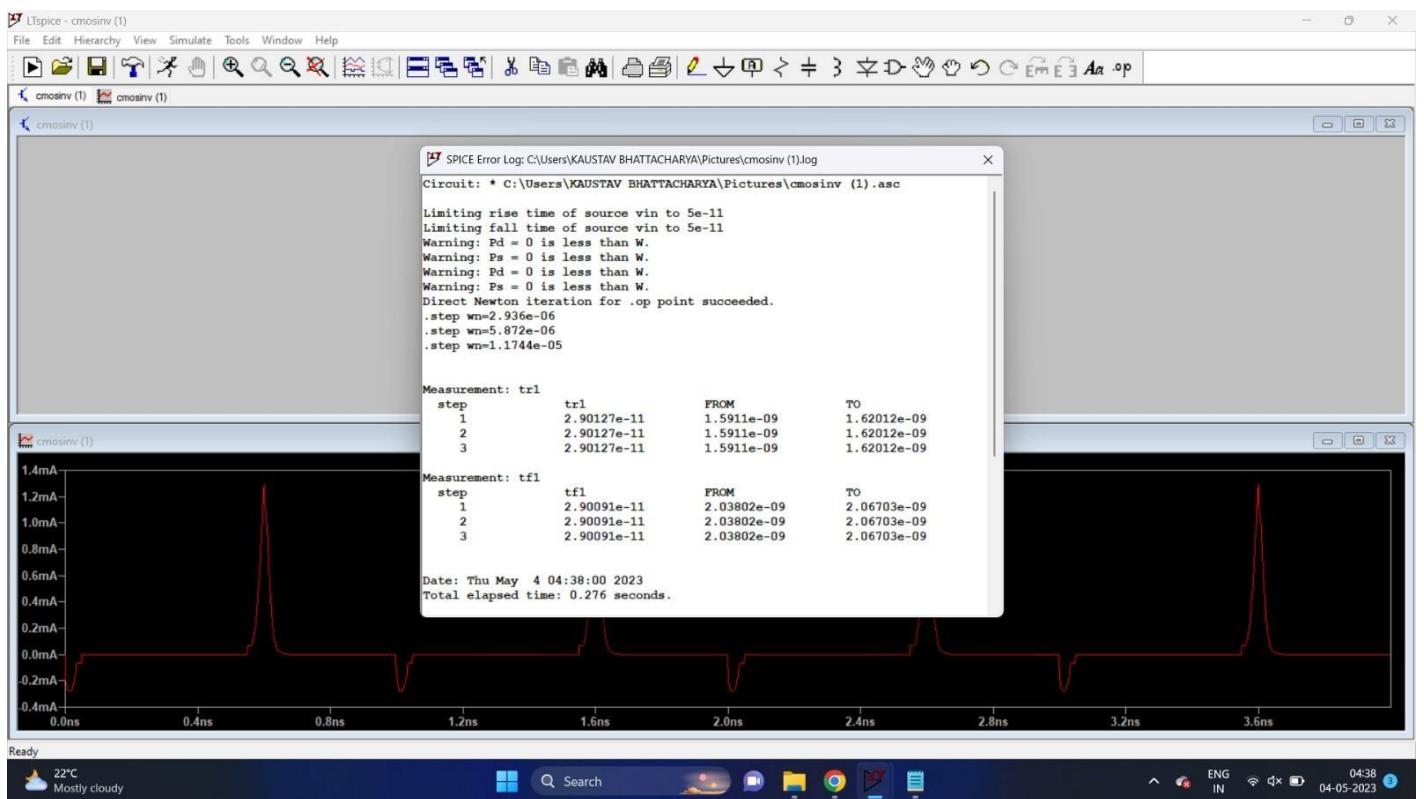
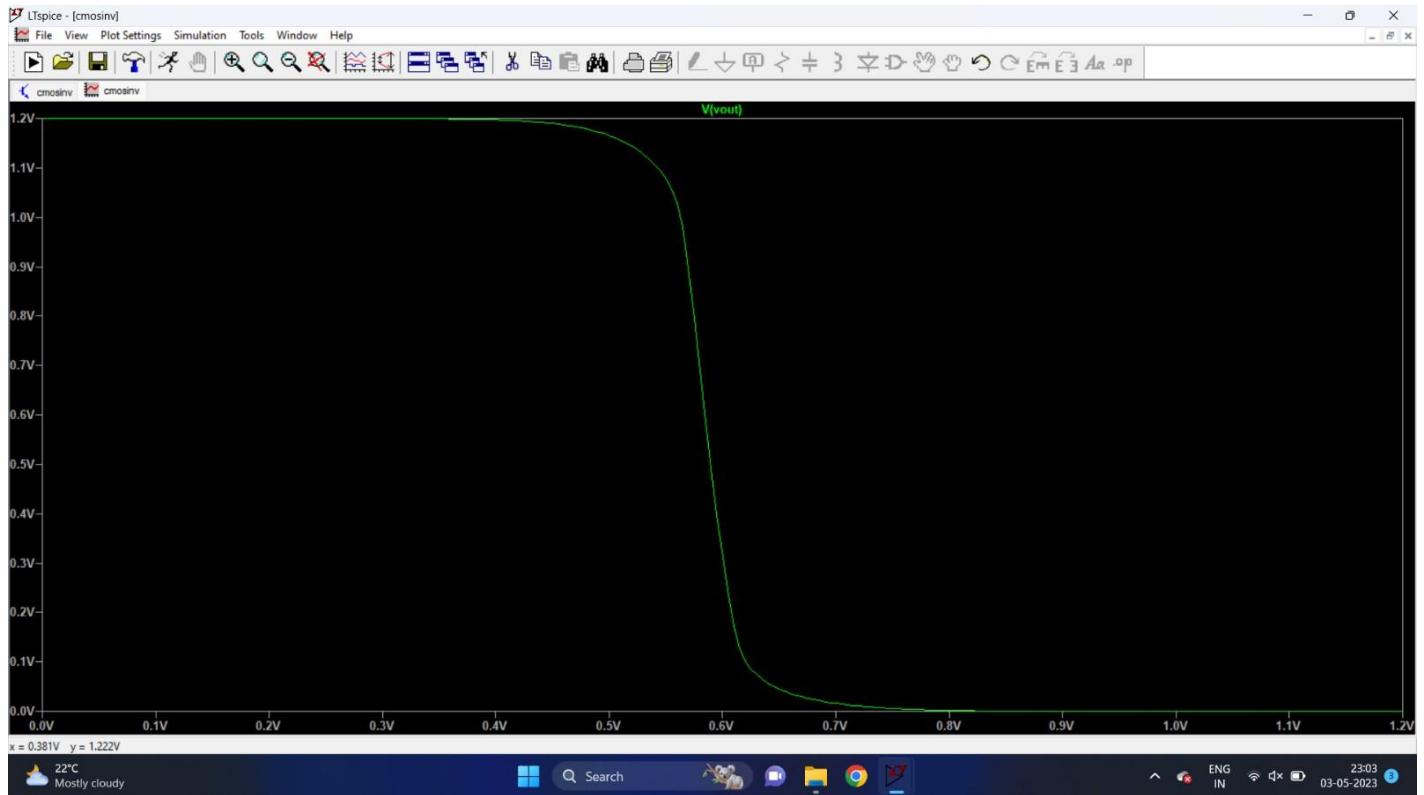


Problem 2:

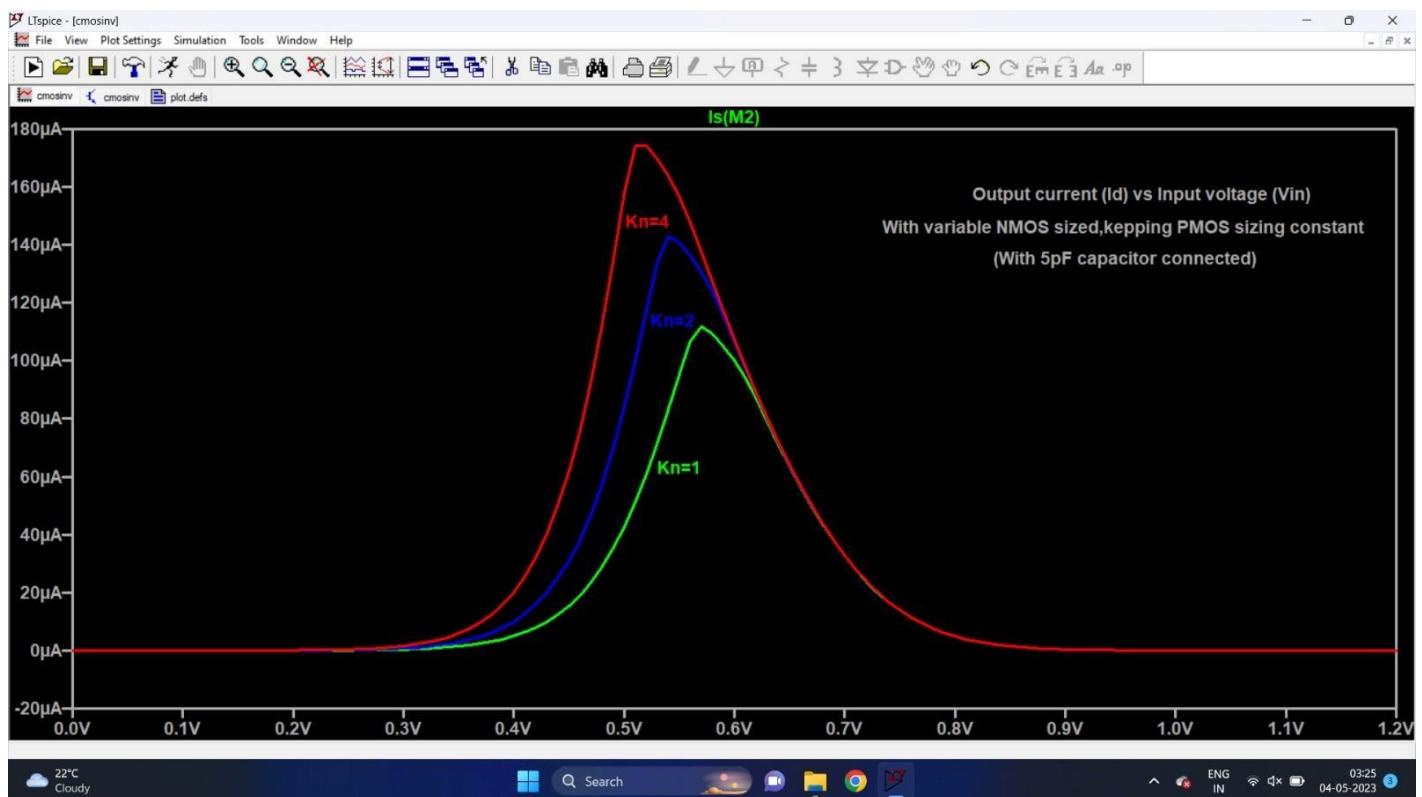
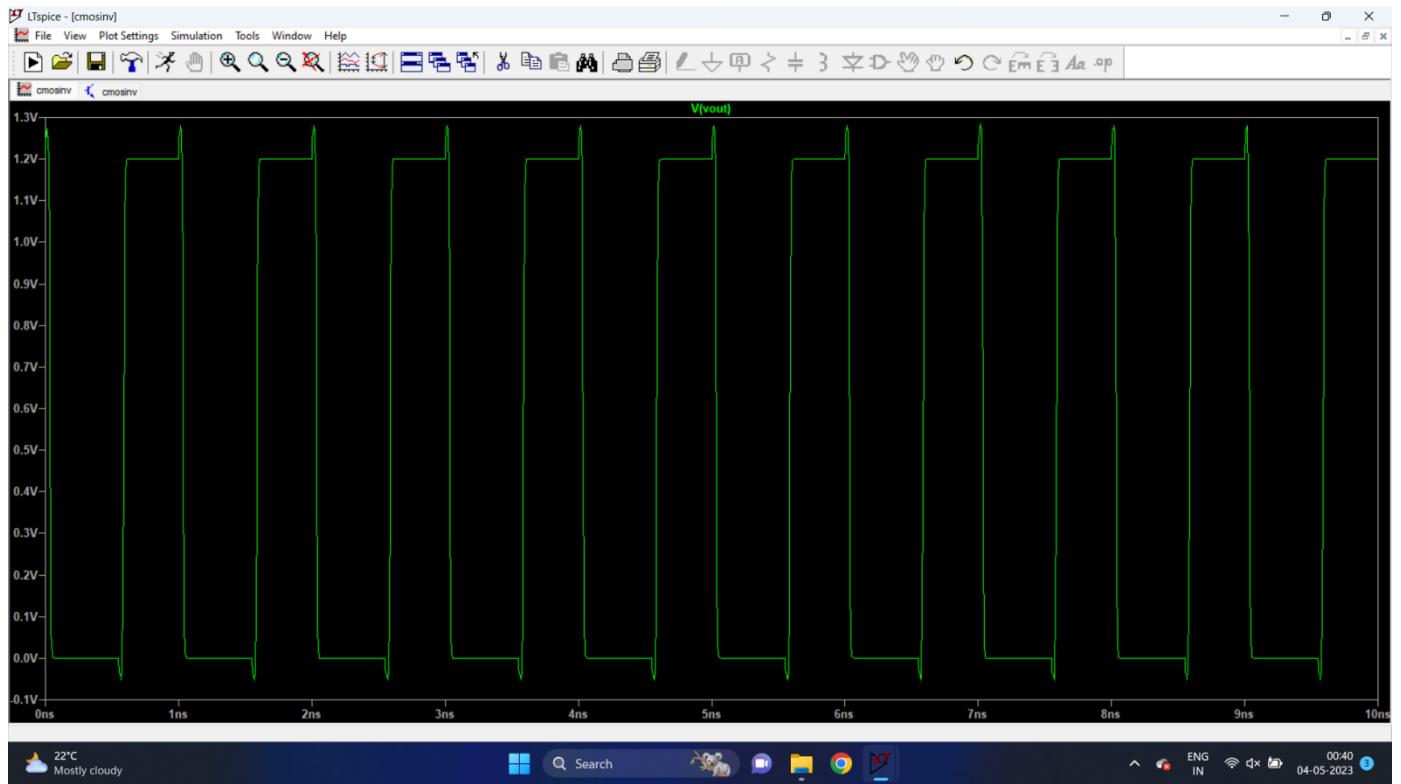
Carry out transient analysis to find out the rise time and fall time delays of a CMOS inverter sized $S = 1, 2, 4$, when (i) no external capacitor is attached, (ii) an external capacitor of 5 pF is attached to the output node. Plot the timing characteristics in a single graph with clearly labelled axes and legends for each value of S and for part (i) and (ii), and tabulate the rise time and fall time delays obtained. Find out the current drawn from the power supply in all cases as the input voltage is swept slowly w.r.t the output, and plot the current vs input voltage in a single graph with clear legends for each value of S and for part (i) and (ii). Calculate and tabulate the static and dynamic power dissipations in all cases, i.e., for each value of S and for part (i) and (ii).

Solution:

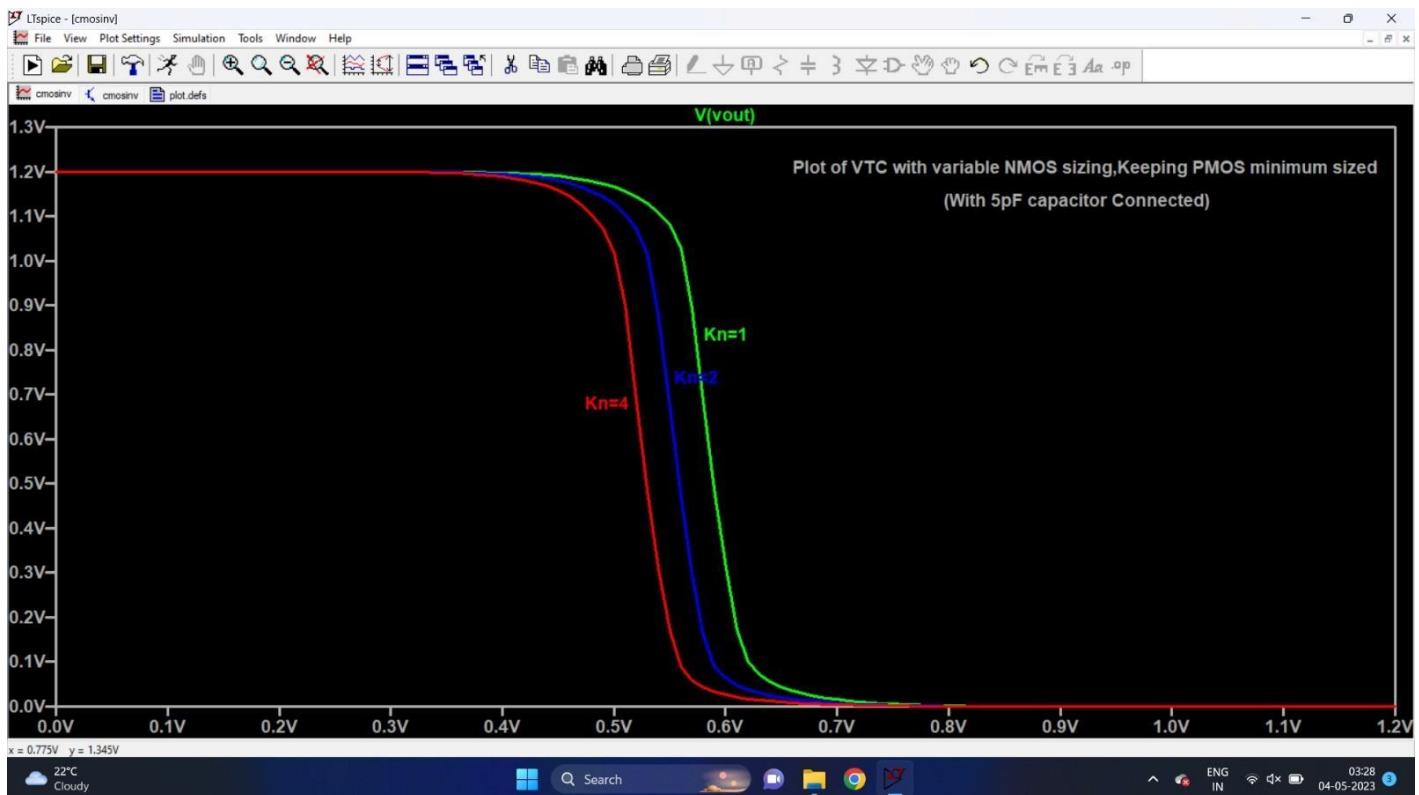
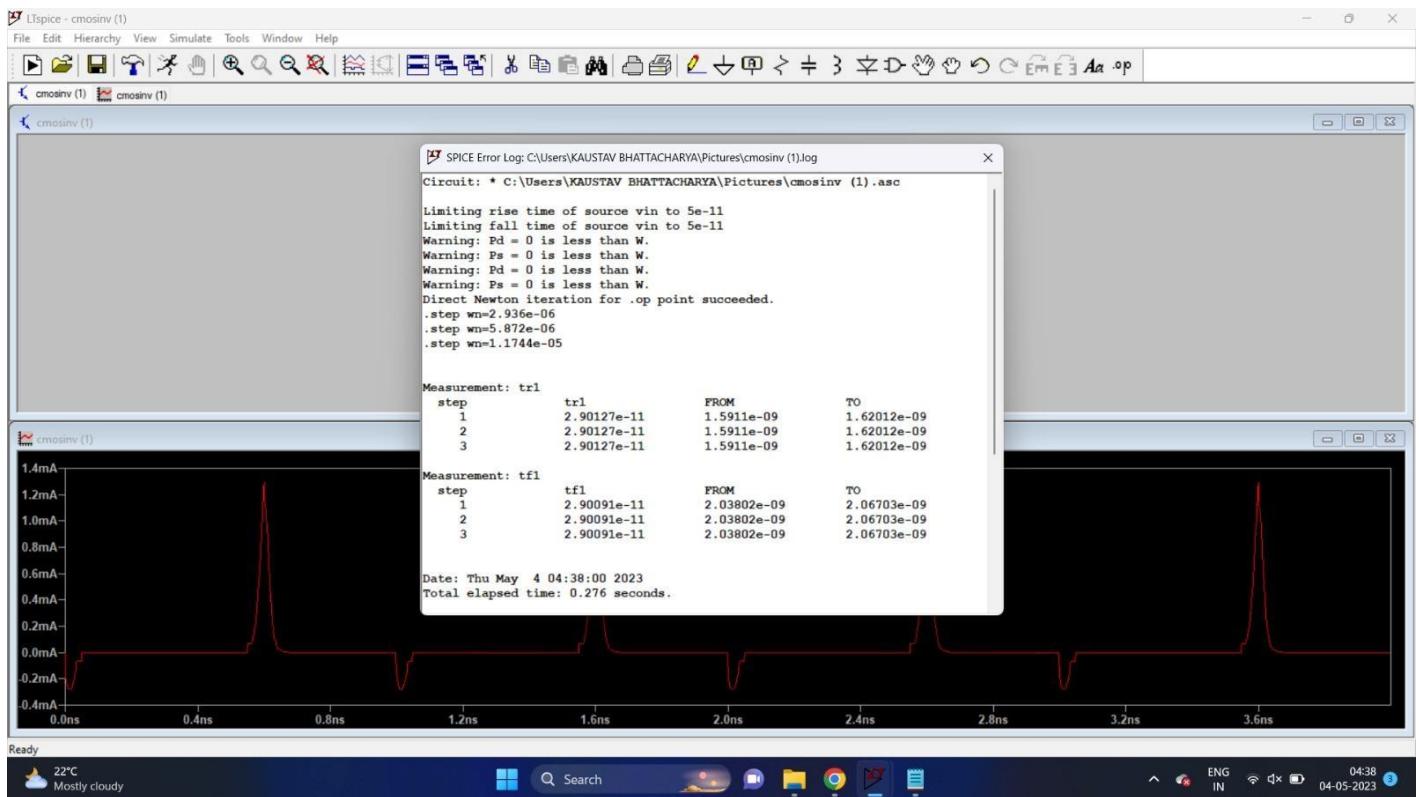
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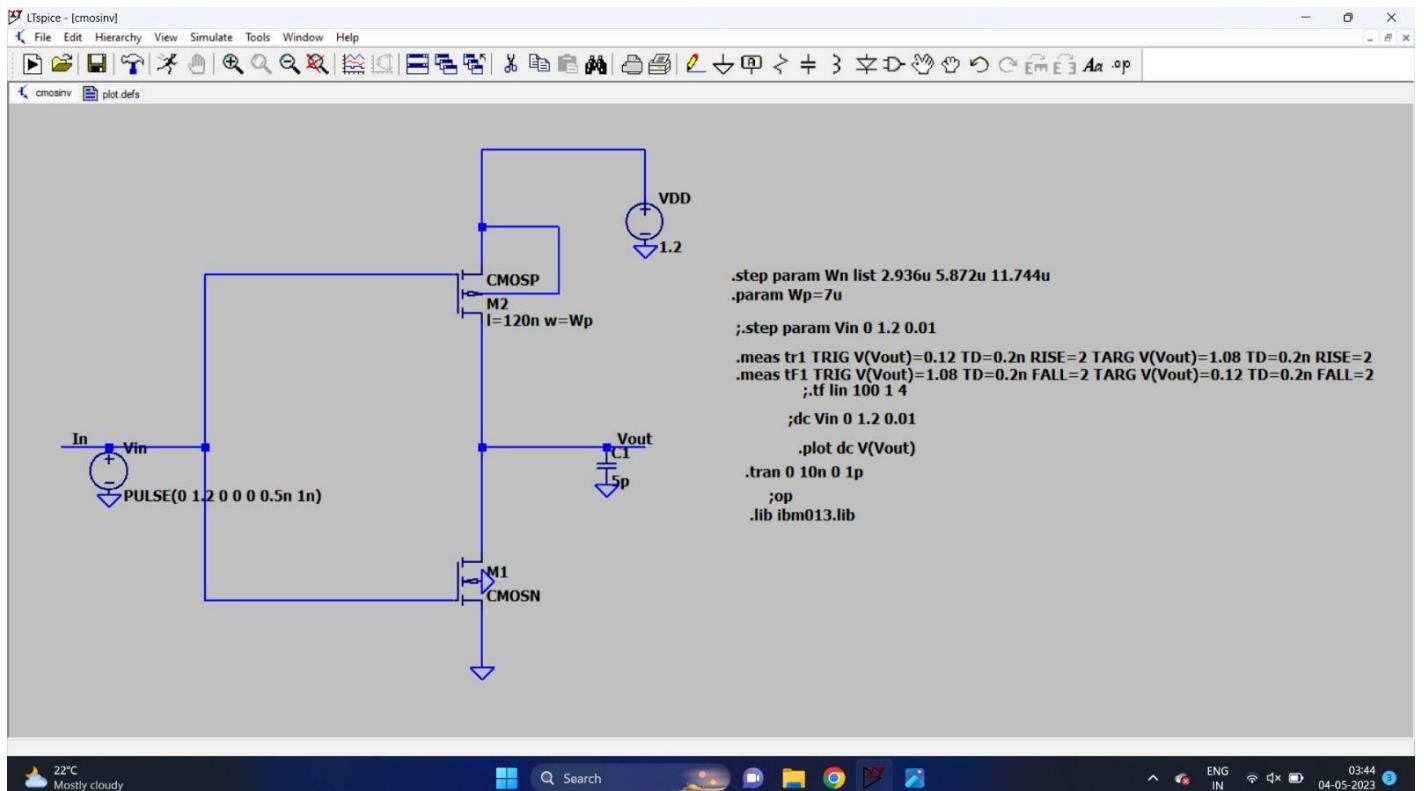
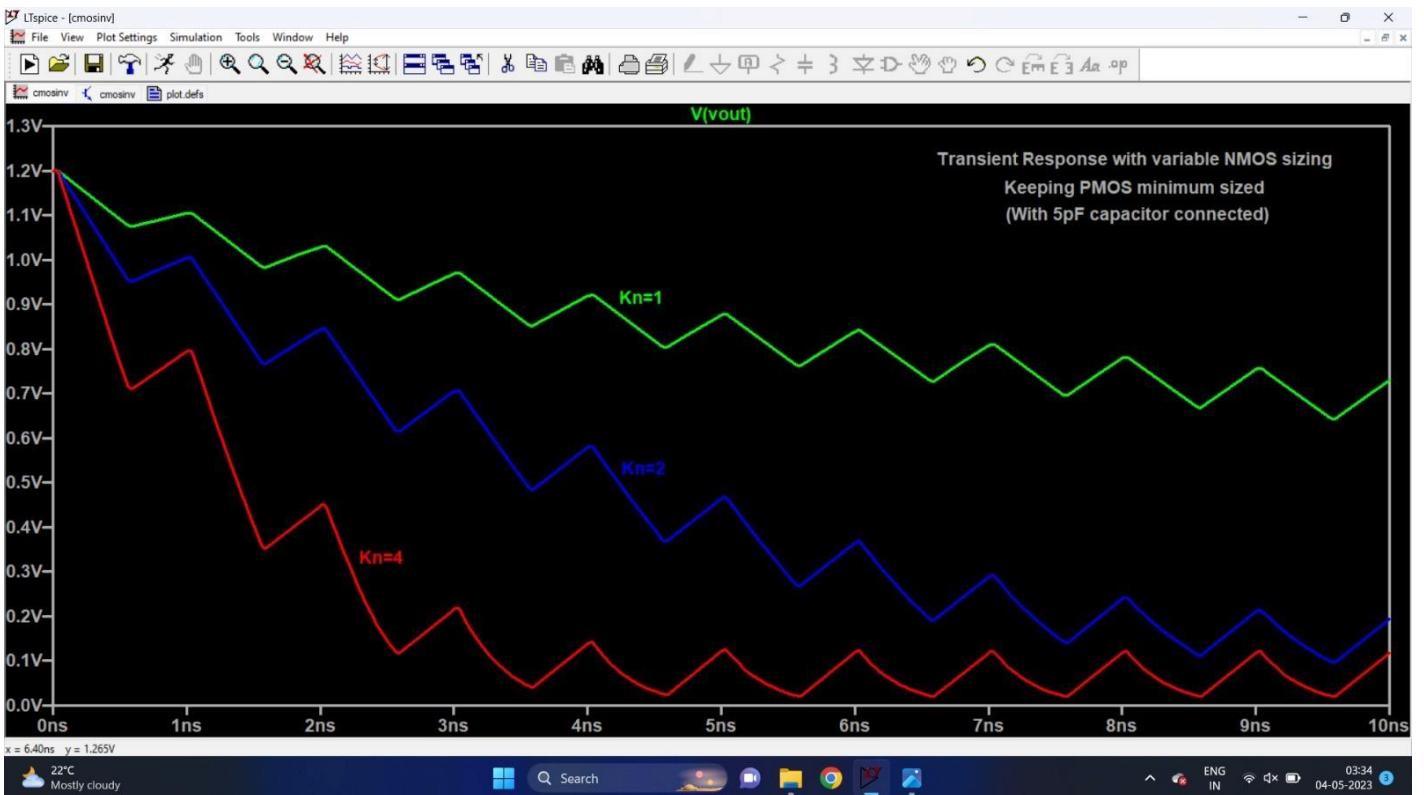
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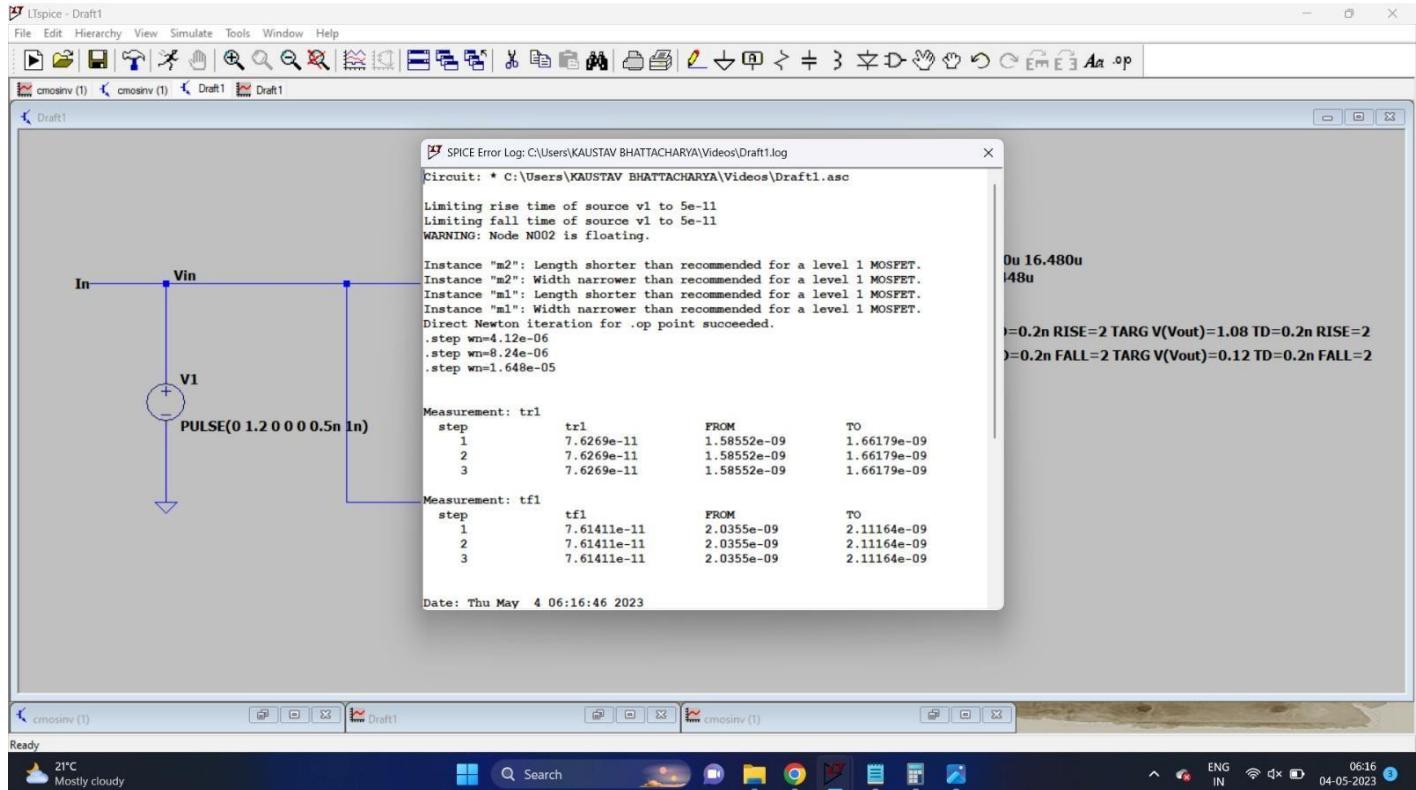
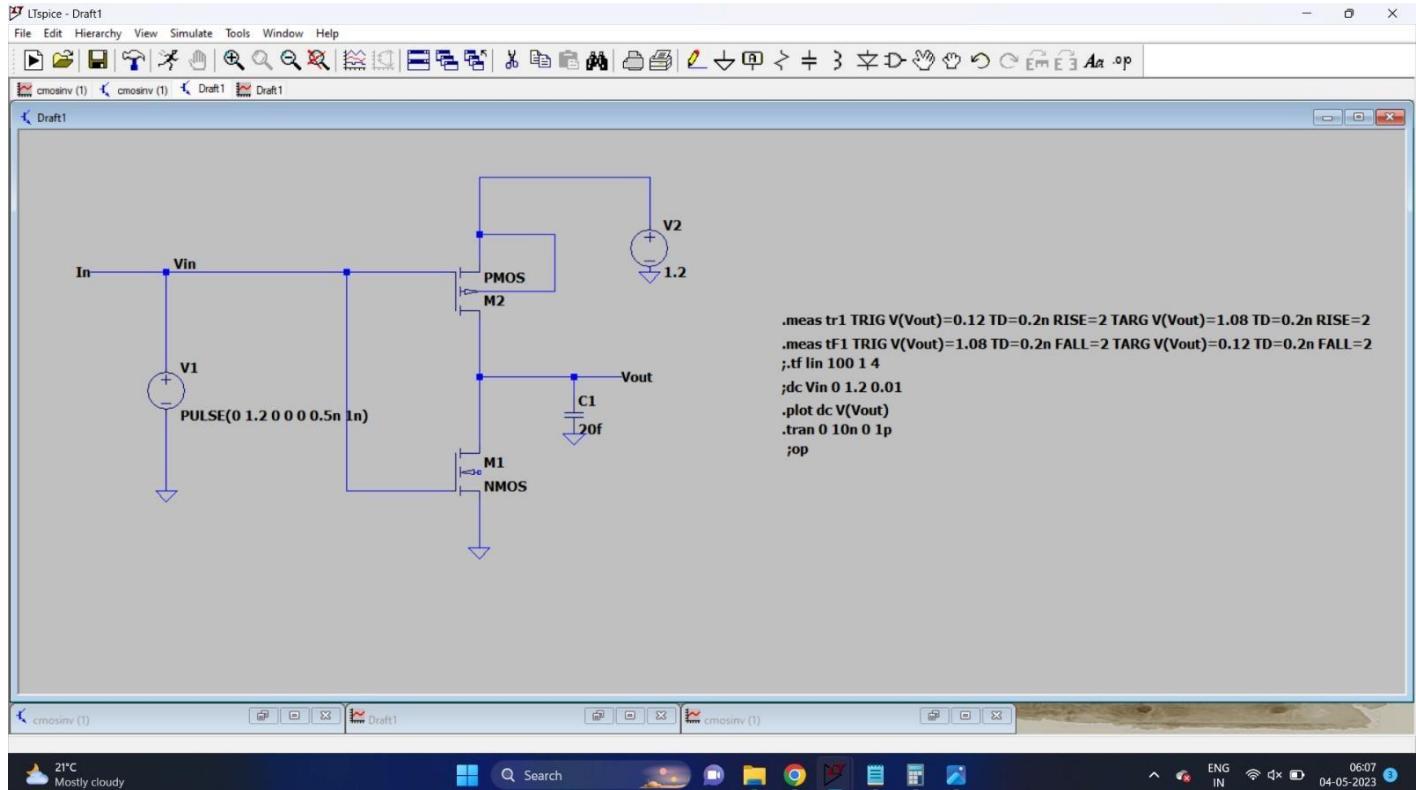
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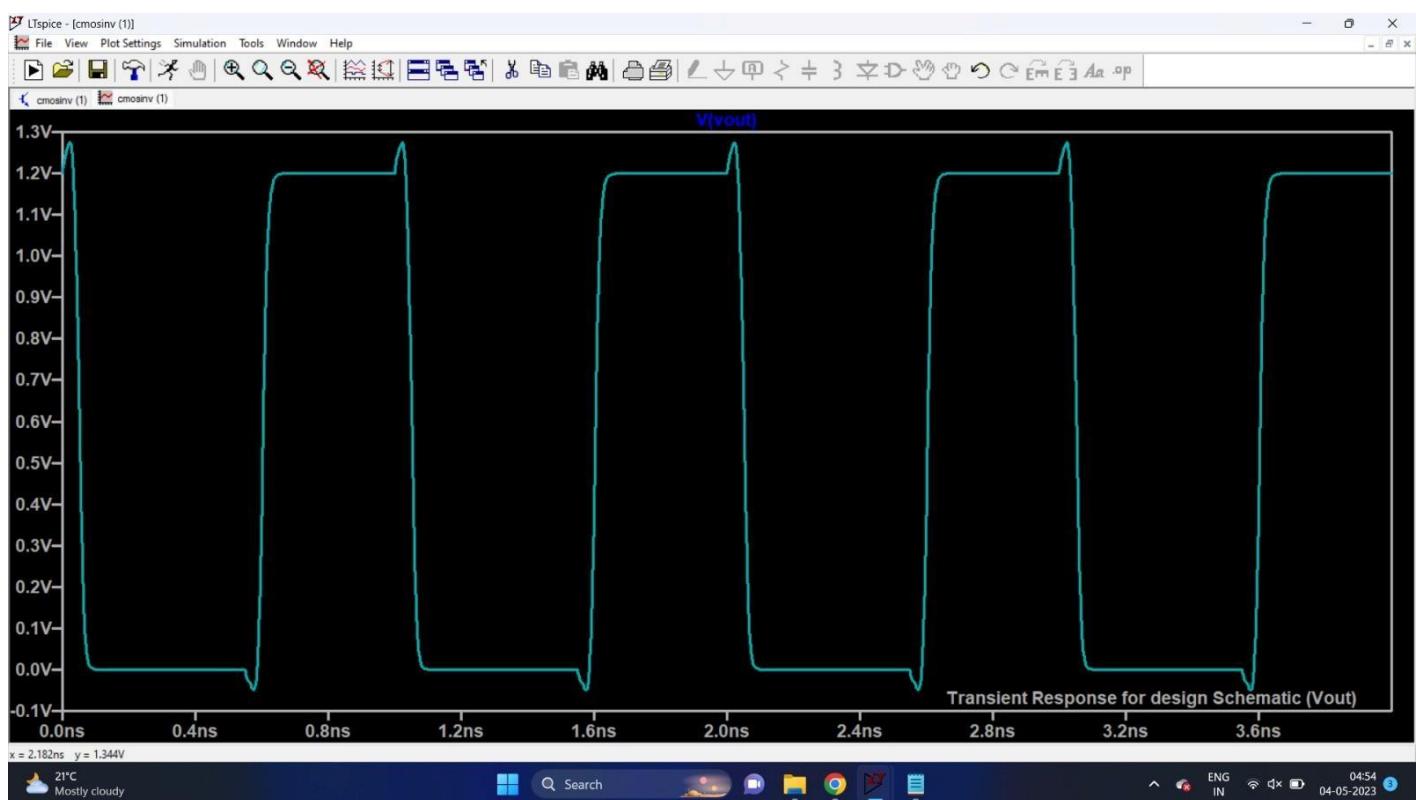
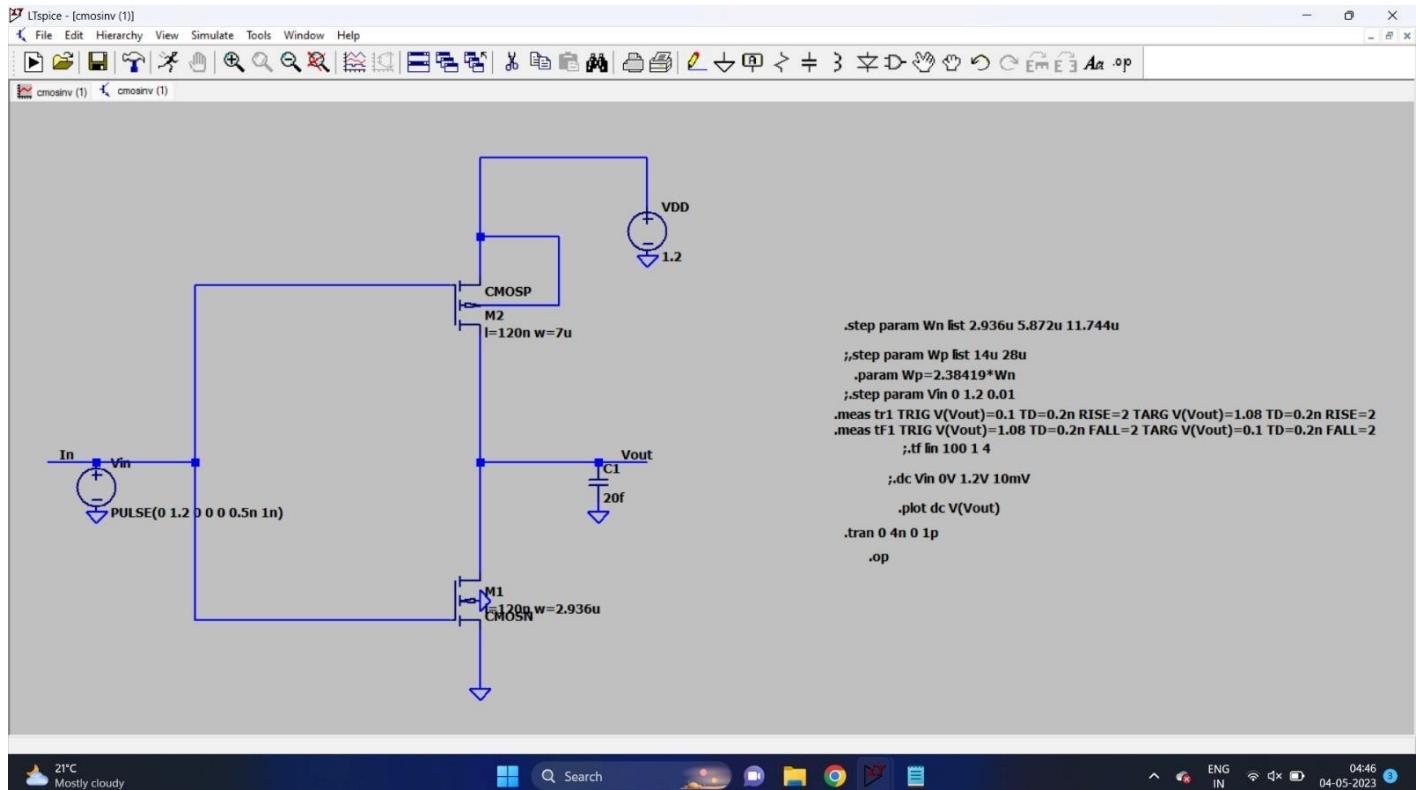
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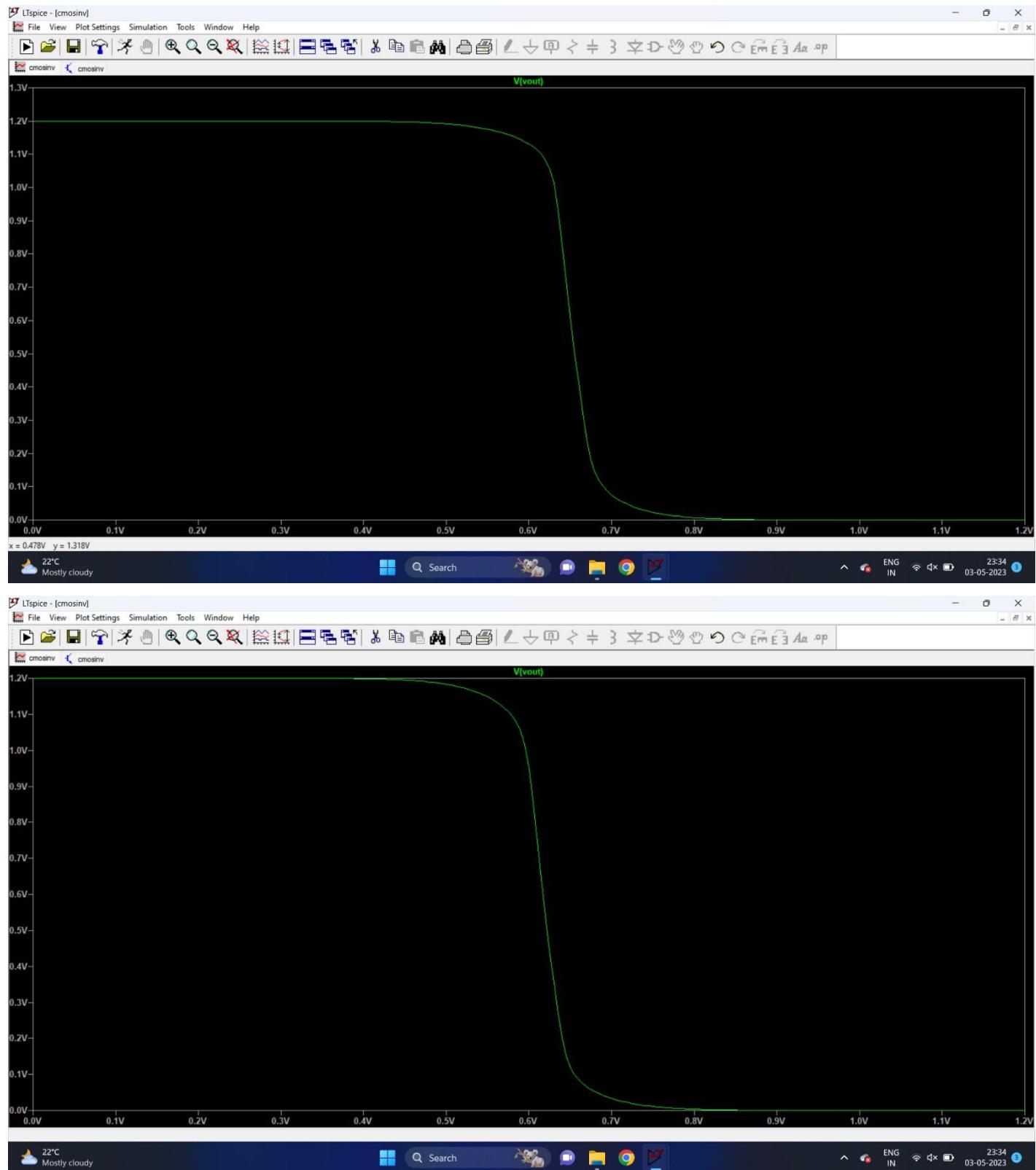
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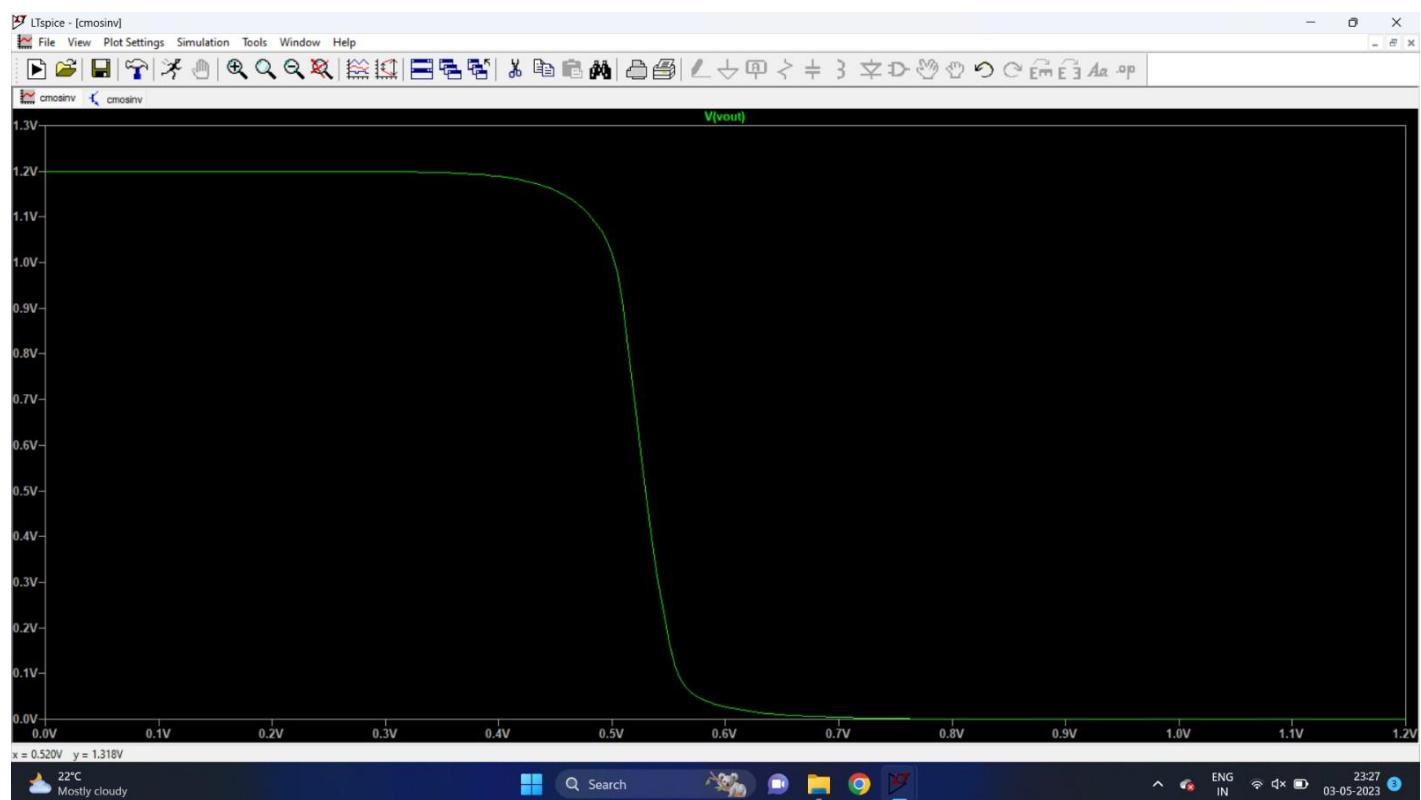
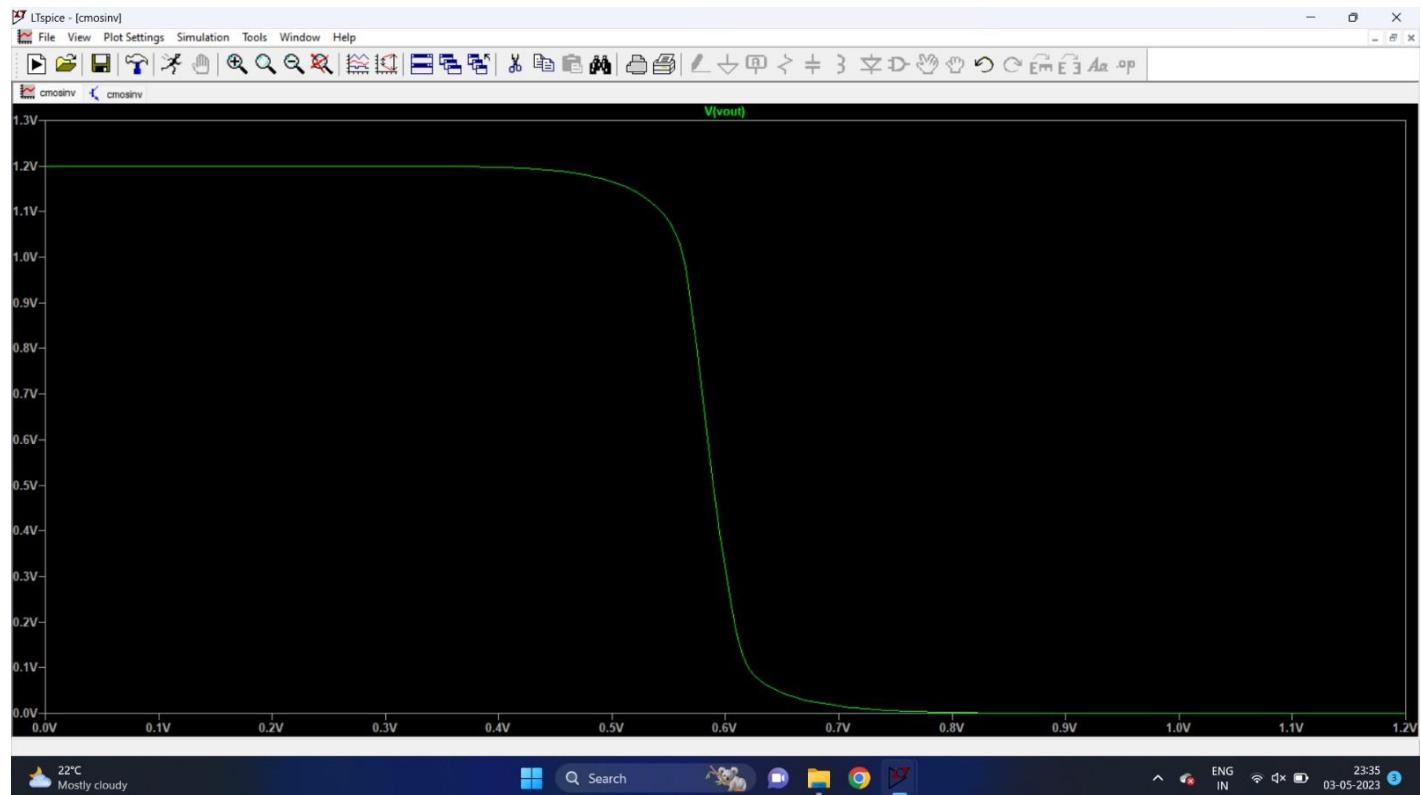
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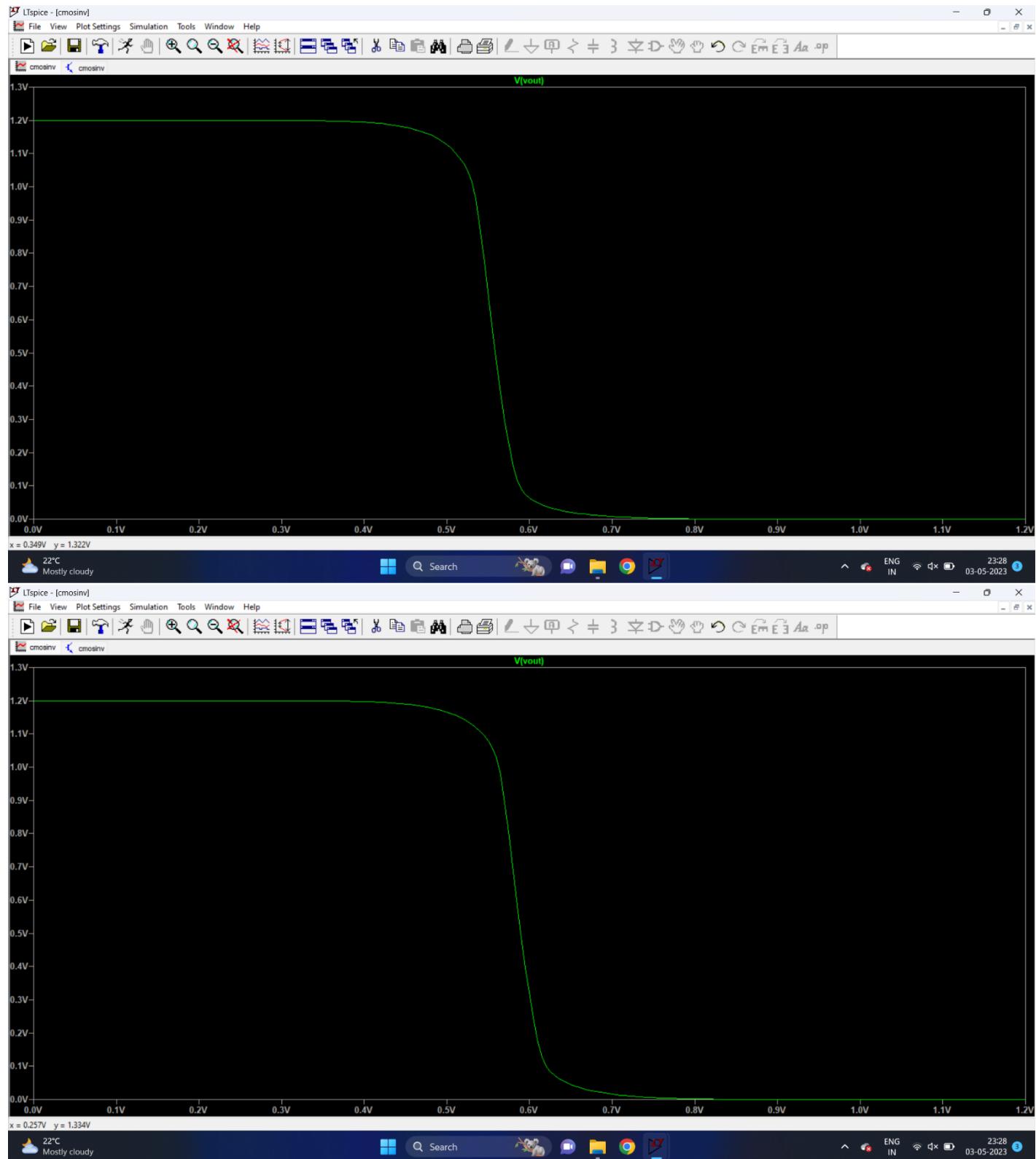
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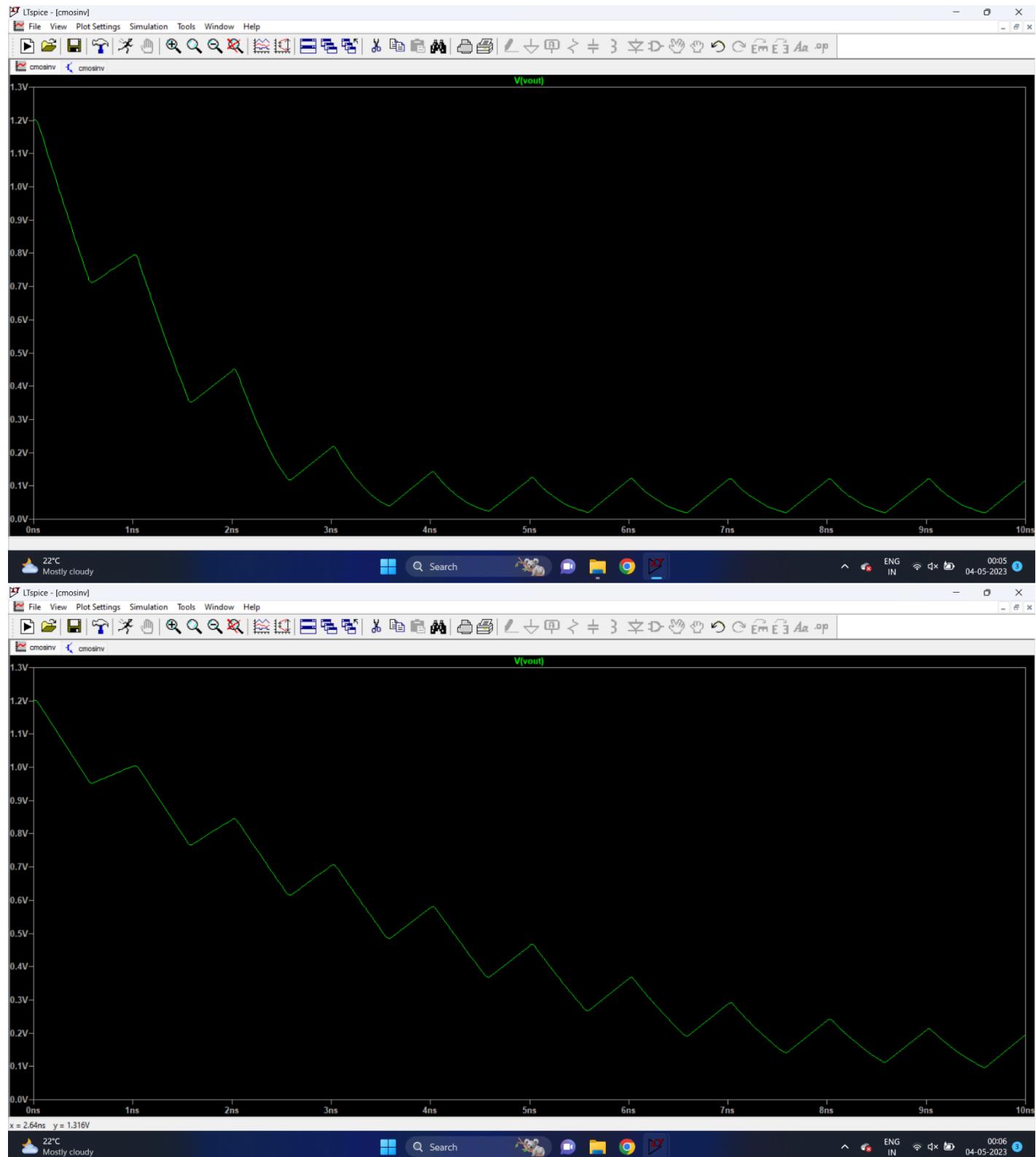
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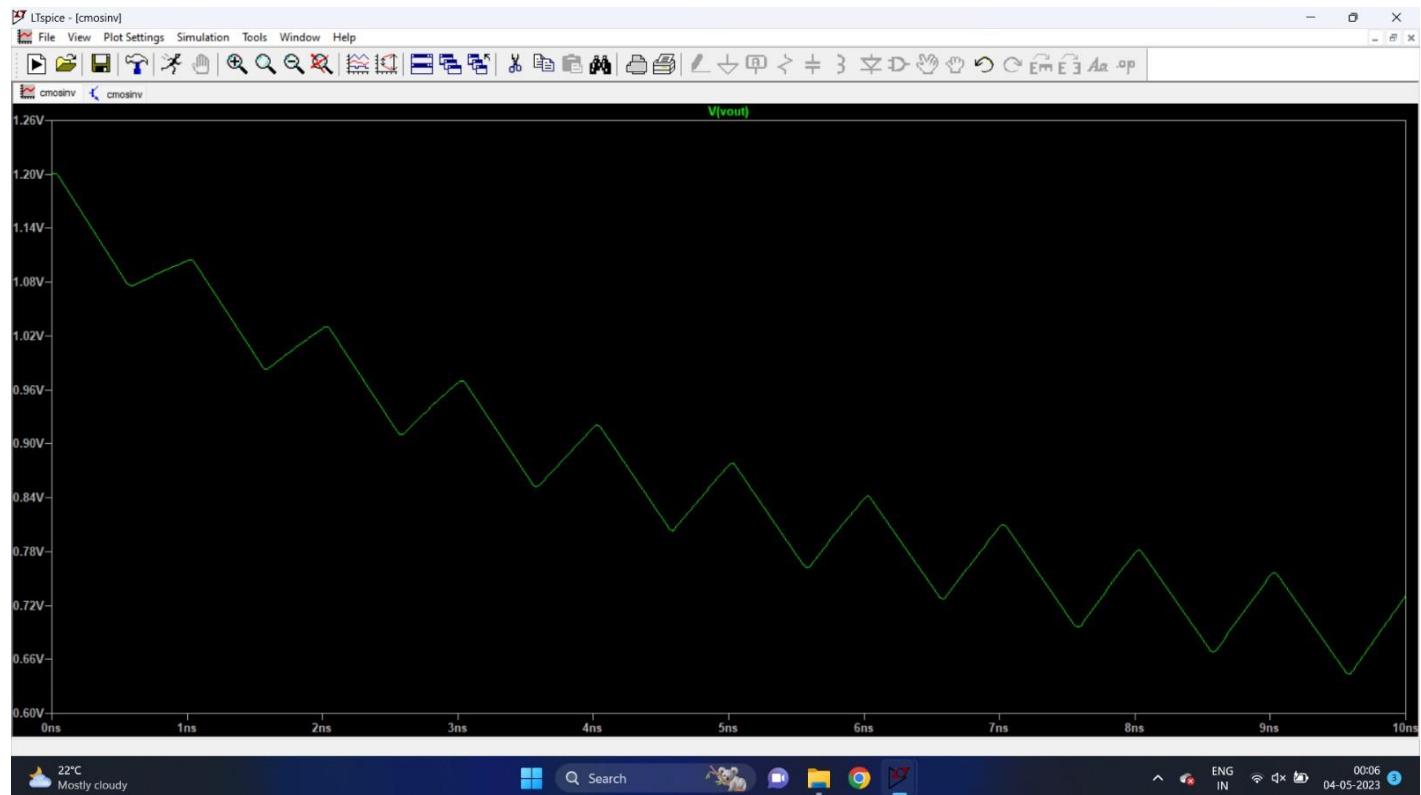
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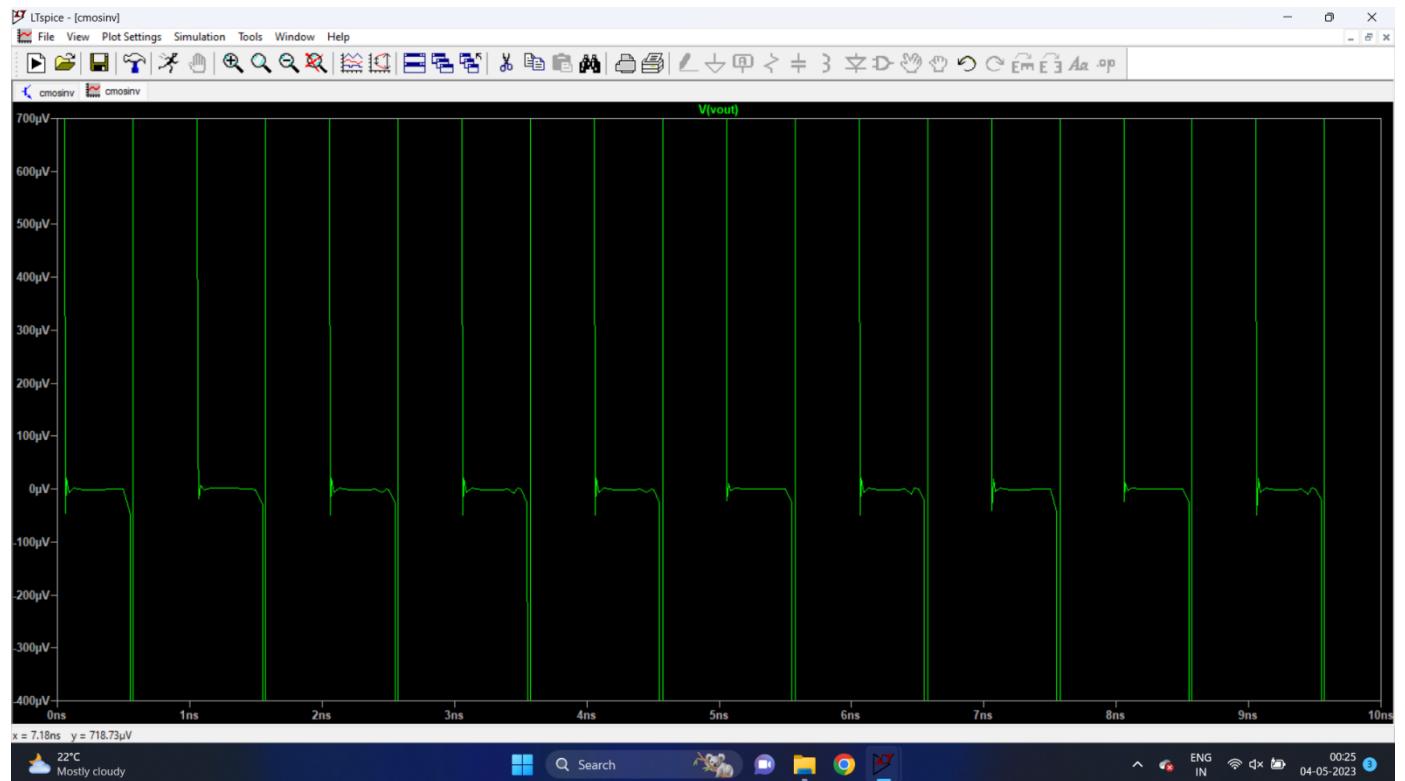
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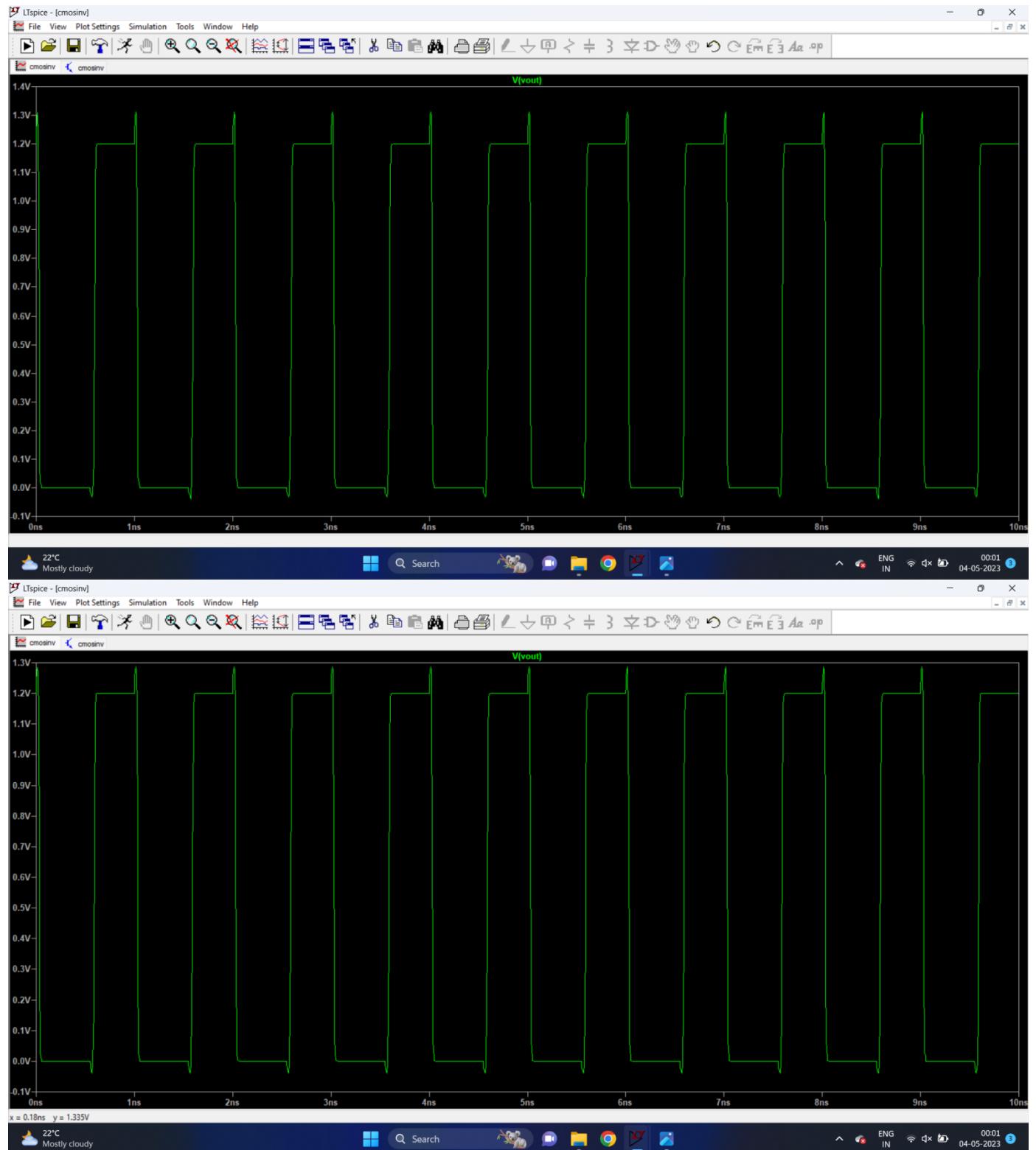
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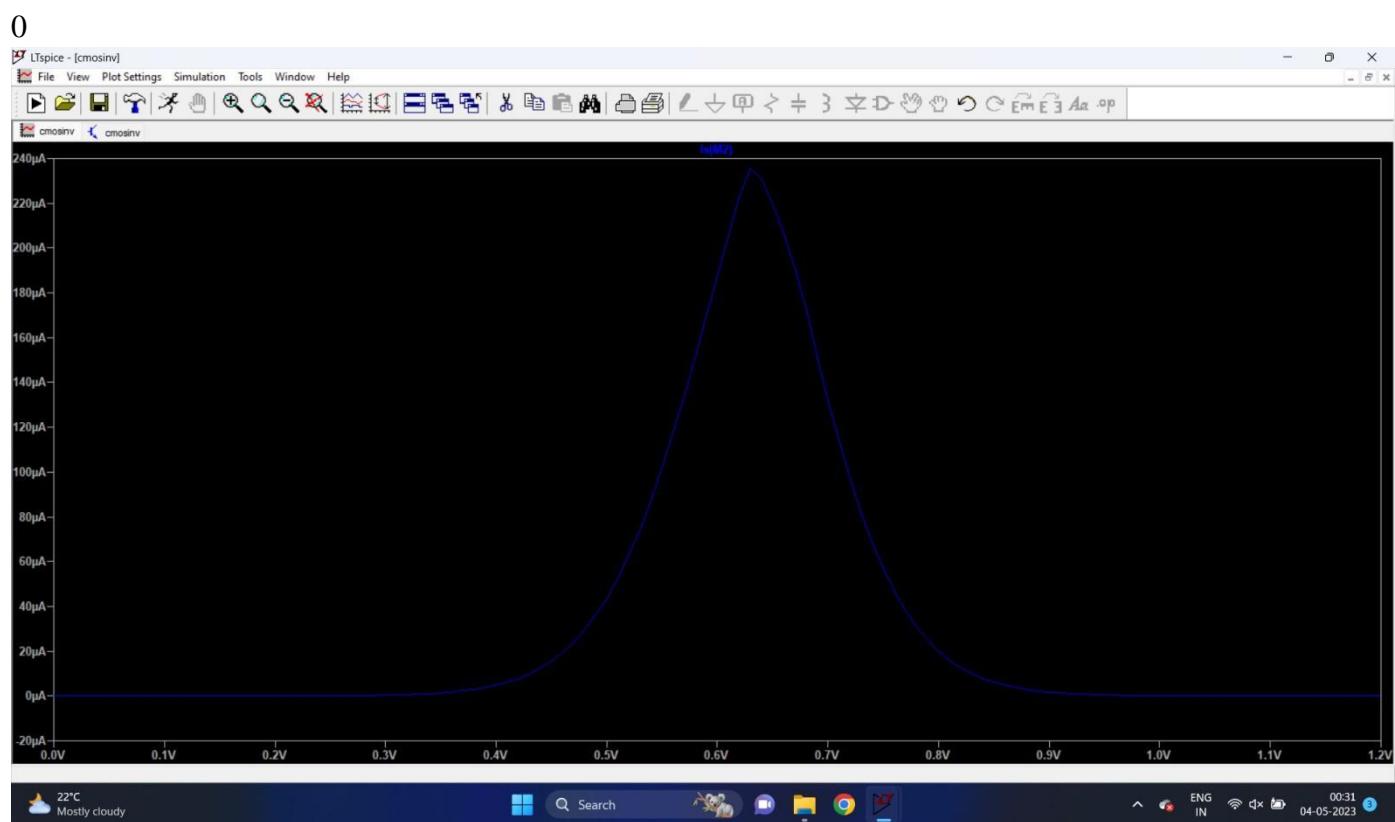
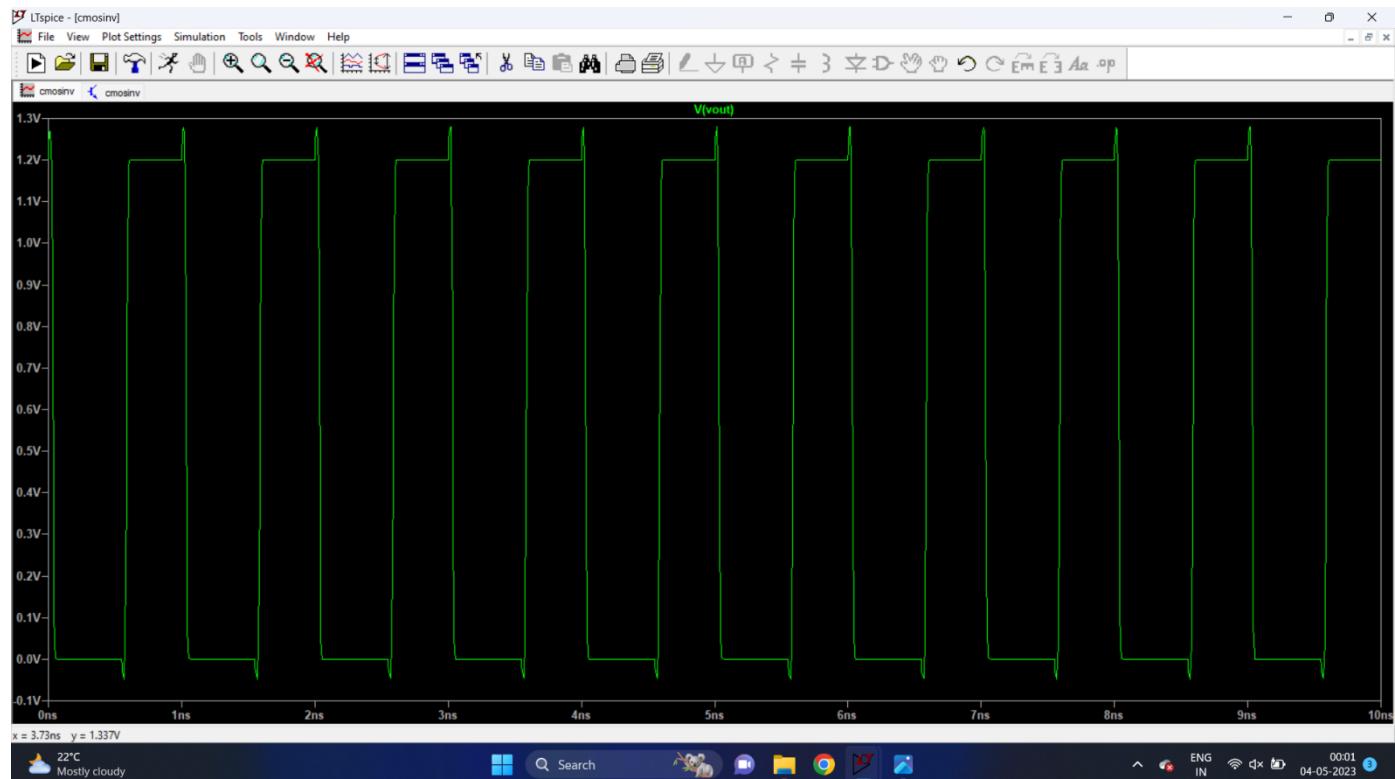
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